

MSP432 入门速成

m-RNA
2021/9

8-1 定时器A中断

参考资料

slau356h.pdf P783

msp432p401r.pdf P6

3 Device Comparison

Table 3-1 summarizes the features of the MSP432P401x microcontrollers.

Table 3-1. Device Comparison⁽¹⁾

DEVICE	FLASH (KB)	SRAM (KB)	Precision ADC (Channels)	COMP_E0 (Channels)	COMP_E1 (Channels)	Timer_A ⁽²⁾	eUSCI_A: UART, IrDA, SPI	eUSCI_B: SPI, I ² C	20-mA DRIVE I/O	TOTAL I/Os	PACKAGE
MSP432P401RIPZ	256	64	24 ext, 2 int	8	8	5, 5, 5, 5	4	4	4	84	100 PZ
MSP432P401MIPZ	128	32	24 ext, 2 int	8	8	5, 5, 5, 5	4	4	4	84	100 PZ
MSP432P401RIZXH	256	64	16 ext, 2 int	6	8	5, 5, 5	3	4	4	64	80 ZXH
MSP432P401MIZXH	128	32	16 ext, 2 int	6	8	5, 5, 5	3	4	4	64	80 ZXH
MSP432P401RIRGC	256	64	12 ext, 2 int	2	4	5, 5, 5	3	3	4	48	64 RGC
MSP432P401MIRGC	128	32	12 ext, 2 int	2	4	5, 5, 5	3	3	4	48	64 RGC

19.1 Timer_A Introduction

Timer_A is a 16-bit timer/counter with up to seven capture/compare registers. Timer_A can support multiple capture/compares, PWM outputs, and interval timing. Timer_A also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

Timer_A features include:

- Asynchronous 16-bit timer/counter with four operating modes
- Selectable and configurable clock source
- Up to seven configurable capture/compare registers
- Configurable outputs with pulse width modulation (PWM) capability
- Asynchronous input and output latching

Timer_A的特性包括:

- ◇具有4种操作模式的异步16位定时/计数器;
- ◇可选择和可配置的时钟源;
- ◇最多达7个可配置的捕获/比较模块;
- ◇具有PWM 功能的可配置输出;
- ◇异步输入和输出锁存。

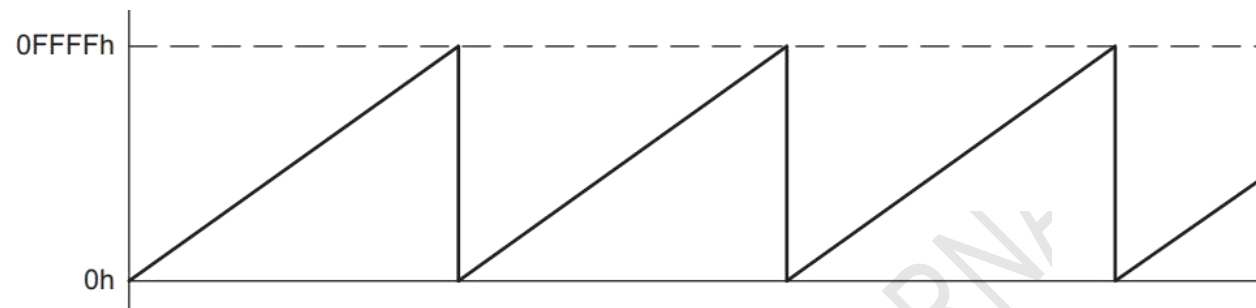


Figure 19-4. Continuous Mode

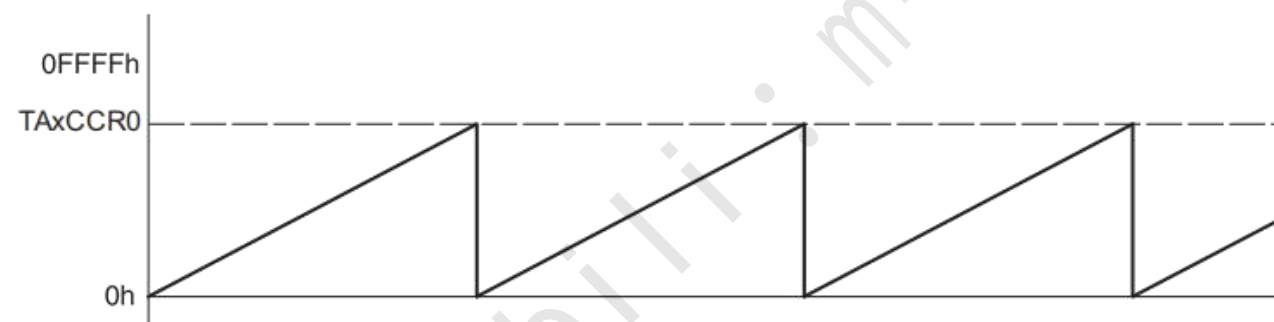


Figure 19-2. Up Mode

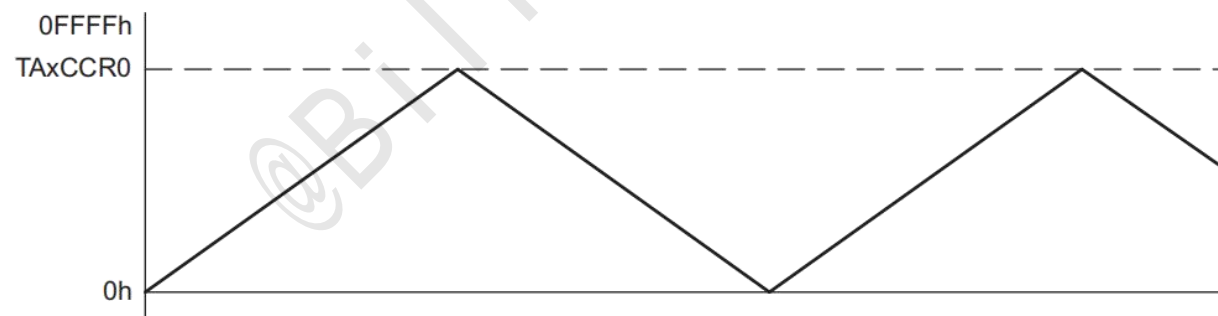


Figure 19-7. Up/Down Mode

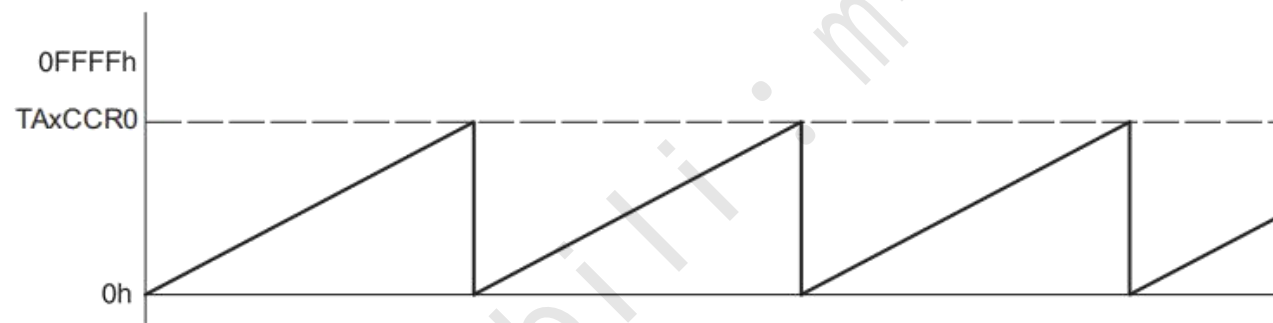


Figure 19-2. Up Mode

timer_a.h

1 初始化定时器模块

```
Timer_A_configureUpMode(TIMER_Ax_BASE, &upConfig);
```

2 选择模式开始计数

```
Timer_A_startCounter(TIMER_Ax_BASE, TIMER_A_UP_MODE);
```

3 清除比较中断标志

```
Timer_A_clearCaptureCompareInterrupt(TIMER_Ax, REGISTER_0);
```

interrupt.h

4 开启定时器 A 端口中断

`Interrupt_enableInterrupt(INT_TAx_0);`

5 开启总中断

`Interrupt_enableMaster(void);`

一般配置步骤

- 0.配置时钟
- 1.配置结构体
- 2.初始化定时器A
- 3.选择模式开始计数
- 4.清除比较中断标志位
- 5.开启定时器端口中断
- 6.开启总中断
- 7.编写TIMA ISR

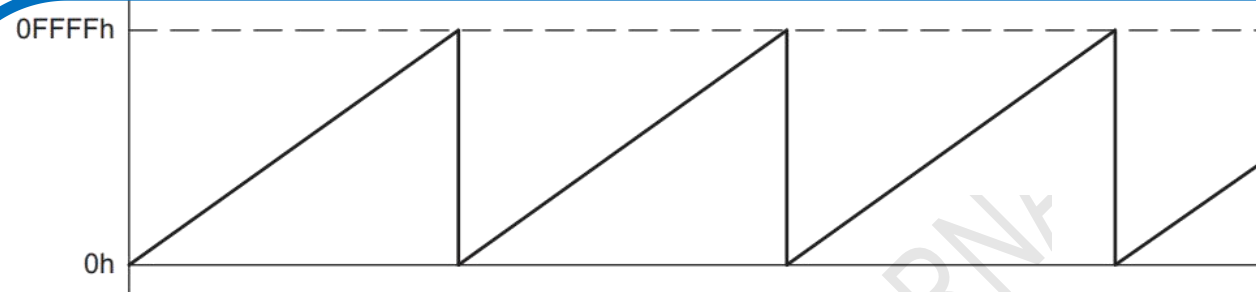


Figure 19-4. Continuous Mode

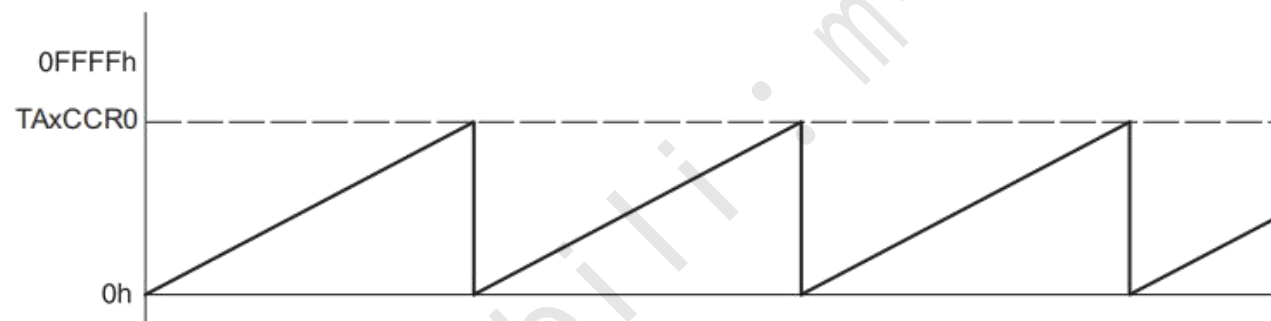


Figure 19-2. Up Mode

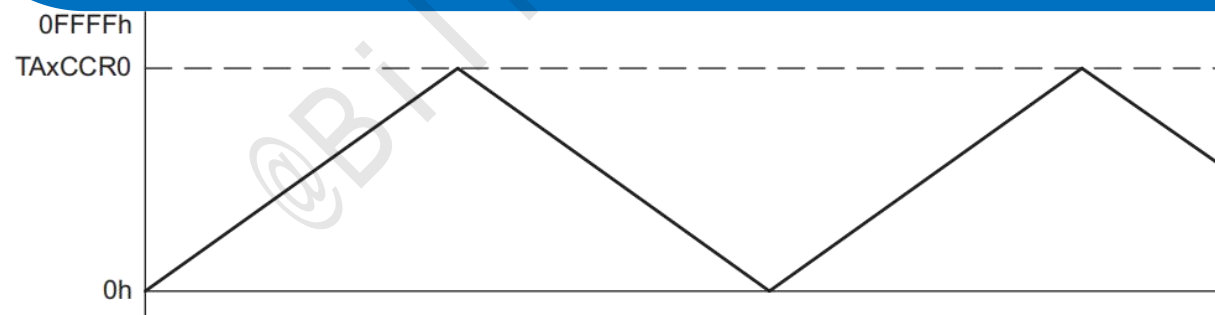


Figure 19-7. Up/Down Mode

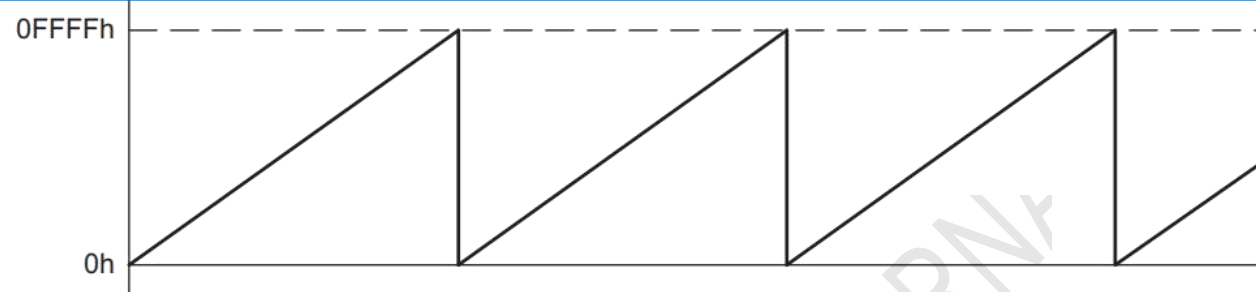


Figure 19-4. Continuous Mode

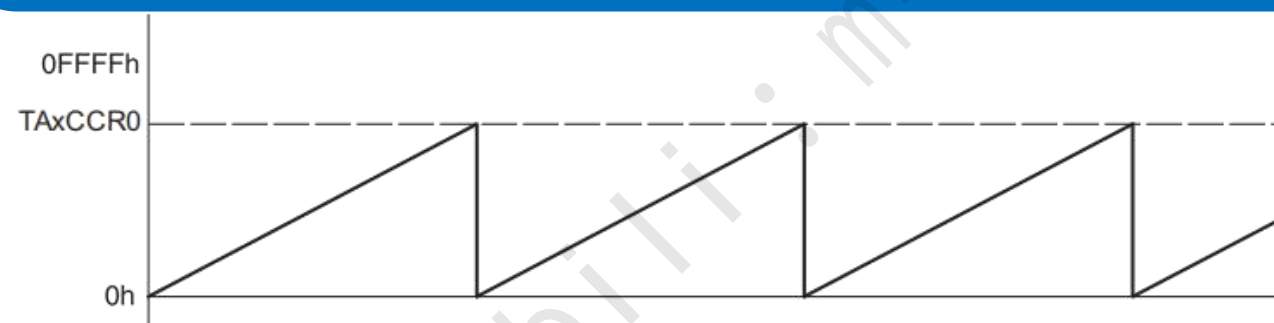


Figure 19-2. Up Mode

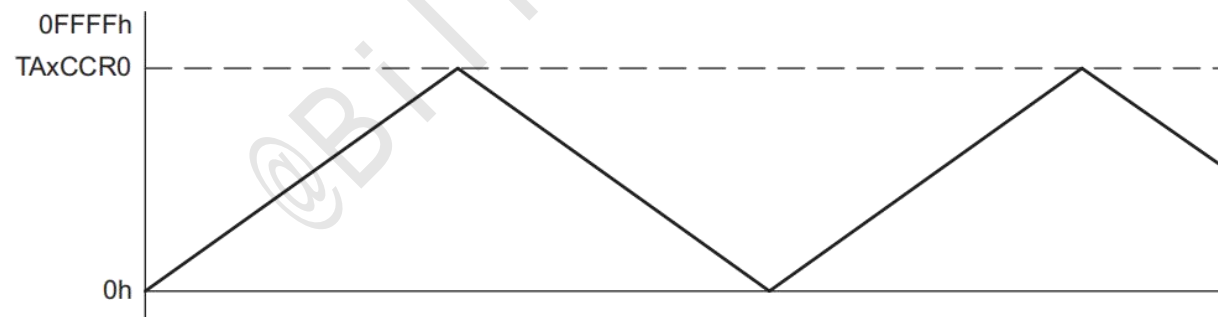


Figure 19-7. Up/Down Mode

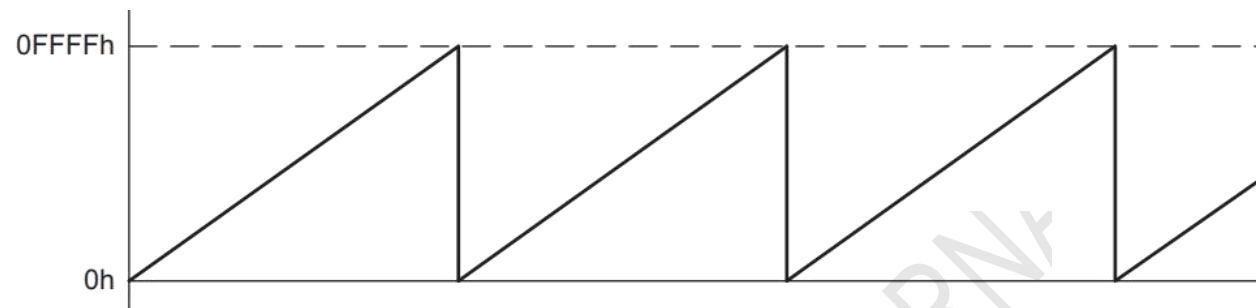


Figure 19-4. Continuous Mode

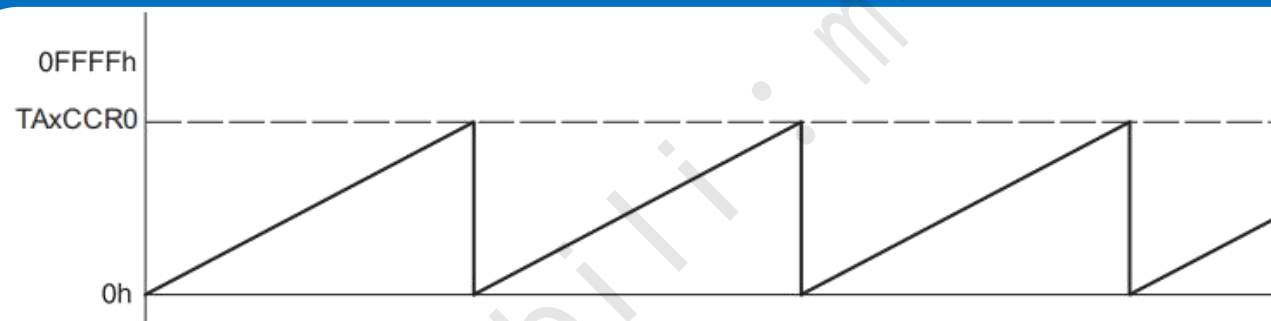


Figure 19-2. Up Mode

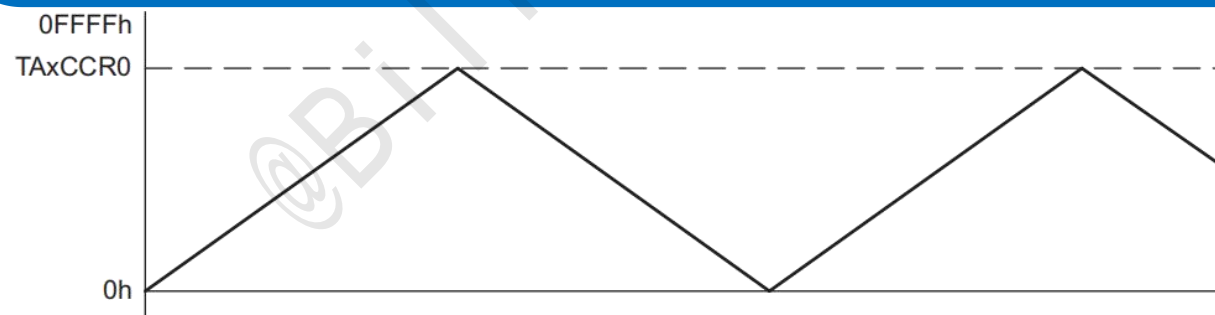


Figure 19-7. Up/Down Mode

TIMER_A -> INT/PWM

$$T_{timer_a} = \frac{ClkDiv \times (CCR0 + 1)}{f_{clk}}$$

CLKDIV \in [1, 8] \cup {10, 12, 14, 16, 20, 24, 28, 32, 40, 48, 56, 64 };

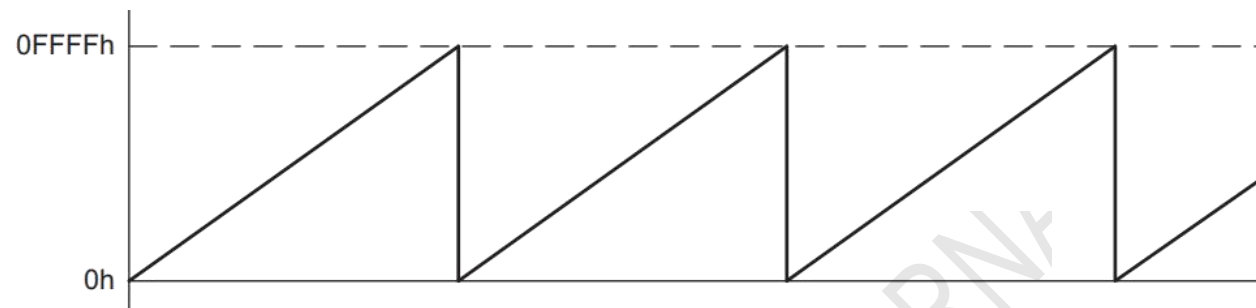


Figure 19-4. Continuous Mode

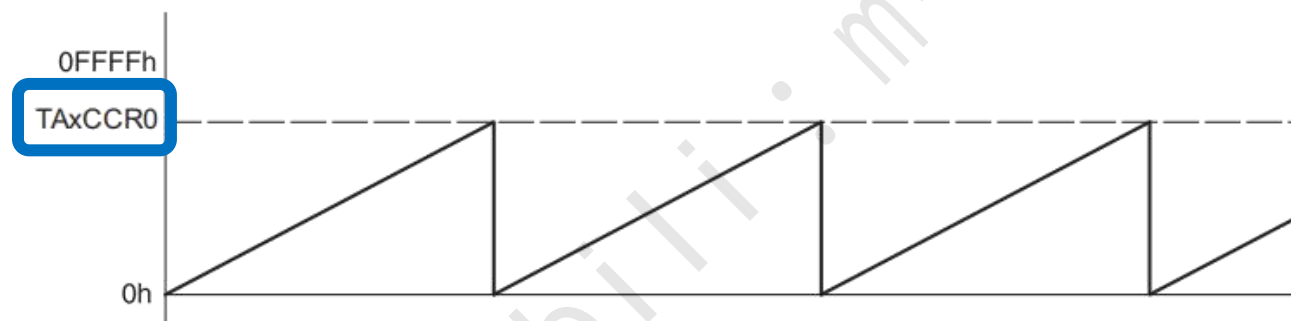


Figure 19-2. Up Mode

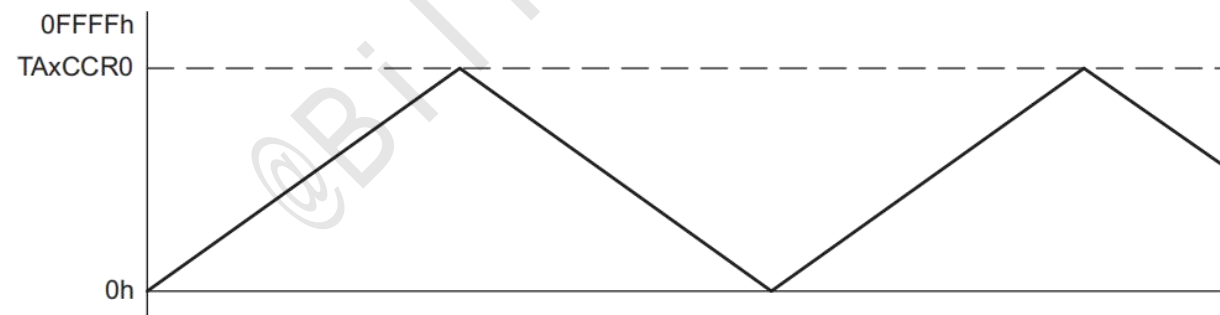


Figure 19-7. Up/Down Mode

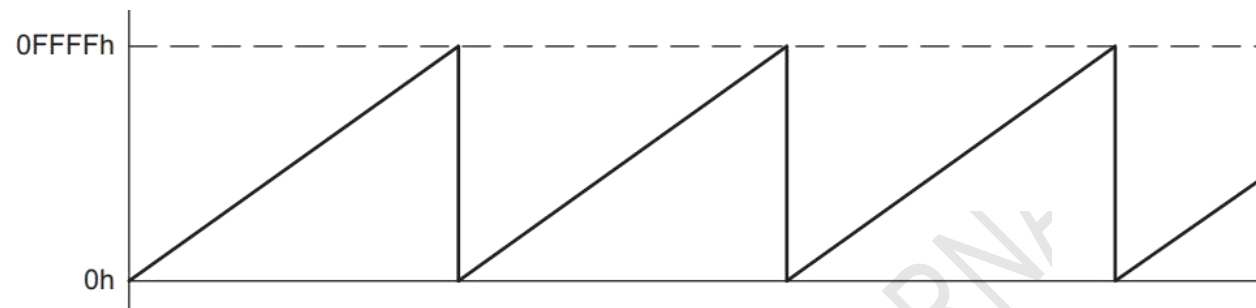


Figure 19-4. Continuous Mode

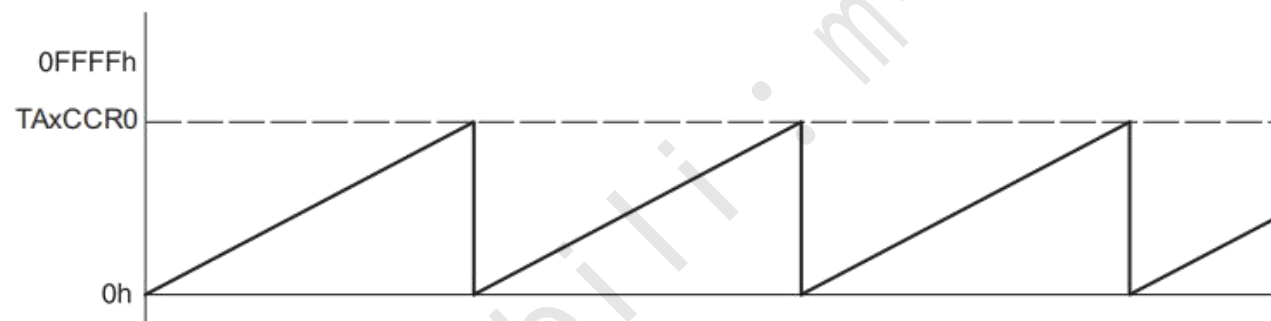


Figure 19-2. Up Mode

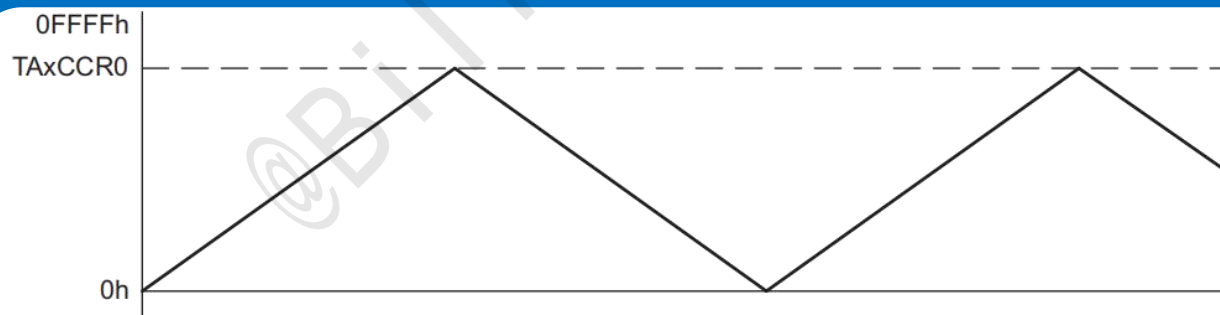


Figure 19-7. Up/Down Mode

8-2 定时器A PWM

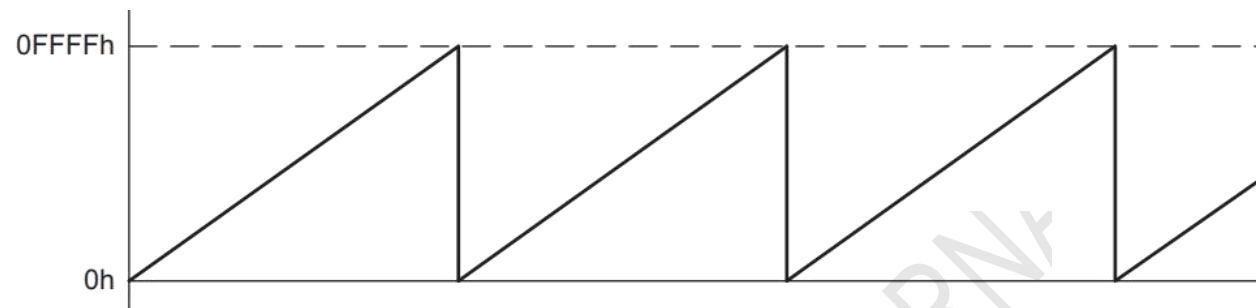


Figure 19-4. Continuous Mode

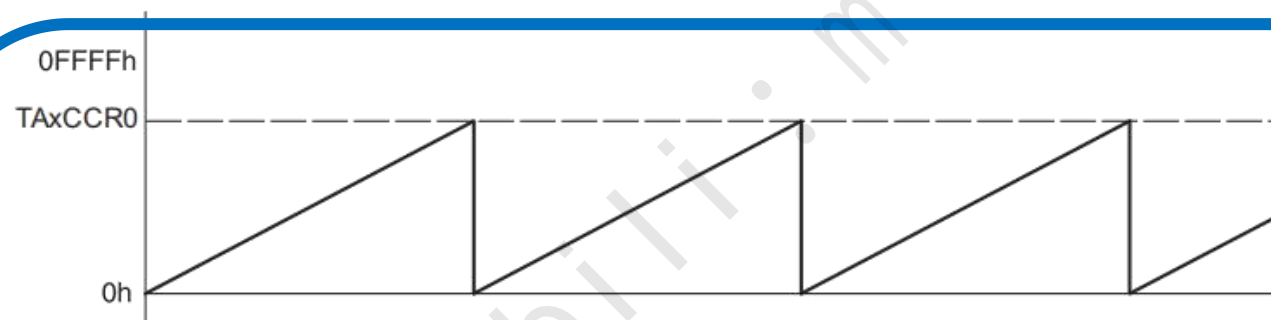


Figure 19-2. Up Mode

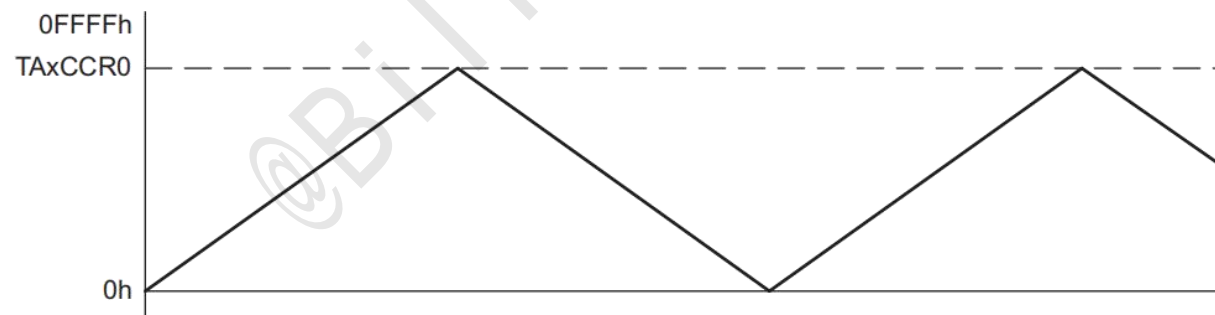


Figure 19-7. Up/Down Mode

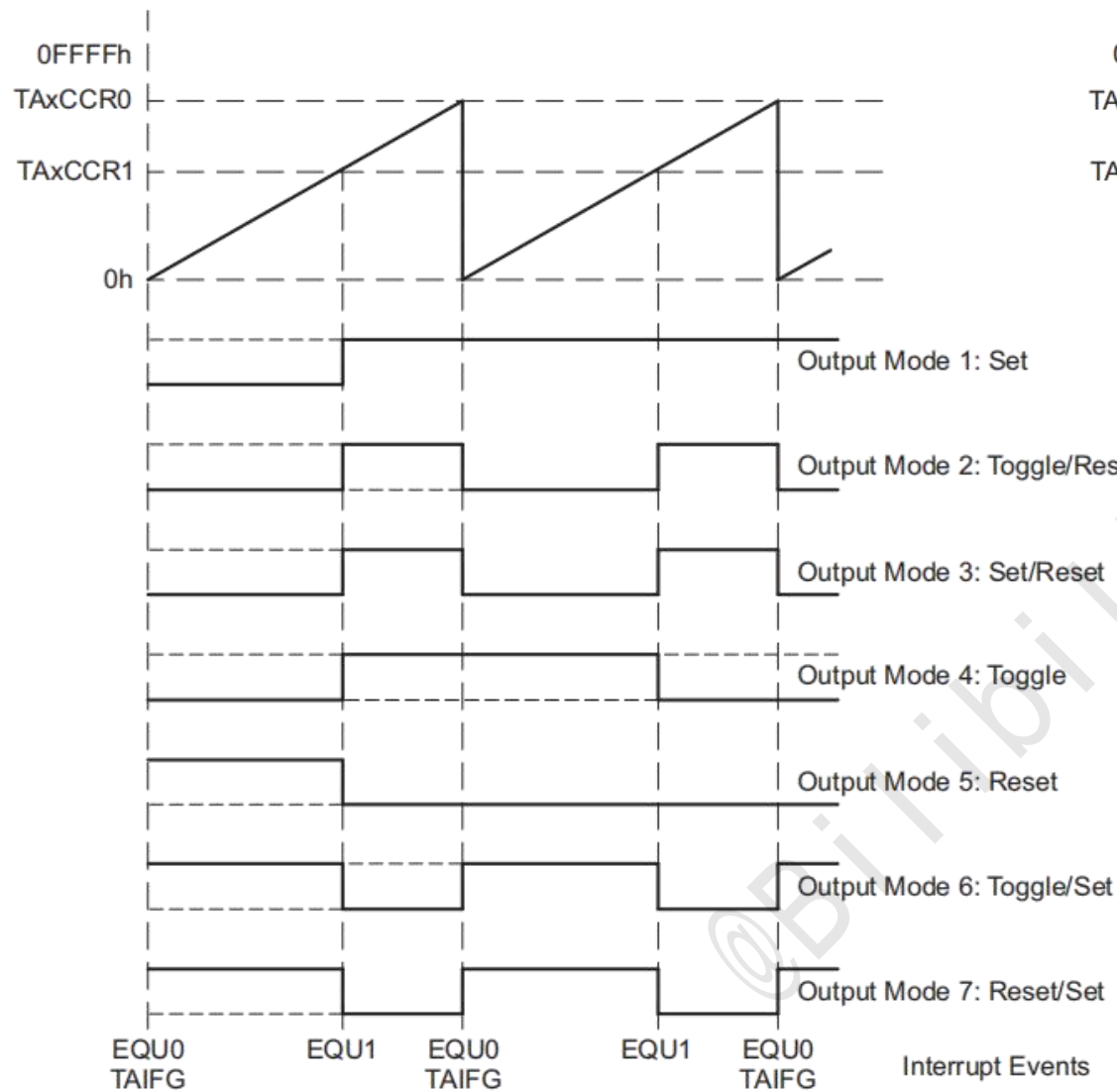


Figure 19-12. Output Example – Timer in Up Mode

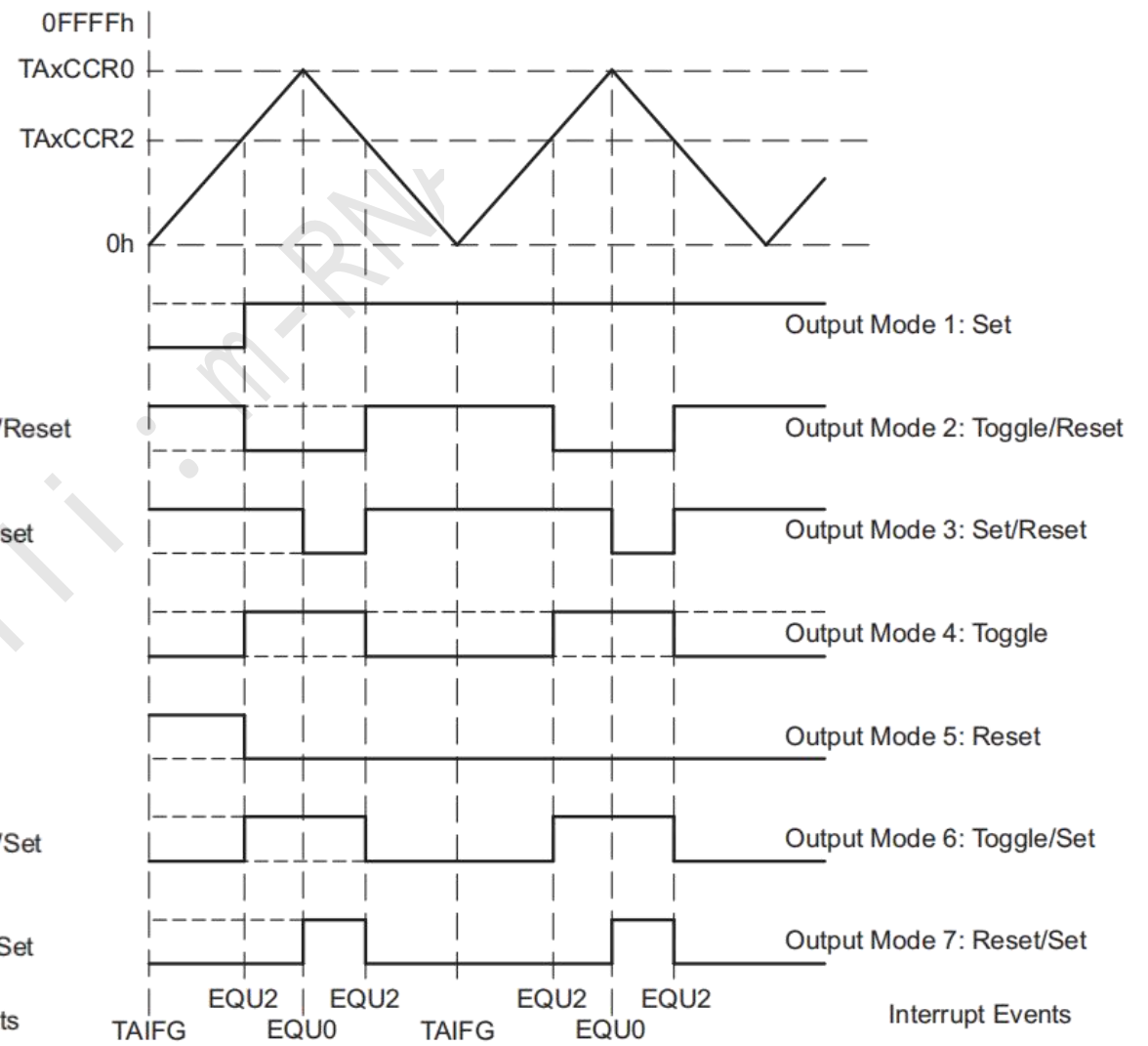
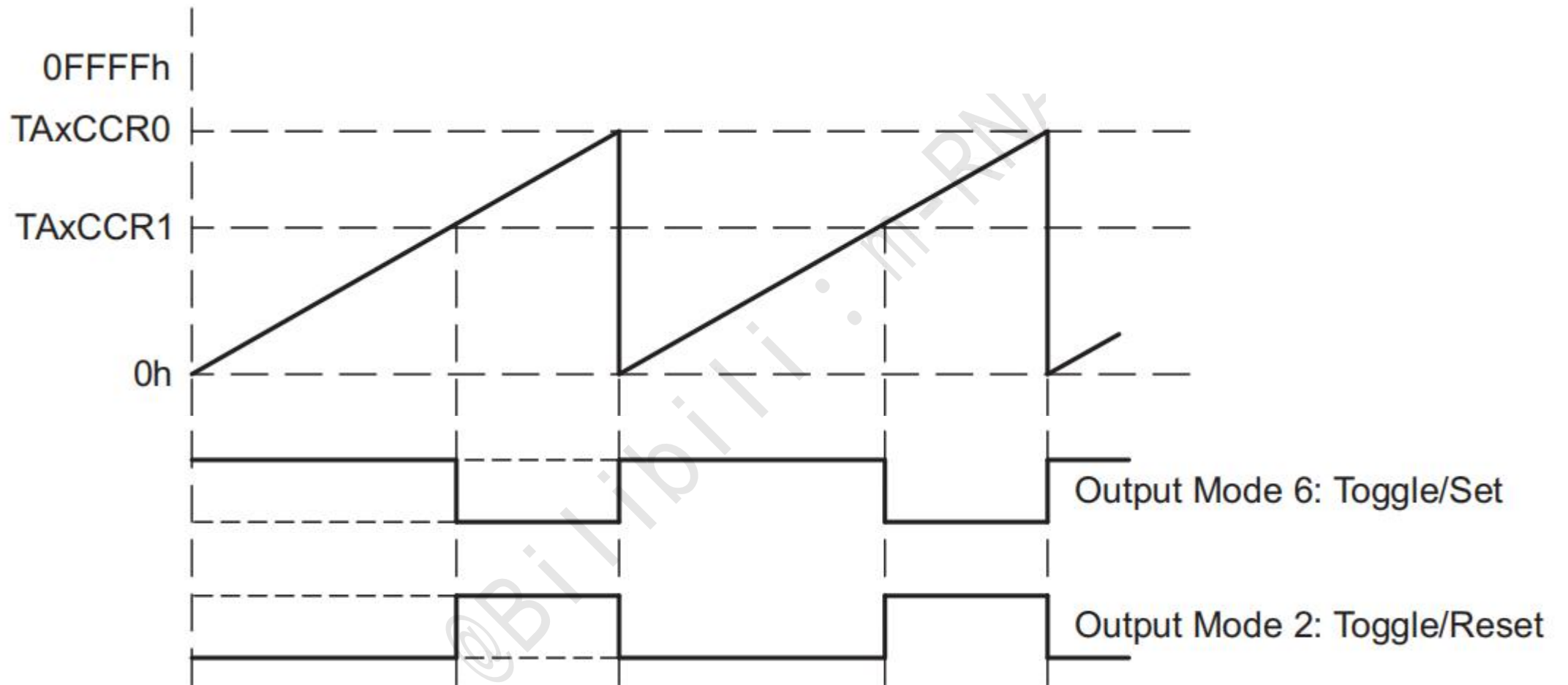
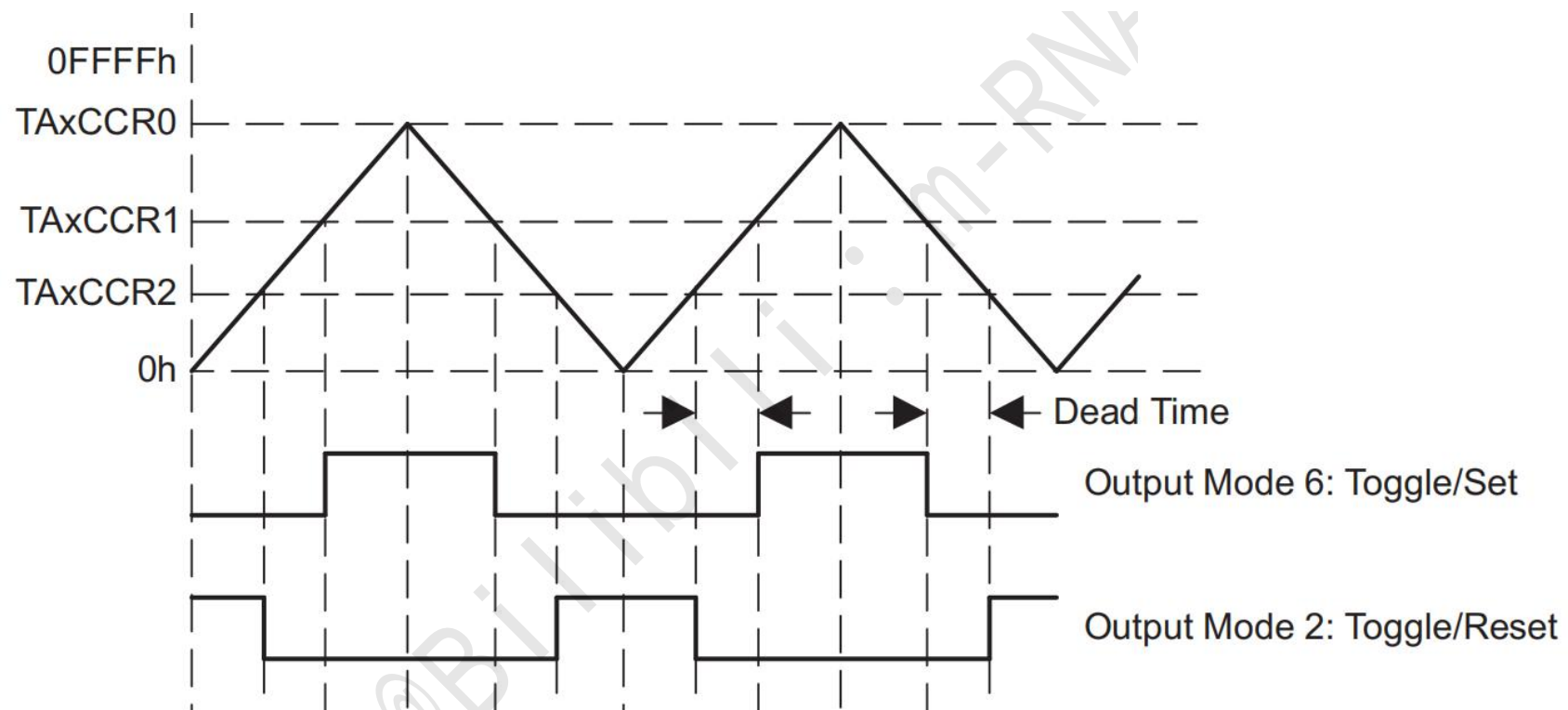
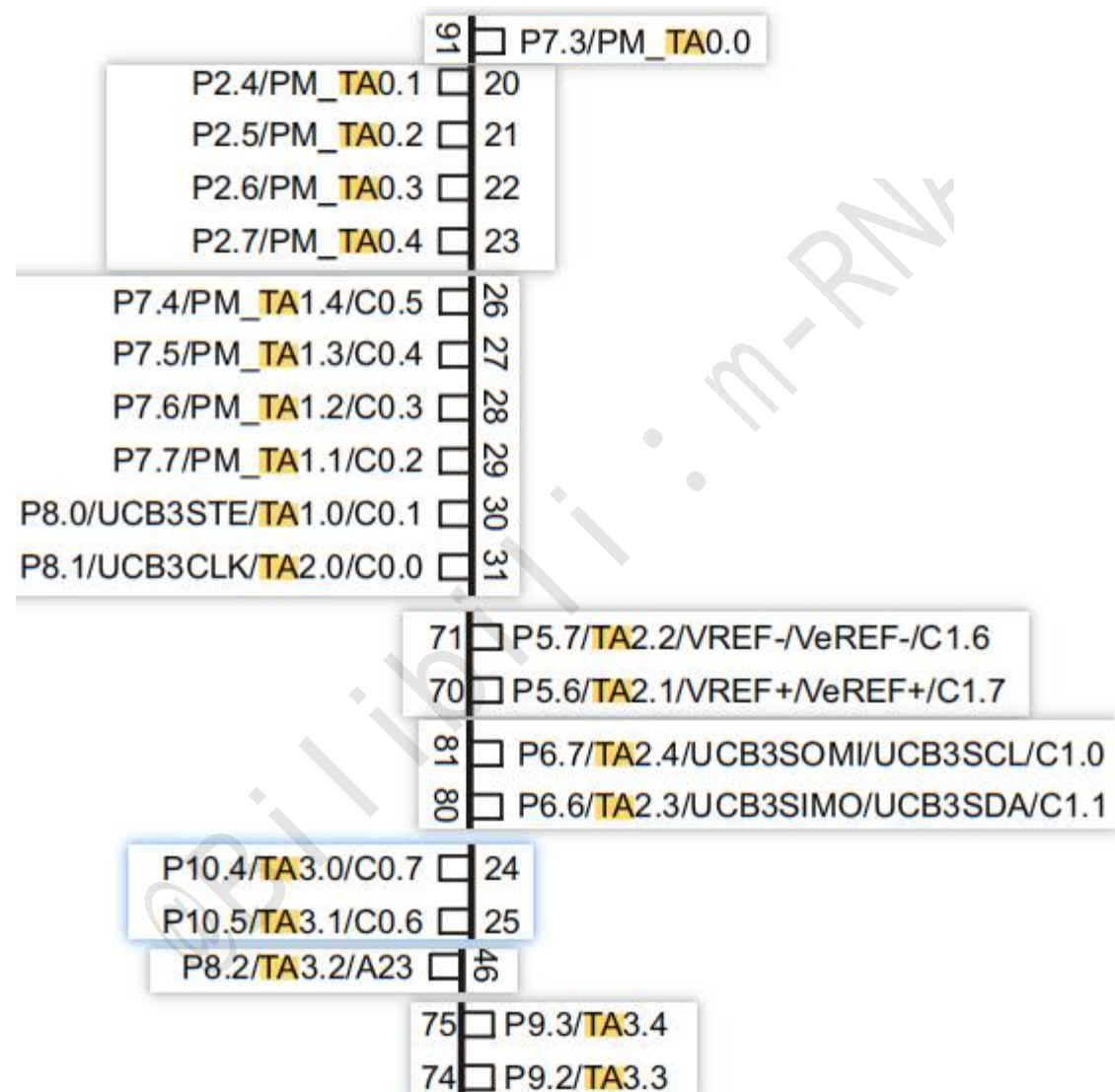


Figure 19-14. Output Example – Timer in Up/Down Mode







MSP432P401R 定时器A

TAx.x	0	1	2	3	4
TA0	P7.3	P2.4	P2.5	P2.6	P2.7
TA1	P8.0	P7.7	P7.6	P7.5	P7.4
TA2	P8.1	P5.6	P5.7	P6.6	P6.7
TA3	P10.4	P10.5	P8.2	P9.2	P9.3

timer_a.h

1 初始化定时器为PWM模式

Timer_A_generatePWM(TIMESTAMP_Ax_BASE, &TimAx_PWMConfig);

2 改变比较值（占空比/周期）

Timer_A_setCompareValue(TIMESTAMP_Ax, COMPARE_REGISTER_x, CCR);

一般配置步骤

- 0.配置时钟
- 1.配置GPIO复用
- 2.配置结构体
- 3.初始化定时器

PIN NAME (P7.x)	x	FUNCTION	CONTROL BITS OR SIGNALS ⁽¹⁾			
			P7DIR.x	P7SEL1.x	P7SEL0.x	P7MAPx
P7.4/PM_TA1.4/C0.5 ⁽²⁾	4	P7.4 (I/O)	I: 0; O: 1	0	0	X
		TA1.CCI4A	0	0	1	default
		TA1.4	1			
		N/A	0	1	0	X
		DVSS	1			
		C0.5 ⁽³⁾⁽⁴⁾	X	1	1	X
P7.5/PM_TA1.3/C0.4 ⁽²⁾	5	P7.5 (I/O)	I: 0; O: 1	0	0	X
		TA1.CCI3A	0	0	1	default
		TA1.3	1			
		N/A	0	1	0	X
		DVSS	1			
		C0.4 ⁽³⁾⁽⁴⁾	X	1	1	X
P7.6/PM_TA1.2/C0.3 ⁽²⁾	6	P7.6 (I/O)	I: 0; O: 1	0	0	X
		TA1.CCI2A	0	0	1	default
		TA1.2	1			
		N/A	0	1	0	X
		DVSS	1			
		C0.3 ⁽³⁾⁽⁴⁾	X	1	1	X
P7.7/PM_TA1.1/C0.2 ⁽²⁾	7	P7.7 (I/O)	I: 0; O: 1	0	0	X
		TA1.CCI1A	0	0	1	default
		TA1.1	1			
		N/A	0	1	0	X
		DVSS	1			
		C0.2 ⁽³⁾⁽⁴⁾	X	1	1	X

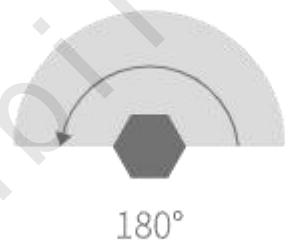
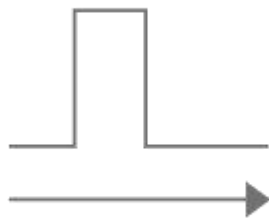
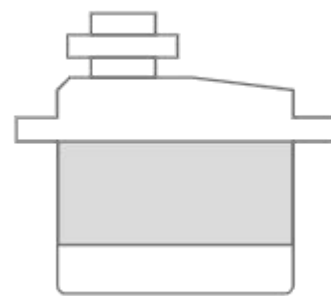
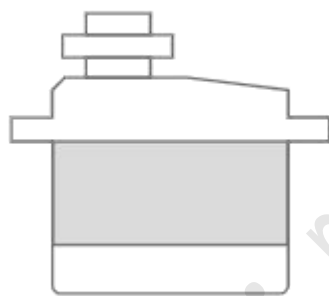
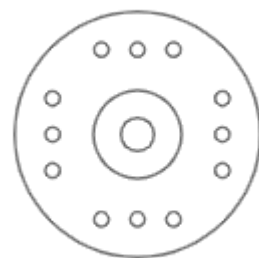
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P7

TIMER_A

$$T_{timer_a} = \frac{ClkDiv \times (CCR0 + 1)}{f_{clk}}$$

CLKDIV \in [1, 8] \cup {10, 12, 14, 16, 20, 24, 28, 32, 40, 48, 56, 64 };



频率：50Hz 占空比：2.5% ~12.5%

8-3 定时器 A 捕获

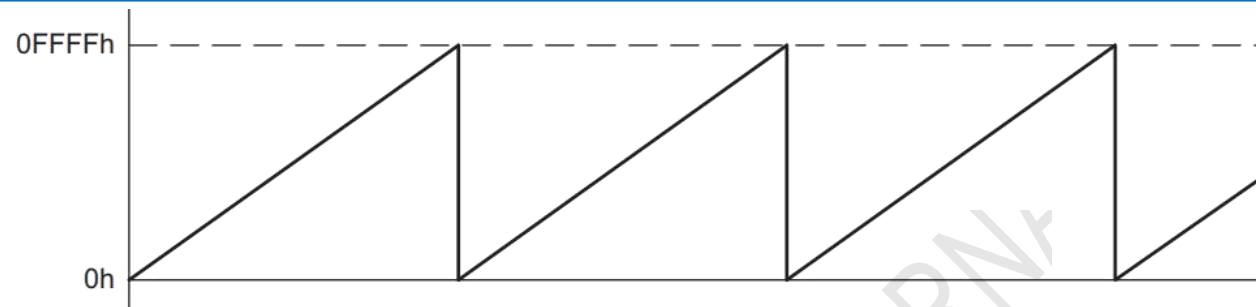


Figure 19-4. Continuous Mode

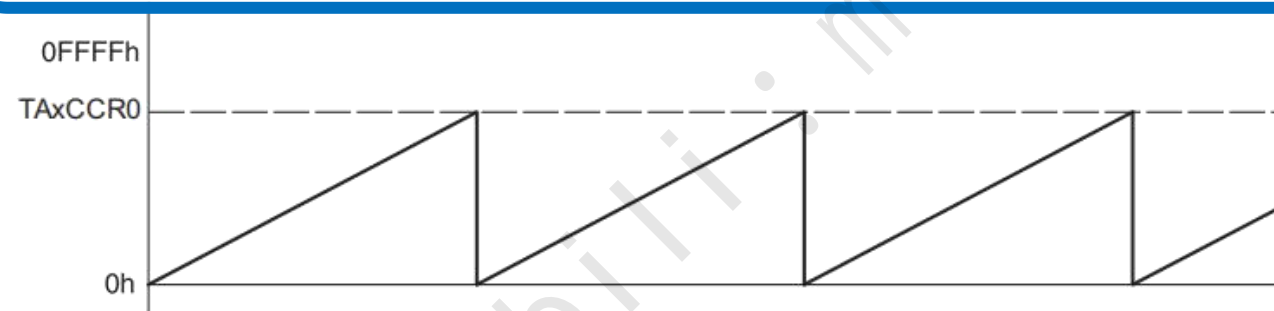


Figure 19-2. Up Mode

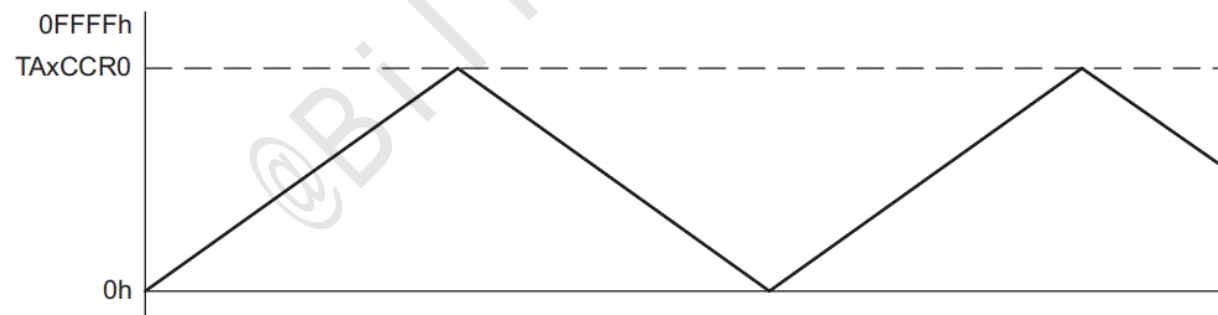


Figure 19-7. Up/Down Mode

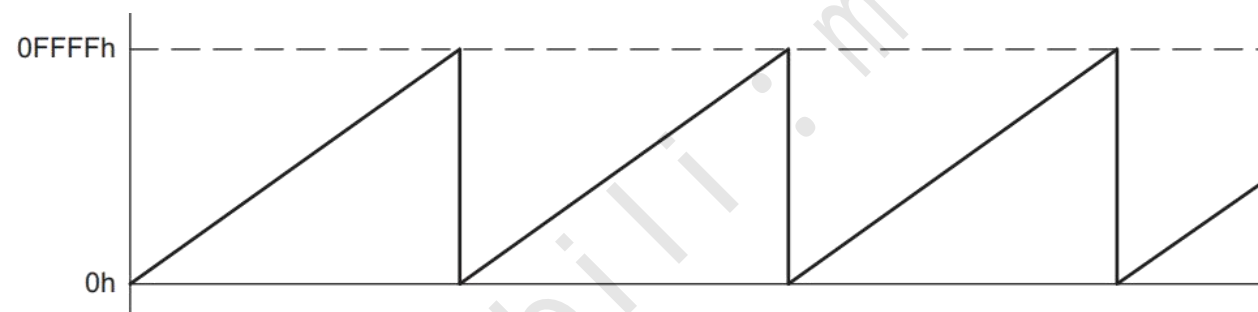


Figure 19-4. Continuous Mode

timer_a.h

1 初始化定时器为连续计数模式

```
Timer_A_configureContinuousMode(TIMER_Ax, &continuousModeConfig);
```

2 配置定时器的捕获模式

```
Timer_A_initCapture(TIMER_Ax_BASE, &captureModeConfig);
```

3 选择模式开始计数

```
Timer_A_startCounter(TIMER_Ax_BASE, TIMER_A_CONTINUOUS_MODE);
```

timer_a.h

4 清除定时器溢出中断标志位

Timer_A_clearInterruptFlag(TIMESTAMP_Ax_BASE);

5 清除定时器捕获中断标志位

Timer_A_clearCaptureCompareInterrupt(TIMESTAMP_Ax, REGISTER_N);

timer_a.h

6 获取定时器溢出中断状态

Timer_A_getEnabledInterruptStatus(TIMER_Ax_BASE);

7 获取定时器捕获中断状态

Timer_A_getCaptureCompareEnabledInterruptStatus(TIMER_Ax, REGISTER_N);

timer_a.h

8 获取定时器捕获电平状态

Timer_A_getSynchronizedCaptureCompareInput(TIMER_Ax, REGISTER_N, Setting);

返回值:

TIMER_A_OUTPUTMODE_OUTBITVALUE_LOW

TIMER_A_OUTPUTMODE_OUTBITVALUE_HIGH

interrupt.h

9 开启定时器 A 端口中断

Interrupt_enableInterrupt(INT_TAx_N);

10 开启总中断

Interrupt_enableMaster(void);

一般配置步骤

- 0.配置时钟
- 1.复用引脚
- 2.配置连续计数结构体
- 3.初始化定时器连续计数
- 4.配置捕获结构体
- 5.初始化定时器为捕获
- 6.选择模式开始计数
- 7.清除中断标志位
- 8.开启定时器端口中断
- 9.开启总中断
- 10.编写TIMA ISR

TIMER_A -> CAP

$$t_{cap} = \frac{ClkDiv \times (CCRN + 1)}{f_{clk}}$$

CLKDIV \in [1, 8] \cup {10, 12, 14, 16, 20, 24, 28, 32, 40, 48, 56, 64 };

表 6-75. Port P5 (P5.6 and P5.7) Pin Functions

PIN NAME (P5.x)	x	FUNCTION	CONTROL BITS OR SIGNALS ⁽¹⁾		
			P5DIR.x	P5SEL1.x	P5SEL0.x
P5.6/TA2.1/VREF+/VeREF+/ C1.7	6	P5.6 (I/O)	I: 0; O: 1	0	0
		TA2.CCI1A	0	0	1
		TA2.1	1		
		N/A	0	1	0
		DVSS	1		

| 谢 谢 |

如有错误，请发到邮箱：m-RNA@qq.com