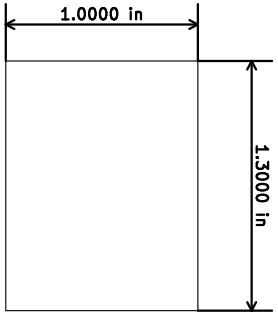
GENERAL NOTES

1) DESIGN CRITERIA
    A) MIN TRACE WIDTH = 0.0050 INCH / 0.127 MM
    B) MIN TRACE SPACING = 0.0050 INCH / 0.127 MM
    C) MIN DEVICE PITCH = 0.0236 INCH / 0.600 MM
    D) MIN DRILL SIZE = 0.0118 INCH / 0.300 MM
2) FABRICATION
    A) FABRICATE PER IPC-6012 CLASS 2 UNLESS OTHERWISE SPECIFIED
    B) PCB SHALL BE ROHS COMPLIANT / LEAD-FREE
    C) LAMINATE: FR-4 WITH Tg RATING 150C MIN, PER IPC-4101/24 OR 26
    D) FLAMMABILITY RATING: UL 94V-0
    E) FINISHED THICKNESS = 0.0624 INCH / 1.6 MM (STANDARD 4 LAYER BOARD PROCESS)
    F) COPPER CLADDING: PER IPC-MF-150, 1.0 oz
    G) PLATING ENIG PER IPC-4552
    H) SOLDERMASK: PLI MATERIAL PER IPC-5M-840 CLASS T OR M, COLOR BLUE
    I) SILKSCREEN: PERMANENT ORGANIC, NON-CONDUCTIVE INK, COLOR WHITE, 300 DPI
    J) BOARD OUTLINE DEFINED IN LAYER "Edge.Cuts.gbr"
    K) DE-BURR/BREAK ALL SHARP EDGES
    L) EDGE HOLES SHALL BE CASTELLATED BY FOLLOWING EDGE CUTS THROUGH BOARD EDGE THROUGH HOLES
3) MANUFACTURING
    A) MARK MFG IO, DATE CODE (YYWW) ON BOTTOM SILK LAYER, NOT TO INTERFERE WITH EXISTING SILK
    B) PCB MANUFACTURER CAN PANELIZE ASSEMBLER SPECIFICATION
    C) 100% NETLIST ELECTRICAL VERIFICATION REQUIRED
4) PACKAGING
    A) PCB SURFACES MUST BE PROTECTED FROM MOISTURE.
    B) PCB SURFACES MUST BE PROTECTED FROM ABRASION DURING SHIPPING.



LAYER	NAME	MATERIAL	THICKNESS	CONSTANT	FILE EXT
1	TOP SILK	SILKSCREEN	N/A	N/A	F.SilkS
2	TOP SOLDER	SOLDER RESIST	0.010mm	3.5	F.Mask
3	TOP LAYER	COPPER	0.035mm		Top
4	DIELECTRIC 1	FR-4	0.230mm	4.2	
5	GROUND LAYER	COPPER	0.035mm		DigitalGND
6	DIELECTRIC 2	FR-4	1.000mm	4.2	
7	POWER LAYER	COPPER	0.035mm		VDD
8	DIELECTRIC 3	FR-4	0.230mm	4.2	
9	BOTTOM LAYER	COPPER	0.035mm		Bottom
10	BOTTOM SOLDER	SOLDER RESIST	0.010mm	3.5	B.Mask
11	BOTTOM SILK	SILKSCREEN	N/A	N/A	B.SilkS

Hologram

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Title: Minimus Prime

Size: A4	Date: 2018-03-05	**Rev: 1.1**
KiCad E.D.A. kicad 4.0.6		Id: 1/1