National Semiconductor

February 19, 2010

DAC121S101/DAC121S101Q

12-Bit Micro Power, RRO Digital-to-Analog Converter

General Description

The DAC121S101 is a full-featured, general purpose 12-bit voltage-output digital-to-analog converter (DAC) that can operate from a single +2.7V to 5.5V supply and consumes just 177 µA of current at 3.6 Volts. The on-chip output amplifier allows rail-to-rail output swing and the three wire serial interface operates at clock rates up to 30 MHz over the specified supply voltage range and is compatible with standard SPI™, QSPI, MICROWIRE and DSP interfaces. Competitive devices are limited to 20 MHz clock rates at supply voltages in the 2.7V to 3.6V range.

The supply voltage for the DAC121S101 serves as its voltage reference, providing the widest possible output dynamic range. A power-on reset circuit ensures that the DAC output powers up to zero volts and remains there until there is a valid write to the device. A power-down feature reduces power consumption to less than a microWatt.

The low power consumption and small packages of the DAC121S101 make it an excellent choice for use in battery operated equipment.

The DAC121S101 is a direct replacement for the AD5320 and the DAC7512 and is one of a family of pin compatible DACs, including the 8-bit DAC081S101 and the 10-bit DAC101S101. The DAC121S101 operates over the extended industrial temperature range of −40°C to +105°C while the DAC121S101Q operates over the Grade 1 automotive temperature range of −40°C to +125°C. The DAC121S101 is available in a 6-lead TSOT and an 8-lead MSOP and the DAC121S101Q is available in the 6-lead TSOT only.

Features

- DAC121S101Q is AEC-Q100 Grade 1 qualified and is manufactured on an Automotive Grade Flow.
- Guaranteed Monotonicity
- Low Power Operation
- Rail-to-Rail Voltage Output
- Power-on Reset to Zero Volts Output
- Wide Temperature Range of −40°C to +125°C
- Wide Power Supply Range of +2.7V to +5.5V
- Small Packages
- Power Down Feature

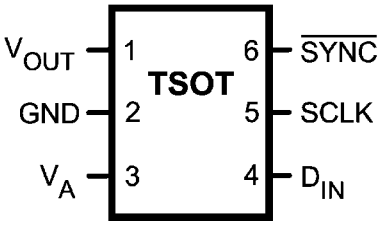
Key Specifications

Resolution	12 bits
DNL	+0.25, -0.15 LSB (typ)
Output Settling Time	8 µs (typ)
Zero Code Error	4 mV (typ)
Full-Scale Error	−0.06 %FS (typ)
Power Consumption	
— Normal Mode	0.64mW (3.6V) / 1.43mW (5.5V) typ
— Pwr Down Mode	0.14µW (3.6V) / 0.39µW (5.5V) typ

Applications

- Battery-Powered Instruments
- Digital Gain and Offset Adjustment
- Programmable Voltage & Current Sources
- Programmable Attenuators
- Automotive

Pin Configuration



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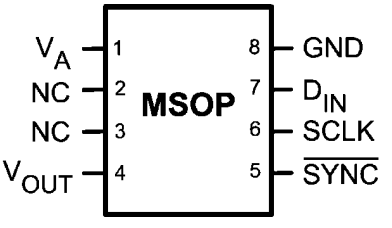

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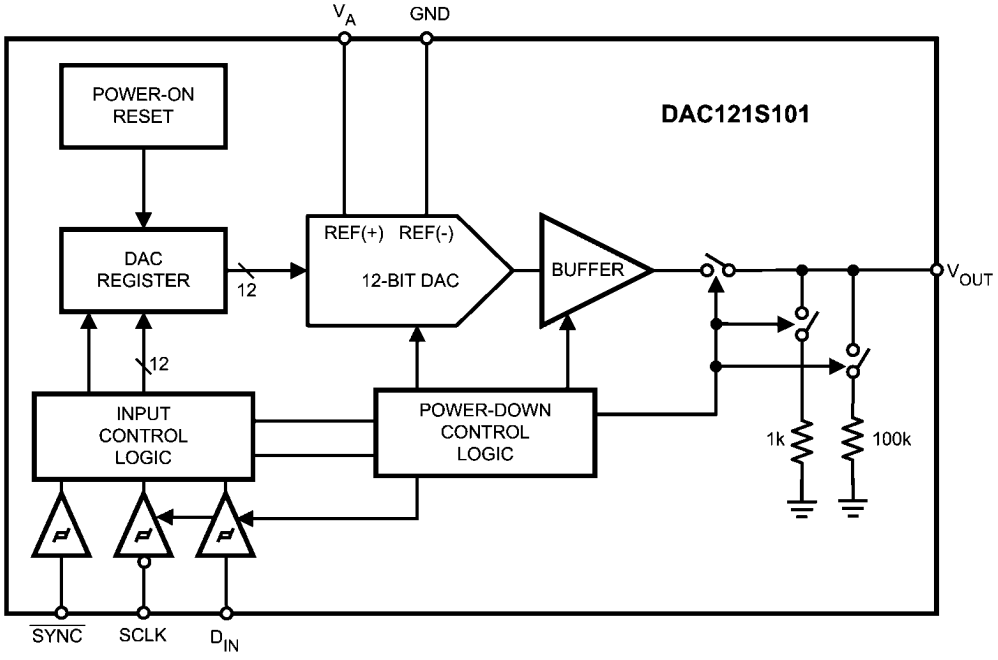
Ordering Information

Order Numbers	Temperature Range	Package	Top Mark	Feature
DAC121S101CIMM	$-40°C \le T_A \le +105°C$	MSOP	X60C	
DAC121S101CIMMX	$-40°C \le T_A \le +105°C$	MSOP T/R		
DAC121S101CIMK	$-40°C \le T_A \le +105°C$	TSOT	X61C	
DAC121S101CIMKX	$-40°C \le T_A \le +105°C$	TSOT T/R		
DAC121S101QCMK	$-40°C \le T_A \le +125°C$	TSOT	X61Q	AEC-Q100 Grade 1 Qualified; Automotive Grade Production Flow
DAC121S101QCMKX	$-40°C \le T_A \le +125°C$	TSOT T/R		
DAC121S101EVAL	Evaluation Board	TSOT		

Block Diagram



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Pin Descriptions

TSOT (SOT-23) Pin No.	MSOP Pin No.	Symbol	Description
1	4	V_{OUT}	DAC Analog Output Voltage.
2	8	GND	Ground reference for all on-chip circuitry.
3	1	V_A	Power supply and Reference input. Should be decoupled to GND.
4	7	D_{IN}	Serial Data Input. Data is clocked into the 16-bit shift register on the falling edges of SCLK after the fall of $\overline{SYNC}$.
5	6	SCLK	Serial Clock Input. Data is clocked into the input shift register on the falling edges of this pin.
6	5	$\overline{SYNC}$	Frame synchronization input for the data input. When this pin goes low, it enables the input shift register and data is transferred on the falling edges of SCLK. The DAC is updated on the 16th clock cycle unless $\overline{SYNC}$ is brought high before the 16th clock, in which case the rising edge of $\overline{SYNC}$ acts as an interrupt and the write sequence is ignored by the DAC.
	2, 3	NC	No Connect. There is no internal connection to these pins.

A.C. and Timing Characteristics

The following specifications apply for V_A = +2.7V to +5.5V, R_L = 2kΩ to GND, C_L = 200 pF to GND, f_{SCLK} = 30 MHz, input code range 48 to 4047. **Boldface limits apply for $T_{MIN} \leq T_A \leq T_{MAX}$**: all other limits T_A = 25°C, unless otherwise specified.

Symbol	Parameter	Conductions		Typical	Limits	Units (Limits)
f_{SCLK}	SCLK Frequency				**30**	MHz (max)
t_s	Output Voltage Settling Time (*Note 10*)	400h to C00h code change, R_L = 2kΩ	$C_L \leq$ 200 pF	8	**10**	µs (max)
			C_L = 500 pF	12		µs
		00Fh to FF0h code change, R_L = 2kΩ	$C_L \leq$ 200 pF	8		µs
			C_L = 500 pF	12		µs
SR	Output Slew Rate			1		V/µs
	Glitch Impulse	Code change from 800h to 7FFh		12		nV-sec
	Digital Feedthrough			0.5		nV-sec
t_{WU}	Wake-Up Time	V_A = 5V		6		µs
		V_A = 3V		39		µs
$1/f_{SCLK}$	SCLK Cycle Time				**33**	ns (min)
t_H	SCLK High time			5	**13**	ns (min)
t_L	SCLK Low Time			5	**13**	ns (min)
t_{SUCL}	Set-up Time $\overline{SYNC}$ to SCLK Rising Edge			−15	**0**	ns (min)
t_{SUD}	Data Set-Up Time			2.5	**5**	ns (min)
t_{DHD}	Data Hold Time			2.5	**4.5**	ns (min)
t_{CS}	SCLK fall to rise of $\overline{SYNC}$	V_A = 5V		0	**3**	ns (min)
		V_A = 3V		−2	**1**	ns (min)
t_{SYNC}	$\overline{SYNC}$ High Time	2.7 ≤ V_A ≤ 3.6		9	**20**	ns (min)
		3.6 ≤ V_A ≤ 5.5		5	**10**	ns (min)

Transfer Characteristic

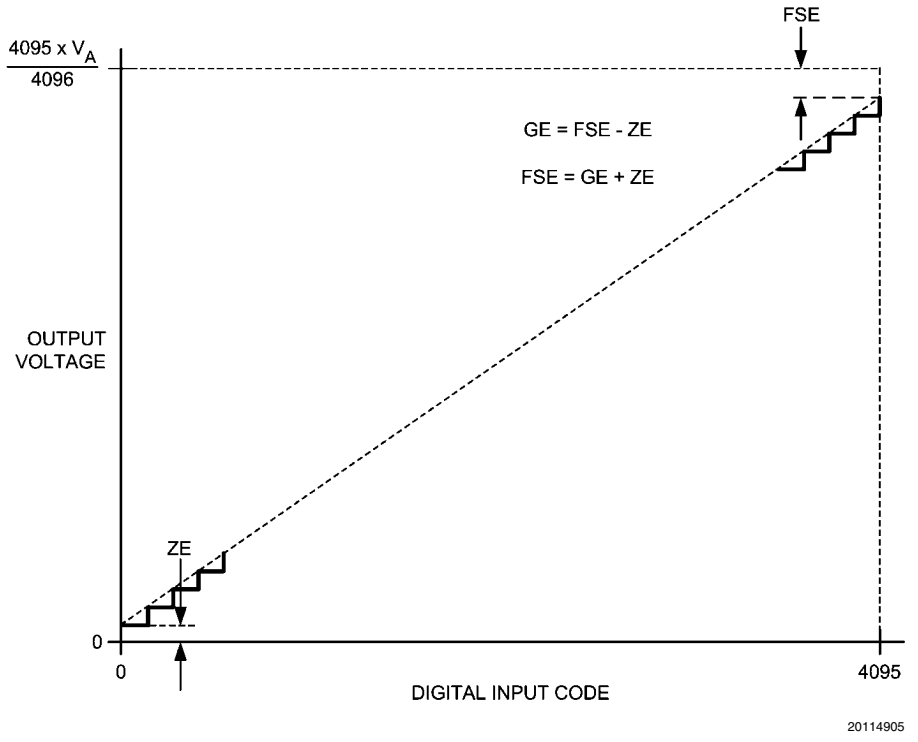

FIGURE 1. Input / Output Transfer Characteristic

Timing Diagram

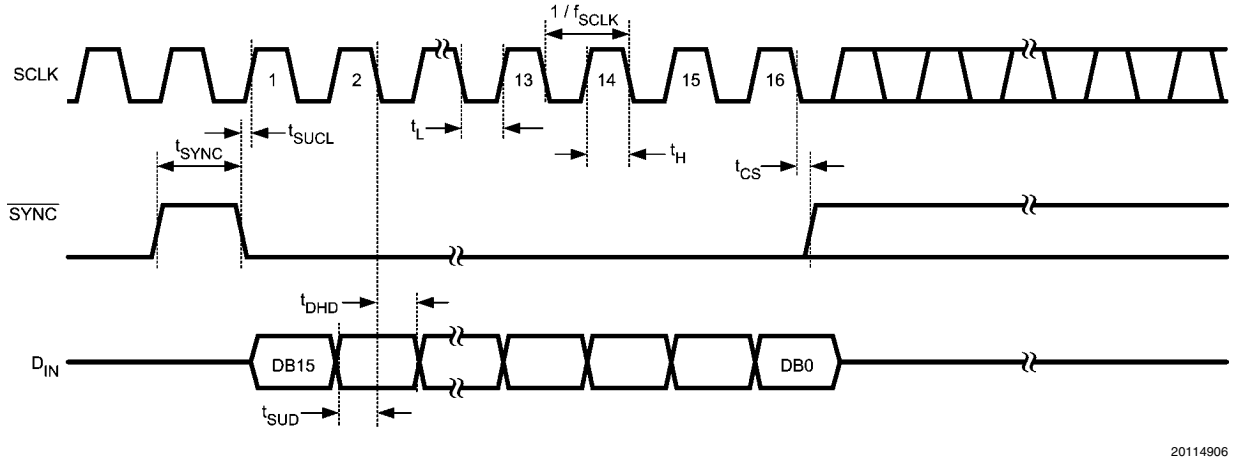

FIGURE 2. DAC121S101 Timing

1.0 Functional Description

1.1 DAC SECTION

The DAC121S101 is fabricated on a CMOS process with an architecture that consists of switches and a resistor string that are followed by an output buffer. The power supply serves as the reference voltage. The input coding is straight binary with an ideal output voltage of:

$$V_{OUT} = V_A \times (D / 4096)$$

where *D* is the decimal equivalent of the binary code that is loaded into the DAC register and can take on any value between 0 and 4095.

1.2 RESISTOR STRING

The resistor string is shown in *Figure 3*. This string consists of 4096 equal valued resistors with a switch at each junction of two resistors, plus a switch to ground. The code loaded into the DAC register determines which switch is closed, connecting the proper node to the amplifier. This configuration guarantees that the DAC is monotonic.

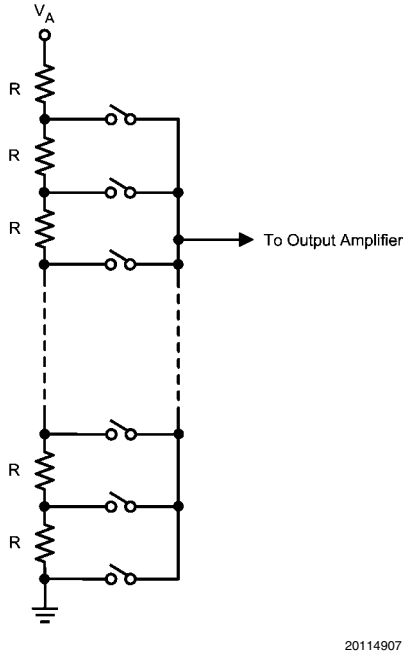

FIGURE 3. DAC Resistor String

1.3 OUTPUT AMPLIFIER

The output buffer amplifier is a rail-to-rail type, providing an output voltage range of 0V to V_A. All amplifiers, even rail-to-rail types, exhibit a loss of linearity as the output approaches the supply rails (0V and V_A, in this case). For this reason, linearity is specified over less than the full output range of the DAC. The output capabilities of the amplifier are described in the Electrical Tables.

1.4 SERIAL INTERFACE

The three-wire interface is compatible with SPI, QSPI and MICROWIRE, as well as most DSPs. See the Timing Diagram for information on a write sequence.

A write sequence begins by bringing the $\overline{SYNC}$ line low. Once $\overline{SYNC}$ is low, the data on the D_{IN} line is clocked into the 16-bit serial input register on the falling edges of SCLK. On the 16th falling clock edge, the last data bit is clocked in and the programmed function (a change in the mode of operation and/or a change in the DAC register contents) is executed. At this point the $\overline{SYNC}$ line may be kept low or brought high. In either case, it must be brought high for the minimum specified time before the next write sequence as a falling edge of $\overline{SYNC}$ can initiate the next write cycle.

Since the $\overline{SYNC}$ and D_{IN} buffers draw more current when they are high, they should be idled low between write sequences to minimize power consumption.

1.5 INPUT SHIFT REGISTER

The input shift register, *Figure 4*, has sixteen bits. The first two bits are "don't cares" and are followed by two bits that determine the mode of operation (normal mode or one of three power-down modes). The contents of the serial input register are transferred to the DAC register on the sixteenth falling edge of SCLK. See Timing Diagram, *Figure 2*.

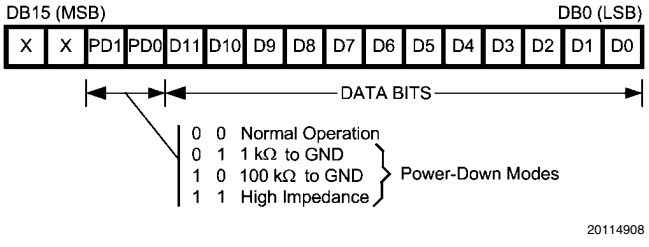

FIGURE 4. Input Register Contents

Normally, the $\overline{SYNC}$ line is kept low for at least 16 falling edges of SCLK and the DAC is updated on the 16th SCLK falling edge. However, if $\overline{SYNC}$ is brought high before the 16th falling edge, the shift register is reset and the write sequence is invalid. The DAC register is not updated and there is no change in the mode of operation or in the output voltage.