MIPS 5 Stage Pipelined CPU

By Brandon Nguyen and Christopher Kenyon

**Design**

In order to create a 5 stage pipelined CPU, we used the single stage MIPS CPU we had created previously as a baseline. We added several key modules to the single stage CPU in order to support pipelining, including additional registers in between the modules for each of the pipeline stages, a hazard detection unit and a forwarding unit. The 5 stages are D (Decode, also denoted as ID), F (Fetch, also denoted as IF), X (Execute, also denoted as EX), M (Memory, also denoted as MEM), and W (Write). THe naming conventions in our code can be easily understood knowing what we referred to each stage as. The logic for the hazard detection unit and forwarding unit was taken from the textbook and is implemented in the files hazardDetectionUnit.v and forwardingUnit.v, respectively. These units will use the instruction codes to set values for hazardPCenable, hazardIFIDenable, hazardIDEXenable, fwdA\_D, fwdB\_D, fwdA\_X and fwdB\_X which are used by the registers between stages entitled ID\_EX, IF\_ID, MEM\_WB, and EX\_MEM, to denote the stages that the registers are between. The implementation of signals to flush registers was also necessary to support branching instructions. The logic for these flush signals can be found in the IF\_ID, and ID\_EX verilog files.

**Results**

The program concluded after 179 clock cycles. The length of each clock cycle was 20 ns. Although we expected that the code would take 183 cycles to complete, we can account for our program finishing 4 cycles earlier than expected as a result of needing to flush the last 4 stages before true completion where the cpu is ready for further processing. During our debugging process, we checked to make sure that not only were the contents of the registers correct at the end of execution, but also along the way after each type of MIPS instruction so that we could be sure that our CPU executed all types of MIPS instructions correctly. The contents of all the relevant registers at the conclusion of the project appears as follows:

# --------------------CYCLE 179--------------------

#

# $0: 0 $at: 0

# $t0: 40 $t1: 0

# $t2: 4294967280 $t3: 21

# $t4: 21 $t5: 1

# $t6: 0 $t7: 0

# $s0: 0 $s1: 9

# $s2: 5 $s3: 9

# Minimum: -16 Maximum: 21