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Mach-Zehnder Interferometer Proposal

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1 Introduction

In silicon photonics, the Mach-Zehnder interferometer (MZI) serves as a fundamental building block for a vast array of optical applications. By splitting an input optical signal into two distinct arms and subsequently recombining them, the MZI translates phase differences—induced by thermal, electrical, or environmental changes—into measurable intensity variations.

This proposal outlines a design proposal for an imbalanced MZI and provides its simulation results.

2 Modelling and Simulation

2.1 Waveguide Geometry and Simulation

For this design, strip waveguide with 500 nm width and 220 nm height was chosen, with TE polarization. The simulated waveguide mode profiles are shown.

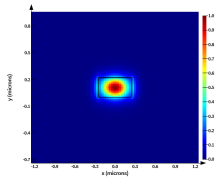

Fig. 1 E intensity, 500 x 220 x 500

Compact model for the waveguide

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2.2 Transmission spectrums and table of parameter variations

The design: 5 unbalanced MZIs with path length differences of 62, 162, 262, 362, and 462 microns. The goal to analyze how path length differences impact FSR experimentally versus theoretically.

2.3 Plot of effective and group index of the waveguide, versus wavelength

The compact model of the waveguide was calculated as:

$$n_{eff}(\lambda) = 2.447 - 1.13(\lambda - \lambda_0)^2$$

The transfer function of the interferometer vs wavelength:

The transfer function for the MZI can be written as follows:

$$I_o = \frac{I_i}{4}\left|e^{-i\beta_1 L_1 - \frac{\alpha_1}{2}L_1} + e^{-i\beta_2 L_2 - \frac{\alpha_2}{2}L_2}\right|^2 \tag{2}$$

For this design, identical waveguides are used, resulting in a simplified transfer function:

$$I_o = \frac{I_i}{2}[1 + cos(\beta \Delta L)] \tag{3}$$

The spectral distance between successive transmission maxima, known as the Free Spectral Range (FSR), is determined by the group index and the path length difference:

$$FSR_\lambda = \frac{\lambda^2}{n_g \Delta L} \tag{4}$$

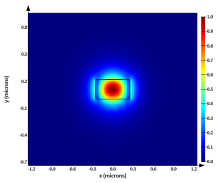

Fig. 2 Ex - TE mode

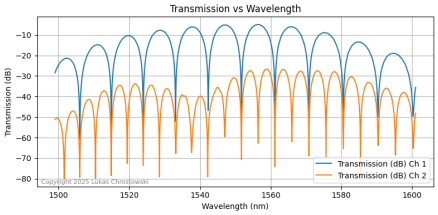

Fig. 3 MZI 1 with delta L of 62 microns

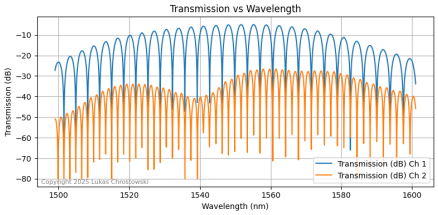

Fig. 4 MZI 2 with delta L 162 microns

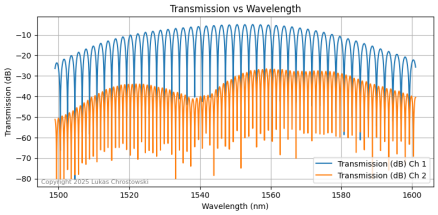

Fig. 5 MZI 3 with delta L of 262 microns

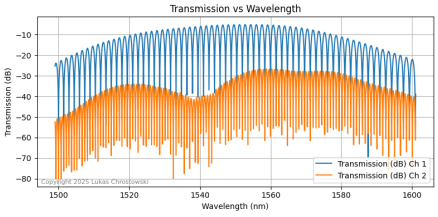

Fig. 6 MZI 4 with delta L of 362 microns

where the group index, n_g, is defined as

$$n_g(\lambda) = n_{eff}(\lambda) - \lambda * \frac{dn_{eff}(\lambda)}{d\lambda} \quad (5)$$

Table of parameter variations and expected performance for each:

Circuit geometry

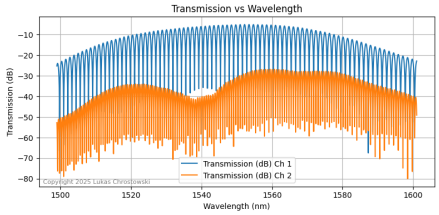

Fig. 7 MZI 5 with delta L of 462 microns

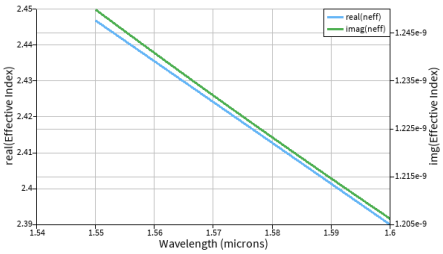

Fig. 8 Wavelength vs effective index

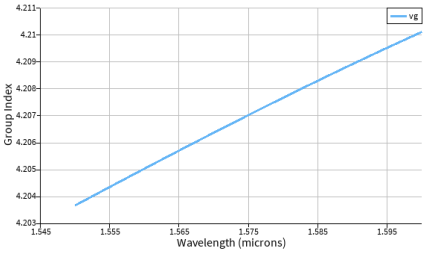

Fig. 9 Wavelength vs group index

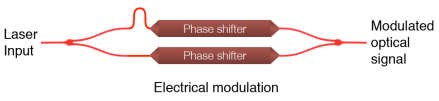

Fig. 10 Imbalanced interferometer, used to extract modulator parameters [1]

Length WG 1	Length WG 2	dL	FSR (pm)
37.95	100	62.05	10791.44
37.95	200	162.05	4132.2
37.95	300	262.05	2555.33
37.95	400	362.05	1849.54
37.95	500	462.05	1449.25

lambda	1550
n	3.47
dn/dlambda	-0.0
ng	3.59

Table 1 MZI parameters and theoretical FSR

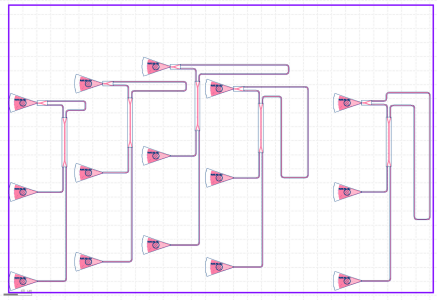

Fig. 11 This is a caption

3 Fabrication

Two chips were fabricated in this course. Either report on one dataset, or on both. Choose the text as appropriate. (TODO)

3.1 Washington Nanofabrication Facility (WNF) silicon photonics process:

The devices were fabricated using 100 keV Electron Beam Lithography [[1]]. The fabrication used silicon-on-insulator wafer with 220 nm thick silicon on 3 μm thick silicon dioxide. The substrates were 25 mm squares diced from 150 mm wafers. After a solvent rinse and hot-plate dehydration bake, hydrogen silsesquioxane resist (HSQ, Dow-Corning XP-1541-006) was spin-coated at 4000 rpm, then hotplate baked at 80 °C for 4 minutes. Electron beam lithography was performed using a JEOL JBX-6300FS system operated at 100 keV energy, 8 nA beam current, and 500 μm exposure field size. The machine grid used for shape placement was 1 nm, while the beam stepping grid, the spacing between dwell points during the shape writing, was 6 nm. An exposure dose of 2800 μC/cm2 was used. The resist was developed by immersion in 25% tetramethylammonium hydroxide for 4 minutes, followed by a flowing deionized water rinse for 60 s, an isopropanol rinse for 10 s, and then blown dry with nitrogen. The silicon was removed from unexposed areas using inductively coupled plasma etching in an Oxford Plasmalab System 100, with a chlorine gas flow of 20 sccm, pressure of 12 mT, ICP power of 800 W, bias power of 40 W, and a platen temperature of 20 °C, resulting in a bias voltage of 185 V. During etching, chips were mounted on a 100 mm silicon carrier wafer using perfluoropolyether vacuum oil.

3.2 Applied Nanotools, Inc. NanoSOI process:

The photonic devices were fabricated using the NanoSOI MPW fabrication process by Applied Nanotools Inc. (`http://www.appliednt.com/nanosoi`; Edmonton, Canada) which is based on direct-write 100 keV electron beam lithography technology. Silicon-on-insulator wafers of 200 mm diameter, 220 nm device thickness and 2 μm buffer oxide thickness are used as the base material for the fabrication. The wafer was pre-diced into square substrates with dimensions of 25x25 mm, and lines were scribed into the substrate backsides to facilitate easy separation into smaller chips once fabrication was complete. After an initial wafer clean using piranha solution (3:1 H2SO4:H2O2) for 15 minutes and water/IPA rinse, hydrogen silsesquioxane (HSQ) resist was spin-coated onto the substrate and heated to evaporate the solvent. The photonic devices were patterned using a Raith EBPG 5000+ electron beam instrument using a raster step size of 5 nm. The exposure dosage of the design was corrected for proximity effects that result from the backscatter of electrons from exposure of nearby features. Shape writing order was optimized for efficient patterning and minimal beam drift. After the e-beam exposure and subsequent development with a tetramethylammonium sulfate (TMAH) solution, the devices were inspected optically for residues and/or defects. The chips were then mounted on a 4” handle wafer and underwent an anisotropic ICP-RIE etch process using chlorine after qualification of the etch rate. The resist was removed from the surface of the devices using a 10:1 buffer oxide wet etch, and the devices were inspected using a scanning electron microscope (SEM) to verify patterning and etch quality. A 2.2 μm oxide cladding was deposited using a plasma-enhanced chemical vapour deposition (PECVD) process based on tetraethyl orthosilicate (TEOS) at 300ºC. Reflectrometry measurements were performed throughout the process to verify the device layer, buffer oxide and cladding thicknesses before delivery.

4 Experimental Data

To characterize the devices, a custom-built automated test setup [[2]] with automated control software written in Python was used (`http://siepic.ubc.ca/probestation`). An Agilent 81600B tunable laser was used as the input source and Agilent 81635A optical power sensors as the output detectors. The wavelength was swept from 1500 to 1600 nm in 10 pm steps. A polarization maintaining (PM) fibre was used to maintain the polarization state of the light, to couple the TE polarization into the grating couplers [[3]]. A 90^{o} rotation was used to inject light into the TM grating couplers [4]. A polarization maintaining fibre array was used to couple light in/out of the chip [www.plcconnections.com].

Plots of experimental data. The following figure was generated using a built-in Python interpreter!

5 Analysis

Data analysis to extract waveguide group index, etc.

Comparison of experimental results with simulations.

6 Conclusion

The conclusion goes here.

7 Acknowledgements

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References

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3. Wang Y, Wang X, Flueckiger J, et al. (2014) Focusing sub-wavelength grating couplers with low back reflections for rapid prototyping of silicon photonic circuits. Opt Express 22:20652. `https://doi.org/10.1364/oe.22.020652`