Investigation of Switching-Induced Local Defects in Oxide-Based CBRAM Using Expanded Analytical Model of TDDB

Reika Ichihara, Shosuke Fujii, Marina Yamaguchi, Yoko Yoshimura, Yuichiro Mitani, and Masumi Saitoh

***Abstract*— The degradation behavior of Ag/SiO_2-based conductive bridging RAM (CBRAM) is analyzed by conventional and expanded time-dependent dielectric breakdown (TDDB) models. By comparing the total cycling stress with time-to-breakdown (t_{bd}) of the SiO_2 used as a solid-electrolyte switching layer, it is clarified that the cycling stress does not reach the level at which dielectric breakdown of the SiO_2 is triggered. On the other hand, we found that the t_{bd} distribution after several cycles of set/reset stress agrees well with the simulated t_{bd} distribution derived from expanded TDDB models, in which we assumed that a large amount of defects exists locally in the device area. This approach is useful for understanding the degradation in solid-electrolyte oxide of CBRAM.**

***Index Terms*— Conductive bridging RAM (CBRAM), deposited SiO_2, endurance, reset failure, stress-induced leakage current (SILC), time-dependent dielectric breakdown (TDDB).**

I. Introduction

THE conductive bridging RAM (CBRAM) is one of the promising candidates for the future nonvolatile memory [1]–[3]. The resistive switching in the CBRAM is based on the formation and the disruption of metallic filament (usually composed of Ag or Cu) through an electrolyte layer with high resistivity [4]–[7]. From the viewpoint of manufacturability, a SiO_2 or metal–oxide is often used as the electrolyte layer.

Endurance becomes one of the critical issues in the CBRAM with such oxide film-based switching layer as well as in oxide-based RAM (OxRAM), in which resistive switching originates from the change of oxygen vacancy distribution [8], [9]. In many cases, the devices become stuck in the low resistance state in cycling and fall into reset failure [10]–[14]. To understand the physical mechanism of the reset failure, many attempts to investigate the degradation behavior have been reported in the past. In [12] and [13], using *in situ* transmission electron microscopy (TEM), it was revealed that the distribution or the density of Cu in the switching layer is changed by cycling stress. In [14], using TEM and energy dispersive X-ray spectrometry (EDS), it was demonstrated that Ag filament penetrates into the inert electrode after the unexpected negative-set behavior. The investigation based on the physical analysis is extremely useful to understand the physical photograph directly. However, such method has the difficulty in obtaining statistical data.

As a statistical analysis, some approaches using a well-known percolation model that explains the dielectric breakdown of oxide film [15] have been reported. In [16]–[21], it is shown that the variations of set and reset characteristics are understood well by using the percolation model. Reference [22] can be cited as a study which applies such a technique to understand the degradation of OxRAM during cycles. In [22], the modified percolation model, assuming two kinds of defects, set-induced oxygen vacancy and high-field stress-induced trap, was presented. The authors compared the simulation using this modified model and the experimentally obtained set-disturb lifetime after constant voltage stress (CVS) imitating an excessive stress in cycling, and succeeded in explaining the abrupt and drastic set-disturb lifetime degradation after cycling. In this method, in addition to the oxygen deficiency concentration of the filament rupture region in high-resistance state, the generation rate and the size of the two types of defects are required for simulation. In the case of OxRAM, by referring to well-known characteristics of stress-induced leakage current (SILC), reasonable values can be assumed as parameters in the simulation, because the switching itself is similar to the breakdown process of oxide. Likewise, it is considered to be reasonable to regard CVS as a cycling stress. However, in the case of CBRAM, the degradation is expected to depend on the movement of metal ions. Therefore, it is impossible to simply refer to the generation of oxide defects as a model of degradation. Moreover, in the quantitative analysis, CVS cannot be simply regarded as cycling stress.

In this paper, to understand the degradation behavior in CBRAM, a simpler and more direct analysis which does not require the information on the specific behaviors of metal ions is presented. We propose a time-dependent dielectric breakdown(TDDB) evaluation method combined with the CBRAM cycling stress, and an expanded percolation model that can consider local damage in the oxide. This paper organized as follows. First of all, it is carefully investigated whether the

Manuscript received January 29, 2019; revised March 1, 2019; accepted March 10, 2019. Date of current version April 22, 2019. The review of this paper was arranged by Editor G.-H. Koh. *(Corresponding author: Reika Ichihara.)*

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Digital Object Identifier 10.1109/TED.2019.2904984

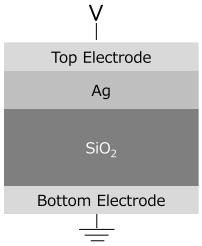

Fig. 1. Cross-sectional view of the CBRAM device used in this paper.

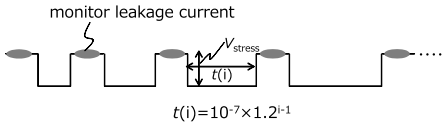

Fig. 2. Measurement flow for TDDB evaluation.

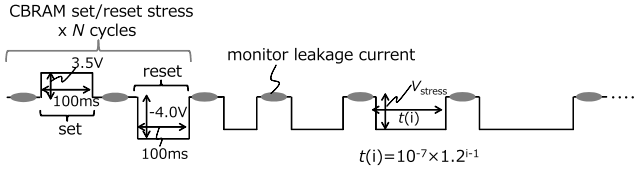

Fig. 3. Applied stress patterns for the evaluation of the effect of set/reset on the degradation of SiO_2. Several cycles of set/reset stresses are applied before TDDB measurement. The number of cycles is set such that reset failure is not caused.

percolation model is applicable to the deposited SiO_2 used as the electrolyte layer (Section III). In Section IV, we compare the total cycling stress up to failure with the dielectric breakdown lifetime of the deposited SiO_2. In Section V, the results obtained by a new analytical method are presented and discuss the physical photograph of degradation. Finally, we summarize the conclusion in Section VI.

II. Experiment

A cross-sectional view of a CBRAM device used in this paper is shown in Fig. 1. As a solid-electrolyte layer, a SiO_2 film was deposited on the bottom electrode. Unless otherwise noted, the thickness of the SiO_2 is 3.5 nm. An active Ag film was then formed. To evaluate the characteristics of degradation and dielectric breakdown in the deposited SiO_2, we used a TDDB measurement method shown in Fig. 2. CVS was repeatedly applied to the device. The width of the stress pulse is increased step-by-step. The leakage current was monitored periodically between the stresses. In order to avoid unexpected formation of Ag filament during this measurement, the polarity of the stress voltage is set to be opposite to that of set operation.

In addition, the measurement shown in Fig. 3 is also performed to investigate the impact of CBRAM switching on the SiO_2 degradation. In this measurement, several cycles of set/reset stresses were applied before the TDDB measurement. All of the data were measured at room temperature.

III. Degradation and Dielectric Breakdown in Deposited SiO_2

There exists a large database about TDDB in SiO_2. The percolation model is commonly accepted as an explanation of the breakdown [15], [23], [24]. This model assumes that a conductive path connecting between anode and cathode made from randomly generated defects causes dielectric breakdown. In the simplified cell-based analytic percolation model [15] (Fig. 4), the relationship between the cumulative probability of breakdown (F) and the defect density λ (λ is equal to the probability that any cell is defective) is expressed as

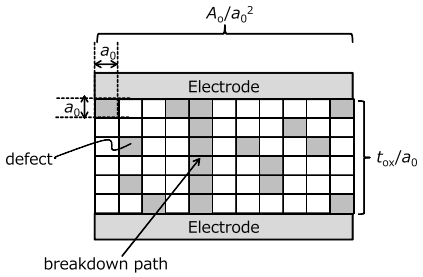

Fig. 4. Schematic of the cell-based analytic percolation model [15].

$$F = 1 - \left(1 - \lambda^{\frac{t_{ox}}{a_0}}\right)^{\frac{A_0}{a_0^2}} \tag{1}$$

$$\ln\{-\ln(1-F)\} = \ln\left[-\frac{A_0}{a_0^2}\cdot\ln\left(1-\lambda^{\frac{t_{ox}}{a_0}}\right)\right] \tag{2}$$

where A_o is the device area, t_{ox} is the thickness of dielectric, and a_0 is the diameter of a cell. Physically, a_0 means a typical distance between neighboring defects that are effective in forming a conductive path. Using the approximation of $\ln(1-\lambda^n) \approx -\lambda^n$, which is valid when $\lambda \ll 1\lambda \ll 1$ (2) is simplified to

$$\ln\{-\ln(1-F)\} = \ln\left(\frac{A_0}{a_0^2}\right) + \frac{t_{ox}}{a_0}\cdot\ln(\lambda). \tag{3}$$

Equation (3) explains the area dependence and thickness dependence of breakdown statistics [15]. However, most of the studies have been performed for thermally grown SiO_2. There is insufficient information on breakdown statistics for deposited SiO_2. Hence, first of all, we evaluate degradation and dielectric breakdown of deposited SiO_2 used in this paper, and compare these characteristics with the conventional model described above, which is valid for thermally grown SiO_2.

A. SILC Characteristics

In this paper, SILC is defined as

$$\text{SILC} = \frac{I - I_{\text{initial}}}{I_{\text{initial}}} \tag{4}$$

where I is the leakage current monitored after each stress pulse, and I_{initial} is the leakage current of the as-fabricated device. Fig. 5 shows the time-dependent SILC obtained by the measurement shown in Fig. 2. The SILC is gradually increased, and then, the current suddenly increases greatly. This indicates that the defect density gradually increases still the breakdown occurs. This photograph roughly agrees with the conventional model.

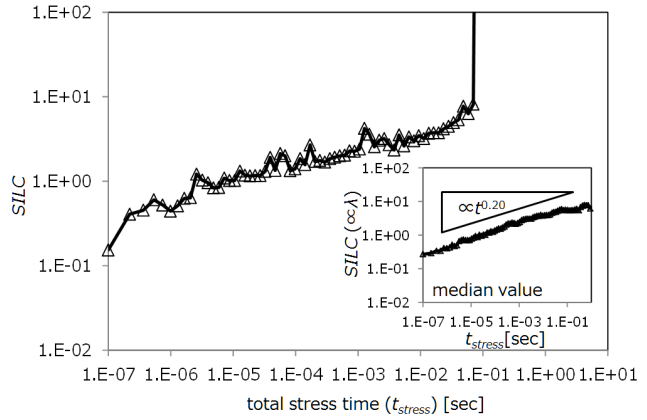

Fig. 5. SILC dependence on the total stress time. Inset: median value of 40 devices.

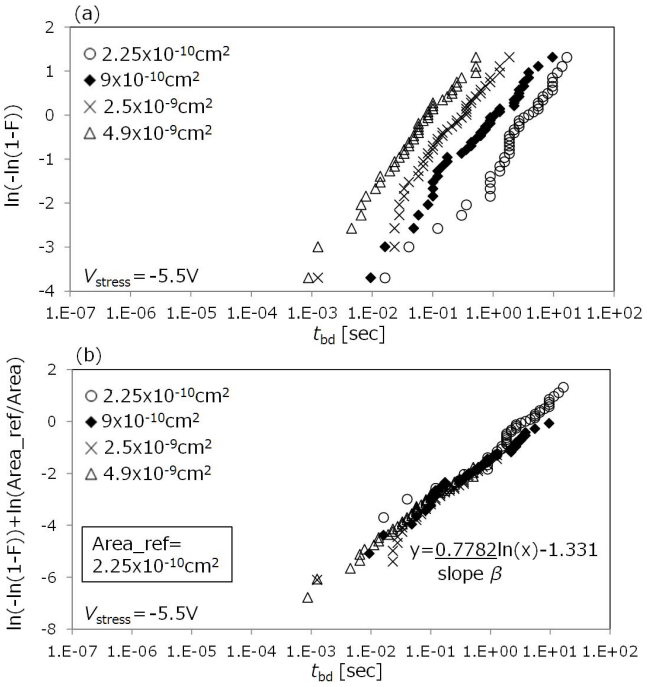

Fig. 6. (a) t_{bd} distributions for different device areas. (b) t_{bd} distributions normalized to 2.25×10^{-10} cm^2.

B. Area Dependence of Dielectric Breakdown

Time-to-breakdown (t_{bd}) distributions for different device areas are shown in Fig. 6(a). At the same stress time, larger device shows larger probability of breakdown. Then, area normalization of the breakdown probability is performed using the following equation, which is derived from (3):

$$\ln\{-\ln(1-F_1)\} - \ln\{-\ln(1-F_2)\} = \ln\left(\frac{A_1}{A_2}\right) \quad (5)$$

where A_1 and A_2 are the two different device areas, and F_1 and F_2 are the cumulative breakdown probability of devices with the areas of A_1 and A_2, respectively. This relationship originates from the assumption that the breakdown occurs randomly and locally in the device area. ("Locally" means breakdown is inevitable when at least one conductive path is formed.) Fig. 6(b) shows area-normalized t_{bd} distributions. Data for different areas are located on the single curve. Thus, the Poisson random statistics and locality of breakdown are valid for the deposited SiO_2 breakdown.

C. Random component in Thickness Direction

As described in (1)–(3), the conventional percolation model assumes that defects are generated randomly in the thickness direction, as well as in the lateral direction. In other words, the generation of a defect does not trigger generation of another defect on the same line in the thickness direction. To confirm whether this photograph is valid in the deposited SiO_2, we extracted t_{ox}/a_o using the procedure below.

On the presumption that the SILC is proportional to the defect density (λ) in the dielectric [25], which is valid if the dimension of the device area is large enough compared to that of the dielectric thickness, (3) can be transformed into a function of stress time (t_{stress}) using time-dependent SILC. As shown in the inset of Fig. 5, λ is described as

$$\lambda = \alpha \cdot t_{stress}^{0.2}. \quad (6)$$

Replacing (6) with λ in (3), t_{bd} distribution is written as

$$\ln\{-\ln(1-F)\} = \ln\left(\frac{A_0}{a_0^2}\right) + \frac{t_{ox}}{a_0}\cdot\ln(\alpha) + \frac{t_{ox}}{a_0}\cdot 0.2\cdot\ln(t). \quad (7)$$

Hence, the Weibull plot of $\ln(t_{bd})$ should be a straight line, and its slope β is

$$\beta = \frac{t_{ox}}{a_0}\cdot 0.2. \quad (8)$$

By comparing the actual slope β shown in Fig. 6(b) with the above theory, t_{ox}/a_o, which is the number of cells in the thickness direction, is extracted to be around 4. a_0 is derived as 0.88 nm. $t_{ox}/a_o > 1$ and the reasonable value of a_0 imply that a random component exists in the thickness direction.

From these results shown in Sections III-A–III-C, the degradation and the breakdown behaviors of deposited SiO_2 used as the switching layer of the CBRAM agree well with the conventional percolation model. Therefore, we can use this model for the analysis of degradation in the CBRAM operation.

IV. Comparison Between Cycling Stress and Degradation of SiO_2

Fig. 7 shows an example of cycling characteristics of the CBRAM under the voltage ramp-up verification procedure. In this case, the device falls into reset failure at the 49th cycles. When the read current cannot become lower than reset criterion current in the reset sequence, we assume that the device falls into reset failure. We confirmed that the failure mode in all of the devices we measured was reset failure. In order to verify whether or not the reset failure simply originated from the degradation in SiO_2 regardless of switching behavior, the amount of cycling stress is compared quantitatively with the TDDB of the SiO_2. In the switching operation with the voltage ramp-up verification procedure, multiple pulses with different voltages are applied repeatedly. To compare the cycling stress with the TDDB under CVS,

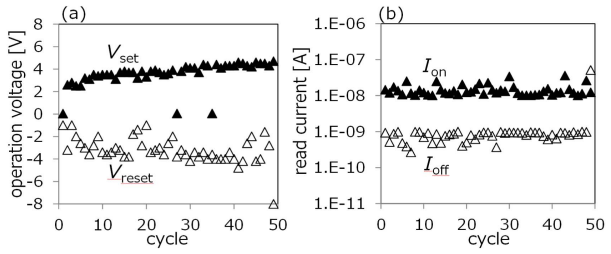

Fig. 7. Example of the cycling characteristic for the CBRAM under voltage ramp-up verification procedure. The voltage of set/reset operating pulse is ramped up by 0.1 V until the read current satisfies the criteria. Read is carried out after each operating pulse. The operating pulsewidth is 100 ms. (a) Set voltage (V_{set}), reset voltage (V_{reset}), (b) on current (I_{ON}), off current (I_{OFF}), as a function of cycle number.

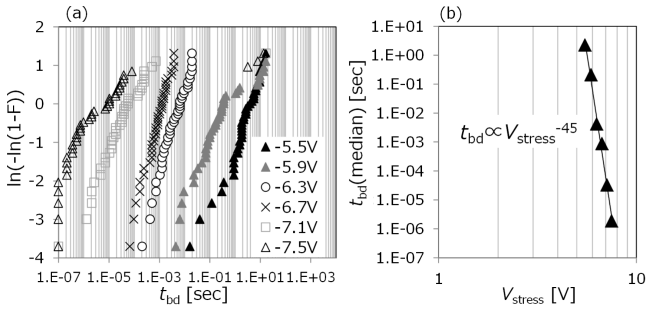

Fig. 8. (a) t_{bd} distributions for a different V_{stress}. Device area is 2.25×10^{-10} cm^2. (b) t_{bd} at 50% versus V_{stress}.

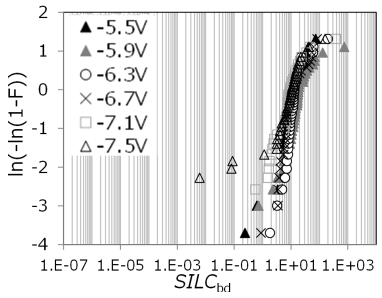

Fig. 9. $SILC_{bd}$ for a different V_{stress}.

impact of stress voltage (V_{stress}) on breakdown should be examined first.

Fig. 8(a) shows t_{bd} distributions for different V_{stress}. t_{bd} shifts to shorter time range with higher V_{stress}. As shown in Fig. 8(b), t_{bd} follows power-law voltage acceleration which is expressed as

$$t_{bd} \propto V_{stress}^{-z}$$
$$z = 45. \tag{9}$$

On the other hand, as shown in Fig. 9, the SILC just before breakdown ($SILC_{bd}$) does not depend on V_{stress}. This suggests a photograph in which accumulation of defects generated by the stress triggers breakdown and the critical number of defects for the breakdown is independent of the stress amplitude. In this situation, we can use (10) to convert each voltage step in cycling operation to an equivalent t_{stress} (t_{eff}) under CVS at a reference voltage (V_{ref})

$$t_{eff} = \sum \Delta t\,(i) \left(\frac{V\,(i)}{V_{ref}}\right)^{z} \tag{10}$$

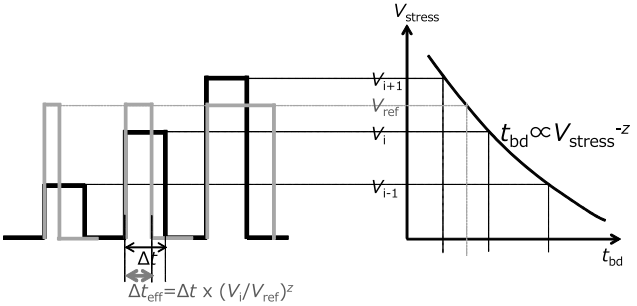

Fig. 10. Schematic for the translation of stress pulses with various voltages to the equivalent pulses of reference voltage.

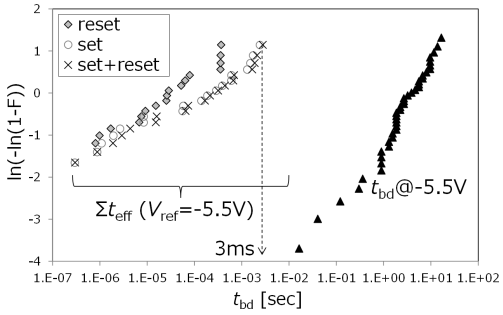

Fig. 11. Distribution of the total stress time ($V_{ref} = -5.5$ V) of the cycling operation before the reset failure extracted by (10) and that of t_{bd} for the fresh SiO_2 under $V_{stress} = -5.5$ V.

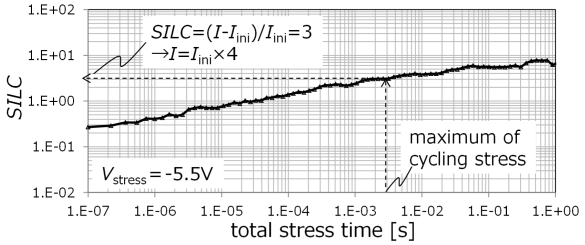

Fig. 12. Time-dependent SILC under V_{stress} of -5.5 V. The data are the same as those of the inset of Fig. 5.

where z is the voltage acceleration factor of t_{bd} in accordance with the power law and $\Delta t(i)$ is the pulsewidth of each set and reset pulses. Fig. 10 shows a schematic illustration of this conversion method. This method was proposed by Kerber *et al.* [26] and widely used as a reliability testing tool.

Fig. 11 shows the comparison of the distribution of total cycling stress time equivalent to $V_{ref} = -5.5$ V extracted by (10) and t_{bd} distribution of fresh SiO_2 at $V_{stress} = -5.5$ V. The sum of the cycling stress is distributed over three decades, but it stays in a time domain much shorter than t_{bd}. It is therefore clarified that the cycling stress does not reach t_{bd} of fresh SiO_2.

Even if the dielectric breakdown did not occur, the leakage current of the SiO_2 gradually increases with defect generation and may exceed the reset criterion current. Next, we address this possibility. As shown in Fig. 11, the maximum time of total cycling stress equivalent to $V_{ref} = -5.5$ V is about 3 ms. Fig. 12 indicates that SILC is about 3 at 3 ms. That is, the leakage current is about 4 times larger, at most, than that of the initial state. Fig. 13 shows the distributions of initial read current (I_{ini}) and $I_{ini} \times 4$. $I_{ini} \times 4$ is lower than the reset

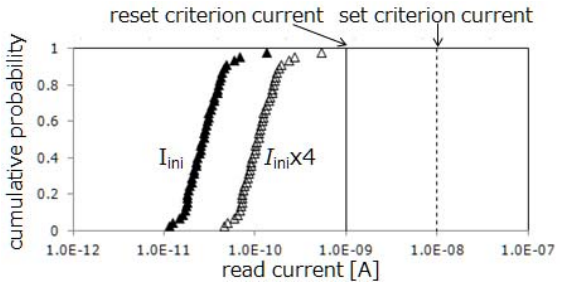

Fig. 13. Distributions of I_{ini} and $I_{ini} \times 4$.

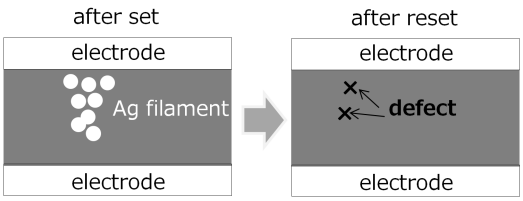

Fig. 14. Schematic images of the set/reset inducing localized degradation in a SiO_2 layer.

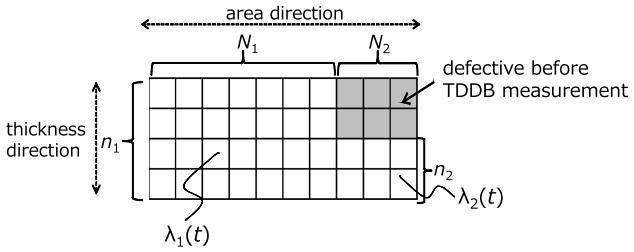

Fig. 15. Schematic of expanded cell-based analytic percolation model (model 2).

criterion current for cycling indicating that SILC is not the direct cause of reset failure.

V. Analysis Considering Local Damage Induced by Switching Operation

As described above, the dielectric breakdown and increase in leakage current induced by cumulative cycling stress regardless of switching operation are not the main causes of reset failure. Therefore, CBRAM switching probably has an additional effect on the degradation of the SiO_2.

Fig. 14 shows the schematic images of set and reset. Even if reset (disruption of Ag filament) is completed, part of the traces of Ag filament may become defective. Thus, the local defects could be generated at a rate much higher than the usual case and it may accelerate reset failure. In order to confirm this hypothesis, we simulate t_{bd} distribution when the defects exist locally in the filament area. In addition, we measured the actual t_{bd} distribution after applying several cycles of set/reset stress, and compared it with the simulation.

A. Simulation of t_{bd} Distribution Considering Local Damage

To simulate t_{bd} distribution when the local damage exists, the analytic percolation cell-based model [15] is expanded to "model 2," in which a device has two regions with different characteristics. Fig. 15 shows a schematic illustration

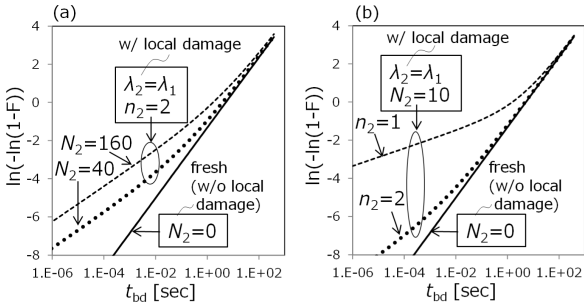

Fig. 16. Simulated t_{bd} distribution. (a) Case where N_2 region of $n_2 = 2$ becomes larger. (b) Case where n_2 of region N_2 becomes smaller.

of model 2. We suppose that N_1 and N_2 regions may have different parameters of n and $\lambda(t)$. n is the number of defects in the thickness direction required for formation of a breakdown path. $\lambda(t)$ is the probability that a cell becomes defective after applying stress of time $= t$. Here, nondestructive probabilities or survival rates in regions N_1 and $N_2$are described as

$$1 - F_1 = \{(1 - \lambda_1(t))^{n_1}\}^{N_1} \tag{11}$$

where F_1 is the cumulative probability of breakdown in N_1 region.

$$1 - F_2 = \{(1 - \lambda_2(t))^{n_2}\}^{N_2} \tag{12}$$

where F_2 is the cumulative probability of breakdown in N_2 region. Nondestructive probability in the whole device is the probability that the breakdown does not occur in both N_1 and N_2 regions, and thus,

$$1 - F = (1 - F_1) \times (1 - F_2) \tag{13}$$

where F is the cumulative probability of breakdown in the whole device. From (11) to (13), cumulative probability breakdown (F) in a device having two regions with different characteristics is

$$F = 1 - \{(1 - \lambda_1(t))^{n_1}\}^{N_1} \times \{(1 - \lambda_2(t))^{n_2}\}^{N_2}. \tag{14}$$

We now simulate t_{bd} distributions in several situations based on the assumptions described below.

Assumptions: Degradation mechanism in N_1 region is the same as that of fresh SiO_2, and these are as follows.

1) $a_0 = 0.88$ nm (extracted in Section III-C).
2) $\lambda_1(t, V_{stress} = -5.5\ V) = 0.055 \times t^{0.2}$. (Prefactor of 0.055 is uniquely extracted from t_{bd} distribution at $V_{stress} = -5.5$ V shown in Fig. 6(b) and time-dependent SILC shown in the inset of Fig. 5.)
3) a_0 in N_2 region is the same as that of fresh SiO_2.
4) $N_1 + N_2 =$ device area/a_0^2.

In addition, we assume that λ_2 equals λ_1, because standard percolation model, in which generation of a defect does not trigger generation of another defect on the same line in the thickness direction, can explain well the experimental results [15].

The simulated t_{bd} distributions based on model 2 are shown in Fig. 16. Fig. 16(a) shows the case where N_2 region with $n_2 = 2$ becomes larger, which corresponds to the situation that the damaged area expands in lateral direction. On the

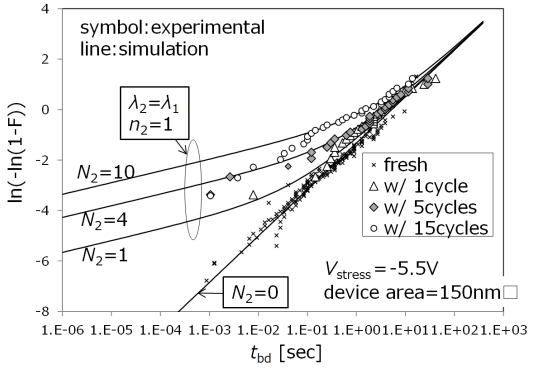

Fig. 17. Experimental t_{bd} distributions with and without several cycles of set/reset stresses and simulated t_{bd} distributions.

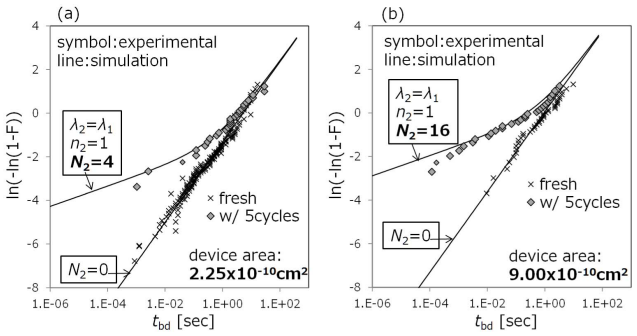

Fig. 18. Simulated t_{bd} distributions and experimental data with and without 5 cycles of set/reset stresses. (a) Device area is 2.25×10^{-10} cm^2. (b) Device area is 9×10^{-10} cm^2. The same stress conditions are used for (a) and (b).

other hand, Fig. 16(b) shows the case where n_2 of region N_2 becomes smaller, which means that the damaged area expands in vertical direction. In both cases, the t_{bd} distribution in a short time range deviates from that of the fresh SiO_2. The degree of the deviation becomes more significant as the damaged area expands. On the other hand, the upper tail of the t_{bd} distributions converges to the distribution of the fresh SiO_2. If the assumption that CBRAM switching causes the local damage in SiO_2 is correct, the actual t_{bd} distributions after several set/reset cycles are expected to be similar to this simulation results.

B. Experimental t_{bd} Distributions After Several Cycles of CBRAM Operating Stress

Fig. 17 shows t_{bd} distribution of the fresh SiO_2 and t_{bd} distributions after several set/reset cycles obtained by the measurements shown in Figs. 2 and 3. The t_{bd} distributions after set/reset cycles show that the lower tail deviates from the fresh SiO_2 distribution, and the upper tail is almost the same as that of the fresh SiO_2. In addition, the degree of the deviation becomes larger as the set/reset cycle proceeds. This trend agrees qualitatively with the simulation considering the local damage shown in Section V-A. It is therefore proved that the CBRAM operation causes the local damage in SiO_2 and the damaged area expands with cycling.

In order to provide a clearer photograph of degradation, simulation parameters that quantitatively reproduce the measured value are also shown in Fig. 17. The experimental data agree well with the simulated t_{bd} distributions under the assumption that N_2 region with $n_2 = 1$ expands to $N_2 = 1$, 4, and 10 with cycling number = 1, 5, and 15. That is, the damaged area expands in the lateral direction with cycling. This results implies that the switching position can vary from cycle to cycle. On the other hand, the expansion rate of the damaged area is not linear, but becomes slower with the number of cycles. This can be explained as follows. As shown in Fig. 7(a), V_{set} tends to increase with cycling. In other words, it becomes difficult for Ag filament to grow as cycling proceeds. In the measurement shown in Fig. 3, the set/reset stresses are constant regardless of the number of cycles. In this situation, the trend of the increase in damaged area induced by the formation of Ag filament could become slower with

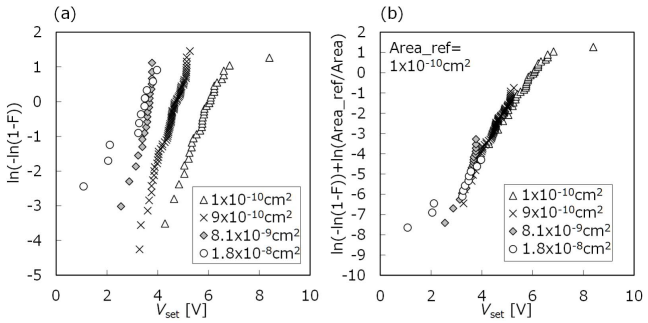

Fig. 19. (a) V_{set} distributions for different device areas. The SiO_2 thickness of CBRAM used in this experiment is 5 nm. (b) V_{set} distributions normalized to 1×10^{-10} cm^2.

the number of cycles. The assumption we imposed in Fig. 17 is, hence, qualitatively consistent with the real case.

In addition, we confirmed that the parameters shown in Fig. 17 are applicable to the devices with different areas. The simulated t_{bd} distributions and the experimental data for different device areas are shown in Fig. 18. Compared to the characteristics for the device area of 2.25×10^{-10} cm^2 [Fig. 18(a)], the t_{bd} distribution of the 9×10^{-10} cm^2 device [Fig. 18(b)] shows a larger amount of deviation from the trend of fresh SiO_2. This result is quantitatively reproduced when we assume that the ratio of the damaged area N_2 increases linearly with the device area.

To facilitate discussion of the validity of this assumption, V_{set} distributions of the CBRAMs with different device areas are shown in Fig. 19(a). Here, V_{set} is defined as the minimum voltage under voltage ramp-up stress that realizes the same read current regardless of the device area. V_{set} is decreased for the larger device. In Fig. 19(b), the area-normalized V_{set} distributions derived from (5) are shown. Data for different areas are located on the single curve. Therefore, similar to the dielectric breakdown or forming process in an OxRAM [27], the set process of the CBRAM is a spatially random event, and the probability of the set in the unit area is constant. It means that if an applied set stress is the same regardless of the device area and if a current limitation is not imposed, the average number of generated filaments is proportional to the device area. In this paper, the set/reset stresses applied before TDDB measurement are constant regardless of the device area, and

no-current limitation was imposed. Therefore, the assumptions for the simulation are reasonable; that is, the damaged region may be induced by the formation of filament, and it is proportional to the device area. The parameters shown in Fig. 17 were found to be applicable to different device areas with only reasonable changes.

It should be emphasized that there are countless sets of parameters that reproduce the actual data if we can change all parameters freely, and the example shown here is not a unique solution. However, the reproducibility of the results under many experimental conditions with only a few reasonable changes of the parameters indicates that the photograph presented here well represents the real situation of degradation in the CBRAM.

VI. Conclusion

In this paper, the degradation behavior of the deposited SiO_2 used in the CBRAM was analyzed using conventional and expanded TDDB methods. As a result, it was clarified that the sum of cycling stress does not reach the level causing the TDDB of the fresh SiO_2. On the other hand, we found that the t_{bd} distribution after several cycles of set/reset stresses agrees well with the simulated t_{bd} distribution, in which we assumed that high density of defects exists locally in the device area. The assumption that the damaged area becomes larger in the lateral direction with cycling can reproduce the experimental data. The local degradation in SiO_2 expanding with cycling, which may be associated with the change of Ag filament position between cycles, could accelerate reset failure. The suppression of the change of switching position during cycles may be a key factor to avoid the expansion of damaged area. The proposed model is considered to be effective in the understanding of the degradation in CBRAM with oxide electrolyte layer.

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