Role of Grain Boundary Percolative Defects and Localized Trap Generation on the Reliability Statistics of High-κ Gate Dielectric Stacks

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Abstract — **Grain boundary (GB) microstructural defects in polycrystalline high-κ dielectric thin films may cause localized non-random trap generation during the percolation breakdown (BD) process. We study the effect of this non-random trap generation on the reliability statistics of the metal gate (MG) – high-κ (HK) stack. For the first time, we propose a fundamental physics-based Kinetic Monte Carlo (KMC) model considering the thermodynamics and kinetics of bond breaking, generation of oxygen vacancy traps and simulating the trap evolution process in a dual-layer HK - interfacial layer (IL) gate stack. Our simulation model helps explain the non-Weibull distribution trends for time dependent dielectric breakdown data (TDDB) and also determine the sequence of BD which is found to be independent of the thickness ratio of (t_{HK} : t_{IL}) and gate voltage (V_g). Results show that the IL layer is always more susceptible to early percolation and circuit level failure may only be caused by multiple soft BD (SBD) events in the IL layer. The possibility of a sequential IL → HK breakdown is very unlikely for operating voltage conditions of V_{op} = 1V.**

Keywords – Grain boundary, Percolation, Thermochemical model, Time dependent dielectric breakdown (TDDB), Trap generation rate, Weibull distribution.

I. INTRODUCTION

With the advent of high-κ (HK) dielectric films such as HfO_2 as a replacement to silicon oxynitride (SiON) for aggressive equivalent oxide thickness (EOT) scaling according to Moore's Law, reliability assessment of MG-HK stacks required comprehensive studies from an electrical [1] - [5], statistical [6] – [8], theoretical [9, 10] and physical [11] – [14] viewpoint. Based on in-depth analysis by various reliability groups presented in literature, there are two important complexities to be addressed in HK stacks in the context of time dependent dielectric breakdown (TDDB). One of them is the presence of a dual layer dielectric comprising HK and interfacial layer sub-oxide (IL - SiO_x) films. Given a dual layer stack, the sequence of breakdown (BD) has to be determined and it is also essential to find out whether device and circuit failure occur due to a complete stack hard BD (HBD) or multiple soft BD (SBD) events in one of these dielectric layers. Currently, there is no unified understanding on the sequence of BD. While some studies point to the HK layer being the first to percolate [3, 5, 15], others indicate IL to be more vulnerable [1, 16-20]. Since each of these studies are based on very different set of electrical tests, voltage polarity (gate / substrate injection) [21] and analytical techniques, it is hard to objectively assess the robustness and limitations of these findings. The effect of a dual layer oxide stack on the statistical distribution of BD also has to be analyzed. It is clear that the standard Weibull distribution which could very well describe the TDDB phenomenon in SiO_2 / SiON, does not represent the case of HK gate stack failures [20, 22, 23]. The origin of deviations from Weibull trends need to be understood as these are bound to have a big effect on the extrapolated lifetime estimates by many orders of magnitude.

The second complexity is the role played by the microstructure of the high-κ thin film. While SiON is amorphous, HK films tend to be polycrystalline either during the deposition or the annealing step in the fabrication process [24]. While amorphous films tend to have a random defect generation process, polycrystalline films tend to have a higher defect generation rate at the grain boundary (GB) locations relative to the grain [25] – [28]. The GB fault lines with a size of 4-5Å [29] are defective interfaces between crystalline grains and consist of many oxygen vacancy traps even prior to voltage stress. The effect of this localized non-random trap generation in HK films on the statistical distribution of TDDB failures has not been analyzed in-depth yet.

The key objective of this study is to simulate the trap generation kinetics in dual layer HK-IL stacks and probe the statistical nature of the TDDB distribution accounting for the role played by the individual HK and IL layers and the effect of the grain boundary. We use the Kinetic Monte Carlo (KMC) simulation routine here to represent the percolation process. The novelty of the presented approach lies in the use of a thermochemical non-empirical model [30] to describe the defect generation rate (***k***), where the defect is an oxygen vacancy (V_0), as confirmed previously by physical analysis [31, 32], arising from the Si-O / Hf-O bond breakage.

The layout of the paper is as follows. Section II presents an overview of the analytical and simulation models presented in recent literature for HK gate stacks and their assumptions / limitations. This is followed by a description of our KMC algorithm in Section III. We present and discuss the results of

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our simulation model in sufficient detail in Section IV investigating the BD sequence, GB effect, shape of the statistical distribution as well as correlation between IL and HK BD events. Finally, we conclude the study with potential suggestions for further analysis and other possible applications of the model developed.

II. Overview of Current Statistical Models

Various analytical percolation models and simulation routines have been developed in the recent past in an attempt to better describe the statistical nature of breakdown in HK-IL stacks. Each of these models has helped improve our ability to understand and characterize the stochastics and kinetics of the complex multi-layer TDDB phenomenon.

The KMC model presented by Nigam *et. al.* [33] is a pioneering effort to simulating the percolation in the HK-IL stacks. The study accounted for different defect generation rates in the HK and IL layers and explained the non-Weibull or bimodal distribution trends with steeper Weibull slope (β) for low percentile failures. However, the defect generation was only empirically modeled using a power law expression and the exponent (α) for stress induced leakage current (SILC) degradation was assumed to be 0.38 for both the HK and IL layers. Moreover, the study does not decode the individual distributions for the HK and IL times to failure, which may provide us with some additional insight. While the model is fitted to describe the electrical TDDB test data very well, it may be necessary to consider the possibility of the second dielectric layer failing abruptly after the first one percolates during accelerated stress tests, owing to the high voltage stress (exceeding critical field strength), in which case, we may not be studying the intrinsic reliability of the whole gate stack.

The statistical cell-based percolation model proposed by Suňé *et. al.* [34] is a note worthy and commendable effort in being able to analytically describe the bimodal Weibull slope trends in HK-IL TDDB distribution (explicitly considering the exponential saturation of defect generation probability) and it complements the simulation results in Ref. [33] very well. However, a direct extension of the breakdown probability expression from one-layer to two-layer dielectric is questionable because it is necessary to consider the fact that the percolation of the whole stack does not occur as a single catastrophic event. Since the two dielectric films have different robustness to trap generation, their degradation kinetics can be very different. Moreover, the stress experienced by the second layer is not constant (time-dependent two step stress) and it increases after the first layer percolates. In such cases of time-varying stress, use of the standard Weibull statistics may have to be re-examined. In fact, analytical modeling of HK-IL stack failure distribution is complicated by this time-varying stress and it requires more robust reliability theories such as the cumulative damage and load sharing model [35, 36] for accurate modeling of the statistics.

The generic percolation model proposed by Krishnan *et. al.* [37] to describe various possible hypothetical scenarios of defects in an oxide serves as a very useful reference. In their work, the Weibit relationship (W_{BD}) as a function of injected charge (Q) was investigated accounting for the possibility of random defects and pre-existing process-induced traps. They showed analytically that the Weibull statistics ceases to hold true in the presence of pre-existing defects, especially at the low percentile region. However, the analysis did not consider the possibility of localized weak links with high defect concentration, which is representative of the GB region in high-κ films.

With the above models as a motivation and basis, the next section shall describe the KMC algorithm we propose for the dual-layer gate stack, making use of the thermochemical model of bond breaking to represent defect generation.

III. Kinetic Monte Carlo Model

A. Thermodynamics of Trap Generation

Based on physical analysis of the BD spot using electron energy loss spectroscopy (EELS) [31] and the electron spin resonance (ESR) techniques [32], the defect causing percolation in the oxide is identified to be the oxygen vacancy, (V_0). These vacancies are generated due to dislodged oxygen ions from the dielectric structure during bond breaking of Si-O or Hf-O bonds corresponding to the IL and HK layers respectively. The oxygen ions tend to migrate towards the metal gate and are gettered there or they drift to the silicon substrate oxidizing it, depending on the stress polarity [38]. Using McPherson's thermochemical model [30, 39] for bond dissociation, the trap generation rate (TGR), $\boldsymbol{k}$, can be expressed by an Arrhenius relationship in Eqn. (1), using standard thermodynamics, where E_a, p, κ, ν and k_B refer to the field-free activation energy, dipole moment, relative permittivity, vibration frequency and Boltzmann constant respectively. The stress factors here are the electric-field (ξ) and temperature (T).

$$k = \nu \cdot exp\left(-\frac{E_a - p \cdot (2+\kappa)/3 \cdot \xi}{k_B T} \right) = \nu \cdot exp\left(-\frac{E_{a-eff}}{k_B T} \right) \quad (1)$$

TABLE I. Value of the Model Parameters used for the Thermochemical Analysis representing the Trap Generation Rate

Thermochemical Model Parameters	*Value*
Field-Free Activation Energy (SiO_x)	2.34 eV [30]
Field-Free Activation Energy (HfO_2)	4.40 eV [9]
Critical BD Field (HfO_2)	5-6 MV/cm
Critical BD Field (SiO_x)	12-18 MV/cm
Lattice vibration frequency (ν)	10^{13} s^{-1}
HfO_2 Bulk Grain (κ_G)	25
HfO_2 Grain Boundary (κ_{GB})	27-30
Unstressed SiO_x (κ_{IL})	6 [32]
Post Breakdown SiO_x ($\kappa_{IL\text{-}BD}$)	8.5
Dipole Moment (HfO_2)	10.2 eÅ [39]
Dipole Moment (SiO_x, IL)	4.875 eÅ [30]

Our KMC model is based on this equation with different values of material parameters for HfO_2 (HK) and IL as listed above in Table I. The second term in the exponential factor of Eqn. (1) represents the field-induced barrier lowering due to contribution from the dipole moments pointing in a direction opposite to the applied electric field. Collectively, we simplify the expression with a term called the effective activation barrier for bond breaking ($E_{a\text{-}eff}$). The critical BD field of the dielectric can be extracted by solving for the condition $\rightarrow E_{a\text{-}eff}$ = 0eV [39].

The trend of TGR for the two dielectrics as a function of V_g and thickness ratio (t_{HK} : t_{IL}) is plotted in Figs. 1 and 2 for varying IL and HK thickness respectively. The horizontal line represents the case of $E_{a\text{-}eff}$ = 0eV, corresponding to the critical BD field for each of the dielectrics. It can be seen that for all cases, the critical field BD condition is attained first for the IL layer. Moreover, it is important to note that the TGR for the IL is always a few orders higher than that of the HK for all values of V_g up to the IL BD criterion. The criss-cross of the TGR patterns of the HK and IL layer occur for much higher V_g values, where the IL is no longer intact. This implies that the first layer to BD is always the IL layer for all possible combinations of (t_{HK} : t_{IL}) and stress voltage, V_g, based on the material parameters used for HfO_2 and SiO_x, adopted from Refs. [9, 30, 32, 39]. This analysis confirms to us that sequence of BD is universal and that IL is the first to percolate for all possible circumstances given the HfO_2-SiO_x material stack.

We shall now present the KMC algorithm, following which, various simulation results on the statistical nature of HK-IL TDDB distribution can be probed and discussed. It is to be noted in the above analysis that the voltage drop across the HK and IL layers is computed using the standard Gauss law theory [40], assuming zero surface charge.

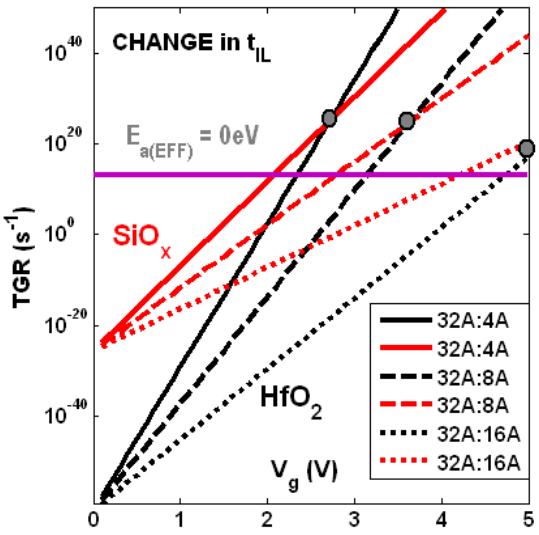


Figure 1. Trap generation rate in the HfO_2 and SiO_x layers for different IL layer thickness (t_{IL} = 4, 8, 16Å) and fixed HK thickness (t_{HK} = 32Å). The black and red line plots correspond to HK and IL respectively.

B. *Monte Carlo Simulation Algorithm*

The flowchart in Fig. 3 provides a complete description of the step-by-step procedure we have adopted for simulating the dynamic percolation process. Initially, we have two separate percolation processes for the individual HK and IL layers to determine which one would break down first at some finite time $t = t_0$. This is followed by a second stage, where the surviving dielectric is simulated starting again from time $t = 0$, such that it has lower stress up to $t = t_0$ and for all $t > t_0$, it is subject to a higher voltage stress at the BD location.

The grain boundary and the breakdown spot region in IL/HK, which are very oxygen deficient, are modeled to have a slightly higher permittivity than their bulk values. This is based on reports which suggest that oxygen deficient dielectrics will have a higher permittivity (κ) value [41, 42]. In fact, SiO_x (κ ~ 6-7) itself has a higher dielectric constant than SiO_2 (κ ~ 3.9) due to the oxygen deficiency [32].

Note that the simulation model here involves the use of two different random numbers for each oxide layer [43]. One is used for random selection of the cell to be classified as a "new defect" and the other one is used for updating the simulation clock. Having presented the model in detail, we will now present the simulation results and discussion in Section IV.

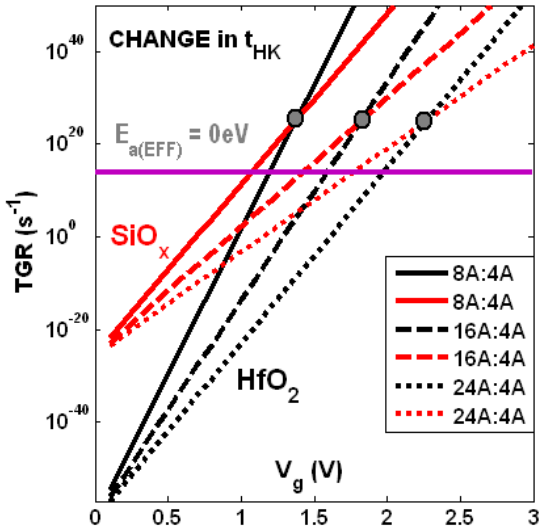
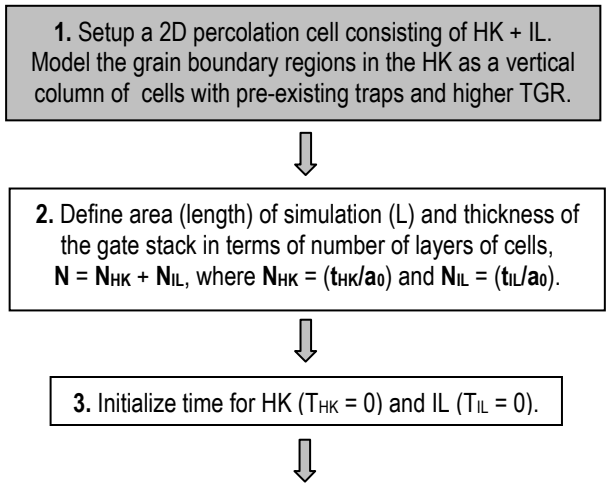


Figure 2. Trap generation rate in the HfO_2 and SiO_x layers for different HK layer thickness (t_{HK} = 8, 16, 24Å) and fixed ultra-thin IL thickness (t_{IL} = 4Å). The black and red line plots correspond to HK and IL respectively.



4. Initialize the TGR for $k_{HK\text{-}B}$, $k_{HK\text{-}GB}$, $k_{IL\text{-}B}$, $k_{IL\text{-}GB}$. The cells in the HK grain (bulk) and corresponding IL region below have a different TGR, as compared to the cells in the HK GB and the IL region below it.

Here HK-B and HK-GB refer to high-K bulk and grain boundary cells, while IL-B and IL-GB refer to the cells in the IL layer directly below HK-B and HK-GB respectively.

⇩

5. Calculate "Total TGR"
For HK : Calculate $k_{TOT\text{-}HK} = [\Sigma k_{HK\text{-}B} + \Sigma k_{HK\text{-}GB}]$.
For IL : Calculate $k_{TOT\text{-}IL} = [\Sigma k_{IL\text{-}B} + \Sigma k_{IL\text{-}GB}]$.

⇩

6. Calculate the accumulative value of the TGR separately for all the HK and IL cells in an order, where p and q are the index for the cells : p = (1, 2, 3, …, N_{HK} × L) and q = (1, 2, 3, …, N_{IL} × L).
$\Sigma k_{HK}(p) = \Sigma k_{HK}(p\text{-}1) + k_{HK}$.
$\Sigma k_{IL}(q) = \Sigma k_{IL}(q\text{-}1) + k_{IL}$.

⇩

7. For any two random numbers between (0,1) :
Find the index "p" and "q" such that
$\Sigma k_{HK}(p\text{-}1) < rand1 * k_{TOT\text{-}HK} < \Sigma k_{HK}(p)$
$\Sigma k_{IL}(q\text{-}1) < rand2 * k_{TOT\text{-}IL} < \Sigma k_{IL}(q)$

⇩

8. Generate defect at cell "p" ⟶ Set $k_{HK}(p) = 0$.
Generate defect at cell "q" ⟶ Set $k_{IL}(q) = 0$.
Increment time for T_{HK} and T_{IL} as follows :
$T_{HK} = T_{HK} - ln\ (rand3) / k_{TOT\text{-}HK}$.
$T_{IL} = T_{IL} - ln\ (rand4) / k_{TOT\text{-}IL}$.

⇩

9. Check for percolation in HK.
Check for percolation in IL.
If no percolation observed : Return to **Step 5**.
If percolation observed, move to **Step 10**.

⇩

10. *IF* $T_{HK} < T_{IL}$ – HK first layer to BD.
Find BD location in HK and modify k_{IL} there.
ELSE-IF $T_{IL} < T_{HK}$ – IL first layer to BD.
Find BD location in IL and modify k_{HK} there.

Here modifying the "*k*" refers to representing an increase in voltage stress in the local region around the BD spot of the first layer. This is done by increasing the permittivity of the BD region as it is highly oxygen deficient.

⇩

11. IL first BD : Re-run the trap simulation only for HK layer from start ($T_{HK} = 0$) in **Step 3** again such that k_{HK} is low (original value) for $T < T_{IL}$ and high for $T > T_{IL}$ at the BD location.

If HK breaks down first, follow the vice-versa.

Continue trap generation in second layer until it percolates. Identify second layer BD location.

⇩

12. Repeat **Steps 1-11** for a sample size of 100-1000 and then carry out analysis of the distribution statistics.

Figure 3. Algorithm showing the step-by-step procedure to set up a KMC routine for trap generation simulation in a dual layer dielectric stack. Note that the whole algorithm involves two stages – first is to determine the initial layer that would break down and the second is to simulate the trap generation in the surviving dielectric accounting for the increased voltage load at the BD location of the first layer. Note that there are four random number generators used in this routine, two each for probabilistic defect identification and simulation time clock update in the HK and IL layers.

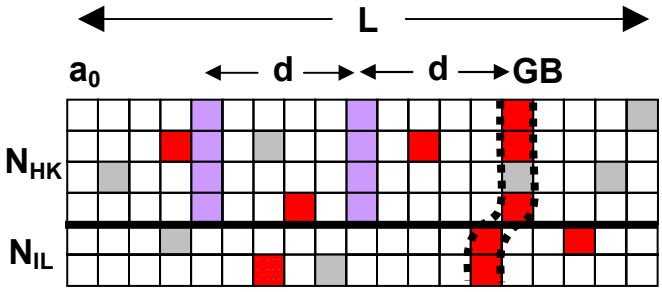


Figure 4. Schematic showing the 2D percolation cell model we have developed for the dual layer gate stack. Based on experimental evidence of the GB size, we consider the GB (purple cells) to be distributed at regular intervals (with spacing "*d*") in the oxide (to keep it simple). This is equivalent to having a random distribution of GB lines for a large area device under test. The parameter, a_0, is the trap size (cell dimension). L is the total length of sample (equivalent to area in a 3D case) and N_{HK} and N_{IL} represent the number of layers of HK and IL in the stack. The grey and red cells represent the process and stress induced traps in the oxide respectively.

IV. Results and Discussion

For the model simulation, we use the square cell structure in Fig. 4 with every cell representing a trap. The length of the cell is taken to be $L = 200$ and the grain size $d = 24$ nm, which is an integral multiple of the assumed trap (cell) size of $a_0 = 8$Å). The value of the grain size is based on statistical evidence from scanning tunneling microscopy (STM) studies on blanket high-κ films [44]. The chosen length of $L = 200$ is equivalent to simulating a device with an area > 10 × 10 nm^2. Every result is based on 300-1000 cycles of trials. In this section, we will first analyze the effect of GB by focusing on pure HK films, which can be considered the ideal stack for future sub-16 nm technology nodes of zero IL (ZIL) logic devices. This

will be followed later by analysis of the dual-layer HK-IL stacks and the correlation of the BD locations in the two films.

A. Statistics of Grain Boundary in Pure High-κ Films

The Weibull plot in Fig. 5 shows the simulated time to failure (TTF) distribution for an (a) amorphous and (b) polycrystalline HfO_2 film (t_{HK} ~ 3.2 nm), with permittivity (κ_{GB} = 26) > (κ_G = 25) which translates to the TGR being ~60 times larger at the GB sites, based on Eqn. (1). While the amorphous stack shows a linear trend in the Weibit scale clearly representative of the standard Weibull distribution, as is the case for SiO_2 and SiON, the polycrystalline microstructure shows convexial trends with steeper low percentile (higher β_{LP}) and shallower high percentile (lower β_{HP}) data. Since the only parameter change in these two cases is $\kappa_{GB} \neq \kappa_G$, it can be implied that non-uniform localized trap generation leads to the convexial TTF distribution trends. When the BD location was monitored using the simulation, it turns out as shown in the histogram plot of Fig. 6(c), that all the BD events occurred at the GB. For the amorphous film, since TGR is uniform throughout, we observed a uniform distribution of the BD location all along the film (Fig. 6(a)). For intermediate cases, wherein the TGR is say only 4 times larger at the GB (corresponding to κ_{GB} = 25.3), some BD events may still occur in the grain bulk as illustrated by Fig. 6(b). The extent of defectivity in the GB therefore plays a major role in governing the shape of the statistical distribution.

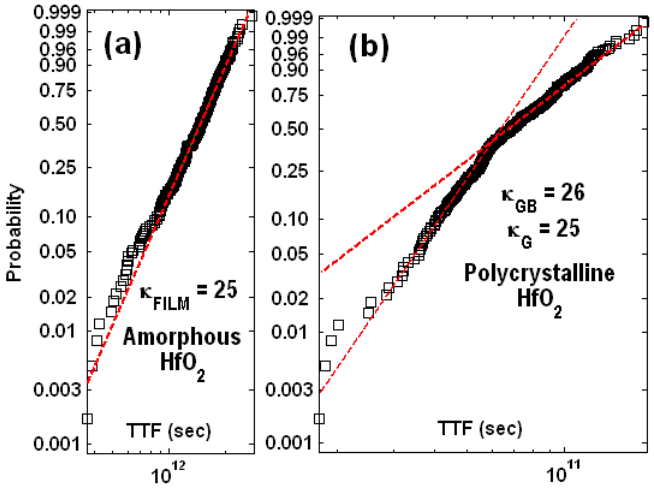


Figure 5. Simulated failure time distribution at V_g = 1V for (a) amorphous (κ = 25) and (b) polycrystalline (κ_G = 25, κ_{GB} = 26) HK thin film of thickness, t_{HK} = 32Å. Higher localized trap generation rate at the GB causes the distribution to be non-Weibull.

In Fig. 7, we intentionally induced traps in a random fashion at time t = 0 in the GB with a probability (p_{GB}) where p_{GB} = 5%, 15% and 25% and simulated the percolation process. It is to be noted that a low percentile "extrinsic" shallow tail (with very low β_{LP}) turns out for increasing values of p_{GB}. This implies that for a very defective poly-HK film, the low percentile distribution can be very different with a concave shape and very few stress induced traps may be needed to induce breakdown. However, such trends are generally not observed in accelerated stress tests. Therefore, it is possible that p_{GB} < 5% in processed polycrystalline HK films, corresponding to the convex trend of TDDB data in Fig. 7 (see data plotted in red). The relationship between β and t_{ox} is an important one for any oxide breakdown study [45, 46]. This relationship was also probed (considering V_g = 0.5V) using our simulation routine for amorphous and polycrystalline samples, as plotted in Fig. 8.

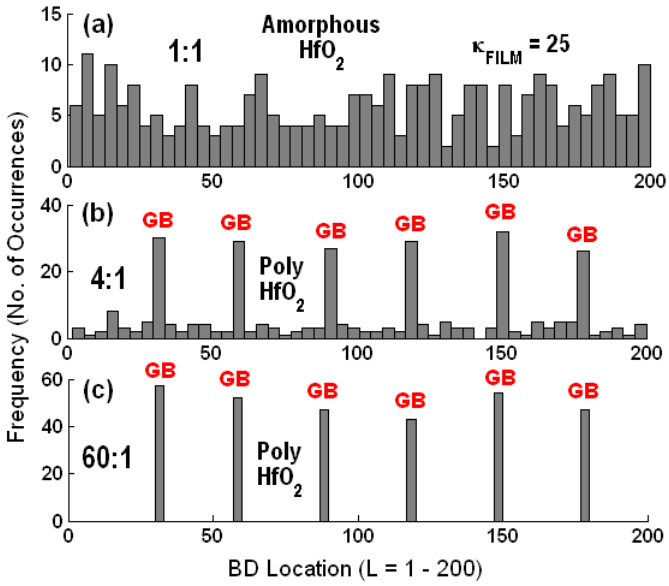


Figure 6. Histogram plot of the BD location in the HK film (t_{HK} = 32Å) for different trap generation rate ratio of GB to bulk degradation – (a) 1:1 (amorphous), (b) 4:1 and (c) 60:1. As expected, BD occurs preferentially at GB locations as the ratio increases by a factor of 10.

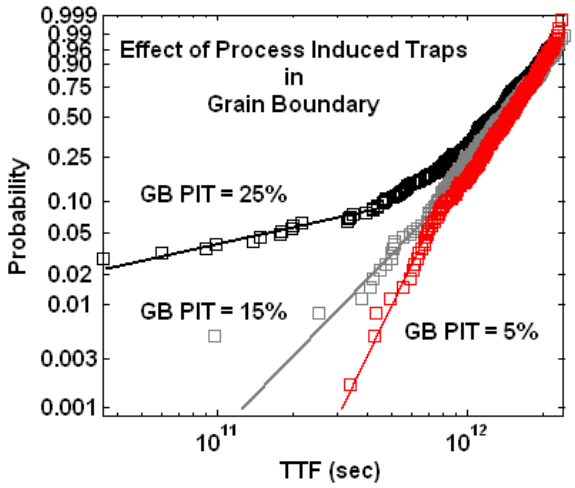


Figure 7. Failure distribution plot of the HK film (t_{HK} = 32Å) at V_g = 1V for different probability of process induced traps (defectivity) in the GB → p_{GB} = 5%, 15% and 25%.

There are a few key inferences from this set of data. As expected, the value of β is greater for the amorphous film since more traps have to be generated to cause percolation, in the absence of process induced traps that tend to segregate at the GB, if it had existed. The slope of the linear fitting gives an SILC time exponent of α ~ 0.5, which is larger than typically reported values of 0.26-0.40 [47] – [49]. If the defect

count (density) during the simulation is plotted with time on a logarithmic scale and force-fitted using a power law, we obtain an "effective" time exponent ~ 1 (not shown here for brevity), which is similar to experimental reports by Cartier *et. al.* [50]. In the β - t_{ox} trend, the best fit curves both show a non-zero y-intercept (γ) [37], indicative of more traps needed for breakdown (N_{TOT}) than predicted by the percolation model, which can be represented by Eqn. (2), where N' is the additional number of traps required for percolation. This is a deviation from the conventional understanding where we generally tend to observe a zero intercept when extrapolating the β - t_{ox} experimental data. The value of $N' \sim 1$ for poly and $N' \sim 2$ for amorphous films. One possible interpretation for this is that the higher number of traps needed for breakdown could be associated with the interface traps of HK with silicon. In other words, in addition to the bulk traps, additional interface traps are also needed for the percolation failure to occur. The observed non-zero y-intercept also explains why a dielectric with only a single layer of cells would still need around two traps (one bulk + one interface) for it to breakdown. Other plausible explanations include the possibility of inclined percolation paths that would need more traps for weakest link formation or misalignment of the traps. All these possibilities are illustrated by the cartoon in Fig. 9.

$$\beta = \alpha \cdot \left(\frac{t_{ox}}{a_0}\right) + \gamma = \alpha \cdot \left(\frac{t_{ox}}{a_0} + \frac{\gamma}{\alpha}\right) = \alpha \cdot \left(N + N'\right) = \alpha \cdot \left(N_{TOT}\right) \quad (2)$$

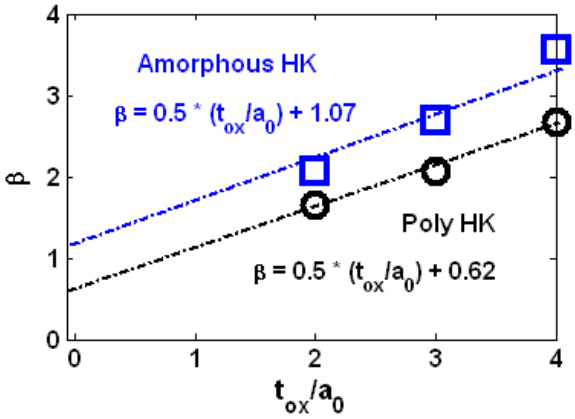


Figure 8. Trend of Weibull slope (β) versus oxide thickness (t_{ox}) for amorphous and polycrystalline HK dielectric films. A non-zero y-intercept is observed in both cases, with the amorphous HK having a higher intercept.

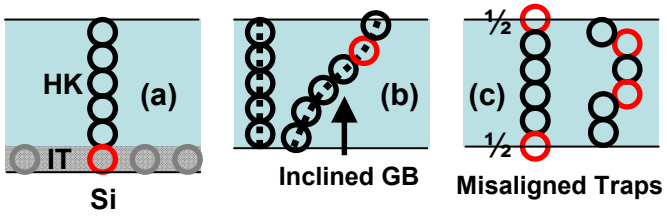


Figure 9. Hypothetical scenarios that could explain the non-zero positive y-intercept for β - t_{ox} relationship in Fig. 8. The additional trap needed could be (a) interface (IT) related, (b) due to inclined non-vertical GB fault lines or (c) misalignment of traps.

The effect of area scaling is presented in Fig. 10 for the polycrystalline HK film, considering four different areas of L = 100, 200, 2000 and 20,000 cells. It is interesting to note that while the data show convex trends for low L, the distribution is almost Weibull for larger areas of L = 2000 and 20,000. While area scaling may not be applicable for very small device area due to the random distribution of GB where some devices may have many of these fault lines while others may have none, it is valid for large area devices considering the average distribution of GB across the HK film. As an ideology, we can imagine the HK film to consist of two parts, one comprising GB region and the other involving the bulk grains. Taking this perspective, it is easy to infer the validity of area scaling for HK films, because larger area films will have proportionately more GB columns on the average. The inset in Fig. 10 shows the increase in β for larger device area. Such trends have been reported previously in HK gate stacks [23, 33, 51] and it can again be attributed to the non-random defect generation in poly-HK. In the presence of many weak-link GB columns, we would expect the failure distribution to be tighter with less spread which reflects in the higher β for larger area devices. It is to be noted that the Weibit value corresponding to slope transition observed in our study (when normalized to 1μm^2) would be much higher than that reported in Refs. [19] and [23], implying that the convexial deviation of TTF data is observed for a larger proportion of our simulated samples.

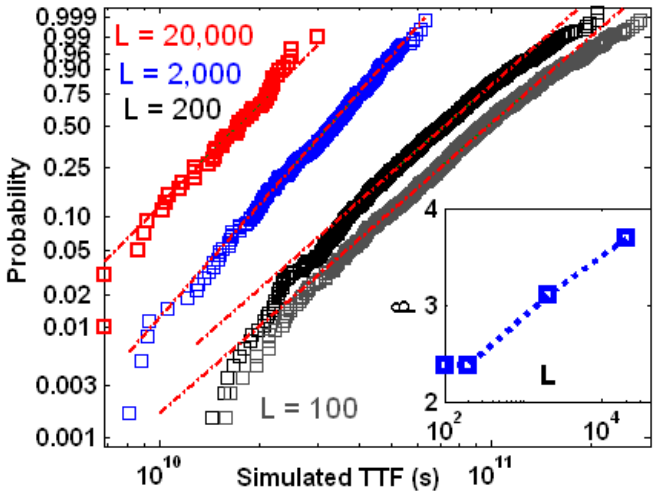


Figure 10. Simulated TTF distribution for poly-HfO_2 film with t_{HK} = 32Å at V_{op} = 1V for four different device areas of L = 100, 200, 2000 and 20,000 cells. Area scaling is only valid for large device areas corresponding to L > 2000. Although not shown here, for amorphous films, area scaling is always valid for all cases. The inset shows a plot of the Weibull slope (β) increasing for larger area devices. It is expected to saturate for larger device areas, which we did not simulate due to prolonged computational time.

B. Statistics of Dual Layer Gate Stack Breakdown

Having discussed the various non-ideal factors in HK films and their impact on the breakdown distribution, we now take a look into the dual layer gate stack comprising HfO_2 and sub-stoichiometric SiO_x ($x < 2$). Although ZIL stacks are desired from an extreme equivalent oxide thickness (EOT) scaling point of view, it is practically difficult to achieve a purely HK

film considering the trace amounts of oxygen in the deposition or anneal ambient that lead to very thin IL layers of 3-8Å in thickness. Based on our TGR trends for the HK and IL layer for various t_{HK} : t_{IL} thickness combinations and gate voltage conditions, we were able to infer previously from Figs. 1 and 2 that this rate is a few orders higher in the IL layer for all cases. We further confirm this in Fig. 11 for (t_{HK} = 32Å, t_{IL} = 16Å), which plots the ratio of T_{HK} / T_{IL} for a wide range of V_g, where T_{HK} and T_{IL} refer to the time it would have taken for the first percolation event to occur in the HK and IL layers respectively, if they were subjected to voltage stress levels of V_{HK} and V_{IL}, determined by the Gauss Law. As expected, T_{HK} / T_{IL} >> 1 and the ratio is as high as 10-20 orders of magnitude for practical voltage conditions.

We then simulate the TTF distribution for the IL and HK layers in Fig. 12, considering the higher voltage drop across the HK layer after IL BD, again using Gauss Law. When the IL layer breaks down, it is still in the SBD regime, as the HK layer is still intact. For the case of SBD, the percolated IL region is not purely Si ($x \sim 0$) [11], rather it is only more oxygen depleted than the initial unstressed SiO_x. Therefore, we model this by assuming the local permittivity of the percolated SiO_x region to be ($\kappa_{IL\text{-}BD} \sim 8.5$) > ($\kappa_{IL} \sim 6$).

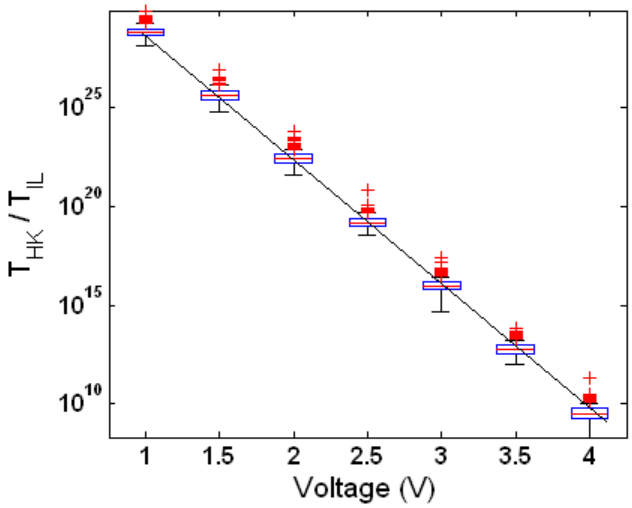


Figure 11. Plot of the ratio of time to first HK and IL break down in a dual layer gate stack comprising 32Å HfO_2 and 16Å SiO_x for a wide range of gate voltage stress conditions (each 300 simulation trials). It is clear that lifetime of the HK layer is many orders of magnitude larger than that of the IL layer.

For the IL TTF distribution, the poly-HK stack shows significant non-linearity below the 10% probability line as indicated by the black dot in Fig. 12(a). The amorphous film shows less convexity and is almost linear except for slight deviations. The non-linearity is again due to the GB defects in the HK film. The IL layer experiences higher voltage stress directly below the low resistivity GB regions, as compared to the other regions below the bulk grains. As an example, considering the thickness combination of (t_{HK} = 32Å, t_{IL} = 16Å), we can compute using Gauss law that $V_{IL} = 0.77V_g$ at the GB and $V_{IL} = 0.735V_g$ in the bulk, for κ_{GB} = 30 and κ_G = 25. The mean lifetime for the HK layer is about 20 orders higher than that for the IL layer.

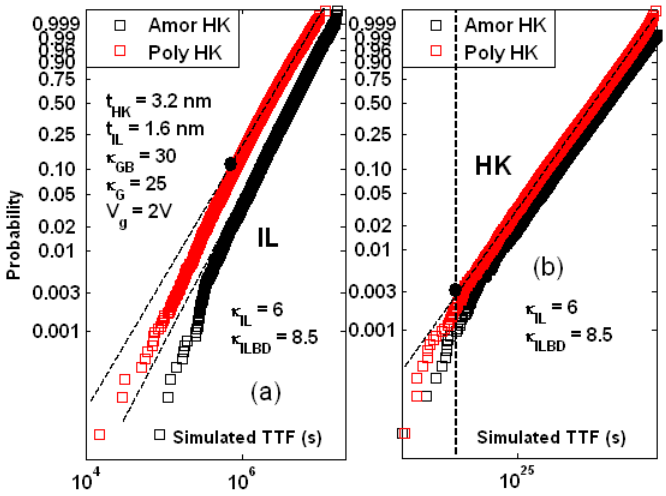


Figure 12. Weibull plot of simulated time to failure for a HK-IL dual layer gate stack at V_g = 2V, comprising 32Å HfO_2 and 16Å SiO_x. The figure on the left is for the IL first BD, while the figure on the right is for the HK BD. Data in red and black correspond to polycrystalline and amorphous HK films.

This suggests that it may not be feasible during nominal operating conditions of an integrated circuit to observe a sequential breakdown of the IL and HK films in logic devices. Fig. 13 is a histogram plot of the IL-BD location which is random for the amorphous HK film and increasingly localized for the polycrystalline microstructure. These results are similar to that presented earlier in Fig. 6.

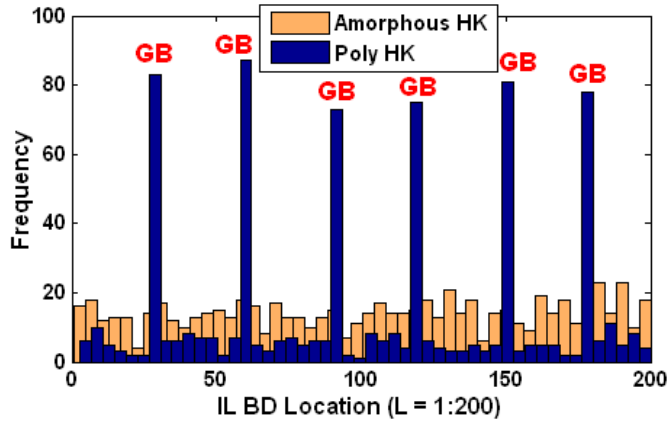


Figure 13. Histogram plot of the first layer (IL) break down location for the amorphous and polycrystalline HK based dual layer gate stack with t_{HK} = 32Å and t_{IL} = 16Å. First layer BD in the amorphous stack is fully random as expected. As for the poly film, it is mostly confined to the regions below the GB fault lines in the HK.

There are only two possibilities for circuit level failure of a HK based gate stack. One possibility is the sequential BD of the IL and the HK layer followed by a progressive analog degradation of the percolation path to high leakage current values, similar to that observed in SiO_2 / SiON. The other possibility is the nucleation of multiple IL SBD events across the circuit such that the summation of the leakage currents from these BD spots causes the circuit leakage to exceed the standard criterion of 10μA at V_{op} = 1V. Ideally, it may also be possible to observe a competition of single BD spot

progressive degradation and multiple SBD evolution. In order to evaluate these possibilities, we simulated the likelihood of multiple IL BD events, as shown in Fig. 14 for t_{HK} : t_{IL} = 32Å : 16Å. While the statistics is non-Weibull, our simulation shows that the 1% time to failure for 10 SBD events is only an order of magnitude higher than that taken for the 1st SBD event. For increasing number of BD events, the distributions get closer to each other and therefore, even for 1000 BD events (considering nano-ampere level leakage from every IL SBD spot), the lifetime enhancement as compared to the 1st BD event will not be more than a factor of 1000. This result can be estimated using Eqn. (3) [52], which is an approximation for the non-Weibull failure stochastic that we examine here. The symbols *K, F* and *W* refer to the number of BD events, failure percentile and corresponding Weibit value (*ln(-ln(1-F))*) respectively. Since T_{HK} / T_{IL} >> 10^{10} and $T_{IL\text{-}BD}(1000)$ / $T_{IL\text{-}BD}(1)$ ~ 10^3, we can convincingly conclude that circuit level failure only occurs by multiple IL SBD events. There is no possibility of a HK BD event under nominal operating conditions. Progressive BD is also not apparent in the case of IL-only BD events because the leakage current (nA level) and thermal joule heating is very minimal to cause any wear-out of the percolation path. Only if the percolation event had occurred through the whole dual layer stack would the wear-out effect be dominant. Fig. 15 summarizes our understanding of how the dual layer stack based integrated circuit is likely to breakdown at V_{op} = 1V. Our electrical tests show a complete HK-IL stack BD only because we test very small devices at accelerated stress conditions and therefore, forcibly cause the HK layer to percolate. Another key result to take note is that the voltage drop across HK before and after BD only changes by about 0.08V_g for a change in κ_{IL} from 6 to 8.5 (based on Gauss Law). It is not appropriate to simply assume that the entire gate voltage would drop across the HK layer even after the IL breaks down.

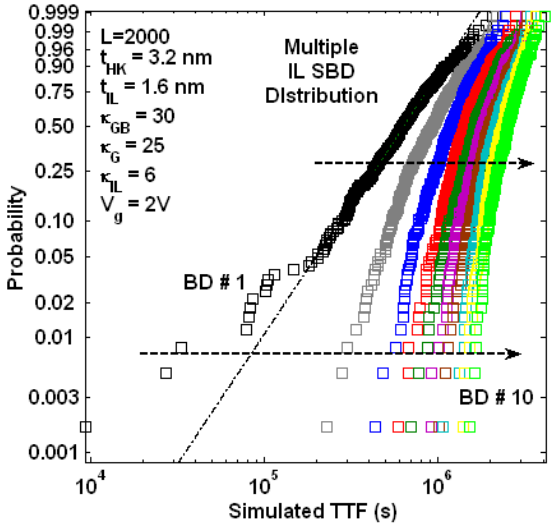


Figure 14. Statistical distribution of the time taken for multiple breakdown spot evolution (up to 10 BD events) in the IL layer simulated for V_g = 2V using the proposed thermochemical KMC model. The distributions are non-Weibull and β increases for larger number of BD events, as justified previously in Refs. [51] - [53].

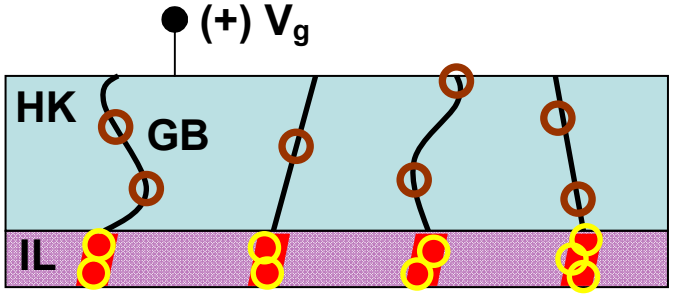


Figure 15. Illustration showing the most plausible scenario of circuit level gate stack failure which will involve multiple IL SBD events that are uncorrelated laterally and localized around the grain boundary contours in the polycrystalline high-κ film.

$$\frac{T_{BD-K}(F)}{T_{BD-1}(F)} = (K!)^{1/K\beta} \cdot exp\left\{-W\left(\frac{K-1}{K\beta}\right)\right\} \qquad (3)$$

Using our simulation model, we further investigated the area scaling property for IL BD as shown in Fig. 16(a). The area scaling law is valid for the first layer BD event. However, since the HK and IL breakdown events tend to be correlated [7], as shown in Fig. 16(b), area scaling is generally not applicable for the HK [19] (which anyway does not fail for practical time durations).

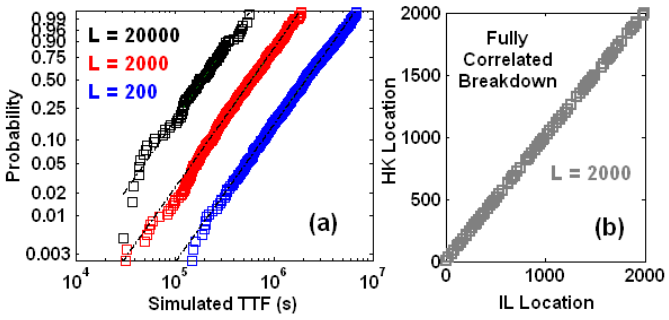


Figure 16. (a) Time to failure distribution in a stack with N_{HK} = 4 and N_{IL} = 2 at V_g = 1V for first layer IL BD shows validity of area scaling rule. (b) The scatter plot of HK and IL breakdown location generally shows perfect correlation, which implies that area scaling is not applicable for the second layer HK BD.

Considering that GB tends to be the favored region for segregation of oxygen vacancies even prior to electrical stress [29], we decided to investigate the dependence of GB defectivity on the degree of correlation in the IL and HK BD locations, as shown by the scatter plot in Fig. 17. Traps were randomly placed in the GB with a probability, p_{GB} = 0%, 5% and 20% at time zero. With increasing process induced defects in the GB, there is less correlation in the IL and HK BD locations. This is because although the HK region above the IL BD experiences a higher voltage stress of about 0.08V_g relative to the other GB locations, it is possible that there are some GB lines that already have many intrinsic traps and therefore, very few additional traps are needed for BD. In such cases, the HK may percolate at a location uncorrelated to where the IL broke down (Fig. 17).

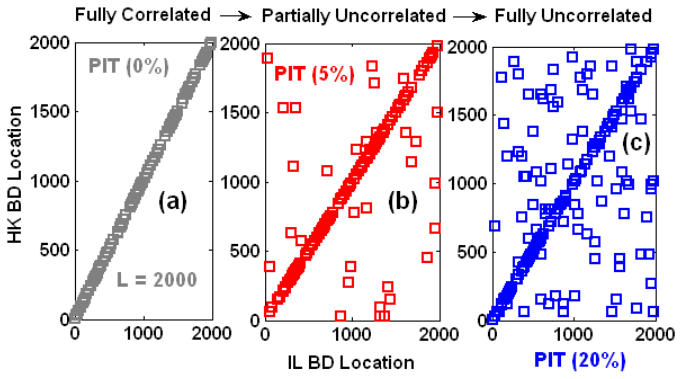


Figure 17. Scatter plot of IL and HK breakdown locations in a stack with N_{HK} = 4 and N_{IL} = 2 as a function of the GB defectivity (p_{GB}). With higher density of process induced traps, it is possible for the HK BD location to be completely uncorrelated to the percolation in the IL.

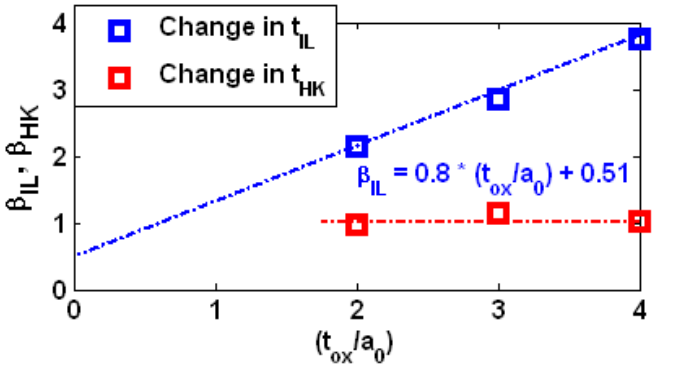


Figure 18. Plot of the $\beta - t_{ox}$ relationship (V_g = 2V) for different values of t_{HK} and t_{IL} in the dual layer gate stack. While β_{IL} shows a linear relationship with t_{IL}, there is no dependence of β_{HK} on t_{HK} because BD is only controlled by the IL layer.

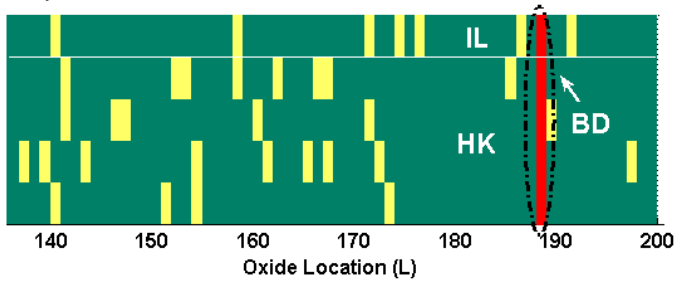


Figure 19. Percolation map illustrating a typical scenario of trap generation in a HK-IL stack and the correlated IL → HK BD spot at the location L ~ 188.

The β - t_{ox} relationship was also investigated for the dual layer stack by changing the IL thickness (16Å, 24Å, 32Å) for fixed t_{HK} = 32Å and then changing the HK thickness (16Å, 24Å, 32Å) for a fixed t_{IL} = 16Å. From these simulation trials, as shown in Fig. 18, we observe a linear dependence of $\beta - t_{IL}$ with a positive y-intercept which can be explained based on the logic presented previously. However, there is no dependence of β on t_{HK} which may be due to the localized region of higher stress and BD in the HK. This again confirms that the breakdown of the stack is governed only by the IL layer and not the HK. Similar trends of β - t_{HK} insensitivity have been reported by Kauerauf *et. al.* [54] and Lee *et. al.* [55] using electrical tests results and the trend is attributed to extrinsic weak link defects in the HK, which we refer to as the grain boundary in this study. Fig. 19 shows a typical percolation snapshot of one of the simulation trials for an L = 200 small area device, where the HK-IL correlated breakdown can be clearly observed.

V. Conclusion

In this study, we have presented a comprehensive analysis of the statistics of polycrystalline high-κ films (in comparison to amorphous films) and dual layer HK-IL gate stacks. The novelty lies in the use of a physics-based thermochemical Monte Carlo model to represent the time-dependent oxygen vacancy defect generation process in SiO_x and HfO_2 dielectrics. The key inferences from this study and their implications on future high-κ gate stack technology are summarized below.

- Non-Weibull statistics in HK-based stacks is due to the locally enhanced trap generation rate in the defective GB regions.
- For all combinations of t_{HK} : t_{IL} and voltage stress conditions, the TGR for SiO_x is a few orders of magnitude higher than that of the HfO_2.
- The SiO_x dielectric (IL) is the first to breakdown in the dual-layer gate stack.
- Circuit level failure of dual layer stacks can only occur by multiple SBD events in the IL layer. Sequential BD of the IL and HK layers is not feasible, considering that the HK layer is very robust and has a very low defect generation rate.
- Generally, breakdown in the IL and HK are correlated. However, uncorrelated IL and HK BD events are possible if the GB fault lines are already very defective prior to electrical stress.
- The Weibull slope – oxide thickness trends show a non-zero positive y-intercept which can be indicative of the non-aligned traps in the percolation path or the role played by the interface traps, which we did not explicitly address in our analysis.

It would be interesting to further build-up the proposed KMC model here to account for the other sources of defect generation such as anode hole injection and hydrogen release [56, 57] and investigate whether the inferences on the breakdown sequence and statistical distribution are affected in any way. As mentioned earlier, our choice of the thermochemical description here is based on solid physical analysis evidence of the presence of oxygen vacancies in the percolation path [11]. Further work is needed to extract the material parameters such as {κ, E_a, p} using atomistic simulations and electrical characterization and compare our simulation results with experimental TDDB distributions for different gate stack thickness combinations. The model can be improved by removing the assumption of the same trap size, a_0 (8Å) for both the HK and IL. Considering that the trap size depends on the energy depth of the V_0 defect in the dielectric material, which is different for SiO_x and HfO_2 , the value of a_0

may be different for these two materials [33]. The proposed model also finds application in understanding the switching statistics and variability in resistive random access memory devices considering that switching is analogous to breakdown and its recovery in high-κ insulators.

The analysis presented here is complementary to our previous efforts of using analytical models to describe the statistical nature of TDDB in GB (HK-only) [58] and HK-IL gate stacks [59]. Use of the KMC simulation routine is an easier and more effective approach to understanding the statistics and dynamics of time dependent defect generation, as compared to the use of analytical models. It helped us in decoding the separate β values and lifetime for the HK and IL.

Our results clearly indicate that grain boundary microstructure can be detrimental to the gate stack performance (high leakage due to trap-assisted tunneling) and TDDB reliability and it complicates the statistical distribution as well. Therefore, caution has to be exercised in using Weibull stochastics for reliability predictions and extrapolation for HK-based stacks. It is worth noting that for future extreme-EOT scaled devices with ultra-thin HK films < 2-nm, nucleation of GB may not be thermodynamically feasible because the crystallization temperature for ultra-thin films may be exceed the standard temperature annealing conditions. In such cases, the analysis may become simpler and straight-forward bringing back the usefulness of the standard Weibull analysis.

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