Understanding Metal Oxide RRAM Current Overshoot and Reliability Using Kinetic Monte Carlo Simulation

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Abstract – A Kinetic Monte Carlo (KMC) numerical simulator is developed for metal oxide resistive random access memory (RRAM). In this work, substantial improvements are made on the stochastic model in [1] by including multiple conduction mechanisms, local field and local temperature profile, and tracking of the individual oxygen migration path. The improved simulator shows extended capability to study a full set of RRAM characteristics such as set/forming current overshoot, endurance, and retention, etc. The simulations suggest that 1) eliminating the forming process and decreasing the parasitic capacitance is required for minimizing the overshoot effect and reducing the reset power consumption; 2) the degradation of endurance can be explained by oxygen escaping from the electrode during cycling; 3) the oxygen migration barrier can be extracted from the retention baking test over a suitable temperature range.

I. Introduction

Metal oxide RRAM is a promising candidate for future non-volatile memory application [2-5]. The switching mechanism has been attributed to the formation/rupture of conductive filament (CF) with oxygen vacancies [6-9]. To study the substantial switching variability of HfO_x RRAM, we developed a stochastic model in [1], and suggested that the variability originates from the random oxygen vacancy (Vo) generation/recombination and oxygen ion (O^{2-}) migration processes. Besides the variability issue, understanding the set/forming current overshoot [10] and retention/endurance degradation [11] mechanisms are also required for optimizing RRAM characteristics. In this work, we further improve our stochastic model by taking more physical effects into account, and aim to gain insights on the evolution of CF configuration during the overshoot transient period and during the endurance cycling and retention baking tests.

II. Model and Simulation Description

For the typical bipolar switching RRAM, during the forming/set process (transition from high resistance state (HRS) to low resistance state (LRS)), O^{2-} are pulled out from lattice and Vo are generated and form CF connecting both electrodes (Fig.1). During the reset process (transition from LRS to HRS), CF is ruptured by the recombination of Vo with the O^{2-} that migrate from the oxygen reservoir at the electrode/oxide interface (Fig. 2), thus a tunneling gap is formed between the electrode and the residual CF. The previous stochastic model [1] considers that trap-assisted-tunneling (TAT) is the dominant conduction mechanism at low bias regime for the high resistance state (HRS) in HfO_x RRAM, in which case that the electrons are in the localized states where Vo are far away from each other. In this work, two more conduction mechanisms are added into the simulator (Fig. 3): the FN tunneling at high bias regime for HRS, and the metallic conduction at low resistance state (LRS) in which case that the electrons are partially in the extended states where Vo are very close to each other. The metallic conduction is implemented by a resistor network model [12] composed of non-linear resistors with resistance that exponentially depends on the distance between adjacent Vo. Fig. 4 shows the KMC simulation flow. Given a CF configuration, the current is first calculated. Then the local field and local temperature is given by the resistor network and the Fourier heat transfer equation, respectively. Finally, the CF configuration is updated using a KMC method [1] by calculating the event probability of the Vo generation/recombination and O^{2-} migration based on the activation energy of these processes. The local temperature and local field play an important role for determining the CF configuration because the event probability is both field and temperature dependent. The evolution path of every Vo and O^{2-} in the oxide matrix is traced. The simulations are performed on a 2D matrix. Fig. 5 shows the I-V curve of the simulated device with gap ~1nm. Multiple conduction mechanisms contribute to the total current, and the total current exponentially decreases with increasing the gap distance (Fig. 6). Fig. 7 shows an example of the simulated local electric potential in HRS with a gap between top electrode and residual CF. The field is enhanced at the gap region, thus the CF tends to reconnect there during the next set process. Fig. 8 shows an example of the simulated local temperature in LRS when CF connects both electrodes. The raised temperature enhances the O^{2-} migration during the next reset process. The raised temperature is only noticeable in LRS because the heat generation in HRS is negligible.

III. Simulation of Current Overshoot

Current overshoot in RRAM refers to the experimental observation that the reset current is larger than the forming/set compliance current [10]. Fig. 9 shows the simulated I-V with overshoot effect for three cases: 1) forming with a RC time constant τ=100 ns; 2) forming with τ=10 ns; 3) set with τ=100 ns. (Note 1 pF parasitic capacitance and 100 kΩ R_{on} can lead to 100 ns τ). Due to the parasitic capacitance, the voltage dropped on RRAM cannot follow the abrupt resistance change. Instead, it exponentially decays after the compliance current is reached (Fig. 10). Therefore, the transient current may achieve a level higher than the pre-defined compliance current (Fig. 11). It is noted that the overshoot is most remarkable for case 1): forming with larger τ (Fig. 11). To understand what happens inside the RRAM cell during the overshoot period, the CF configurations of the three cases are tracked: For a fresh cell, a few intrinsic Vo (in pink color) exist at the grain boundary [13] (Fig. 12). At the onset moment for case 1), the O^{2-} (in blue color) start migrating towards the top electrode which is positively biased (Fig. 13). At the end of the overshoot period, the CF grows wider laterally (Fig. 14), suggesting that more Vo are undesirably generated due to the high voltage and high temperature during the overshoot period. Fig. 15 & 16 show the CF configuration at the onset moment and at the end of the overshoot period for case 2): the smaller τ as compared to case 1) effectively shortens the high voltage and high temperature period, thus the overshoot is suppressed with limited CF lateral growth. Fig. 17 shows the CF configuration after the reset with the case 1): the O^{2-} at the interface migrate back and partially rupture CF. Fig. 18 & 19 show the CF configuration at the onset moment and at the end of the overshoot period for case 3): only a portion of the CF tip is connected to the electrode during the next set process, and the overshoot is also suppressed as compared with the initial forming process due to a lower voltage during the overshoot transient period, although the overshoot period length is the same as case 1). Experimentally [14], the reset current after the 1^{st} set are reduced as compared with the reset current right after the forming (Fig. 20). This is because of the reduced overshoot effect in the set as compared to the overshoot of the forming process. To summarize, eliminating the forming process and decreasing the parasitic capacitance by integrating the RRAM cell with a selection transistor or a current limiter with a saturating I-V characteristics is helpful for overcoming the overshoot problem.

IV. Simulation of Reliability

Our simulator can continuously cycle the device, and the DC I-V curves, resistance distribution and switching voltage distribution during the cycling as shown in Fig. 21, 22 & 23 aiming at reproducing the experimental data in [14]. During the endurance test [14], the HRS resistance decreases with the cycling (Fig. 24). To shorten the simulation time, the endurance simulation is performed at 125 ^{o}C (Fig. 25), which results in a faster degradation of HRS as compared with the endurance simulation at room temperature (Fig. 26). The number of available O^{2-} in the cell keeps decreasing during the cycling due to an enhanced escaping rate out of the cell top boundary at 125 ^{o}C (Fig. 27), and eventually there are insufficient O^{2-} for recombining Vo, and the device gets stuck at LRS (Fig. 28). The O^{2-} that leak to the top electrode such as TiN may bond with the TiN to form TiON layer [15] thus cannot migrate back. Our simulator can also project the retention behavior versus time (Fig. 29). The LRS resistance increases gradually during a high temperature baking test. The LRS failure time distribution at three baking temperatures is shown in Fig. 30. The slope of extracted mean failure time vs. 1/kT agrees well with O^{2-} migration barrier parameter (~1.3 eV) used in the simulation (Fig. 31), which suggests that the LRS retention failure is caused by the O^{2-} migration from the interfacial oxygen reservoir. When the LRS fails, the tip of CF is ruptured by O^{2-} migration back from the interface (Fig. 32).

V. Conclusion

The key achievements in this work include: 1) the evolution of CF configuration during the current overshoot period, endurance cycling and retention baking tests is investigated; 2) eliminating the forming process and decreasing the parasitic capacitance is suggested to be beneficial for minimizing the current overshoot effect; 3) the degradation of endurance is attributed to the oxygen escaping from the electrode; 4) the oxygen migration barrier can be extracted from the retention tests performed at various temperatures. This paper provides new understandings of the current overshoot problem and reliability degradation mechanism, and sets up a platform to study a full set of RRAM characteristics including the variability in the DC sweep, pulse transient, endurance, and retention properties.

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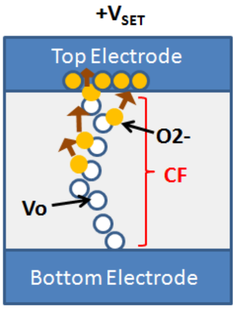

Fig. 1. During the set process, O^{2-} are pulled out from lattice and migrate towards interface and Vo are generated and form CF connecting both electrodes.

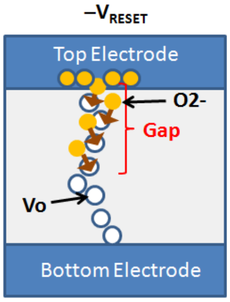

Fig. 2. During the reset process, CF is ruptured by recombination of Vo with the O^{2-} that migrate from the interfacial oxygen reservoir, and a tunneling gap is formed.

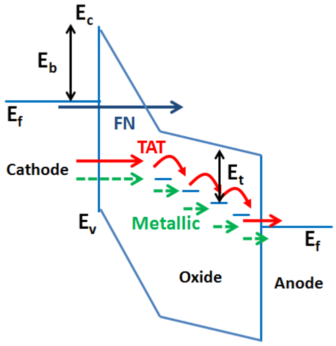

Fig. 3 Multiple electronic conduction mechanisms through the RRAM oxide stack: Trap-assisted-tunneling (TAT), FN tunneling, and metallic conduction.

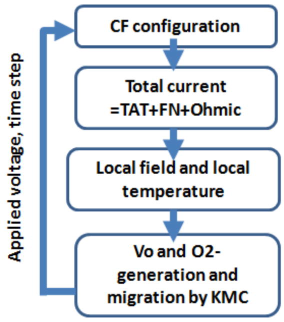

Fig. 4 Flow chart of the Kinetic Monte Carlo (KMC) simulator. It has the current solver, the local field and temperature solver, and the Vo and O^{2-} evolution tracker by KMC.

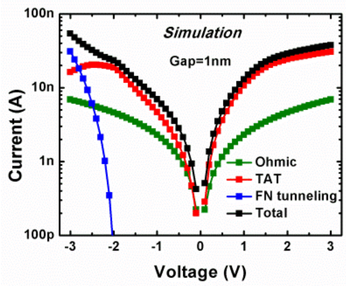

Fig. 5 Conduction components of the simulated I-V curve of a single 1D Vo chain in RRAM cell with 1nm tunneling gap. KMC Vo and O^{2-} tracker is turned off.

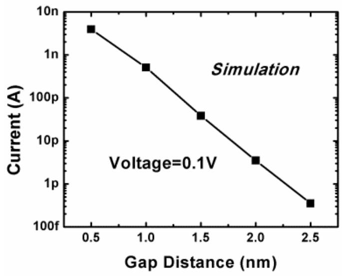

Fig. 6 The simulated dependence of total current on the tunneling gap distance between the CF tip and the electrode.

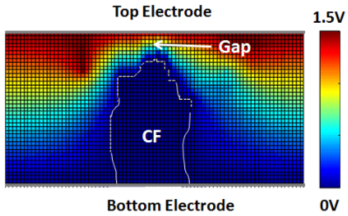

Fig. 7 The simulated local electric potential in HRS with a gap between top electrode and residual CF. The field is enhanced at the gap region, thus the CF tends to reconnect there during the set.

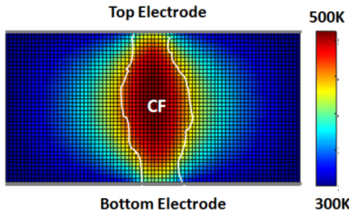

Fig. 8 The simulated local temperature by solving the Fourier heat conduction equation in LRS when CF connects both electrodes. The raised temperature enhances the O^{2-} migration during the reset.

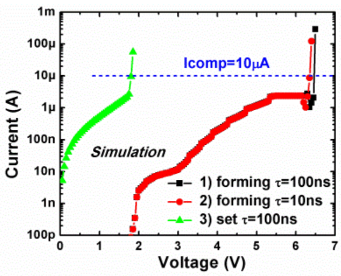

Fig. 9 Simulated I-V curves with overshoot effect for 3 cases: 1) forming with τ=100ns; 2) forming with τ=10ns; 3) set with τ=100ns.

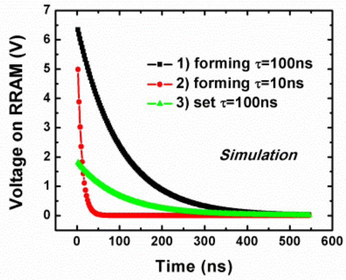

Fig. 10 Simulated voltage drop on the RRAM as a function of time during the overshoot period for the same cases as in Fig. 9.

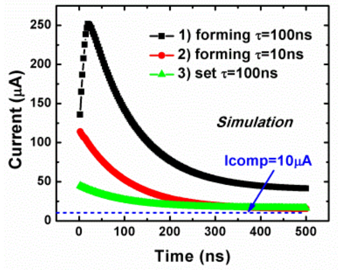

Fig. 11 Simulated current during the overshoot period for the same cases as in Fig. 9. Overshoot is observed for case 1).

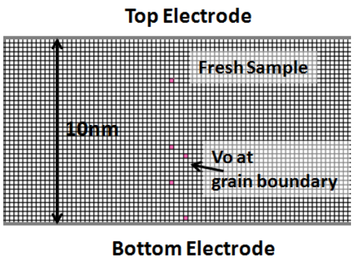

Fig. 12 Initial Vo distribution along a grain boundary in the as-fabricated RRAM cell. Pink dots are Vo.

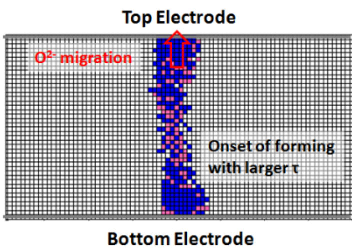

Fig. 13 Vo (pink) and O^{2-} (blue) distribution at the onset moment for case 1): forming with τ=100ns, corresponding to the **black** symbol in Fig. 9.

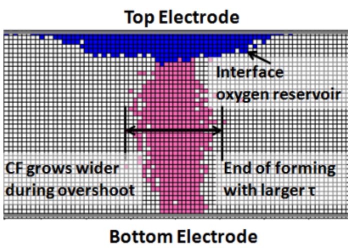

Fig. 14 Vo (pink) and O^{2-} (blue) distribution at the end of the overshoot period for case 1): Compared with Fig. 13, CF laterally grows due to the high voltage and high temperature in the overshoot period.

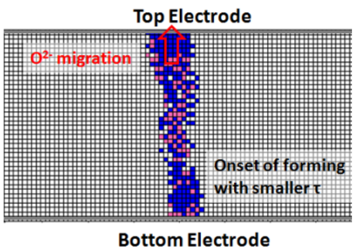

Fig. 15 Vo (pink) and O^{2-} (blue) distribution at the onset moment for case 2): forming with τ=10ns, corresponding to the **red** symbol in Fig. 9.

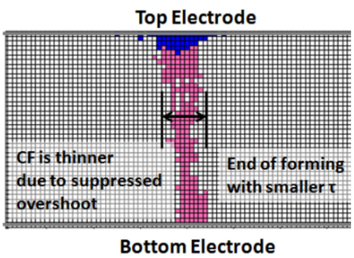

Fig. 16 Vo (pink) and O^{2-} (blue) distribution at the end of the overshoot period for case 2): Compared with Fig. 14, lateral growth of CF is suppressed due to a shorter overshoot period caused by smaller RC delay.

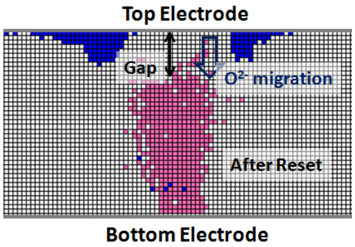

Fig. 17 Vo (pink) and O^{2-} (blue) distribution after the 1st reset applied on the cell in Fig. 14. O^{2-} migrate back due to a reversed electric field, and CF is ruptured and a tunneling gap is formed.

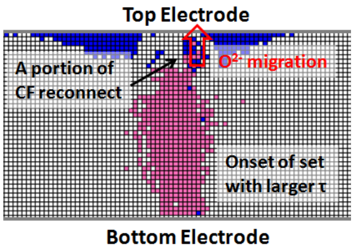

Fig. 18. Vo (pink) and O^{2-} (blue) distribution at the onset moment for case 3): set with τ=100ns, corresponding to the **green** symbol case in Fig. 9. Only a portion of the CF is reconnected.

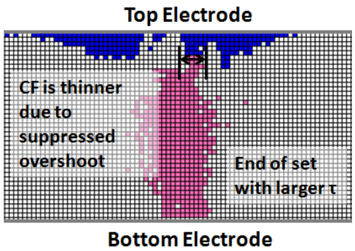

Fig. 19 Vo (pink) and O^{2-} (blue) distribution at the end of the overshoot period for case 3): since set voltage is smaller, lateral growth of CF is also suppressed with the same overshoot period.

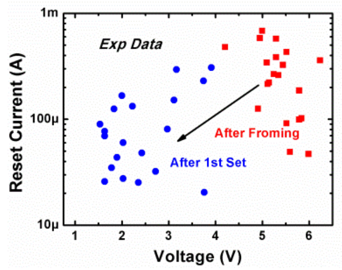

Fig. 20 Experimental data of TiN/HfOx/Pt RRAM [14]: the reset currents after the 1st set are reduced as compared with those after the forming because the overshoot in set is suppressed.

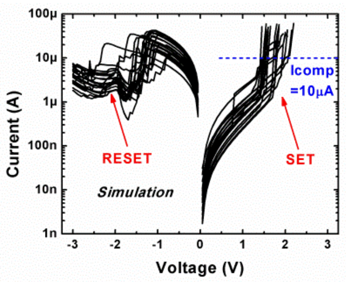

Fig. 21 Simulated I-V curves of repeated cycling of the RRAM cell. Abrupt set, gradual reset, and the variation are reproduced.

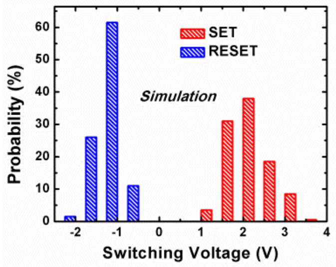

Fig. 22 Simulated switching voltage distribution during the repeated 200-cycle DC sweep of the RRAM cell.

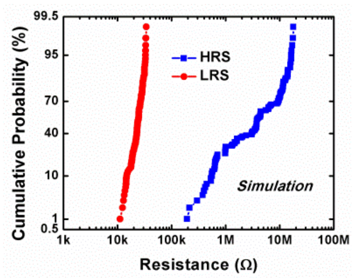

Fig. 23 Simulated resistance distribution during the repeated 200-cycle DC sweep of the RRAM cell.

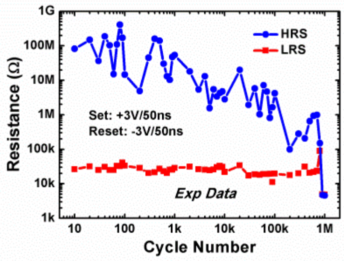

Fig. 24 Measured endurance of TiN/HfOx/Pt RRAM [14]. During the cycling, HRS decreases, and the final failure is at LRS.

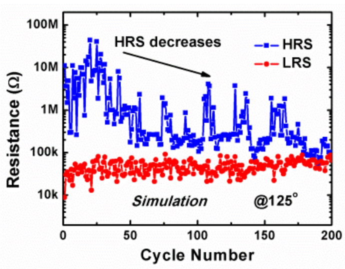

Fig. 25 Simulated endurance at 125 °C. Similar to Fig. 24, HRS decreases, and the final failure is at LRS.

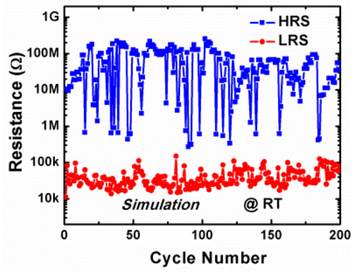

Fig. 26 Simulated endurance at room temperature. HRS does not degrade although significant variation is observable.

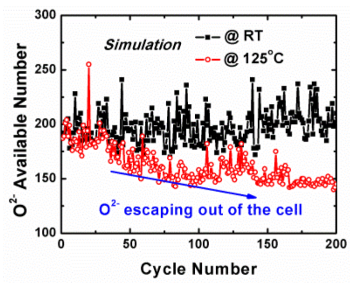

Fig. 27 Number of available O^{2-} at the interfacial reservoir during the cycling for the case in Fig. 25 & 26. High temperature accelerates the leakage of O^{2-} out of the cell.

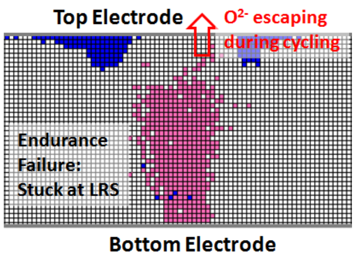

Fig. 28 Vo and O^{2-} distribution at the endurance failure at the end of cycling in Fig 25. Insufficient O^{2-} at the interface makes the reset impossible for the RRAM cell.

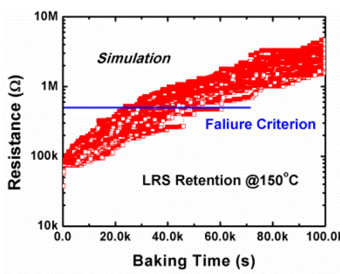

Fig. 29 Statistically simulated LRS retention of the RRAM cells @ 150°C. The resistance gradually increases due to the gradual dissolution of CF.

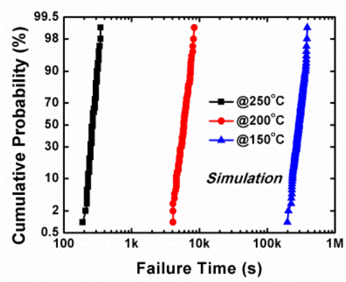

Fig. 30 Statistically simulated distribution of failure time of LRS at different temperatures.

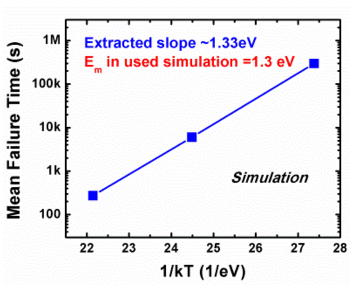

Fig. 31 Extracted mean failure time (from Fig. 30) vs. 1/kT. The slope (~1.33 eV) agrees well with the migration barrier of O^{2-} (~1.3 eV) used in simulation.

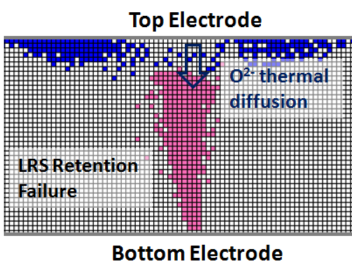

Fig. 32 Vo and O^{2-} distribution when the LRS failure occurs in a retention simulation. The CF is ruptured by the O^{2-} that thermally diffuse back from the oxygen reservoir at the interface.