Analysis and Simulation of Interface Quality and Defect Induced Variability in MgO Spin-Transfer Torque Magnetic RAMs

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***Abstract*— Device-to-device variability of CoFeB/MgO based STT-MRAMs is studied based on experiments and simulations taking into account the influence of interface quality, temperature variation and device dimensionality. Metal-induced gap states resulting from electron transfer at the ferromagnet-tunnel barrier interface significantly influence the effective energy barrier height of these devices irrespective of their diameters. Switching voltage and parallel - antiparallel resistance values vary by as much as 43% and 30% respectively for about 13% variation of the energy barrier, whereas the tunneling magnetoresistance remains typically unaffected. WRITE cycles of highly scaled STT-MRAMs are therefore more susceptible to device-to-device variations resulting from microscopic variations in the interface quality, rather than the READ cycles. Such variations are observed to be independent of temperature, as well as spatial distribution of the defects.**

***Index Terms*— STT-MRAM, variability, magnetoresistance, Monte Carlo simulation.**

I. Introduction

SPIN-TRANSFER torque magnetic random access memories (STT-MRAMs) are promising candidates for next-generation data storage owing to their non-volatility, fast access times, scalability, low-power consumption and compatibility with conventional CMOS technologies [1]–[5]. Small dimensionalities, as well as inherently stochastic switching characteristics of STT-MRAMs make them significantly prone to device-to-device, as well as cycle-to-cycle variations. Previous studies on STT-MRAM variability primarily focused on variability arising from process, temperature and operating conditions in magnetic tunneling junction (MTJ)/CMOS circuits or arrays [6]–[15]. Though significant insights on the variability and reliability of STT-MRAMs have been obtained from these studies, the ongoing drive towards utilizing highly-scaled variants of these devices for memory, as well as neuromorphic applications necessitates variability analysis from a microscopic point of view. In particular, aspects related to the role of interface quality and defects on device-to-device variation needs to be investigated in detail to have a better understanding of the source of variability in these devices.

In this letter we present experiments and simulations to investigate the variability of standalone CoFeB/MgO STT-MRAMs taking into account the role of defects, interface quality, operating temperature and dimensions of the devices. In contrast to previous studies, which incorporated defects as resistive shorts or opens in equivalent circuit models of STT-MRAMs [10], [16], this work employs multiscale simulation and ab-initio calculations which relate microscopic/atomistic properties of a device to its spintronic output characteristics. The results of this work indicate that WRITE cycles of STT-MRAMs are more susceptible to variations induced by interface quality than the READ cycles. This work also correlates effective energy barrier height with interface quality of these devices and shows that it can be exploited to predict device-to-device variabilities of STT-MRAM devices.

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II. Modeling and Simulation Setup

STT-MRAM stacks have been deposited by magnetron sputtering on 300 mm Si wafers. The MTJ pillars tested are circular with nominal diameters of 60, 70 and 80 nm (schematic shown in Fig 1(c)). To prevent oxidation of MgO, the sidewall was encapsulated by a dielectric gap-fill material. The influence of sidewall on device variability is expected to be negligible as cross-sectional area of the device is about 15 to 20 times larger than the MgO sidewall area because of the very small thickness (∼1 nm) of the MgO layer. For variability study, 15-20 devices of each diameter were fabricated on the same wafer. As these devices were located in the central dies of the wafer, RA non-uniformity is expected to be small- typically within $\pm 0.2\Omega\text{-}\mu m^2$.

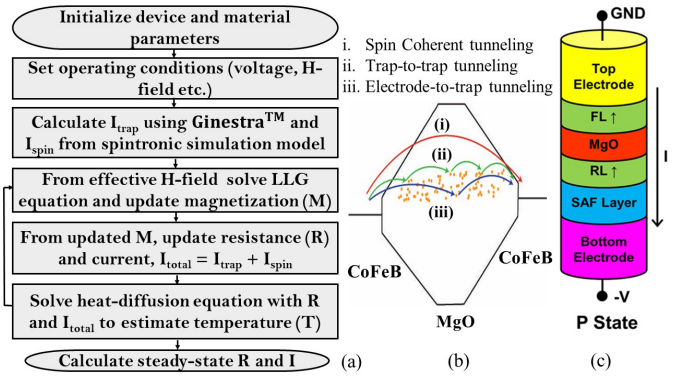
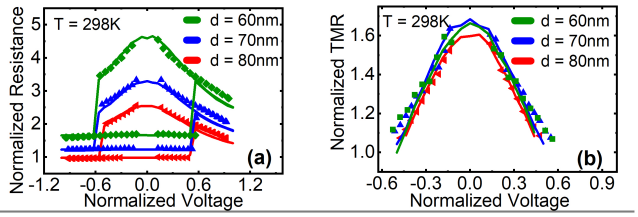


Fig. 1. (a) Flowchart illustrating simulation model. (b) Band diagram of the MTJ device involving MIGS. (c) Schematic illustration of fabricated MTJ pillar.



Parameters	Value used	Ab-initio Calculations/experiments
E_T	3.2 eV	3.3 eV (F^+*) [24]
		3.2 eV (F^+*) [32]
		3.4 eV (Bulk F^o) [33]
E_{rel}	1 eV	0.9 eV (F) [33]
φ	1.25 eV	1.1-1.7 eV (CoFe/Fe/MgO/CoFe, CoFe/ MgO/CoFe) [22]
		0.39 eV (Fe/MgO/Fe) [18]
		0.45-0.59 eV (CoFeB/MgO/CoFeB) [23]
		0.62 (P)-0.5 (AP) eV (FeCoB/MgO/FeCoB) [24]
		1.2 (P)-0.8 (AP) eV (FeCoB/MgO/FeCoB) [24]

(c)

Fig. 2. Measured (symbols) and simulated (lines) results of (a) R-V loops and (b) TMR vs voltage characteristics. (c) Defect parameters and barrier height extracted from experimental results and comparison with ab-initio calculations.

Experimental steady-state output characteristics of the devices were analyzed based on a spintronic simulation model in combination with the multi-scale simulation platform of Ginestra™ [17]. In this model (shown in Fig. 1(a)), Landau-Lifshitz-Gilbert (LLG) equation is self-consistently solved to calculate spin-dependent direct tunneling current (I_{spin}), taking into account temperature and voltage dependence of tunneling magnetoresistance (TMR) [18]–[21]. Trap assisted tunneling current (I_{trap}) is calculated using Ginestra™, which performs statistical simulation by randomly generating every device and its constituent oxygen vacancies in the MgO layer, and applies Kinetic Monte Carlo simulation technique to account for the stochastic nature of charge transport. The total current (I_{total}) resulting from I_{spin} and I_{trap} in effect influences the overall magnetic switching characteristics, thereby creating a self-consistent loop.

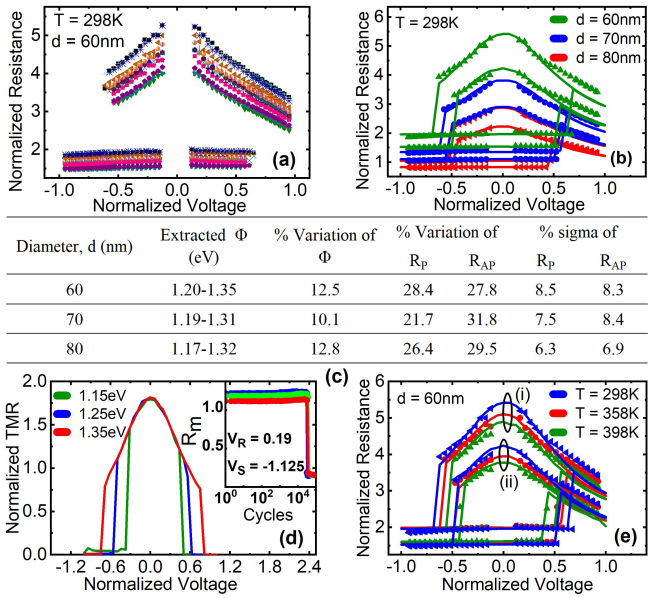
III. Results and Discussions

A parameter fundamental to the estimation of parallel spin state resistance of an STT-MRAM is its energy barrier height (ϕ). For MgO based MTJ devices, the reported energy barrier heights range from 0.39-1.2eV [18], [22] [23], [24], even though the ideal barrier height of bulk MgO is 3.7eV [25]. Such deviation of ϕ from the ideal value hints towards the significant influence of interface quality on electronic properties of ultra-thin MgO tunnel barriers in MTJs. In fact, ab-initio calculations and experimental results suggest that spatial penetration of metal wave functions as well as hybridization of electronic states arising from the defects, may lead to the formation of gap states in the tunnel barrier. Such states, which are known as metal induced gap states (MIGS), effectively reduce the MgO bandgap at the CoFeB/MgO interface [26]–[28].

To incorporate the effect of MIGS, the present simulation framework considers a gradually varying energy band profile (Fig. 1(b)). This is in accordance with previous spectroscopic and first principle calculation based reports [29]–[31], which suggest gradual as well as local change of MgO bandgap because of intermixing and interdiffusion between tunnel barrier and magnetic contact layers. Good agreement between numerical simulations and experimental results are obtained for all three diameters of the STT-MRAMs considering such band profiles (Figs. 2(a)-(b)). The effective value of ϕ extracted for these devices is 1.25eV. Trap energy (E_T) and relaxation energy (E_{rel}) are estimated from the calculation of I_{trap}. Comparison of these values with ab-initio simulation results indicate the presence of neutral (F) or singly charged (F^+) oxygen vacancy defects in these devices [24], [32], [33]. Process induced edge damage has been neglected herein as our previous studies on self-heating corrected area scaling of time dependent dielectric breakdown (TDDB) demonstrated edge damage to have secondary effects on the reliability of such industry grade devices [34].

As shown in Fig. 3(a), significant variation in the measured resistance vs. voltage (R-V) characteristics exists in the devices having diameter, d = 60nm. Percentage standard deviation (%sigma) of switching voltage from parallel (anti-parallel) to anti-parallel (parallel) state of these devices is ~5.1% (7.3%), whereas the minimum resistance varies by about 7.7%. Similar variations are observed for devices of 70 and 80nm diameters as well. To understand the microscopic origin of such variability, R-V loops with the highest and lowest resistance values for each diameter of the devices are analyzed (Fig. 3(b)). The extracted values of ϕ (shown in Fig. 3(c)) suggest that the energy barrier height is uncorrelated to the diameter of the device. However it is noteworthy that the parallel (R_P) and anti-parallel (R_{AP}) resistances vary up to about 28% and 32%, respectively, over this extracted range of ϕ.

According to Fig. 3(d), the switching voltage is positively correlated to ϕ such that 0.2eV variation of ϕ results in about 43% variation of switching voltage. TMR of these devices however essentially remains constant over this range of ϕ. The read voltage of STT-MRAMs is typically within 0.01-0.20V and for such small voltages the devices show similar resistance values after multiple READ cycles. This is further illustrated in Fig. 3(d), which shows as an inset the minimum value of normalized parallel resistance (R_m) obtained from consecutive READ cycles during TDDB



Diameter, d (nm)	Extracted Φ (eV)	% Variation of Φ	% Variation of R_P	% Variation of R_{AP}	% sigma of R_P	% sigma of R_{AP}
60	1.20-1.35	12.5	28.4	27.8	8.5	8.3
70	1.19-1.31	10.1	21.7	31.8	7.5	8.4
80	1.17-1.32	12.8	26.4	29.5	6.3	6.9

Fig. 3. (a) Measured R-V loops of d = 60nm devices fabricated on the same wafer. (b) Measured (symbols) and simulated (lines) R-V loops for highest and lowest resistance values of each diameter. (c) Extracted values of ϕ, and measured percentage (%) variation and percentage standard deviation (%sigma) of R_p and R_{AP}. (d) Effect of ϕ on TMR of the device; inset shows R_m obtained for multiple READ cycles during TDDB measurements where V_R and V_S refer to normalized READ and stress voltages respectively. (e) Effect of temperature variation on R-V loops corresponding to extracted values of (i) ϕ = 1.35-1.36eV and (ii) $\phi = 1.20$-1.23eV.

measurement of three devices having identical diameters. Even in the presence of a stress voltage much higher than the READ voltage, a %sigma variation of only about 0.7% is obtained for R_m. Such variation corresponds to a change of energy barrier height by only about 20meV. This suggests that variation of energy barrier height has minimal effect on READ cycles. To understand the effect of temperature on energy barrier induced variability, highest and lowest resistance valued R-V loops measured at three different temperatures have been analyzed (Fig. 3(e)). The extracted values of ϕ suggest that for a 100°C change of temperature, the energy barrier height changes only by about 10-20meV. Consequently temperature variation over such a range has negligible effect on the variability of these devices.

To understand whether device-to-device variability in MTJs is governed more by the density and distribution of defects, rather than by the slight change of energy barrier height resulting from material and interfacial properties, trap-assisted tunneling currents have been calculated considering different density and spatial distributions of bulk defects (Fig. 4(a)). It is observed that for all defect densities, I_{trap} remains about two orders of magnitude smaller than I_{spin}, thereby having minimal effect on the R-V characteristics (shown as inset of Fig. 4(a)). Therefore variability in these devices primarily arises from interface quality, which manifests itself in MIGS induced lowering of ϕ. To further elucidate this aspect, statistical simulation of 25 devices is performed considering uniform spread of the spatially varying bandgap of MgO. As shown in Fig. 4(b), the results of statistical simulation are well within the range of trap current calculated using the extracted

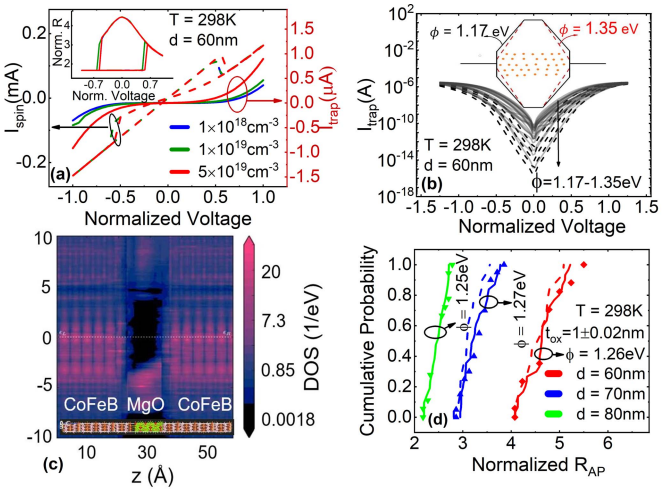


Fig. 4. (a) Comparison of spin (solid lines) and trap current (dashed lines) densities for different concentrations of bulk defects (effect on R-V loop shown as inset). (b) Trap currents calculated from linear (dashed lines) and statistical (solid lines) variation of ϕ; inset shows energy band diagram illustrating the physical significance of ϕ. (c) Ab-initio calculations showing density of states (DOS) in CoFeB/MgO/CoFeB. (d) CDF plot of zero-bias R_{AP} considering statistical variation of t_{ox} (experimental results shown as symbols whereas dashed lines show fits with a fixed value of $\phi = 1.25$eV for all devices).

values of ϕ. These results further validate the use of an effective barrier to correctly represent the gradually varying band profile.

The spatial variation of bandgap becomes further evident from ab-initio calculations (Fig. 4(c)), which have been performed using linear combination of atomic orbitals with PseudoDojo basis [35]. The physical significance of ϕ is further emphasized by the cumulative distribution function (CDF) plot of Fig. 4(d), which shows that statistical variation of oxide thickness (t_{ox}) alone fails to accurately predict device-to-device variability if a fixed value of ϕ is considered for all devices. As shown by solid lines, experimental results for all three diameters of the devices fit well with statistical analysis if energy barrier heights of corresponding devices are duly considered. These results establish the significance of effective barrier height as a figure of merit of the interface quality of ultra-scaled STT-MRAMs and provides evidence that it can be utilized to predict WRITE cycle device-to-device variabilty.

IV. Conclusion

The microscopic origin of device-to-device variability of STT-MRAMs is investigated based on experiments and simulations taking into account the role of defects and interface quality. It has been shown that the effective energy barrier height can serve as a figure of merit of interface quality of these devices and it can also be utilized to predict WRITE cycle variability. Bulk defect density and distribution, as well as temperature, are observed to have minimal effect on such variabilities of STT-MRAMs.

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