Technion – Israel Institute of Technology
Viterbi Faculty of Electrical and Computer Engineering

Advanced Circuits and Architectures with Memristors

Homework 2

Sneak Path & Write Disturbance

Submission until 28/12/2022 at 11:59pm

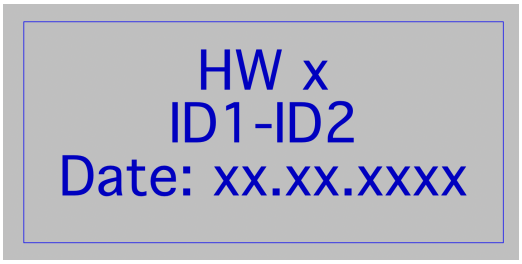
If you have questions, please either post on the course forum (on Moodle) or send an email to course046265@gmail.com

General Instructions

- Items marked with  are "Dry" and only require calculations, explanations and/or simple graph plotting.
- Items marked with  are "Wet" and require simulation using MATLAB/LTspice.
- The answer sheet should be submitted **in PDF format**, with answers to all questions, and with all requested plots pasted as pictures inside.
- **The entire submission should be a single PDF file named ID1-ID2.pdf for ID1 and ID2 the ID numbers of the students**. The submission is to be uploaded to Moodle.
- **Late Submission Policy:** Submission of the assignment past the deadline without permission from the course staff reduces 5 points per day, for a maximum of 3 days.

Wet Instructions

- Circuit schematics, graphs, and waveforms requested in the question prompt must be **explicitly shown** (pasted into the PDF).
- **Refer to the Appendices for guides on LTspice usage in this homework.**
- **All schematics must include the following header (shown with the schematic):**

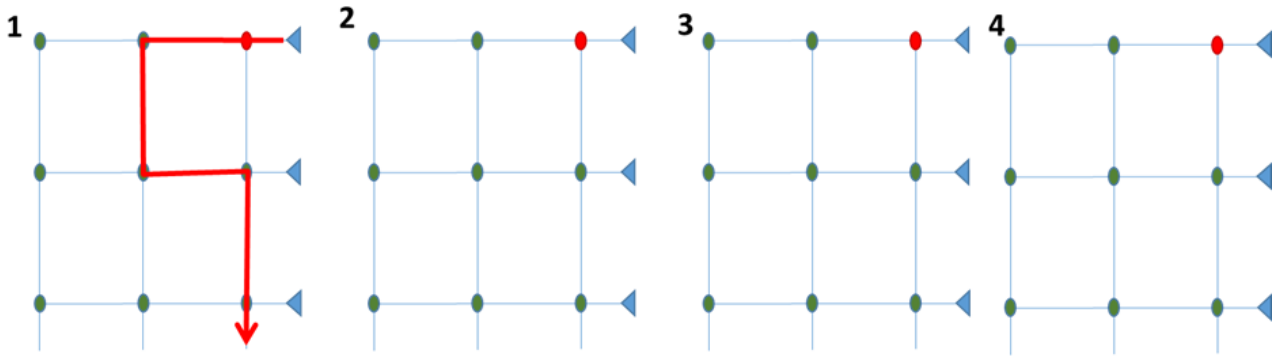


Question 1 – Sneak Path

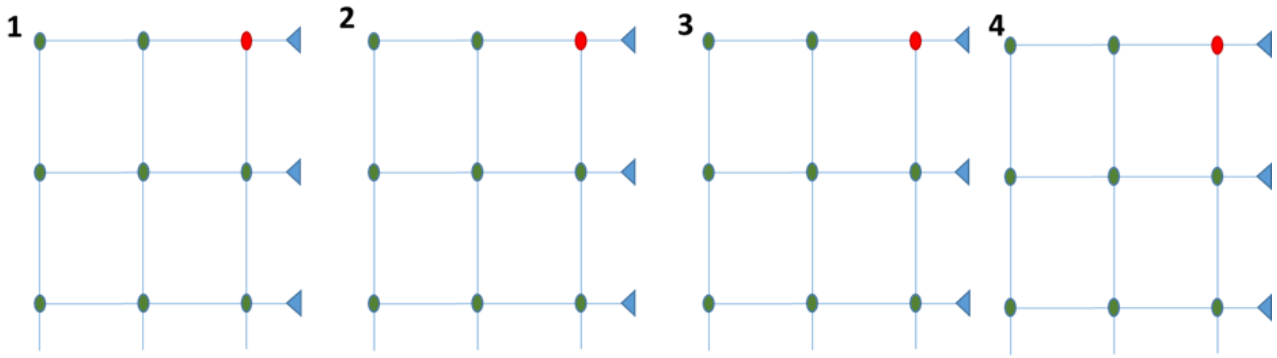
This question deals with understanding the sneak-path phenomenon in 3×3 crossbar arrays.

a. In the following subsections, determine the *potential* sneak paths that may be encountered when reading the red memristor (a circle represents a single memristor).

(a) Find all 3-turn paths and draw them (the first path is given):



(b) Find all 5-turn paths and draw them:



(c) Are 7-turn sneak paths possible? Explain.

(d) What is the total number of potential sneak paths?

b. In the following subsections, you will determine a set of criteria that guarantee a successful read operation even in the presence of sneak paths. Consider the following parameters, assuming that $R_{ON} \ll R_{OFF}$:

Parameter	Value
V_r	Read voltage
R_L	Reference resistor
R_{ON}	Low resistance value of the memristors (represents '1')
R_{OFF}	High resistance value of the memristors (represents '0')
$I_{1,min}$	Minimum current that flows through the load resistor R_L and read is considered as a '1'
$I_{0,max}$	Maximum current that flows through the load resistor R_L and read is considered as a '0'

(a) What is the criterion for a successful read operation? Select the correct condition:

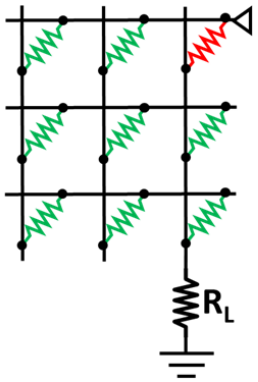
$$I_{1,min} \quad < / > \quad I_{0,max} \tag{1}$$

(b) What conditions (value of the read memristor and the values of all the other memristors) will lead to sensing $I_{1,min}$? That is, what conditions that should be interpreted as reading 1 will lead to the lowest current flowing through the load resistor R_L?

(c) What conditions (value of the read memristor and the values of all the other memristors) will lead to sensing $I_{0,max}$? That is, what conditions that should be interpreted as reading 0 will lead to the highest current flowing through the load resistor R_L?

(d) Assuming the resistance of the read memristor is R_{read} and the resistance of all other memristors is R_{other}, find the equivalent resistance of the entire circuit when sensing the read memristor.

Guidance: Consider the reading circuit shown below (for reading the value of the red memristor). Draw the equivalent circuit in a simplified form (the read memristor connected in parallel to a circuit containing all of the other memristors) and then compute the equivalent resistance.



(e) Determine what are the values of $I_{1,min}$ and $I_{0,max}$.

(f) Simplify the expression of $I_{1,min}$, assuming $R_{ON} \ll R_{OFF}$.

(g) What is the resulting criterion for a successful read operation assuming $R_{on} \ll R_{off}$?

Question 2 – Sneak Paths and Mitigation

In this question, you will investigate the sneak path phenomenon and its mitigation techniques in LTspice by designing a 4×4 memory array. Use the Joglekar model from HW1, with the following parameters:

Parameter	Value
R_{ON} (Ron)	100Ω
R_{OFF} (Roff)	$10k\Omega$
D (D)	$10N$
μ (uv)	$10F$
p (p)	1

where R_{init} is chosen according to the question (either R_{ON} or R_{OFF}).

a. Build a 4×4 crossbar array in LTspice configured to read the state of the memristor at the top-right location. Include all the necessary circuitry for reading the state of that memristor, including a voltage source with $V_r = 200mA$ and a load resistor with $R_L = 100\Omega$. Simulate the reading operation for the following four cases:

   (a) All of the cells in the array are in the R_{OFF} state.
   (b) All of the cells in the array are in the R_{ON} state, except for the cell that you are trying to read (the top-right cell) which is in the R_{OFF} state.
   (c) All of the cells in the array are in the R_{OFF} state, except for the cell that you are trying to read (the top-right cell) which is in the R_{ON} state.
   (d) All of the cells in the array are in the R_{ON} state.

   Include the schematics and waveforms for $V(t), I(t)$ that demonstrate the reading operation. Interpret the currents in the waveforms. Show that a successful read operation is not always guaranteed (**Hint:** see Question 1b).

b. Repeat (a) with the technique of grounding unselected cells and explain why successful read operation is now guaranteed. What are the disadvantages of this technique?

c. Repeat (a) with the technique of diode selector and explain why successful read operation is now guaranteed. For bipolar memristors, are write operations still possible? If not, what similar alternative technique can be used?

   Use the following diode parameters and see the Appendix for importing a diode into LTspice:

Parameter	Value
R_{ON} (Ron)	1
R_{OFF} (Roff)	1Meg
V_{fwd} (Vfwd)	0.1
V_{rev} (Vrev)	10

Question 3 – Write Disturbance and Mitigation

In this question, you will investigate the write disturbance phenomenon and its mitigation techniques in LTspice by designing a 4×4 memory array. Use the Joglekar model from HW1, with the following parameters (notice that the parameters are different from Question 2):

Parameter	Value
R_{ON} (Ron)	100Ω
R_{OFF} (Roff)	$10k\Omega$
D (D)	$1N$
μ (uv)	$1000F$
p (p)	1

where R_{init} is chosen according to $9k\Omega$ for "0" and 200Ω for "1".

a. Why is R_{init} chosen as either 200Ω or $9k\Omega$ instead of 100Ω or $10k\Omega$?

b. Build a 4×4 crossbar array in LTspice storing the following information:

$$\begin{pmatrix} 0 & 0 & 1 & 1 \\ 0 & 1 & 1 & 0 \\ 0 & 1 & 1 & 1 \\ 0 & 1 & 0 & 0 \end{pmatrix} \tag{2}$$

Find a pair of cells that can demonstrate the write-disturbance phenomenon: both cells currently store a zero, yet writing a one to one of the cells will unintentionally also lead to the other cell switching to one. Simulate such a write operation with an input voltage source $V_w = 2V$, and include the schematic of the array. Provide the following waveforms:

(a) Input voltage as a function of time
(b) State variable of the target memristor as a function of time
(c) State variable of the memristor that switches unintentionally as a function of time

Mark the two memristors on the array, or provide their locations in your response. Explain the results, highlighting the unintentional write.

Hint: you will need to modify the pulse duration to find full switching of both memristors within the simulation time.

c. Show the waveform of the power used to switch (write) the target cell from "0" to "1". Explain the shape of the waveform. How much total energy is used?

Guidance: Integration in LTspice can be computed on a waveform using Ctrl-Left Click on the waveform name. See the LTspice workshop for details.

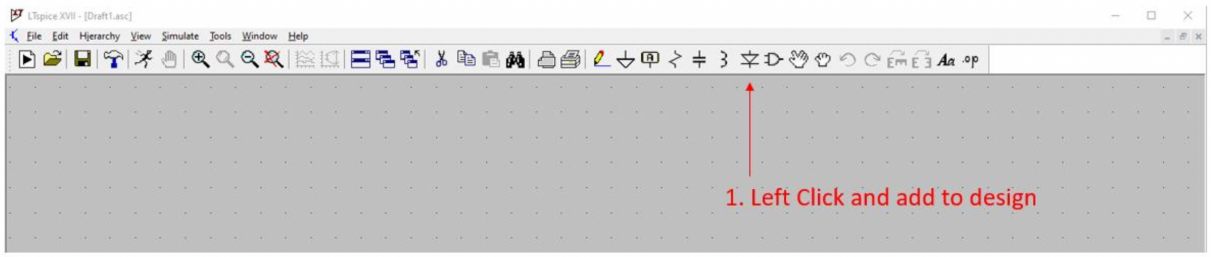
d. Show the waveform of the overall array power during the write operation. Explain the shape of the waveform. How much total energy is used?

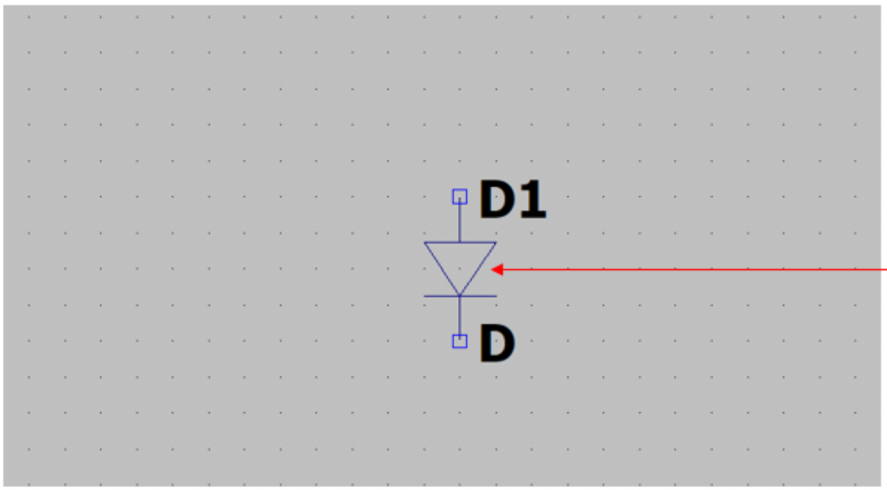
Hint: make sure that the sign of the power in the waveform is correct (i.e., positive).

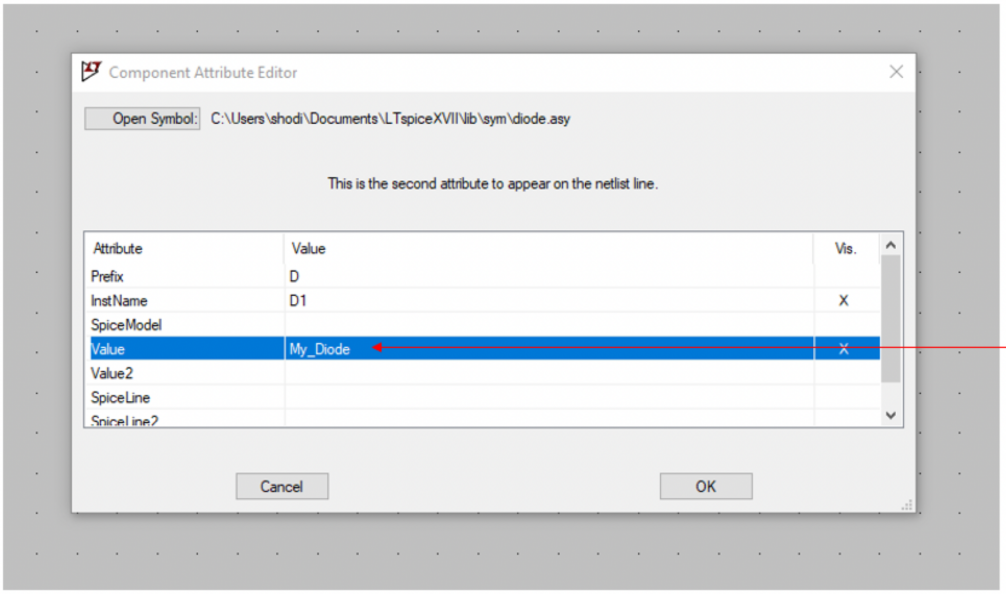
e. What is the energy efficiency of the write procedure to this cell (energy that was used for the intended switching compared to the total energy)?

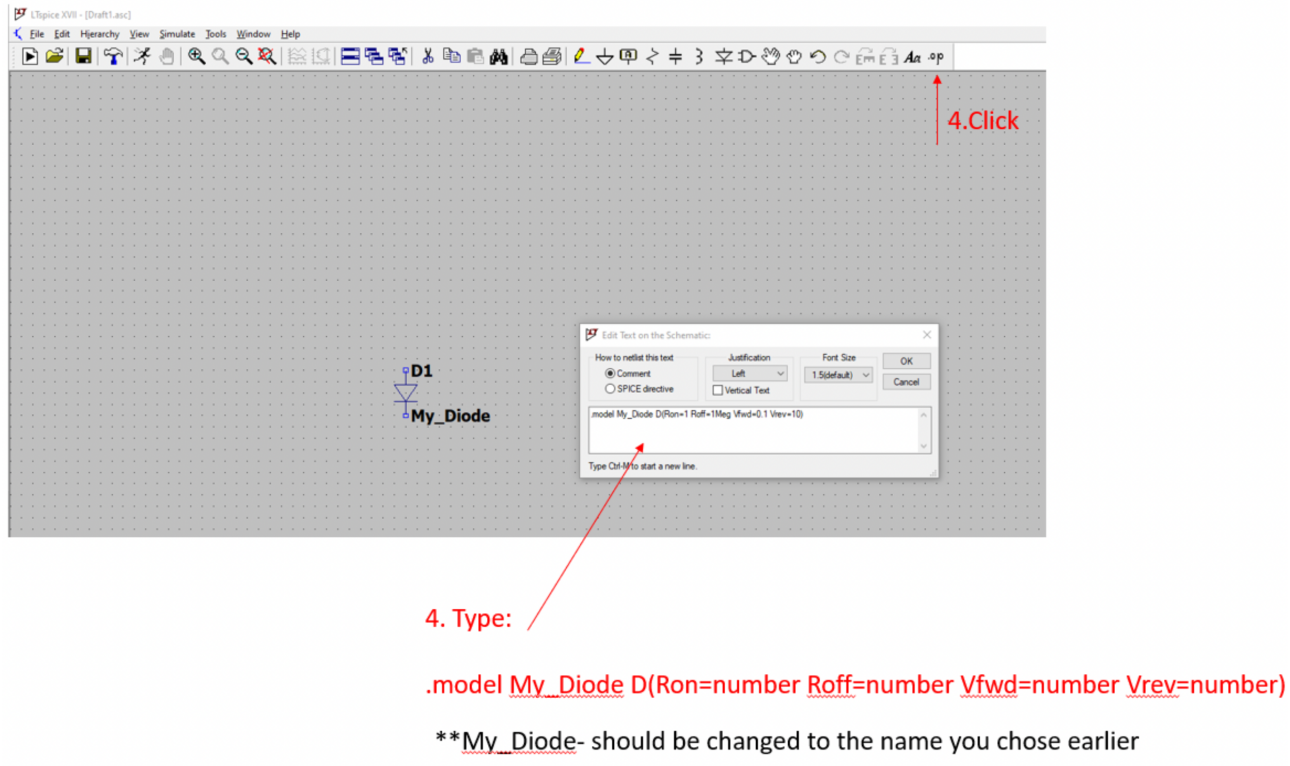
f. Repeat (b)–(e) with the half-select mitigation method to reduce the effect of the write disturbance. Use the same two memristors as before with the same pulse duration. Is the effect of the write disturbance reduced? What is the trade-off of the half-select method?

Appendix – Importing Diodes into LTspice









The diode parameters correspond to the following:

Name	Description	Units	Default
Ron	Resistance in forward conduction	Ω	1.
Roff	Resistance when off	Ω	1./Gmin
Vfwd	Forward threshold voltage to enter conduction	V	0.
Vrev	Reverse breakdown voltage	V	Infin.
Rrev	Breakdown impedance	Ω	Ron
Ilimit	Forward current limit	A	Infin.
Revilimit	Reverse current limit	A	Infin.
Epsilon	Width of quadratic region	V	0.
Revepsilon	Width of reverse quad. region	V	0.