TECHNION – ISRAEL INSTITUTE OF TECHNOLOGY
VITERBI FACULTY OF ELECTRICAL AND COMPUTER ENGINEERING

Advanced Circuits and Architectures with Memristors

Homework 4

Neuromorphic Computing

Submission until 26/01/2023 at 11:59pm

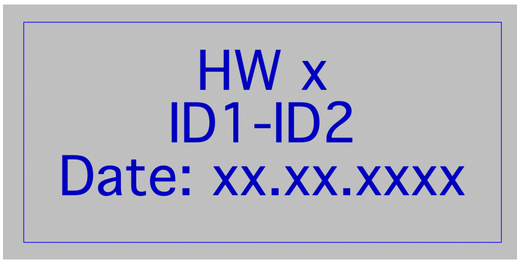
If you have questions, please either post on the course forum (on Moodle) or send an email to course046265@gmail.com

General Instructions

- Items marked with are "Dry" and only require calculations, explanations and/or simple graph plotting.
- Items marked with are "Wet" and require simulation using MATLAB/LTspice.
- The answer sheet should be submitted **in PDF format**, with answers to all questions, and with all requested plots pasted as pictures inside.
- **The entire submission should be a single PDF file named ID1-ID2.pdf for ID1 and ID2 the ID numbers of the students**. The submission is to be uploaded to Moodle.
- **Late Submission Policy:** Submission of the assignment past the deadline without permission from the course staff reduces 5 points per day, for a maximum of 3 days.

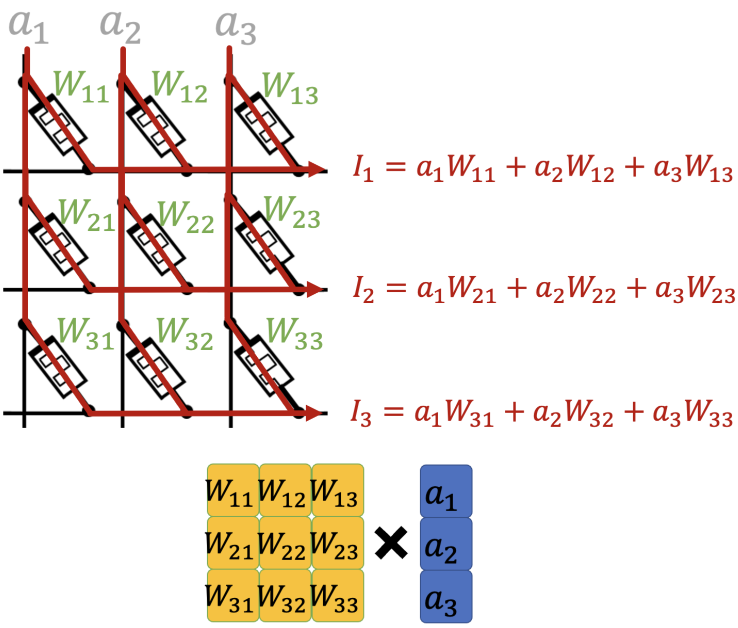
Wet Instructions

- Circuit schematics, graphs, and waveforms requested in the question prompt must be **explicitly shown** (pasted into the PDF).
- **Refer to the Appendices for guides on LTspice usage in this homework.**
- **All schematics must include the following header (shown with the schematic):**



Question 1 – Matrix Multiplication

In this question, you will simulate an analog matrix-vector multiplication operation using a memristive crossbar array. Recall from the tutorial that a crossbar computes an analog matrix multiplication:



for a_1, a_2, a_3 the input voltages and $W_{1,1}, W_{1,2}, \ldots, W_{3,3}$ the **conductances** of the memristors. You will simulate this operation in LTspice over the next subsections.

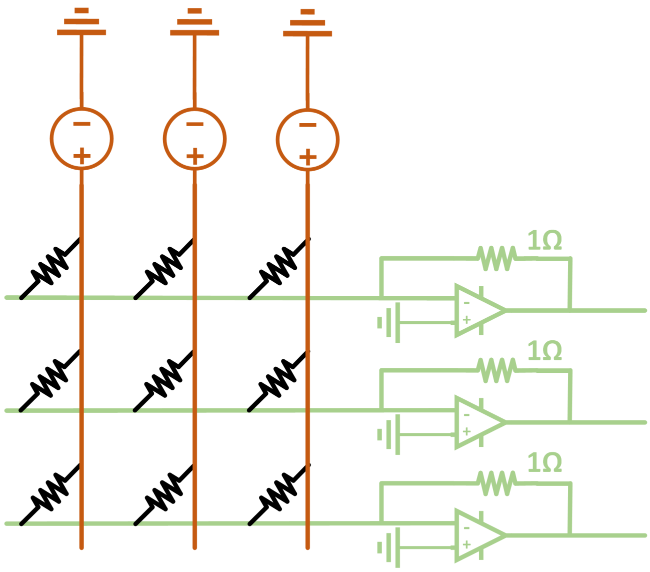
a. Throughout this question, we seek to compute the following matrix-vector multiplication:

$$\begin{pmatrix} 1 & 1/2 & 1/3 \\ 1/4 & 1/5 & 1/6 \\ 1/7 & 1/8 & 1/9 \end{pmatrix} \begin{pmatrix} 1.2 \\ 3.3 \\ 5 \end{pmatrix} \approx \begin{pmatrix} 4.52 \\ 1.79 \\ 1.14 \end{pmatrix}$$

What voltages a_1, a_2, a_3 and **conductance** values $W_{1,1}, W_{1,2}, \ldots, W_{3,3}$ should be applied to compute this matrix-vector multiplication? What are the resistances $R_{1,1}, R_{1,2}, \ldots, R_{3,3}$?

Guidance: Use voltages in the range $[0, 5V]$ and conductances in the range $[1/9\Omega^{-1}, 1\Omega^{-1}]$ (which leads to resistances in the range $[1\Omega, 9\Omega]$).

b. We will begin in this subsection by simulating a crossbar of **resistors** (instead of memristors) performing the operation from Question 1a. Construct the following circuit in LTspice:

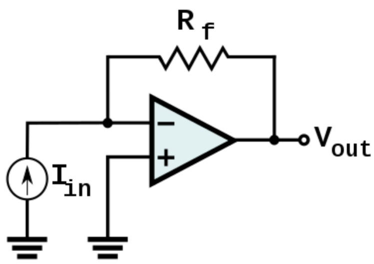


Choose the input voltage and resistance values according to Question 1a. Simulate the circuit in LTspice, provide the schematic, and explain the following waveforms:

- Input voltages as a function of time.
- Output voltages as a function of time.

Verify that the output voltages correspond to the expected results from Question 1a.

Reminder: The transimpedance amplifier (current to voltage converter) in the above circuit is defined according to:



$$\frac{V_{out}}{I_{in}} = -R_f$$

Guidance: Use the `UniversalOpAmp` component with `Avol=10Meg GBW=1000Meg Vos=0`. Negative output voltages are fine, as long as the magnitude is correct.

c.  What parameter in Question 1b can be modified to use resistance values in the range $[1000\Omega, 9000\Omega]$ instead of $[1\Omega, 9\Omega]$? The input voltages and output voltages should be unchanged.

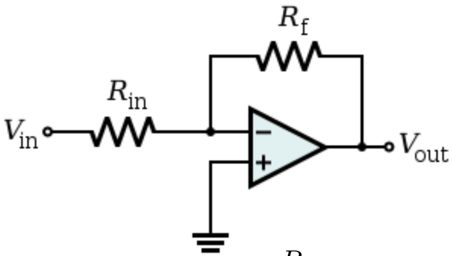
d.  In this question you will replace the resistors from Question 1b with memristors.[1] You should also ensure that the memristances of the memristors **do not** change significantly throughout the simulation (with simulation time $1\mu s$). Use the following memristor parameters:

[1] The benefit of memristors over resistors is that the weight matrix can be modified through write operations (compared to a resistor array that is read-only).

Parameter	Value
R_{ON} (Ron)	100
R_{OFF} (Roff)	$10k$
R_{init} (Rinit)	Question 1c
D (D)	$1N$
μ (uv)	$500F$
p (p)	5

Include the schematic and the same waveforms as Question 1b. Explain the waveforms.

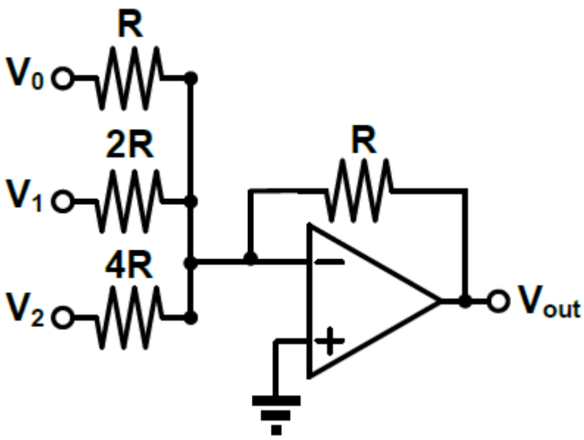
Hint: To guarantee that the memristances do not change significantly, you will need to reduce the voltages applied on the memristor while keeping the input voltages identical. To that end, you can use the following circuit:



$$V_{out} = -\frac{R_f}{R_{in}} V_{in}$$

Question 2 – Digital to Analog Converter

In this question, you will implement a 3-bit binary-weighted (BW) digital-to-analog converter (DAC) based on neural networks using the below circuit. For several years, real implementations of this DAC architecture was not possible due to the process variations that affect the resistances of the resistors in integrated circuits, and due to the large resistance changes with temperature. Recently, the use memristive synapses for BW DACs was proposed [1] as they allow for online resistance tuning.



a. Derive an expression for V_{out} as a function of V_0, V_1, V_2. Explain.

b. Simulate the circuit in LTspice for $R = 1k\Omega$. Show all input combinations in the simulations, with the input voltages being either $0V$ or $1V$ at each time point (the simulation should demonstrate the output voltage in all 8 combinations of input voltages). Attach the schematic and waveforms of V_0, V_1, V_2, V_{out} over time.

   Hint: Define each of the input voltages with a different pulse duration to lead to the desired behavior of all 8 input combinations.

c. Repeat Question 2b with memristors instead of resistors, using the following parameters:

Parameter	Value
R_{ON} (Ron)	100
R_{OFF} (Roff)	$10k$
R_{init} (Rinit)	Depends
D (D)	$10N$
μ (uv)	$10F$
p (p)	1

   Choose the simulation time to be sufficiently small such that the memristors do not change their state significantly over the simulation.

References

[1] L. Danial *et al.*, "DIDACTIC: A Data-Intelligent Digital-to-Analog Converter with a Trainable Integrated Circuit using Memristors," *IEEE Journal on Emerging and Selected Topics in Circuits and Systems*, vo. 8, no. 1, pp. 146–158, 2017.