Technion – Israel Institute of Technology
Viterbi Faculty of Electrical and Computer Engineering

Advanced Circuits and Architectures with Memristors

Homework 3

Multi-Level Cells & Stateful Logic

Submission until 11/01/2023 at 11:59pm

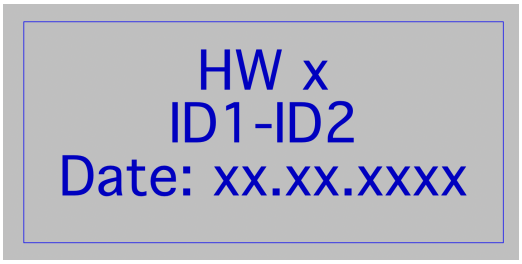
If you have questions, please either post on the course forum (on Moodle) or send an email to course046265@gmail.com

General Instructions

- Items marked with  are "Dry" and only require calculations, explanations and/or simple graph plotting.
- Items marked with  are "Wet" and require simulation using MATLAB/LTspice.
- The answer sheet should be submitted **in PDF format**, with answers to all questions, and with all requested plots pasted as pictures inside.
- **The entire submission should be a single PDF file named ID1-ID2.pdf for ID1 and ID2 the ID numbers of the students**. The submission is to be uploaded to Moodle.
- **Late Submission Policy:** Submission of the assignment past the deadline without permission from the course staff reduces 5 points per day, for a maximum of 3 days.

Wet Instructions

- Circuit schematics, graphs, and waveforms requested in the question prompt must be **explicitly shown** (pasted into the PDF).
- **Refer to the Appendices for guides on LTspice usage in this homework.**
- **All schematics must include the following header (shown with the schematic):**



Question 1 – Multi-Level Cells (MLC)

This question deals with understanding the programming methods for multi-level cells, as discussed in Tutorial 6. Use the Joglekar model from HW1, with the following parameters:

Parameter	Value
R_{ON} (Ron)	100
R_{OFF} (Roff)	$10k$
R_{init} (Rinit)	200
D (D)	$1N$
μ (uv)	$1000F$
p (p)	5

a. In this subquestion, you will simulate the phenomenon shown in the right figure of Tutorial 6 Slide 5. Connect a single memristor to a pulse train with the following parameters,

Parameter	Value
V_1 (V1)	0
V_2 (V2)	1
t_{delay} (Td)	0
t_{rise} (Tr)	$1n$
t_{fall} (Tf)	$1n$
t_{on} (Ton)	$15u$
t_{period} (Tperiod)	$50u$

and a simulation time of $150\mu s$ – where the voltage source is connected to the **negative** end of the memristor. Provide the schematic and the following waveforms:

(a) The input voltage over time

(b) The current over time

(c) The state variable of the memristor over time

(d) The resistance of the memristor over time

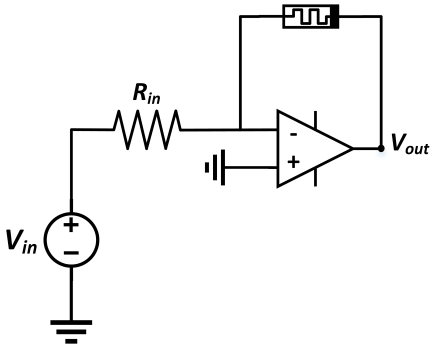
Explain the waveforms. What are the resistances of the **four** different levels (where the first level is approximately R_{ON} and the fourth level is approximately R_{OFF})? Why is this not a uniform level distribution?

b. Repeat (a) with the Incremental Length Pulse Programming (ILPP) technique. Choose the pulse durations so that the resistance levels will be approximately uniform (four levels, with the first being $\approx R_{ON}$ and the last being $\approx R_{OFF}$). The magnitude, simulation time, and the period should be unchanged – modify only the pulse durations. What are the new pulse durations?

Guidance: Use the PWL option in LTspice to model this pulse (see `https://www.analog.com/en/technical-articles/ltspice-generating-triangular-sawtooth-waveforms.html`). As LTspice performs linear interpolations between the data points in PWL, then use two datapoints per sample (e.g., if changing from $1V$ to $0V$ at $t = 50\mu$, then include $(50\mu, 1)$ and $(50.1\mu, 0)$).

c. Repeat (a) with the Incremental Magnitude Pulse Programming (IMPP) technique. Choose the pulse magnitudes so that the resistance levels will be approximately uniform (four levels, with the first being $\approx R_{ON}$ and the last being $\approx R_{OFF}$). The simulation time, pulse length, and the period should be unchanged – modify only the pulse magnitudes. What are the new pulse magnitudes?

d.  In this subquestion, you will use an operational amplifier to automatically adjust the voltage across the memristor, similar to the assignment in Tutorial 6. Construct the following circuit in LTspice:



where V_{in} is chosen according to the same parameters from (a) and R_{in} is chosen so that the resistance levels will be approximately uniform (four levels, with the first being $\approx R_{ON}$ and the last being $\approx R_{OFF}$). Provide the schematic and the following waveforms:

(a) The voltage V_{in} over time

(b) The voltage V_{out} over time

(c) The current through the memristor over time

(d) The state variable of the memristor over time

(e) The resistance of the memristor over time

Explain the waveforms. What are the resistances of the four different levels?

Guidance: Use the `UniversalOpAmp` component in LTspice for the operational amplifier.

Question 2 – Stateful Logic (MAGIC)

In this question, you will simulate the behaviour of the MAGIC NOR gate (shown below) in LTspice. Use the Binarized memristor model from HW1 defined according to:

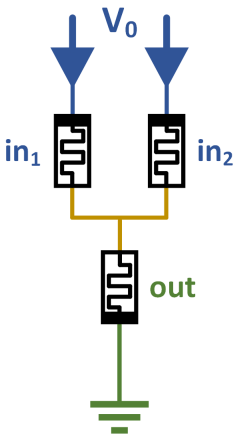
$$\frac{dx}{dt} = \begin{cases} e^{a_1 - x} & v > V_f \\ 0 & V_r \leq v \leq V_f \\ -e^{a_2 + x} & v < V_r \end{cases} \tag{1}$$

$$R(x) = \begin{cases} R_{ON} & x \geq 0 \\ R_{OFF} & x < 0 \end{cases} \tag{2}$$

with the following parameters:

Parameter	Value
R_0	$1k$
R_1	10
a_1	5
a_2	5
V_f	1.2
V_r	-0.5

When initializing a memristor to R_{ON} use $x = 2$, and when initializing to R_{OFF} use $x = -2$.



a. What are the constraints for V_0 that guarantee: (1) the output is correctly computed (NOR gate), and (2) the input memristor states are preserved? Assume that the output memristor is initialized to R_{ON} and that $V_0 \geq 0$.

b. According to the memristor parameters given in the above table, choose a valid value for V_0. What value did you choose?

c. Simulate the MAGIC NOR gate with the parameters in this question for the following cases:

(a) Both input memristors are in the low resistive state ($R_{in_1} = R_{in_2} = R_{ON}$)

(b) The first input memristor is in the low resistive state and the second input memristor is in the high resistive state ($R_{in_1} = R_{ON}$ and $R_{in_2} = R_{OFF}$)

(c) Both input memristors are in the high resistive state ($R_{in_1} = R_{in_2} = R_{OFF}$)

Provide the schematic for the circuit. For each case, provide and explain the following waveforms:

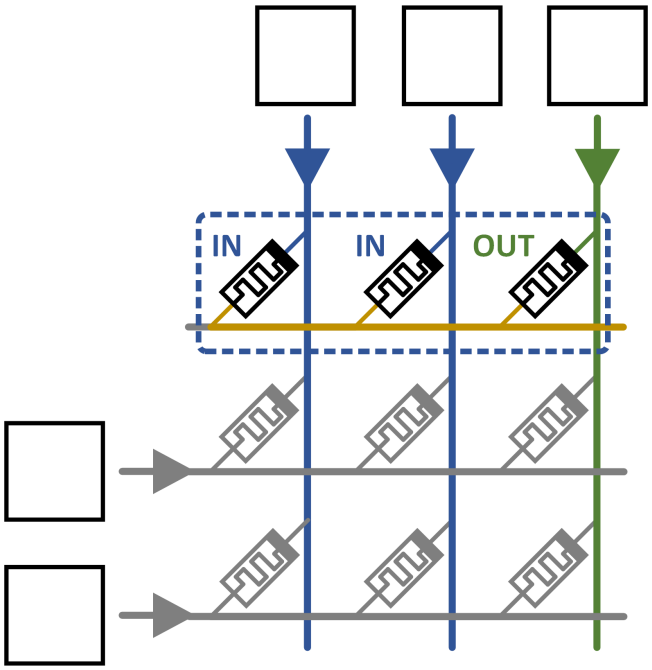
(a) The input voltage $V_0(t)$
(b) The resistance of the first input memristor R_{in_1}
(c) The resistance of the second input memristor R_{in_2}
(d) The resistance of the output memristor R_{out}

Use the following voltage source:

Parameter	Value
V_1 (V1)	0
V_2 (V2)	From Question (b)
t_{delay} (Td)	$10m$
t_{rise} (Tr)	$1n$
t_{fall} (Tf)	$1n$
t_{on} (Ton)	$10m$
t_{period} (Tperiod)	$30m$

with a simulation time of $30ms$.

d. Fill in the voltage values (i.e., numbers) in the below diagram that will lead to a MAGIC NOR gate in **only** the first row of the 3×3 crossbar.



Guidance: First fill in the voltages that will enable the MAGIC NOR gate in the first row, and then find the constraints for the remaining voltages so that the other two rows will not switch. Choose explicit values for those remaining voltages.

e. Simulate the circuit of (d) in LTspice with the following initial memristor states

$$\begin{pmatrix} 0 & 1 & 1 \\ 0 & 1 & 1 \\ 0 & 0 & 0 \end{pmatrix}$$

to demonstrate a valid MAGIC NOR gate in the first row and unchanged states for the second and third rows. Provide the schematic of the circuit. Provide and explain the following waveforms:

- The resistances of each of the memristors in the first row over time
- The resistances of the remaining two memristors in the last column over time

Please clarify in the text or on the waveform which memristor corresponds to which plot.