Memristors HW2

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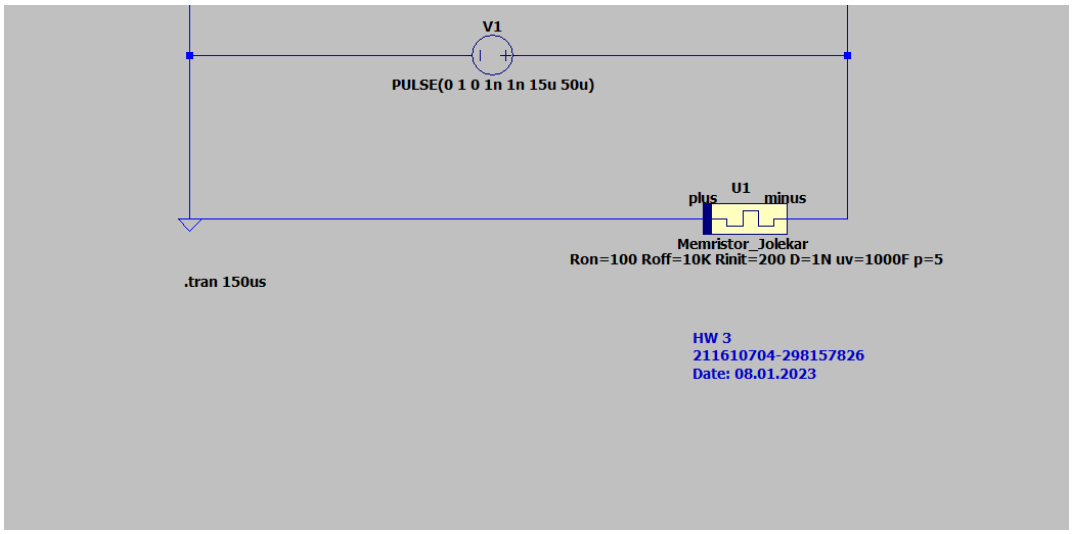
Contents

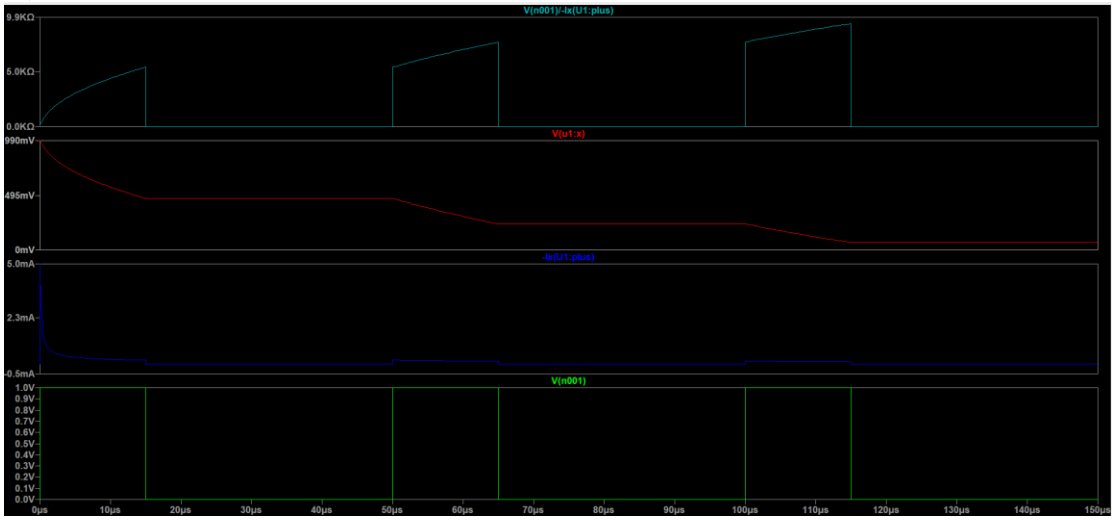
Question 1 – Multi-level cells (MLC)

Part a :

Circuit –



Plot –



Explanation –

Green graph : We can see that the input voltage is a pulse train that swings between 0 and 1.

Blue graph : We get the maximum value of the current when we at 200ohm resistance(lowest) and then the current decreases and the state get lower, resistance increases.

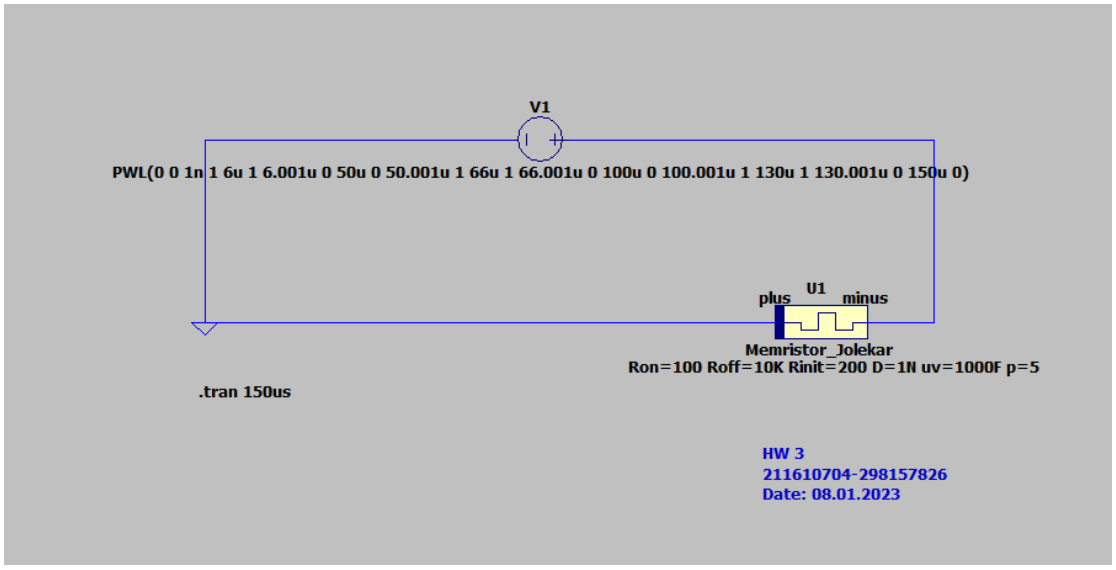
Red graph : from the graph we can see that the state variable is not linear and it decreases in each voltage pulse as expected from the tutorial.

Light blue : The resistance increases with each pulse, in a result of that the state variable decreases.

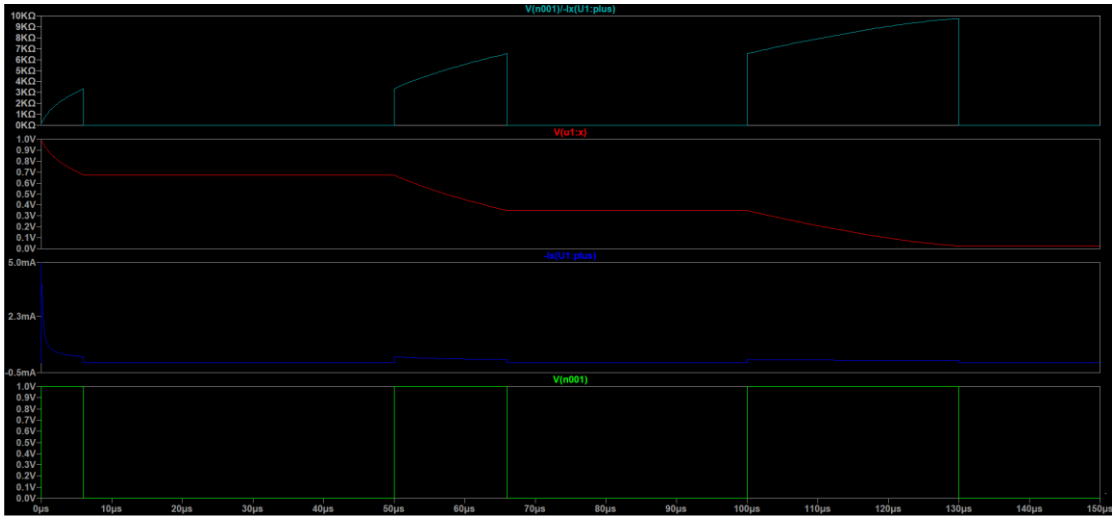
There is 4 levels of resistance – 200ohm, 5.4Kohm, 7.6Kohm, 9.3Kohm.

Part b –

Circuit –



Plot –

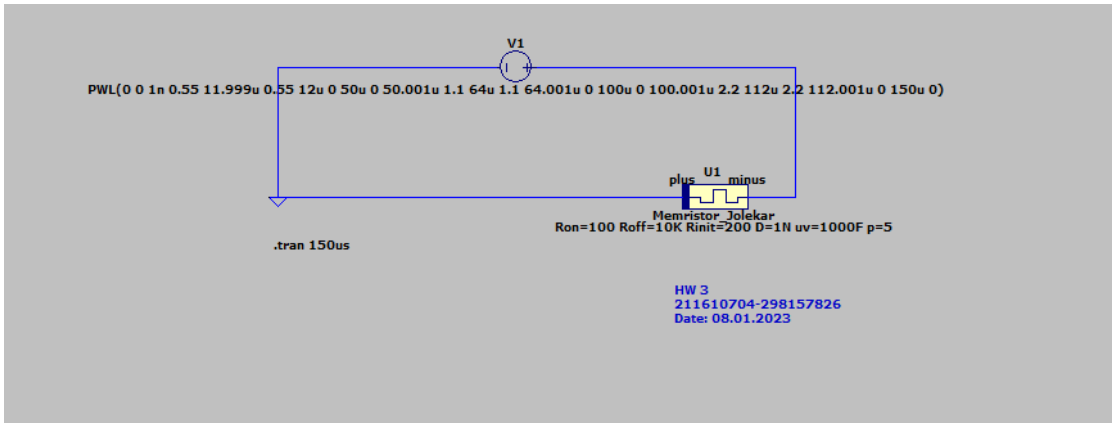


Explanation –

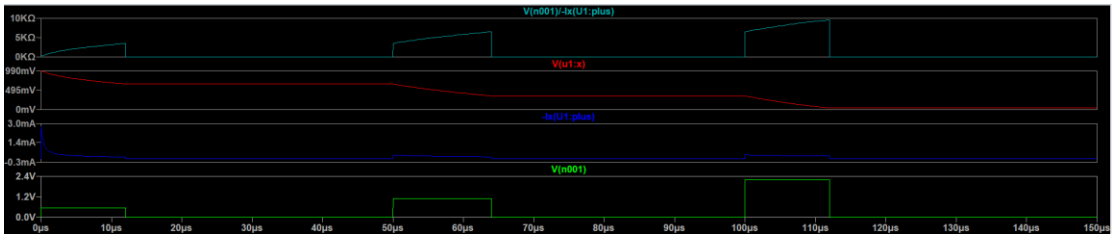
In order to makes the 4 levels of resistances uniform in the range [RON,ROFF] we need to use these pulse durations: $Pulse1$_width ≈ 6μs ⇒ $Ron \rightarrow$ 3.3$K\Omega$ $Pulse2$_width ≈ 16.9μs ⇒ 3.3$K\Omega \rightarrow$ 6.59$K\Omega$ $Pulse3$_width ≈ 32.2μs ⇒ 6.59$K\Omega \rightarrow$ 9.9$K\Omega$

Part c –

Circuit –



Plot –

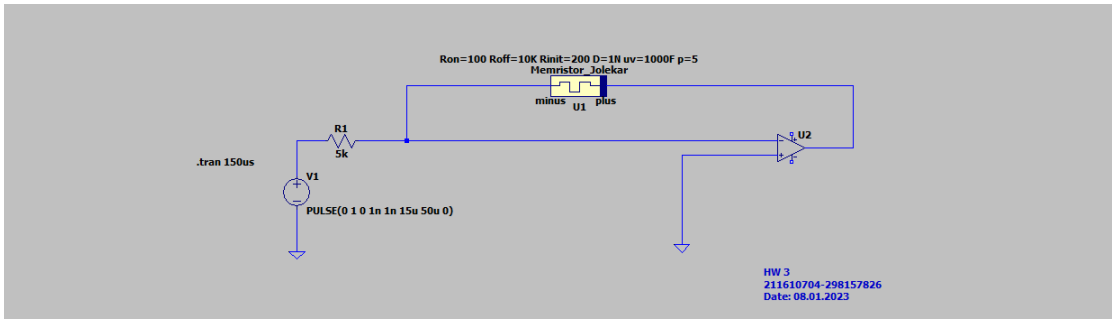


Explanation –

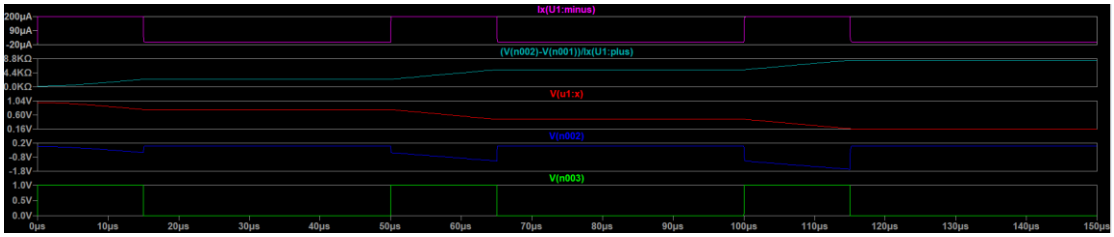
To get an approximately uniform resistance, We chose V1=0.55V for 10.999usec and V2=1.1V for 13.999usec and V3=2.2V for 11.999usec.

Part d –

Circuit –



Plot –



1st graph is the current that passes through the memristor , 2nd graph is the Resistance , 3rd graph is the Memristor state, 4th graph is the voltage the falls on the memristor and 5th graph is the input voltage.

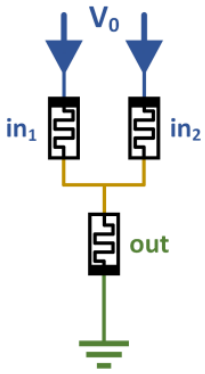
We used step param to determine which Rin to choose that will give us uniform resistance (200ohm, 3.32Kohm, 6.6Kohm, 10Kohm) and we found that Rin = 5Kohm will give us this result.

Question 2 – stateful logic (MAGIC)

$$\frac{dx}{dt} = \begin{cases} e^{a_1 - x} & v > V_f \\ 0 & V_r \leq v \leq V_f \\ -e^{a_2 + x} & v < V_r \end{cases}$$

$$R(x) = \begin{cases} R_{ON} & x \geq 0 \\ R_{OFF} & x < 0 \end{cases}$$

Parameter	Value
R_0	$1k$
R_1	10
a_1	5
a_2	5
V_f	1.2
V_r	-0.5



Part-a

Writing down the constraints will lead to the following assumption:

$$when\ \{in_1 = 0, in_2 = 0\} \rightarrow V_{out} < Vt_{off}$$

$$(1)\ V_o * 2 * \frac{R_{on}}{R_{on} + R_{on}} < Vt_{off} \rightarrow V_0 < |V_f|$$

$$when\ \{in_1 = 1, in_2 = 0\}\ or\ \{in_1 = 0, in_2 = 1\}\ or\ \{in_1 = 1, in_2 = 1\} \rightarrow Vt_{off} < V_{out}$$

$$(2)\ 2 * |V_r| < V_o < |V_r| * \frac{R_{off}}{2R_{on}}$$

Part-b

We plug the numbers from the table above and get:

$$V_0 < 1.2$$

$$1 < V_o < 25$$

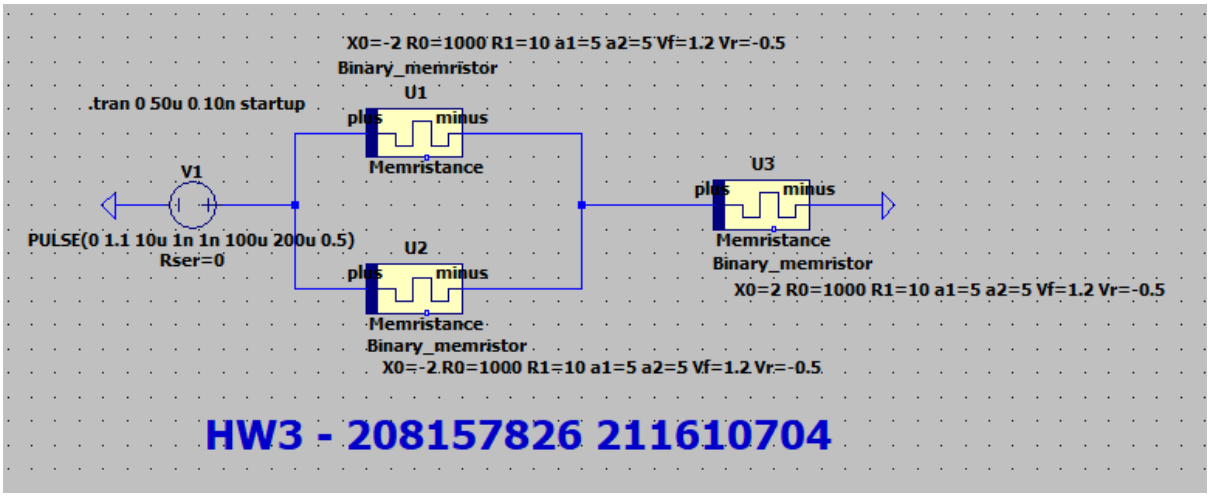
In the end the constraint is:

$$1 < V_o < 1.2$$

We choose $V_o = 1.1$

Part-c

Following schematics



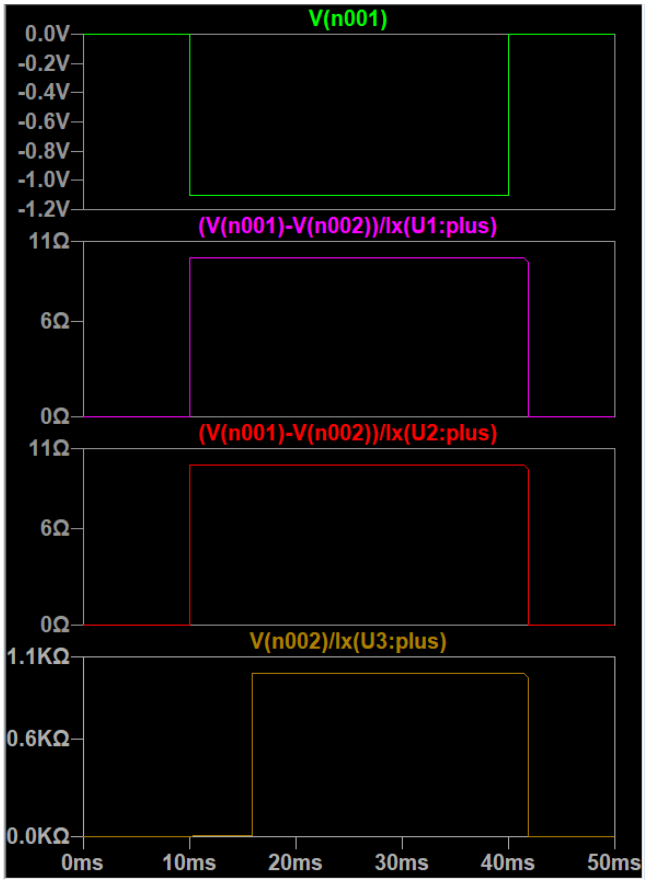
Source voltage in **Green**: V(n001): notice it is negative this is due to the polarity of the memristors.

Resistance of U1 in **Purple**: (V(n001)-V(n002))/I(U1)

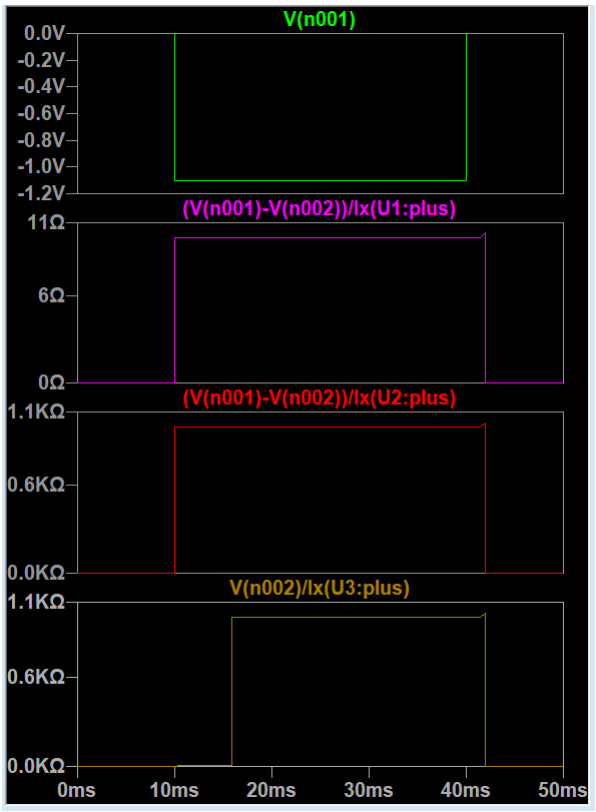
Resistance of U2 in **Red**: (V(n001)-V(n002))/I(U2)

Resistance of U3 in **Gold**: V(n002)/I(U3)

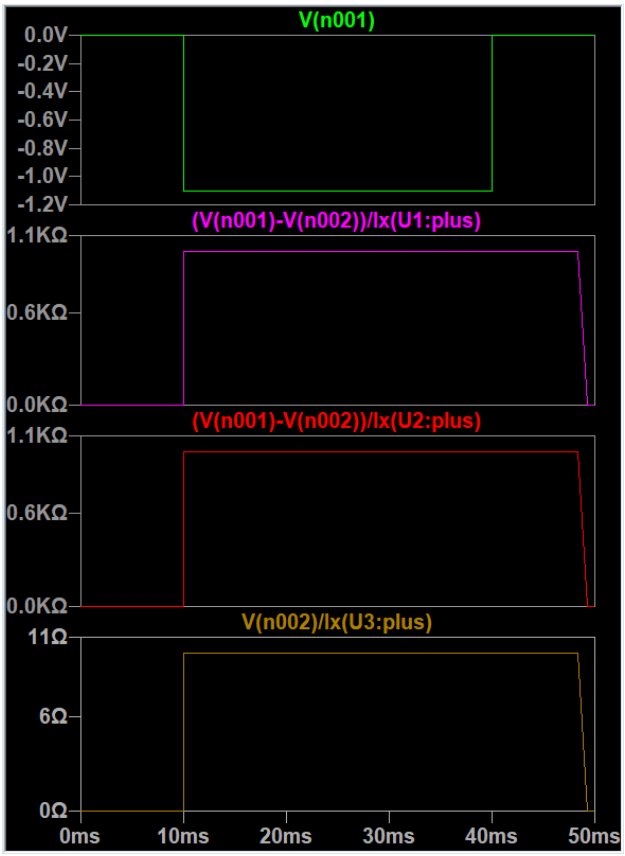
a. $\{in_1 = R_{on}, in_2 = R_{on}\}$



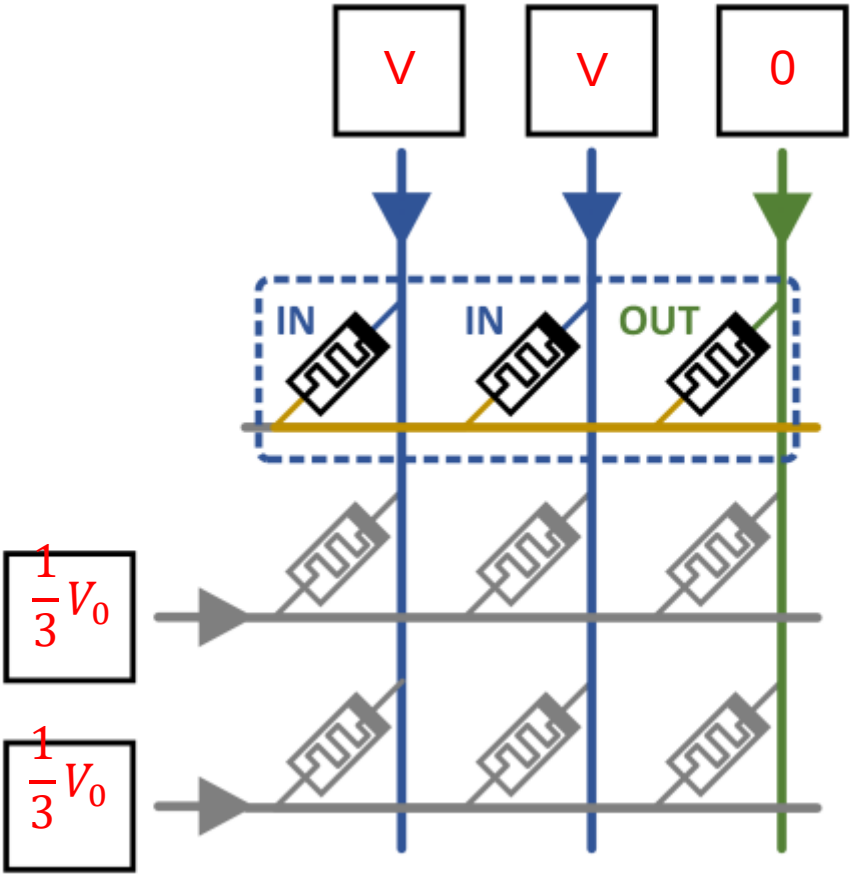
b. $\{in_1 = R_{on}, in_2 = R_{off}\}$



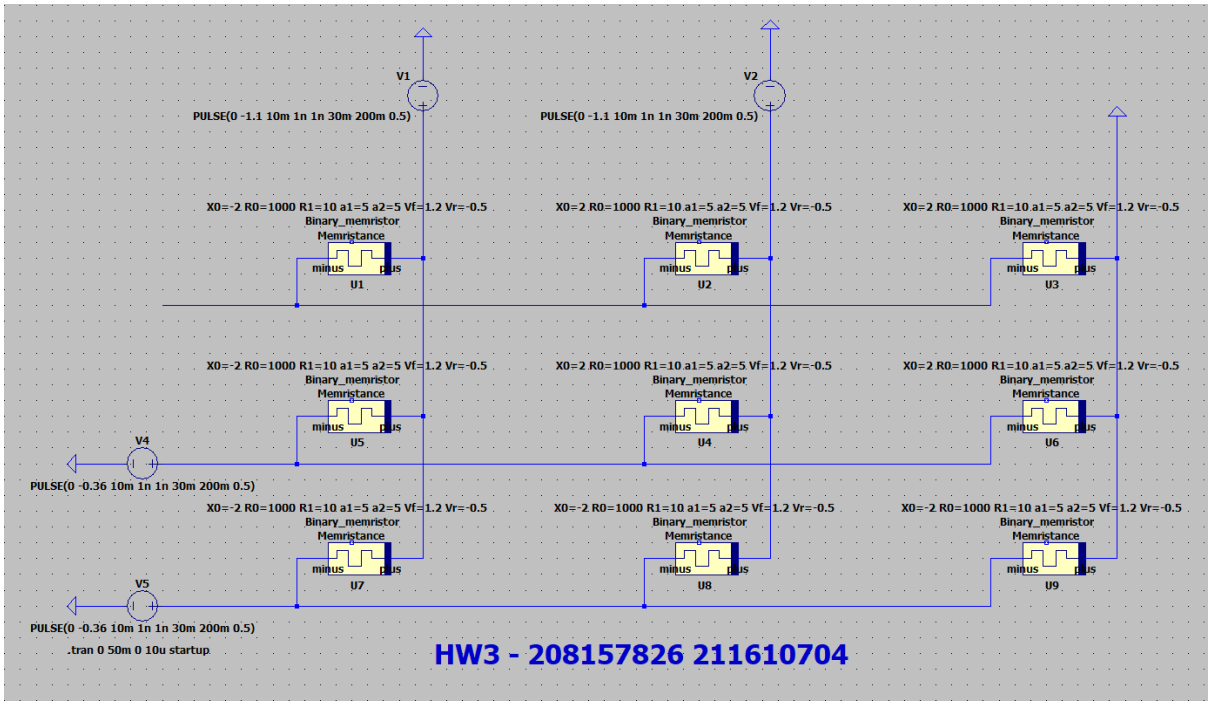
c. $\{in_1 = R_{off}, in_2 = R_{off}\}$


V(n001)
0.0V
-0.2V
-0.4V
-0.6V
-0.8V
-1.0V
-1.2V
(V(n001)-V(n002))/Ix(U1:plus)
1.1KΩ
0.6KΩ
0.0KΩ
(V(n001)-V(n002))/Ix(U2:plus)
1.1KΩ
0.6KΩ
0.0KΩ
V(n002)/Ix(U3:plus)
11Ω
6Ω
0Ω
0ms
10ms
20ms
30ms
40ms
50ms

Part-d


V
V
0
IN
IN
OUT
$\frac{1}{3}V_0$
$\frac{1}{3}V_0$

Part-e



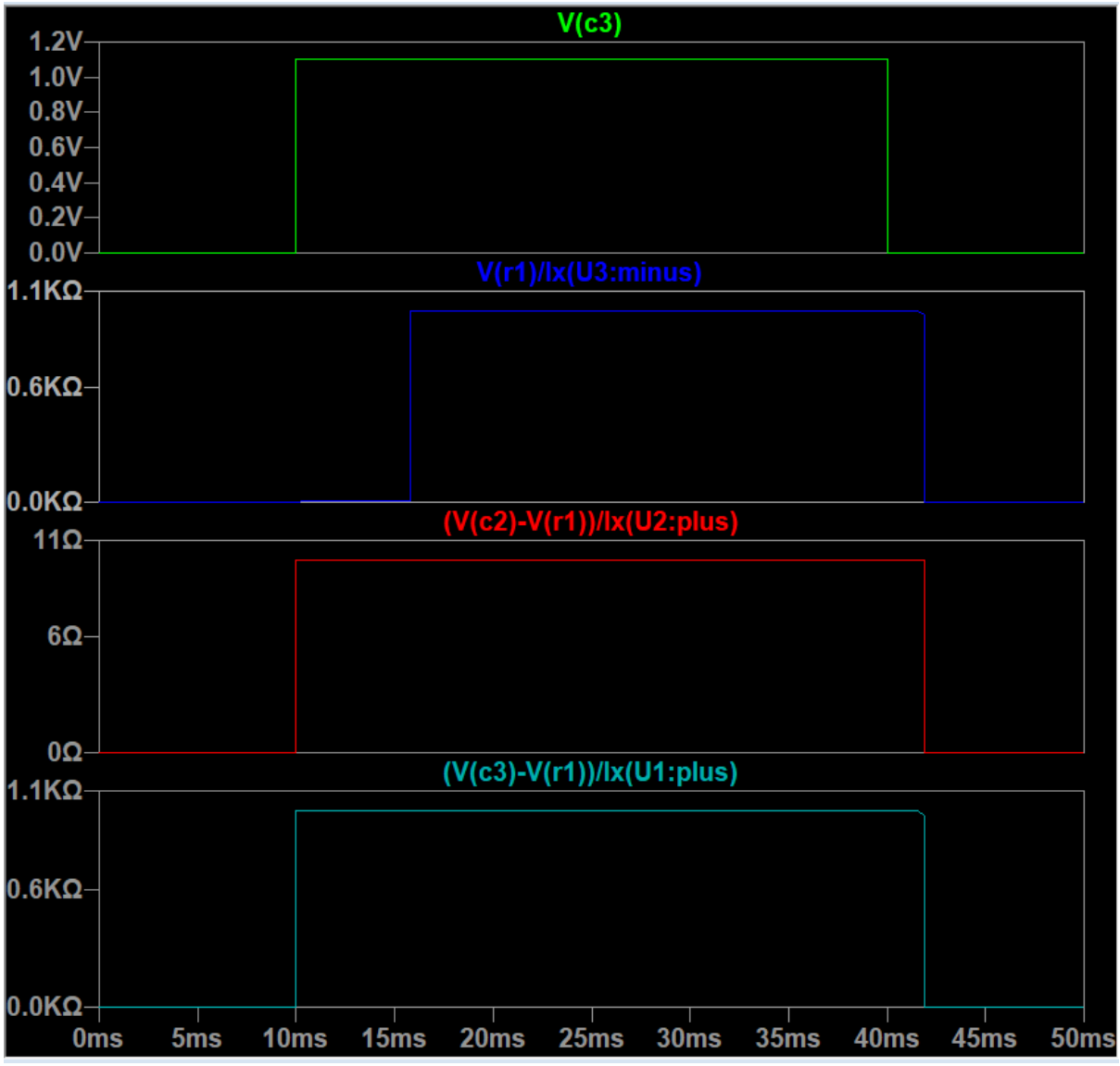
Source voltage in **Green** (V0)

Resistance of U3 in **Blue**

Resistance of U2 in **Red**

Resistance of U1 in **Cayan**

First Row memristors :



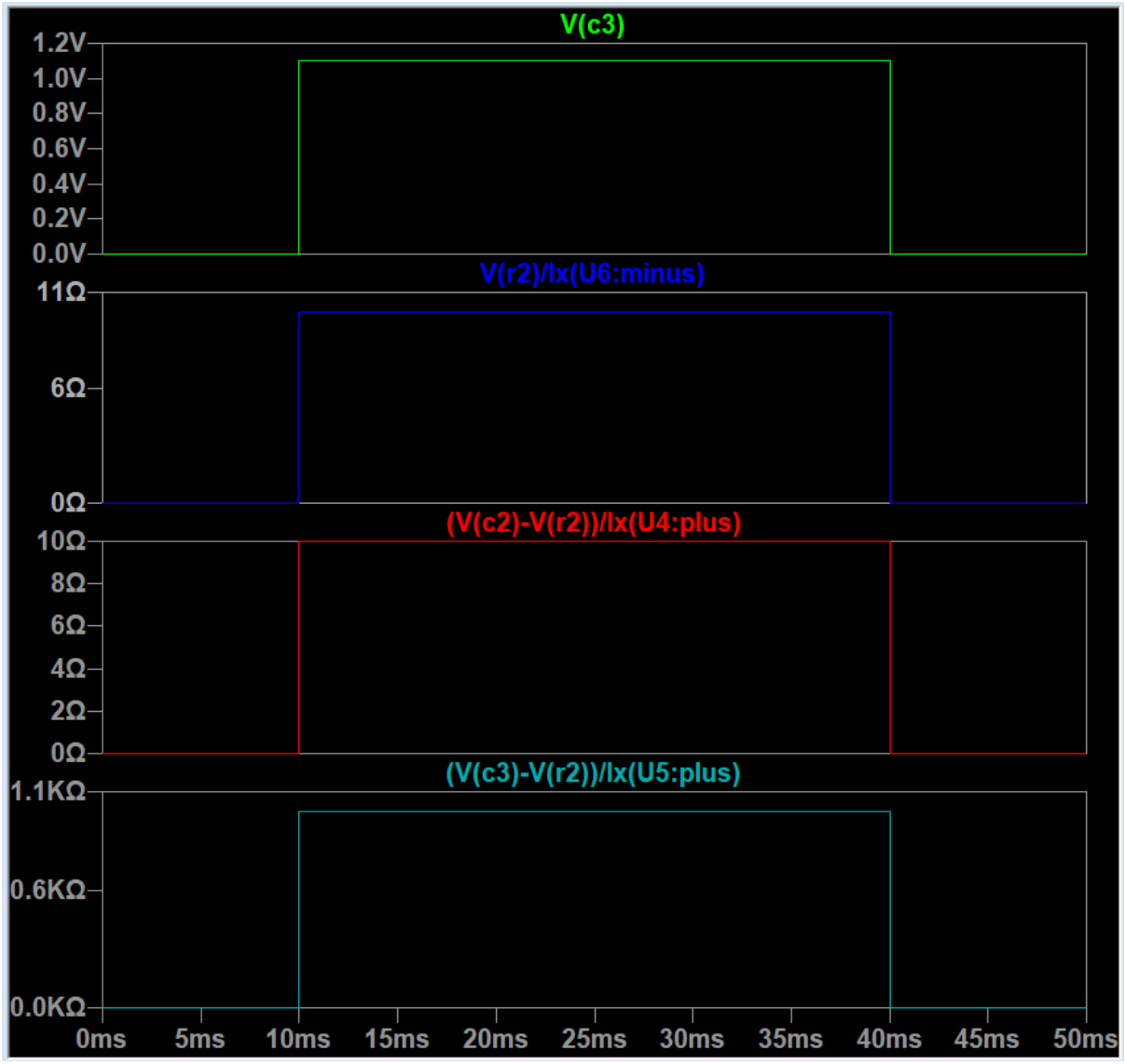
Source voltage in **Green** (V0)

Resistance of U6 in **Blue**

Resistance of U4 in **Red**

Resistance of U5 in **Cayan**

Second Row memristors:



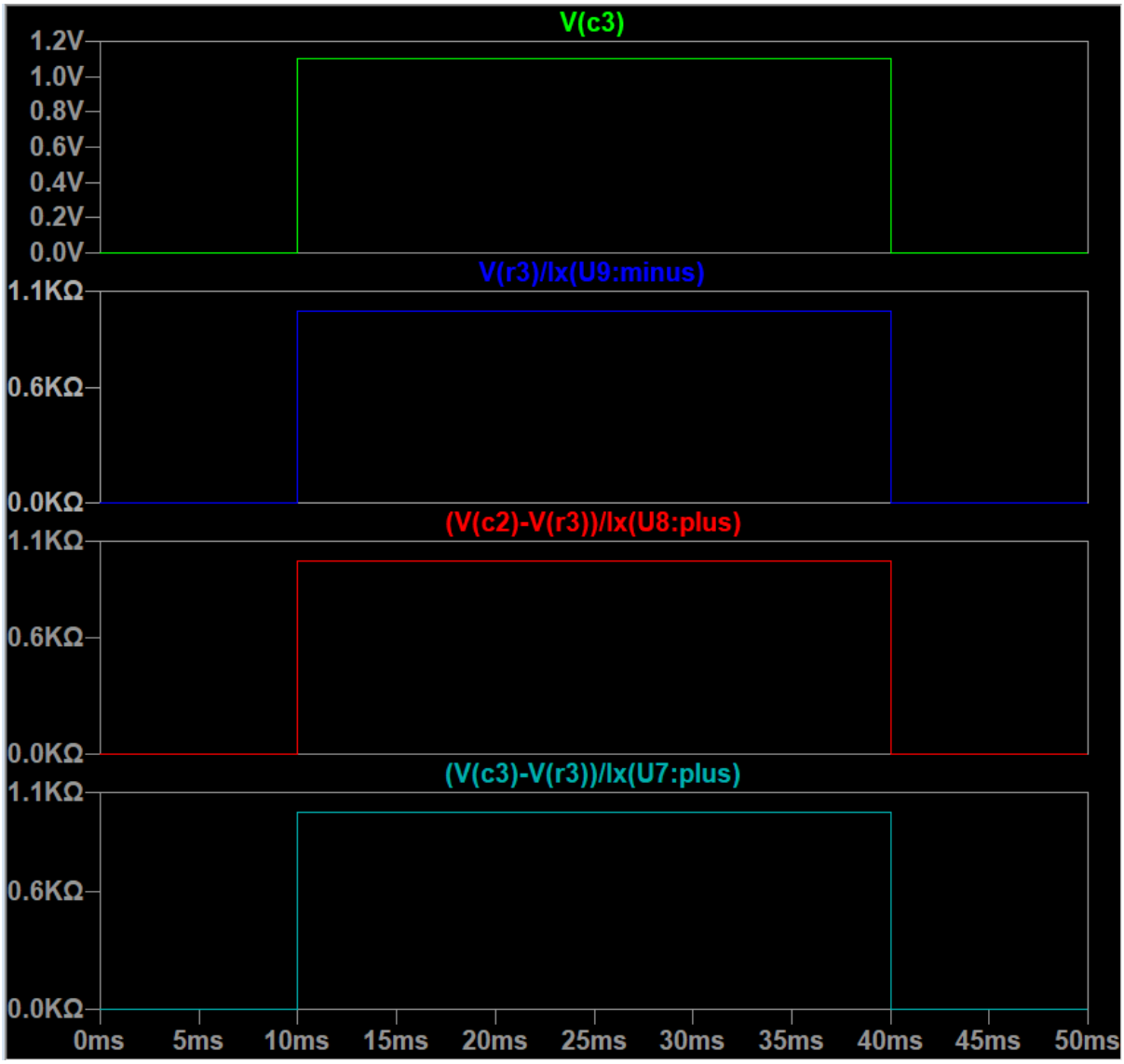
Source voltage in **Green** (V0)

Resistance of U9 in **Blue**

Resistance of U8 in **Red**

Resistance of U7 in **Cayan**

third Row memristors:


V(c3)
1.2V
1.0V
0.8V
0.6V
0.4V
0.2V
0.0V
V(r3)/Ix(U9:minus)
1.1KΩ
0.6KΩ
0.0KΩ
(V(c2)-V(r3))/Ix(U8:plus)
1.1KΩ
0.6KΩ
0.0KΩ
(V(c3)-V(r3))/Ix(U7:plus)
1.1KΩ
0.6KΩ
0.0KΩ
0ms
5ms
10ms
15ms
20ms
25ms
30ms
35ms
40ms
45ms
50ms