Memristors HW3

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# Question 1 – Multi-level cells (MLC)

## Part-a

## Part-b

## Part-c

## Part-d

# Question 2 – stateful logic (MAGIC)

Table

Description automatically generatedDiagram, schematic

Description automatically generatedText, letter

Description automatically generated

## Part-a

Writing down the constraints will lead to the following assumption:

## Part-b

We plug the numbers from the table above and get:

In the end the constraint is:

We choose

## Part-c

Following schematics

Timeline

Description automatically generated

Source voltage in **Green**: V(n001): notice it is negative this is due to the polarity of the memristors.

Resistance of U1 in **Purple**: (V(n001)-V(n002))/I(U1)

Resistance of U2 in **Red**: (V(n001)-V(n002))/I(U2)

Resistance of U3 in **Gold**: V(n002)/I(U3)

A screenshot of a computer

Description automatically generated with medium confidence

A picture containing diagram

Description automatically generated

A picture containing chart

Description automatically generated

## Part-d

Diagram

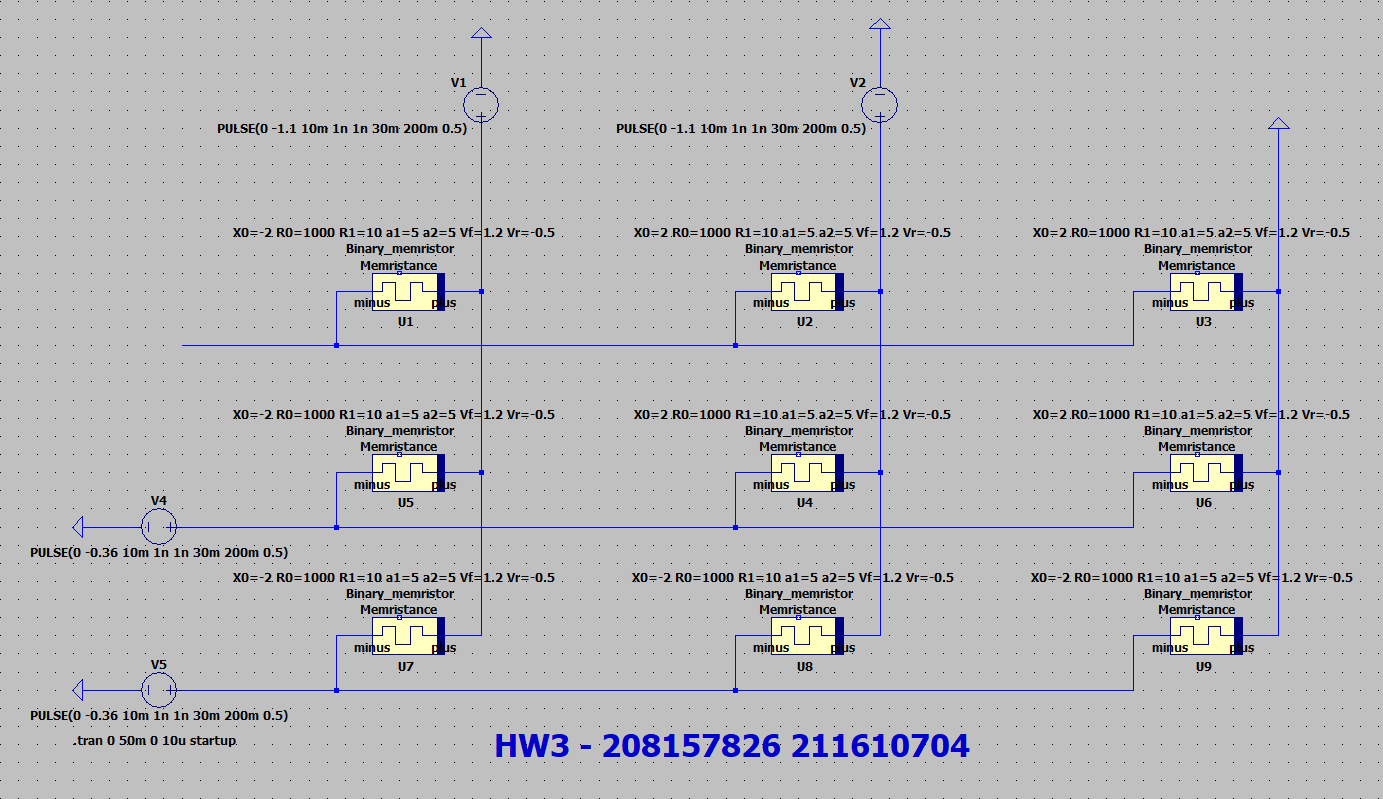
Description automatically generated

0

V0

V0

## Part-e



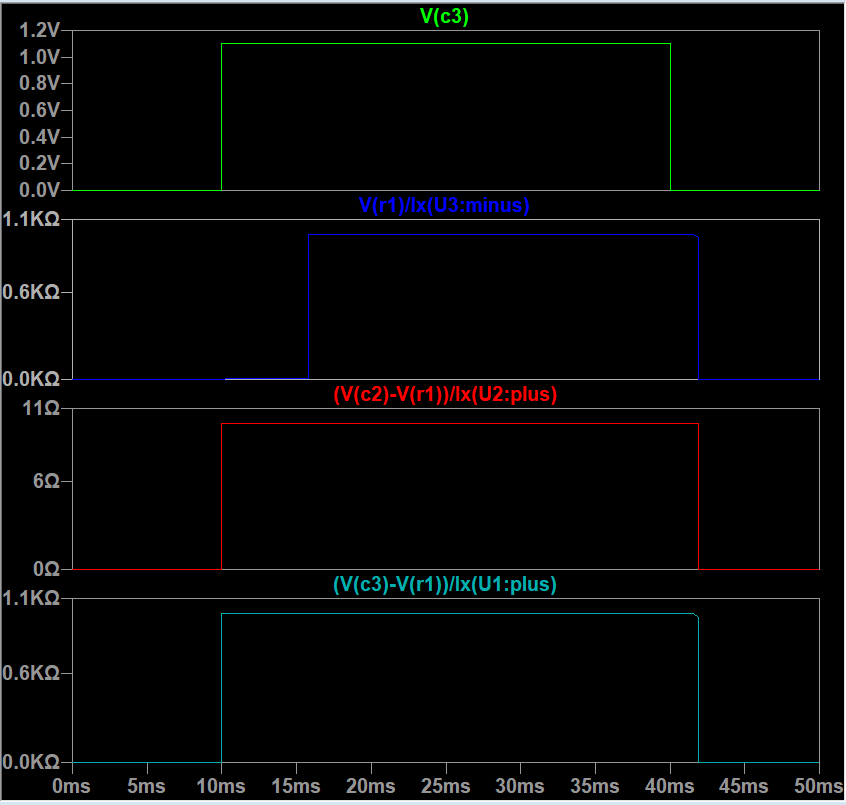
Source voltage in **Green** (V0)

Resistance of U3 in **Blue**

Resistance of U2 in **Red**

Resistance of U1 in **Cayan**

First Row memristors :



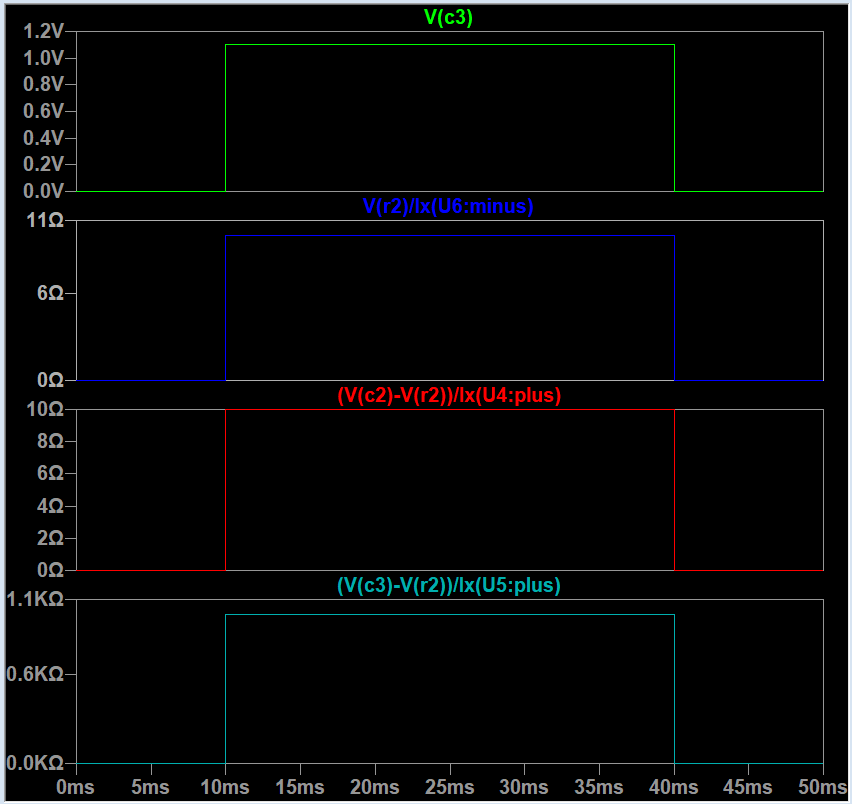
Source voltage in **Green** (V0)

Resistance of U6 in **Blue**

Resistance of U4 in **Red**

Resistance of U5 in **Cayan**

Second Row memristors:



Source voltage in **Green** (V0)

Resistance of U9 in **Blue**

Resistance of U8 in **Red**

Resistance of U7 in **Cayan**

third Row memristors:

