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VI. Discuss the leakage current issue and why it occurs. How does leakage current appear in the described system? Discuss how to modify the inverter in order to show the leakage current. Discuss the leakage currents in 2- and 3-level inverters. 31

Reference

Assignment 3 for 2019

ELEC 9711

Power Electronics for Renewable and Distributed Generation

Part-A

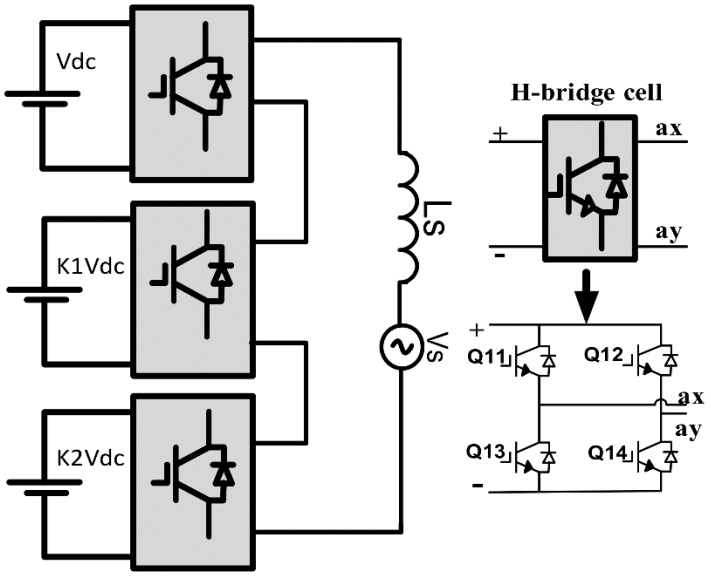


Figure 1: Single Phase Cascaded H-bridge Converter.

A modular cascaded H-bridge inverter topology for single-phase grid-connected PV system is shown in Figure 1. You need to design a 7-level CHB inverter topology using the phase-shifted carrier-based PWM scheme with unipolar modulation.

I.Design

To satisfy the requirement of this question, the design will be divided into two steps. The first step mainly focuses on designing main circuits. Three CHB inverters and dc voltage sources will be used to generate a seven-level output. The second step is to utilize bipolar modulation scheme with phase-shifted carrier-based SPWM technique to control switches.

Step one: The design of Main circuit:

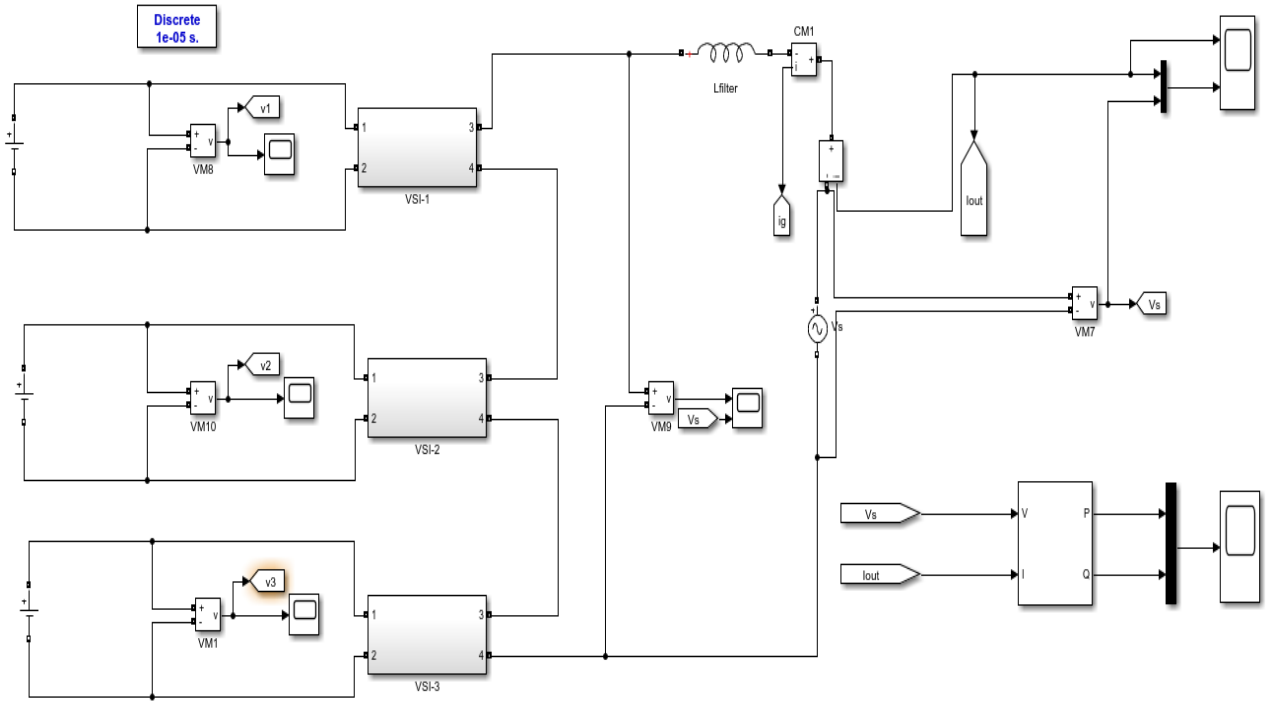


Figure 1.1 Main circuits with three CHB inverters

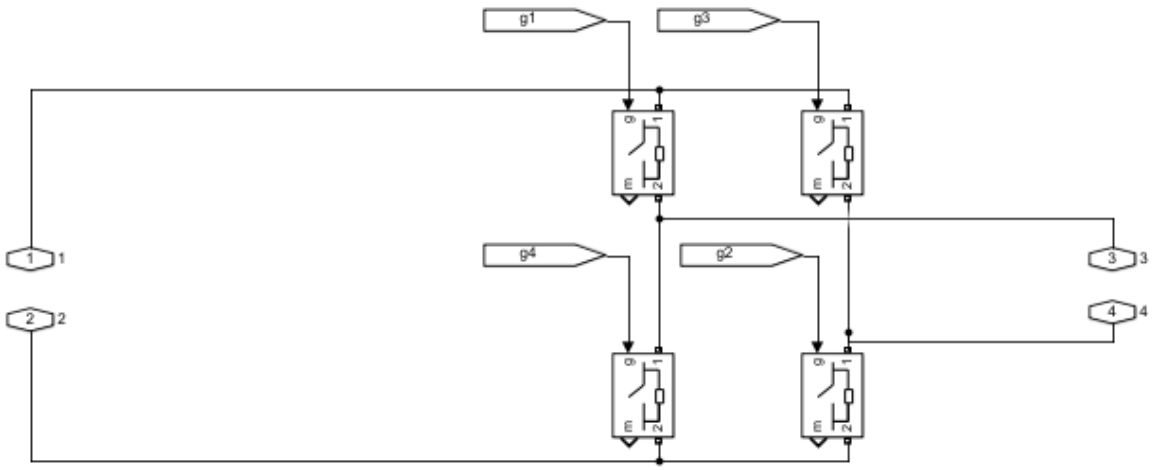


Figure 1. 2 VSI-1

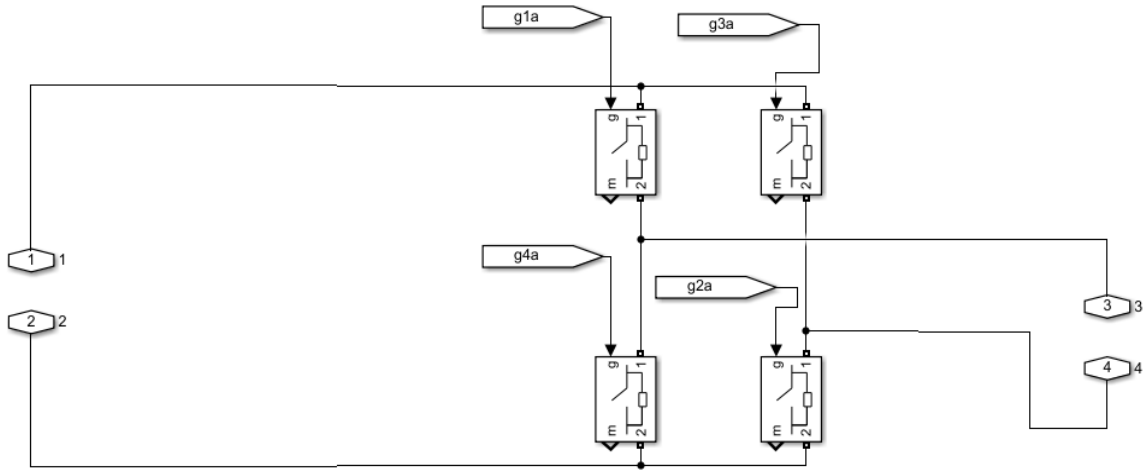


Figure 1.3 VSI-2

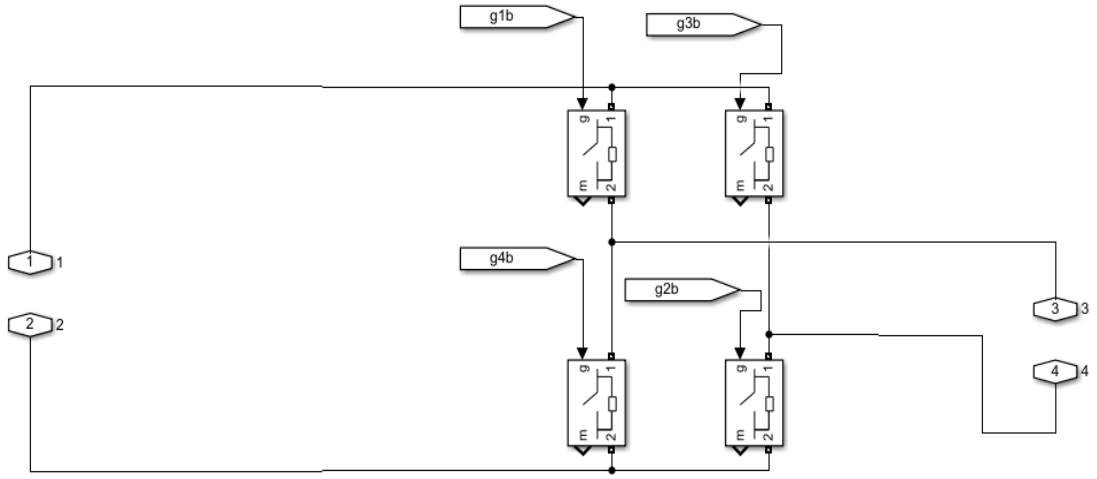


Figure 1. 4 VSI-3

Step Two: The design of SPWM using unipolar modulation

There are two types of unipolar switching. Type one operates both switches pairs at a high frequency. Type two uses a high frequency for one pair and a low frequency for the other pair of switches. We will be building a type two unipolar PWM inverter because it is simpler than type one. To build such PWM, two simulating signals which have 180 degree difference between them and a carrier signal should be used as figure below.

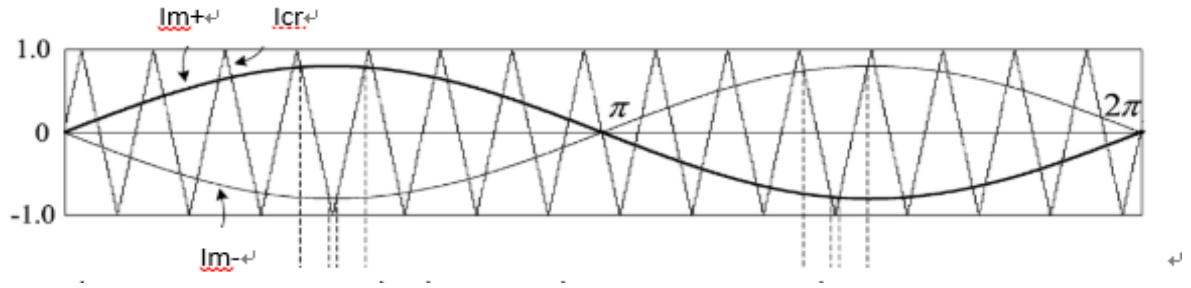


Figure 1.5 Unipolar stimulation

As figure1.2 shown, Im and Im- are simulating signals and Icr is the carrier signal.

In this case, the simulating signal is the generated by a simple feedback process. Firstly, the reference current, which is the desired output current, will compare with the measured current and generate a new current. After PID control, the new current will be compared with the carrier signal to obtain the gate signals. Because there are three CHB bridges, each simulating signals are supposed to control six switches. Also, to obtain a 7-level voltage, there is a phase shift between any two adjacent carrier wave. The phase shift is 120 degree. The gate signals are generated with proper comparison of carrier wave and modulating signal. The gate signals are generated with proper comparison of carrier wave and modulating signal.

Reference current:

$$\mathrm{I_{reference}} = \frac{\mathrm{P}}{U} = \frac{100000}{\sqrt{2} \times 415} = 340A$$

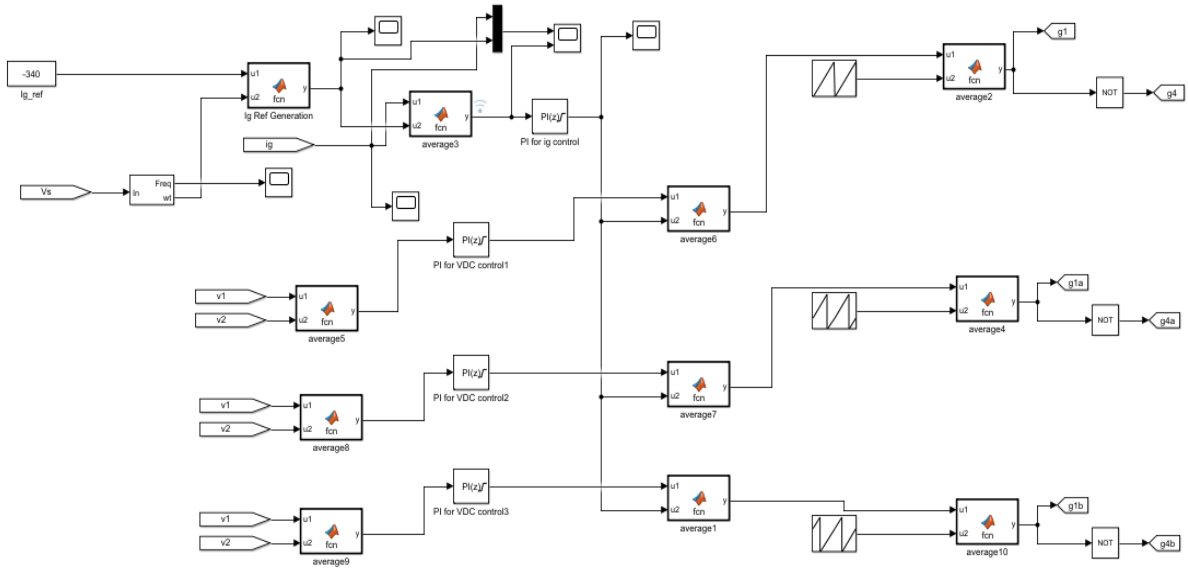


Figure 1.6 SPWM circuit when $\mathrm{I}_{reference}$ = -340 A

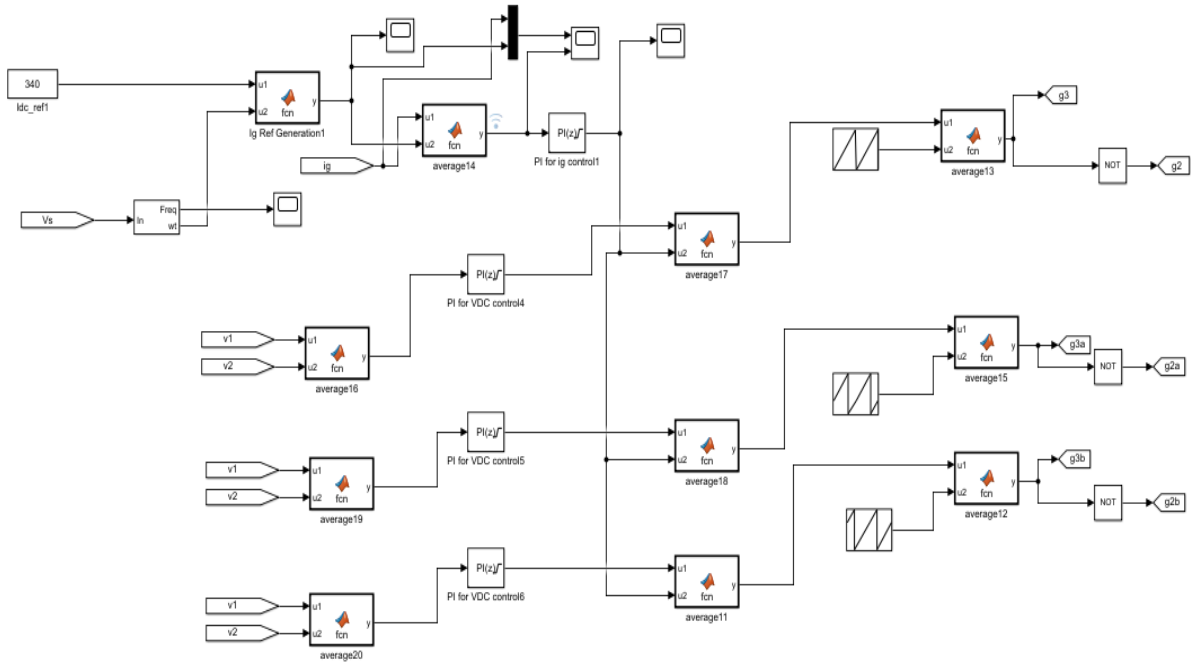


Figure 1.7 SPWM circuit when $I_{reference}$ =340 A

Figure 1.6 shows the circuit for generating gate signal (g1, g4, g1a, g4a, g1b, g4b). g1, g4 controls switches in CHB1, g1a, g4a controls switches in CHB2, g1b, g4b controls switches in CHB3, At the same time, Figure 1.7 displays the circuit for generating gate signal (g2,g3, g2a, g3a, g2b,g3b).

Simulation Results

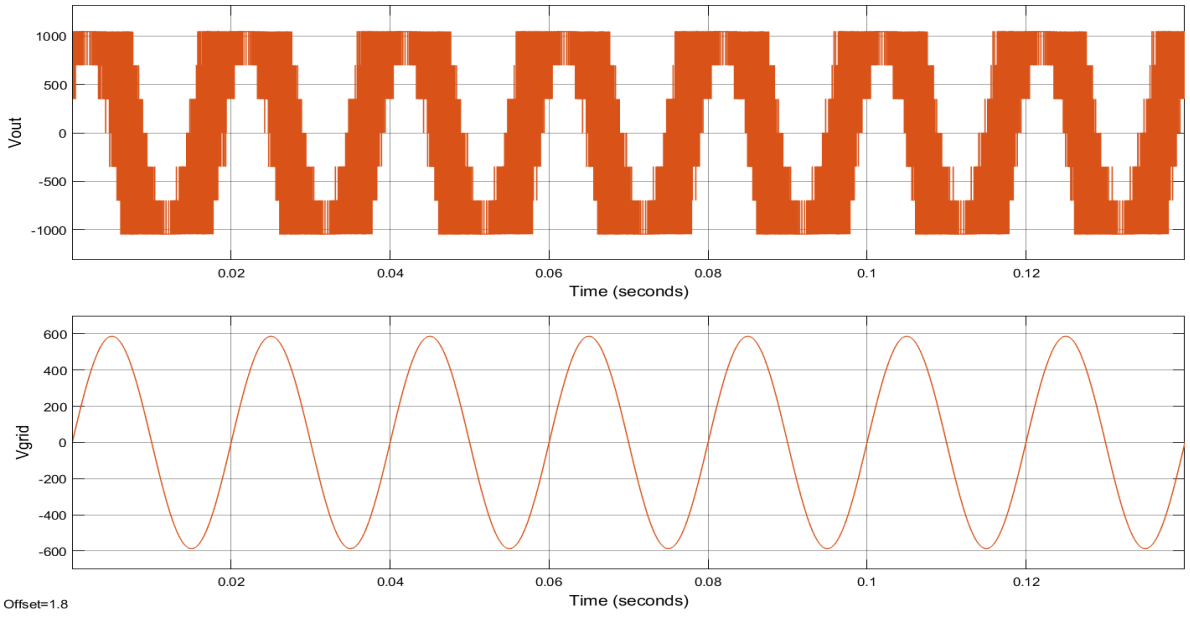


Figure 1.8 The output waveform of Inverter and the grid

Figure 1.8 shows that the number of output voltage level is 7 and the peak voltage of grid is 600. The design satisfy the requirement of the task.

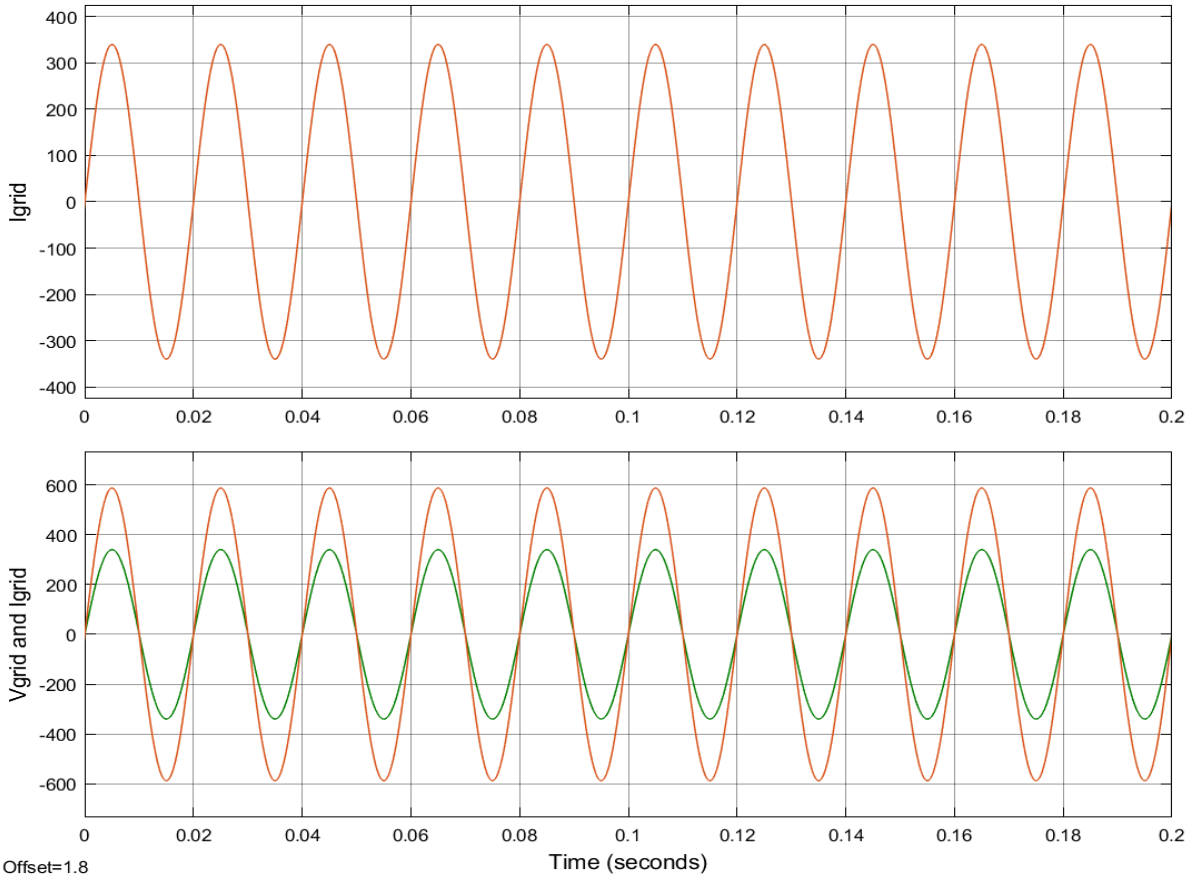


Figure 1.9 The waveform of Vgrid and Igrid

As shown in Figure 1.9, the peak vaule of Igrid is around 340A, which is almost the same as the reference value. Besides, the Vgrid and Igrid are in phase and the power factor is unity.

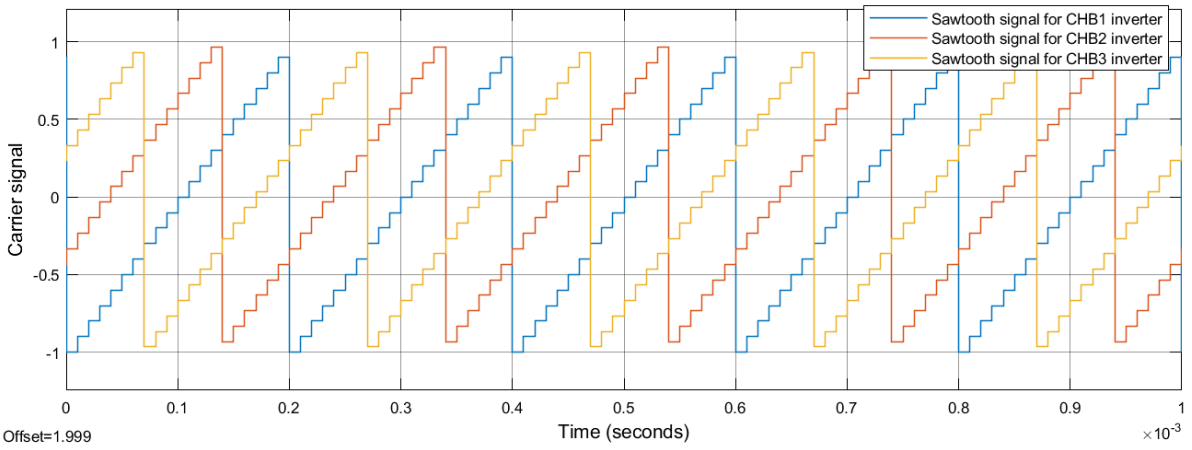


Figure 1.10 The waveform of carrier signals

As shown in Figure 1.10, three carrier signals with 120 degree angular difference between them are used to generate gate signal for CHB, CHB1 and CHB2 inverter respectively.

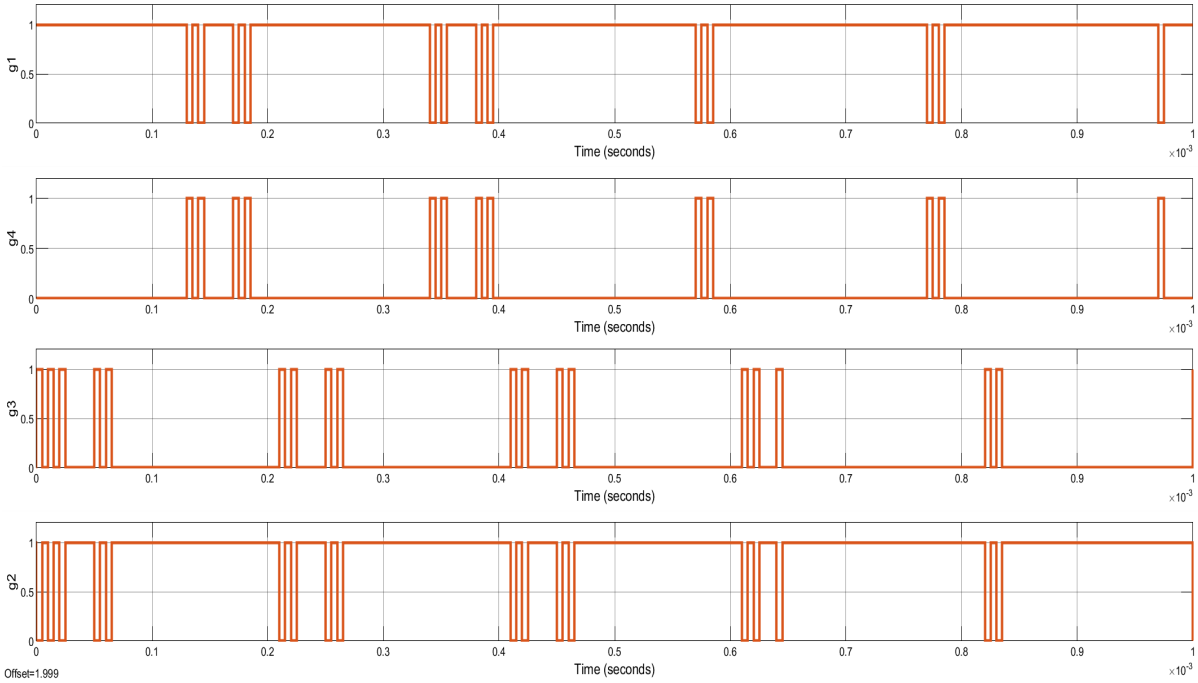


Figure 1.11 Gate signals for CHB1

From Figure1.11, we can see that the gate signal g1 and g4 is completely different(when g1=1, g4=0) and the gate signal g2 and g3 show the same pattern. This results proves that the unipolar modulation is successfully implemented.

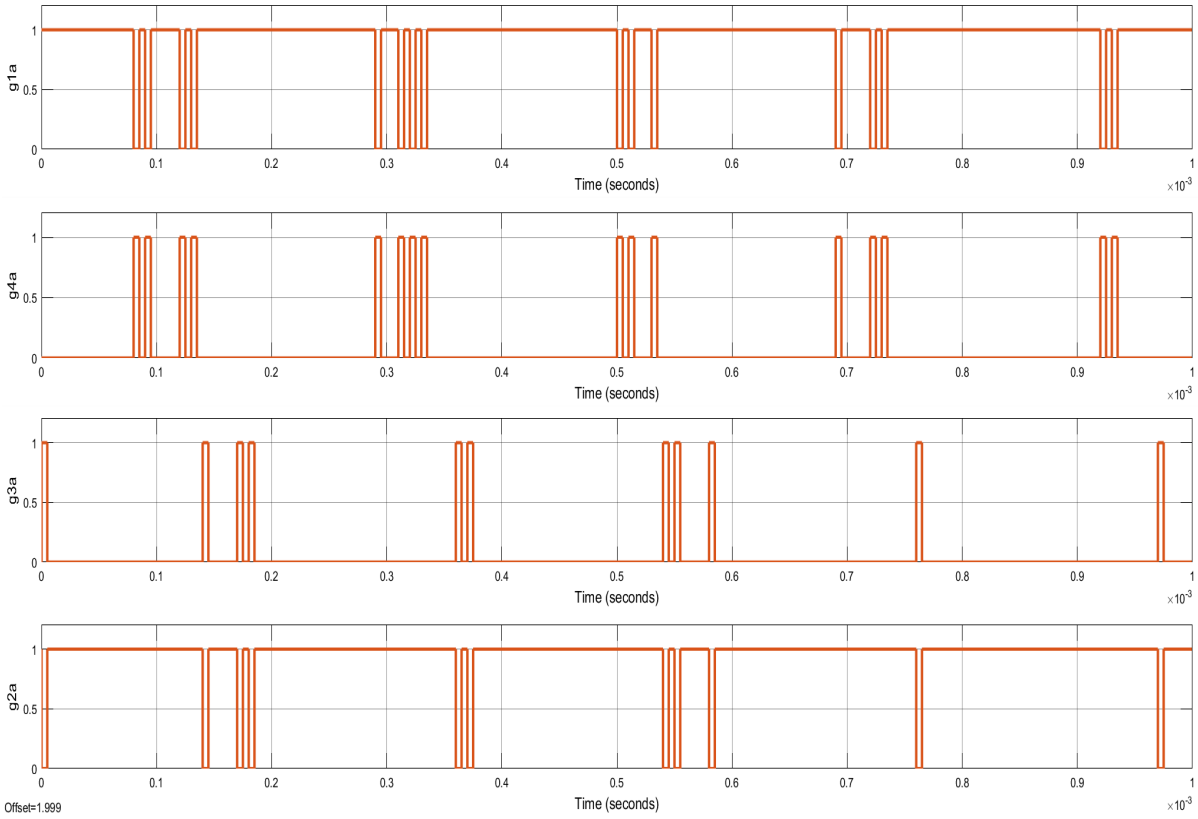


Figure 1.12 Gate signals for CHB2

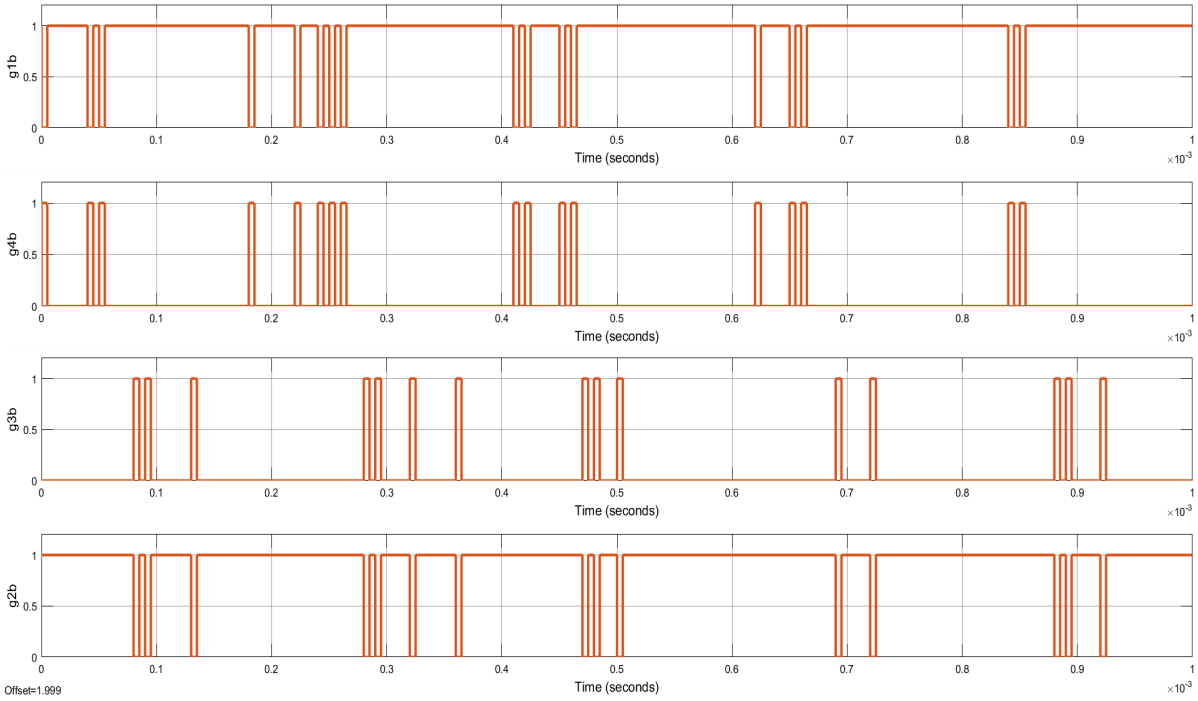


Figure 1.13 Gate signals for CHB3

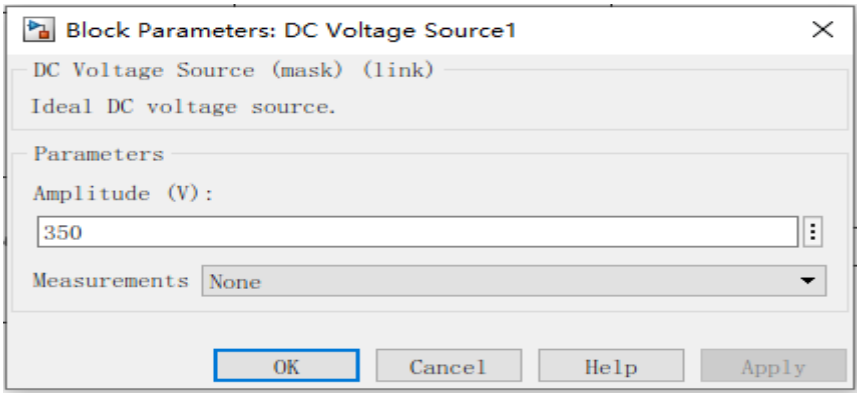


Figure 1.14 The value of DC voltage source

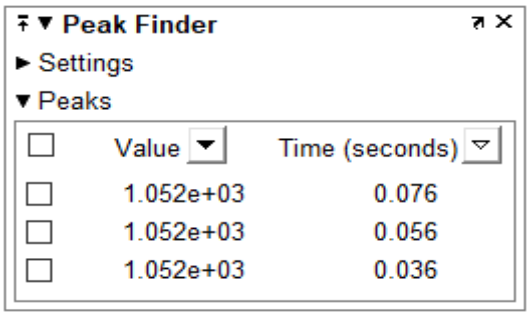


Figure 1.14 The peak value of output voltage

The modulation index:

$$\mathrm{m} = \frac{V_{out}}{V_{dc}} = \frac{1052}{3 \times 350} = 1.0019 \approx 1$$

Overmodulation:

For m > 1, over-modulation occurs.

$$\mathrm{m} = \frac{V_{out}}{V_{dc}} = \frac{750}{3 \times 200} = 1.25 \geq 1$$

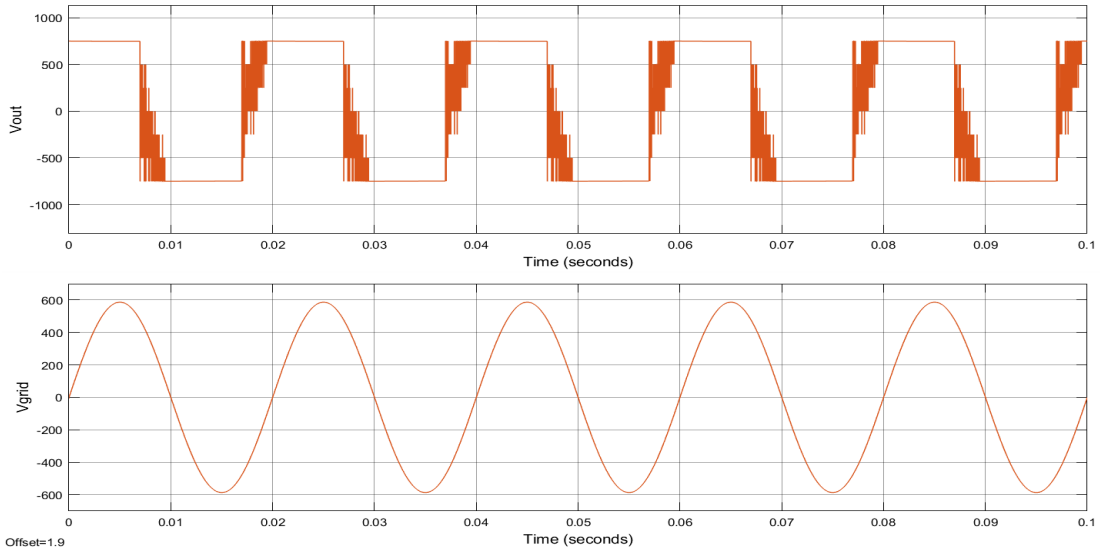


Figure 1.15 The waveform of output voltage

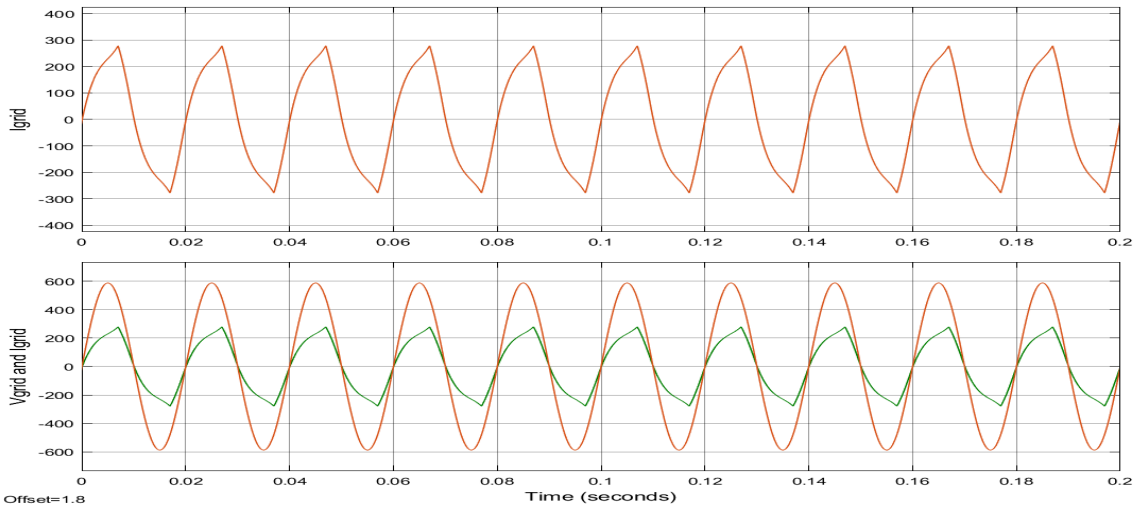


Figure 1.16 The waveform of output voltage and current

As shown in Figure 1.16, the grid current is not a sinusoidal waveform. Because of overmodulation, the number of lower order harmonics in the output voltage is increased. This

distorted voltage will result in a distorted output current. We can control m to avoid overmodulation.

II. *d-q* current control scheme

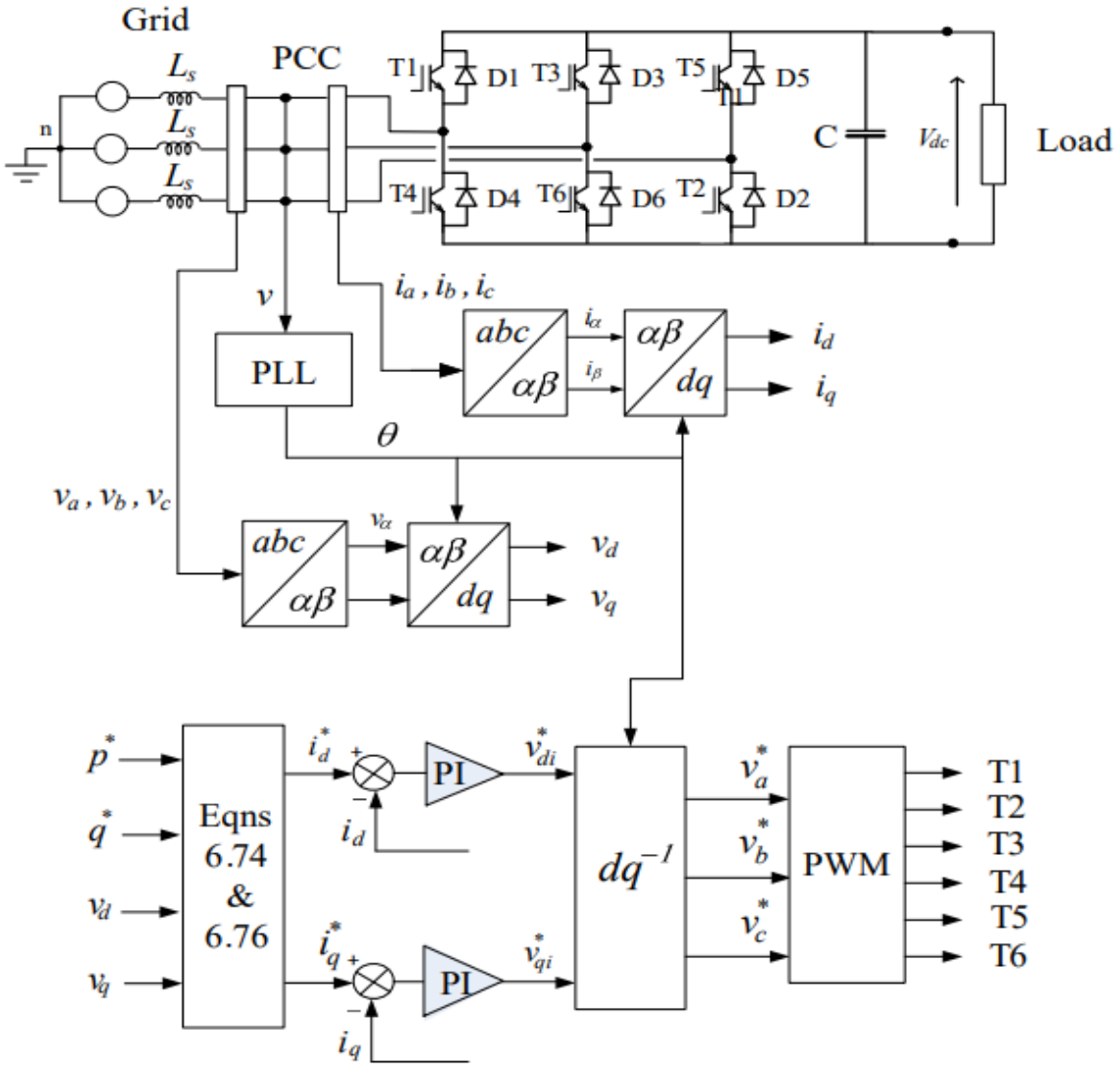


Figure 1.17 The current control Scheme without using instantaneous PQ theory

The current control scheme are often used with instantaneous PQ theory and dq control to better control the output of inverters.

Instantaneous PQ theory:

$$P_{\alpha\beta} = \frac{3}{2}(V_d I_d + V_q I_q)$$

$$Q_{\alpha\beta} = \frac{3}{2}(V_q I_d - V_d I_q)$$

The d-q control is using the abc to dq transformation module to transform the control variables from their natural frame abc to a frame that synchronously rotates with the frequency of the grid voltage. As a consequence, the control variables are becoming dc signals. This control structure is the necessity of information about the phase angle of utility voltage in order to perform the transformation. Normally, proportional–integral (PI) controllers are associated with this control structure. A typical transfer function of a PI controller is given by

$$PI(s)=Kp+Kis$$

where Kp is the proportional and Ki is the integral gain of the controller.

The implementation of current control scheme is quite simple . Firstly, voltages and currents at the PCC are measured and transformed into αβ frames and dq frames first. The PLL synchronizes voltage and obtains the angle of the voltage at the PCC. However, in stead of applying PQ theory with reference active and reactive power, we directly use the reference current calculated in last part to compare with the real-time current. After that, reference currents are to be regulated continuously by PI controllers which produces voltage references.

III. The phase-shifted and level-shifted carrier-based SPWM.

For level-shifted modulations, the carriers are distributed continuously and uniformly over the entire vertical extent of thus generating different levels of location for each carrier, i.e. a vertical carrier distribution [1]. This technique is divided into 3 types: In Phase disposition, Phase opposition disposition, alternate phase opposition disposition PWM.

For the phase-shifted modulation, all the carriers are arranged in the same phase. The PS modulations distribute the carriers at the same vertical level, but with a 360/N phase shift between them, thus characterizing a horizontal carrier distribution. PS modulation carriers may be sawtooth (SCRPWM) or triangular (PSCPWM). In this situation, we use 3 sawtooth waves with 120 degree phase shift twice to achieve our goal.

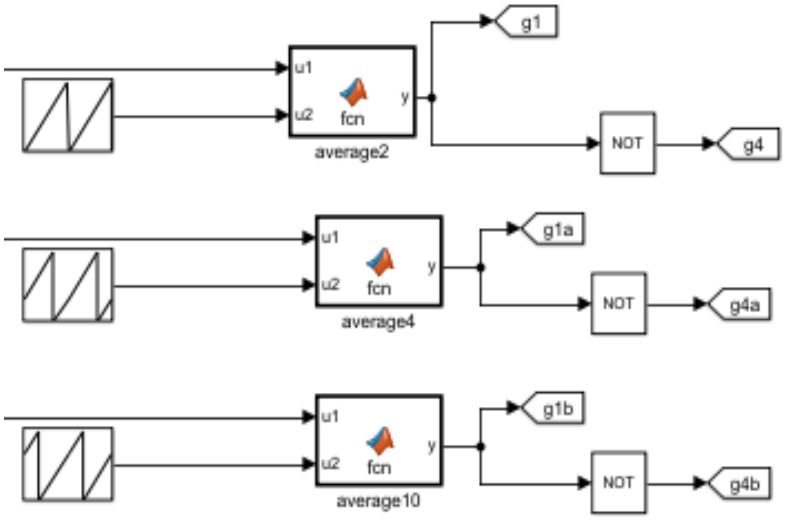


Figure 1.18 Phase-shifted based PWM

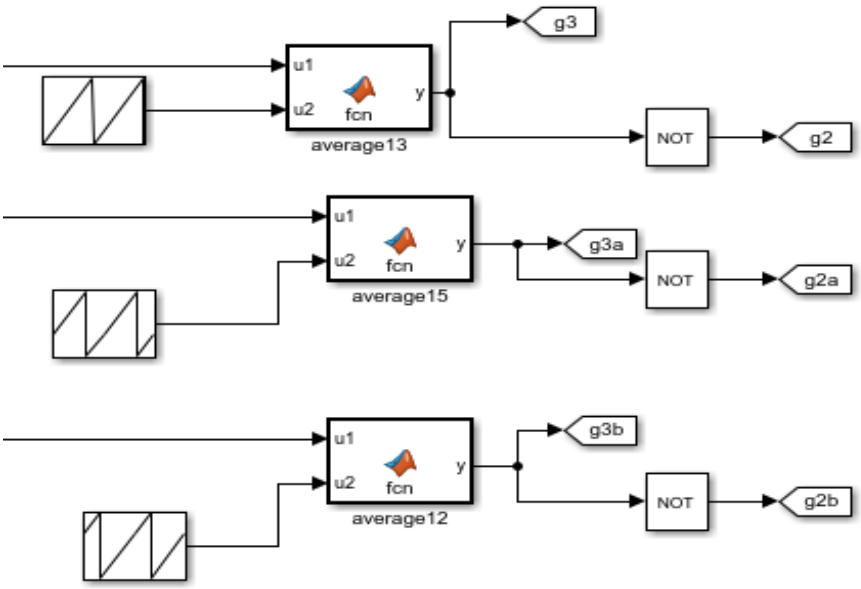


Figure 1.19 Phase-shifted based PWM

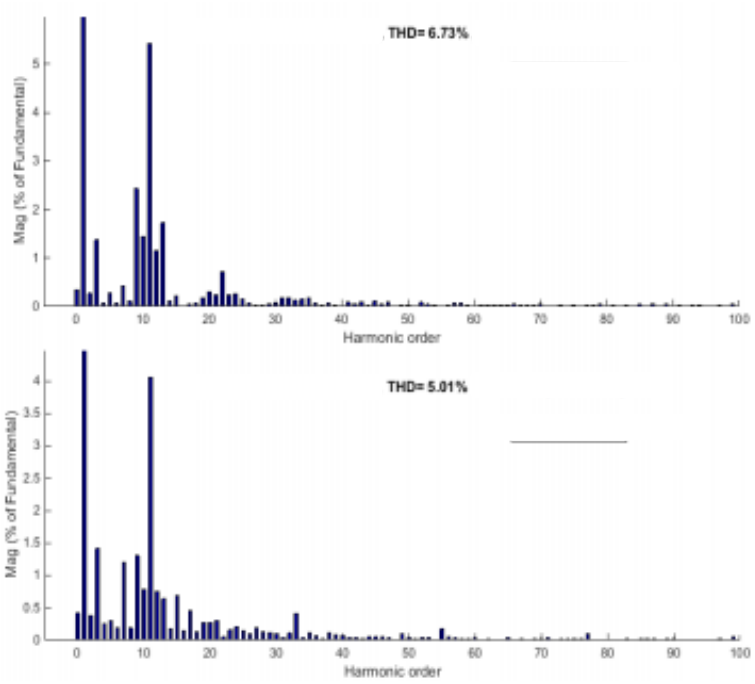


Figure 1.20 total harmonic disorder analysis

As shown in Figure 1.20, the THD of line voltage under level-shifted modulation is bigger than that under phase-shifted modulation (6.73% and 5.01% respectively).

Several studies highlighted the same result. According to [2], Level-shifted PWM has worse harmonic content in the line-to-line voltages when compared to the phase-shifted technique PWM because it does not synthesize the closest PWM level in these voltages. Table 1 shows their result.

Strategy	THD I_a (%)	THD V_{ab} (%)	Medium Error (V)
PDPWM	28.68	40.42	215.5
PODPWM	28.99	42.85	318.7
APODPWM	24.86	37.08	200.2
PSCPWM	6.96	21.58	23.26
SCRPWM	5.13	13.24	17.94

Table-1: THD of the line voltage and average error (for the first 2s) of the 5 carrier-based modulation techniques considering m= 11 and L = 8mH.

We can see that both the THD and the average errors of the PS techniques were much lower when compared to the LS techniques.

IIII. Discuss advantages and disadvantages of the CHB converter

Table2

Multilevel converters	Advantages	Disadvantages
Cascaded H-bridge (CHB) Inverter	1. Higher voltage output [3]. For the same input voltage, the voltage output with this inverter is twice compared with other multilevel converter. 2. High power applications [3]. CHB inverter doesn't require any clamping diodes or capacitors, which makes it suitable to use in high power applications. 3. Low manufacturing cost. This converter has modular structures composed of several identical units. The structure helps to reduce complexity and money when manufacturing.	1. Limited application. Because every H bridge requires a separate DC source, which is not realistic in industrial production.
Neutral Point Clamped (NPC) Inverter	1. No dynamic voltage sharing problem. Each switches in NPC inverter endures only half of the total dc voltage. 2. Static voltage equalization without additional components. This can be achieved when the leakage current of the top and bottom switches in a inverter leg is selected to be lower than that of the inner switches.	1. Uneven loss distribution in the devices. In a fundamental cycle, the conduction period of the inner devices is more than the outer devices. This causes unequal losses in devices in a leg. 2. The fluctuation of the dc bus midpoint voltage. 3. Additional clamping diodes. 4. Complicated PWM switching pattern design.
Flying capacitor (FLC) Inverter	1. Allowing the control of active and reactive power flow.	1. voltage control is difficult for all capacitors 2. poor switching efficiency High manufacturing costs. Capacitors are expansive.

Part-B

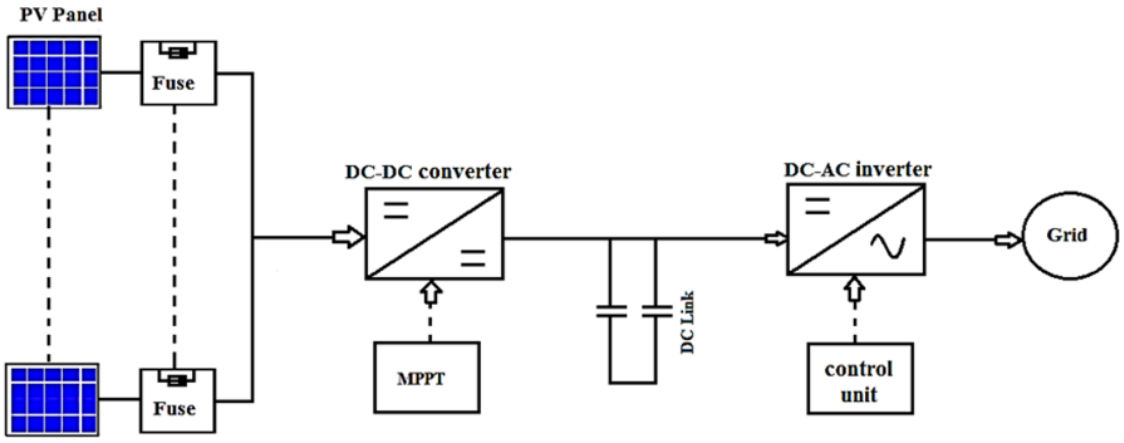


Figure 2: Grid-connected PV-array with Maximum Power-Point Tracking.

The classical structure of a 100kW grid-connected PV system is presented in Figure 2. The PV-array, produces DC power that depends on the environmental conditions and the operating point imposed by the load. A sample simulation model for this structure is provided for you as a reference. You need to write a report by accomplishing the following tasks:

Which MPPT algorithm is employed in the Simulink model?

Explain how this algorithm works.

Incremental conductance method is utilized in this Simulink model. This method is mainly based on a comparison of how the voltage and current change. It requires a perturbation of some control variable to determine the direction of tracking. The control variable could be the voltage, current or duty ratio.

$$\frac{dP}{dV} = \frac{d(IV)}{dV} = I + V.\frac{dI}{dV} = I + V\frac{\Delta I}{\Delta V}$$

When $\frac{dP}{dV} = 0$, The output power is maximum

$$\frac{dP}{dV} = I + V\frac{\Delta I}{\Delta V} = 0$$

$$\Rightarrow \frac{\Delta I}{\Delta V} = -\frac{I}{V}$$

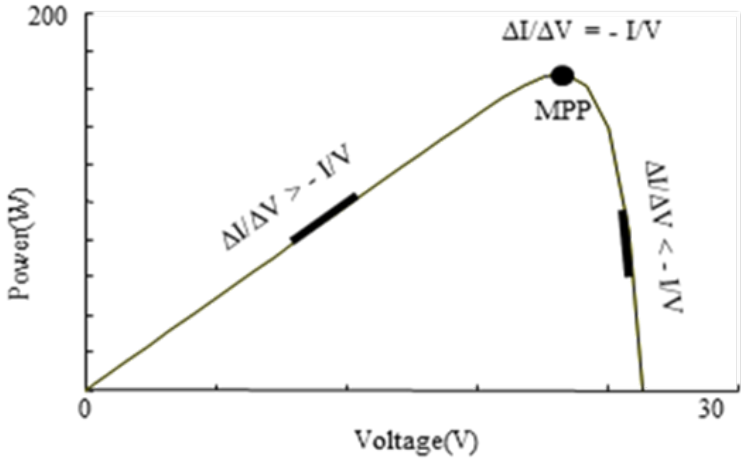


Figure 2.1 P-V Characteristics

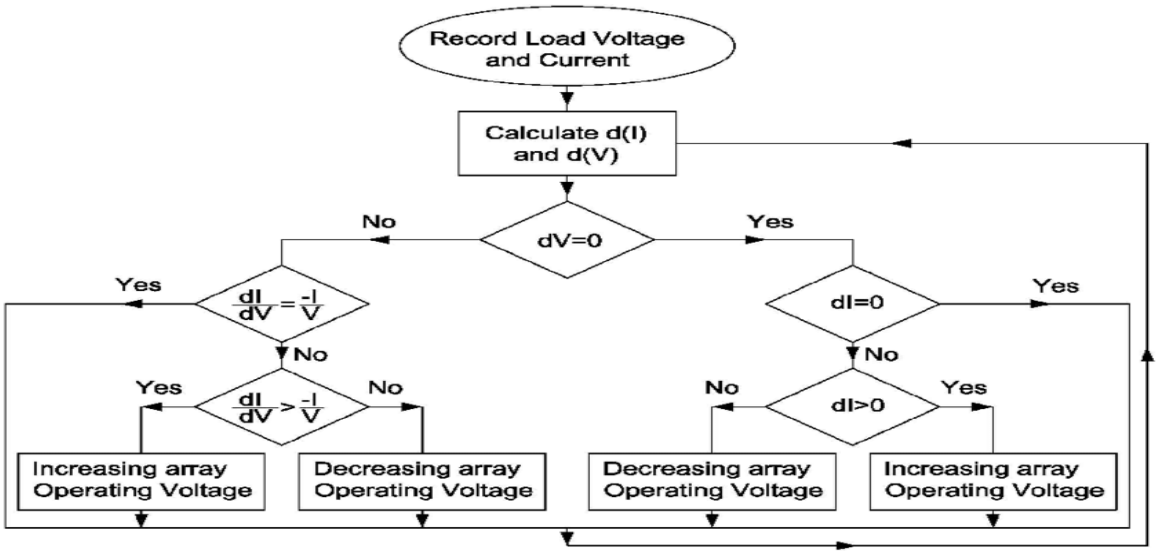


Figure 2.2 Incremental Inductance Algorithm

As shown in Figure 2.1 and 2.2

When $\frac{\Delta I}{\Delta V} > -\frac{I}{V}$, Power is in the left of MPP,

Then the algorithm will increase the control variable and duty cycle.

When $\frac{\Delta I}{\Delta V} < -\frac{I}{V}$, Power is in the right of MPP,

Then the algorithm will decrease the control variable and duty cycle.

When $\frac{\Delta I}{\Delta V} = -\frac{I}{V}$, Power is at MPP,

Then the algorithm will maintain the control variable and duty cycle.

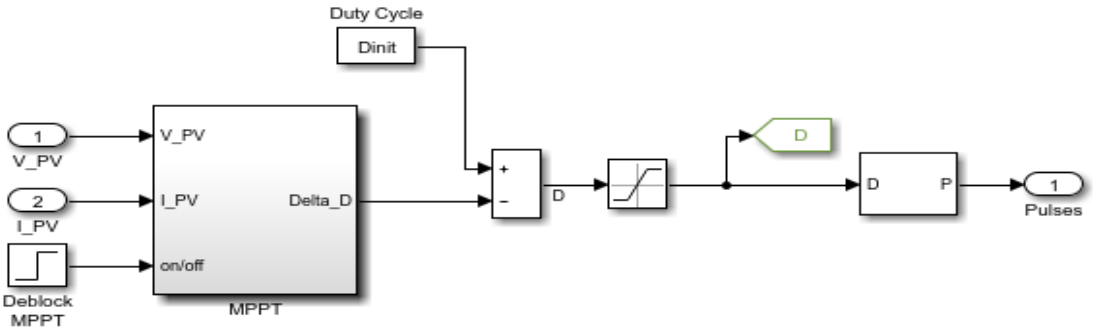


Figure 2.3 Pulse generation

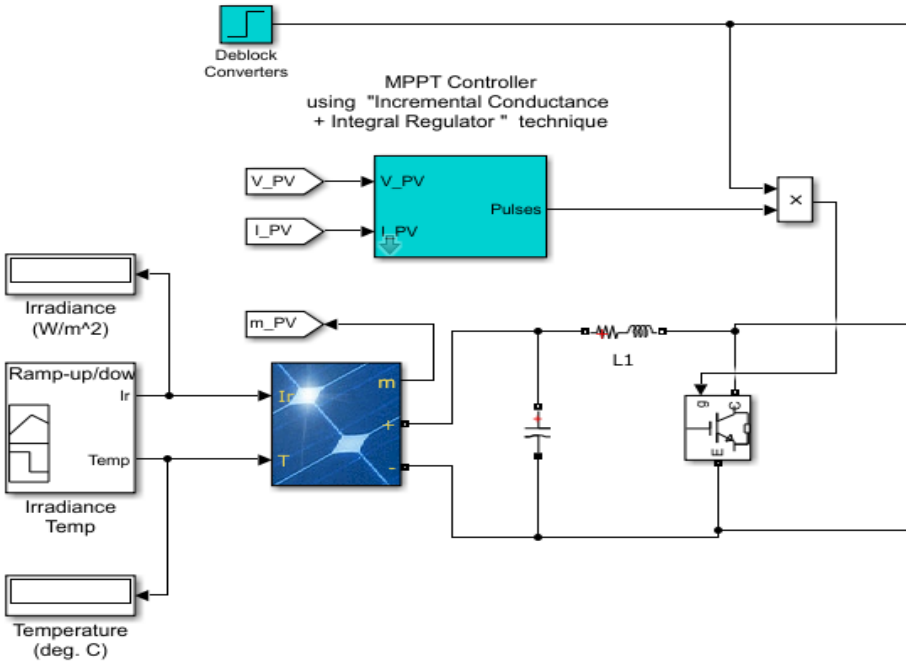


Figure 2.4

II. Explain the control architecture utilized in the model. You need to provide detailed explanations of how each stage works with relevant simulation results.

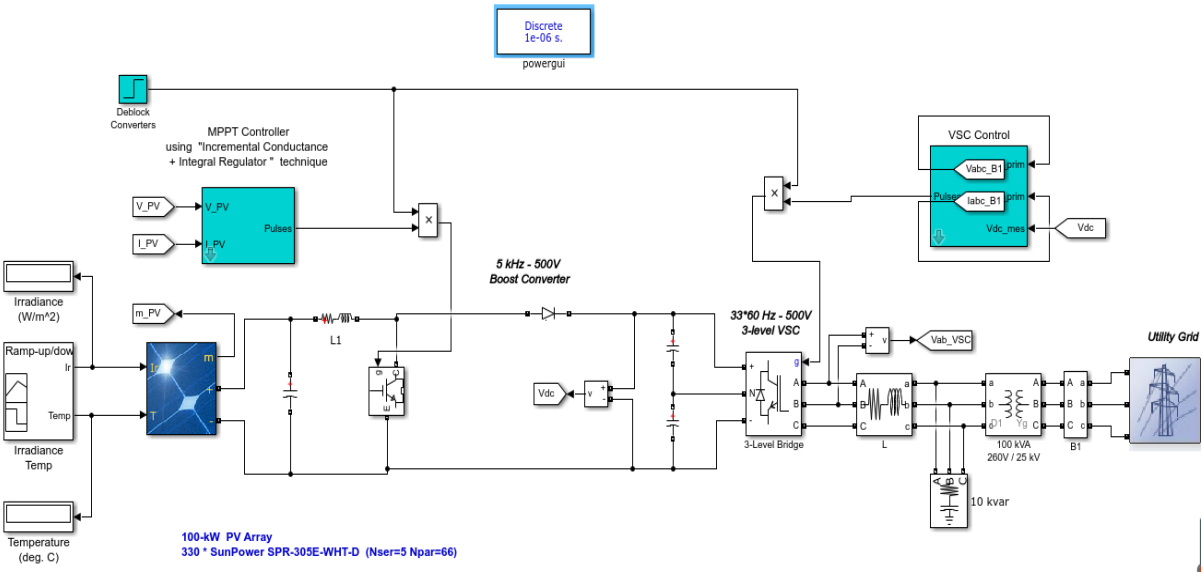


Figure 2.5 100KW Grid connected PV Array

In this model, a 100-kW PV array is connected to a 25-kV grid via a DC-DC boost converter and a three-phase three-level Voltage Source Converter (VSC). Maximum Power Point Tracking ('Incremental Conductance + Integral Regulator' technique.) is implemented in the boost converter.

Stage one - Power generation

Stage one mainly involves PV array and Ramp-up and down block. PV array is built of 66 strings of PV modules connected in parallel. Each string consists of 5 modules connected in series. PV array will absorb the energy from sunlight and deliver a maximum of 100 kW at 1000 W/m^2 sun irradiance. The output power mainly depends on the environment (radiance and cell temperature) which are controlled by the ramp-up and down block.

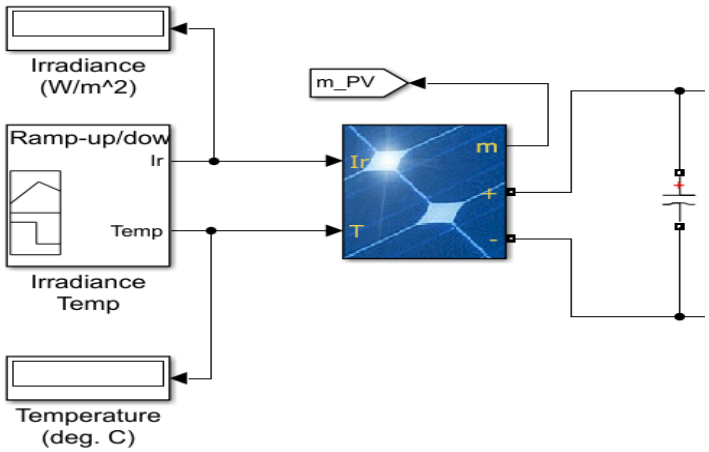


Figure 2.6 Power generation

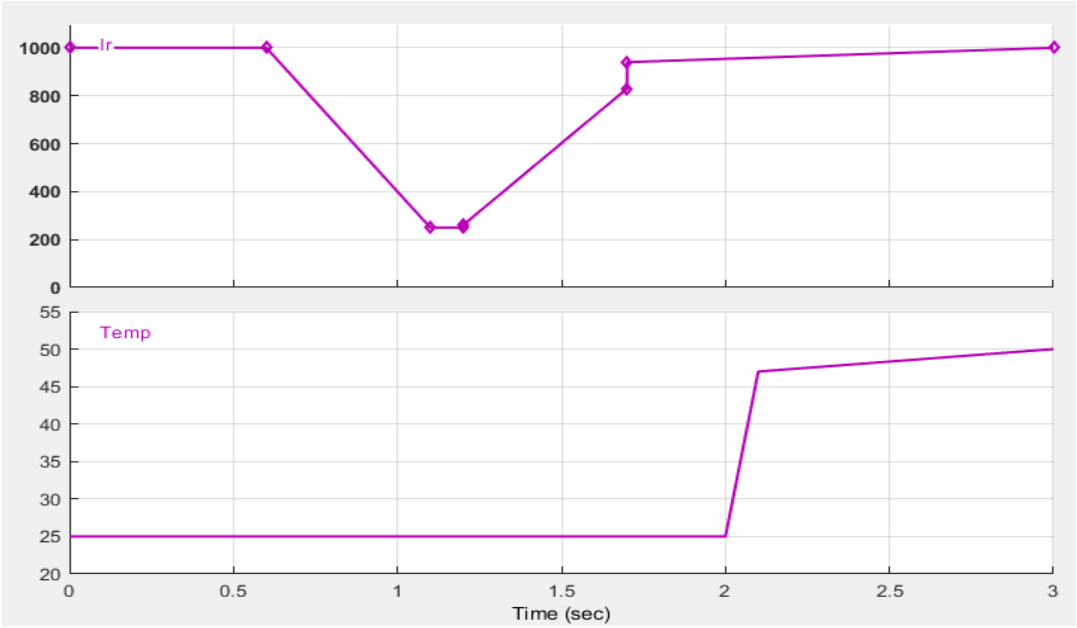


Figure 2.7 Ramp up and down block

Stage two – Boost voltage and MPPT control

A 5-kHz DC-DC boost converter increasing voltage from PV natural voltage (273 V DC at maximum power) to 500 V DC. Switching duty cycle is optimized by a MPPT controller that uses the 'Incremental Conductance + Integral Regulator' technique. This MPPT system automatically varies the duty cycle in order to generate the required voltage to extract maximum power.

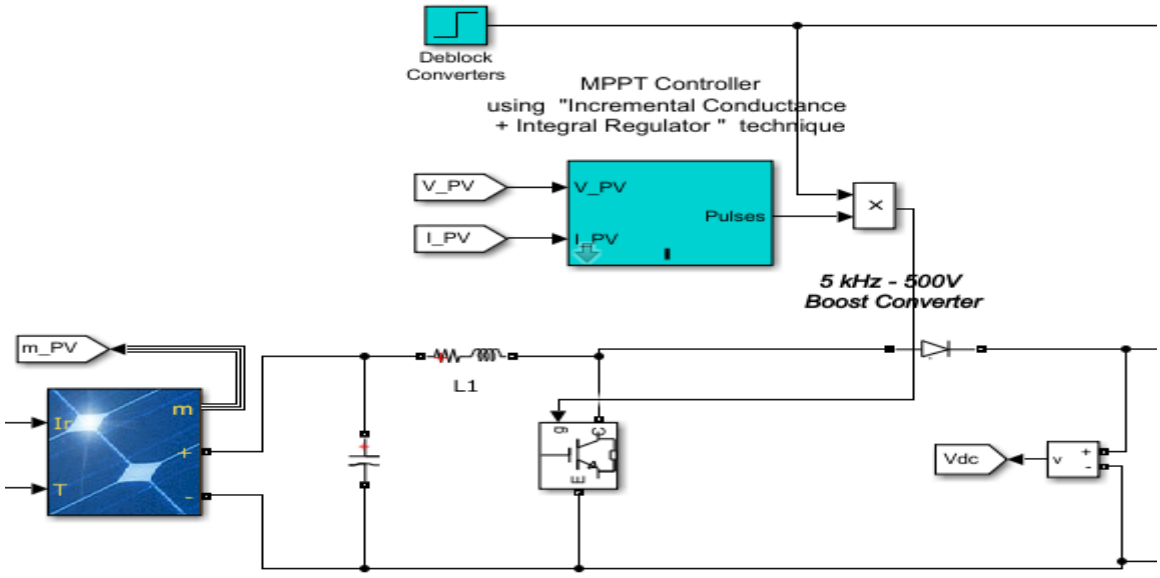


Figure 2.8 Boost converter and MPPT

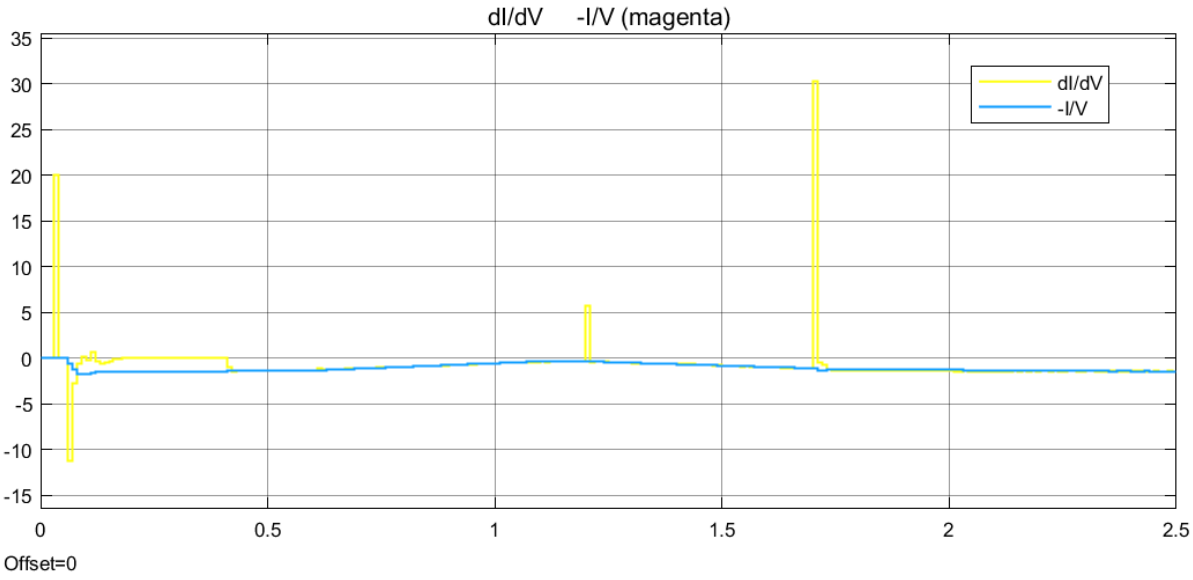


Figure 2.9 Boost converter and PWM

As shown in Figure 2.9, the algorithm constantly compares dI/dV and (– V/I) and adjusts the control value to maintain at MPP. After around 1.7s, the two values are equal and PV generates maximum power.

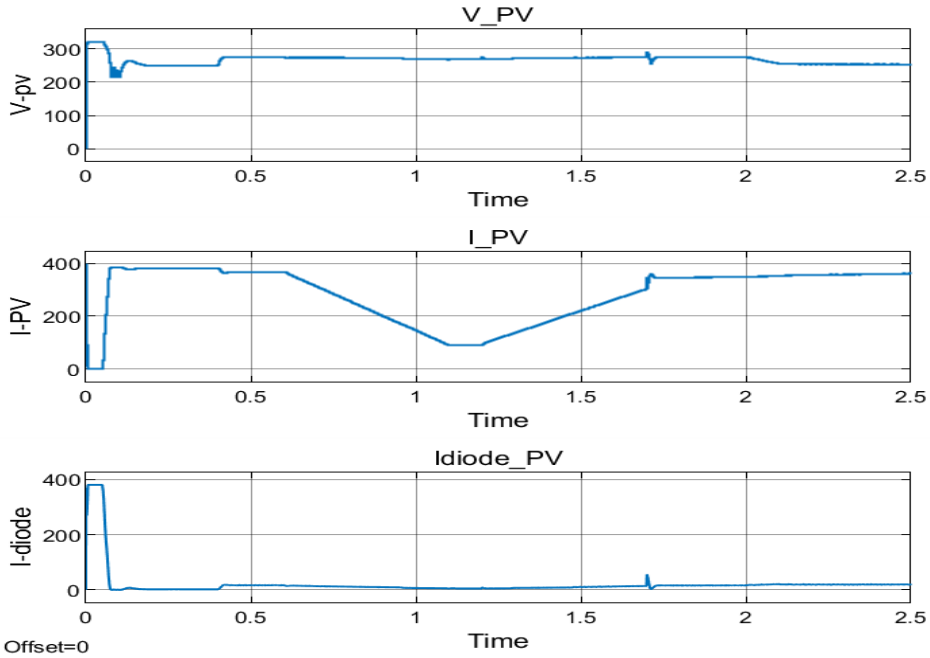


Figure 2.10 Output voltage and current for PV

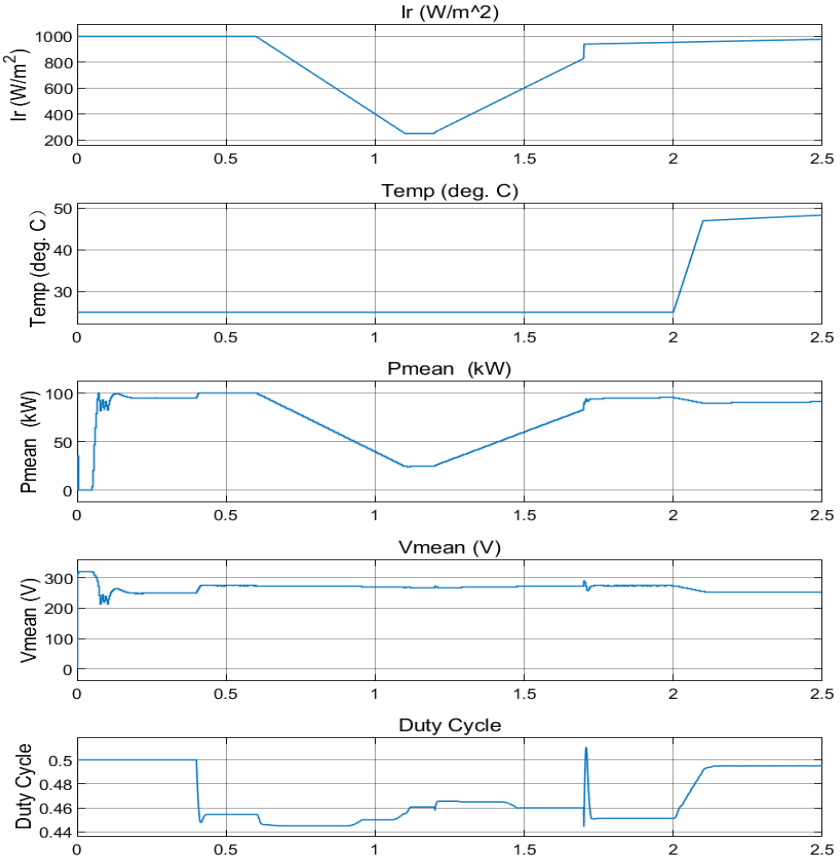


Figure 2.11 Results

As shown in Figures above, we can clearly see that the change in irradiance and temperature can affect the output power. But MPPT can change duty cycle to generate maximum power.

Stage three -Voltage conversion（DC-AC）and Grid connection

A VSC converts the 500 V DC link voltage to 260 V AC and keeps unity power factor. The VSC control system uses two control loops: an external control loop which regulates DC link voltage to +/- 250 V and an internal control loop which regulates Id and Iq grid currents (active and reactive current components). Id current reference is the output of the DC voltage external controller. Iq current reference is set to zero in order to maintain unity power factor. Vd and Vq voltage outputs of the current controller are converted to three modulating signals Uabc-ref used by the PWM Generator. A 10-kvar capacitor bank will be used to filter harmonics produced by VSC. After that, It will connected with a 100-kVA 260V/25kV three-phase coupling transformer and deliver power to the utility grid.

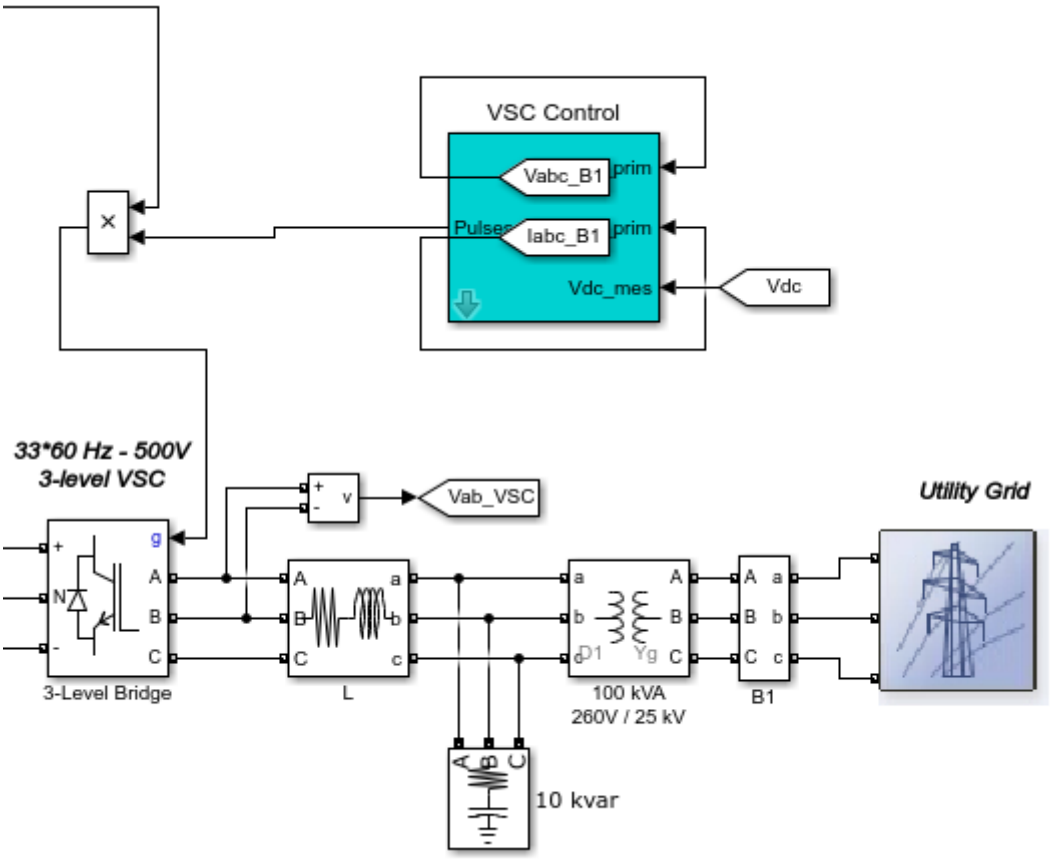


Figure 2.12 Grid Connection

III.How the irradiance profile impacts the maximum power? Vary the irradiance profile to 30% in 5 steps and show how the system adapts to these changes.

(1) The irradiance profile impacts the maximum power

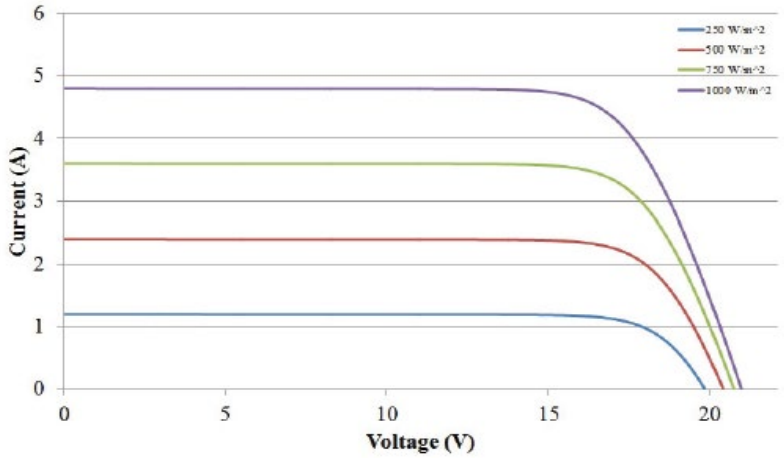


Figure 2. 13 Current-voltage characteristic curves under various irradiance

As we can see in Figure 2.11.When irradiance drops, short-circuit current drops in direct proportion. Cutting insolation in half, for example, drops short circuit current by half. Decreasing insolation also reduces open circuit voltage [4].The decline in voltage and current will definitely lead to the drop of output power. The PV is unable to work at the maximum power point.

(2) Vary the irradiance profile

Set the initial irradiance is 1000 w/m^2 and then decrease irradiance by 140 w/m^2 every 0.2s until it dropped to 300 w/m^2. Keep temperature at 25 degree during the simulation.

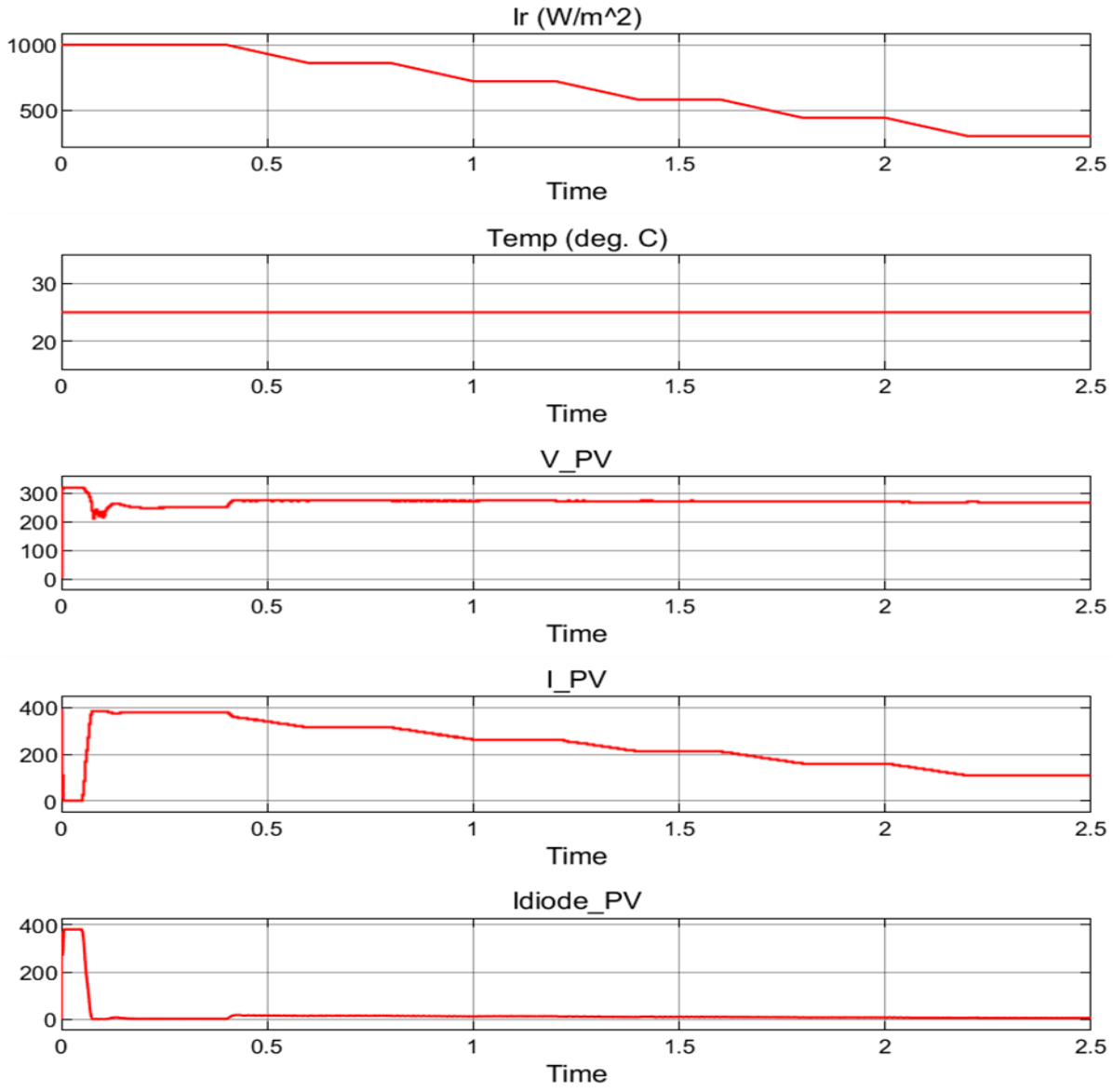


Figure 2. 15 Output voltage and current of PV

From t=0 sec to t= 0.05 sec, pulses to Boost and VSC converters are blocked. PV voltage corresponds to open-circuit voltage (Nser*Voc=5*64.2=321 V, Ipv=0). At t=0.05 sec, Boost and VSC converters are de-blocked. DC link voltage is regulated at Vdc=500V.With the drop in irradiance, the output current will gradually decline, while the output voltage stay stable. It proves that the irradiance will affect output current.

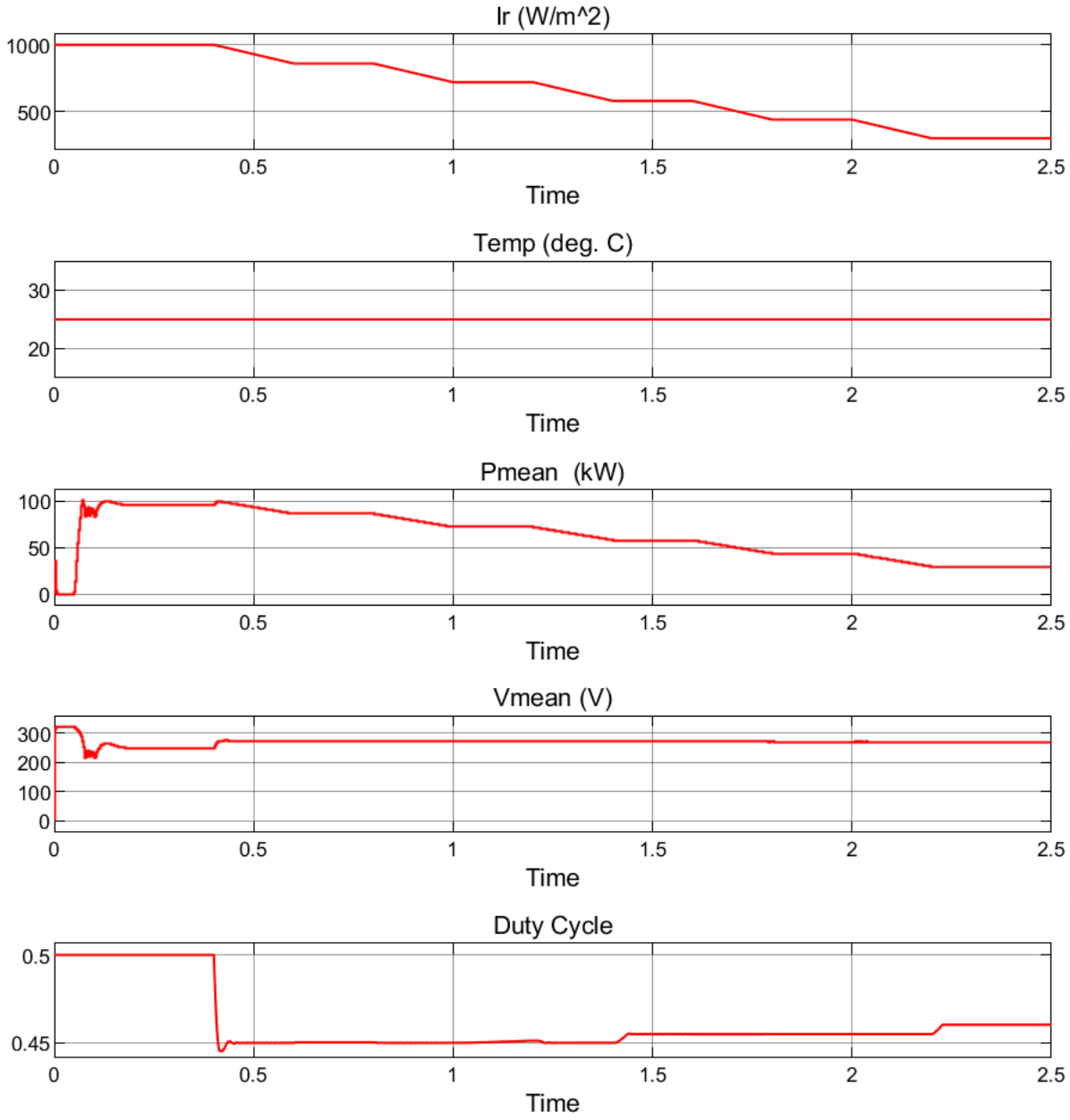


Figure 2. 15 Output voltage and real power of PV when irradiance drops

As shown in this figure, the decline in irradiance results in the decline of output power. Although MPPT algorithm constantly changes duty cycle to ensure that the output power maintain stable, we can see that the output power cannot maintain at 100kw.As Irradiance declines, the duty cycle sometimes drops (at 0.4s, 1.2s) and increases (1.4s and 2.4s).The relationship between duty cycle and irradiance is complex.

IIV. What is the impact of temperature on the PV generation? Vary the temperature profile from 25 – 40 degrees C in three steps and show how the system performs in these changing conditions.

(1) the impact of temperature on the PV generation

As cell temperature increases, the open-circuit voltage decreases substantially while the short-circuit current increases only slightly. Therefore, photovoltaic perform better on cold, clear days than hot ones [4]. For crystalline silicon cells, VOC drops by about 0.37% for each degree Celsius increase in temperature and ISC increases by approximately 0.05%. The net result when cells heat up is the MPP slides slightly upward and toward the left with a decrease in maximum power available of about 0.5%. [4].

(2) Vary the temperature profile

Set initial temperature at 25 degree and then gradually increase temperature by 5 degree until it reaches 40 degree.

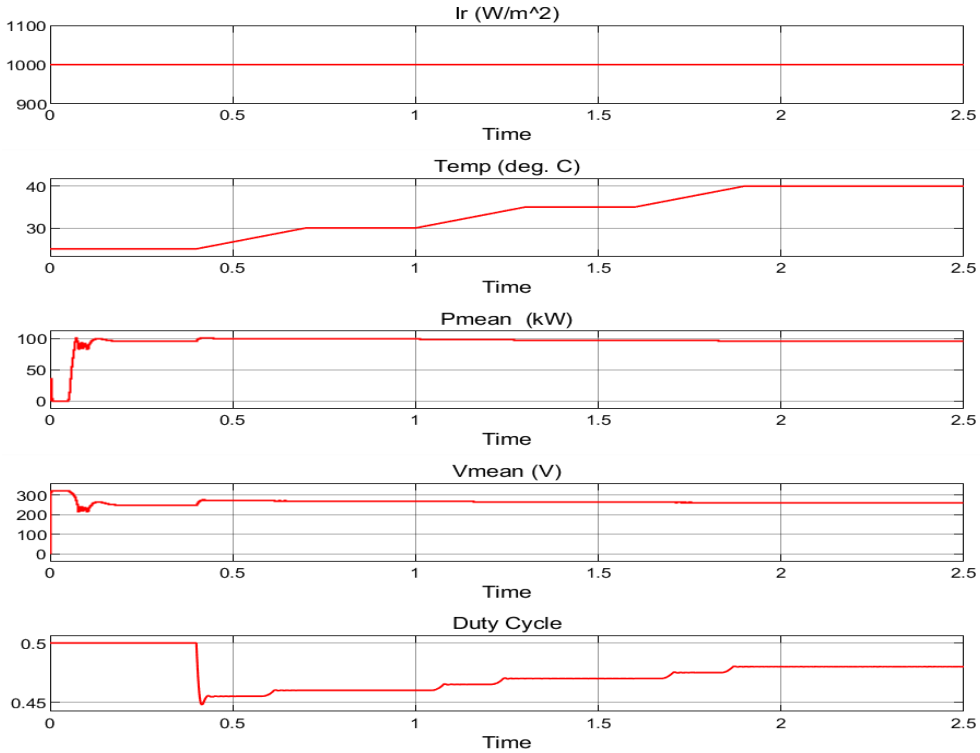


Figure 2. 15 Output voltage and real power of PV when temperature increases

As shown in this figure, the increase in temperature results in change of output power. Although MPPT algorithm constantly increase duty cycle to ensure that the output power maintain stable, we can see that the output power maintain at maximum power point. As temperature increase at 0.4, 1.0s, 1.6s, the duty cycle increases too.

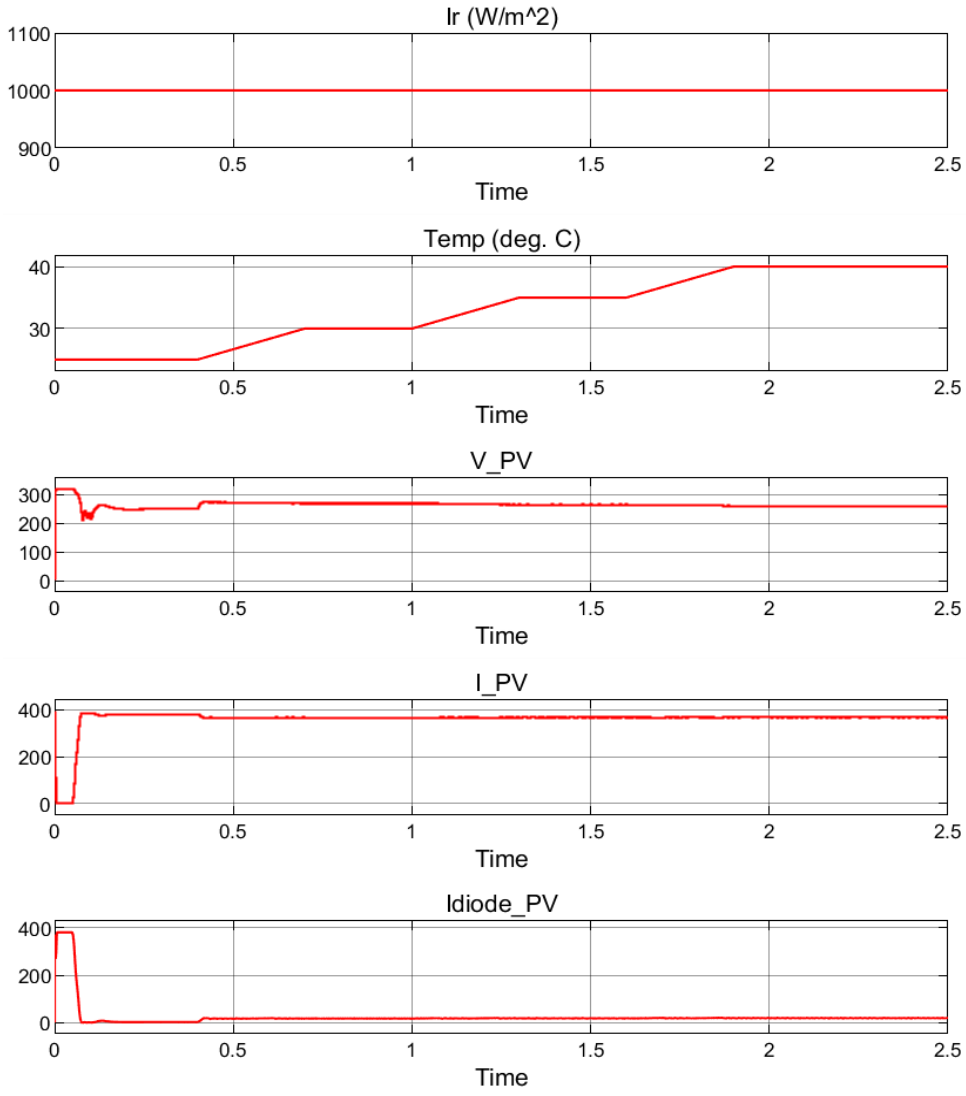


Figure 2. 16 Output voltage and current of PV

With the drop in temperature, the output voltage will slightly decline, while the output current stay stable. It proves that the temperature will affect output current.

V. Discuss the effect of partial shading for the grid-connected PV structure shown above. How to mitigate the shading problem?

(1) Partial shading effect

The output of a PV module can be reduced dramatically when even a small portion of it is shaded. We will discuss the relationship between the number of shaded cells and the output power.

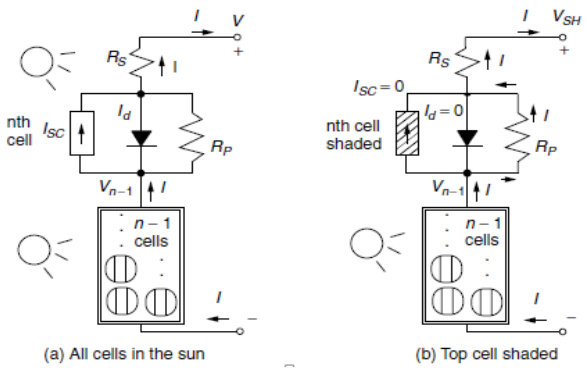


Figure 2.17 A module with n cells in which the top cell is in the sun (a) or in the shade (b)

Condition1. One cell in the module has been shaded

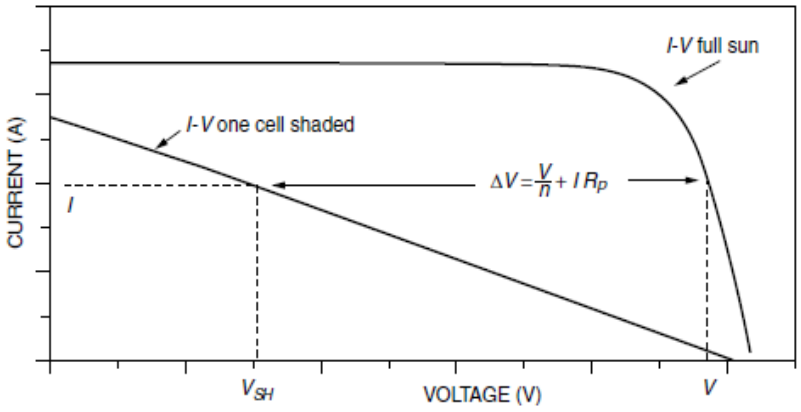


Figure 2.18 Effect of shading one cell in an n-cell module.

As shown in Figure above, at any given current, the I –V curve for the module with one shaded cell drops by ΔV.

Condition2. Several cells in the module has been shaded

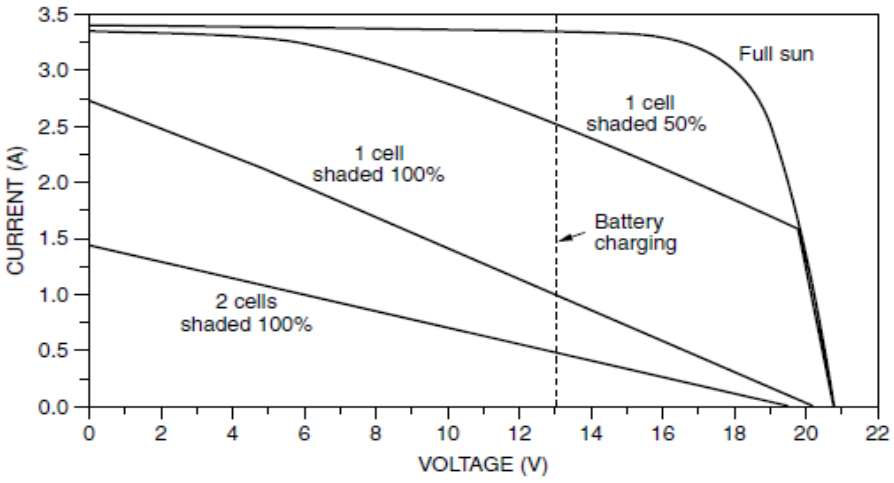
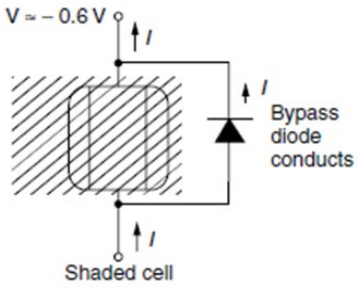
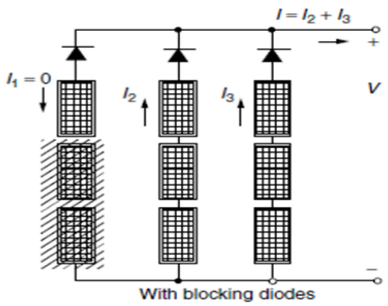
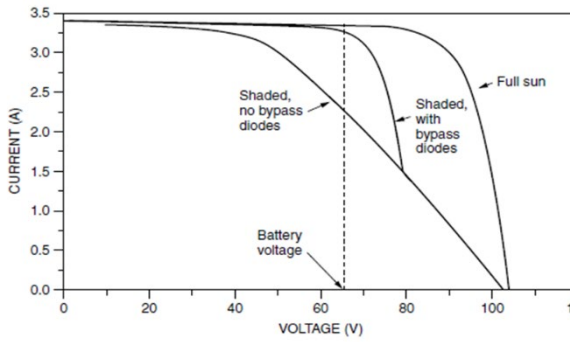


Figure 2.19 Effects of shading on the I –V curves for a PV module.

Figure 26 shows curves for a module under full-sun conditions and with one cell 50% shaded, one cell completely shaded, and two cells completely shaded. The impact on charging current is obviously severe [5] The dashed line at 13 V shows a typical operating voltage for a module charging a 12-V battery. The reduction in charging current for even modest amounts of shading is severe. With just one cell shaded out of 36 in the module, the power delivered to the battery is decreased by about two-thirds [5].

(2)Mitigation methd

<table>
<tr><td>Method for shade mitigation</td><td>Bypass Diode</td><td>Block Diode</td></tr>
<tr><td>Circuit</td><td> 
</td><td> 
</td></tr>
<tr><td>Working principle</td><td>When a solar cell is in the sun, there is a voltage rise across the cell so the bypass diode is cut off and no current flows through it.it is as if the diode is not even there. When the solar cell is shaded, however, the drop that would occur if the cell conducted any current would turn on the bypass diode, diverting the current flow through that diode.</td><td>When strings of modules are wired in parallel, a similar problem may arise when one of the strings is not performing well. A malfunctioning or shaded string can withdraw current from the rest of the array. By placing blocking diodes (also called isolation diodes) at the top of each string, the reverse current drawn by a shaded string can be prevented [2].</td></tr>
<tr><td>Working performance</td><td> 

As can be seen, when just two cells in one module are shaded, the current drops by one-third to about 2.2 A. With a bypass diode across the shaded module, however, the I –V curve is improved considerably as shown in the figure[5].</td><td></td></tr>
</table>

VI. Discuss the leakage current issue and why it occurs. How does leakage current appear in the described system? Discuss how to modify the inverter in order to show the leakage current. Discuss the leakage currents in 2- and 3-level inverters.

(1) leakage current

The parasitic capacitance between the PV array and the ground causes leakage current to flow [6]. A varying common-mode voltage can excite this resonant circuit and generate a common-mode current. The value of parasitic capacitance depends on many factors; some of these are enumerated below: PV panel and frame structure, surface of cells, distance between cells, module frame, weather conditions, humidity and dust covering the PV panel.

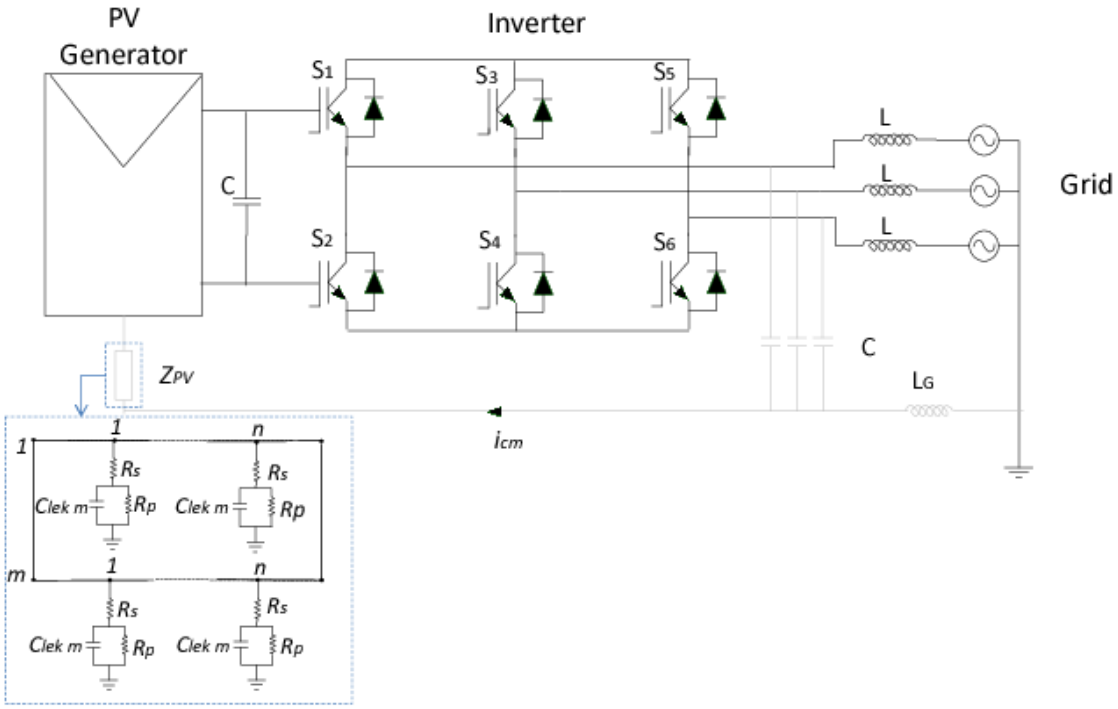


Figure2.20 Equivalent common mode resonant circuit of three phase inverter

As shown in figure above, a common-mode resonant circuit consists of the stray capacitor between the PV modules and the ground, the dc and ac filter elements, and the grid impedance (Fig 2.20). Icm, which is the leakage current ,will flow from Grid to the PV array.

Common mode current due to modulation in power converters introduces numerous problems in electrical systems. In motor drives and electrical networks, common-mode current even has the potential to cause physical damage or unwanted tripping of ground fault relays. In aircraft, for example, inductively coupled currents may interfere with other systems such as sensitive avionics equipment. In industrial applications, such current can cause malfunctions of computers and control equipment [7].

(2) The cause of leakage current

$$\mathrm{Icm} = \mathrm{C}\frac{dV}{dt}$$

According to the formula, when switch states changes so fast for example from (00) to (11), then output voltage will change dramatically, Also the switching time is very small. As a result the leakage current appears and flows from the inverter to PV.

(3)Two and three leakage circuit

Tow-level leakage circuit

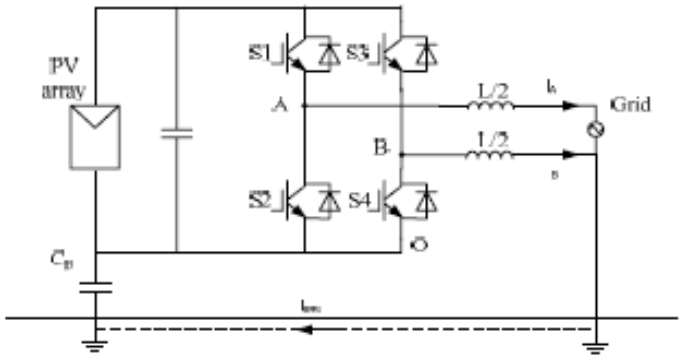


Figure 2.21Tow-level leakage circuit model

Three level leakage circuit:

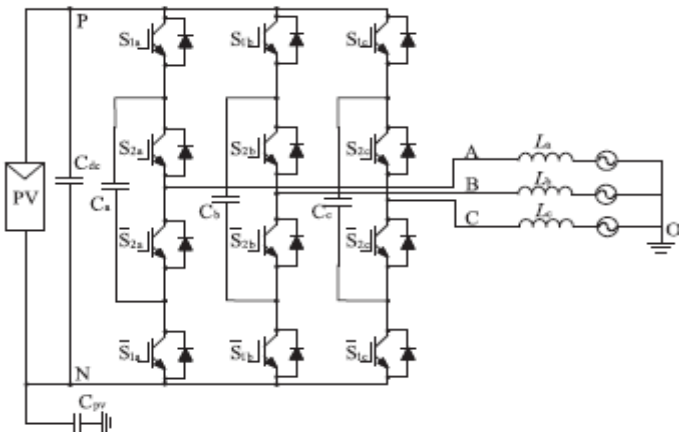


Figure 2.22 Three-level leakage circuit model

Reference

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[2]Abduallah, A.A. et al., 2018. Space vector pulse width modulation control techniques for a five-phase quasi-impedance source inverter. Iet Electric Power Applications, 12(3), pp.379–387.

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