



Fundamentals of Logic Circuit Design

Part IV: Petri Net



HUMAN CAPITAL
HUMAN – BEST INVESTMENT!

EUROPEAN UNION
EUROPEAN
SOCIAL FUND



Project is co-financed by European Union within European Social Fund

A tool for describing concurrent system operation

$$B = (P, T, I, O)$$

- B - Petri net (a bipartite graph)
- P - set of places (nodes of the first kind)
- T - set of transitions (nodes of the second kind)
- I - number of arcs connecting a place to a transition (transition input function)
- O - number of arcs connecting a transition to a place (transition output function)
- N - set of natural numbers including 0

Properties

- No two places are connected by an arc
- No two transitions are connected by an arc
- Only some places are connected to a certain transition
- Only some transitions are connected to a certain place

Marked Petri Net

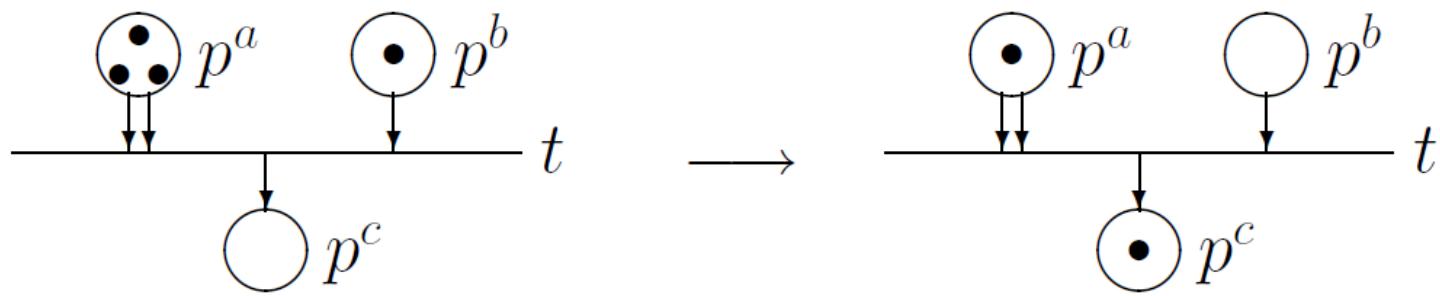
$$M = (B; \mu^0)$$

B - Petri net

μ - marking ($\mu: P \rightarrow N$)

μ^0 - initial marking (indicates how many tokens are there at each place initially)

Functioning of a marked Petri Net



$$P = \{p^a, p^b, p^c\} \quad T = \{t\}$$

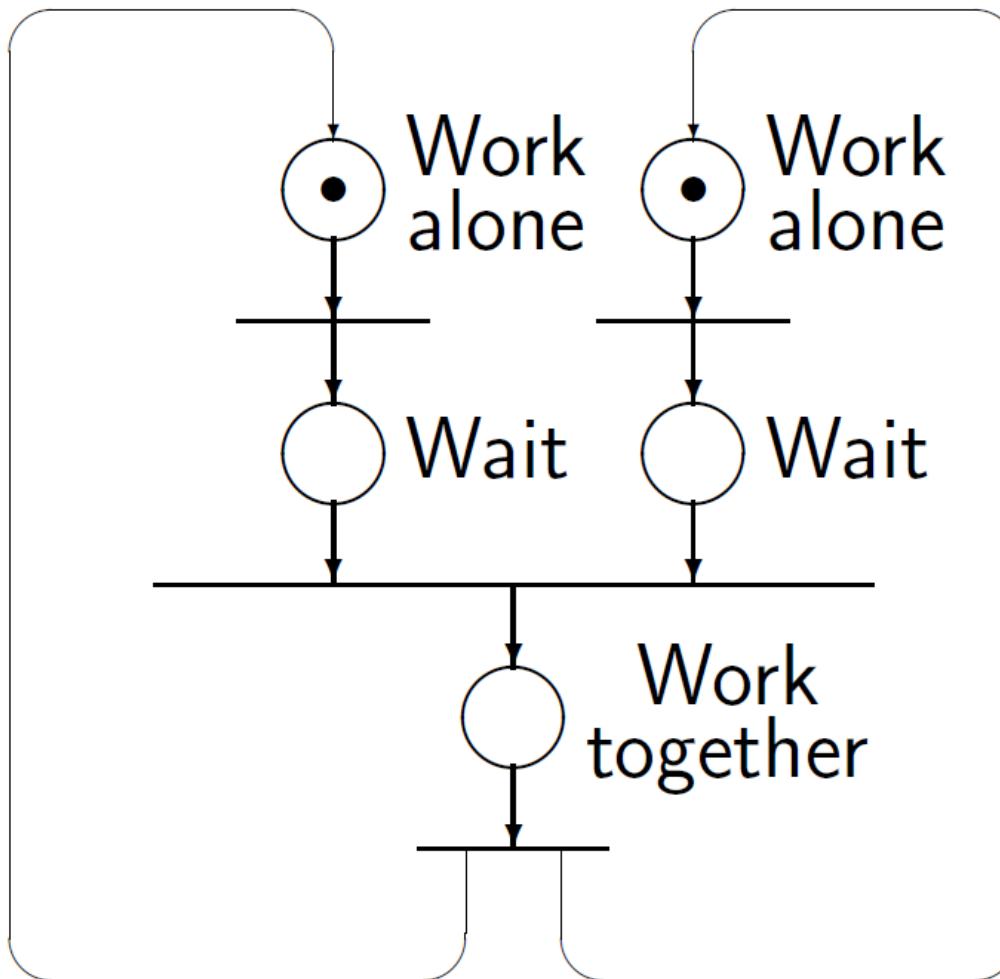
$$I(p^a, t) = 2 \quad I(p^b, t) = 1 \quad I(p^c, t) = 0$$

$$O(t, p^a) = 0 \quad O(t, p^b) = 0 \quad O(t, p^c) = 1$$

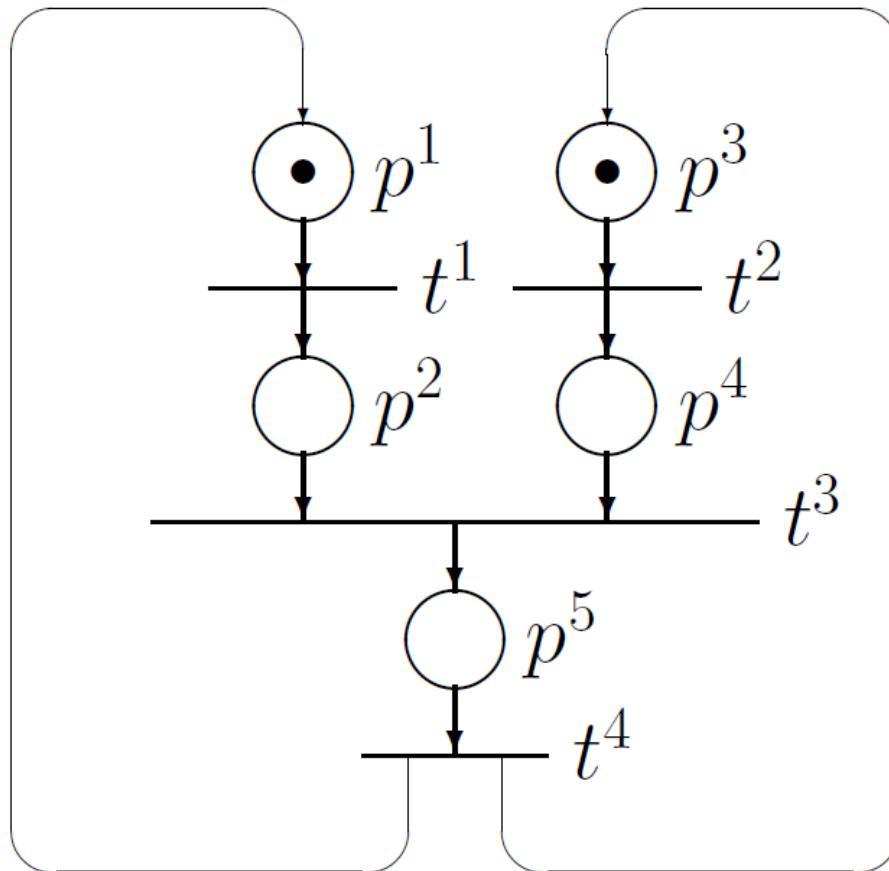
$$\mu^1(p^a) = 3, \quad \mu^1(p^b) = 1, \quad \mu^1(p^c) = 0$$

$$\mu^2(p^a) = 1, \quad \mu^2(p^b) = 0, \quad \mu^2(p^c) = 1$$

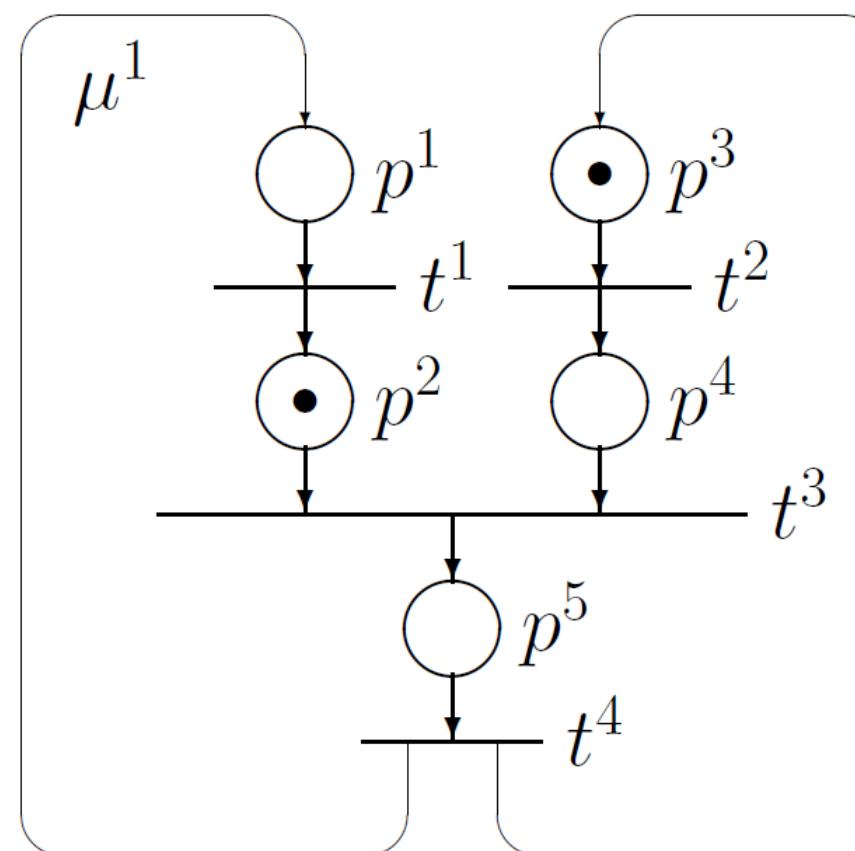
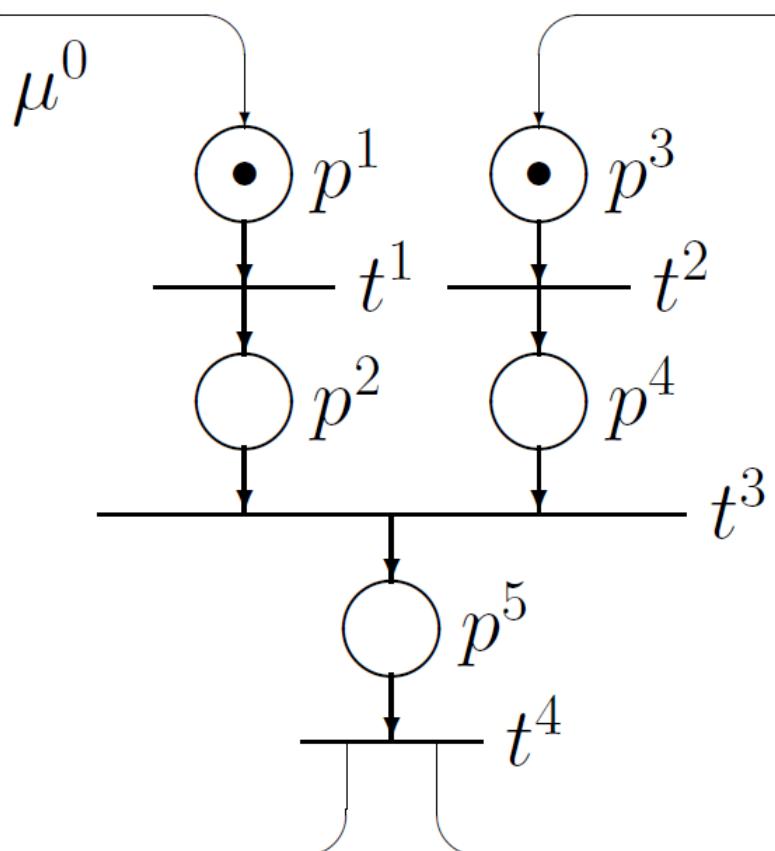
Example: Synchronization of two workers.

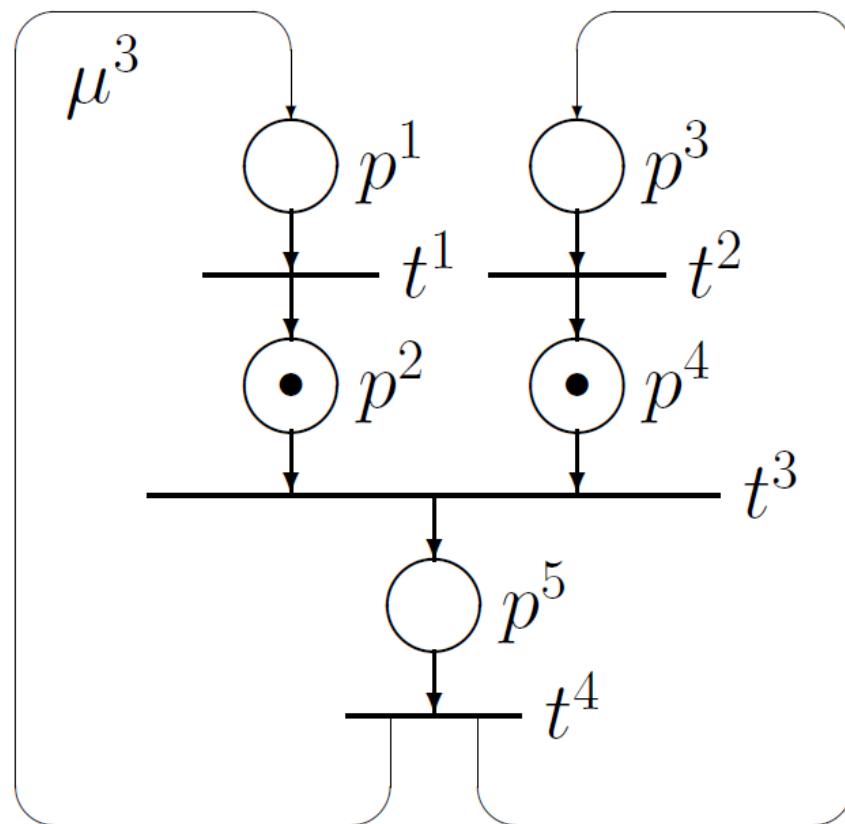
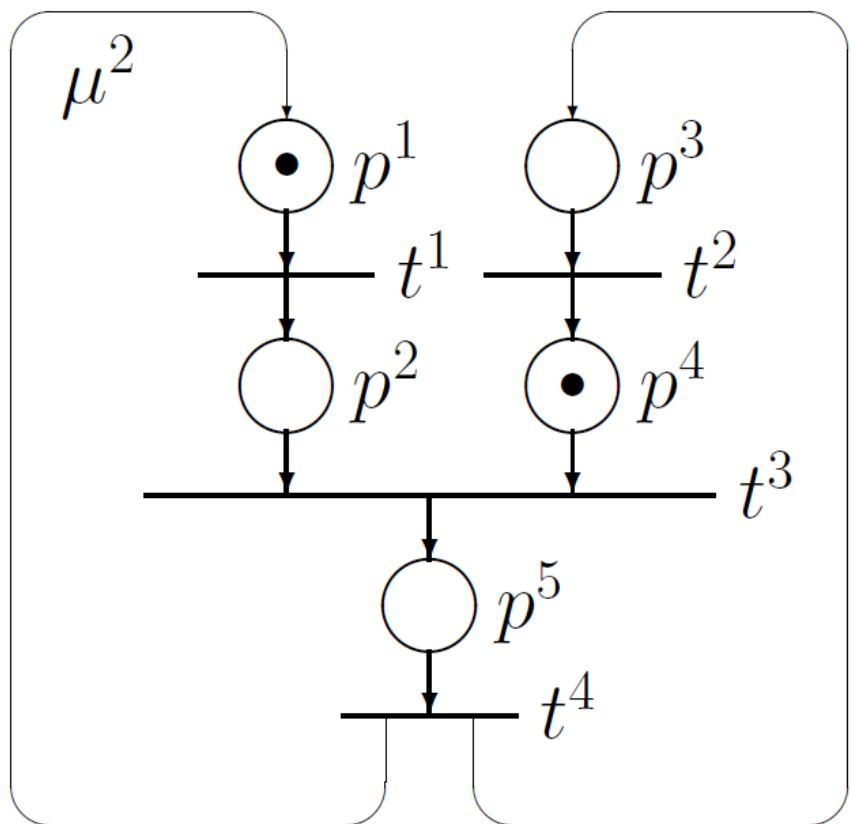


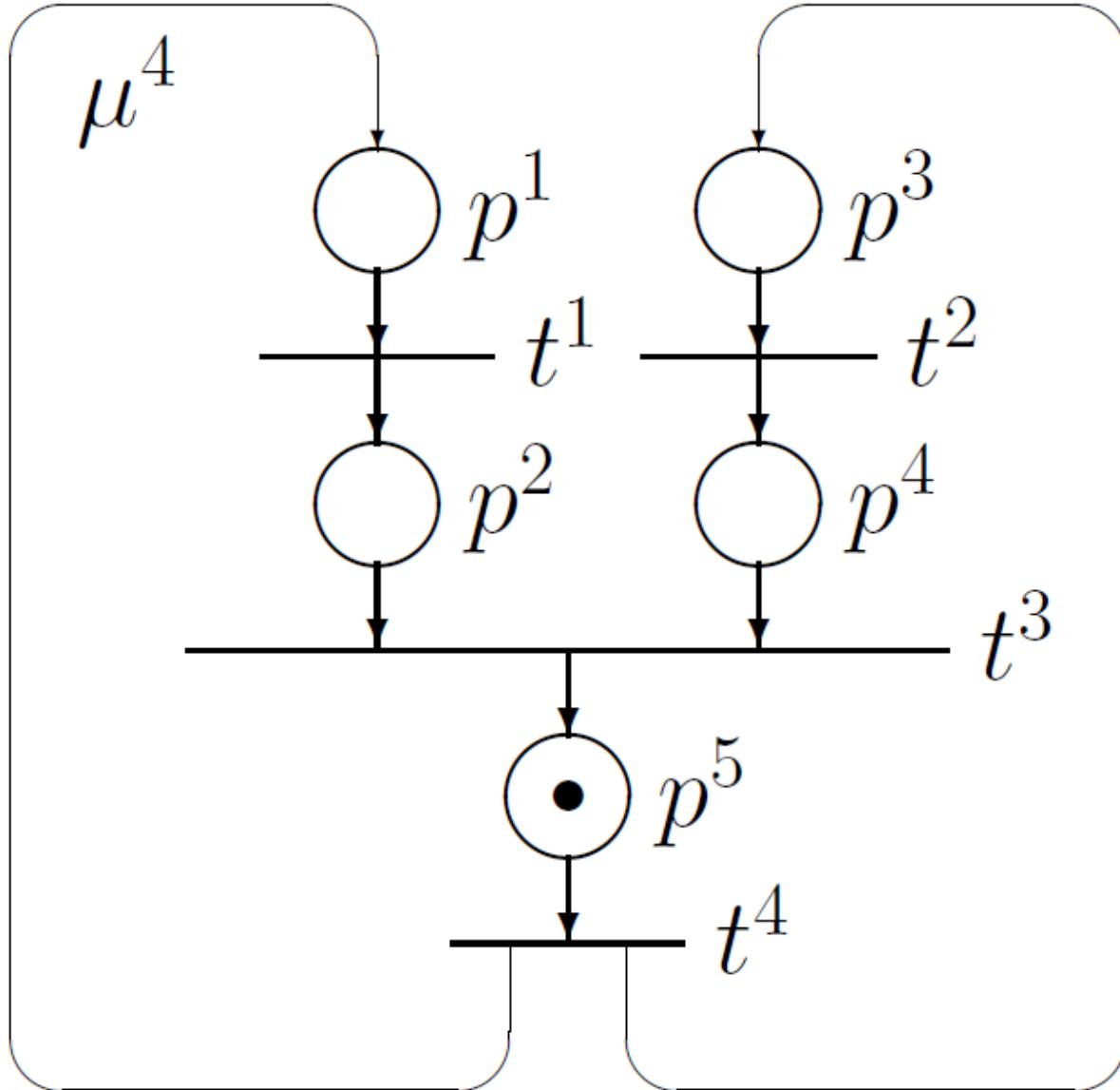
Initial marking of the net



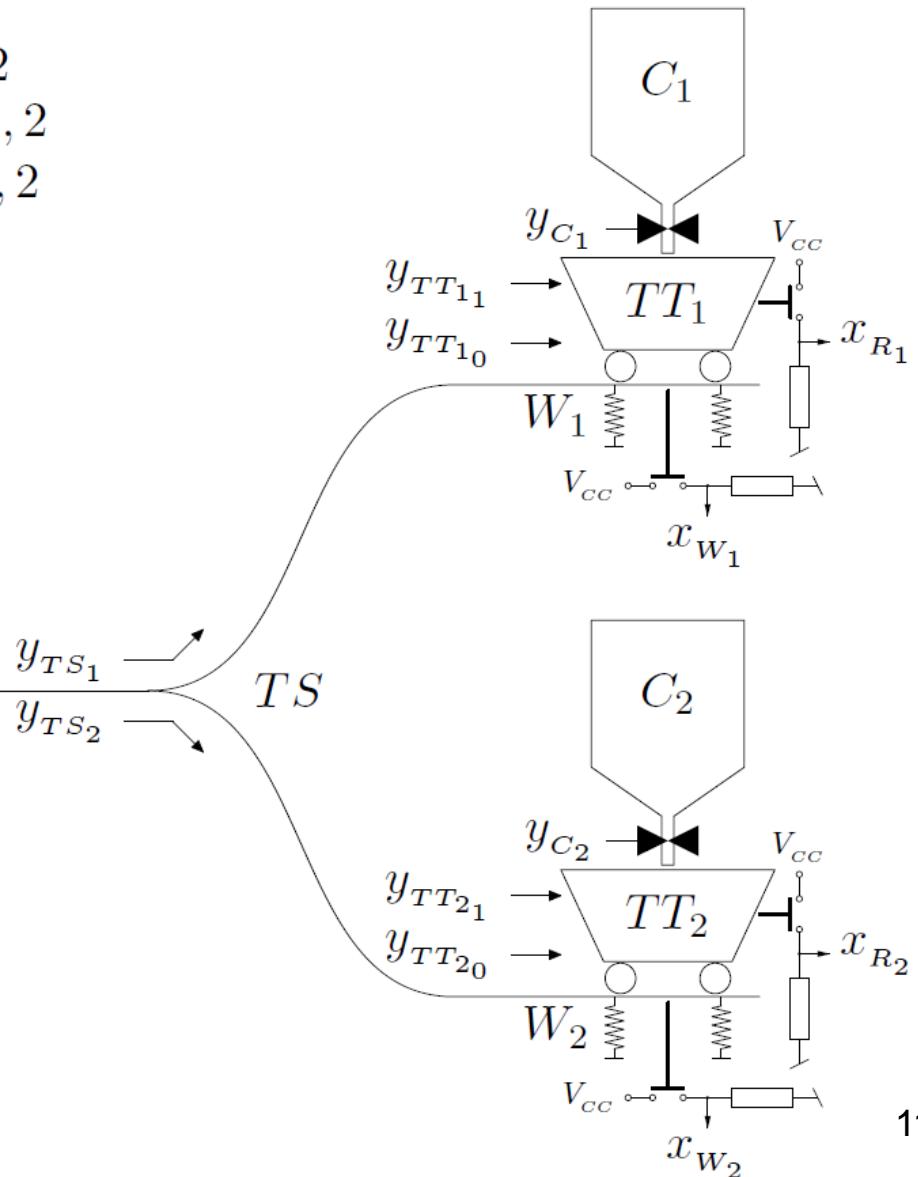
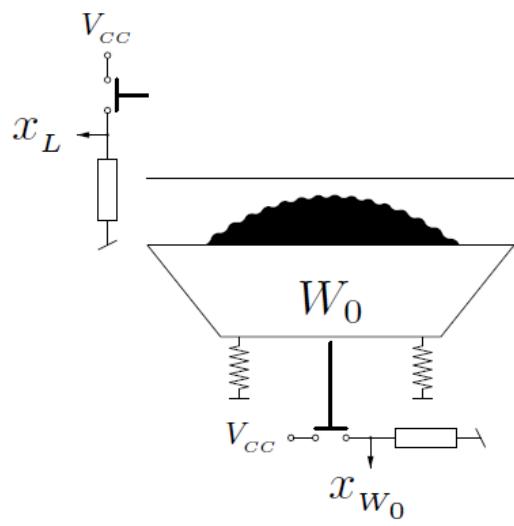
Possible markings of the synchronizing Petri net

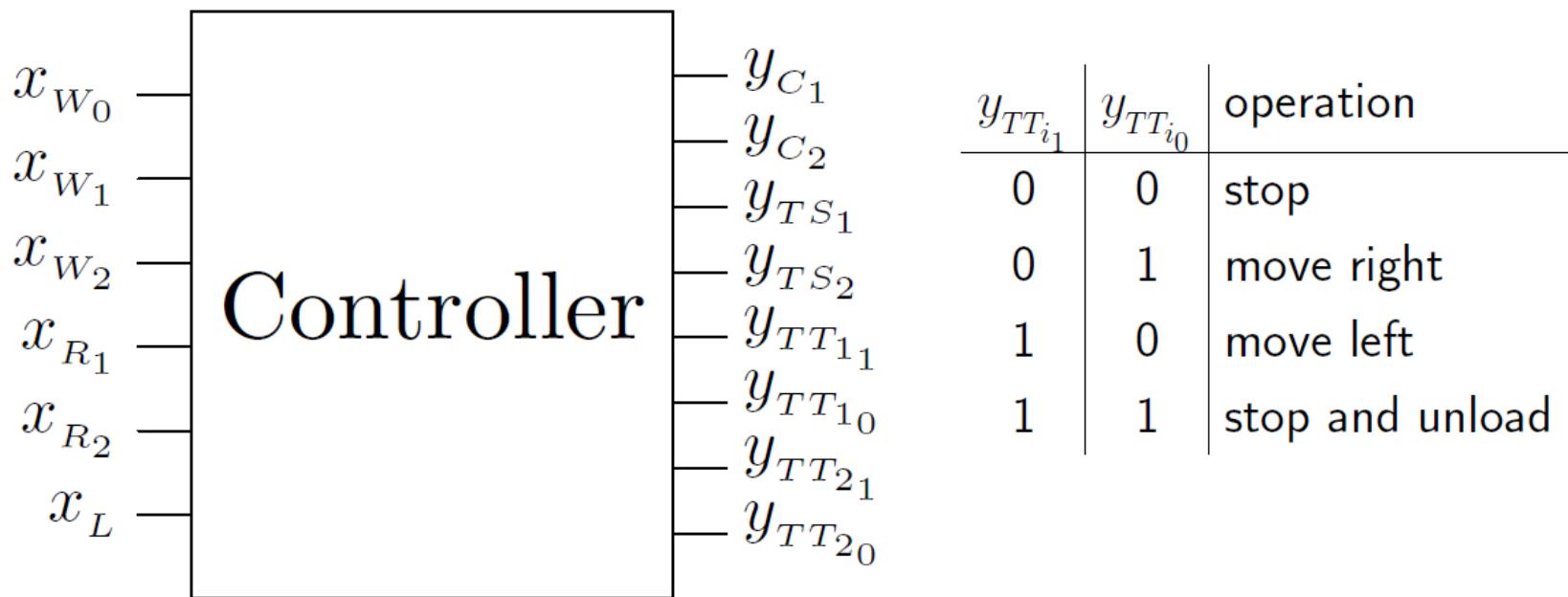




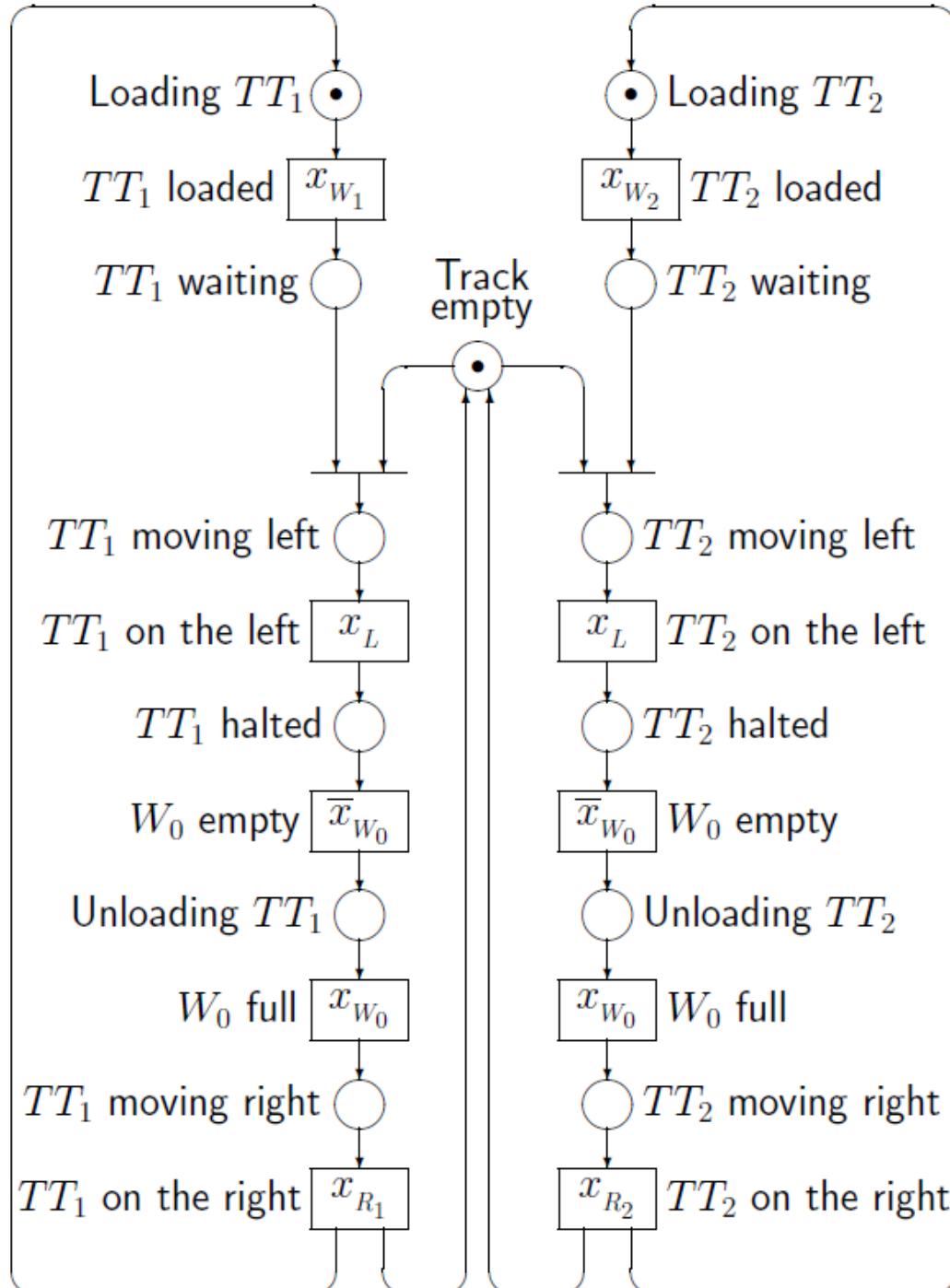


W_i – weight i , $i = 0, 1, 2$
 TT_j – tip-truck j , $j = 1, 2$
 C_k – container k , $k = 1, 2$
 TS – track switch

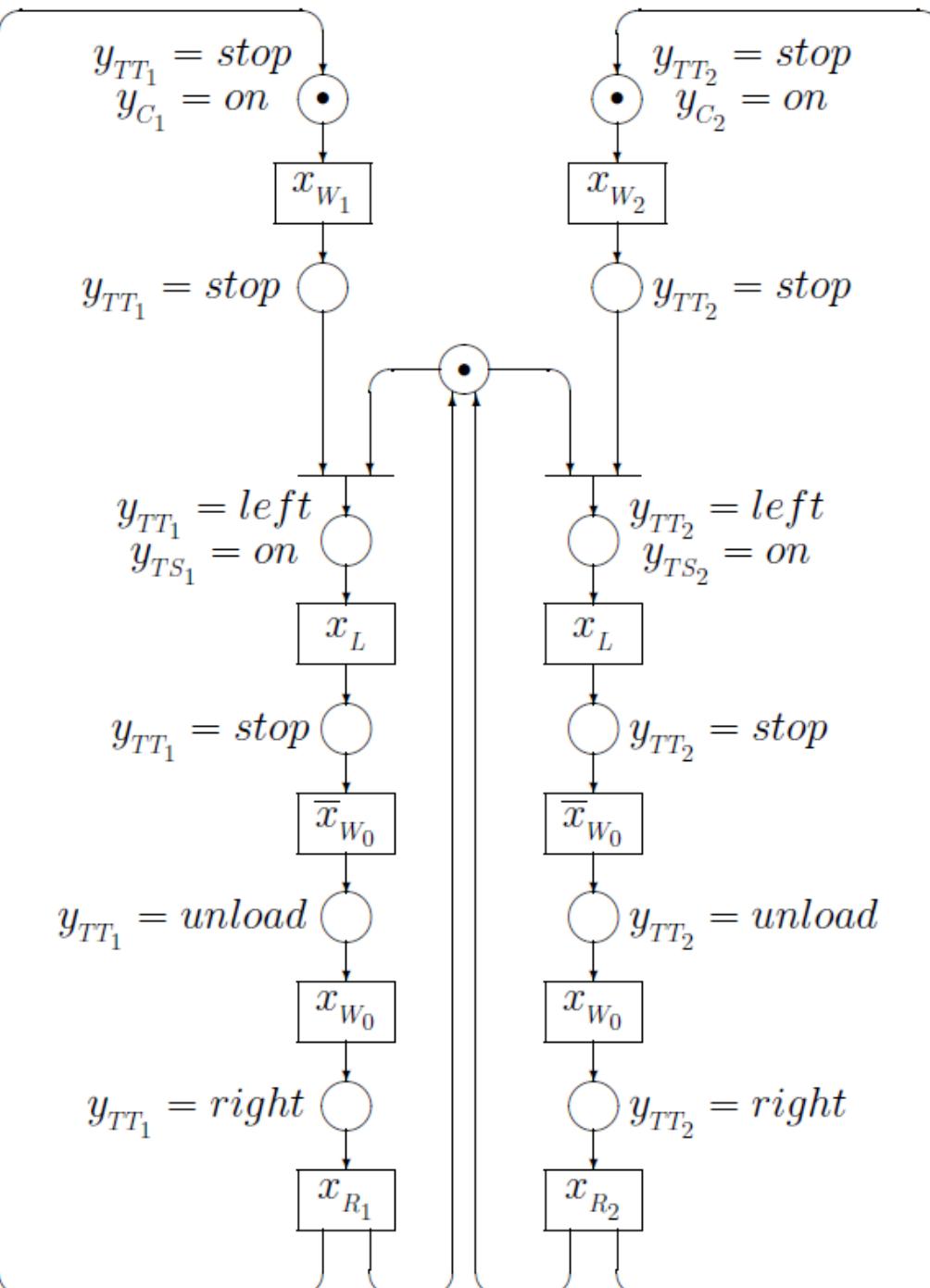




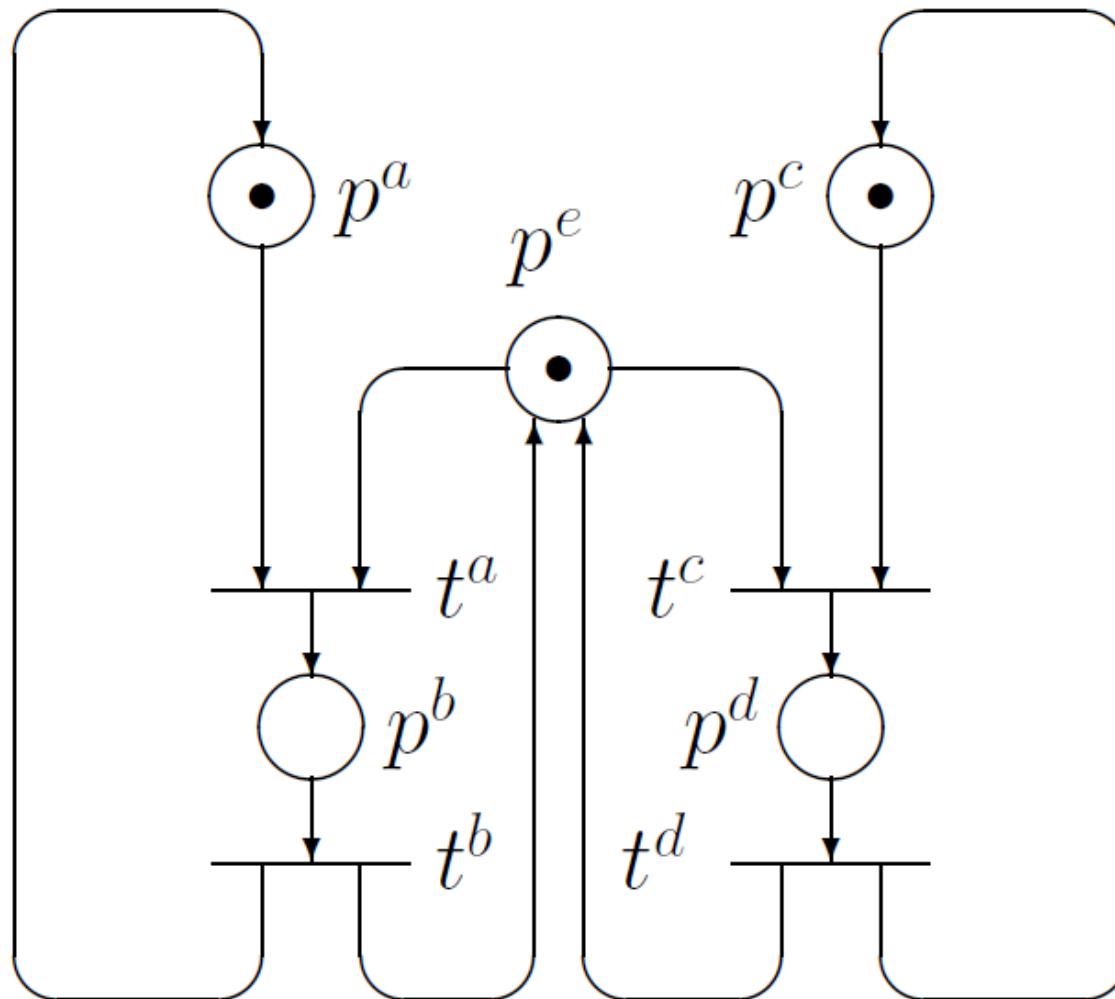
Petri net describing the tip- truck system operation



Petri net describing the tip- truck system operation



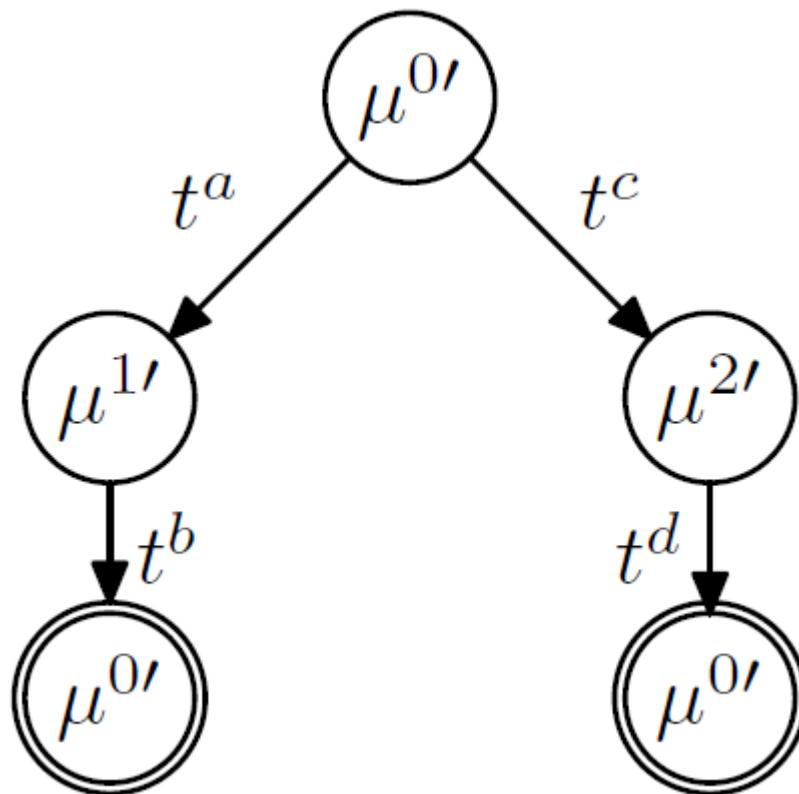
The compressed Petri net



Possible markings of the Petri net

i	$\mu^{i\prime}(p^a)$	$\mu^{i\prime}(p^b)$	$\mu^{i\prime}(p^c)$	$\mu^{i\prime}(p^d)$	$\mu^{i\prime}(p^e)$
0	1	0	1	0	1
1	0	1	1	0	0
2	1	0	0	1	0

Reachability tree

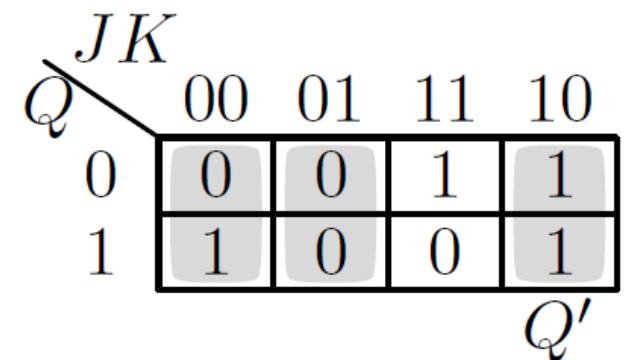
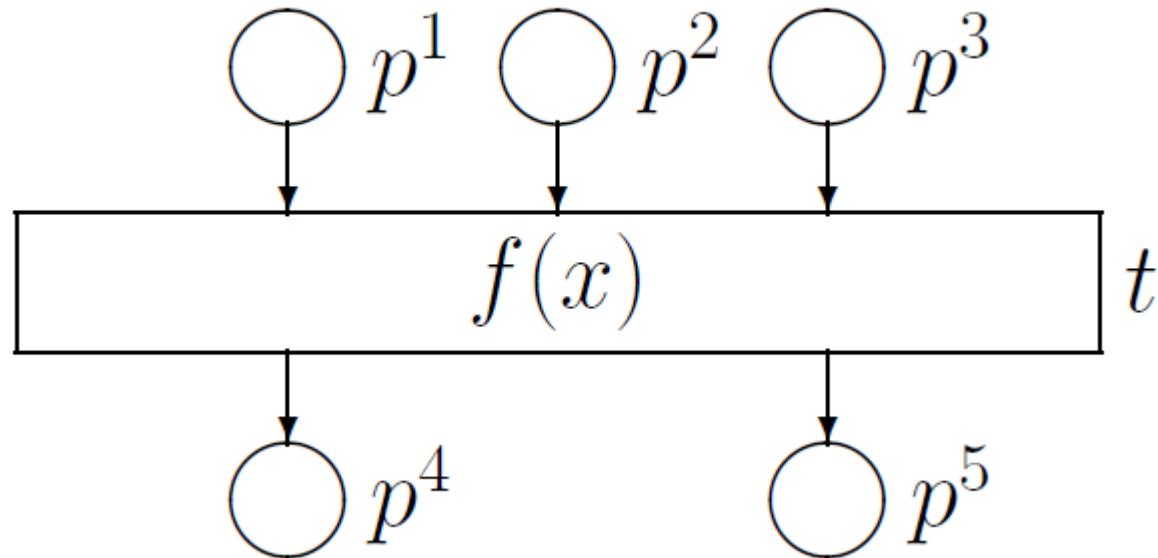


Transformation of the reachability graph into a state transition graph

The reachability graph becomes the state transition graph subject to following modifications:

- Each node of the reachability graph becomes a node of the state transition graph:
- Each arc of the reachability graph becomes an arc of the state transition graph.

Transformation of an extended Petri net into a circuit diagram

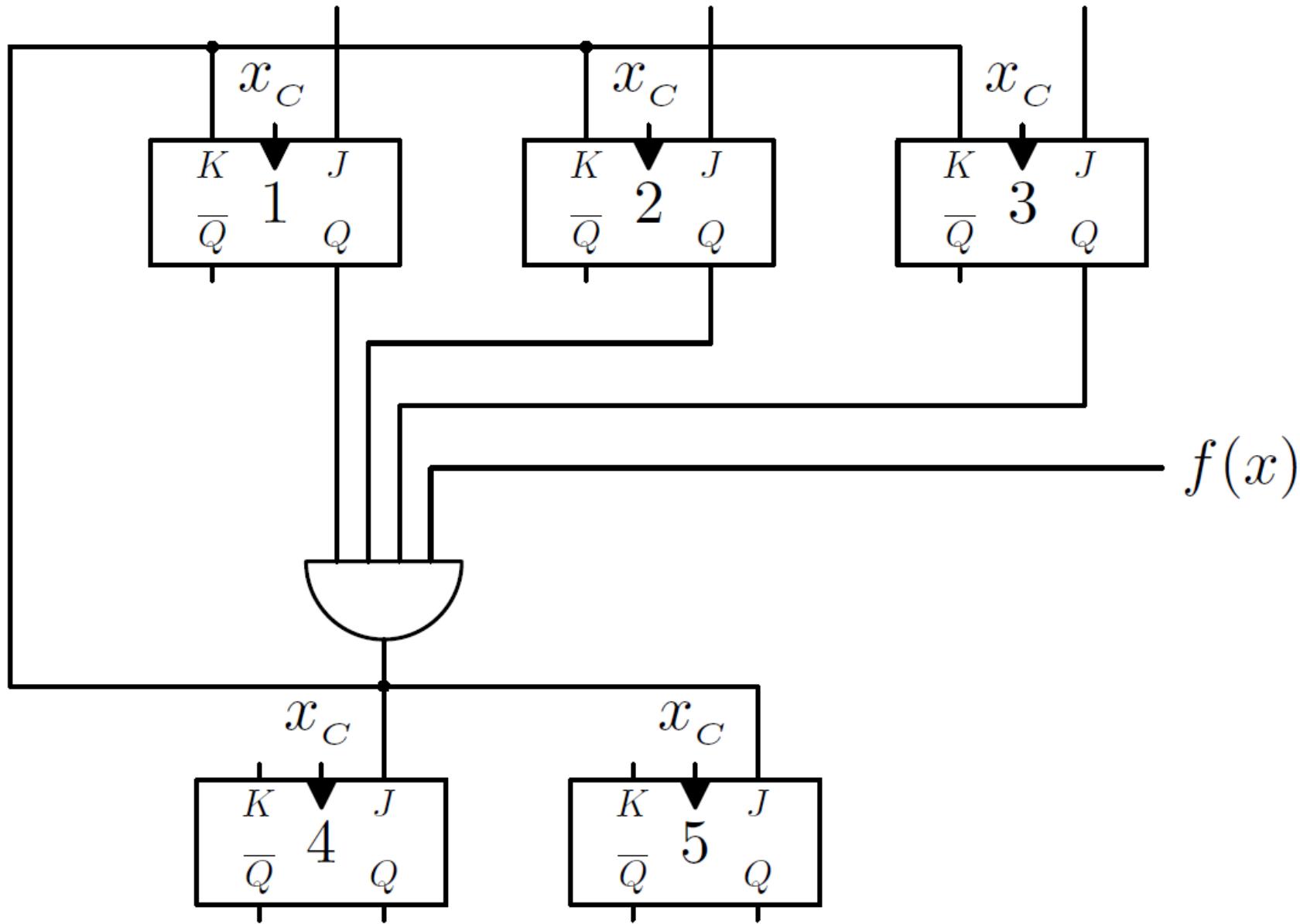


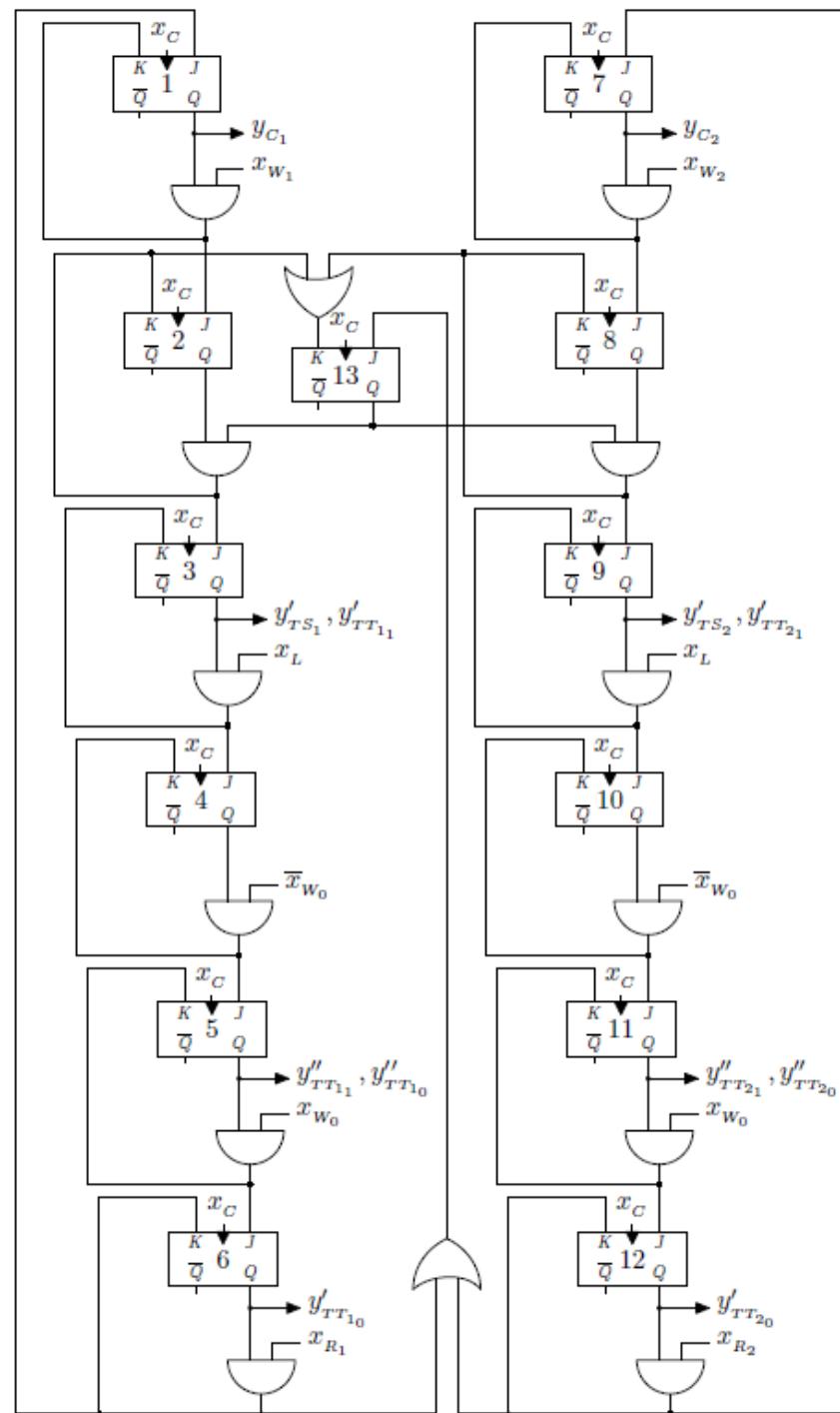
A JK flip-flop truth table showing the relationship between the inputs J and K , the current state Q , and the next state Q' .

J	K	00	01	11	10
0	0	0	0	1	1
1	1	1	0	0	1

The table shows the following transitions:

- From $Q=0$ and $J=0, K=0$ to $Q'=0$
- From $Q=0$ and $J=0, K=1$ to $Q'=1$
- From $Q=1$ and $J=0, K=0$ to $Q'=1$
- From $Q=1$ and $J=0, K=1$ to $Q'=0$
- From $Q=1$ and $J=1, K=0$ to $Q'=0$
- From $Q=1$ and $J=1, K=1$ to $Q'=1$





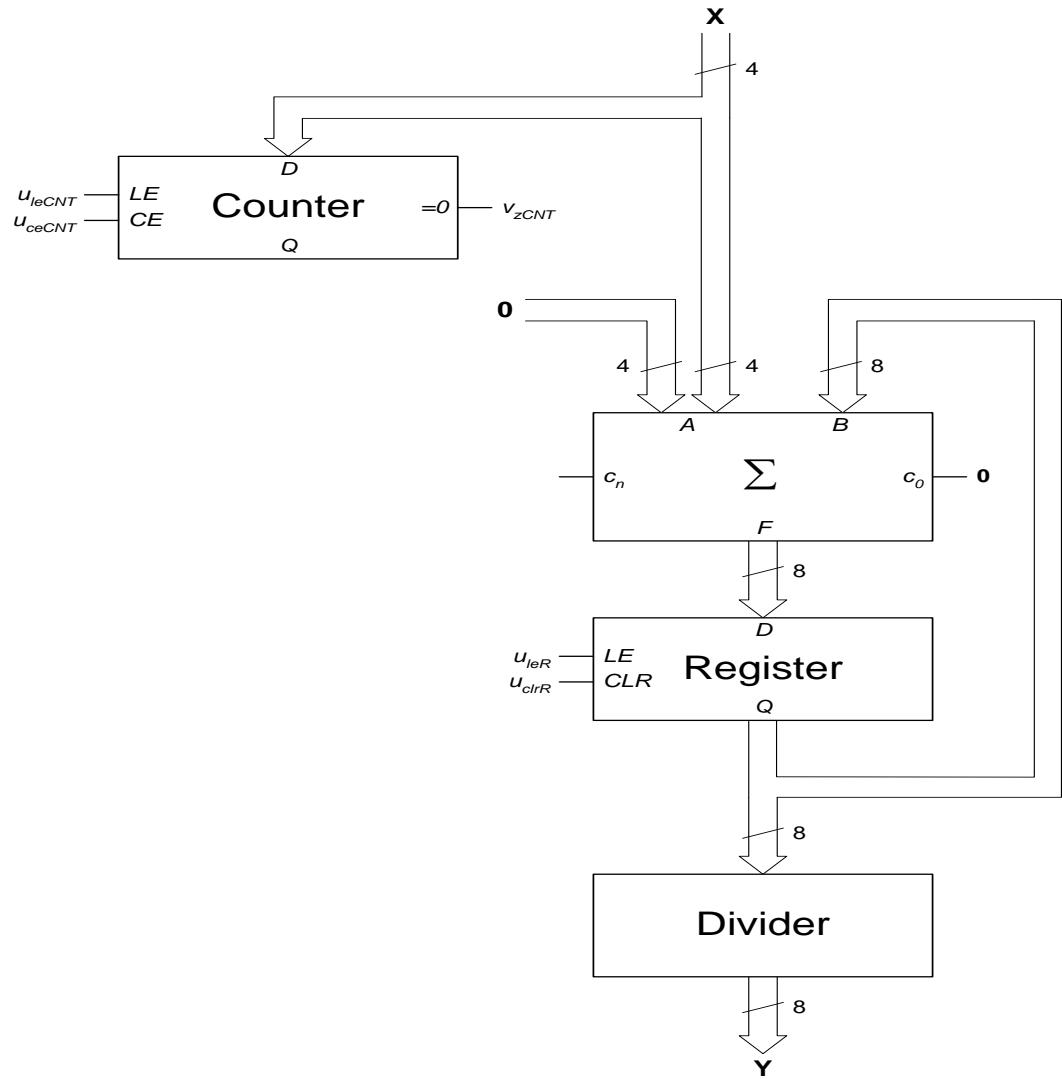
Examination Rules

- Correct, *legible* schematic drawing.
- Microprogramming flow-chart style.
- Use of standardized functional blocks
(mentioned in lecture slides)
- „*Legal*” handshaking.
- Use of names given in the task.

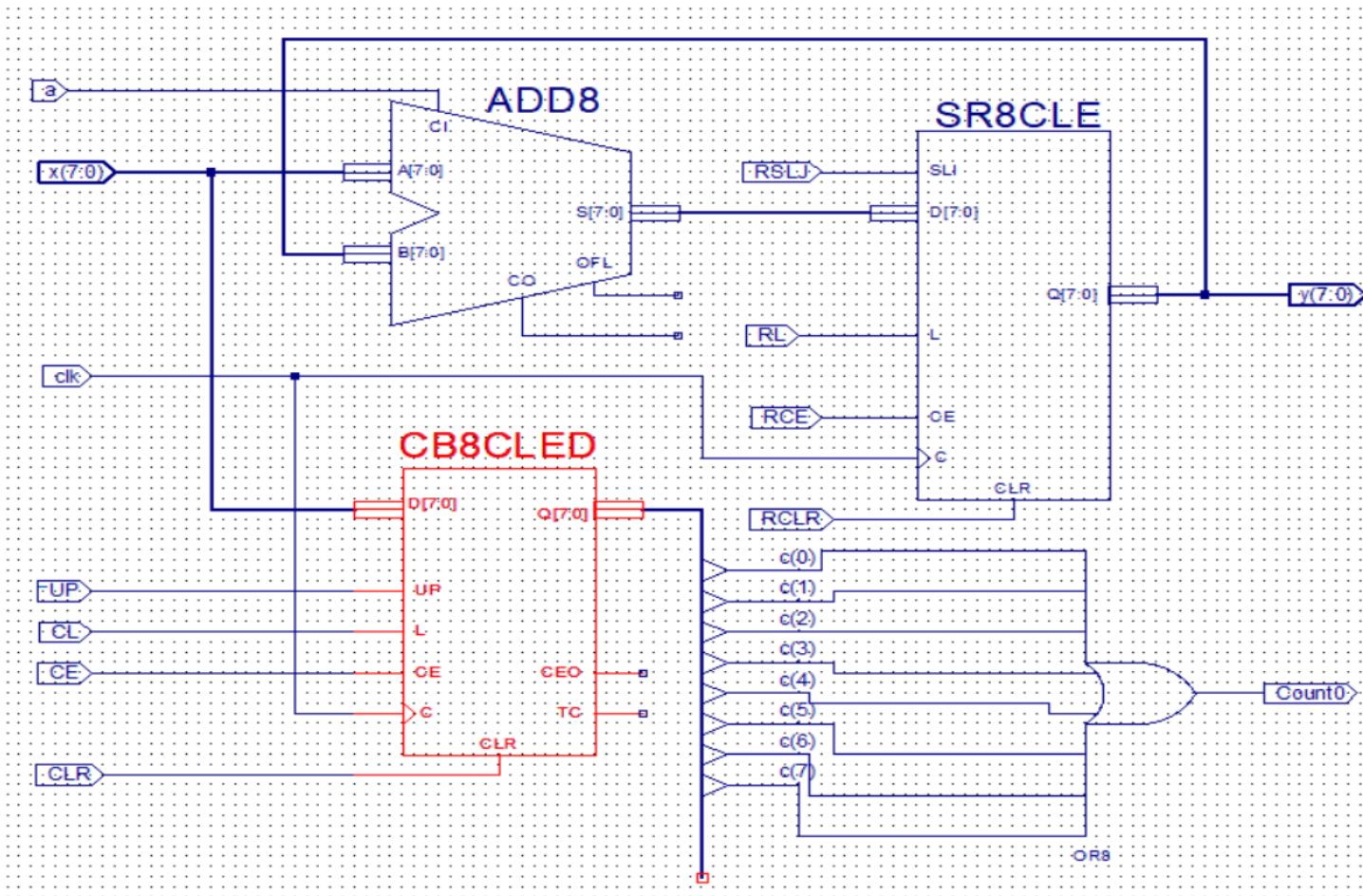
*Works that do not meet all the rules will not
be assessed*



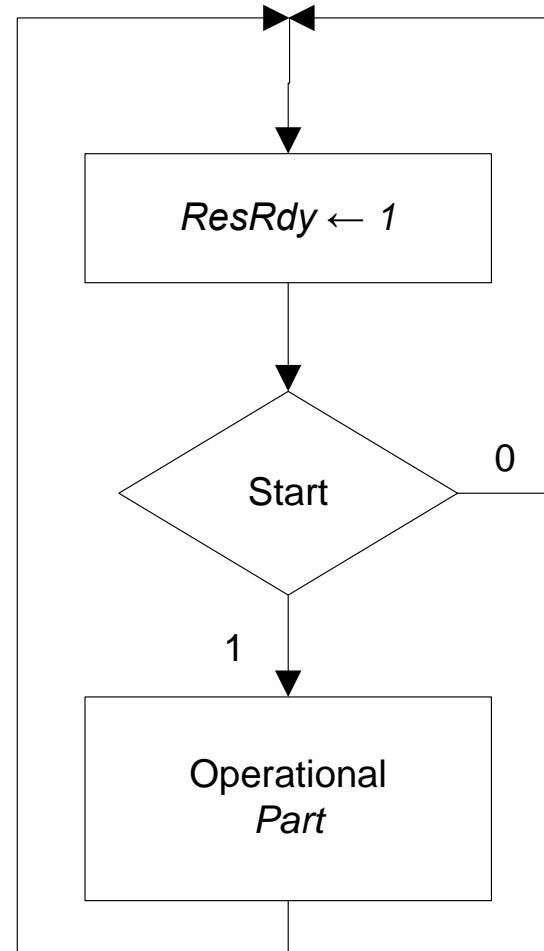
Generic style schematic:



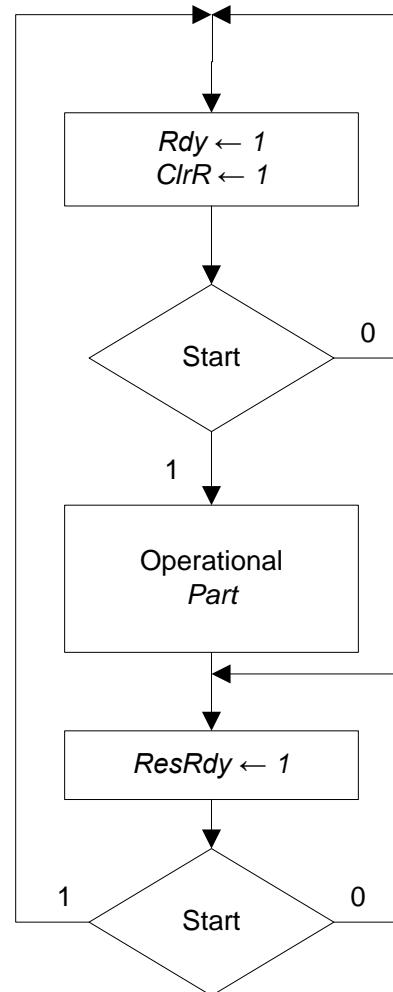
Xilinx style schematic:



Micro- programming Flow-Chart style

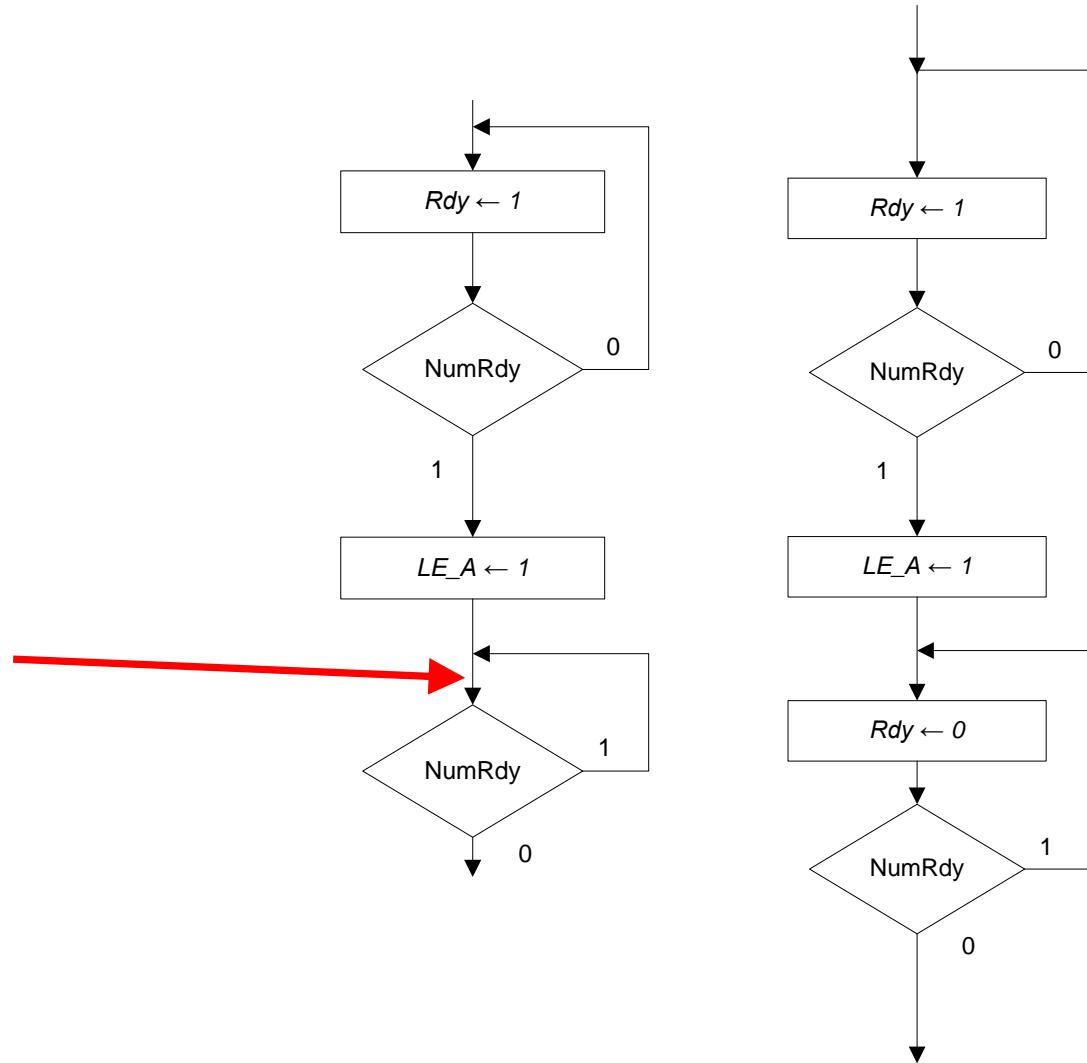


Start / Result Cooperation



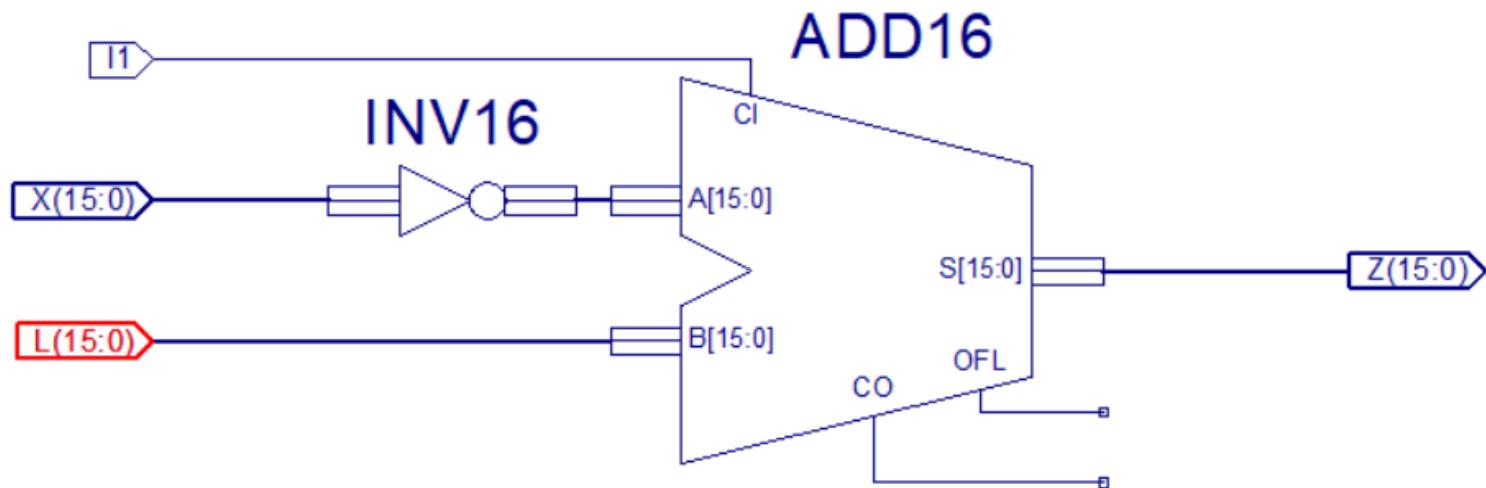
Number Reading

Must insert a state



Positive to negative number conversion

$$-x = \bar{x} + 1$$

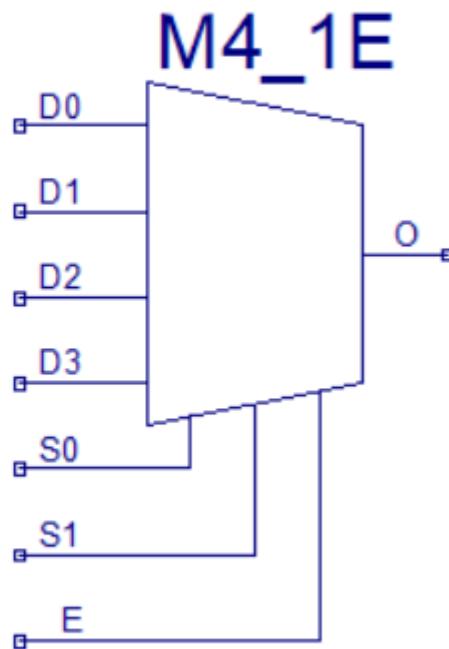
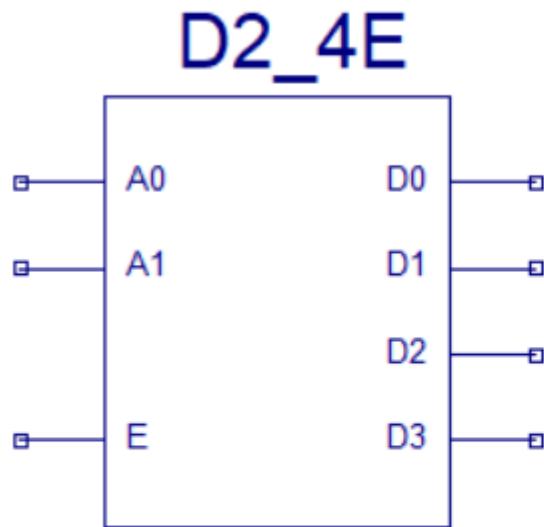


Warning: *In most cases use of dedicated full-adders is impractical*

Hints

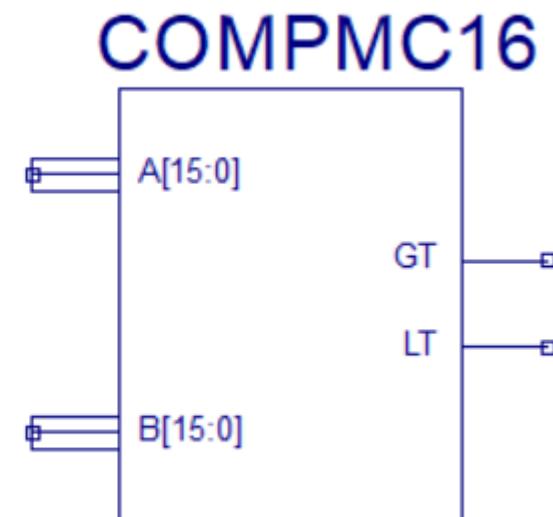
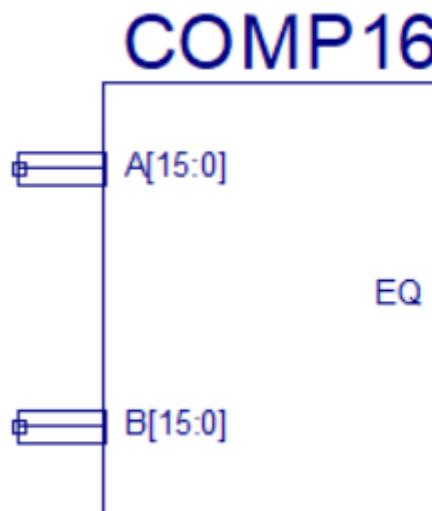
- Use existing adder to add 1
- Set c_{in} to 1 with the control unit
- If it is not possible use half adder
- For controlled addition / subtraction use xor gates

2^k to k conversion

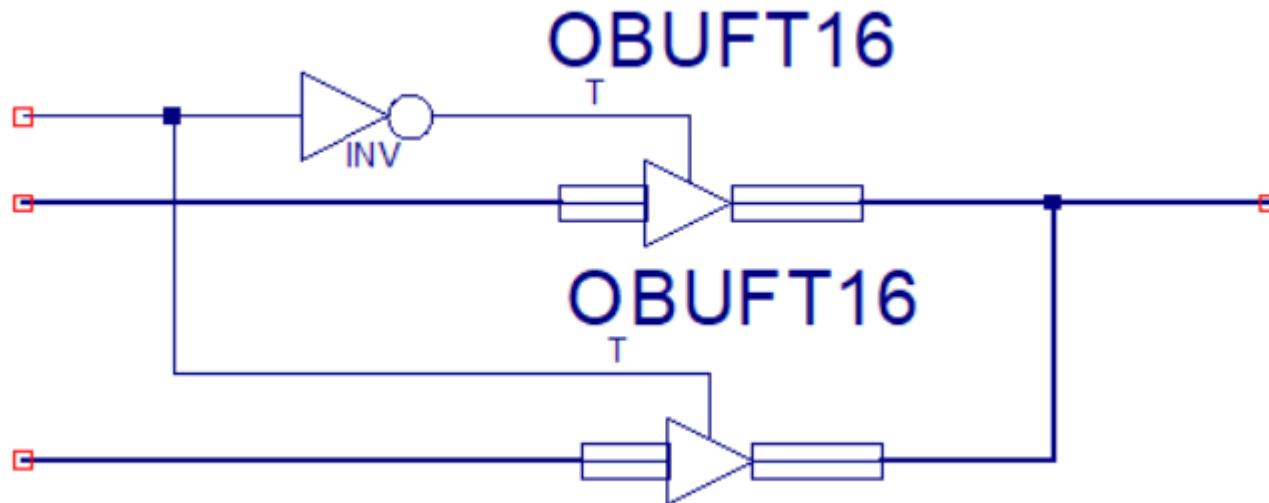




Number comparison



Three state buffer switch – connection of outputs



Examination Problem

Design a digital system computing the mean of the rounded +/- sum of 3th power of the series of the natural binary coded 8 bit numbers:

$$y = INT \left[\sum_{i=0}^{k-1} (-1)^k x_i^3 / k \right] = (x_0^3 - x_1^3 + x_2^3 - x_3^3 \dots) / k$$

$$k = 2^j, j < 8$$

The circuit first receives at a parallel bus A the number j then x_0, x_1, x_2, \dots follows.
Computation speed and accuracy are critical factors.
Hardware optimization is less important but necessary.
Handshaking is implemented using following signals:

- Start = 1 (*start*) : signals beginning of a new data series
- Nrdy = 1 (*number ready*) : signals a new number on the input
- Rdy = 1 (*ready for next number*): requests the next number
- RR = 1 (*result ready*) : signals the readiness of the result

Problem Analysis

- Two stage multiplication: $x*x$, then $x*x^2$
- We need two multiplication units
- Division by $k - j$ times shift to the left
- Input numer is 8 bit, so the square is 16 bits.
- The qube must hold 24 bits.
- Sum of qubes is 31bits.
- Final result is 24 bits.



Algorithm

φ

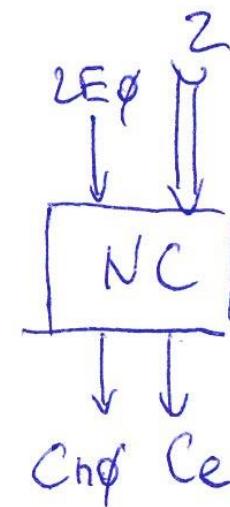
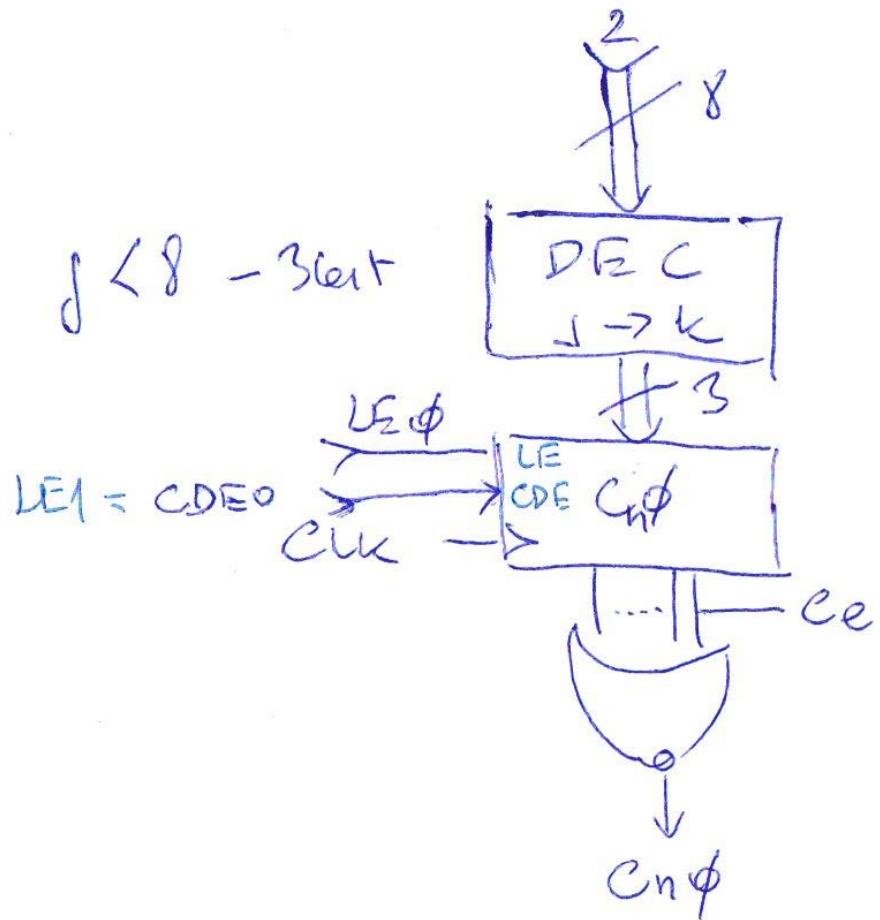
1. Clear result (Reg F)
2. Load j into C1 and k into Cφ
3. Load Z into Reg A, Reg B,
Reg D, clear Reg R
4. Multiply RA × RB
5. Load product into Reg E
6. Multiply RD × RE, adding
1 if $C_{j,\phi}$ is odd

Parallel algorithm ?

NUMBER COUNTER

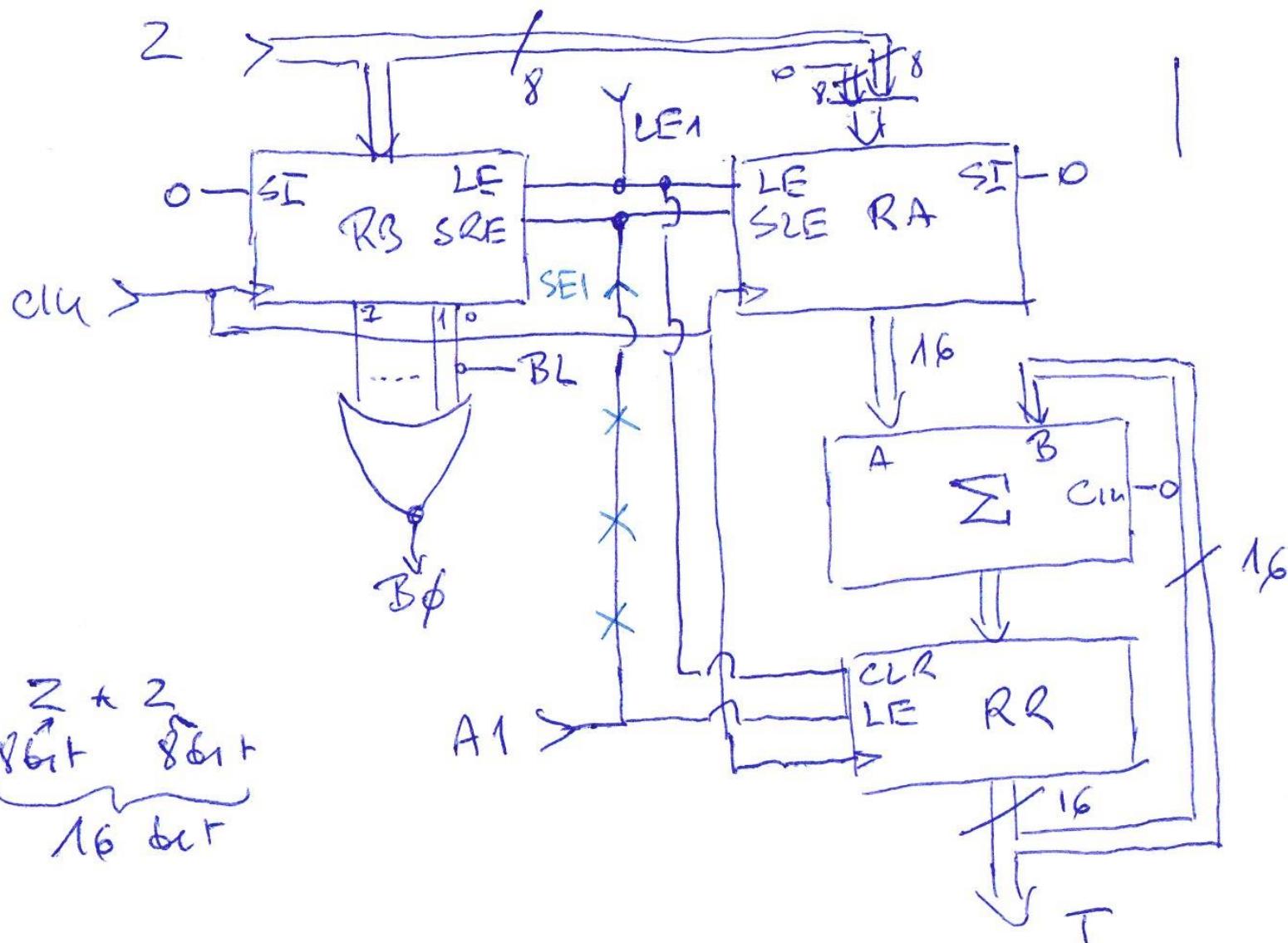
1

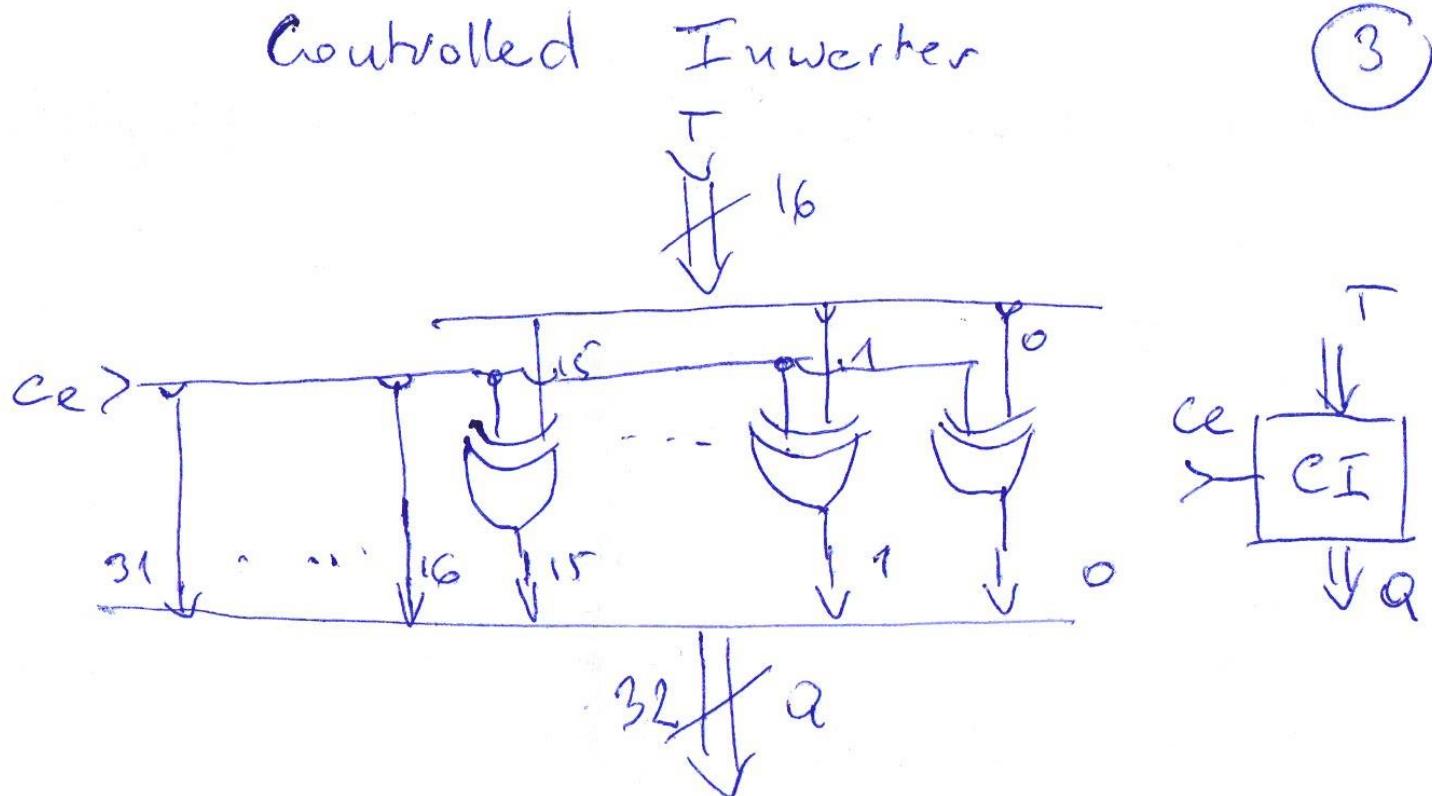
JL8 - 36er



Z^2 multiplication unit

(2)

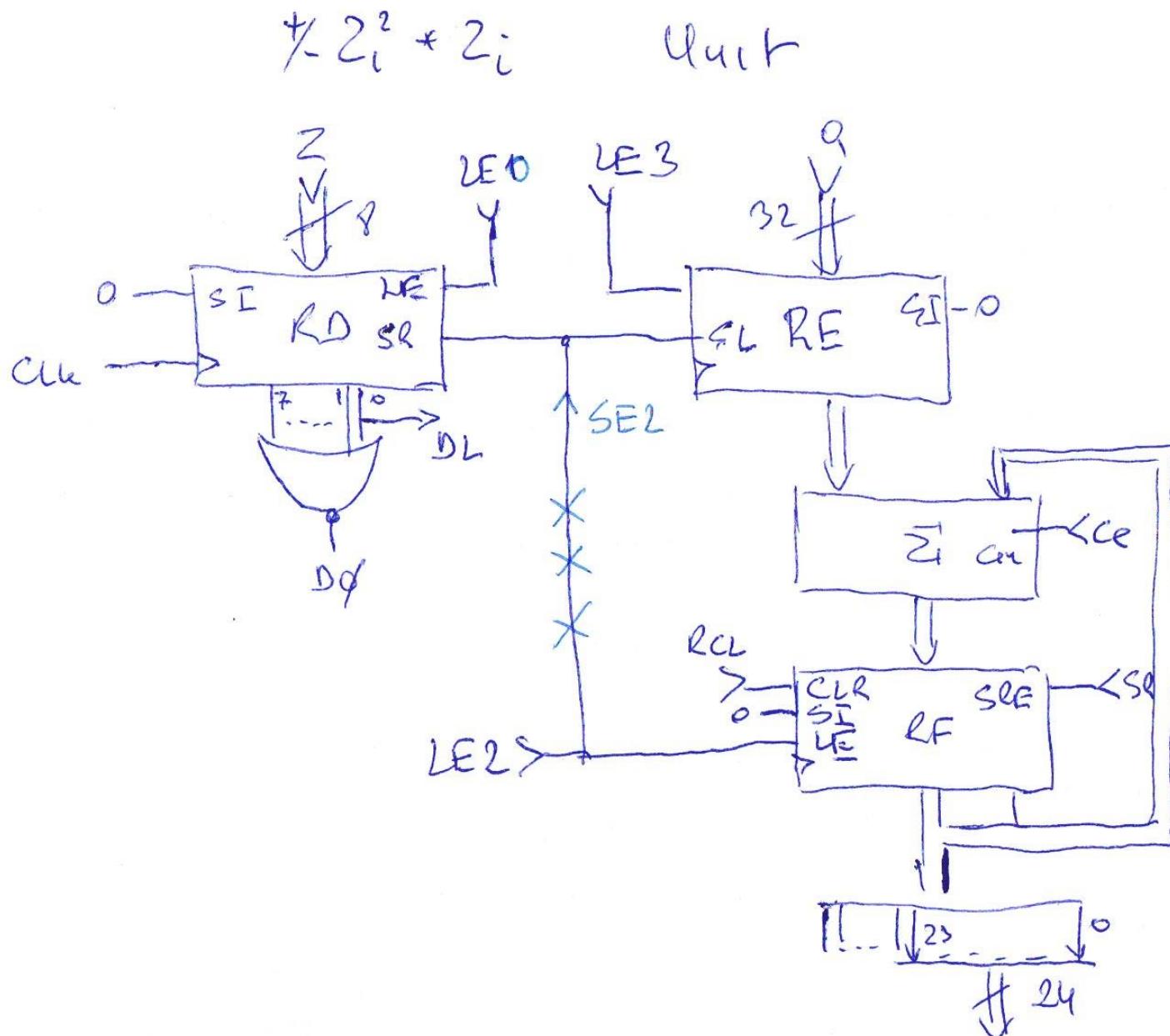




$2 \times 2 \times 2$
8bit 8bit 8bit - 24bit
sum of 2^7 numbers ≈ 31 bit
↓
assumed 32 bit

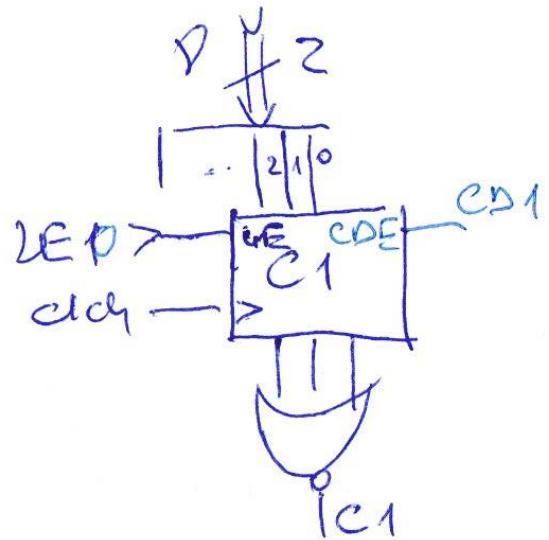
↓ will be added
later

(4)



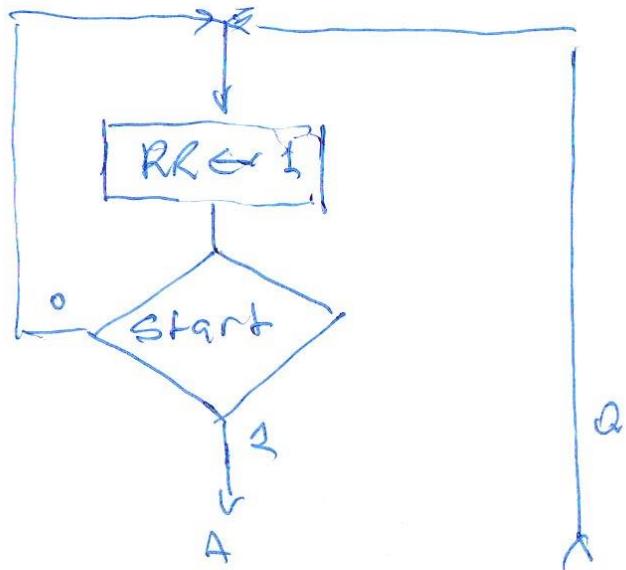
Division unit

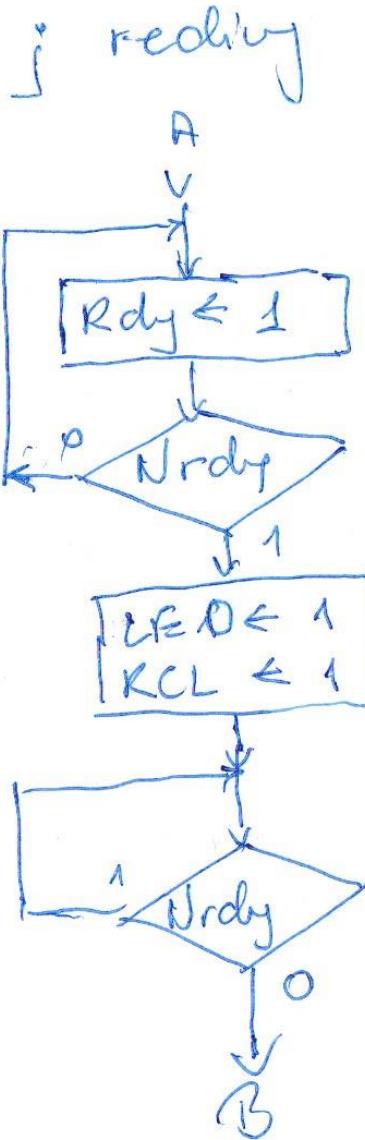
(5)



Flow chart: Start handschrift

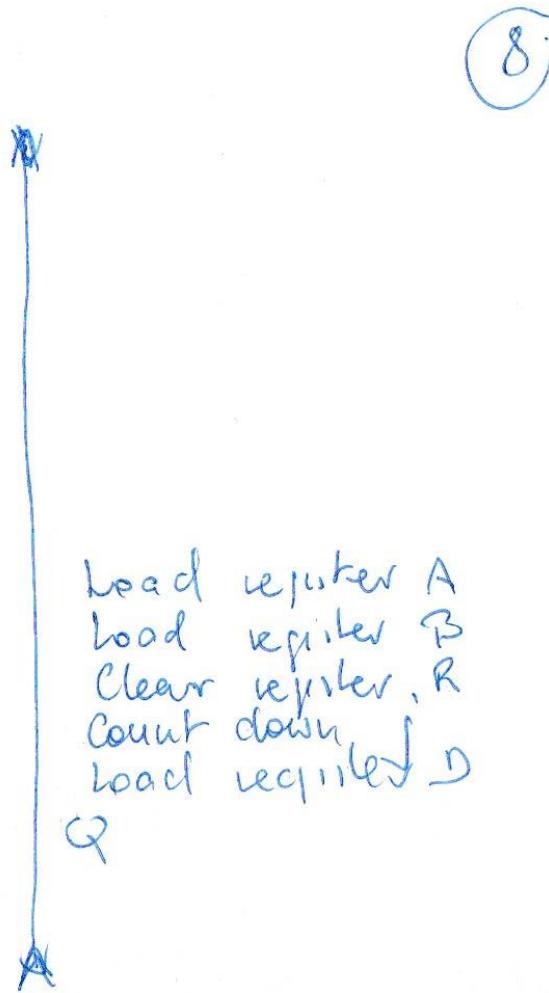
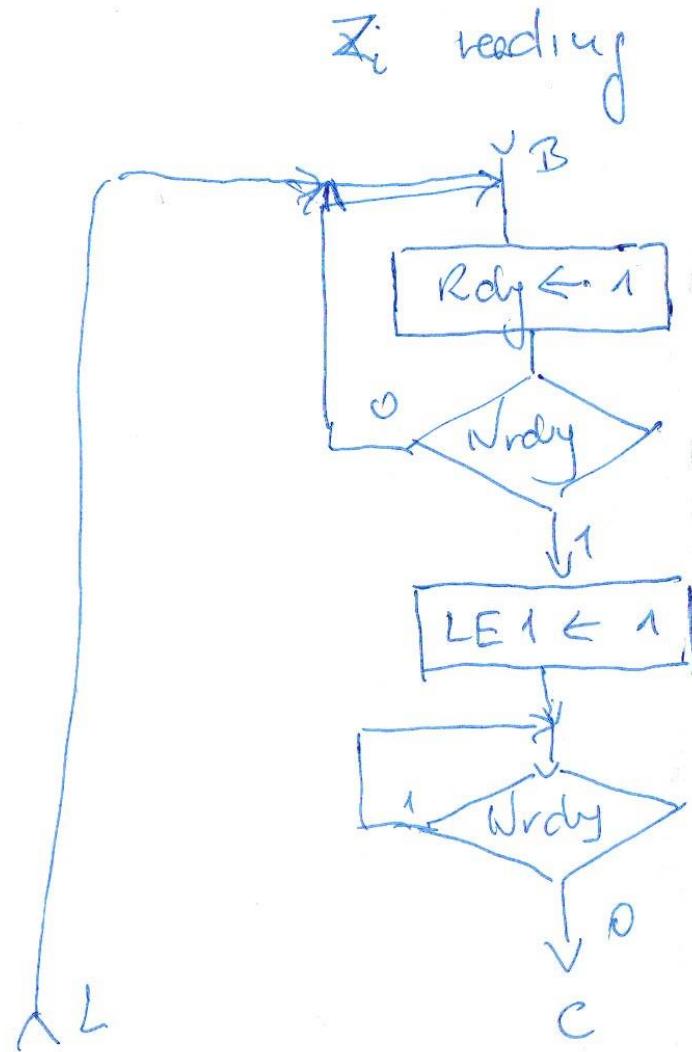
6

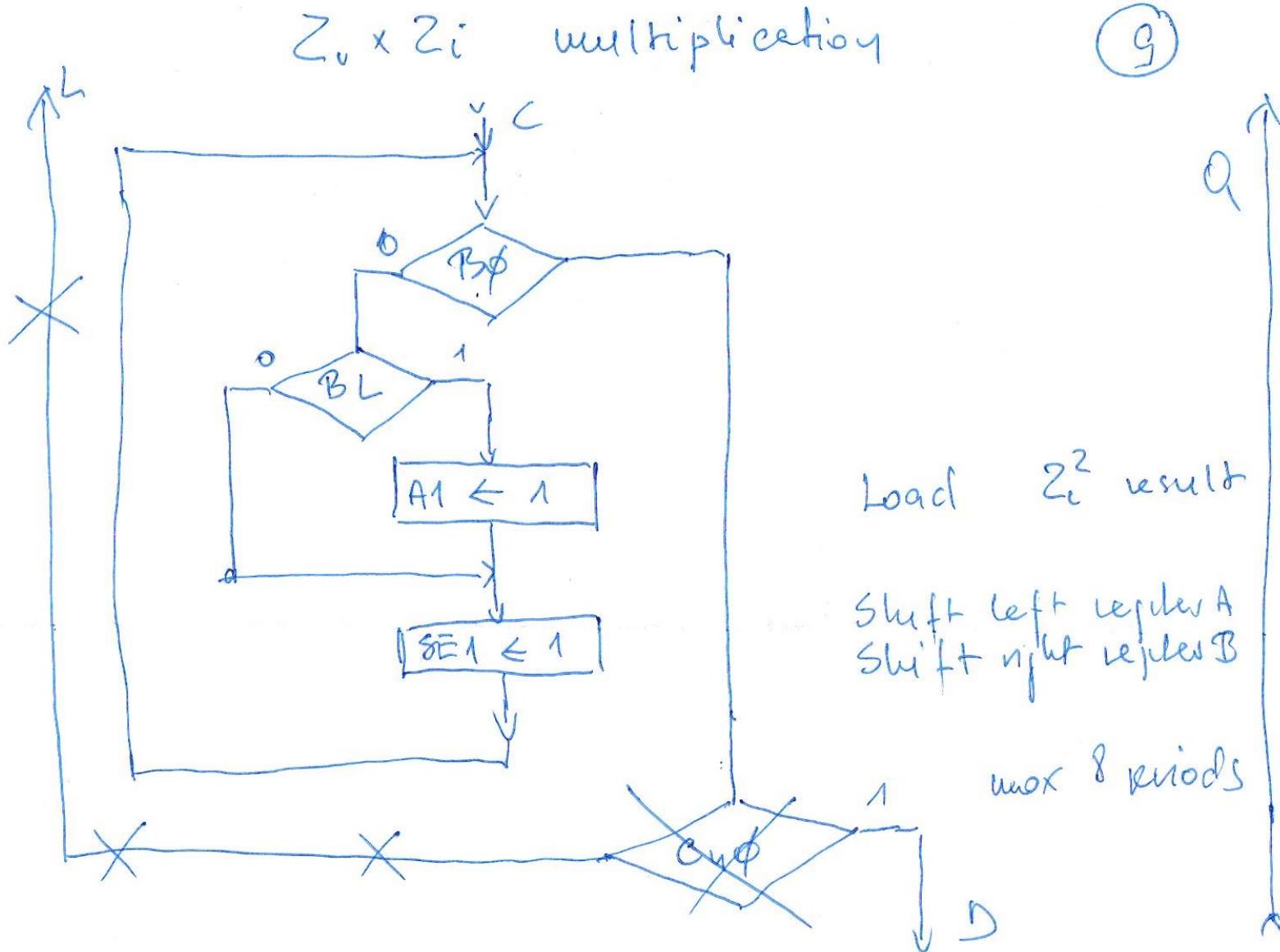




Load counter
Load counter K
Clear result F
Load ?

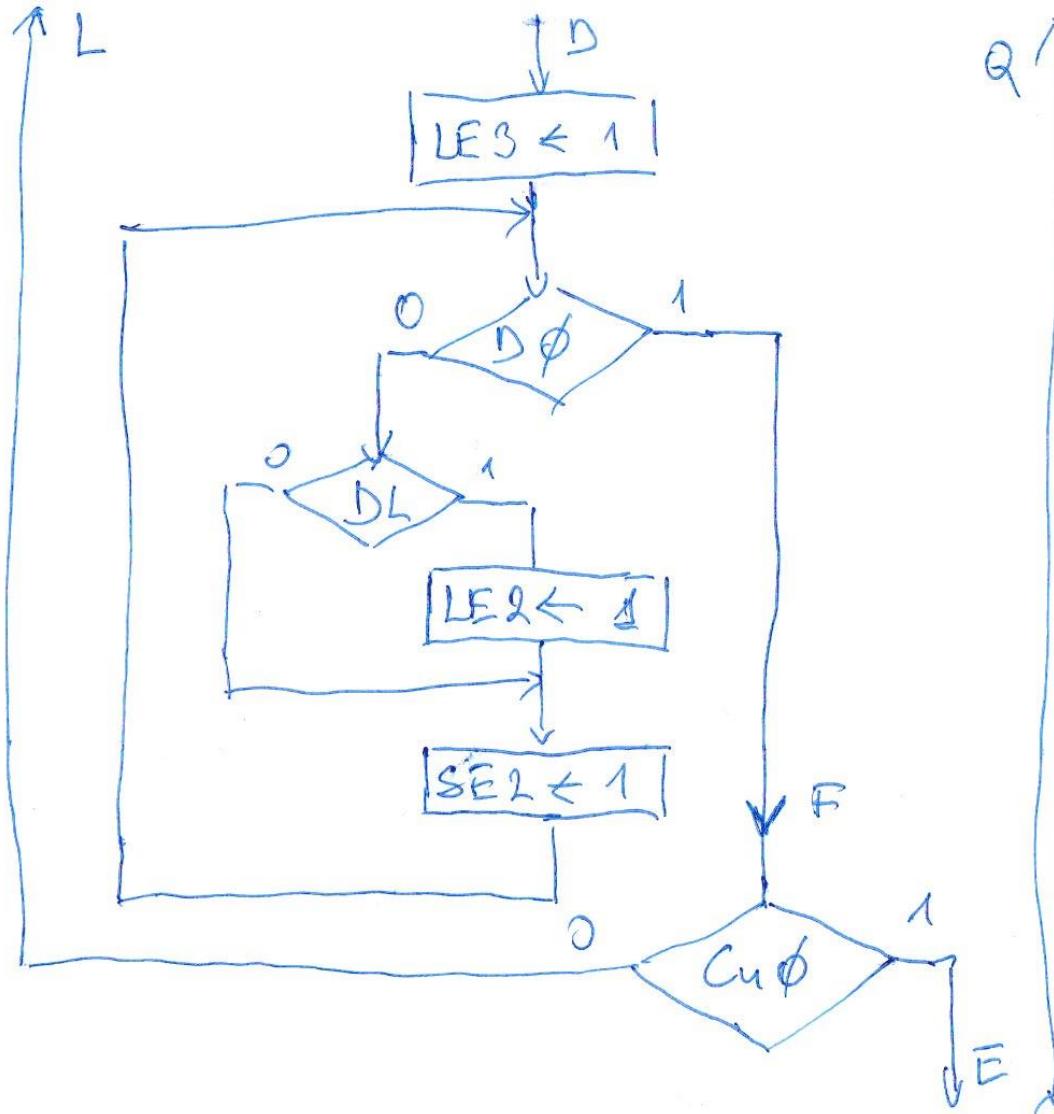
⑦





$2^2 \times 2^2$ multiplication

(10)



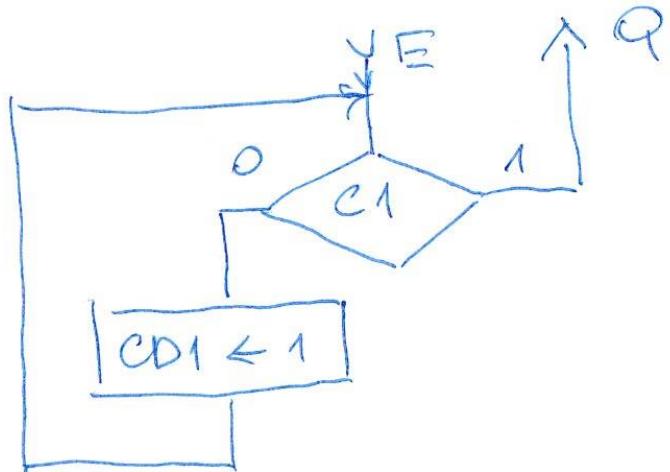
Load register F

Shift left register E
Shift right register D

max 8 periods

Final division

(11)



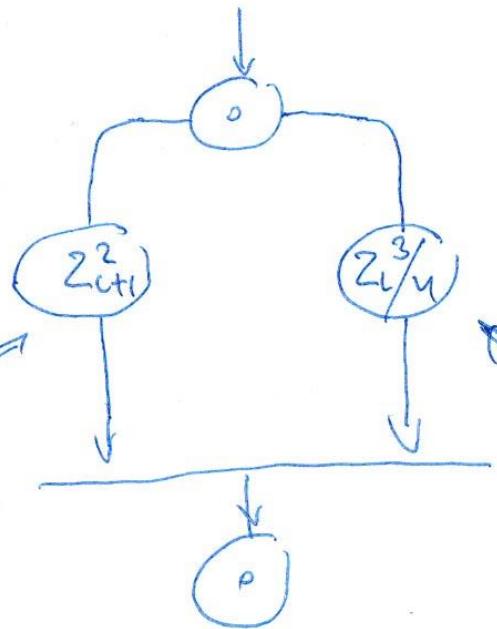
max 7 periods

(12)

Concurrent version

Current square
 (2^{i+1})

8 periods max

Previous number
cube and
division16[?] + 7 periods
max
8!

Examination Problem

Design a digital system computing the mean of the rounded sum of 2nd power of the series of the natural binary coded 8 bit numbers:

$$y = INT \left[\sum_{i=0}^{15} x_i^2 / 16 \right]$$

The circuit first receives at a parallel bus A the x_0, x_1, x_2, \dots

Computation speed and accuracy are critical factors.
Hardware optimization is less important but necessary.
Handshaking is implemented using following signals:

- Start = 1 (*start*) : signals beginning of a new data series
- Nrdy = 1 (*number ready*) : signals a new number on the input
- Rdy = 1 (*ready for next number*) : requests the next number
- ResRdy= 1 (*result ready*) : signals the readiness of the result

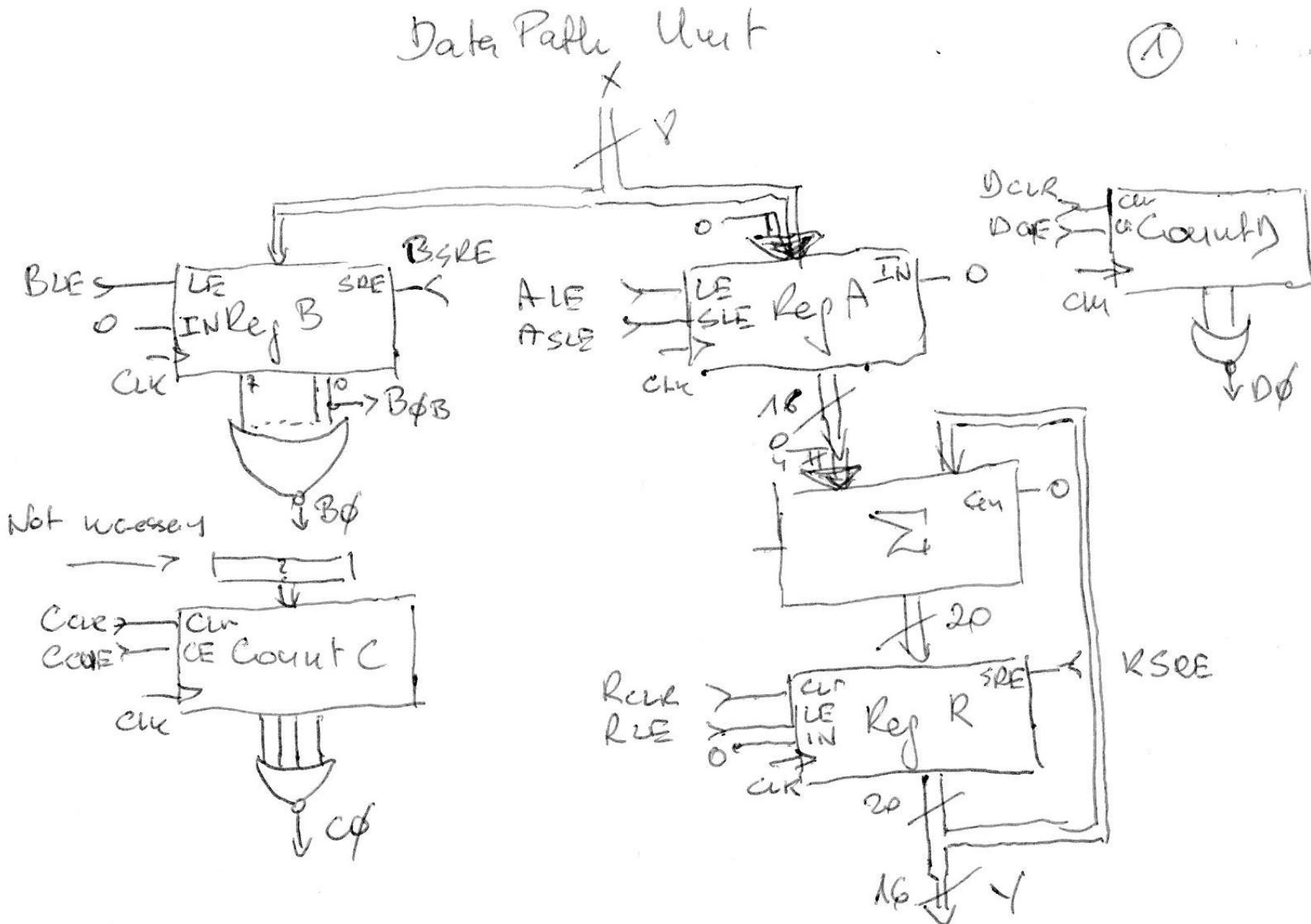


Sketch of Algorithm

φ

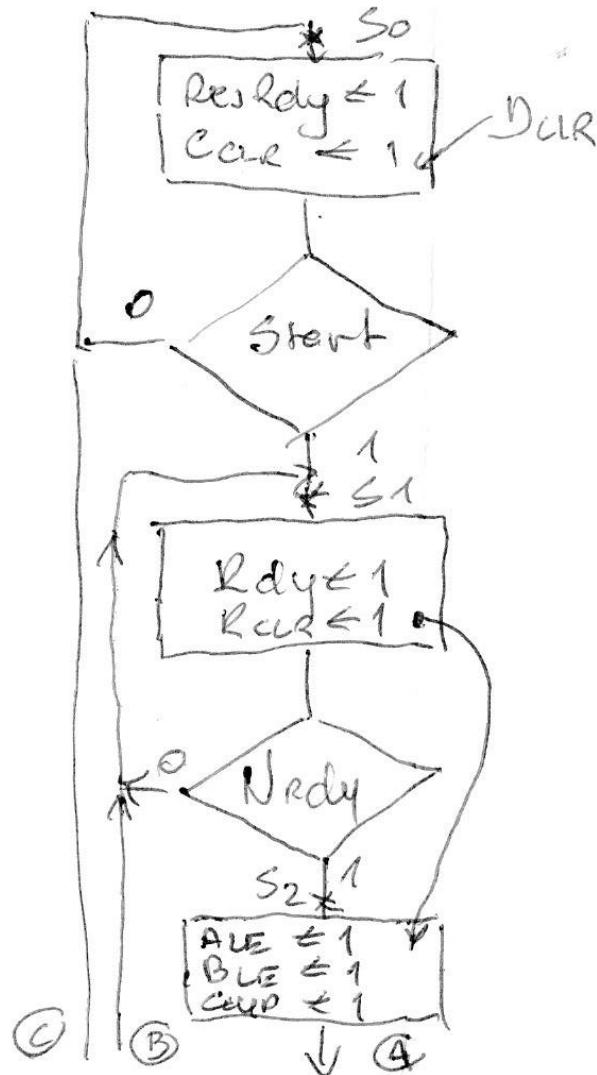
- ① Clear result register R, number counter C,
clear left counter D. count up C ↗
- ② Load input number into Reg. A and Reg B ↓
- ③ Test $B = 0$? if true goto 6
- ④ If LSS of B is 1 load R
- ⑤ Shift left A, shift right B, goto 3
- ⑥ Test $C = 0$, if false goto 2
- ⑦ Count up D, stuff right R
- ⑧ Test $D = 0$, if false goto 7
- ⑨ Show result is ready

Recurrence



(2)

Flowchart 1



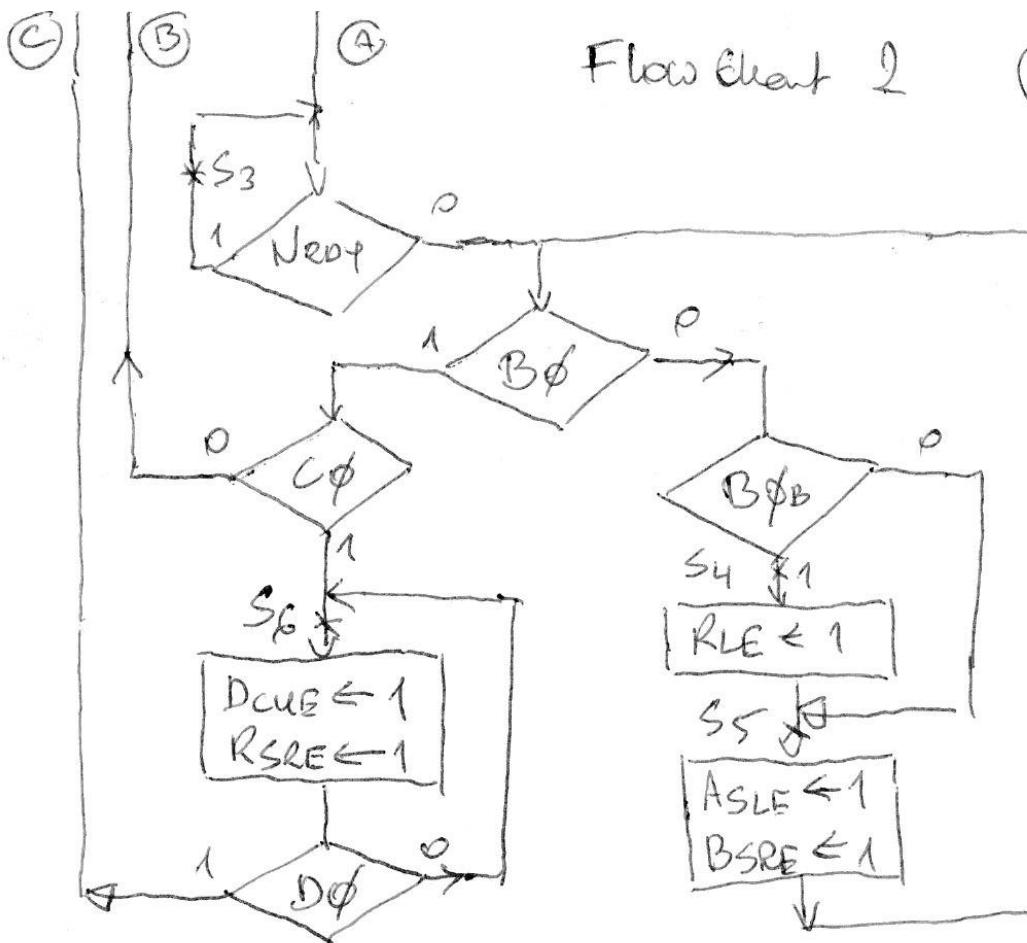
③

④

⑤

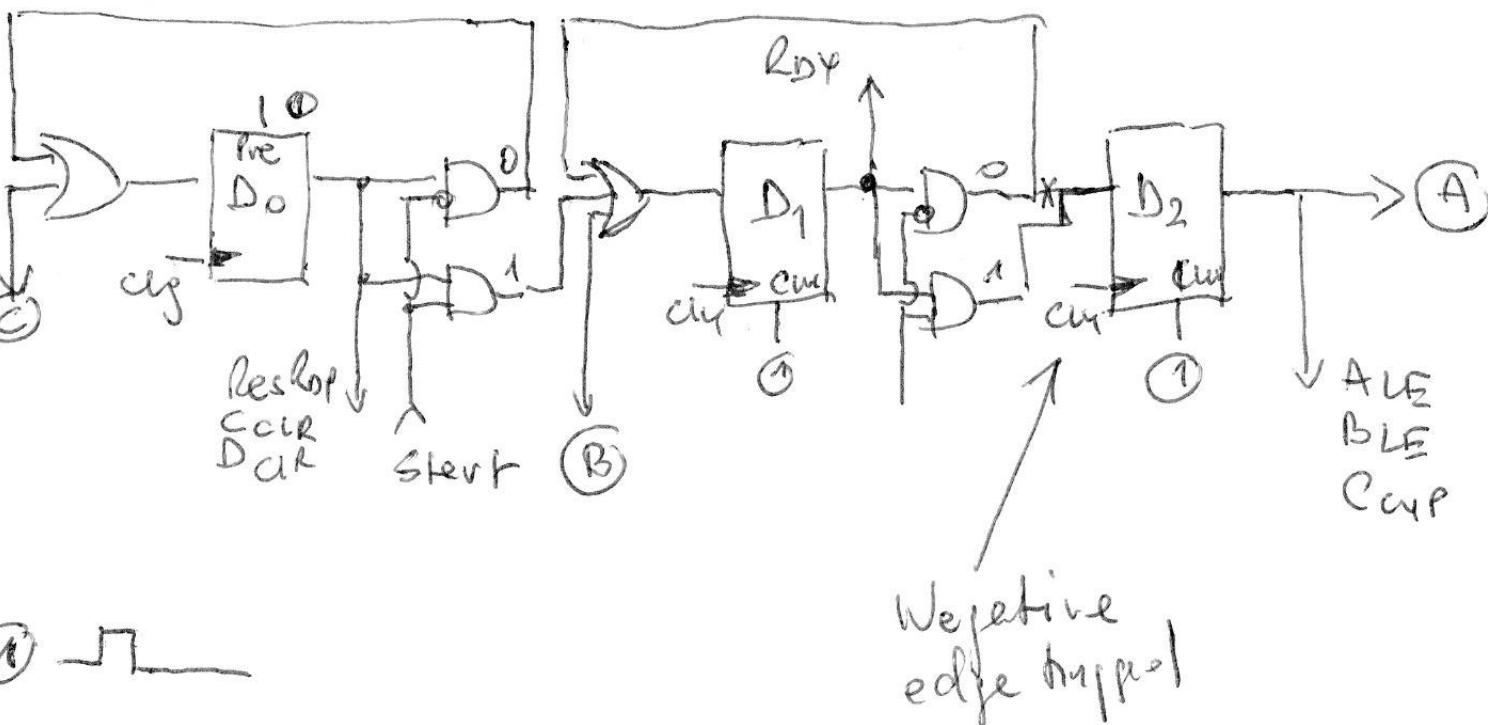
Flowchart 2

③



Sequencer 1

④



Problem Analysis

①

$$f = \text{Int} \left(\sum_{i=0}^{k-1} x_i^2 (-1)^i / k \right) = \text{Int} \left((x_0^2 - x_1^2 + x_2^2 - x_3^2 + \dots - x_{k-1}^2) / k \right)$$

$$f = \text{Int} \left[((x_0 - x_1)(x_0 + x_1) + \dots + (x_{k-2} - x_{k-1})(x_{k-2} + x_{k-1})) / k \right]$$

$$|x_i - x_{i+1}| \leq x_i + x_{i+1}$$

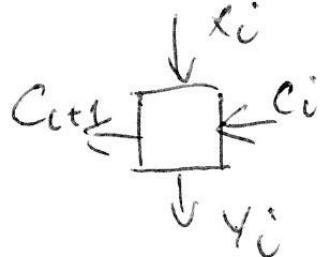
$$|x_i| < 8\text{bit} \quad |x_i| < 1 + 8\text{bit}$$

$$k = 16 - 4\text{bit}$$

- multiplication of absolute values
- addition - two's complement

$$-x = \bar{x} + 1 \quad \text{blocky}$$

(4)



x_i	c_i	0	1
0	1	0	
1	0	1	

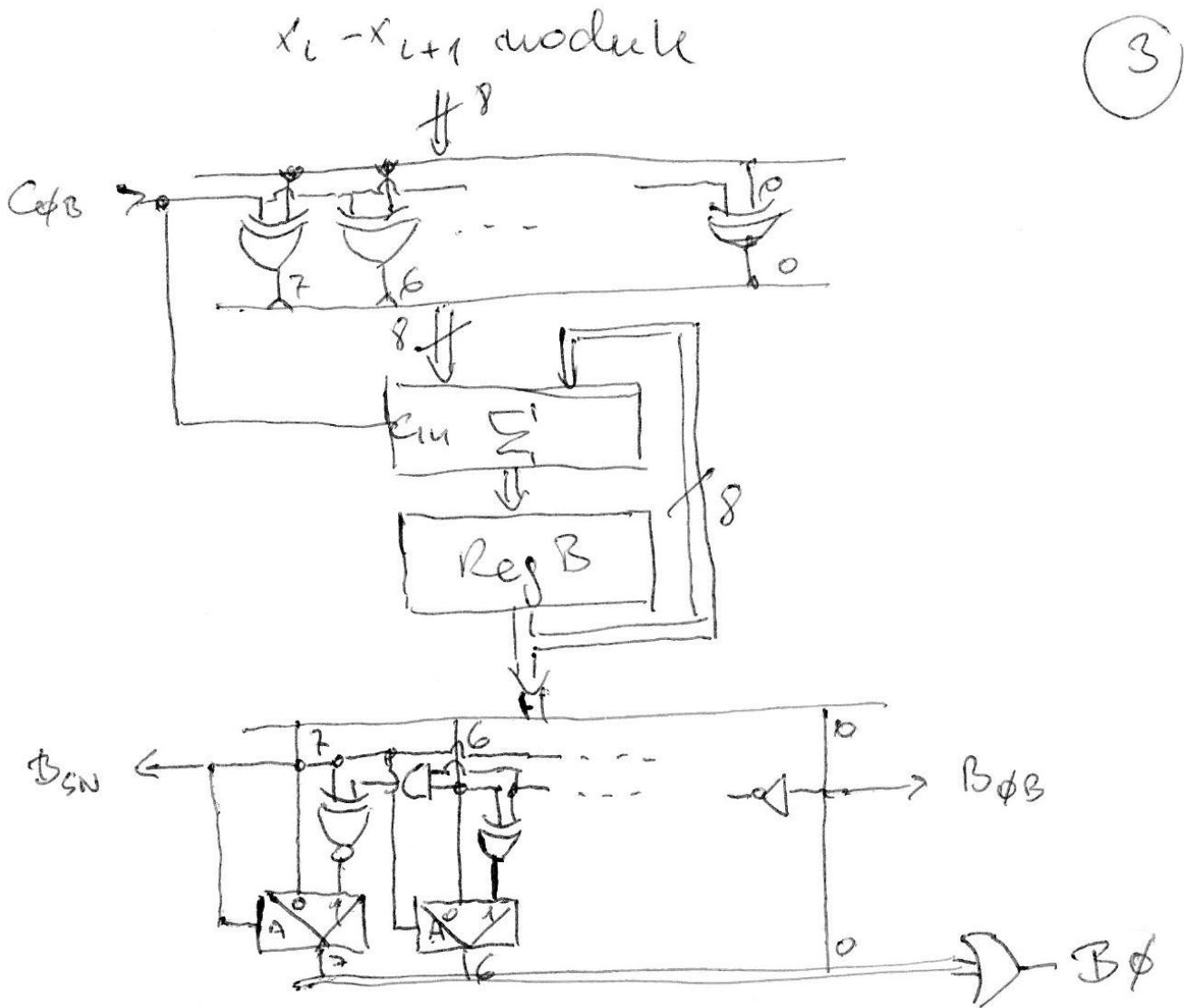
x_i	c_i	0	1
0	c	0	1
1	0	0	

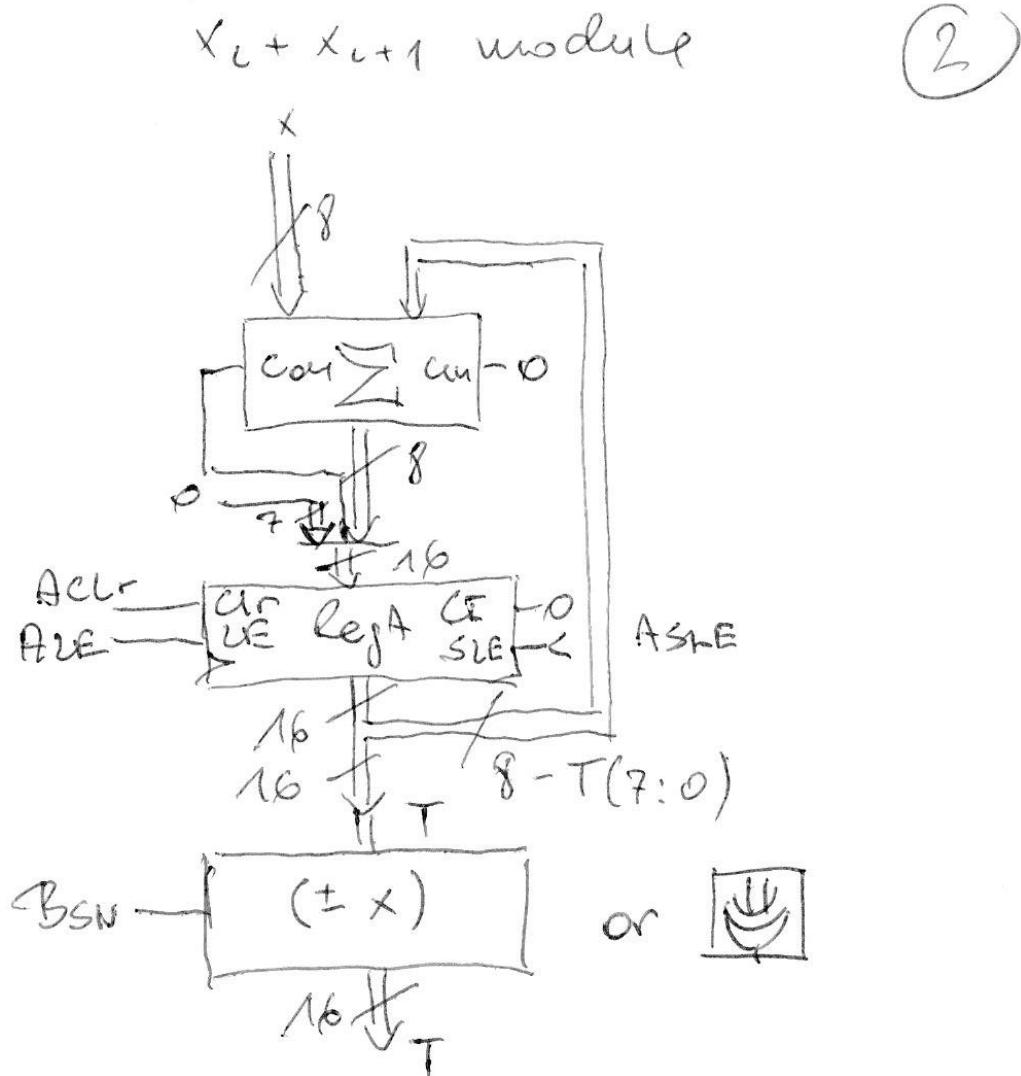
$$y_i = \overline{x_i \oplus c_i}$$

$$c_{i+1} = \bar{x}_i c_i$$

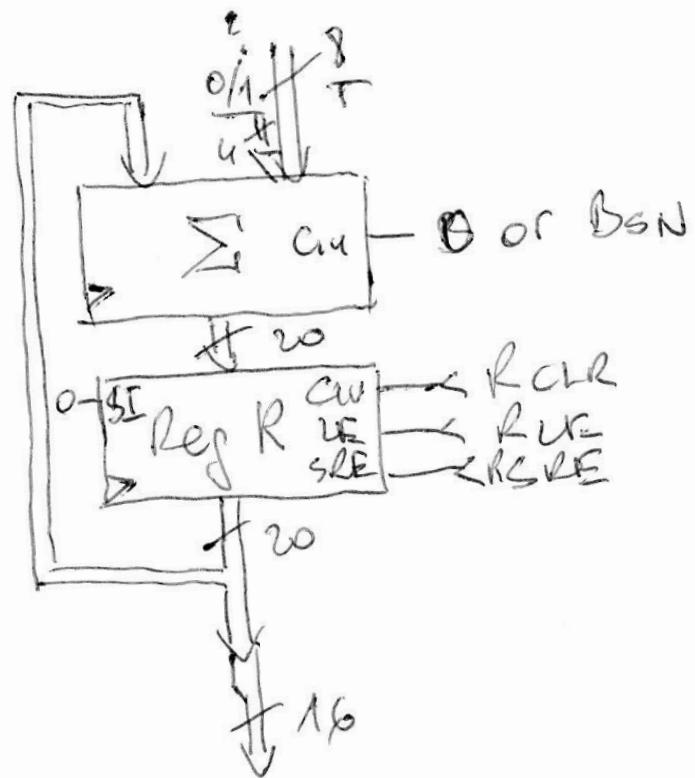
$$y_0 = x_i$$

$$c_0 = \bar{x}_i$$



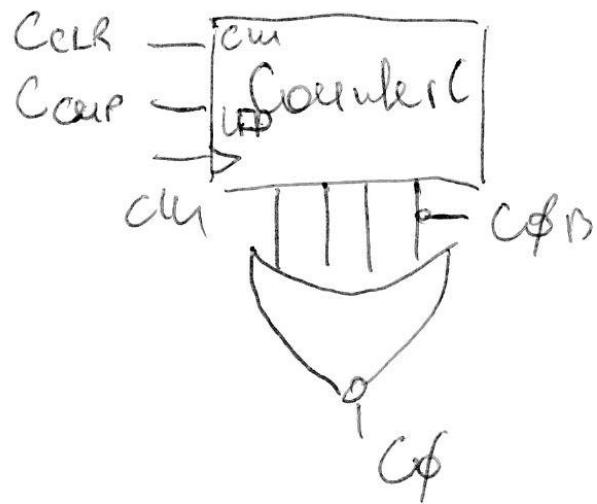


Multiplication Module

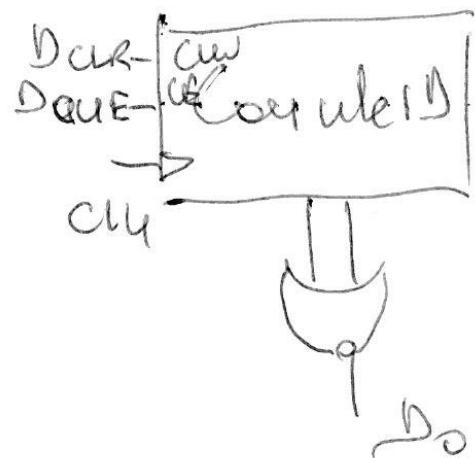


Counters

Numbers



Division





Fundamentals of Logic Circuit Design

Part V



HUMAN CAPITAL
HUMAN – BEST INVESTMENT!

EUROPEAN UNION
EUROPEAN
SOCIAL FUND



Examination Problem

Design a digital system computing:

$$n = 2^j, j < 8$$

$$y = INT \left[\sum_{i=1}^n x_{i-1}x_i / n \right]$$

The project should contain the following items:

- *sketch of the algorithm of operation of the data flow subsystem,*
- *data flow subsystem with necessary widths of buses marked,*
- *flowchart with marking of states of the Moore control automation,*
- control sequencer with initialization circuit,
- information about type of clock used with explanation,
- computation speed, accuracy & decent schematic view.

Please upload results in pdf.

The circuit first receives at the 8 bit bus A the number n then $x_0, x_1, x_2, \dots, x_n$ follows.

Computation speed and accuracy are critical factors.
Hardware optimization is less important but necessary.
Handshaking is implemented using following signals:

- Start = 1 (*start*) : signals beginning of a new data series
- Nrdy = 1 (*number ready*) : signals a new number on the input
- Rdy = 1 (*ready for next number*): requests the next number
- RR = 1 (*result ready*) : signals the readiness of the result



$$y = \text{Int} \left[\sum_{i=1}^n x_{i-1} x_i / n \right] \quad n = \frac{j}{2^{14}} \quad \textcircled{c}$$

Ver. 1

$$y = \text{Int} \left[[x_0 x_1 + x_1 x_2 + \dots + x_{n-1} x_n] / n \right]$$

Ver 2

$$y = \text{Int} \left[[x_1(x_0 + x_2) + x_3(x_2 + x_4) + \dots + x_{n-1}(x_{n-2} + x_n)] / n \right]$$

Cost

Ver 1 - n times multiplication

Ver 2 - $n/2$ times multiplication

R - for result Adder

B - for x_i

C - for x_{i-1}

A - for x_i

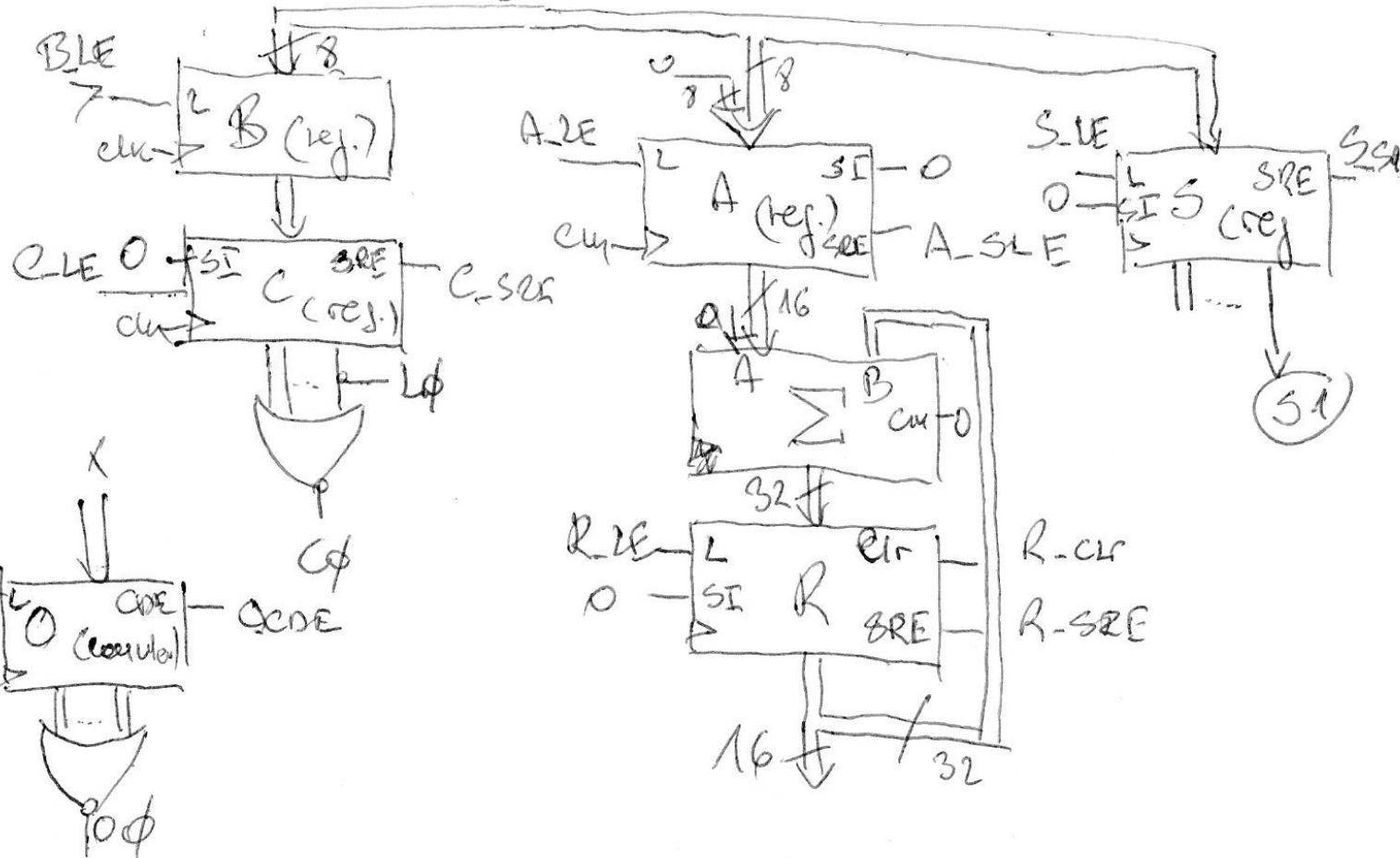
Memory

Ver. 1

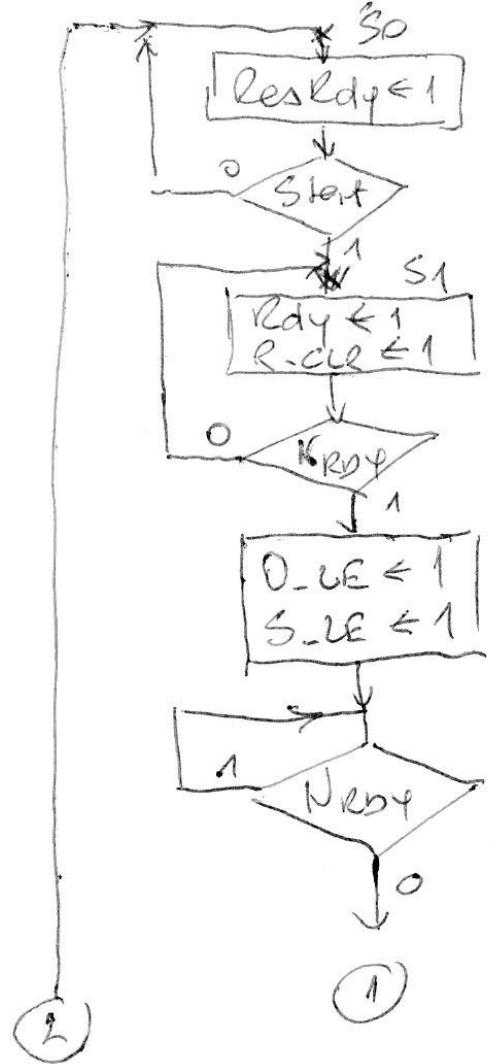
Data path Unit

8

1



Flowchart 1

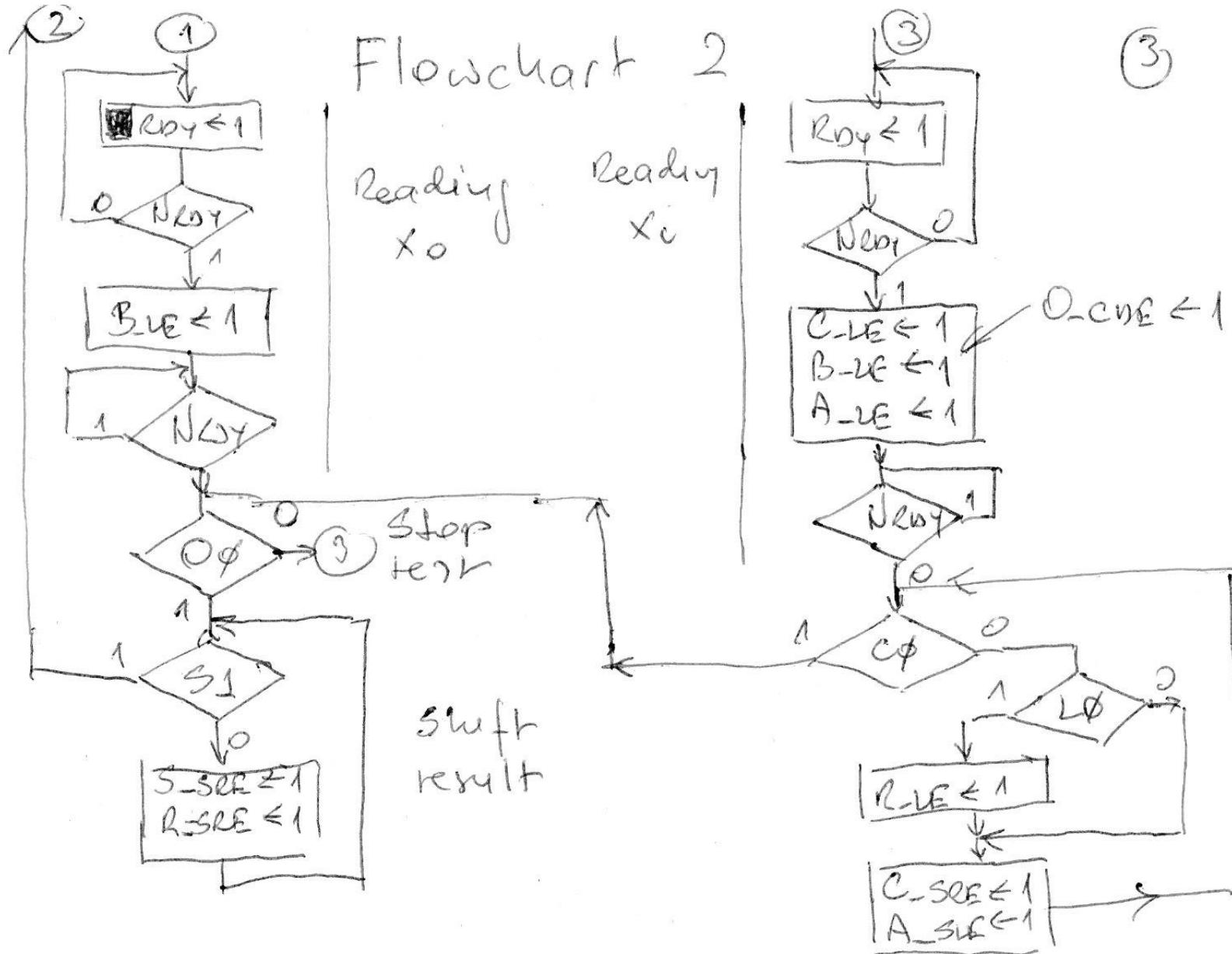


1

2

Reading
n

①



Warning

I consciously introduce examples of common errors on the slides to discuss them during the lecture.

The exam is divided into 5 separate parts. After completing each of them, a solution should be submitted.

Assessment

The basic criterion considered at each stage of assessment is the functioning of the system. If the system works as intended and key aspects are not violated maximum rating is issued, otherwise 0 is issued for the entire exam. Minor errors are acceptable provided that the student encloses the correct description of the system's operation and discusses the role of functional blocks.

The key aspects are:

- The I / O markings of subsystems must match.
- Handshaking must be valid when loading input data.
- The presentation of the result should last long enough.

Examination Problem

Design a digital system computing:

$$n > 0$$

$$y = INT \left[\sum_{i=1}^{2^n} x_i^2 / 2^n \right]$$

The project should contain the following items:

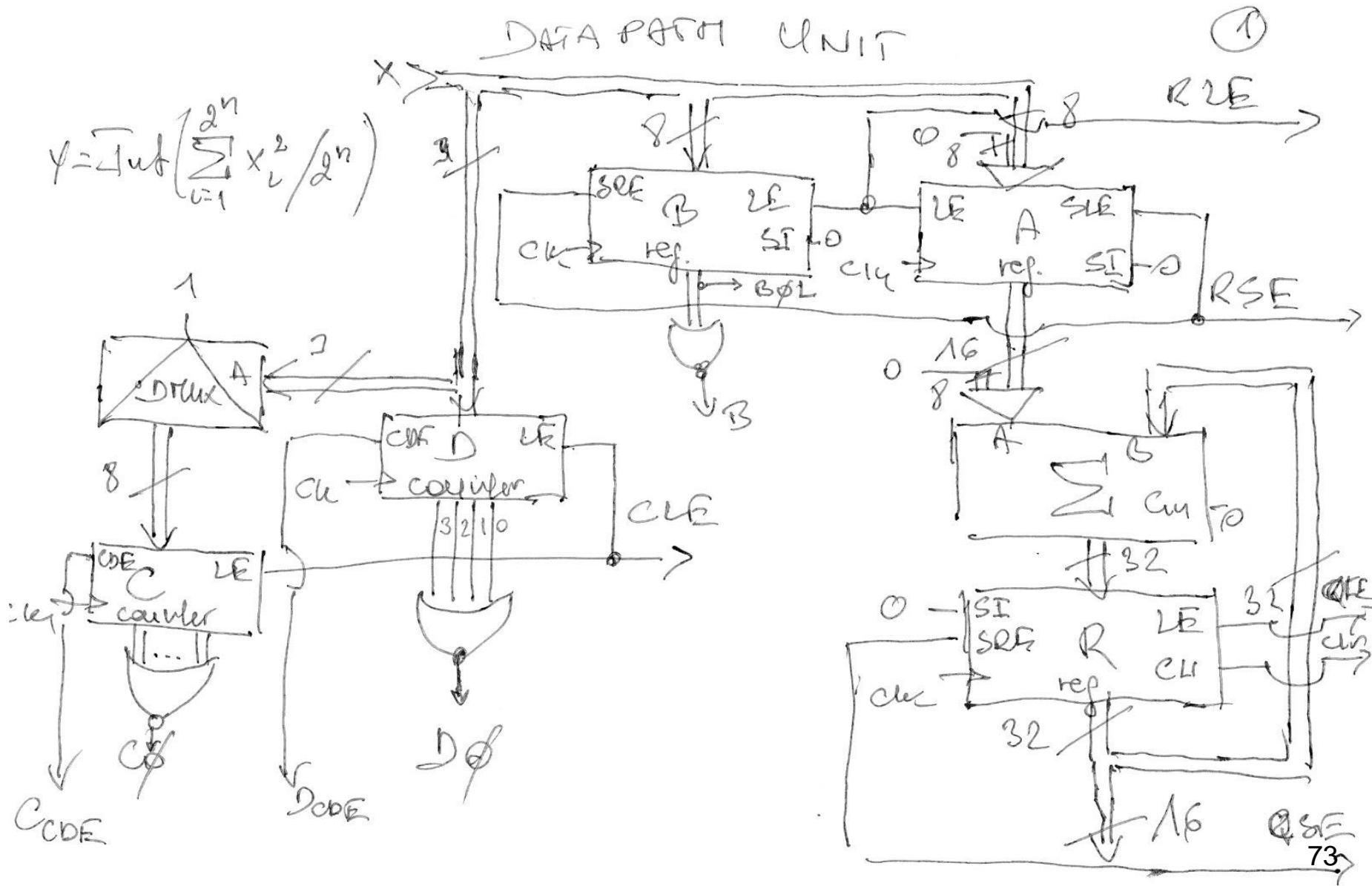
- *sketch of the algorithm of operation of the data flow subsystem,*
- *data flow subsystem with necessary widths of buses marked,*
- *flowchart with marking of states of the Moore control automation,*
- control sequencer with initialization circuit,
- information about type of clock used with explanation,
- computation speed, accuracy & decent schematic view.

Please upload results in pdf.

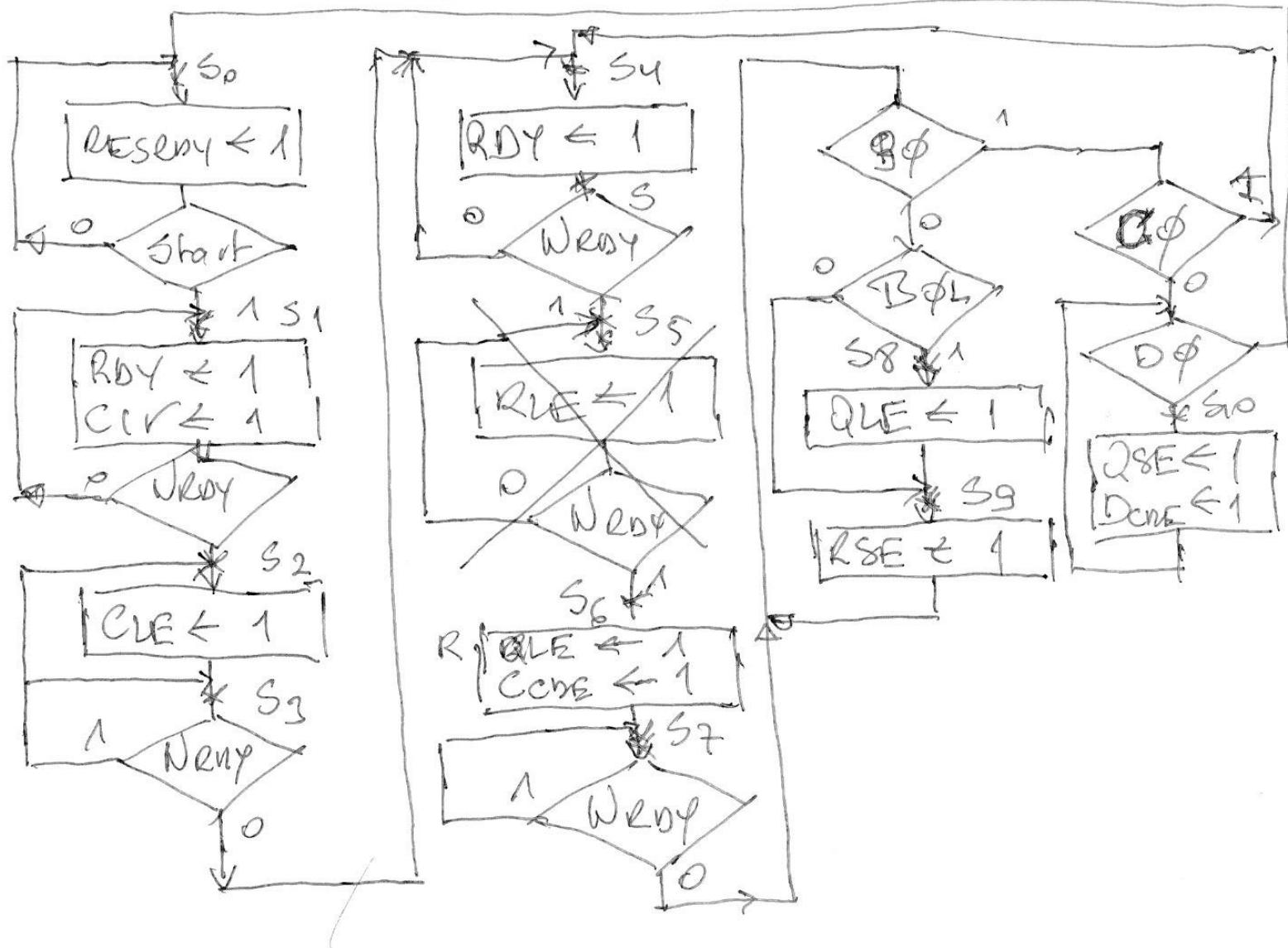
The circuit first receives at the 8 bit bus A the number n then $x_0, x_1, x_2, \dots, x_n$ follows.

Computation speed and accuracy are critical factors.
Hardware optimization is less important but necessary.
Handshaking is implemented using following signals:

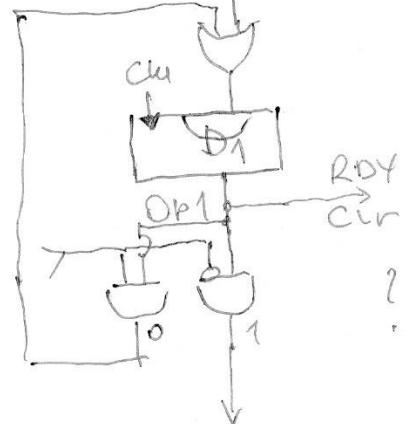
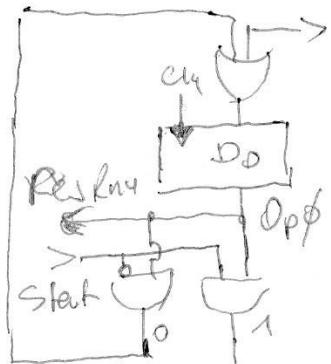
- Start = 1 (*start*) : signals beginning of a new data series
- Nrdy = 1 (*number ready*) : signals a new number on the input
- Rdy = 1 (*ready for next number*): requests the next number
- RR = 1 (*result ready*) : signals the readiness of the result



Flow Chart.



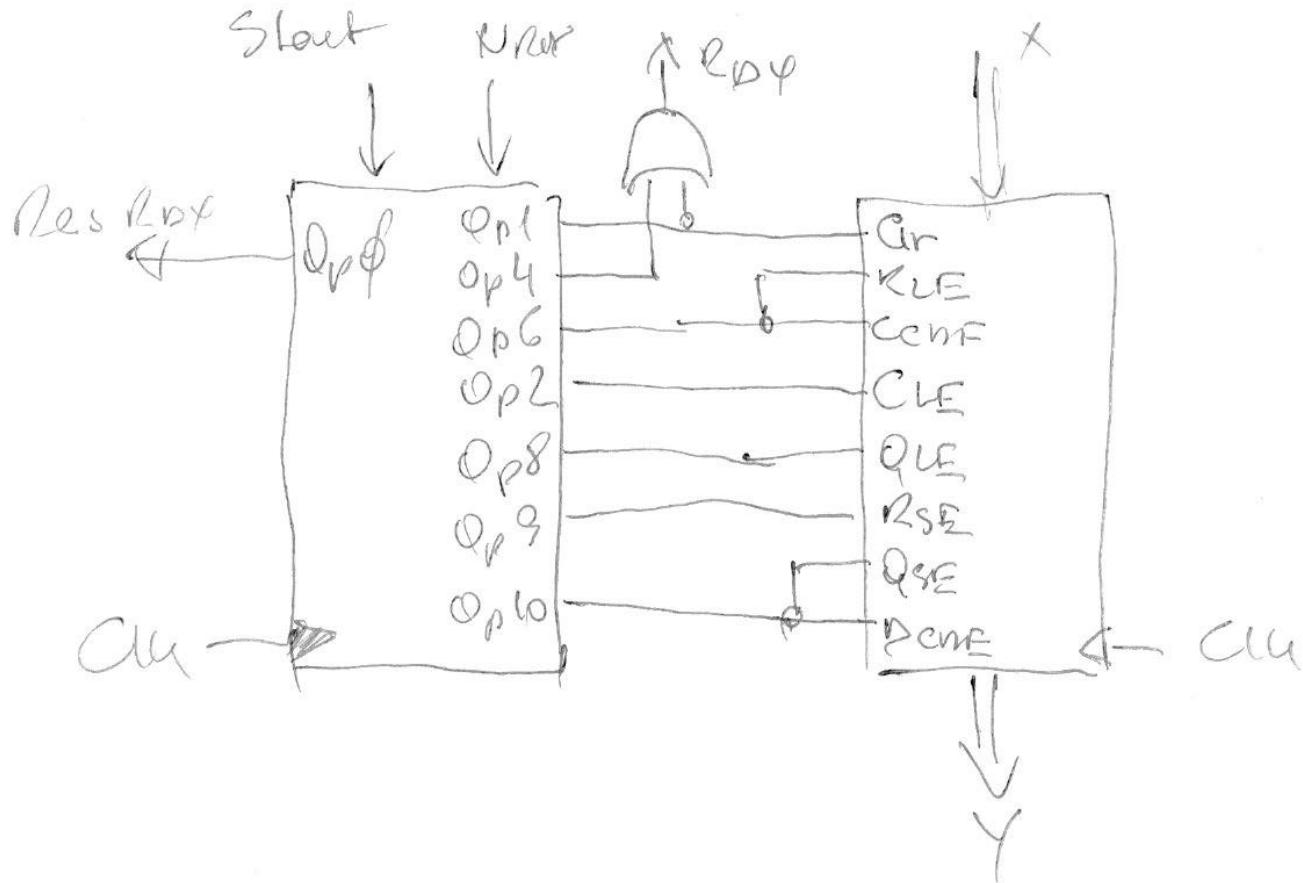
SEQUENCER



?

Manu Schematic

③



Rules applicable during on-line exam

1. During the test, you should have the camera turned on, directed at the desk, tabletop. The camera must cover the mouse and part of the student's silhouette. It doesn't have to cover the face.
2. It is forbidden to use the keyboard. Only use of blank sheets, a pen, a calculator, a personal computer with a monitor, camera, mouse and printer is allowed.
3. It is allowed to use self-made notes in paper form, printed lectures, as well as lectures in the form of a PDF file on your own computer.
4. It is forbidden to use the Internet for purposes other than:
 - a) solving the test on the server
 - b) downloading the solution of a calculation task from the server
 - c) sending the solution to the module.
5. The tutor can check the student's identity on a private connection
6. You must perform the test yourself. Any form of communication and collaboration with other students is forbidden.
7. Text and drawings can only be made by hand



Design the reversible two bit counter using JK flip-flops with asynchronous clear and load. The counter is counting modulo 4 up and down for $x = 0$ and for $x = 1$, respectively. Please prepare report including coded state transition table, excitation tables and formulas.

