WARSAW UNIVERSITY OF TECHNOLOGY
DEVELOPMENT PROGRAMME

Fundamentals of Logic Circuit Design

Part I: Combinatorial Logic

HUMAN CAPITAL
HUMAN – BEST INVESTMENT!

EUROPEAN UNION
EUROPEAN SOCIAL FUND

Project is co-financed by European Union within European Social Fund

A short guide on how to pass the course

- Plagiarism is unacceptable.
- The teacher assesses the work on the basis of observation of the design and implementation of the digital system.
- The key factor is the practical application of whole knowledge.
- You can exchange know-how with each other in the lab.

Definition:

Logic circuits are electronic circuits processing two-valued signals. Their operation is described by logic functions (Boolean algebra).

Notation

x – element (scalar or vector) of a set ($x \in \boldsymbol{X}$)

$\boldsymbol{X}$ – set of elements x ($x \in \boldsymbol{X}$)

x_i – ith component of the vector x ($x = [x_1, \ldots, x_i, \ldots, x_n]$)

x^j – jth element of set $\boldsymbol{X}$ ($x^j \in \boldsymbol{X}$)

$\boldsymbol{X}^k$ – kth subset of set $\boldsymbol{X}$ ($\boldsymbol{X}^k \subset \boldsymbol{X}$)

x^* – sequence of elements x (${}^1x\ {}^2x\ {}^3x \ldots$)

${}^mx$ – mth component of the sequence x^* (${}^1x\ {}^2x \ldots {}^mx \ldots$)

x^{*n} – nth subsequence of the sequence x^*

${}_Ax$ – element associated with automaton A

$\bumpeq$	—	non-contradictory	—	\bumpeq
$\equiv$	—	equivalent	—	\equiv
$\cong$	—	pseudoequivalent	—	\cong
$\approxeq$	—	compatible	—	\approxeq
$\approx$	—	Moore pseudocompatible	—	\approx
$\sim$	—	Mealy pseudocompatible	—	\sim

Suggested reading

1. D. M. Harris, S. L. Harris, *Digital Design and Computer Architecture,* Elsevier, 2013, (721 pages)
2. Wakerly J. F., *Digital Design: Principles and Practices*, Prentice Hall, Englewood Clis, 1994. (840 pages)
3. Zwoliński M.: *Digital System Design with VHDL.* Prentice Hall 2003. (368 pages)
4. Maxfield C.: *The Design Warrior's Guide to FPGAs*, Elsevier, 2004. (560 pages)

Boolean Algebra

- **Variables:** $X \quad \{ 0, 1 \}$
- **Operators:**
  - **not:** $\bar{x} \quad \{ \quad \bar{1} = 0 \, , \bar{0} = 1 \quad \}$
  - **and:** $\cdot \quad \{ \quad 0 \cdot 0 = 0, \; 0 \cdot 1 = 0, \; 1 \cdot 0 = 0, \; 1 \cdot 1 = 1 \quad \}$
  - **or:** $+ \quad \{ \quad 0 + 0 = 0, 0 + 1 = 1, 1 + 0 = 1, 1 + 1 = 1 \quad \}$

Identities for Variable x

- $x \cdot 0 = 0$
- $x \cdot 1 = x$
- $x \cdot x = x$
- $x \cdot \bar{x} = 0$
- $x + 0 = x$
- $x + 1 = 1$
- $x + x = x$
- $x + \bar{x} = 1$
- $\bar{\bar{x}} = x$
- $\bar{\bar{x}} = x$

- **Commutative Law**

$$x \cdot y = y \cdot x \qquad\qquad x + y = y + x$$

- **Distributive Law**

$$x \cdot (y + z) = (x \cdot y) + (x \cdot z)$$

$$x + (y \cdot z) = (x + y) \cdot (x + z)$$

- **Absorptive Law**

$$x \cdot (y + x) = x$$

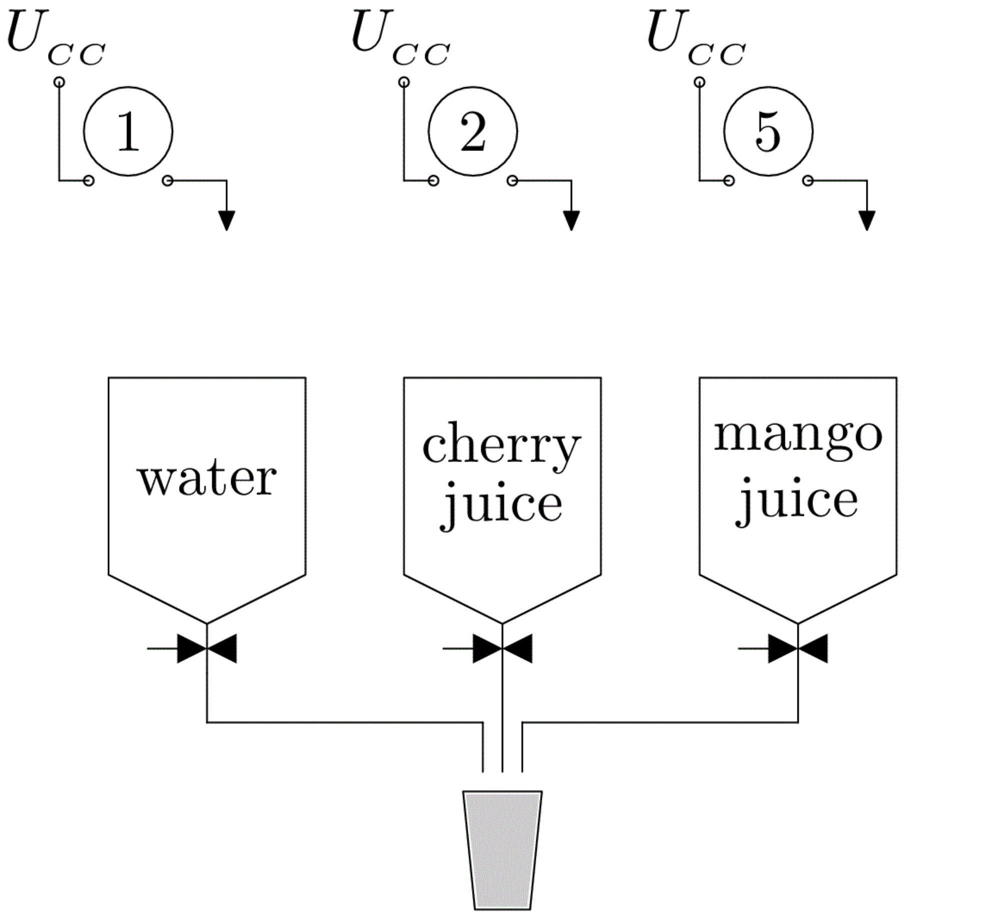
$$x + (y \cdot x) = x$$

Drink dispenser

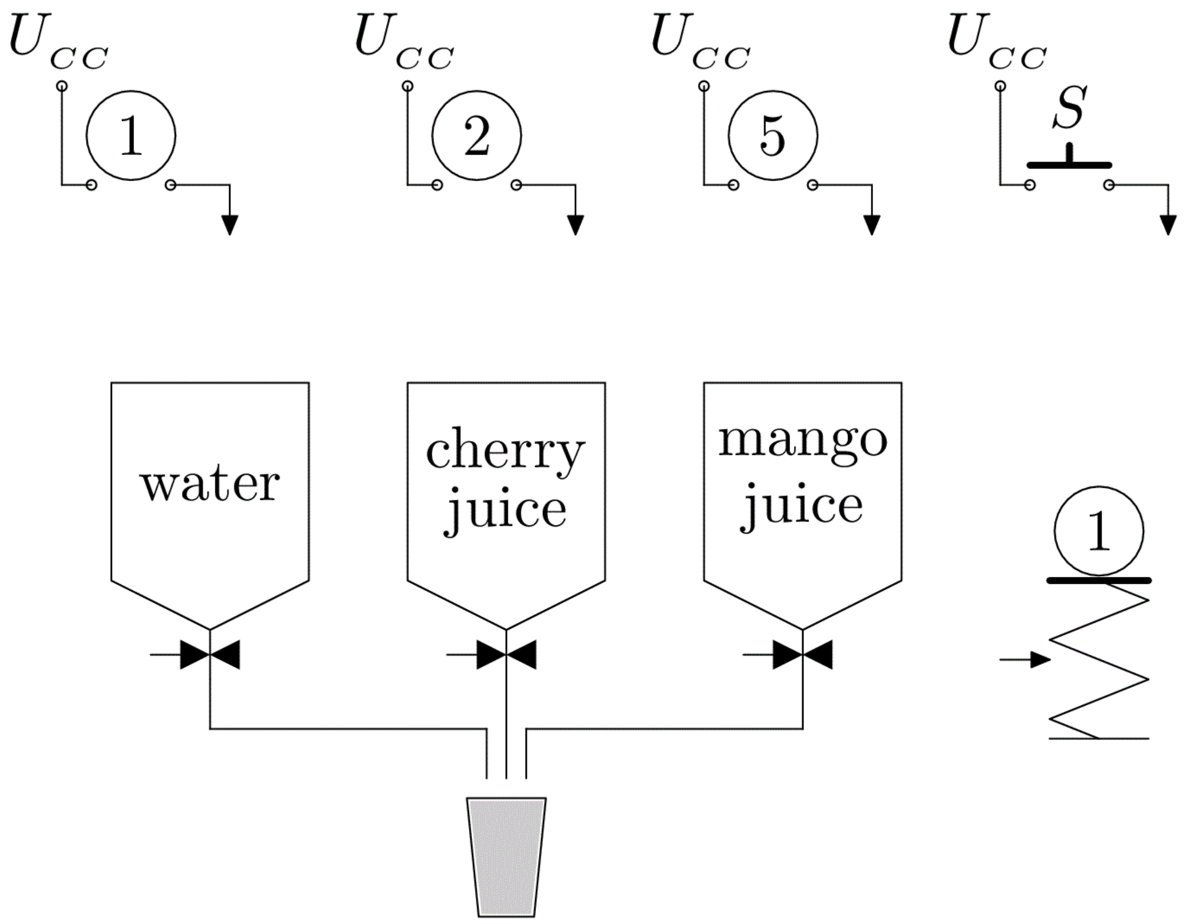
drink	→	price
water	→	5
water + cherry juice	→	7
water + mango juice	→	8

coin	→	name
1	→	one
2	→	two
5	→	five

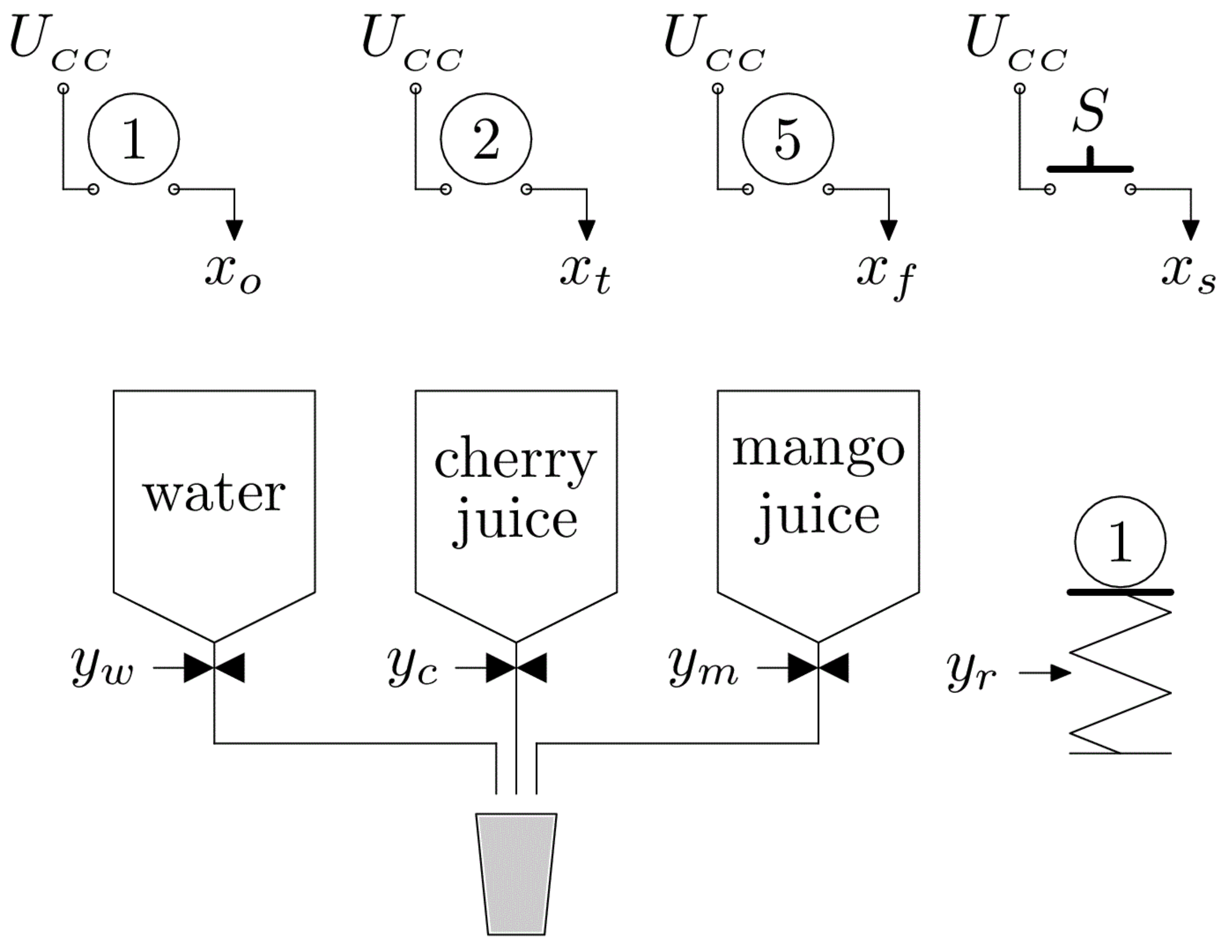
Drink dispenser - initial structure



Drink dispenser - final structure



Drink dispenser - input/output signals

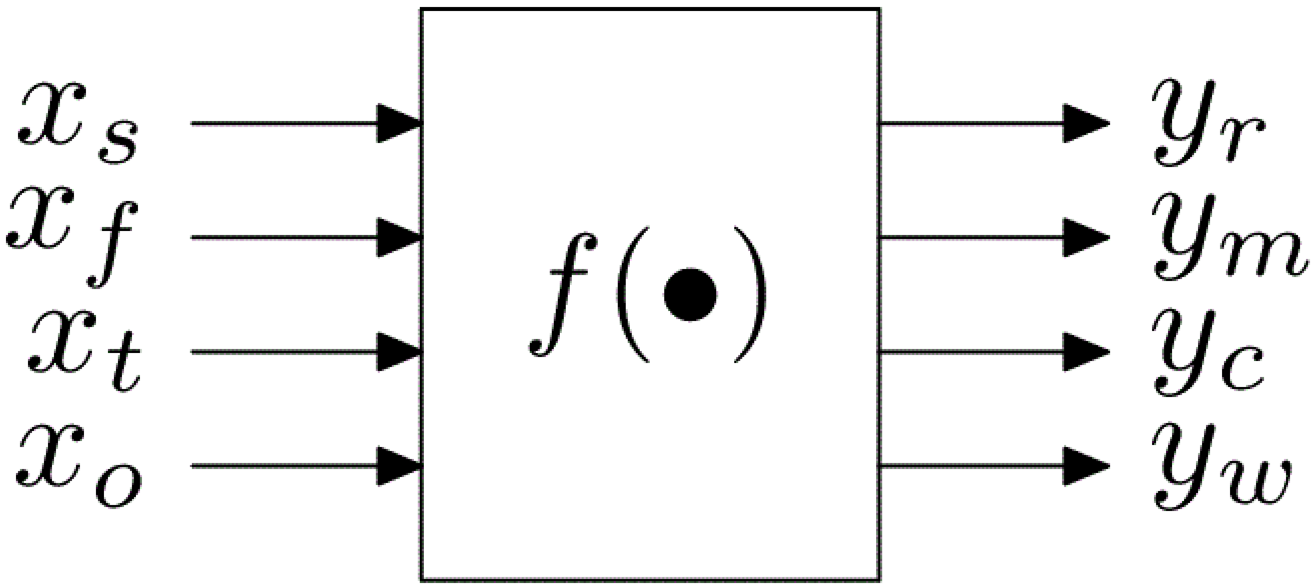


cause	$\longrightarrow$	signal
1	$\longrightarrow$	x_o
2	$\longrightarrow$	x_t
5	$\longrightarrow$	x_f
S	$\longrightarrow$	x_s

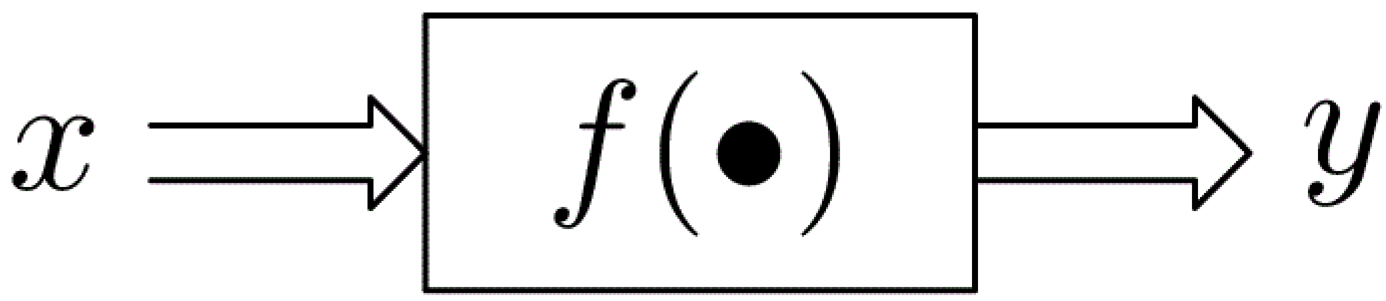
input	$\rightarrow$	action
only coins	$\rightarrow$	do nothing
S	$\rightarrow$	do nothing
$1+S$	$\rightarrow$	return coin
$2+S$	$\rightarrow$	return coin
$1+2+S$	$\rightarrow$	return coins
$5+S$	$\rightarrow$	open water valve
$5+1+S$	$\rightarrow$	return coins
$5+2+S$	$\rightarrow$	open water and cherry juice valves
$5+2+1+S$	$\rightarrow$	open water and mango juice valves

input	→	action	→	output
only coins	→	do nothing	→	—
S	→	do nothing	→	—
$1+S$	→	return coin	→	y_r
$2+S$	→	return coin	→	y_r
$1+2+S$	→	return coins	→	y_r
$5+S$	→	open water valve	→	y_w
$5+1+S$	→	return coins	→	y_r
$5+2+S$	→	open water and cherry juice valves	→	y_w+y_c
$5+2+1+S$	→	open water and mango juice valves	→	y_w+y_m

Structure of the drink dispenser control system



Compact form structure



$$x = [x_s, x_f, x_t, x_o]$$

$$y = [y_w, y_c, y_m, y_r]$$

$$y = f(x)$$

$$\begin{cases} y_w &= f_w(x_s, x_f, x_t, x_o) \\ y_c &= f_c(x_s, x_f, x_t, x_o) \\ y_m &= f_m(x_s, x_f, x_t, x_o) \\ y_r &= f_r(x_s, x_f, x_t, x_o) \end{cases}$$

Input-output relationship

	x_s	x_f	x_t	x_o	y_w	y_c	y_m	y_r
0	0	0	0	0	0	0	0	0
1	0	0	0	1	0	0	0	0
2	0	0	1	0	0	0	0	0
3	0	0	1	1	0	0	0	0
4	0	1	0	0	0	0	0	0
5	0	1	0	1	0	0	0	0
6	0	1	1	0	0	0	0	0
7	0	1	1	1	0	0	0	0

	x_s	x_f	x_t	x_o	y_w	y_c	y_m	y_r
8	1	0	0	0	0	0	0	0
9	1	0	0	1	0	0	0	1
10	1	0	1	0	0	0	0	1
11	1	0	1	1	0	0	0	1
12	1	1	0	0	1	0	0	0
13	1	1	0	1	0	0	0	1
14	1	1	1	0	1	1	0	0
15	1	1	1	1	1	0	1	0

$$y_m = 1 \text{ iff } \begin{array}{cccc} x_s & x_f & x_t & x_o \\ 1 & 1 & 1 & 1 \end{array}$$

$$y_c = 1 \text{ iff } \begin{array}{cccc} x_s & x_f & x_t & x_o \\ 1 & 1 & 1 & 0 \end{array}$$

$$\Rightarrow \begin{aligned} y_m &= x_s \bigwedge x_f \bigwedge x_t \bigwedge x_o \\ y_m &= x_s x_f x_t x_o \end{aligned}$$

$$\Rightarrow y_c = x_s x_f x_t \overline{x}_o$$

$$y_w = 1 \text{ iff } \begin{array}{cccc} x_s & x_f & x_t & x_o \\ 1 & 1 & 1 & 1 \end{array} \text{ or } \begin{array}{cccc} x_s & x_f & x_t & x_o \\ 1 & 1 & 1 & 0 \end{array} \text{ or } \begin{array}{cccc} x_s & x_f & x_t & x_o \\ 1 & 1 & 0 & 0 \end{array}$$

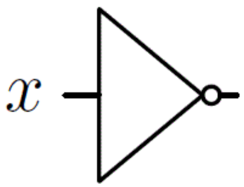
$$\Rightarrow \begin{aligned} y_w &= x_s x_f x_t x_o \ \bigvee \ x_s x_f x_t \overline{x}_o \ \bigvee \ x_s x_f \overline{x}_t \overline{x}_o \\ y_w &= x_s x_f x_t x_o + x_s x_f x_t \overline{x}_o + x_s x_f \overline{x}_t \overline{x}_o \end{aligned}$$

$$y_r = 1 \text{ iff } \begin{array}{cccc} x_s & x_f & x_t & x_o \\ 1 & 0 & 0 & 1 \end{array} \text{ or } \begin{array}{cccc} x_s & x_f & x_t & x_o \\ 1 & 0 & 1 & 0 \end{array} \text{ or }$$

$$\begin{array}{cccc} x_s & x_f & x_t & x_o \\ 1 & 0 & 1 & 1 \end{array} \text{ or } \begin{array}{cccc} x_s & x_f & x_t & x_o \\ 1 & 1 & 0 & 1 \end{array}$$

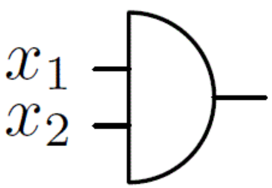
$$\Rightarrow \; y_r \; = \; x_s\overline{x}_f\overline{x}_t x_o + x_s\overline{x}_f x_t\overline{x}_o + x_s\overline{x}_f x_t x_o + x_s x_f\overline{x}_t x_o$$

Basic gates



$$y = \overline{x} = NOT(x)$$

x	y
0	1
1	0

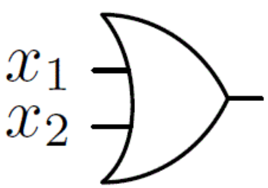


$$y = x_1 x_2 = AND(x_1, x_2)$$

$x_1 \backslash x_2$	0	1
0	0	0
1	0	1

y

Basic gates …

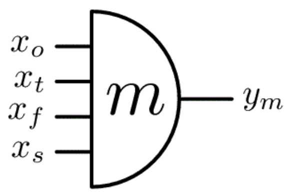


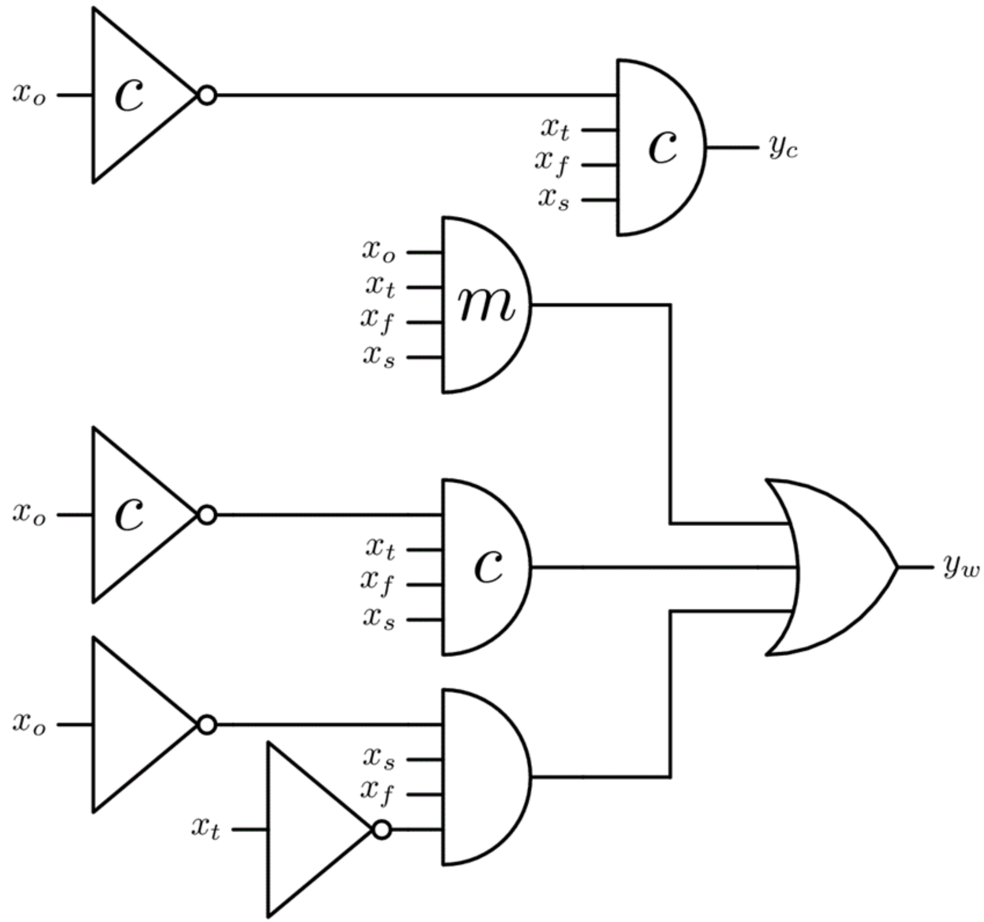
$$y = x_1 + x_2 = OR(x_1, x_2)$$

$x_1 \backslash x_2$	0	1
0	0	1
1	1	1

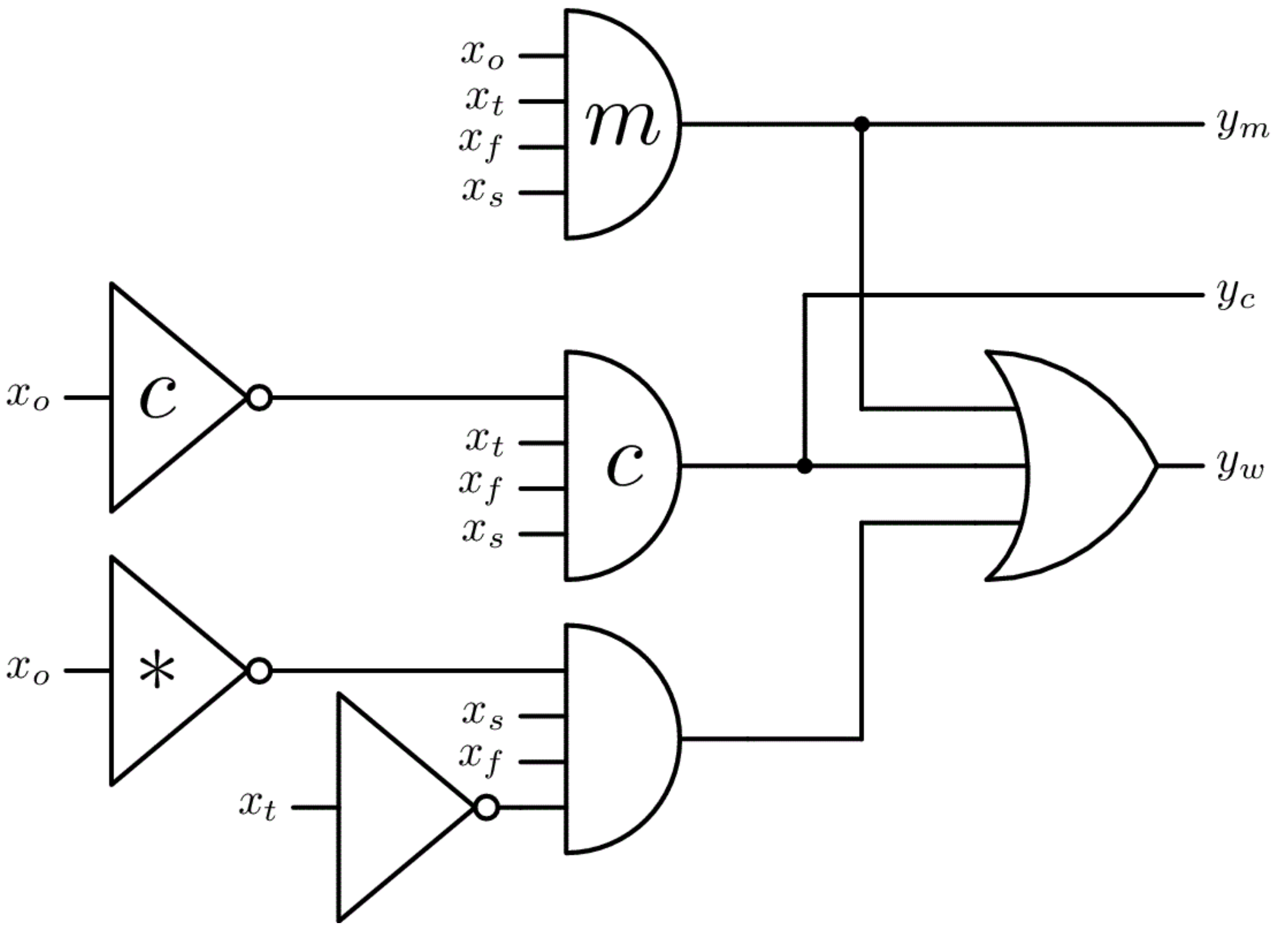
y

Partial circuit diagram of the drink dispenser control system

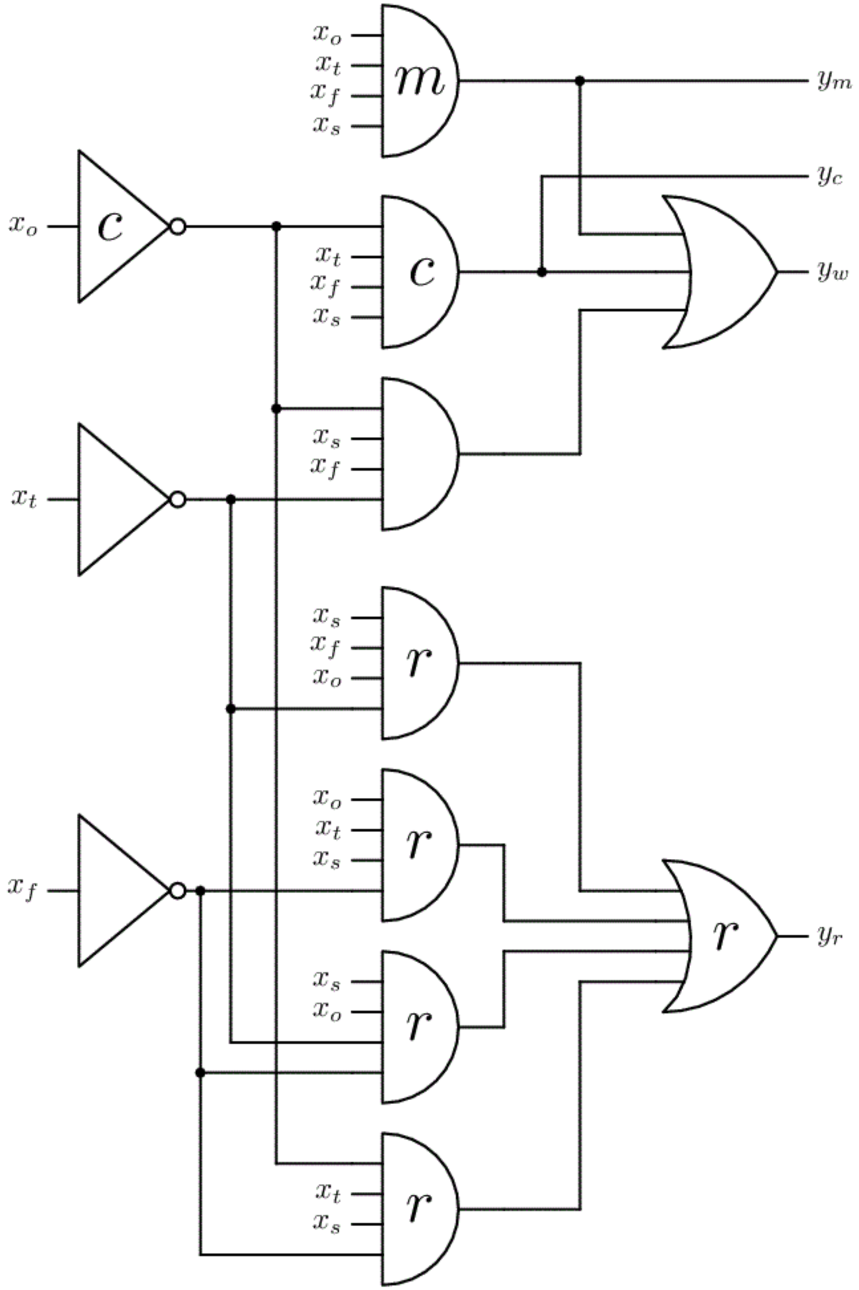




Improved partial circuit diagram of the drink dispenser control system



Full circuit diagram



Modication of y_r part of the circuit

$$y_r = x_s\overline{x}_f\overline{x}_t x_o + x_s x_f \overline{x}_t x_o + x_s\overline{x}_f x_t \overline{x}_o + x_s\overline{x}_f x_t x_o$$

$$y_r = x_s[\overline{x}_f\overline{x}_t x_o + x_f \overline{x}_t x_o + \overline{x}_f x_t \overline{x}_o + \overline{x}_f x_t x_o]$$

$$y_r = x_s[(\overline{x}_f + x_f)\overline{x}_t x_o + \overline{x}_f x_t(\overline{x}_o + x_o)]$$

$$y_r = x_s[(1)\overline{x}_t x_o + \overline{x}_f x_t(1)]$$

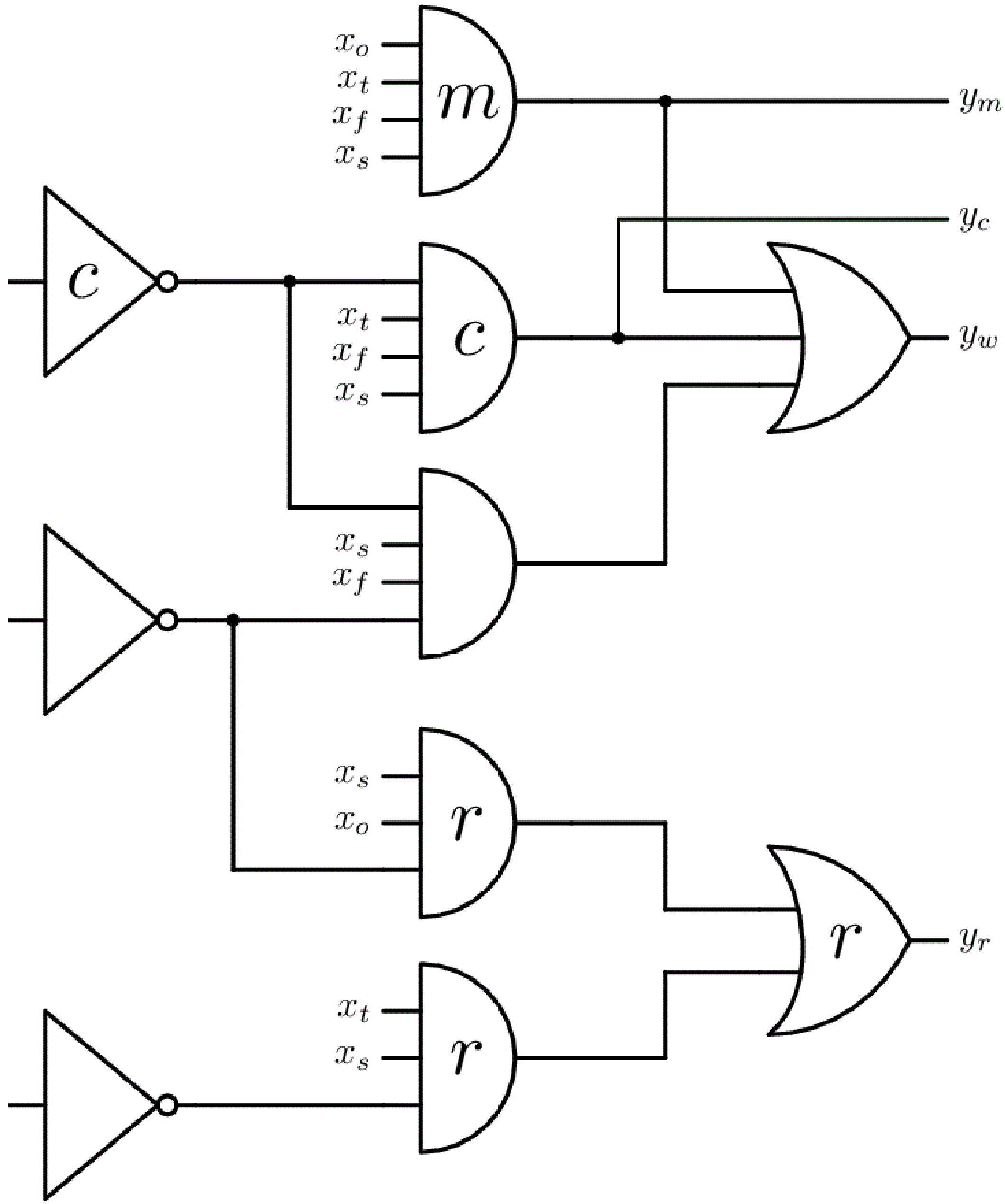
$$y_r = x_s[\overline{x}_t x_o + \overline{x}_f x_t]$$

$$y_r = x_s\overline{x}_t x_o + x_s\overline{x}_f x_t$$

Conclusion:

Algebraic manipulation of expressions can lead to the reduction of the circuit size

Final full circuit diagram

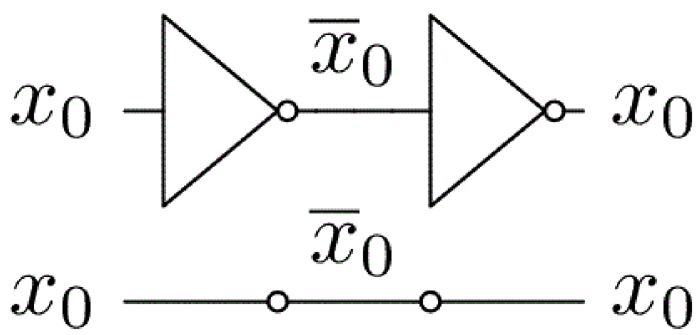


Cost assessment

Gate type	Initial cost	Final cost
NOT	3	3
AND4	7	3
AND3	—	2
OR4	1	—
OR3	1	1
OR2	—	1
gates:	12	10
inputs:	38	26
types of gates:	3	3

- multitude of diverse gates

Afirmation out of double complementation

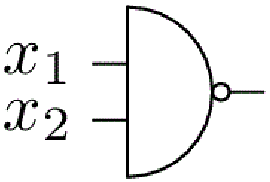


de Morgan's laws:

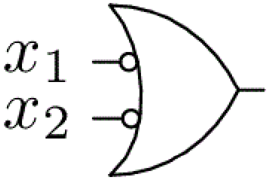
$$\overline{x}_1 + \overline{x}_2 = \overline{x_1 x_2}$$

$$\overline{x}_1 \overline{x}_2 = \overline{x_1 + x_2}$$

NAND gates



$y = \overline{x_1 x_2} = NAND(x_1, x_2)$

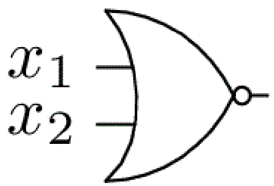


$y = \overline{x}_1 + \overline{x}_2 = NAND(x_1, x_2)$

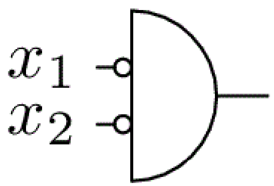
$x_1 \backslash x_2$	0	1
0	1	1
1	1	0

y

NOR gates



$$y = \overline{x_1 + x_2} = NOR(x_1, x_2)$$

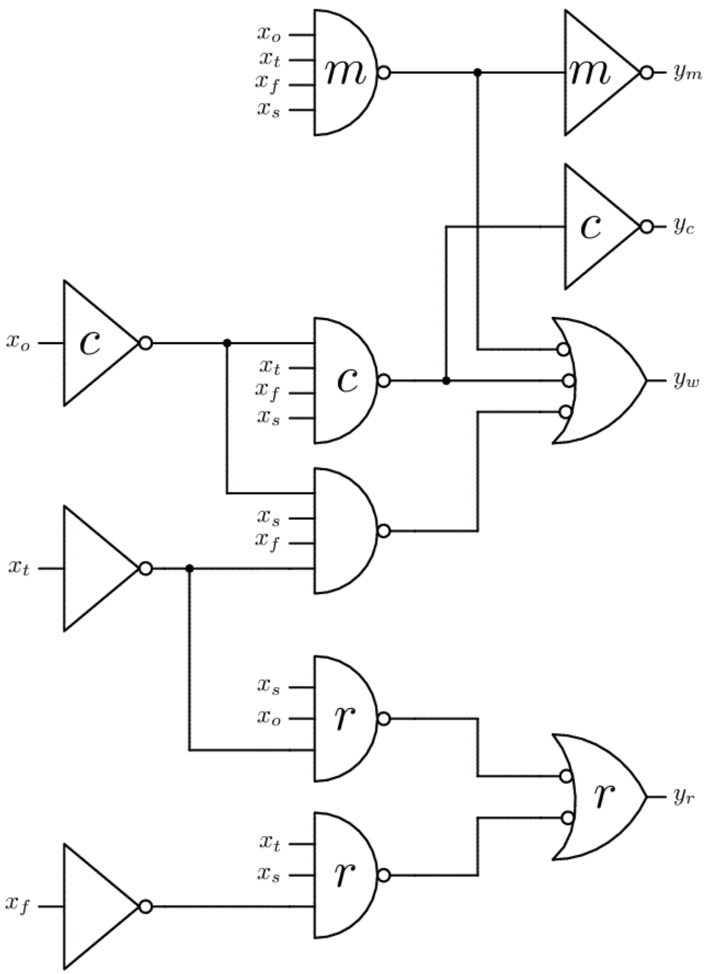


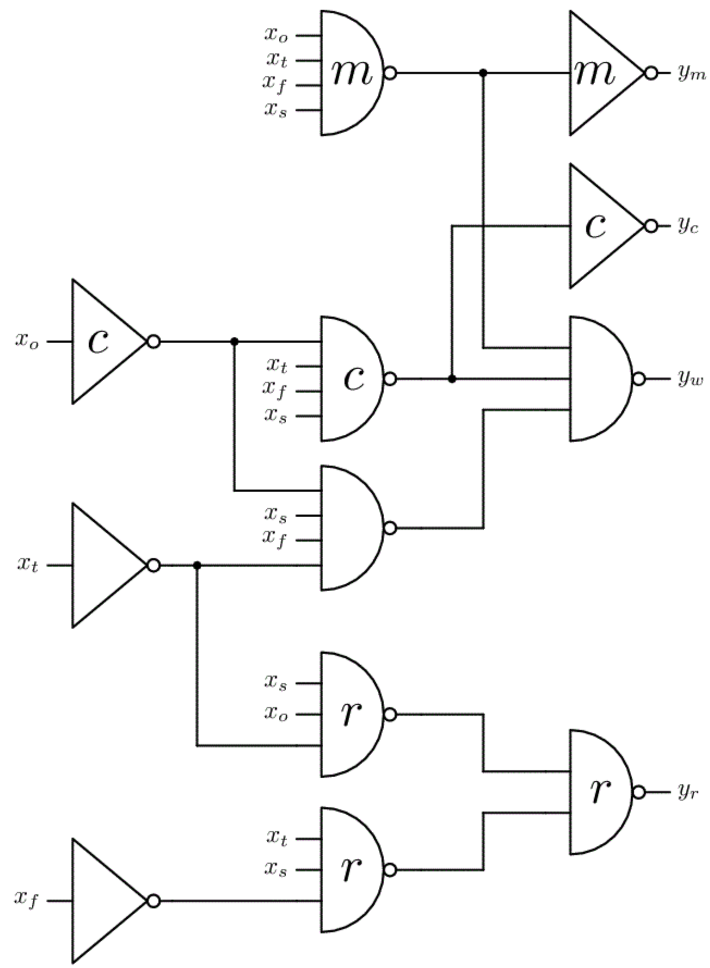
$$y = \overline{x}_1\overline{x}_2 = NOR(x_1, x_2)$$

x_1 \ x_2	0	1
0	1	0
1	0	0

y

Transformed final full circuit diagram

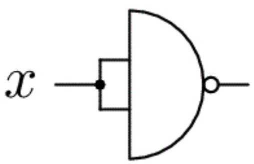




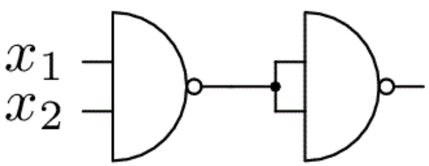
Final cost assessment

Gate type	Initial cost	Final cost diverse gates	Final cost NAND gates
NOT	3	3	5
NAND4	–	–	3
NAND3	–	–	3
NAND2	–	–	1
AND4	7	3	–
AND3	–	2	–
OR4	1	–	–
OR3	1	1	–
OR2	–	1	–
gates:	12	10	12
inputs:	38	26	28
types of gates:	3	3	2/1
integrated circuits	6	5	5
spare gates	4 (3NOT)	6 (3NOT)	5 (1NOT)

NOT and AND produced out of NAND gates

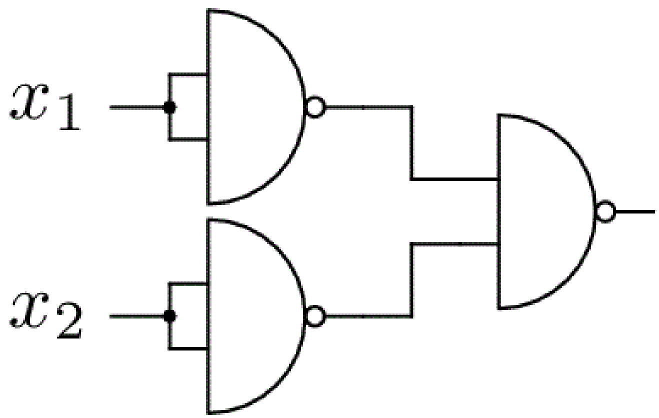


$$y = NAND(x, x) = NOT(AND(x, x)) = NOT(x)$$

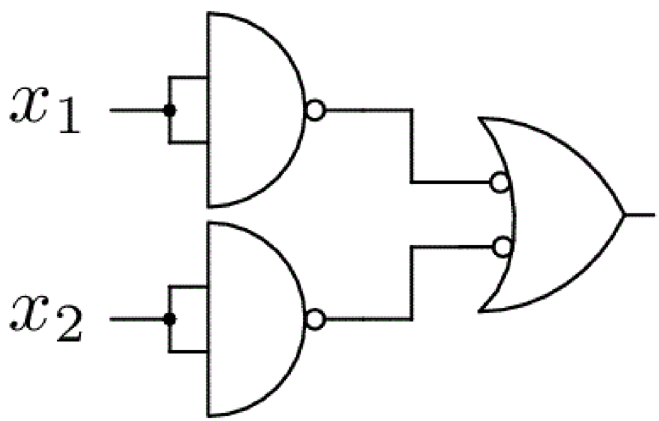


$$\begin{aligned} y &= NOT(NAND(x_1, x_2)) \\ &= NOT(NOT(AND(x_1, x_2))) \\ &= AND(x_1, x_2) \end{aligned}$$

OR gates produced out of NAND gates

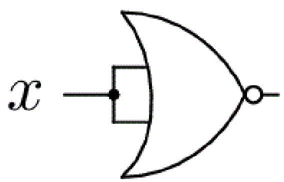


$$y = NAND(\overline{x}_1, \overline{x}_2) = \overline{\overline{x}_1 \overline{x}_2}$$
$$= \overline{\overline{x_1 + x_2}} = x_1 + x_2$$

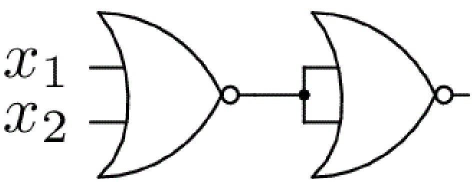


$$y = \overline{\overline{x}}_1 + \overline{\overline{x}}_2 = x_1 + x_2$$

NOT and OR gates produced out of NOR gates

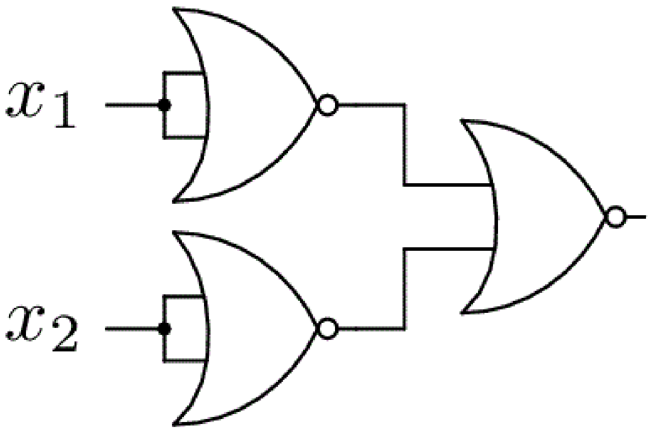


$$y = NOR(x, x) = NOT(OR(x, x)) = NOT(x)$$

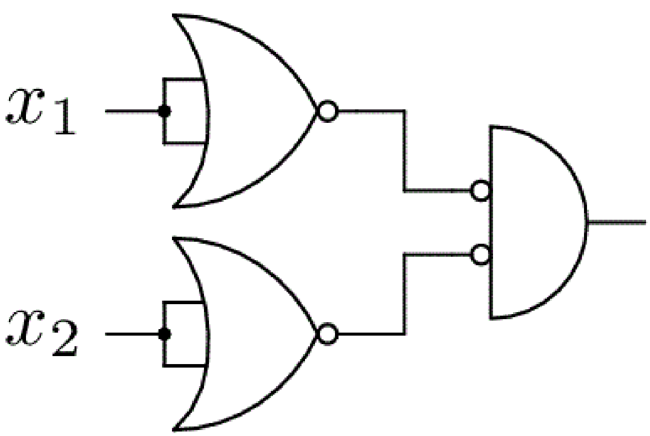


$$\begin{aligned} y &= NOT(NOR(x_1, x_2)) \\ &= NOT(NOT(OR(x_1, x_2))) \\ &= OR(x_1, x_2) \end{aligned}$$

AND gates produced out of NOR gates



$$y = NOR(\overline{x}_1, \overline{x}_2) = \overline{\overline{x}_1 + \overline{x}_2}$$
$$= \overline{\overline{x_1 x_2}} = x_1 x_2$$



$$y = \overline{\overline{x}}_1 \overline{\overline{x}}_2 = x_1 x_2$$

Logic function specification

$$y_r = 1 \text{ iff } \begin{array}{cccc} x_s & x_f & x_t & x_o \\ 1 & 0 & 0 & 1 \end{array} \text{ or } \begin{array}{cccc} x_s & x_f & x_t & x_o \\ 1 & 0 & 1 & 0 \end{array} \text{ or}$$

$$\begin{array}{cccc} x_s & x_f & x_t & x_o \\ 1 & 0 & 1 & 1 \end{array} \text{ or } \begin{array}{cccc} x_s & x_f & x_t & x_o \\ 1 & 1 & 0 & 1 \end{array}$$

SOP - Sum of Products form

$$y_r = x_s\overline{x}_f\overline{x}_t x_o + x_s\overline{x}_f x_t\overline{x}_o + x_s\overline{x}_f x_t x_o + x_s x_f\overline{x}_t x_o$$

$$F^1_{y_r} = \{\ \underbrace{1001_2}_{9_{10}},\ \ \underbrace{1010_2}_{10_{10}},\ \ \underbrace{1011_2}_{11_{10}},\ \ \underbrace{1101_2}_{13_{10}}\ \}$$

$$F^1_{y_r} = \{\ 9,\ \ 10,\ \ 11,\ \ 13\ \}$$

$$y_r = \sum\Big(\ 9,\ 10,\ 11,\ 13\ \Big)$$

Logic function minimization

$$y_r = \underbrace{x_s\overline{x}_f\overline{x}_t x_o + x_s x_f \overline{x}_t x_o}_{y_r^1} + \underbrace{x_s\overline{x}_f x_t \overline{x}_o + x_s\overline{x}_f x_t x_o}_{y_r^2}$$

$$y_r^1 = \underbrace{\underbrace{x_s\ \overline{x}_f\ \overline{x}_t\ x_o}_{1\,0\,0\,1} + \underbrace{x_s\ x_f\ \overline{x}_t\ x_o}_{1\,1\,0\,1}}_{1\,-\,0\,1}$$

$$y_r^1 = x_s\ \overline{x}_t\ x_o\ (\overline{x}_f + x_f)$$

$$y_r^1 = x_s\ \overline{x}_t\ x_o\ (1)$$

$$y_r^1 = \underbrace{x_s\ \overline{x}_t\ x_o}_{1\,-\,0\,1}$$

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Gray's code

1 bit	2 bit	3 bit	4 bit
0	00	000	0000
1	01	001	0001
	11	011	0011
	10	010	0010
		110	0110
		111	0111
		101	0101
		100	0100
			1100
			1101
			1111
			1110
			1010
			1011
			1001
			1000

Karnaugh tables

$x_1x_2 \backslash x_3$	0	1
00	0	1
01	2	3
11	6	7
10	4	5

$x_1x_2x_3$

$x_1x_2 \backslash x_3x_4$	00	01	11	10
00	0	1	3	2
01	4	5	7	6
11	12	13	15	14
10	8	9	11	10

$x_1x_2x_3x_4$

Karnaugh tables (cntd)

$x_1x_2 \backslash x_3x_4x_5$	000	001	011	010	110	111	101	100
00	0	1	3	2	6	7	5	4
01	8	9	11	10	14	15	13	12
11	24	25	27	26	30	31	29	28
10	16	17	19	18	22	23	21	20

$x_1x_2x_3x_4x_5$

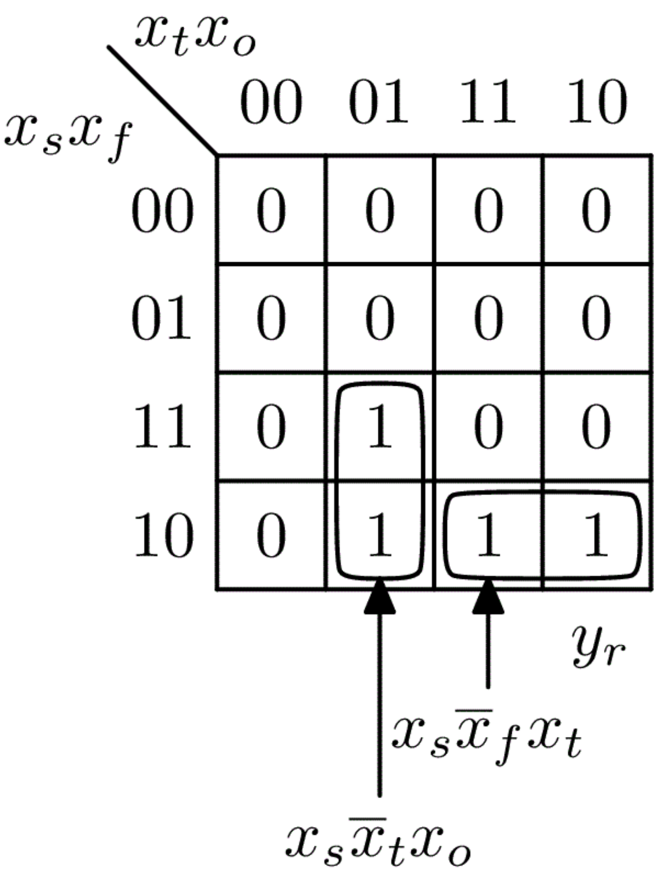
Karnaugh tables (cntd)

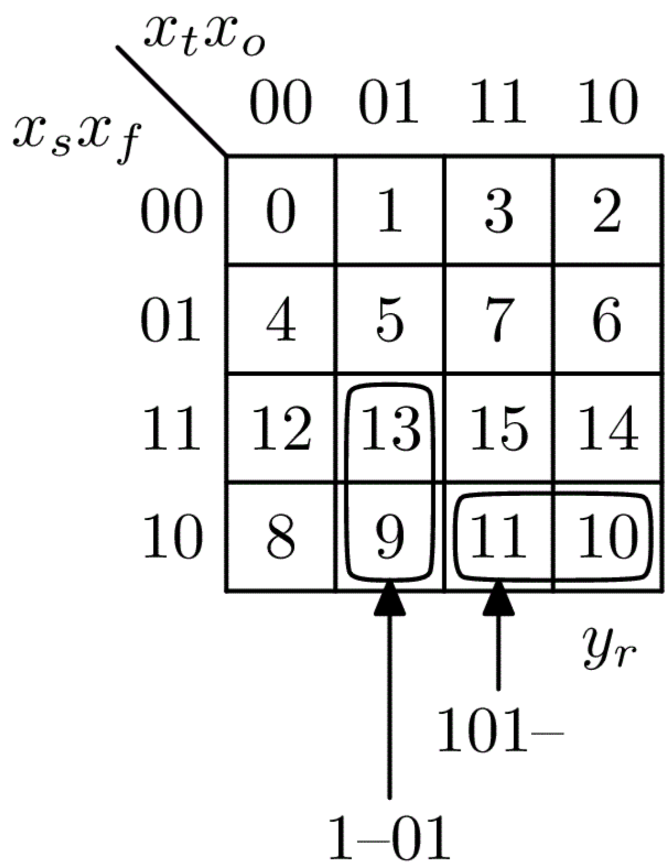
$x_1x_2x_3$ \ $x_4x_5x_6$	000	001	011	010	110	111	101	100
000	0	1	3	2	6	7	5	4
001	8	9	11	10	14	15	13	12
011	24	25	27	26	30	31	29	28
010	16	17	19	18	22	23	21	20
110	48	49	51	50	54	55	53	52
111	56	57	59	58	62	63	61	60
101	40	41	43	42	46	47	45	44
100	32	33	35	34	38	39	37	36

$x_1x_2x_3x_4x_5x_6$

Logic function minimization

$$Y_r = \sum(\,9;\ 10;\ 11;\ 13\,)$$

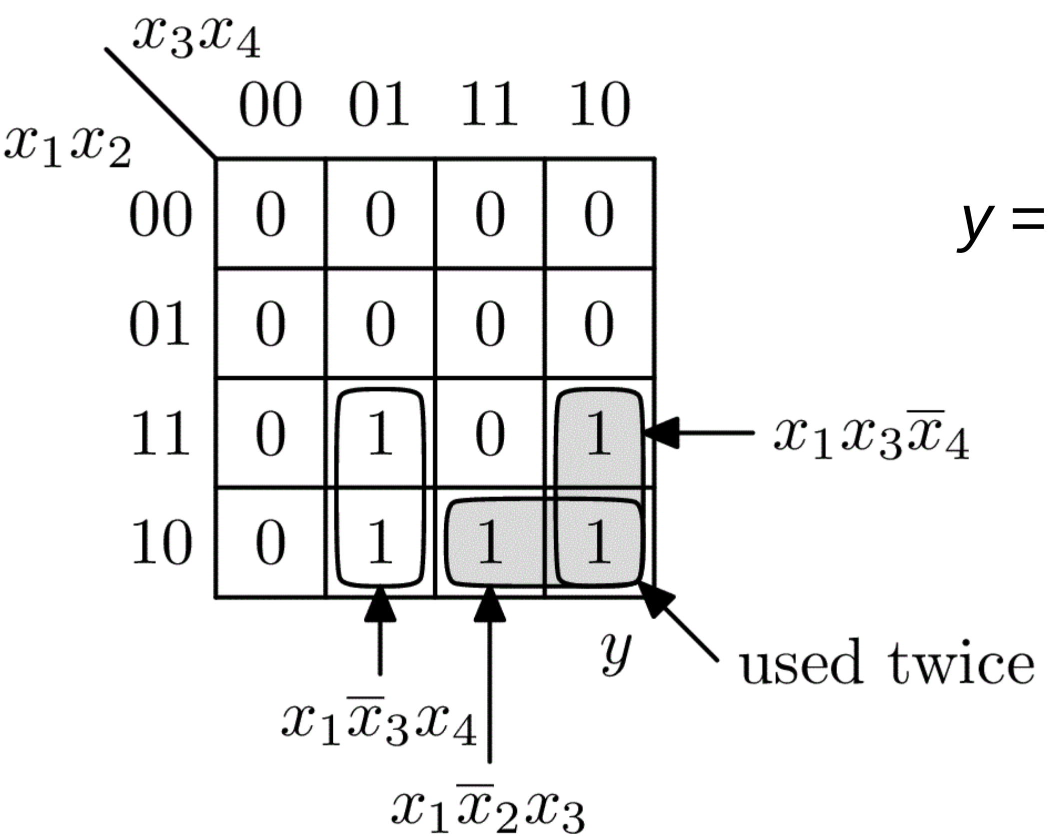




Minimization of logic functions can be carried out without resorting to algebraic manipulation

Logic function minimization

$$Y_r = \sum(\, 9;\ 10;\ 11;\ 13;\ 14\,)$$



$$y = x_1x_3x_4 + x_1x_2x_3 + x_1x_3x_4$$

Mathematical reason

$$y_\star = x_1 x_2 x_3 x_4 + x_1 x_2 x_3 x_4 + x_1 x_2 x_3 x_4$$

$$y_\star = x_1 \overline{x}_2 x_3 x_4 + \underbrace{x_1 \overline{x}_2 x_3 \overline{x}_4}_{a} + \underbrace{x_1 \overline{x}_2 x_3 \overline{x}_4}_{a} + x_1 x_2 x_3 \overline{x}_4$$

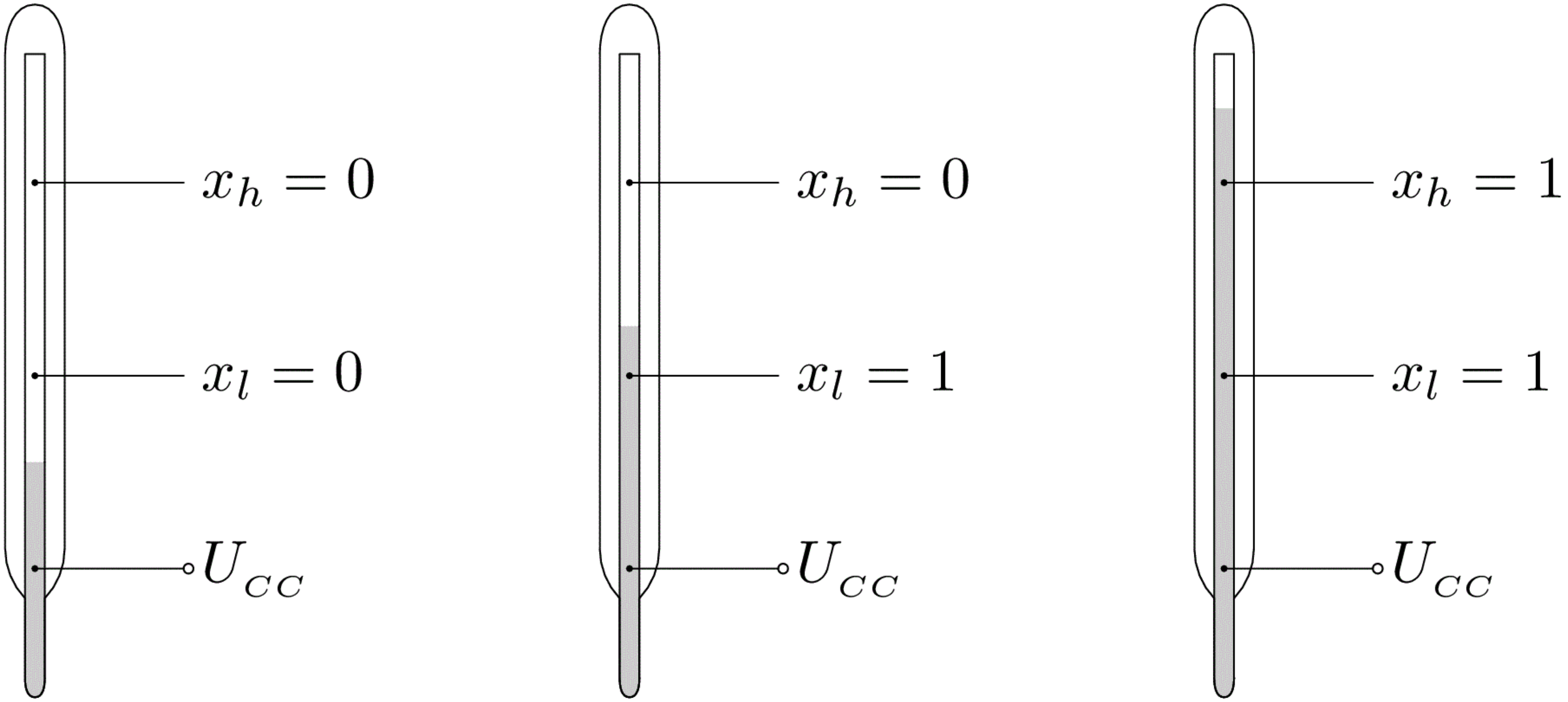
$$a + a = a$$

$$y_\star = x_1 \overline{x}_2 x_3 (x_4 + \overline{x}_4) + x_1 x_3 \overline{x}_4 (\overline{x}_2 + x_2)$$

$$y_\star = x_1 \overline{x}_2 x_3 + x_1 x_3 \overline{x}_4$$

$$\begin{aligned} b &= bx + b\overline{x} = bx + bx + b\overline{x} = bx + b(x + \overline{x}) = bx + b \\ b &= bx + b\overline{x} = bx + b\overline{x} + b\overline{x} = b(x + \overline{x}) + b\overline{x} = b + b\overline{x} \end{aligned}$$

Don't care values



x_l	x_h	situation
0	0	exists
1	0	exists
1	1	exists
0	1	never happens $\Rightarrow$ we don't care

New problem

$$\begin{cases} y_A = \sum\left(1,\ 3,\ 5,\ 6,\ 9,\ 11\quad \underbrace{(2,\ 13)}_{\text{don't care}}\ \right) \\ y_B = \sum\left(7,\ 15\quad \underbrace{(2,\ 13)}_{\text{don't care}}\ \right) \end{cases}$$

$$\Updownarrow$$

$$\begin{cases} F^1_{y_A} = \left\{1,\ 3,\ 5,\ 6,\ 9,\ 11\right\} & F^{\Phi}_{y_A} = \left\{2,\ 13\right\} \\ F^1_{y_B} = \left\{7,\ 15\right\} & F^{\Phi}_{y_B} = \left\{2,\ 13\right\} \end{cases}$$

$x_a x_b \backslash x_c x_d$	00	01	11	10
00	0	1	1	–
01	0	1	0	1
11	0	–	0	0
10	0	1	1	0

y_A

$x_a x_b \backslash x_c x_d$	00	01	11	10
00	0	0	0	–
01	0	0	1	0
11	0	–	1	0
10	0	0	0	0

y_B

First solution - SOP

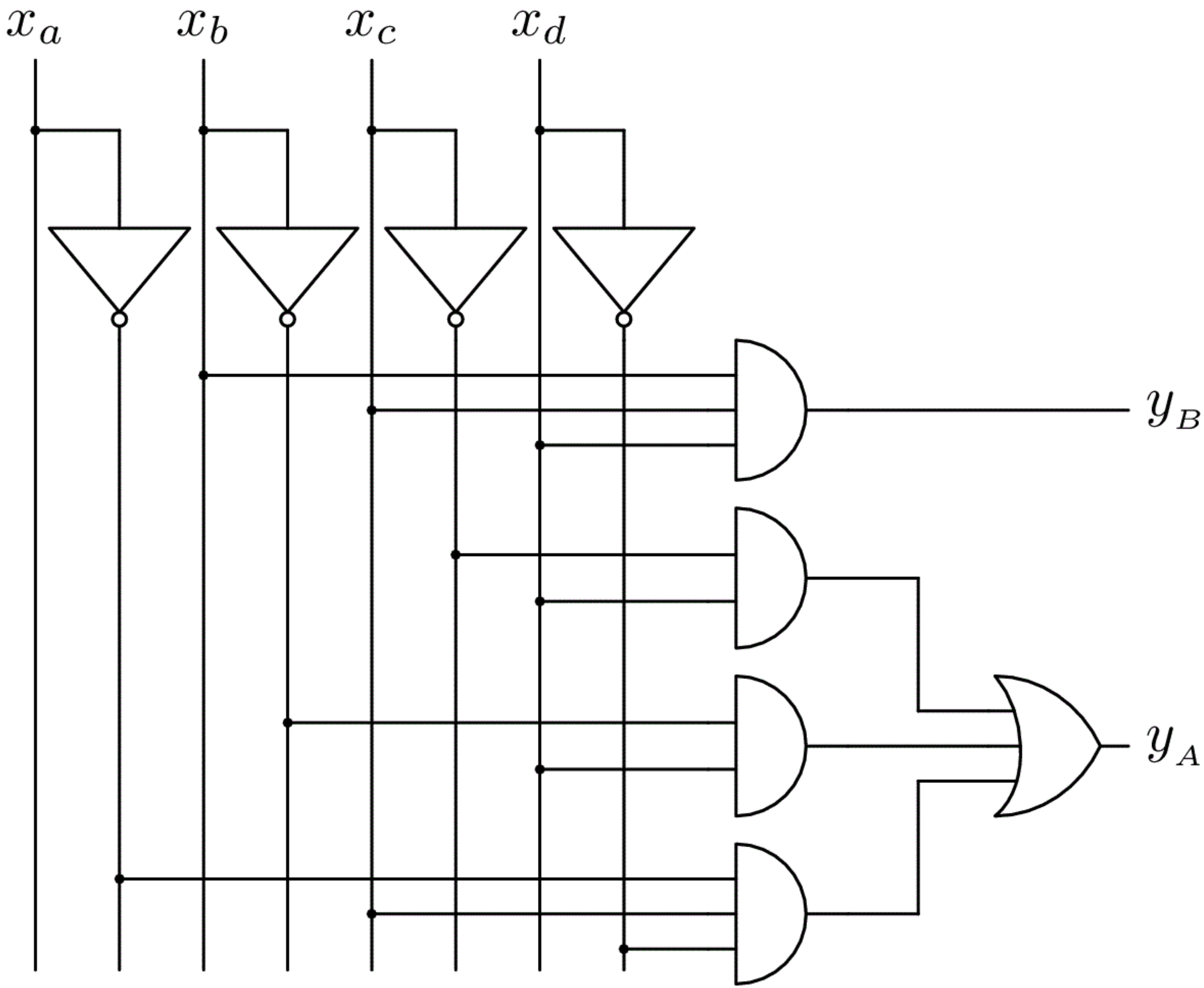
y_A

$x_a x_b$ \ $x_c x_d$	00	01	11	10
00	0	1	1	–
01	0	1	0	1
11	0	–	0	0
10	0	1	1	0

y_B

$x_a x_b$ \ $x_c x_d$	00	01	11	10
00	0	0	0	–
01	0	0	1	0
11	0	–	1	0
10	0	0	0	0

$$\begin{cases} y_A = \overline{x}_c x_d + \overline{x}_b x_d + \overline{x}_a x_c \overline{x}_d \\ y_B = x_b x_c x_d \end{cases}$$


x_a
x_b
x_c
x_d
y_B
y_A

What has really been obtained?

$x_a x_b \backslash x_c x_d$	00	01	11	10
00	0	1	1	—
01	0	1	0	1
11	0	—	0	0
10	0	1	1	0

y_A

$x_a x_b \backslash x_c x_d$	00	01	11	10
00	0	1	1	1
01	0	1	0	1
11	0	1	0	0
10	0	1	1	0

y_A

$$y_A = \sum\left(1,\ 3,\ 5,\ 6,\ 9,\ 11\ (2,\ 13)\right) \qquad y_A = \sum\left(1,\ 2,\ 3,\ 5,\ 6,\ 9,\ 11,\ 13\right)$$

$x_a x_b$ \ $x_c x_d$	00	01	11	10
00	0	0	0	–
01	0	0	1	0
11	0	–	1	0
10	0	0	0	0

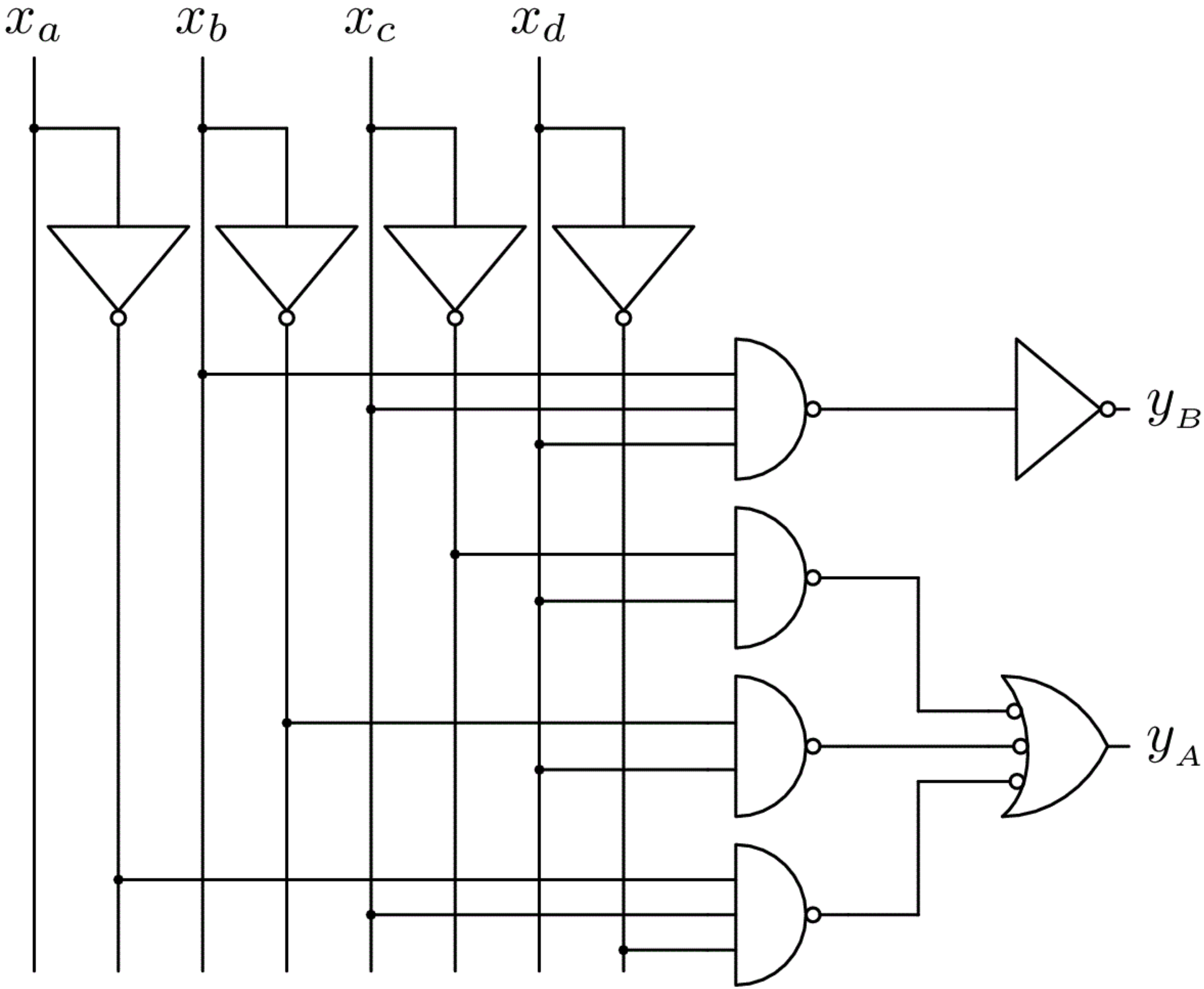
y_B

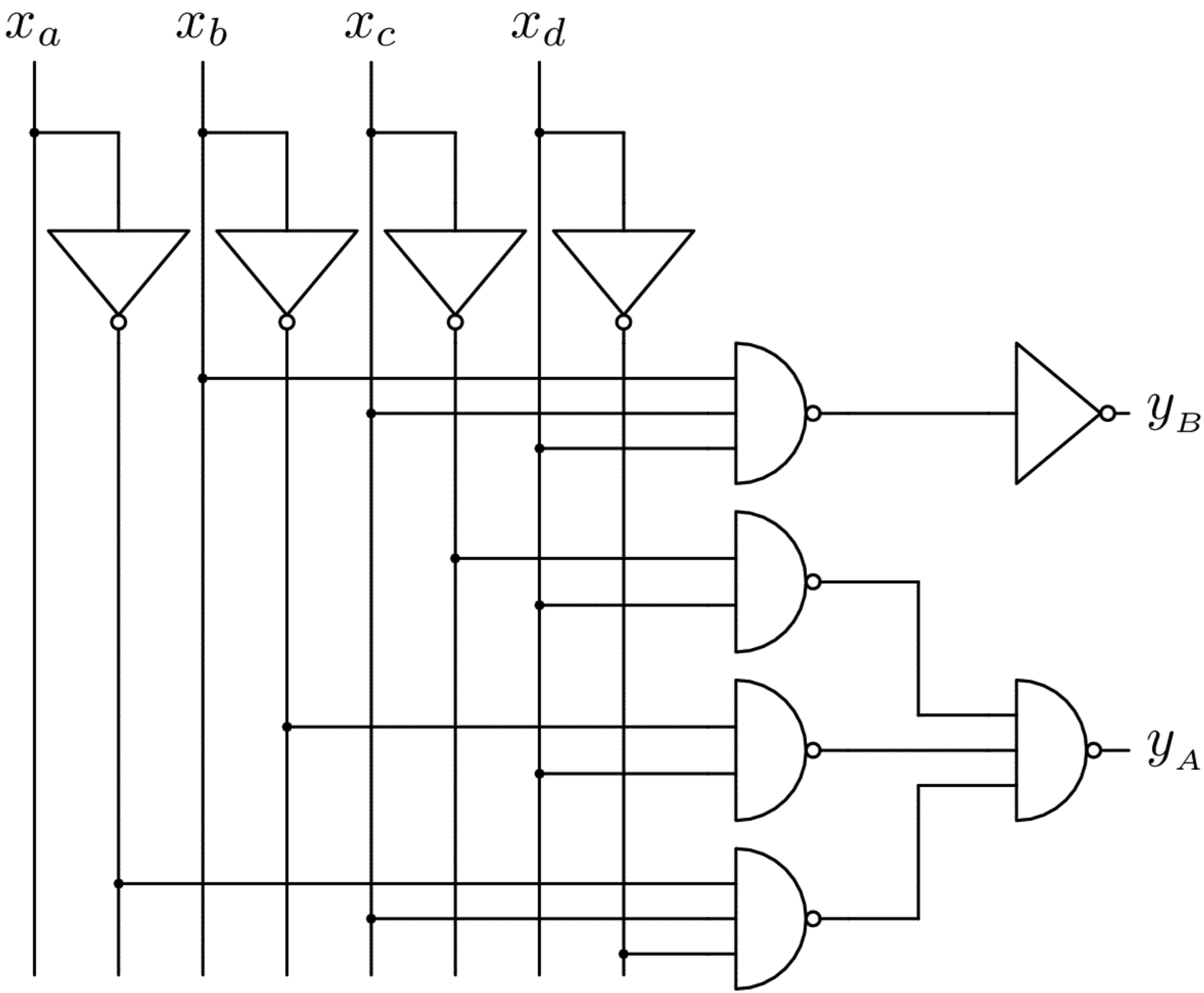
$$y_B = \sum\left(7,\ 15\ (2,\ 13)\right)$$

$x_a x_b$ \ $x_c x_d$	00	01	11	10
00	0	0	0	0
01	0	0	1	0
11	0	0	1	0
10	0	0	0	0

y_B

$$y_B = \sum\left(7,\ 15\right)$$


x_a
x_b
x_c
x_d
y_B
y_A


x_a
x_b
x_c
x_d
y_B
y_A

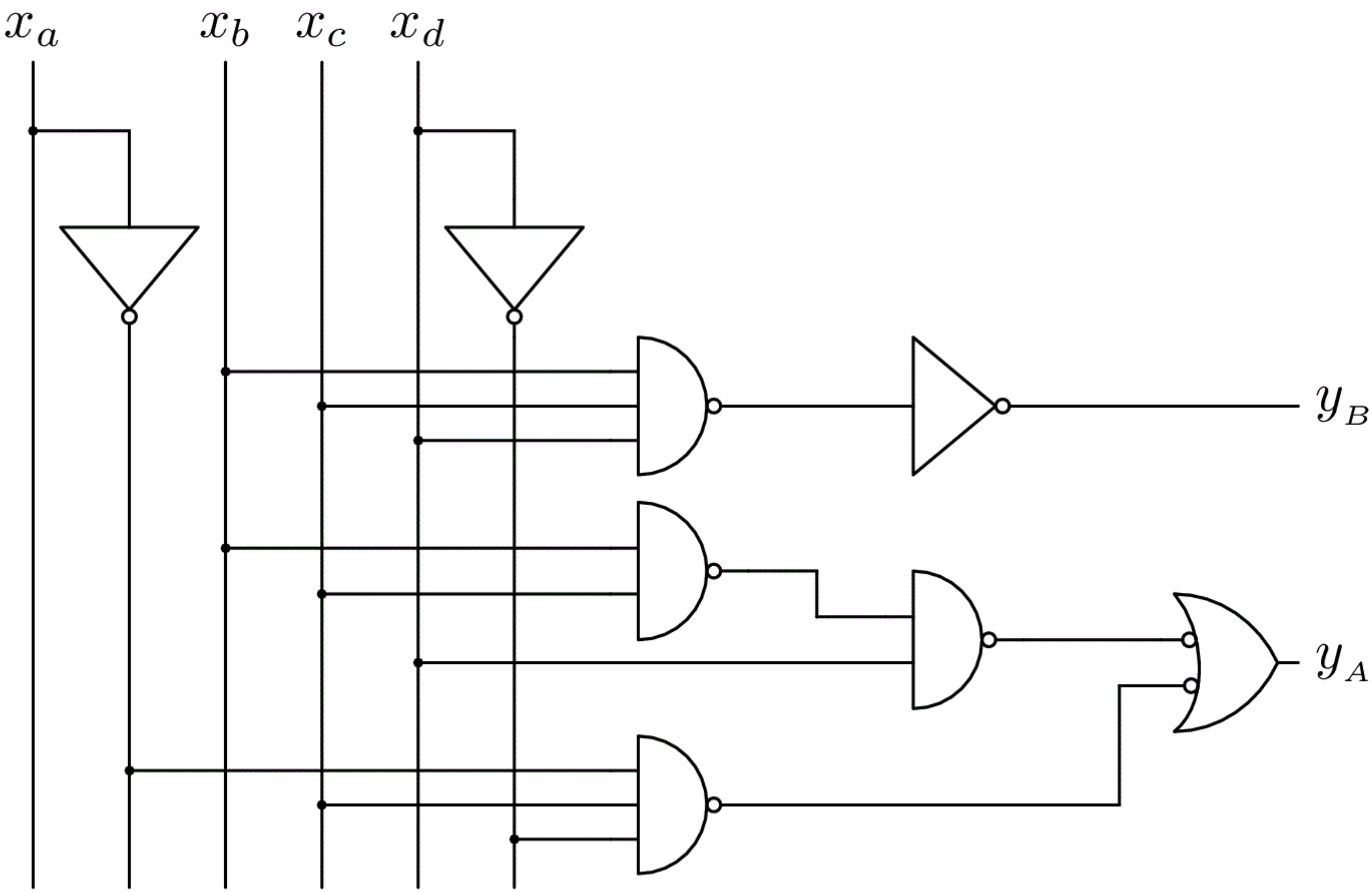
Gate type	NOT+AND+OR	NOT+NAND
NOT	4	5
NAND3	—	3
NAND2	—	2
AND3	2	—
AND2	2	—
OR3	1	—
gates/inputs:	9/17	10/18
integrated circuits	4	3

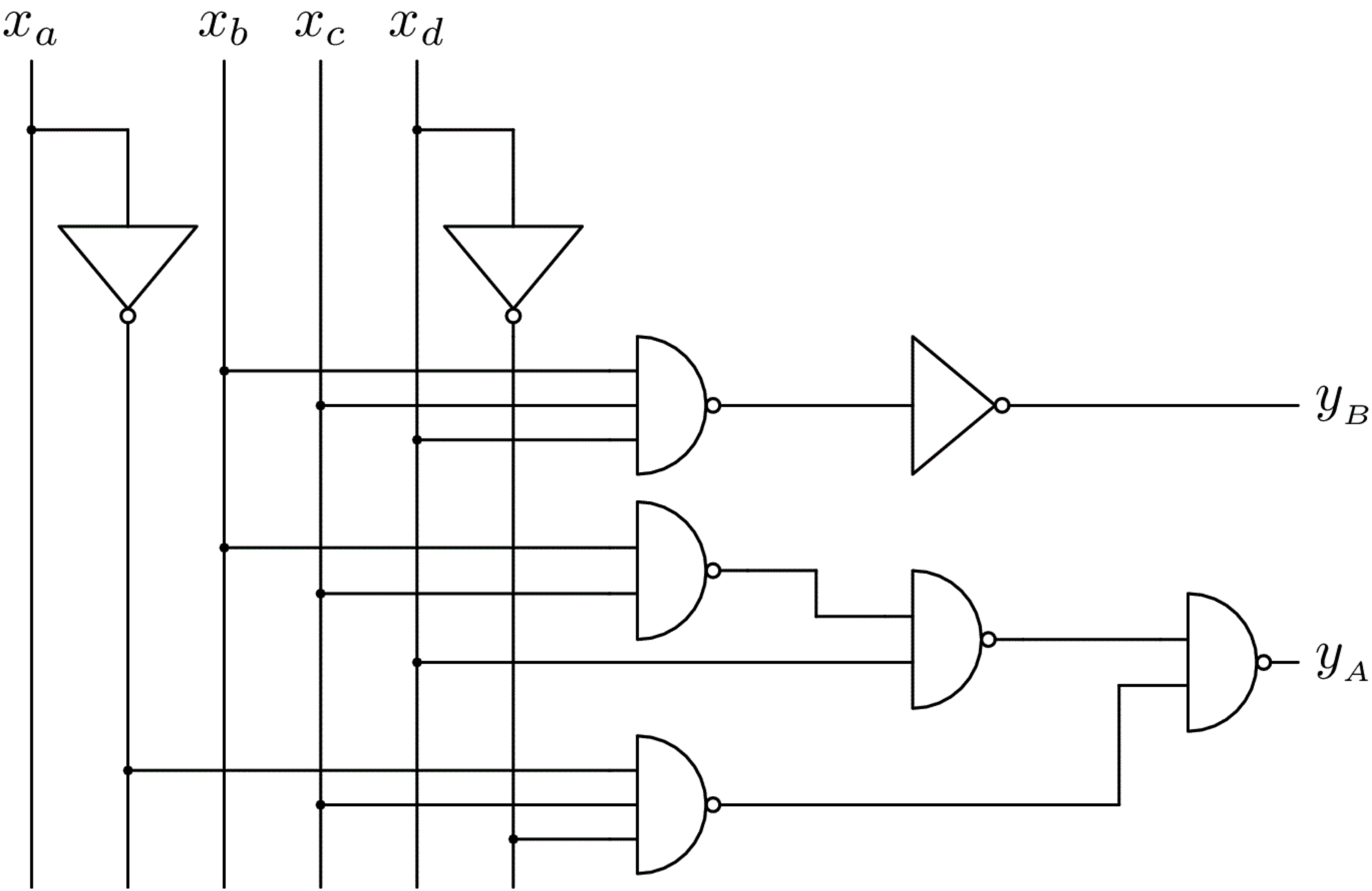
Second solution - factorization

$$\begin{cases} y_A = \overline{x}_c x_d + \overline{x}_b x_d + \overline{x}_a x_c \overline{x}_d \\ y_B = x_b x_c x_d \end{cases}$$

$$\begin{cases} y_A = (\overline{x}_c + \overline{x}_b) x_d + \overline{x}_a x_c \overline{x}_d \\ y_B = x_b x_c x_d \end{cases}$$

$$\begin{cases} y_A = \overline{x_c x_b} x_d + \overline{x}_a x_c \overline{x}_d \\ y_B = x_b x_c x_d \end{cases}$$


x_a
x_b
x_c
x_d
y_B
y_A


x_a
x_b
x_c
x_d
y_B
y_A

Gate type	SOP	SOP NAND	Factori–zation
NOT	4	5	3
NAND3	—	3	2
NAND2	—	2	3
AND3	2	—	—
AND2	2	—	—
OR3	1	—	—
gates/inputs:	9/17	10/18	8/15
integrated circuits	4	3	3
gate levels	3	3	4

Third solution - prohibition

$x_a x_b$ \ $x_c x_d$	00	01	11	10
00	0	1	1	–
01	0	1	0	1
11	0	–	0	0
10	0	1	1	0

y_A^1

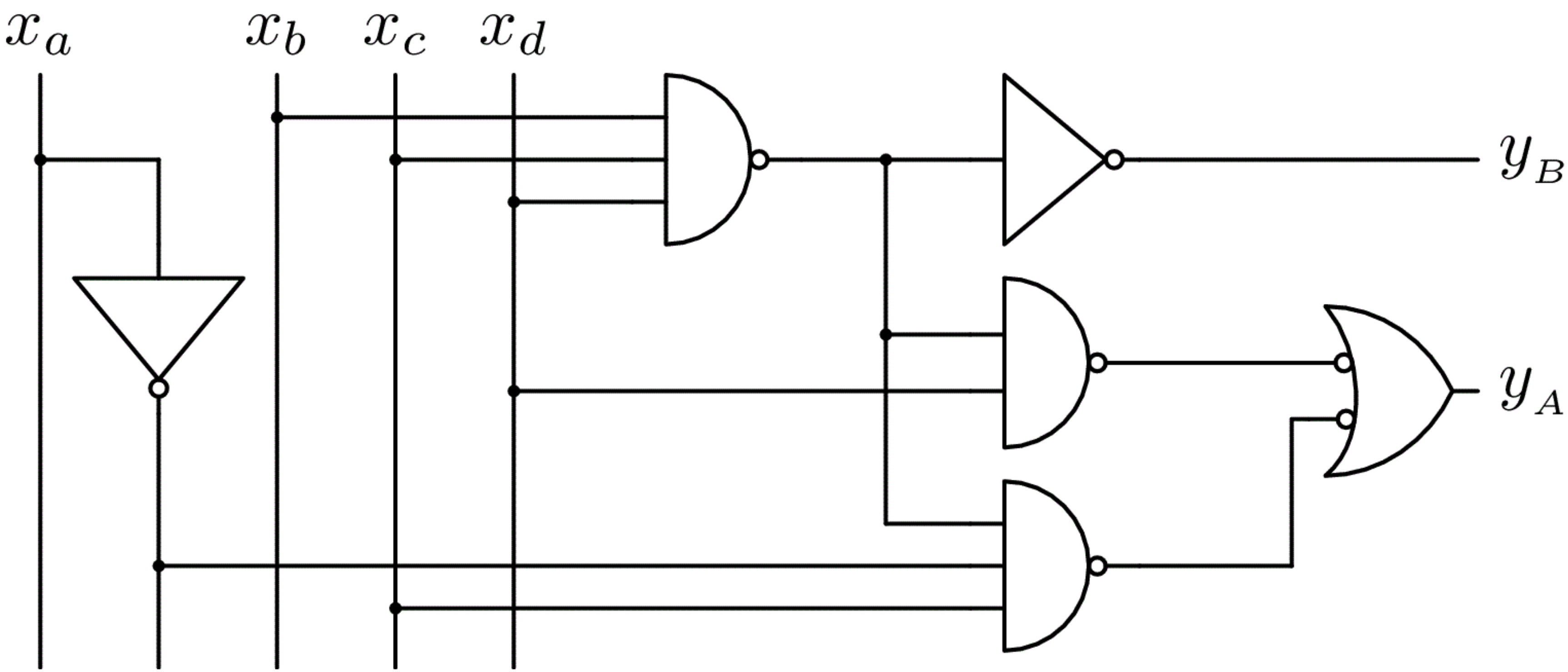
$x_a x_b$ \ $x_c x_d$	00	01	11	10
00	0	0	0	–
01	0	0	1	0
11	0	–	1	0
10	0	0	0	0

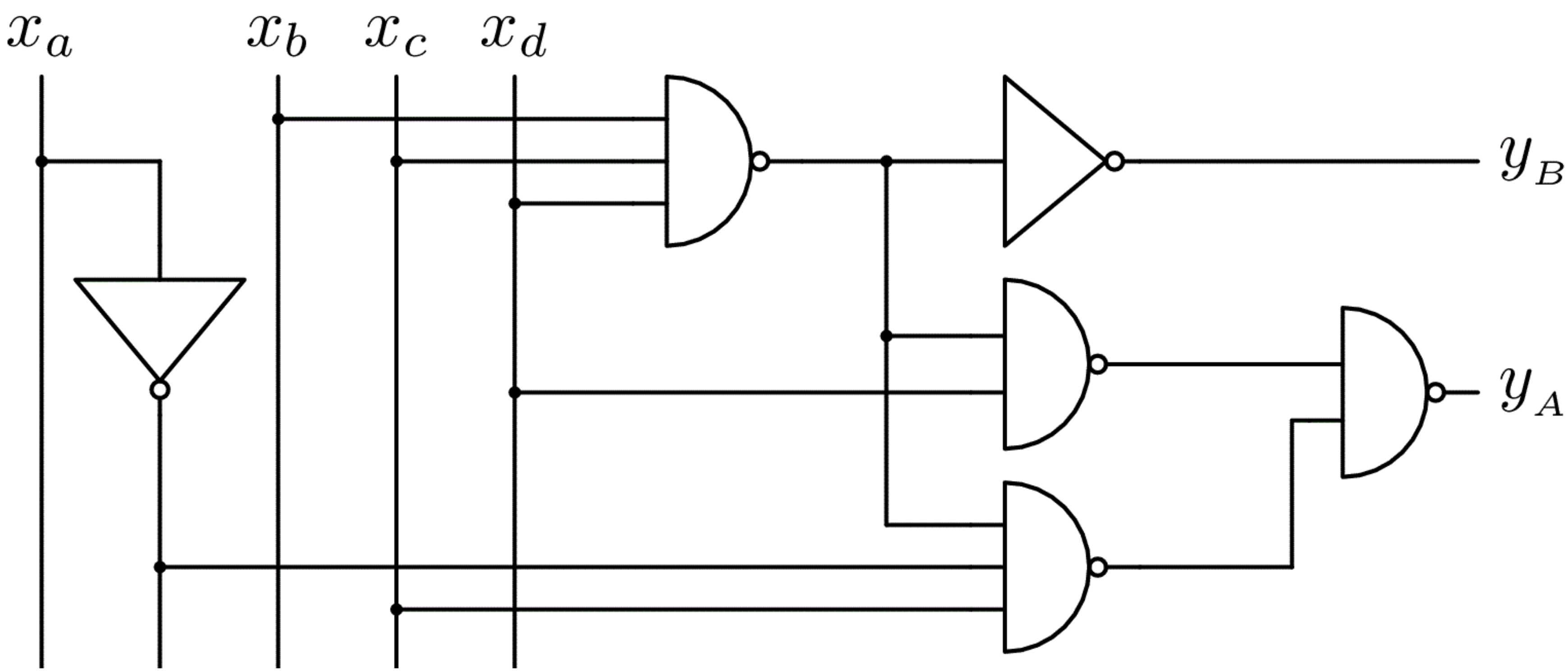
y_B

$x_a x_b \backslash x_c x_d$	00	01	11	10
00	0	1	1	–
01	0	1	0	1
11	0	–	0	0
10	0	1	1	0

y_A^2

$$\begin{cases} y_A = \underbrace{x_d \overline{x_b x_c x_d}}_{y_A^1} + \underbrace{\overline{x}_a x_c \overline{x_b x_c x_d}}_{y_A^2} \\[2em] y_B = x_b x_c x_d \end{cases}$$


x_a
x_b
x_c
x_d
y_B
y_A

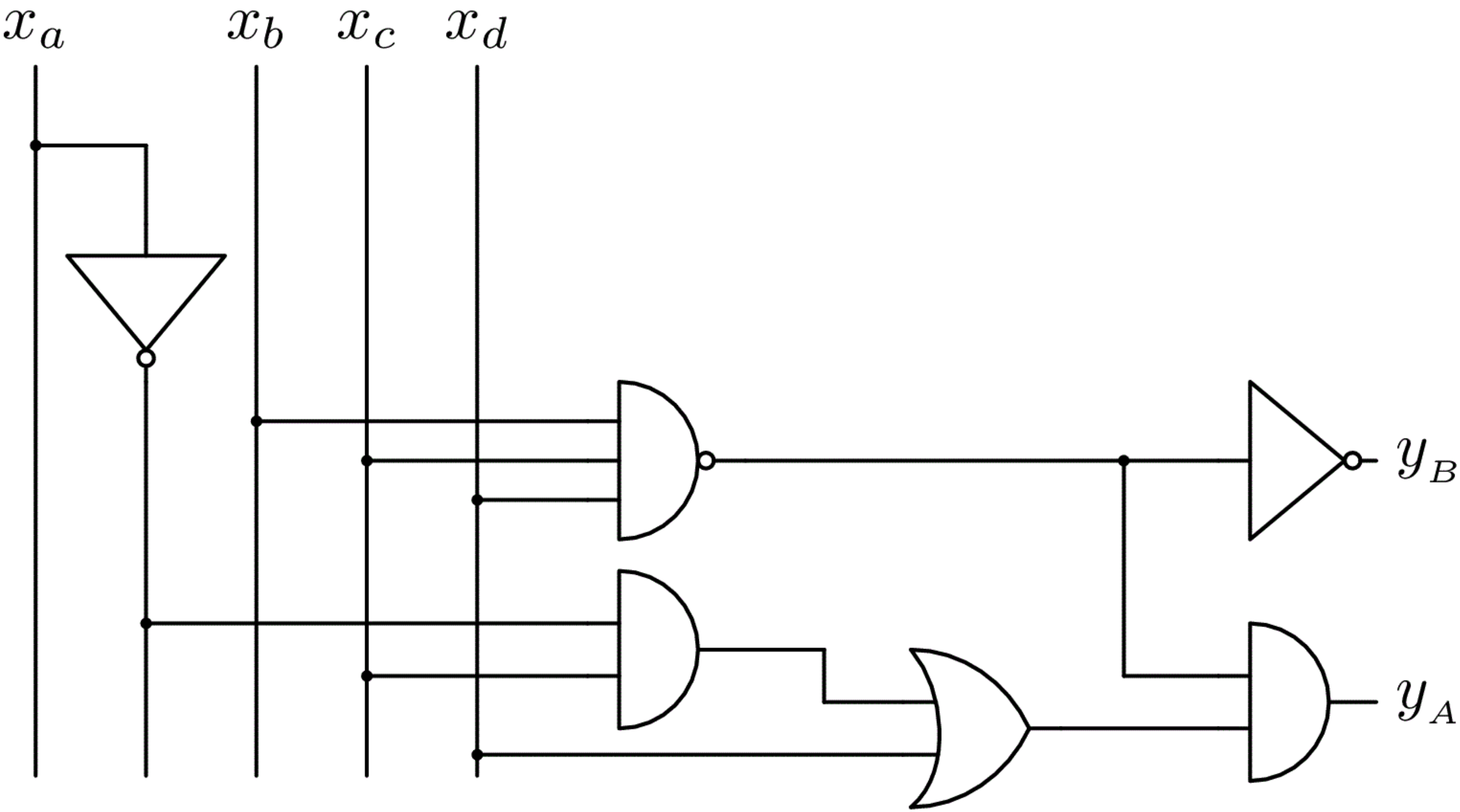

x_a
x_b
x_c
x_d
y_B
y_A

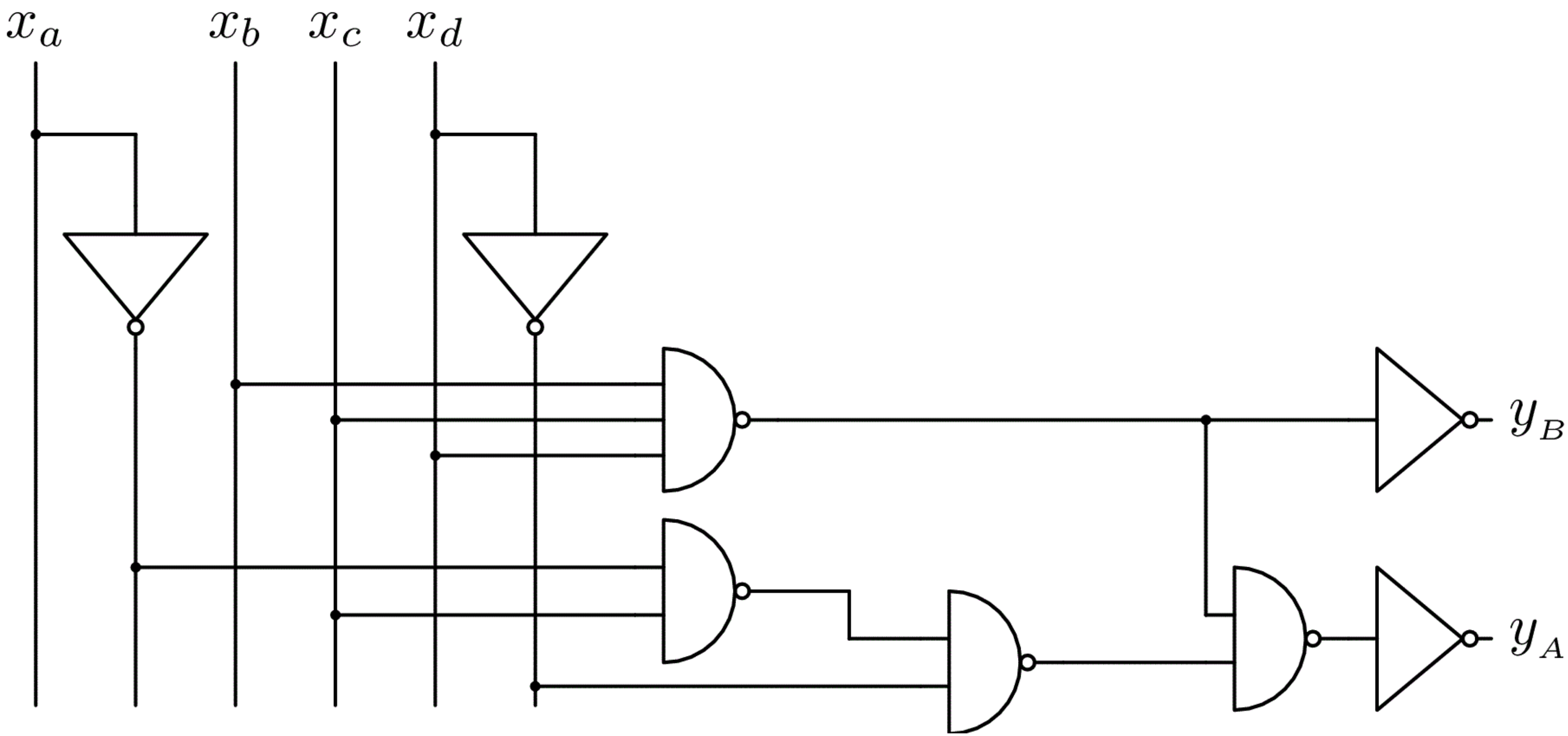
Gate type	SOP	SOP NAND	Factori–zation	Prohi–bition
NOT	4	5	3	2
NAND3	—	3	2	2
NAND2	—	2	3	2
AND3	2	—	—	—
AND2	2	—	—	—
OR3	1	—	—	—
gates/inputs:	9/17	10/18	8/15	6/12
integrated circuits	4	3	3	2
gate levels	3	3	4	4/3

Fourth solution - prohibition & factorization

$$\begin{cases} y_A = x_d\overline{x_b x_c x_d} + \overline{x}_a x_c \overline{x_b x_c x_d} \\ \\ y_B = x_b x_c x_d \end{cases}$$

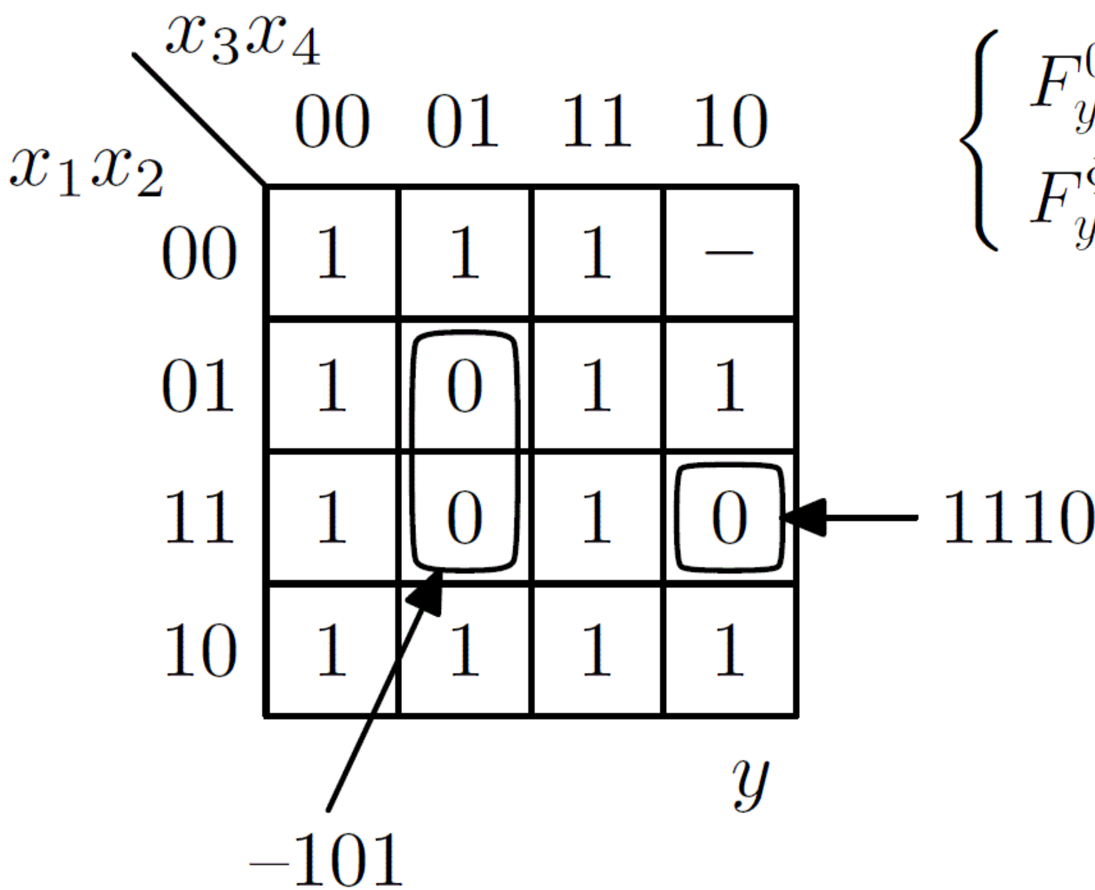
$$\begin{cases} y_A = \left(x_d + \overline{x}_a x_c\right) \overline{x_b x_c x_d} \\ \\ y_B = x_b x_c x_d \end{cases}$$


x_a
x_b
x_c
x_d
y_B
y_A


x_a
x_b
x_c
x_d
y_B
y_A

Gate type	SOP	SOP NAND	Factori–zation	Prohi–bition	P+F AND	P+F NAND
NOT	4	5	3	2	2	4
NAND3	—	3	2	2	1	1
NAND2	—	2	3	2	—	3
AND3	2	—	—	—	—	—
AND2	2	—	—	—	2	—
OR3	1	—	—	—	—	—
OR2	—	—	—	—	1	—
gates	9	10	8	6	6	8
inputs	17	18	15	12	11	13
ICs	4	3	3	2	3	3
levels	3	3	4	4/3	4	5

POS - Product of Sums form



$$\begin{cases} F_y^0 = \{\,5,\ \ 13,\ \ 14\,\} \\ F_y^{\Phi} = \{\,2\,\} \end{cases}$$

$$\begin{array}{cccccccc} y=0 \ \text{if} & x_1 & \text{and} & x_2 & \text{and} & x_3 & \text{and} & x_4 \\ & 1 & & 1 & & 1 & & 0 \end{array}$$

$$\Downarrow$$

$$\begin{array}{cccccccc} y=1 \ \text{if} & x_1 & \text{or} & x_2 & \text{or} & x_3 & \text{or} & x_4 \\ & 0 & & 0 & & 0 & & 1 \end{array}$$

$$\Downarrow$$

$$\overline{x}_1 + \overline{x}_2 + \overline{x}_3 + x_4 = 0 \qquad \text{when } 1110$$
$$\overline{x}_1 + \overline{x}_2 + \overline{x}_3 + x_4 = 1 \qquad \text{when otherwise}$$

$$\begin{array}{cccccccc} y=0 \ \text{if} & x_1 & \text{and} & x_2 & \text{and} & x_3 & \text{and} & x_4 \\ & - & & 1 & & 0 & & 1 \end{array}$$

$$\Downarrow$$

$$\begin{array}{cccccccc} y=1 \ \text{if} & x_1 & \text{or} & x_2 & \text{or} & x_3 & \text{or} & x_4 \\ & - & & 0 & & 1 & & 0 \end{array}$$

$$\Downarrow$$

$$\overline{x}_2 + x_3 + \overline{x}_4 = 0 \qquad \text{when } -101$$
$$\overline{x}_2 + x_3 + \overline{x}_4 = 1 \qquad \text{when otherwise}$$

Finally the product of sums form is obtained:

$$\Rightarrow \quad y = \left(\overline{x}_1 + \overline{x}_2 + \overline{x}_3 + x_4\right)\left(\overline{x}_2 + x_3 + \overline{x}_4\right)$$

$x_1x_2 \backslash x_3x_4$	00	01	11	10
00	1	1	1	–
01	1	0	1	1
11	1	0	1	0
10	1	1	1	1

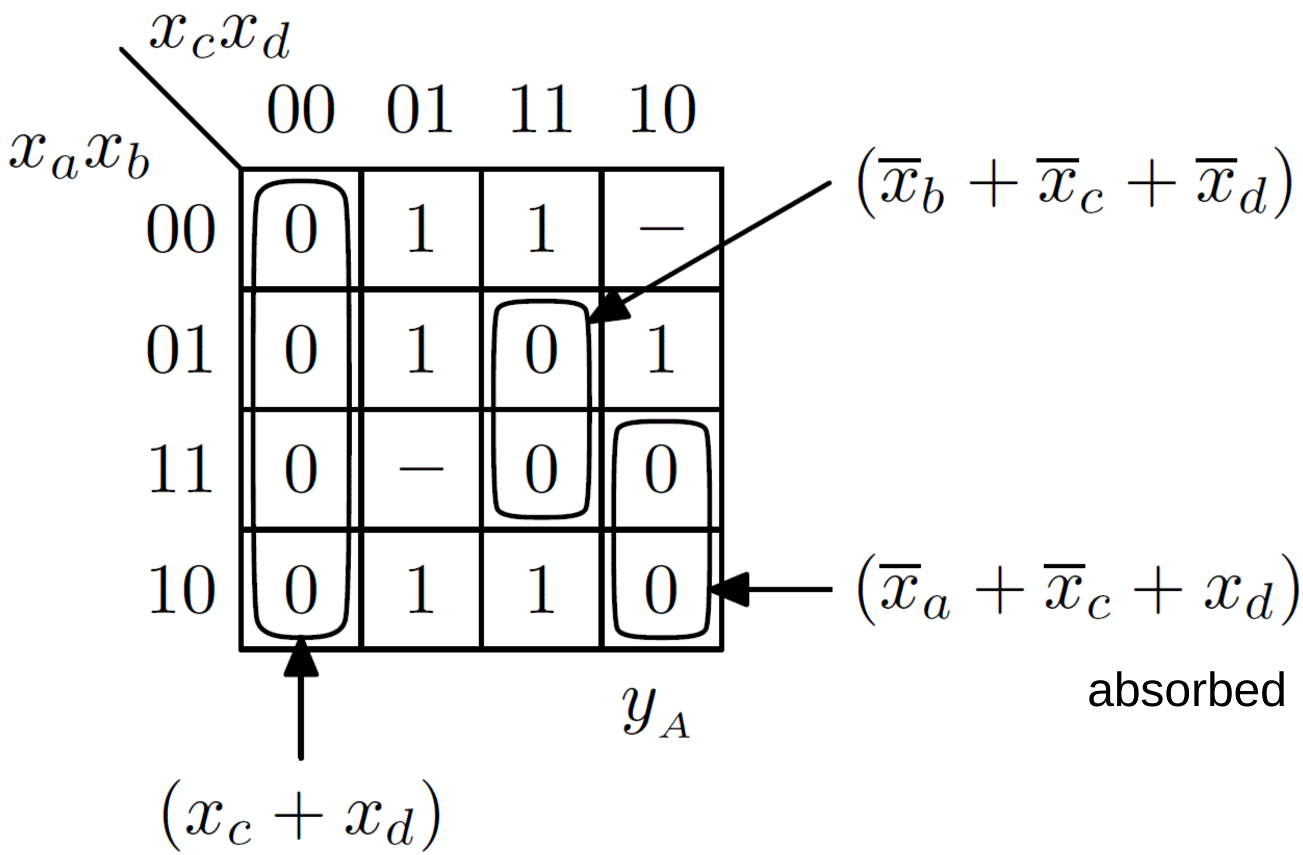
y

$$\overline{x}_1 + \overline{x}_2 + \overline{x}_3 + x_4$$

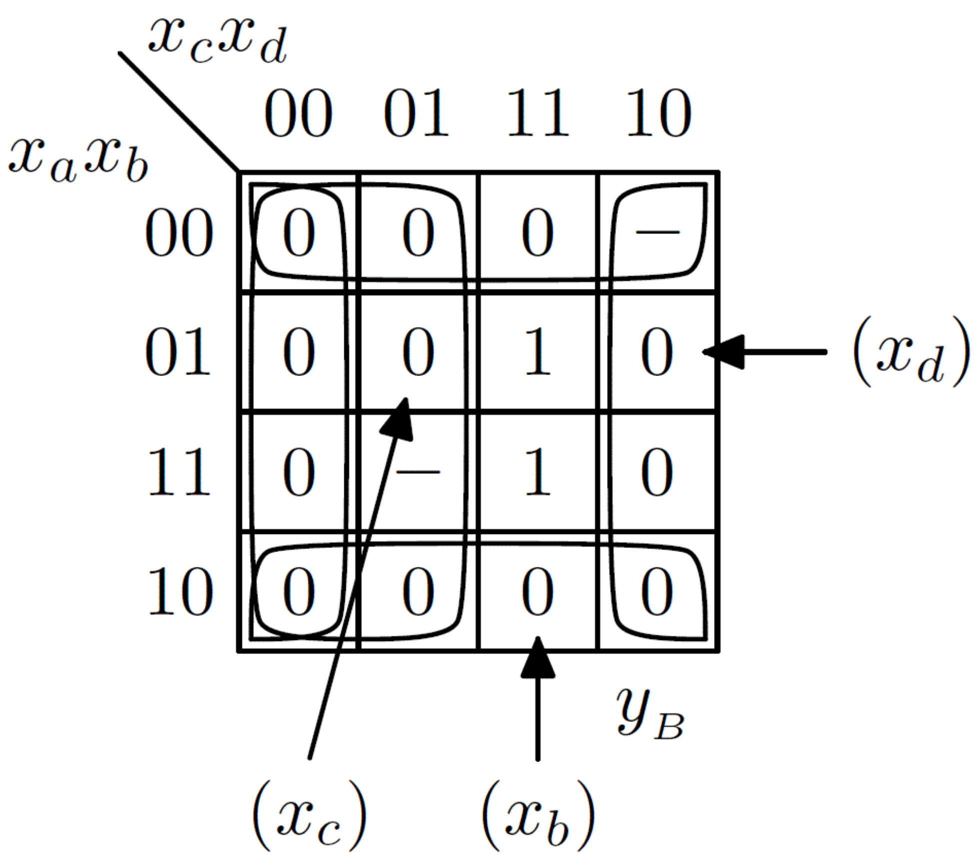
$$\overline{x}_2 + x_3 + \overline{x}_4$$

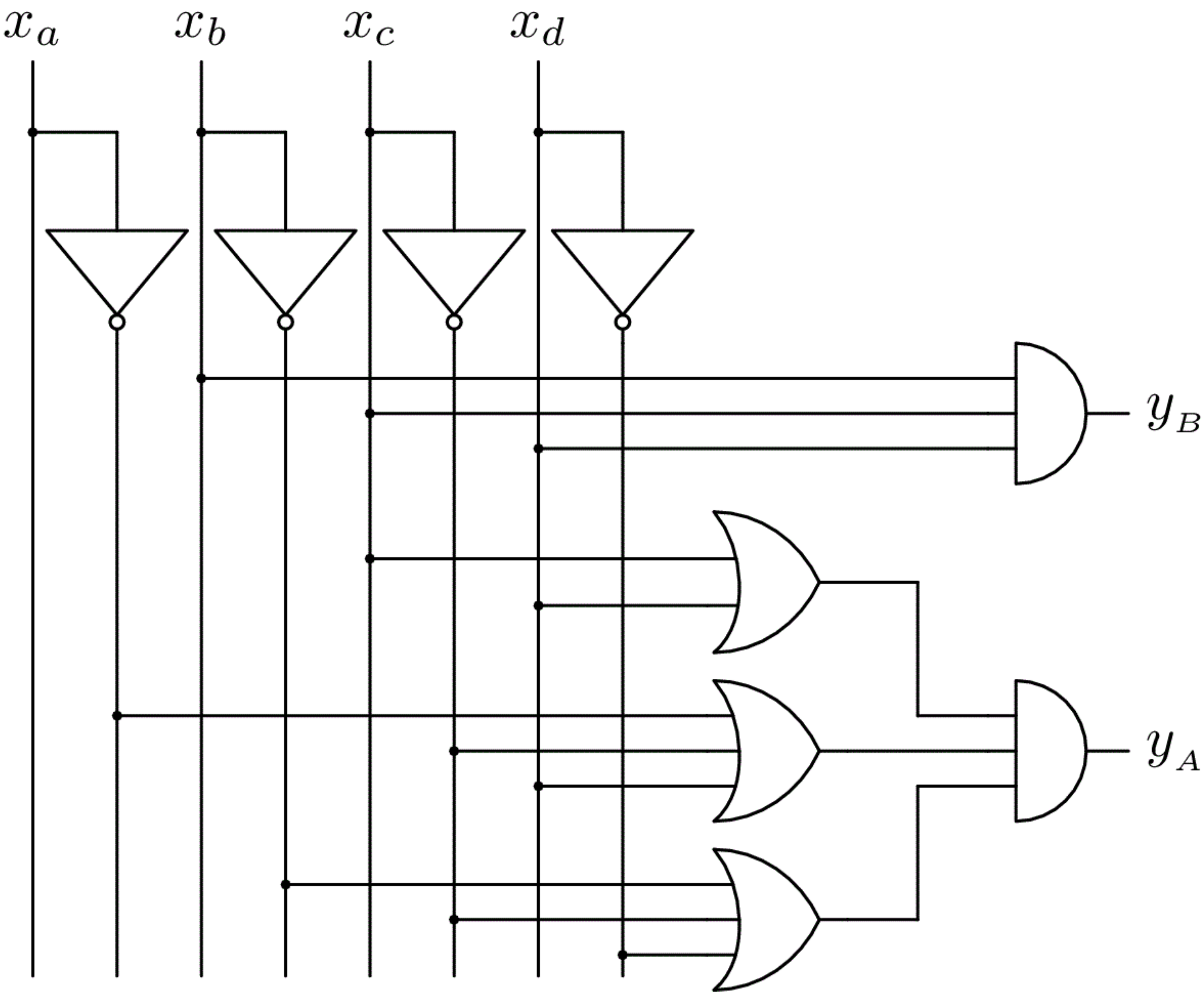
$$y = \prod \left(5,\ 13,\ 14\ (2)\right)$$

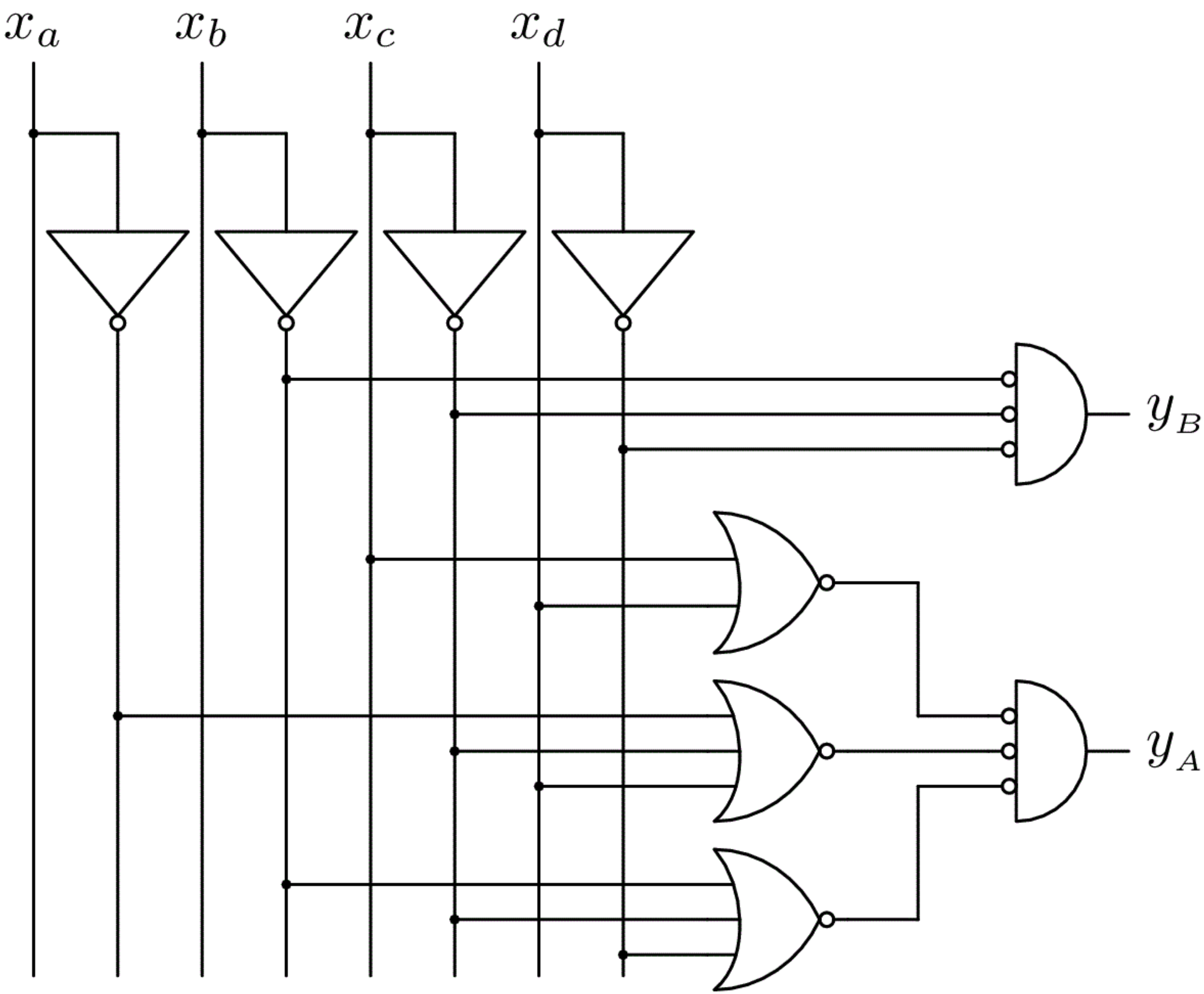
Fifth solution - POS

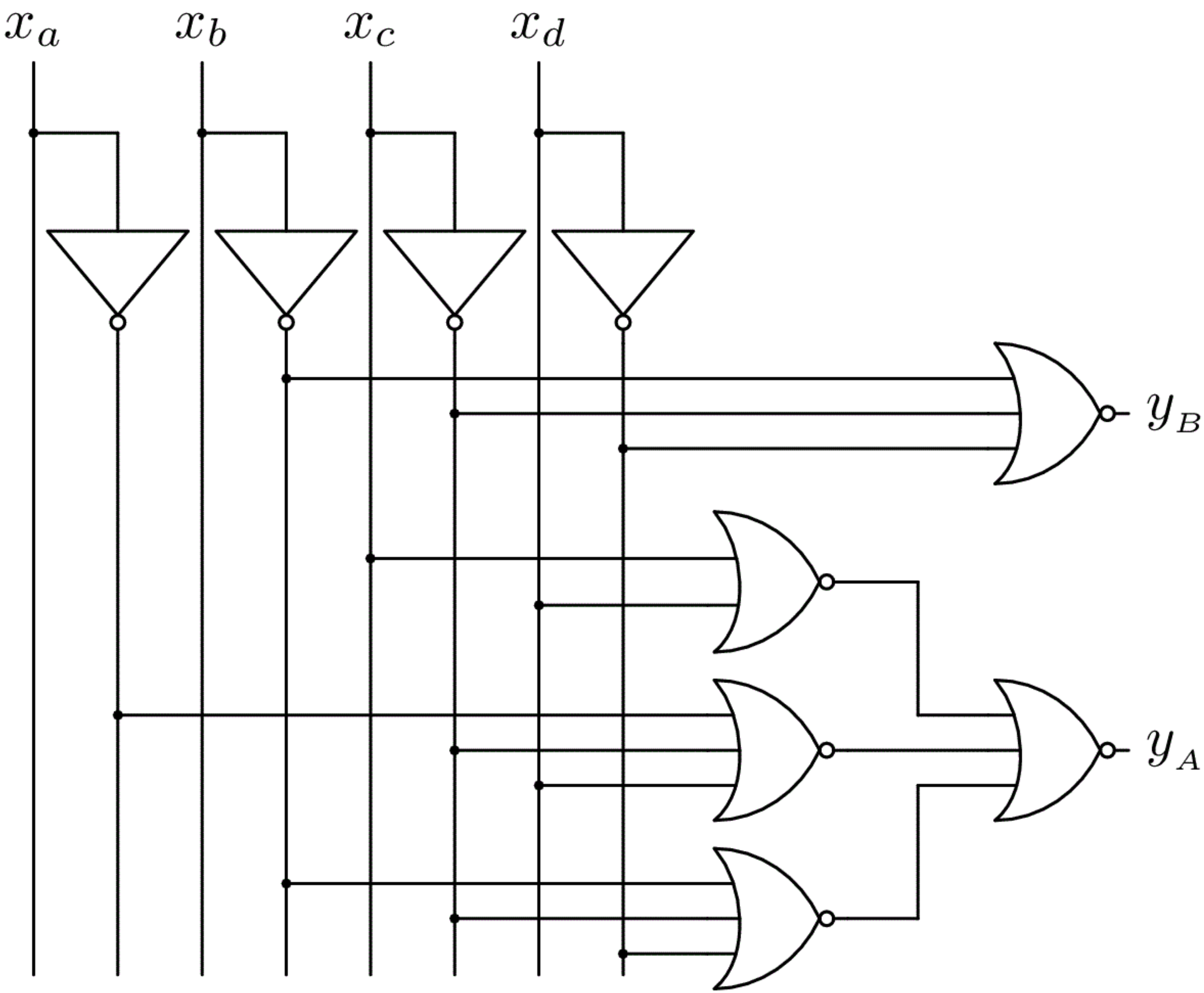


$$\begin{cases} y_A &= (x_c + x_d)(\overline{x}_b + \overline{x}_c + \overline{x}_d)(\overline{x}_a + \overline{x}_c + x_d) \\ y_B &= (x_b)(x_c)(x_d) = x_b x_c x_d \end{cases}$$




x_a
x_b
x_c
x_d
y_B
y_A


x_a
x_b
x_c
x_d
y_B
y_A


x_a
x_b
x_c
x_d
y_B
y_A

Gate type	SOP	SOP NAND	Fact. F	Proh. P	P+F AND	P+F NAND	POS	POS NOR
NOT	4	5	3	2	2	4	4	4
NAND3	–	3	2	2	1	1	–	–
NAND2	–	2	3	2	–	3	–	–
AND3	2	–	–	–	–	–	2	–
AND2	2	–	–	–	2	–	–	–
OR3	1	–	–	–	–	–	2	–
OR2	–	–	–	–	1	–	1	–
NOR3	–	–	–	–	–	–	–	4
NOR2	–	–	–	–	–	–	–	1
gates	9	10	8	6	6	8	9	9
inputs	17	18	15	12	11	13	18	18
ICs	4	3	3	2	3	3	3	3
levels	3	3	4	4/3	4	5	3	3

Minimization of the Boolean Function

- Truth table with Kanaugh islands marked.
- Set of all prime implicants:

$$\Theta = \{ abc, cf, cd, ce \}$$

- Minimal cover function:

$$Y = abc+cd$$

Quine McCluskey method

dec	bin	# 1s
2	0010	1
3	0011	2
6	0110	2
7	0111	3
9	1001	2
12	1100	2
15	1111	4
(4)	0100	1
(10)	1010	2

$$y = \sum \big(2, 3, 6, 7, 9, 12, 15, (4, 10)\big)$$

Stage 1

2	0	0	1	0	
(4)	0	1	0	0	
3	0	0	1	1	
6	0	1	1	0	
9	1	0	0	1	*
(10)	1	0	1	0	
12	1	1	0	0	
7	0	1	1	1	
15	1	1	1	1	

Stage 2

2, 3	0	0	1	–	
2, 6	0	–	1	0	
2, (10)	–	0	1	0	*
(4), 6	0	1	–	0	*
(4), 12	–	1	0	0	*
3, 7	0	–	1	1	
6, 7	0	1	1	–	
7, 15	–	1	1	1	*

Stage 3

2, 3, 6, 7	0	–	1	–	*
2, 6, 3, 7	0	–	1	–	

Prime implicant	Prime implicant	1s of the function							Note
dec	bin	2	3	6	7	9	12	15	
9	1 0 0 1					*			essential prime imp.
$2, (10)$	– 0 1 0	*							eclipsed by $2, 3, 6, 7$
$(4), 6$	0 1 – 0			*					eclipsed by $2, 3, 6, 7$
$(4), 12$	– 1 0 0						*		essential prime imp.
$7, 15$	– 1 1 1				*			*	essential prime imp.
$2, 3, 6, 7$	0 – 1 –	*	*	*	*				essential prime imp.

Dominating rows eclipse dominated rows
$\Rightarrow$ Prime implicant (row) $2, 3, 6, 7$ dominates prime implicants (rows) $2, (10)$ and $(4), 6$

Just a demonstration

Prime implicant	Prime implicant	1s of the function				
dec	bin	2	3	6	7	15
$7,15$	$-\ 1\ 1\ 1$				$*$	$*$
$2,3,6,7$	$0\ -\ 1\ -$	$*$	$*$	$*$	$*$	

Dominated columns eclipse dominating columns
$\Rightarrow$ column 15 is dominated by column 7

Prime implicant	Prime implicant	1s of the function			
dec	bin	2	3	6	15
$7,15$	$-\ 1\ 1\ 1$				$*$
$2,3,6,7$	$0\ -\ 1\ -$	$*$	$*$	$*$	

Final selection (choose all essential prime implicants):

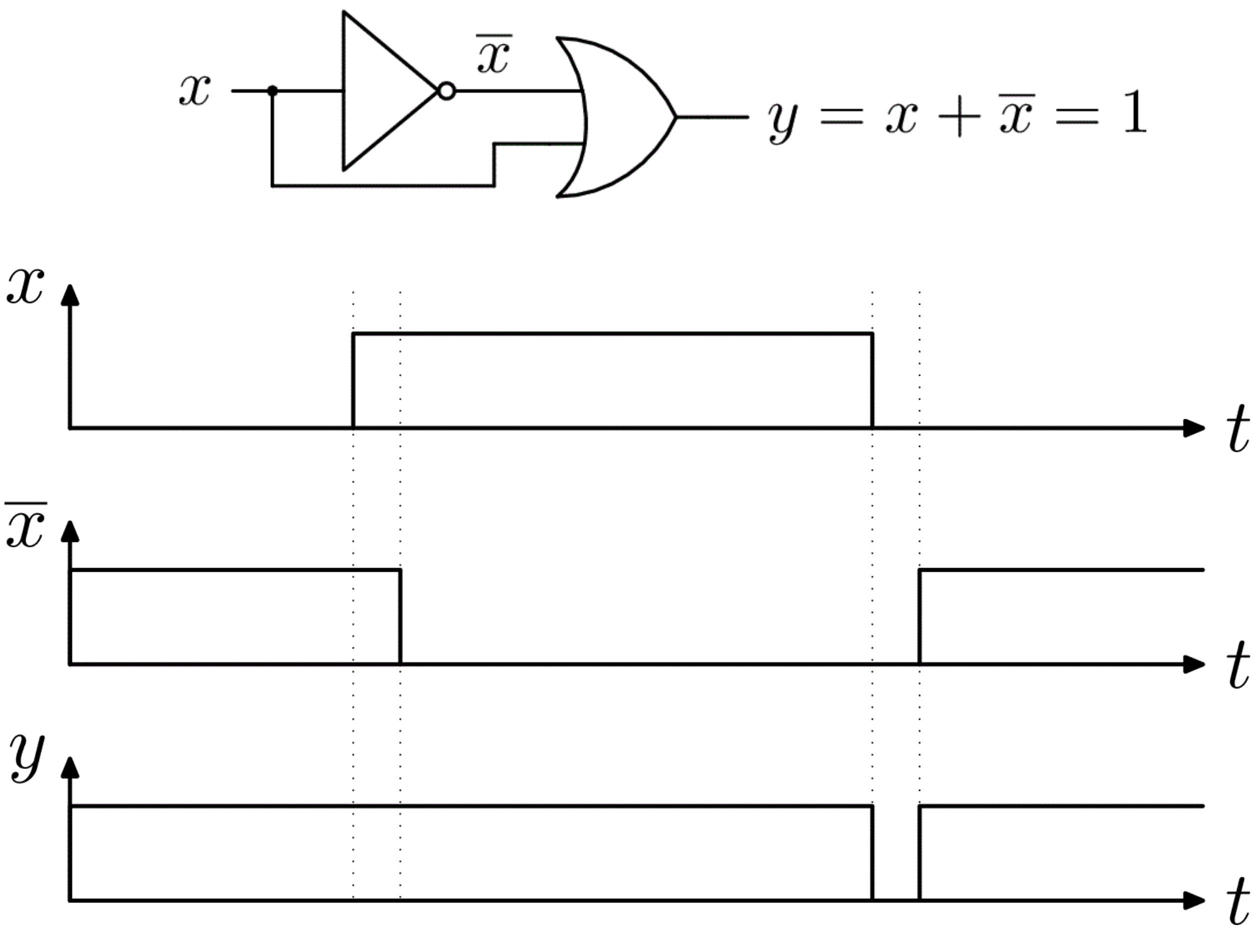
Prime implicant decimal	Prime implicant binary	Prime implicant literal
9	1 0 0 1	$x_1 \; \overline{x}_2 \; \overline{x}_3 \; x_4$
(4), 12	– 1 0 0	$x_2 \; \overline{x}_3 \; \overline{x}_4$
7, 15	– 1 1 1	$x_2 \; x_3 \; x_4$
2, 3, 6, 7	0 – 1 –	$\overline{x}_1 \; x_3$

$$y = x_1\overline{x}_2\overline{x}_3x_4 + x_2\overline{x}_3\overline{x}_4 + x_2x_3x_4 + \overline{x}_1x_3$$

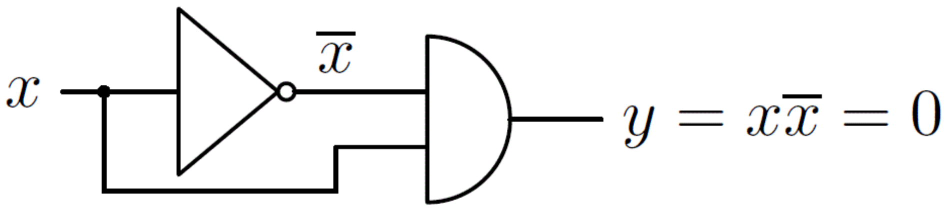
x_1x_2 \ x_3x_4	00	01	11	10
00	0	0	1	1
01	–	0	1	1
11	1	0	1	0
10	0	1	0	–

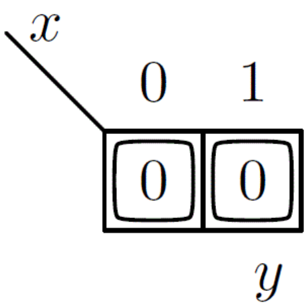
y

Hazard in a SOP realisation

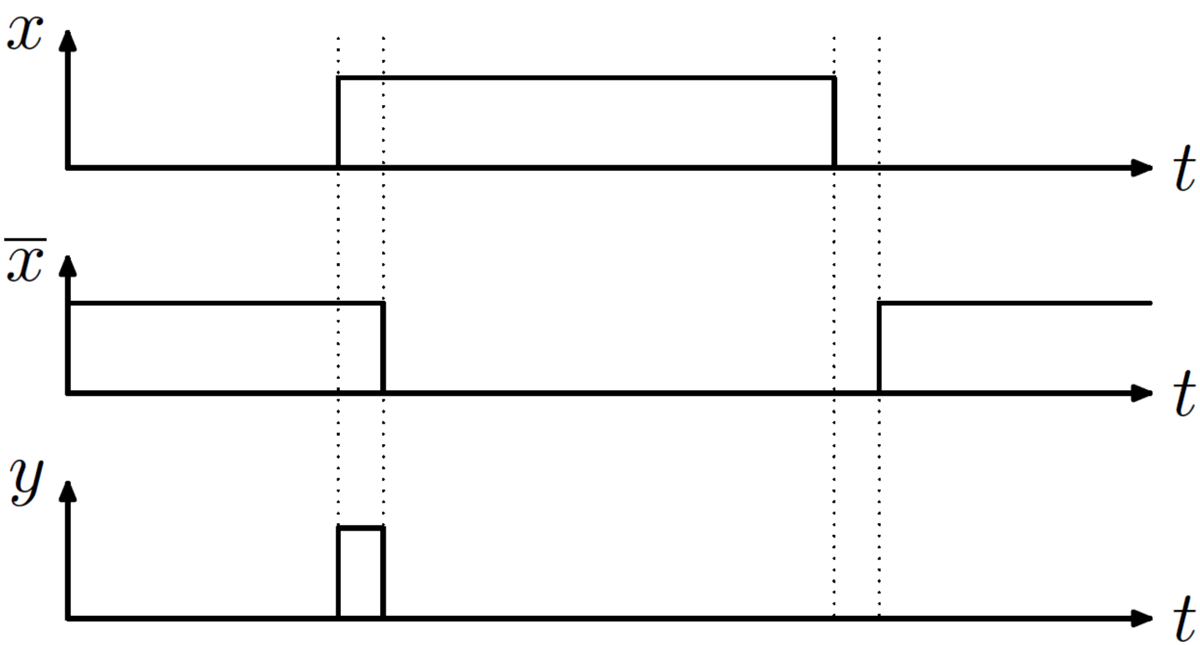


Hazard in a POS realisation





Time plots



Hazard cntd.

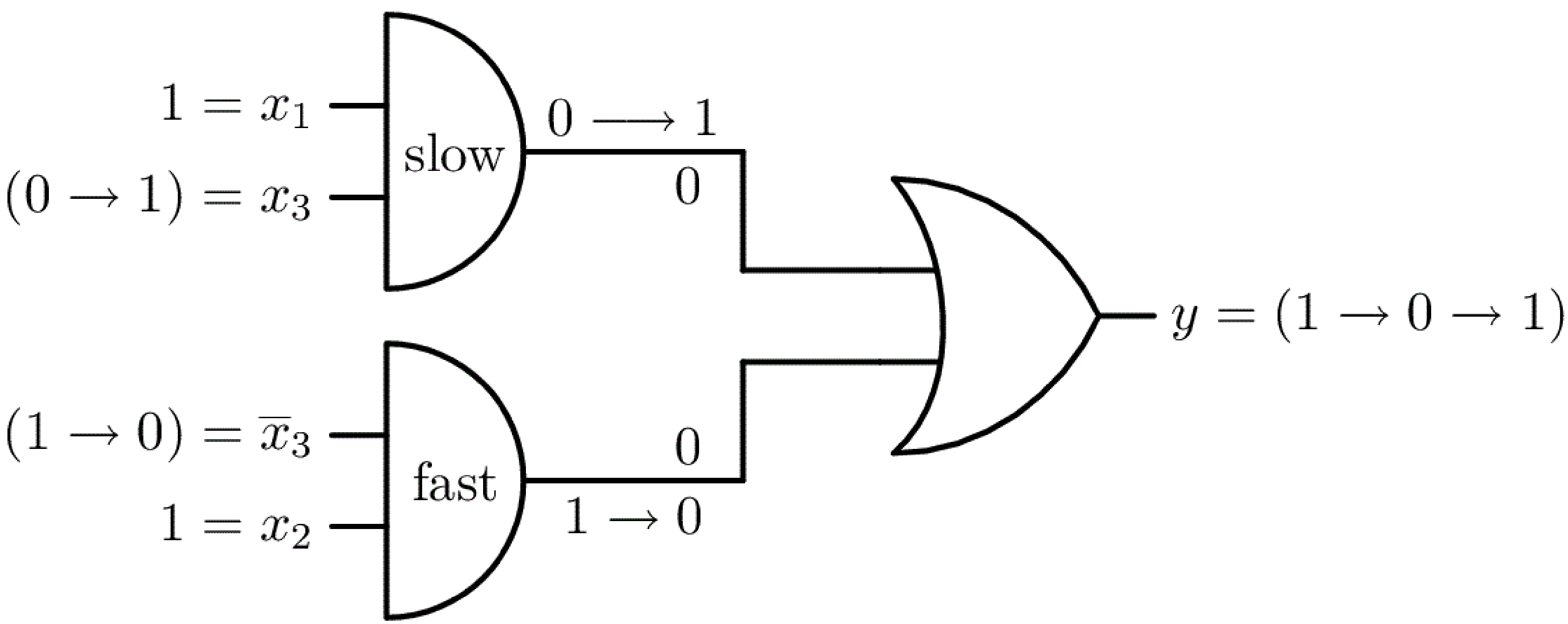
$x_1x_2 \backslash x_3x_4$	00	01	11	10
00	0	0	0	0
01	1	1	0	0
11	1	1	1	1
10	0	0	1	1

y

$$y = x_1x_3 + x_2\overline{x}_3$$

$$\begin{array}{cccc} x_1 & x_2 & x_3 & x_4 \\ \downarrow & \downarrow & \downarrow & \downarrow \\ 1 & 1 & 0 & 1 \end{array} \longrightarrow \begin{array}{cccc} x_1 & x_2 & x_3 & x_4 \\ \downarrow & \downarrow & \downarrow & \downarrow \\ 1 & 1 & 1 & 1 \end{array}$$

The circuit - and the problem



Hazard - solution to the problem

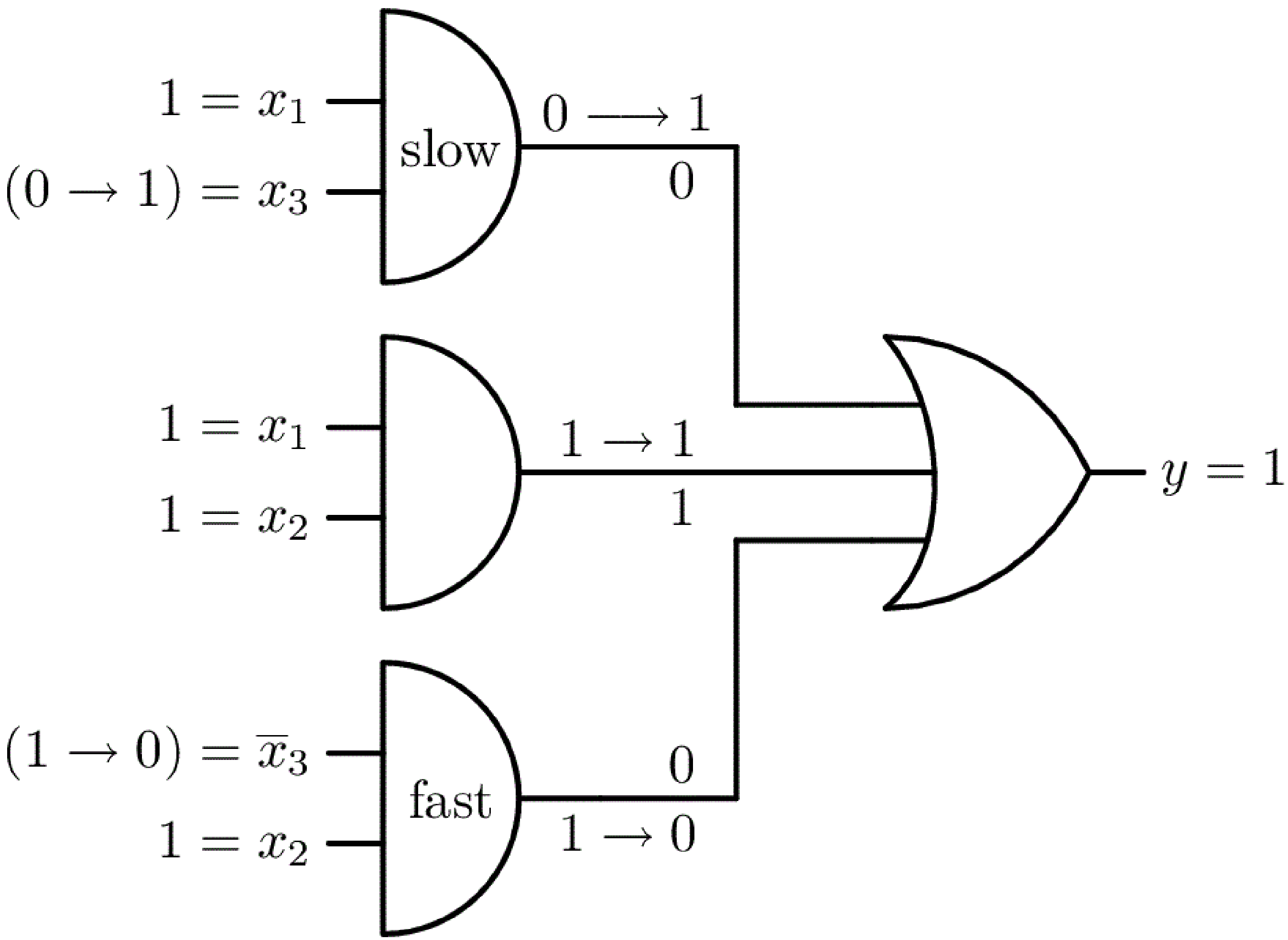
$x_1x_2 \backslash x_3x_4$	00	01	11	10
00	0	0	0	0
01	1	1	0	0
11	1	1	1	1
10	0	0	1	1

y

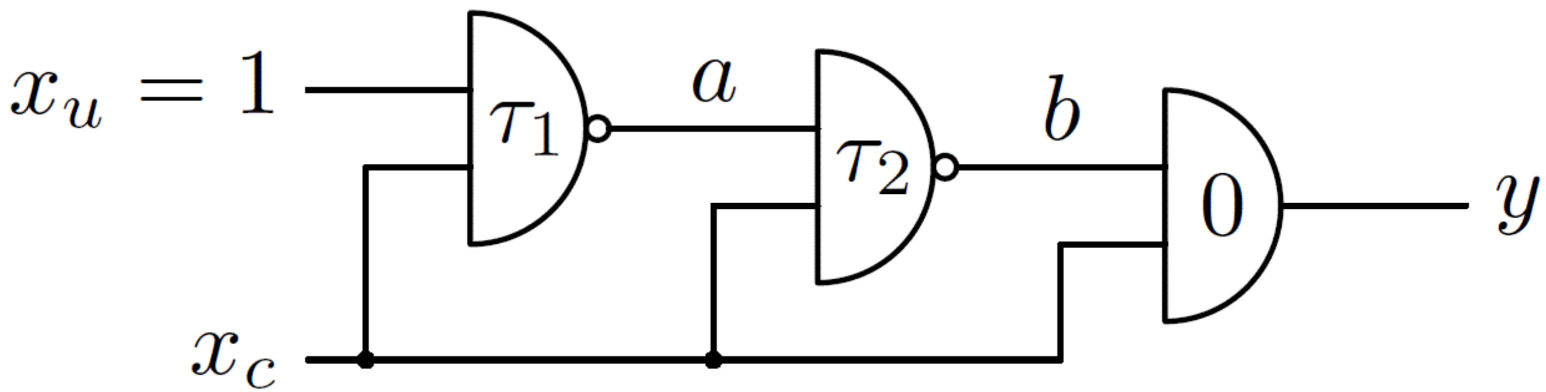
$$y = x_1x_3 + x_2\overline{x}_3 + (x_1x_2)$$

⇨ redundancy

The corrected circuit



Dynamic hazard

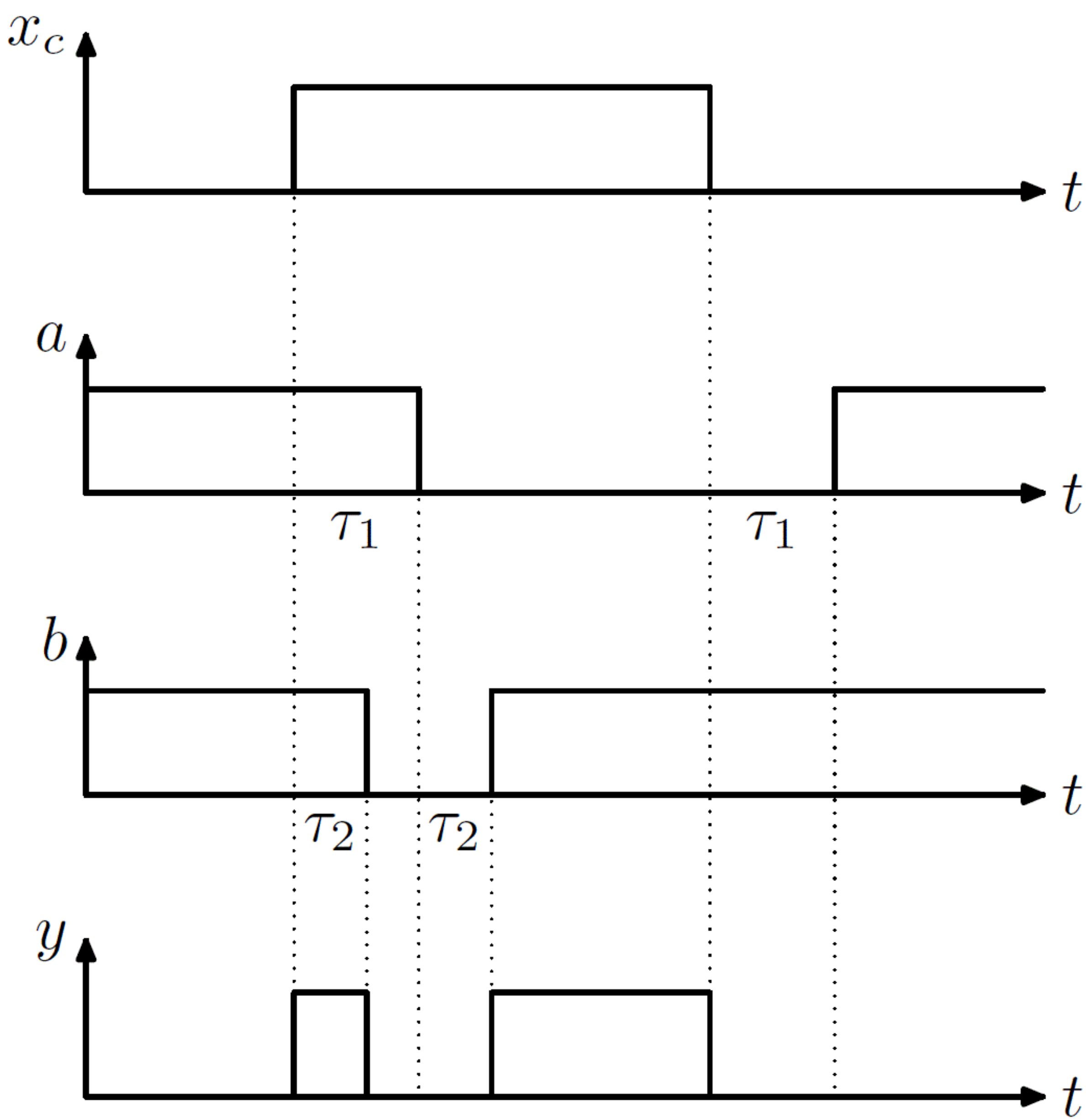


$$x_u = 1 \;\Rightarrow\; y = x_c$$

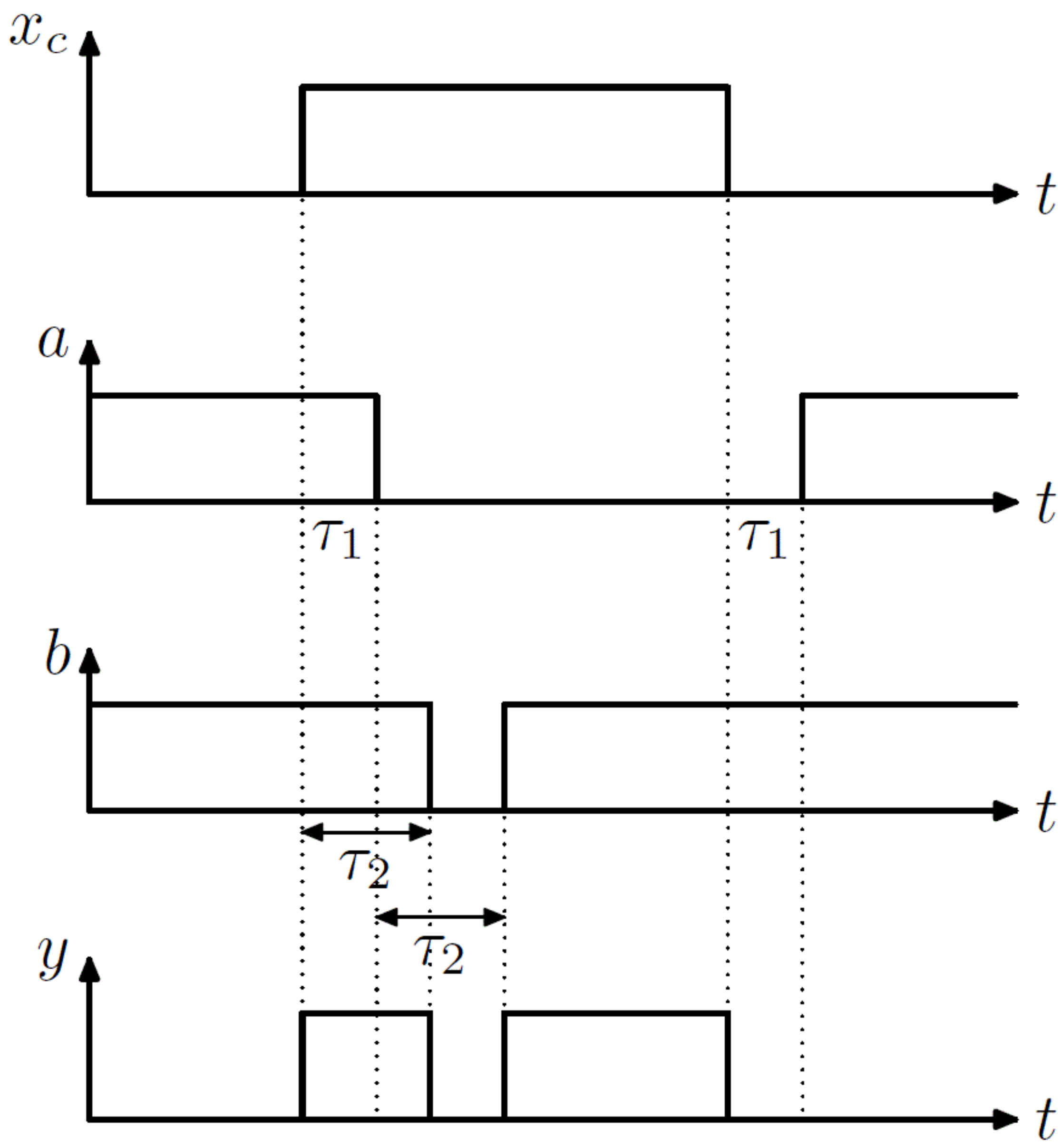
Let $x_c = 0 \nearrow 1 \searrow 0$

$$
\begin{aligned}
y &= \overline{\overline{x_u x_c}\; x_c}\; x_c \\
&= \overline{(\overline{x}_u + \overline{x}_c) x_c}\; x_c \\
&= \overline{(\overline{x}_u x_c + \overline{x}_c x_c)}\; x_c \\
&= \overline{(\overline{x}_u x_c + 0)}\; x_c \\
&= \overline{(\overline{x}_u x_c)}\; x_c \\
&= (x_u + \overline{x}_c)\; x_c \\
&= x_u x_c + \overline{x}_c x_c \\
&= x_u x_c + 0 \\
&= x_u x_c
\end{aligned}
$$

Time plots for $\tau_1 > \tau_2$



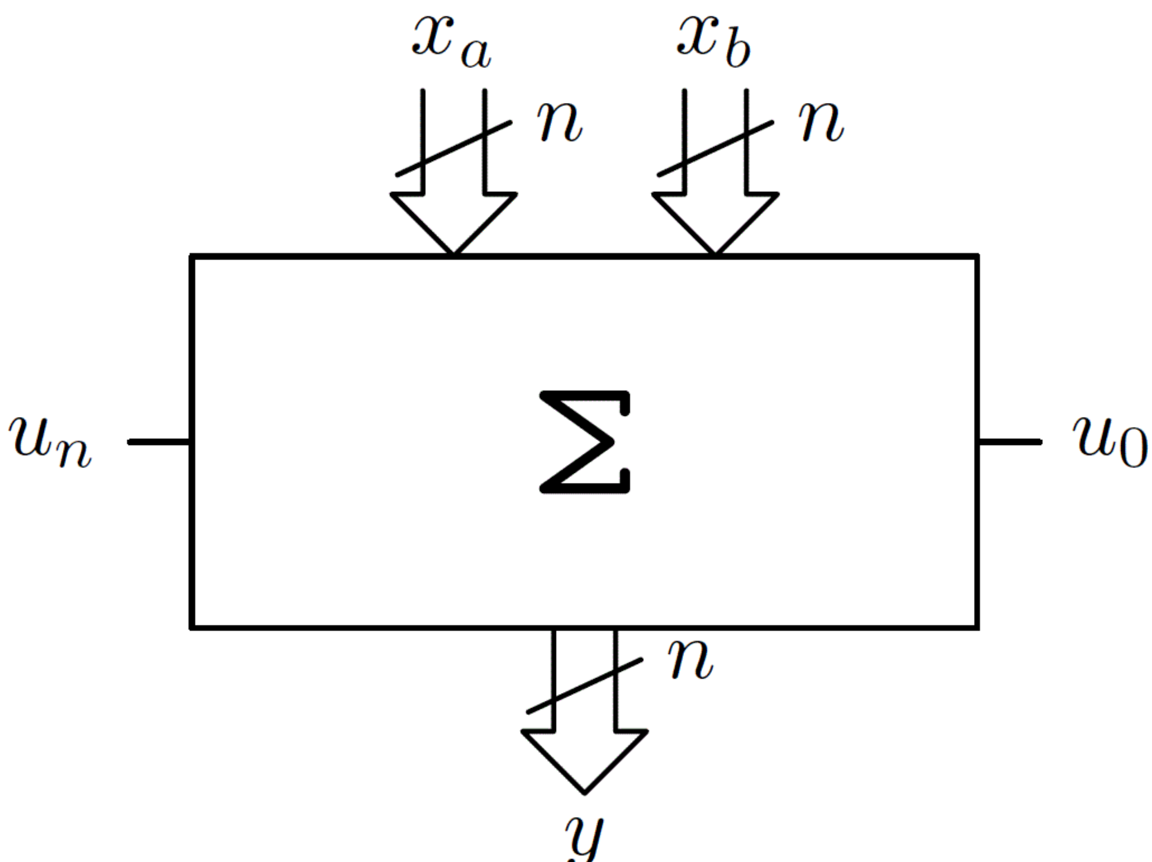
Time plots for $\tau_1 < \tau_2$



Iterative circuits

Example:

n-bit adder

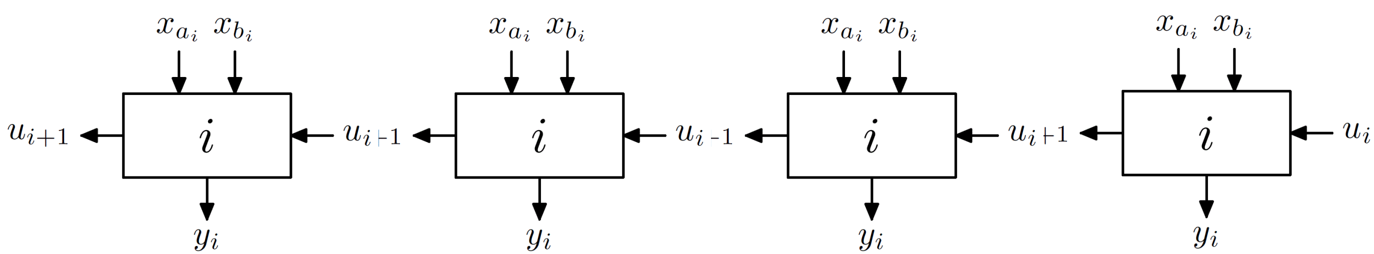


$\Rightarrow$ n-bit adder has $2n+1$ inputs and $n+1$ outputs

$\Rightarrow$ huge Karnaugh tables for large n

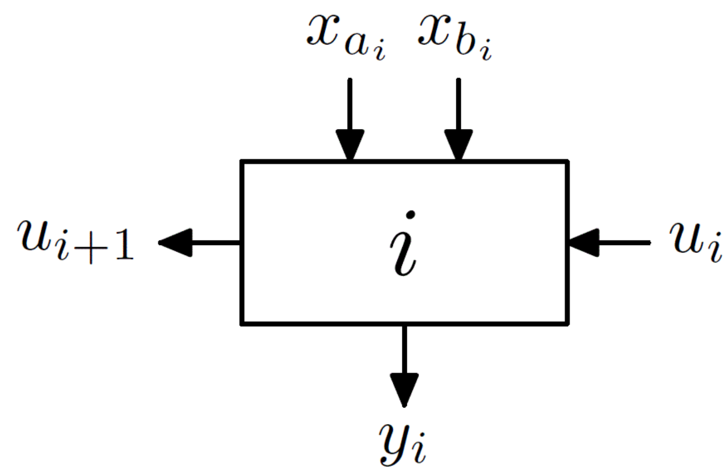
$\Rightarrow$ partition the circuit

X_3 X_2 X_1 X_0



$$
\begin{array}{rr} & \boxed{u_i} \\ + & x_{a_i} \\ + & x_{b_i} \\ \hline \boxed{u_{i+1}} & y_i \end{array}
\quad
\begin{array}{rr} & \boxed{0} \\ + & 0 \\ + & 0 \\ \hline \boxed{0} & 0 \end{array}
\quad
\begin{array}{rr} & \boxed{0} \\ + & 0 \\ + & 1 \\ \hline \boxed{0} & 1 \end{array}
\quad
\begin{array}{rr} & \boxed{0} \\ + & 1 \\ + & 0 \\ \hline \boxed{0} & 1 \end{array}
\quad
\begin{array}{rr} & \boxed{0} \\ + & 1 \\ + & 1 \\ \hline \boxed{1} & 0 \end{array}
$$

$$
\begin{array}{rr} & \boxed{u_i} \\ + & x_{a_i} \\ + & x_{b_i} \\ \hline \boxed{u_{i+1}} & y_i \end{array}
\quad
\begin{array}{rr} & \boxed{1} \\ + & 0 \\ + & 0 \\ \hline \boxed{0} & 1 \end{array}
\quad
\begin{array}{rr} & \boxed{1} \\ + & 0 \\ + & 1 \\ \hline \boxed{1} & 0 \end{array}
\quad
\begin{array}{rr} & \boxed{1} \\ + & 1 \\ + & 0 \\ \hline \boxed{1} & 0 \end{array}
\quad
\begin{array}{rr} & \boxed{1} \\ + & 1 \\ + & 1 \\ \hline \boxed{1} & 1 \end{array}
$$



$x_{a_i}x_{b_i}$ \ u_i	0	1
00	0	0
01	0	1
11	1	1
10	0	1

u_{i+1}

$x_{a_i}x_{b_i}$ \ u_i	0	1
00	0	1
01	1	0
11	0	1
10	1	0

y_i

$$
\begin{cases}
u_{i+1} = x_{a_i}x_{b_i} + u_i x_{a_i} + u_i x_{b_i} \\
y_i = u_i\overline{x}_{a_i}\overline{x}_{b_i} + u_i x_{a_i} x_{b_i} + \overline{u}_i\overline{x}_{a_i} x_{b_i} + \overline{u}_i x_{a_i}\overline{x}_{b_i} \\
\quad = u_i(\,\overline{x_{a_i} \oplus x_{b_i}}\,) + \overline{u}_i(x_{a_i} \oplus x_{b_i}) \\
\quad = u_i \oplus (x_{a_i} \oplus x_{b_i})
\end{cases}
$$

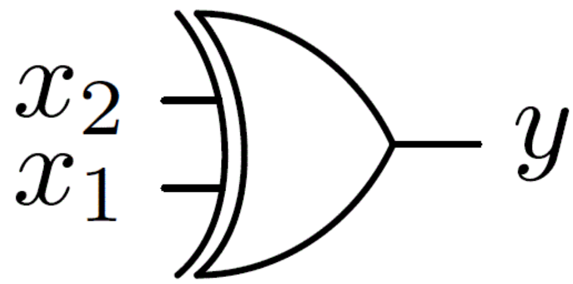
XOR gate

Truth table

$x_2 \backslash x_1$	0	1
0	0	1
1	1	0

y

Symbol



$$y = x_1 \oplus x_2 = x_1\overline{x}_2 + \overline{x}_1 x_2$$

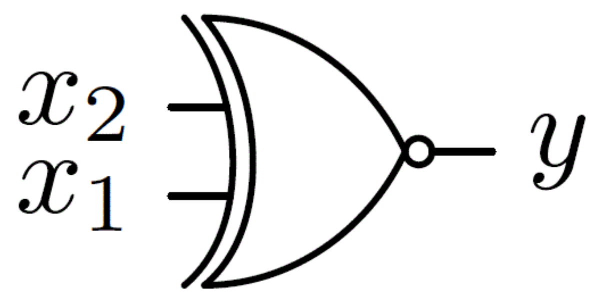
Not XOR gate

Truth table

$x_2 \backslash x_1$	0	1
0	1	0
1	0	1

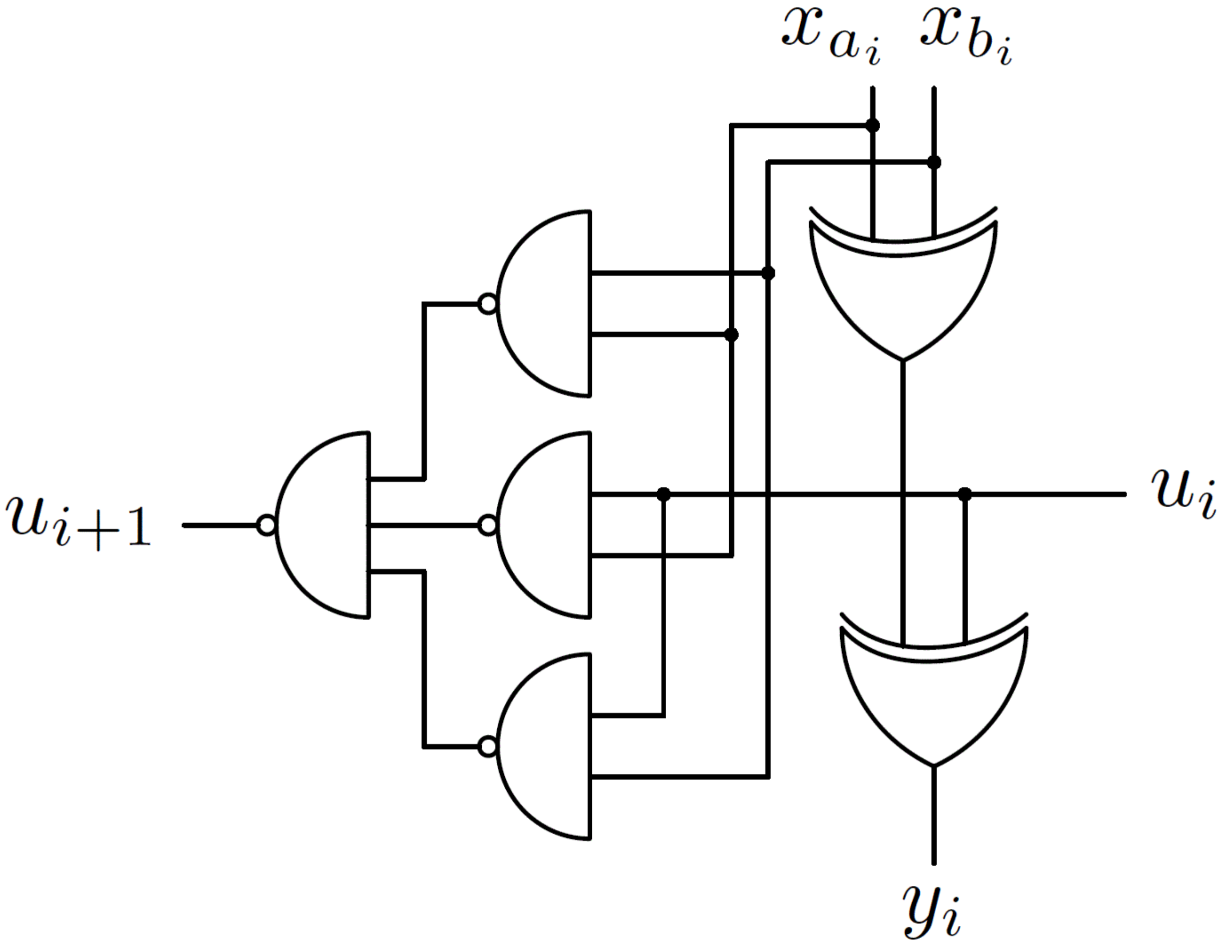
y

Symbol

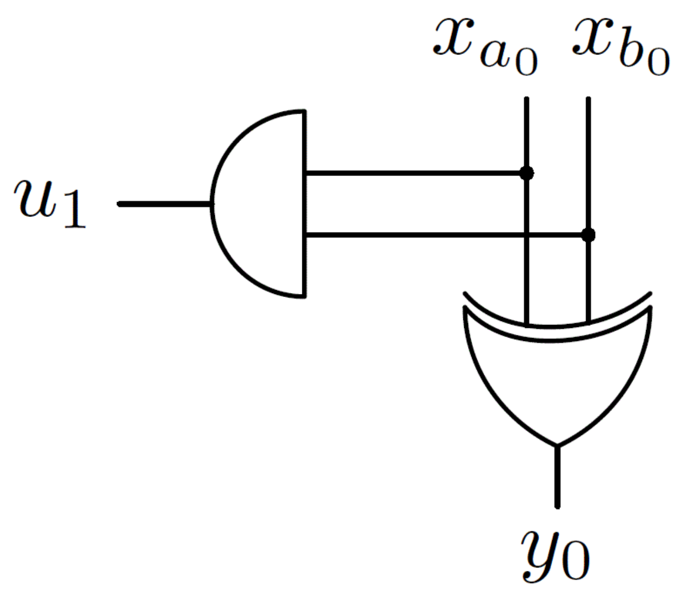


$$y = (x_1 \equiv x_2) = \overline{x_1 \oplus x_2} = \overline{x}_1\overline{x}_2 + x_1x_2$$

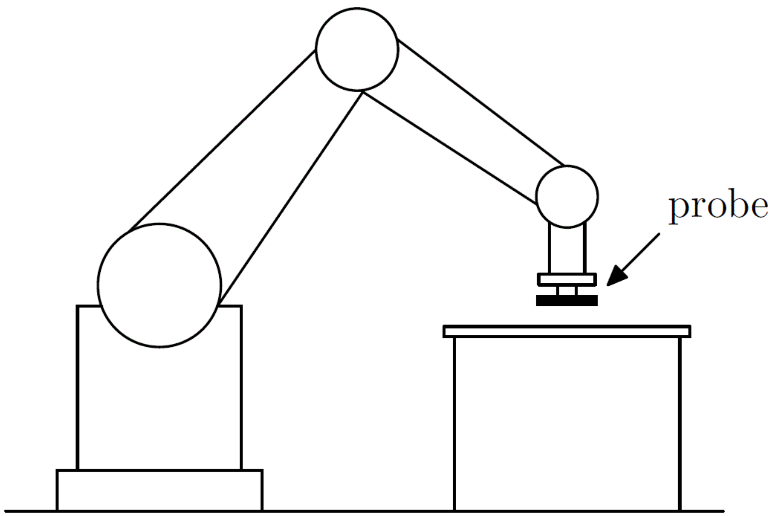
Block i = 0, … ,*n*-1

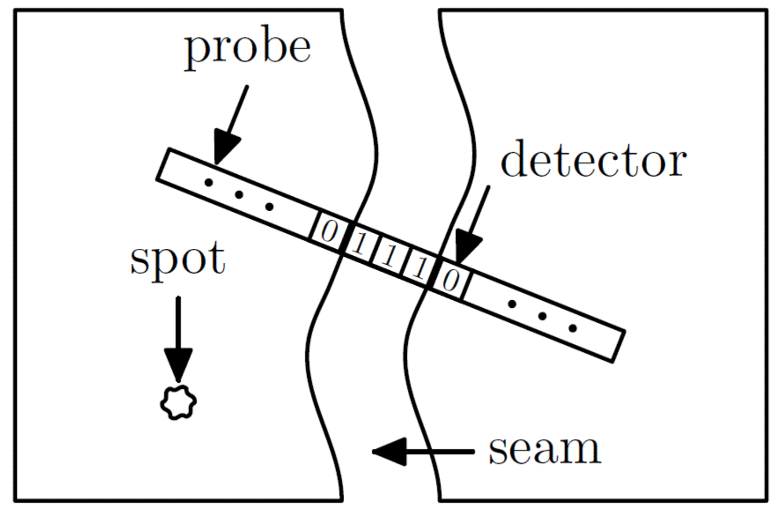


For block i = 0 $\Longrightarrow$ $u_0 = 0$ $\Longrightarrow$



Welding seam detection robot

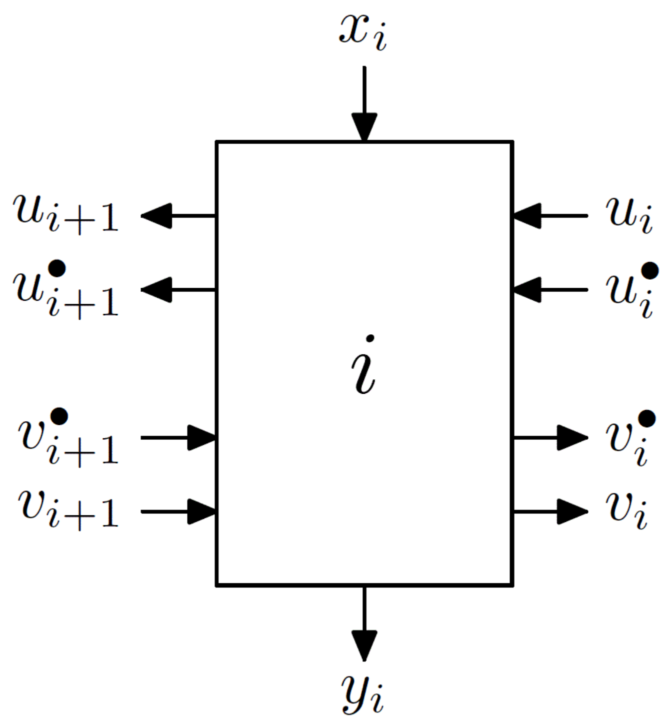




<u>The task:</u>

- Detect the middle 1 of three separate consecutive 1s
  - separate ⇒ bounded by 0s on both sides
  - less than three 1s ⇒ noise
  - more than three 1s ⇒ seam too wide
- The probe houses n detectors

$$\begin{cases} y_i &= f_1(x_i, u_i, u_i^{\bullet}, v_{i+1}, v_{i+1}^{\bullet}) \\ u_{i+1} &= f_2(x_i, u_i, u_{i^{\bullet}}) \\ u_{i+1}^{\bullet} &= f_3(x_i, u_i, u_i^{\bullet}) \\ v_i &= f_4(x_i, v_{i+1}, v_{i+1}^{\bullet}) \\ v_i^{\bullet} &= f_5(x_i, v_{i+1}, v_{i+1}^{\bullet}) \end{cases}$$



$$\ldots\ 0\ 1\ \boxed{1}\ 1\ 0\ \ldots$$

to the left	v_{i+1}	$v_{i+1}^{\bullet}$
$\ldots 0$	0	0
$\ldots 01$	0	1
$\ldots 01 \ldots 1$	1	1
forbidden	1	0

u_i	$u_i^{\bullet}$	to the right
0	0	$0 \ldots$
1	0	$10 \ldots$
1	1	$1 \ldots 10 \ldots$
0	1	forbidden

y_i

$v_{i+1}v^{\bullet}_{i+1}$ \ $x_iu_iu^{\bullet}_i$	000	001	011	010	110	111	101	100
00	0	–	0	0	0	0	–	0
01	0	–	0	0	$\boxed{1}$	0	–	0
11	0	–	0	0	0	0	–	0
10	–	–	–	–	–	–	–	–

$u^{\bullet}_{i+1}$

$u_iu^{\bullet}_i$ \ x_i	0	1
00	0	0
01	–	–
11	0	1
10	0	1

v_i

$v_{i+1}v^{\bullet}_{i+1}$ \ x_i	0	1
00	0	0
01	0	1
11	0	1
10	–	–

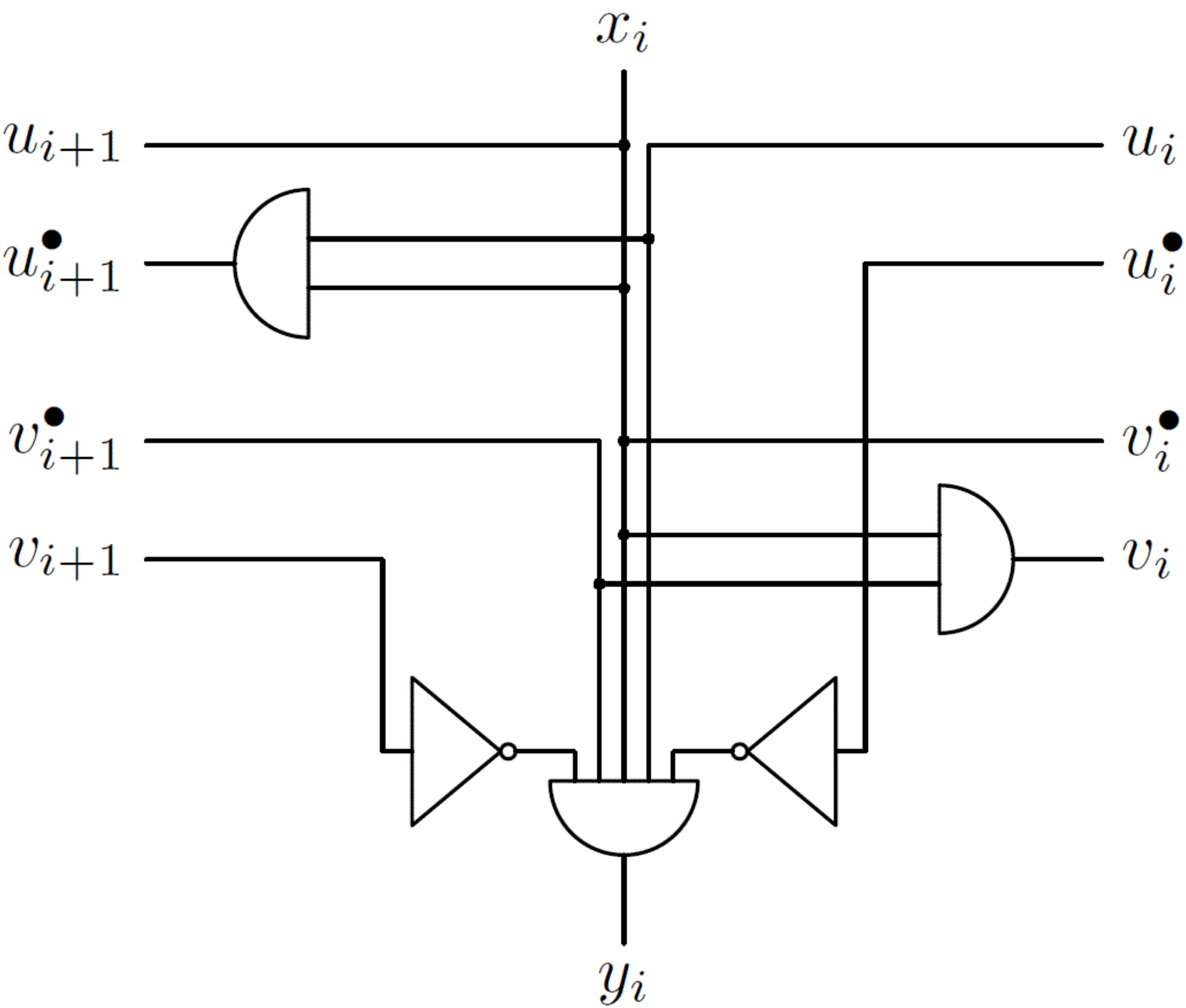
$v^{\bullet}_i$

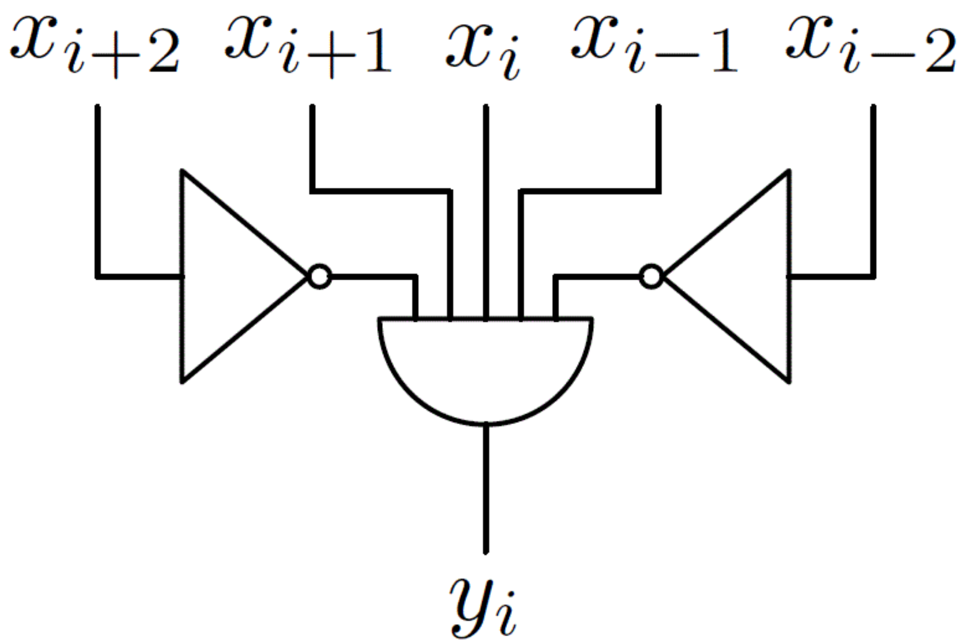
$v_{i+1}v^{\bullet}_{i+1}$ \ x_i	0	1
00	0	1
01	0	1
11	0	1
10	–	–

u_{i+1}

$u_iu^{\bullet}_i$ \ x_i	0	1
00	0	1
01	–	–
11	0	1
10	0	1

$$\begin{cases} y_i & = \overline{v}_{i+1} v^{\bullet}_{i+1} x_i u_i \overline{u}^{\bullet}_i \\ u_{i+1} & = x_i \\ u^{\bullet}_{i+1} & = x_i u_i \\ v_i & = x_i v^{\bullet}_{i+1} \\ v^{\bullet}_i & = x_i \end{cases}$$


x_i
u_{i+1}
u_i
$u^{\bullet}_{i+1}$
$u^{\bullet}_i$
$v^{\bullet}_{i+1}$
$v^{\bullet}_i$
v_{i+1}
v_i
y_i


x_{i+2}
x_{i+1}
x_i
x_{i-1}
x_{i-2}
y_i

Combinational logic utilising multiplexers

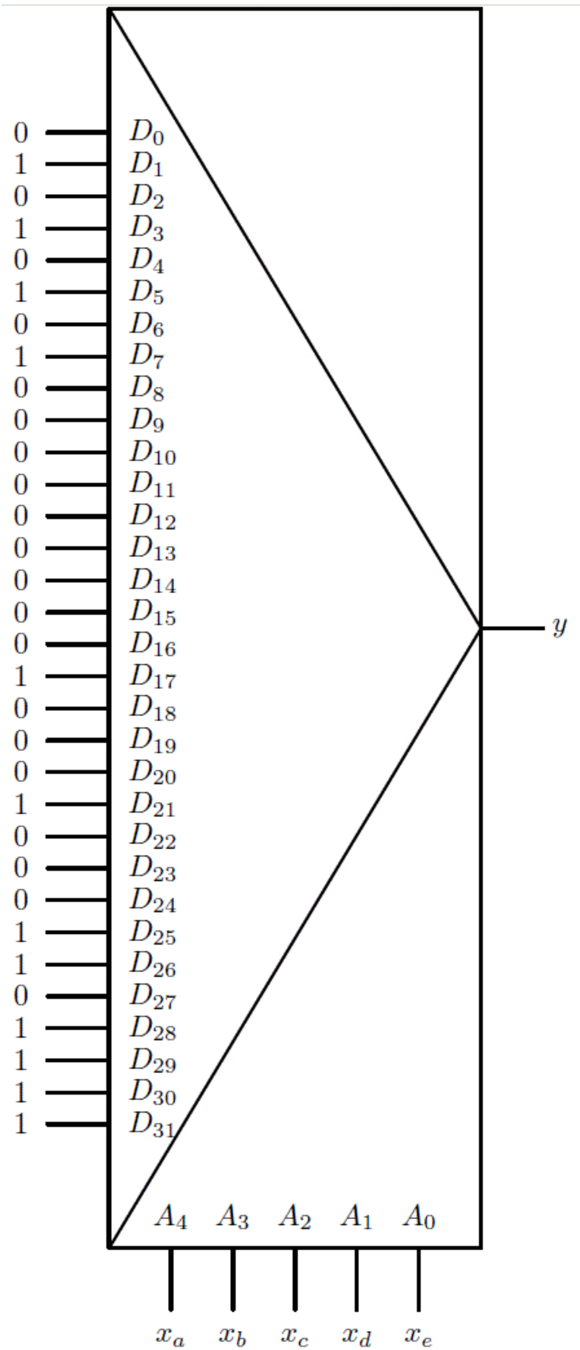
$$y = \sum \left(1, 3, 5, 7, 17, 21, 25, 26, 28, 29, 30, 31\right)$$

MUX5

Decompose the function in the following manner:

$$\begin{aligned}
y &= f_y(x_a, x_b, x_c, x_d, x_e) \\
&= \overline{x}_a\overline{x}_b\overline{x}_c\overline{x}_d\overline{x}_e f_y(0,0,0,0,0) + \overline{x}_a\overline{x}_b\overline{x}_c\overline{x}_d x_e f_y(0,0,0,0,1) + \\
&\quad \overline{x}_a\overline{x}_b\overline{x}_c x_d\overline{x}_e f_y(0,0,0,1,0) + \overline{x}_a\overline{x}_b\overline{x}_c x_d x_e f_y(0,0,0,1,1) + \\
&\quad \overline{x}_a\overline{x}_b x_c\overline{x}_d\overline{x}_e f_y(0,0,1,0,0) + \overline{x}_a\overline{x}_b x_c\overline{x}_d x_e f_y(0,0,1,0,1) + \\
&\quad \overline{x}_a\overline{x}_b x_c x_d\overline{x}_e f_y(0,0,1,1,0) + \overline{x}_a\overline{x}_b x_c x_d x_e f_y(0,0,1,1,1) +
\end{aligned}$$

$$\overline{x}_a x_b \overline{x}_c \overline{x}_d \overline{x}_e f_y(0,1,0,0,0) \; + \; \overline{x}_a x_b \overline{x}_c \overline{x}_d x_e f_y(0,1,0,0,1) \; +$$
$$\overline{x}_a x_b \overline{x}_c x_d \overline{x}_e f_y(0,1,0,1,0) \; + \; \overline{x}_a x_b \overline{x}_c x_d x_e f_y(0,1,0,1,1) \; +$$
$$\overline{x}_a x_b x_c \overline{x}_d \overline{x}_e f_y(0,1,1,0,0) \; + \; \overline{x}_a x_b x_c \overline{x}_d x_e f_y(0,1,1,0,1) \; +$$
$$\overline{x}_a x_b x_c x_d \overline{x}_e f_y(0,1,1,1,0) \; + \; \overline{x}_a x_b x_c x_d x_e f_y(0,1,1,1,1) \; +$$
$$x_a \overline{x}_b \overline{x}_c \overline{x}_d \overline{x}_e f_y(1,0,0,0,0) \; + \; x_a \overline{x}_b \overline{x}_c \overline{x}_d x_e f_y(1,0,0,0,1) \; +$$
$$x_a \overline{x}_b \overline{x}_c x_d \overline{x}_e f_y(1,0,0,1,0) \; + \; x_a \overline{x}_b \overline{x}_c x_d x_e f_y(1,0,0,1,1) \; +$$
$$x_a \overline{x}_b x_c \overline{x}_d \overline{x}_e f_y(1,0,1,0,0) \; + \; x_a \overline{x}_b x_c \overline{x}_d x_e f_y(1,0,1,0,1) \; +$$
$$x_a \overline{x}_b x_c x_d \overline{x}_e f_y(1,0,1,1,0) \; + \; x_a \overline{x}_b x_c x_d x_e f_y(1,0,1,1,1) \; +$$
$$x_a x_b \overline{x}_c \overline{x}_d \overline{x}_e f_y(1,1,0,0,0) \; + \; x_a x_b \overline{x}_c \overline{x}_d x_e f_y(1,1,0,0,1) \; +$$
$$x_a x_b \overline{x}_c x_d \overline{x}_e f_y(1,1,0,1,0) \; + \; x_a x_b \overline{x}_c x_d x_e f_y(1,1,0,1,1) \; +$$
$$x_a x_b x_c \overline{x}_d \overline{x}_e f_y(1,1,1,0,0) \; + \; x_a x_b x_c \overline{x}_d x_e f_y(1,1,1,0,1) \; +$$


0 D_0
1 D_1
0 D_2
1 D_3
0 D_4
1 D_5
0 D_6
1 D_7
0 D_8
0 D_9
0 D_{10}
0 D_{11}
0 D_{12}
0 D_{13}
0 D_{14}
0 D_{15}
0 D_{16}
1 D_{17}
0 D_{18}
0 D_{19}
0 D_{20}
1 D_{21}
0 D_{22}
0 D_{23}
0 D_{24}
1 D_{25}
1 D_{26}
0 D_{27}
1 D_{28}
1 D_{29}
1 D_{30}
1 D_{31}
y
A_4 A_3 A_2 A_1 A_0
x_a x_b x_c x_d x_e

MUX 4

$x_a x_b$ \ $x_c x_d x_e$	000	001	011	010	110	111	101	100
00	0	1	1	0	0	1	1	0
01	0	0	0	0	0	0	0	0
11	0	1	0	1	1	1	1	1
10	0	1	0	0	0	0	1	0

y

$$
\begin{aligned}
y &= f_y(x_a, x_b, x_c, x_d, x_e) \\
&= \overline{x}_a \overline{x}_b x_e + x_a \overline{x}_d x_e + x_a x_b x_c + x_a x_b x_d \overline{x}_e
\end{aligned}
$$

$$
F_y^1 = \left\{ \begin{array}{ccccc}
x_a & x_b & x_c & x_d & x_e \\
0 & 0 & - & - & 1 \\
1 & - & - & 0 & 1 \\
1 & 1 & 1 & - & - \\
1 & 1 & - & 1 & 0
\end{array} \right\}
$$

Choose x's with least "–" as address inputs

$\Rightarrow x_a,\ x_b,\ x_d,\ x_e \Rightarrow x_c$ becomes a data input.

$$
\begin{aligned}
y \; = \; & \overline{x}_a\overline{x}_b\overline{x}_d\overline{x}_e f_y(0,0,x_c,0,0) \; + \; \overline{x}_a\overline{x}_b\overline{x}_d x_e f_y(0,0,x_c,0,1) \; + \\
& \overline{x}_a\overline{x}_b x_d\overline{x}_e f_y(0,0,x_c,1,0) \; + \; \overline{x}_a\overline{x}_b x_d x_e f_y(0,0,x_c,1,1) \; + \\
& \overline{x}_a x_b\overline{x}_d\overline{x}_e f_y(0,1,x_c,0,0) \; + \; \overline{x}_a x_b\overline{x}_d x_e f_y(0,1,x_c,0,1) \; + \\
& \overline{x}_a x_b x_d\overline{x}_e f_y(0,1,x_c,1,0) \; + \; \overline{x}_a x_b x_d x_e f_y(0,1,x_c,1,1) \; + \\
& x_a\overline{x}_b\overline{x}_d\overline{x}_e f_y(1,0,x_c,0,0) \; + \; x_a\overline{x}_b\overline{x}_d x_e f_y(1,0,x_c,0,1) \; + \\
& x_a\overline{x}_b x_d\overline{x}_e f_y(1,0,x_c,1,0) \; + \; x_a\overline{x}_b x_d x_e f_y(1,0,x_c,1,1) \; + \\
& x_a x_b\overline{x}_d\overline{x}_e f_y(1,1,x_c,0,0) \; + \; x_a x_b\overline{x}_d x_e f_y(1,1,x_c,0,1) \; + \\
& x_a x_b x_d\overline{x}_e f_y(1,1,x_c,1,0) \; + \; x_a x_b x_d x_e f_y(1,1,x_c,1,1)
\end{aligned}
$$

$$f_y(0,0,x_c,0,0) = \begin{cases} 0 & \text{for } x_c = 0 \\ 0 & \text{for } x_c = 1 \end{cases} \qquad f_y(1,0,x_c,0,0) = \begin{cases} 0 & \text{for } x_c = 0 \\ 0 & \text{for } x_c = 1 \end{cases}$$

$$f_y(0,0,x_c,0,1) = \begin{cases} 1 & \text{for } x_c = 0 \\ 1 & \text{for } x_c = 1 \end{cases} \qquad f_y(1,0,x_c,0,1) = \begin{cases} 1 & \text{for } x_c = 0 \\ 1 & \text{for } x_c = 1 \end{cases}$$

$$f_y(0,0,x_c,1,0) = \begin{cases} 0 & \text{for } x_c = 0 \\ 0 & \text{for } x_c = 1 \end{cases} \qquad f_y(1,0,x_c,1,0) = \begin{cases} 0 & \text{for } x_c = 0 \\ 0 & \text{for } x_c = 1 \end{cases}$$

$$f_y(0,0,x_c,1,1) = \begin{cases} 1 & \text{for } x_c = 0 \\ 1 & \text{for } x_c = 1 \end{cases} \qquad f_y(1,0,x_c,1,1) = \begin{cases} 0 & \text{for } x_c = 0 \\ 0 & \text{for } x_c = 1 \end{cases}$$

$$f_y(0,1,x_c,0,0) = \begin{cases} 0 & \text{for } x_c = 0 \\ 0 & \text{for } x_c = 1 \end{cases} \qquad f_y(1,1,x_c,0,0) = \begin{cases} 0 & \text{for } x_c = 0 \\ 1 & \text{for } x_c = 1 \end{cases}$$

$$f_y(0,1,x_c,0,1) = \begin{cases} 0 & \text{for } x_c = 0 \\ 0 & \text{for } x_c = 1 \end{cases} \qquad f_y(1,1,x_c,0,1) = \begin{cases} 1 & \text{for } x_c = 0 \\ 1 & \text{for } x_c = 1 \end{cases}$$

$$f_y(0,1,x_c,1,0) = \begin{cases} 0 & \text{for } x_c = 0 \\ 0 & \text{for } x_c = 1 \end{cases} \qquad f_y(1,1,x_c,1,0) = \begin{cases} 1 & \text{for } x_c = 0 \\ 1 & \text{for } x_c = 1 \end{cases}$$

$$f_y(0,1,x_c,1,1) = \begin{cases} 0 & \text{for } x_c = 0 \\ 0 & \text{for } x_c = 1 \end{cases} \qquad f_y(1,1,x_c,1,1) = \begin{cases} 0 & \text{for } x_c = 0 \\ 1 & \text{for } x_c = 1 \end{cases}$$

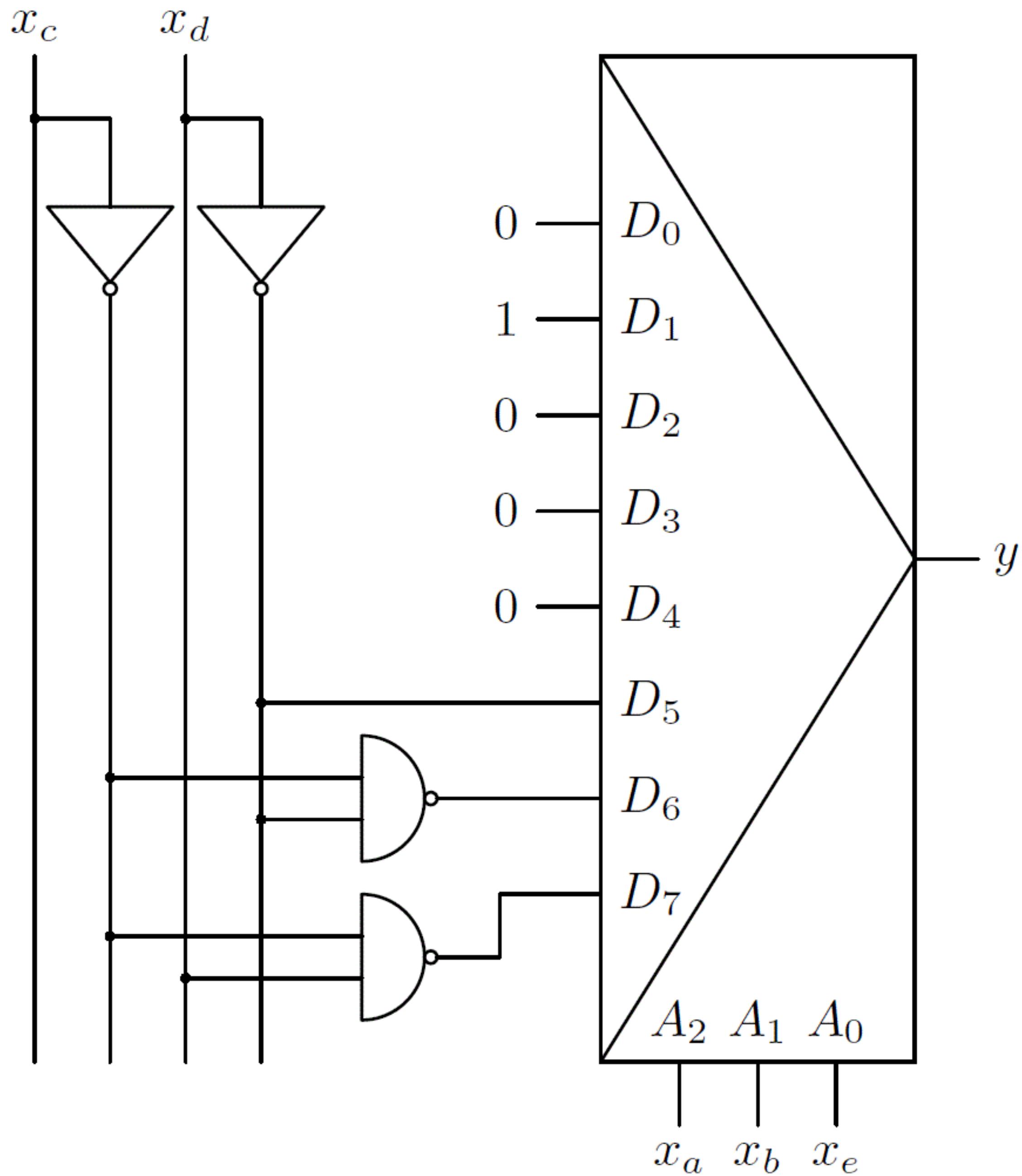
MUX3

Let x_a, x_b, x_e become address inputs
$\Rightarrow$ x_c and x_d become data inputs.

$$
\begin{aligned}
y = {} & \overline{x}_a\overline{x}_b\overline{x}_e f_y(0,0,x_c,x_d,0) + \overline{x}_a\overline{x}_b x_e f_y(0,0,x_c,x_d,1) + \\
& \overline{x}_a x_b\overline{x}_e f_y(0,1,x_c,x_d,0) + \overline{x}_a x_b x_e f_y(0,1,x_c,x_d,1) + \\
& x_a\overline{x}_b\overline{x}_e f_y(1,0,x_c,x_d,0) + x_a\overline{x}_b x_e f_y(1,0,x_c,x_d,1) + \\
& x_a x_b\overline{x}_e f_y(1,1,x_c,x_d,0) + x_a x_b x_e f_y(1,1,x_c,x_d,1)
\end{aligned}
$$

$$
\begin{aligned}
f_y(0,0,x_c,x_d,0) &= 0\\
f_y(0,0,x_c,x_d,1) &= 1\\
f_y(0,1,x_c,x_d,0) &= 0\\
f_y(0,1,x_c,x_d,1) &= 0\\
f_y(1,0,x_c,x_d,0) &= 0\\
f_y(1,0,x_c,x_d,1) &= \overline{x}_d\\
f_y(1,1,x_c,x_d,0) &= x_d + x_c\\
f_y(1,1,x_c,x_d,1) &= \overline{x}_d + x_c
\end{aligned}
$$

$$
F_y^1 = \left\{ \begin{array}{ccccc}
x_a & x_b & x_c & x_d & x_e \\
0 & 0 & - & - & 1 \\
1 & - & - & 0 & 1 \\
1 & 1 & 1 & - & - \\
1 & 1 & - & 1 & 0
\end{array} \right\}
$$


x_c
x_d
0
1
0
0
0
D_0
D_1
D_2
D_3
D_4
D_5
D_6
D_7
A_2 A_1 A_0
y
x_a x_b x_e

MUX 2

Let x_a, x_b become address inputs
$\Rightarrow x_c$, x_d and x_e become data inputs.

$$
\begin{aligned}
y \;=\; & \overline{x}_a\overline{x}_b f_y(0,0,x_c,x_d,x_e) \;+\; \overline{x}_a x_b f_y(0,1,x_c,x_d,x_e) \;+ \\
& x_a\overline{x}_b f_y(1,0,x_c,x_d,x_e) \;+\; x_a x_b f_y(1,1,x_c,x_d,x_e)
\end{aligned}
$$

$$
F_y^1 = \left\{ \begin{array}{ccccc}
x_a & x_b & x_c & x_d & x_e \\
0 & 0 & - & - & 1 \\
1 & - & - & 0 & 1 \\
1 & 1 & 1 & - & - \\
1 & 1 & - & 1 & 0
\end{array} \right\}
$$

$$
\begin{aligned}
f_y(0,0,x_c,x_d,x_e) &= x_e \\
f_y(0,1,x_c,x_d,x_e) &= 0 \\
f_y(1,0,x_c,x_d,x_e) &= \overline{x}_d x_e \\
f_y(1,1,x_c,x_d,x_e) &= x_c + \overline{x}_d x_e + x_d \overline{x}_e \;=\; x_c + (x_d \oplus x_e)
\end{aligned}
$$

MUX2

$$y=\bar{a}\bar{b}\mathrm{e} + \mathrm{a}\bar{d}\mathrm{e} + \mathrm{abc} + \mathrm{abd}\bar{e}$$

$$\mathrm{a}\bar{d}\mathrm{e} = \mathrm{a}\bar{b}\bar{d}\mathrm{e} + \mathrm{ab}\bar{d}\mathrm{e}$$

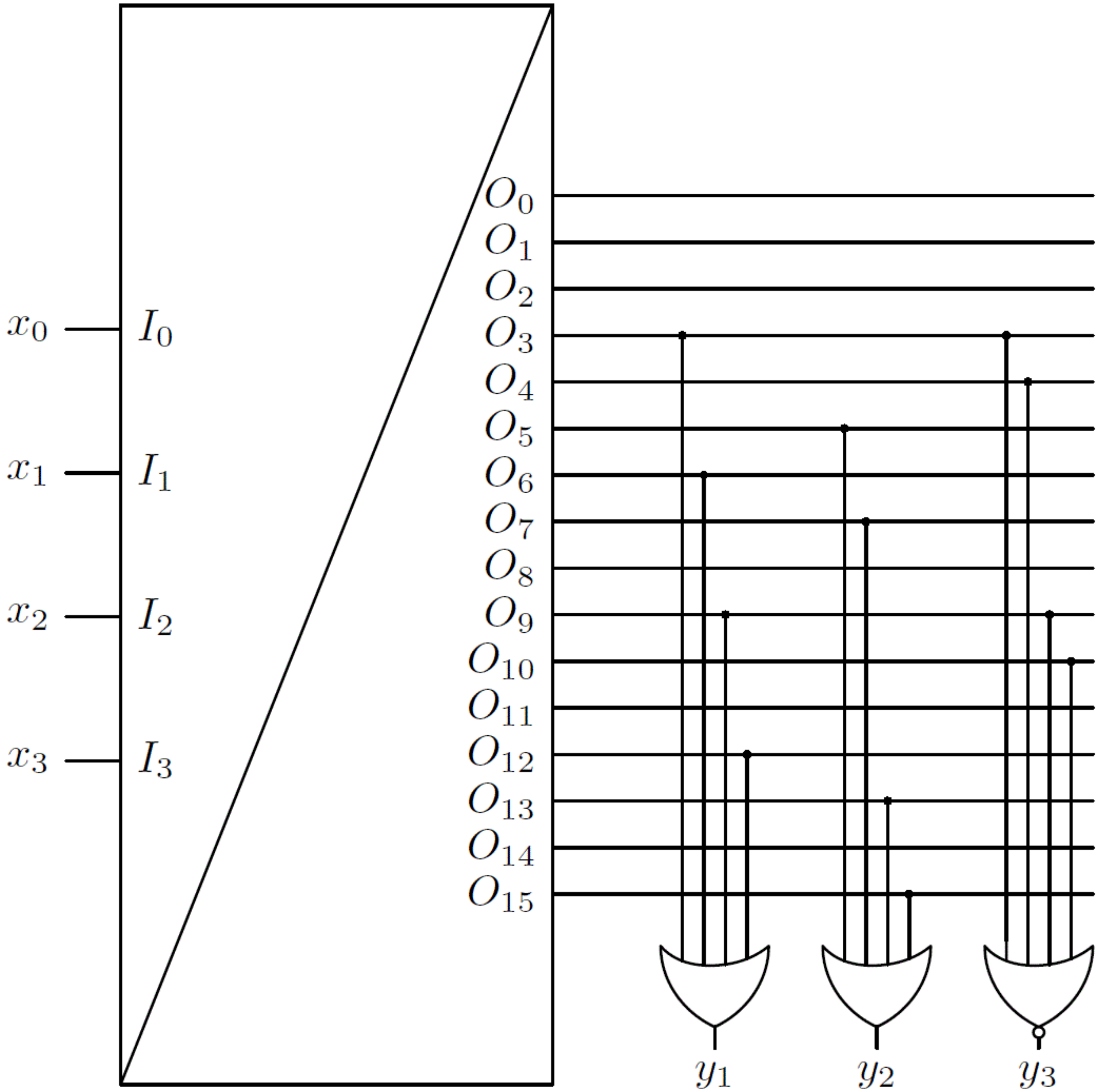
$$y=\bar{a}\bar{b}(\mathrm{e}) + \bar{a}\mathrm{b}(0) + \mathrm{a}\bar{b}(\bar{d}\mathrm{e}) + \mathrm{ab}(\mathrm{c} + \mathrm{d}\bar{e} + \bar{d}\mathrm{e})$$

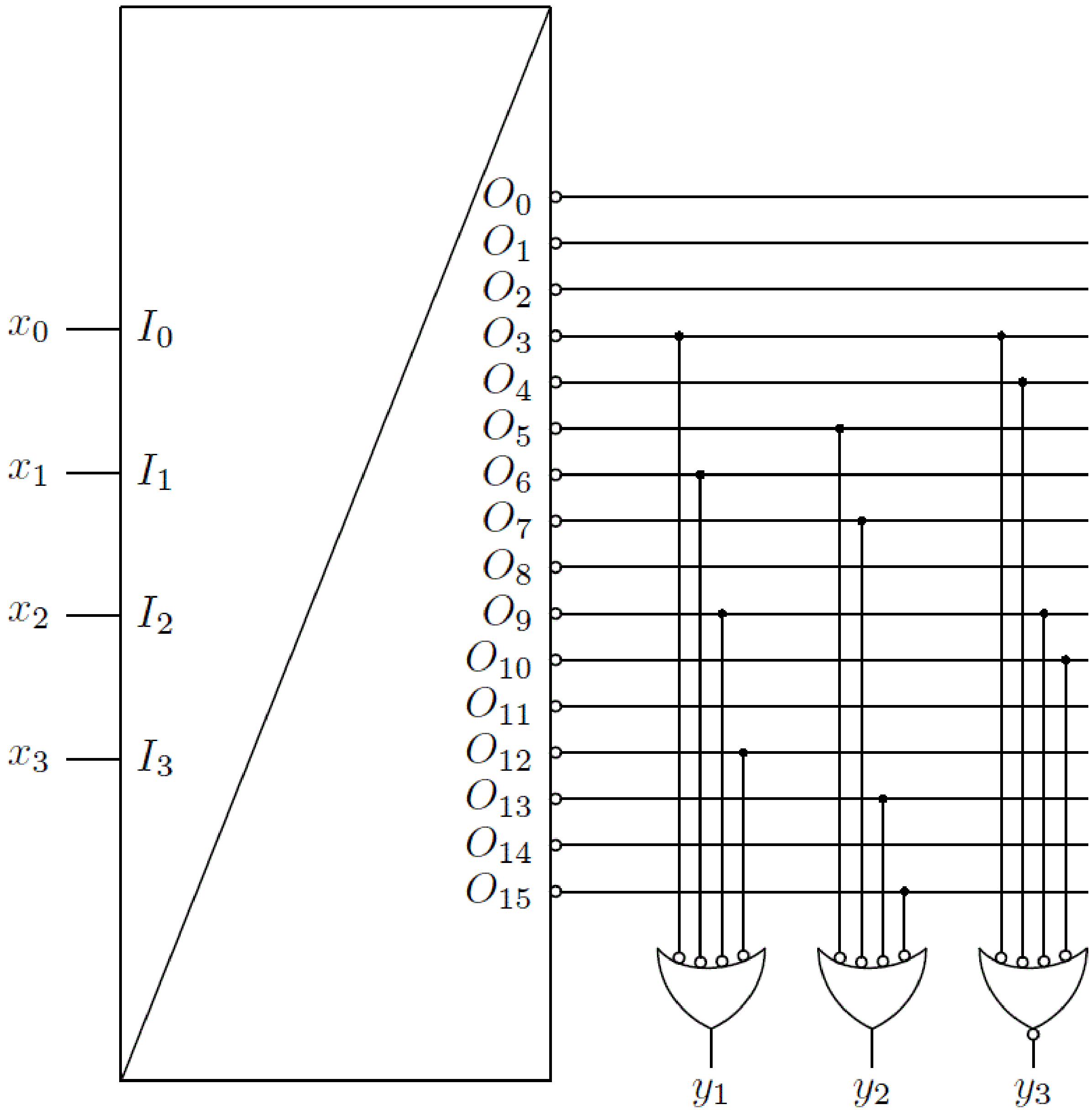
00	01	10	11	bin
0	1	2	3	dec

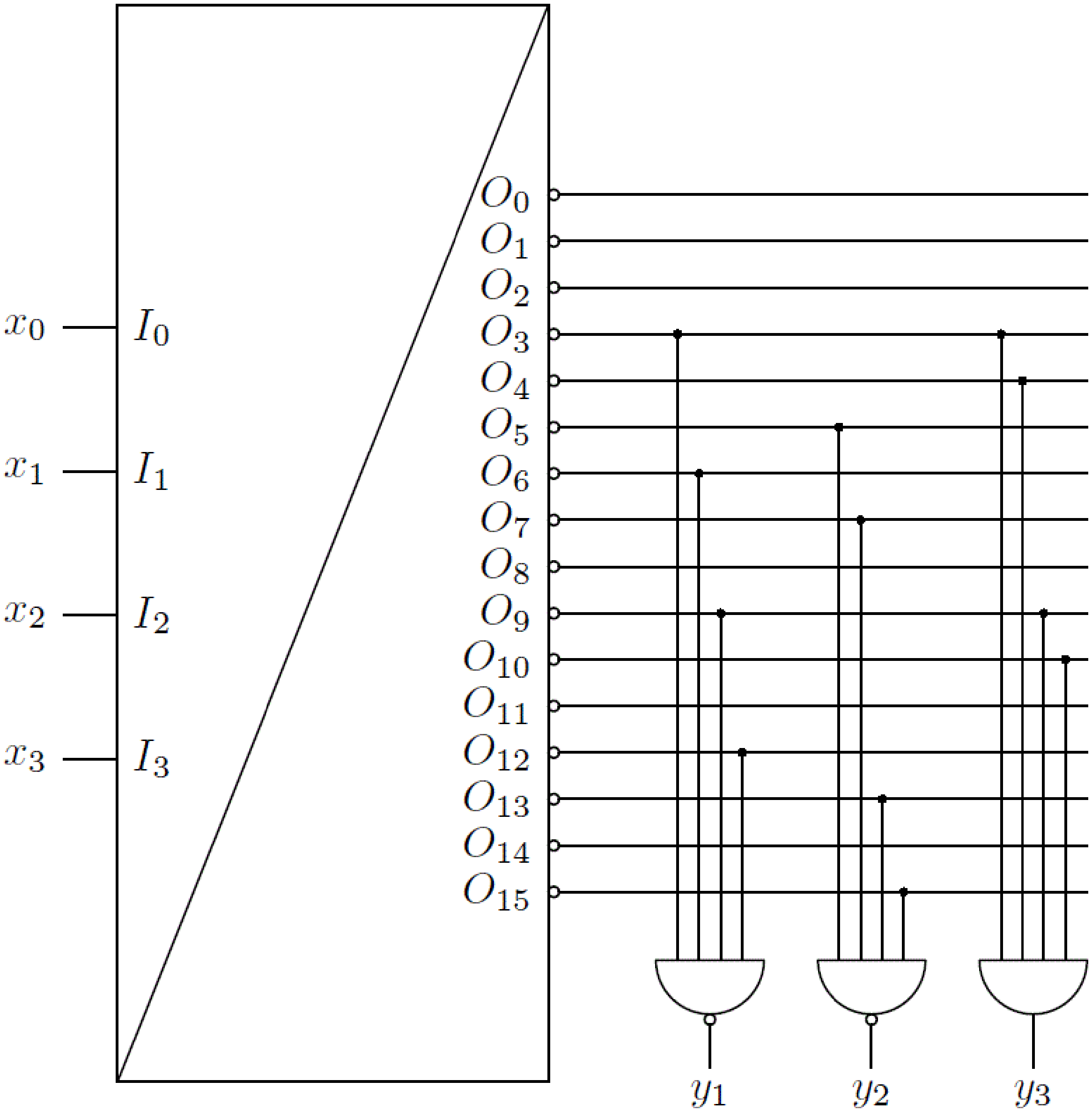
Implementation of combinational functions by using decoders

$$\begin{cases} y_1 &= \sum(3,6,9,12) \\ y_2 &= \sum(5,7,13,15) \\ y_3 &= \sum(0,1,2,3,6,7,8,11,12,13,14,15) \end{cases}$$

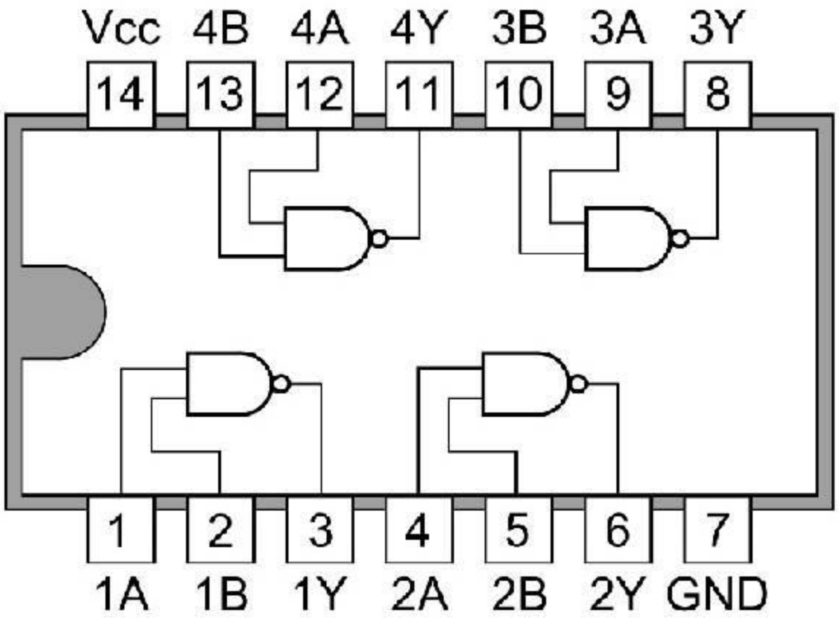
$$\overline{y}_3 = \sum(4,5,9,10)$$

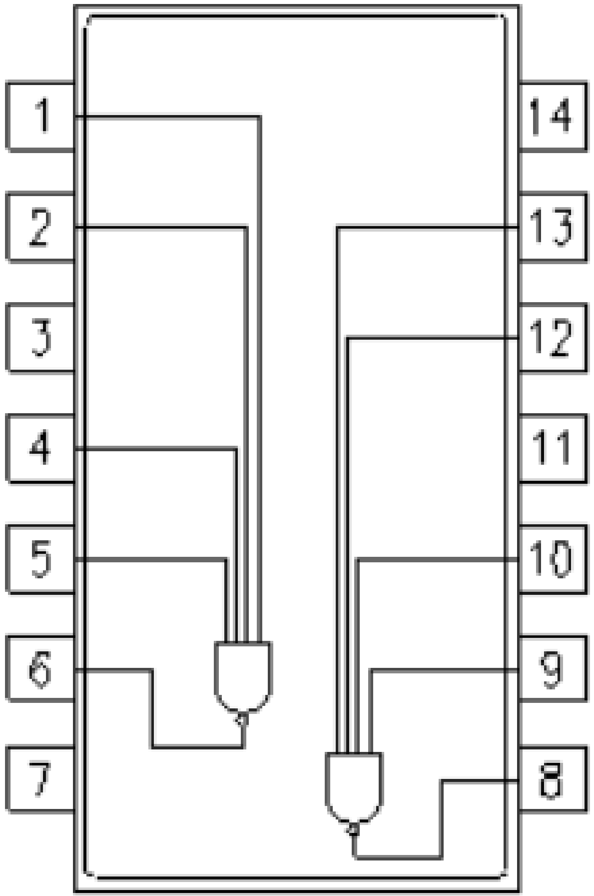

x_0
x_1
x_2
x_3
I_0
I_1
I_2
I_3
O_0
O_1
O_2
O_3
O_4
O_5
O_6
O_7
O_8
O_9
O_{10}
O_{11}
O_{12}
O_{13}
O_{14}
O_{15}
y_1
y_2
y_3


x_0
x_1
x_2
x_3
I_0
I_1
I_2
I_3
O_0
O_1
O_2
O_3
O_4
O_5
O_6
O_7
O_8
O_9
O_{10}
O_{11}
O_{12}
O_{13}
O_{14}
O_{15}
y_1
y_2
y_3


x_0
x_1
x_2
x_3
I_0
I_1
I_2
I_3
O_0
O_1
O_2
O_3
O_4
O_5
O_6
O_7
O_8
O_9
O_{10}
O_{11}
O_{12}
O_{13}
O_{14}
O_{15}
y_1
y_2
y_3

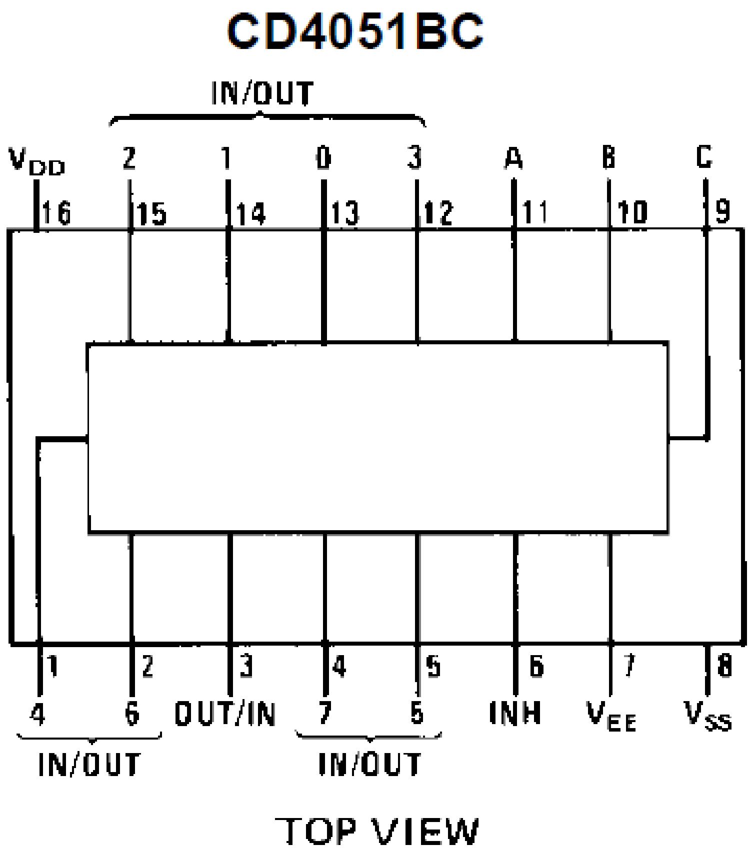
Small-scale Integrated Circuit


Vcc
4B
4A
4Y
3B
3A
3Y
14
13
12
11
10
9
8
1
2
3
4
5
6
7
1A
1B
1Y
2A
2B
2Y
GND



7440
Dual 4–Input
NAND Buffer

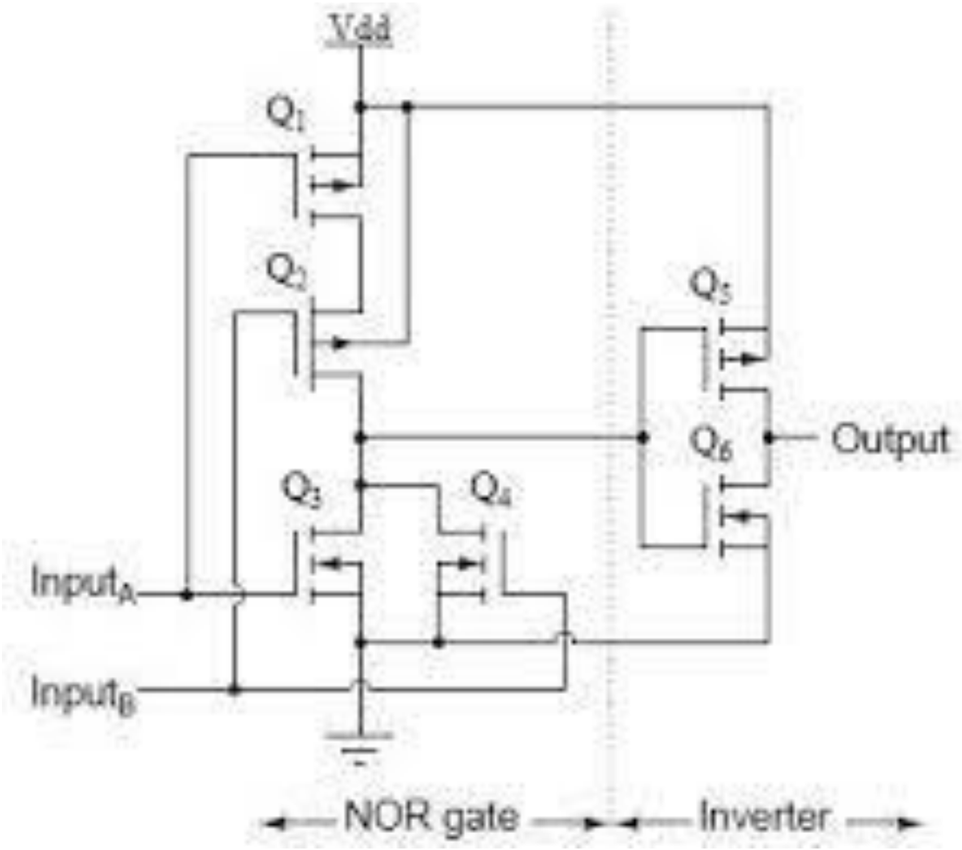
CMOS Multiplexer



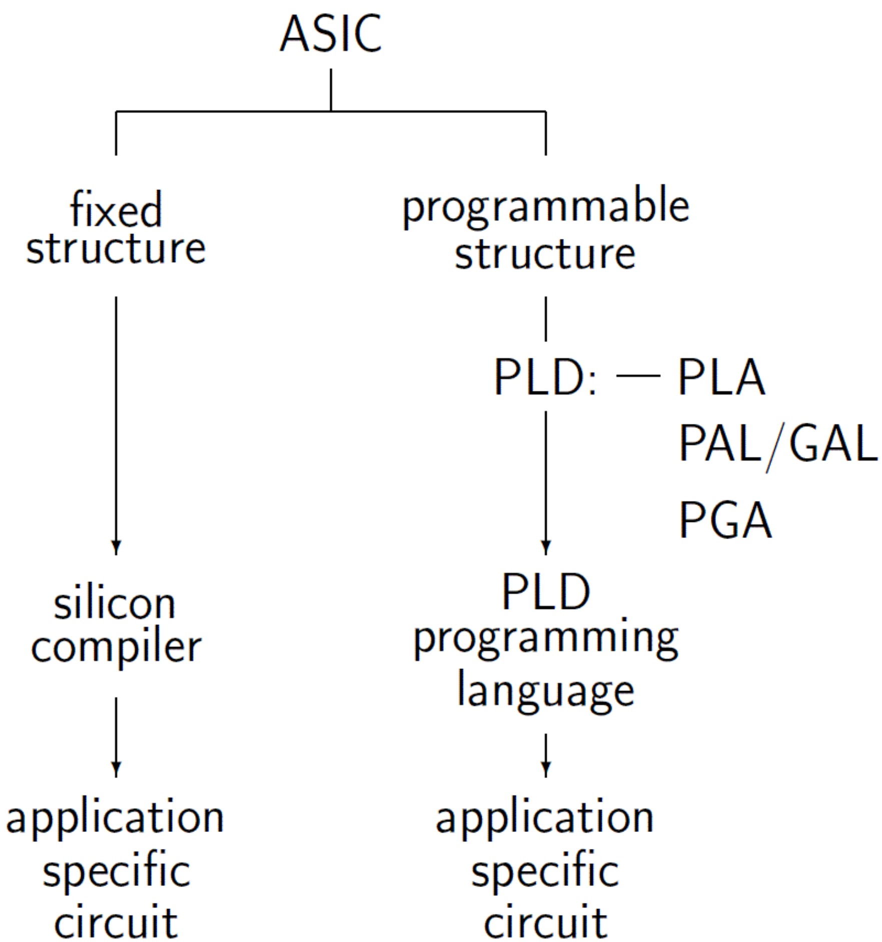
Truth Table

INPUT STATES				"ON" CHANNELS		
INHIBIT	C	B	A	CD4051B	CD4052B	CD4053B
0	0	0	0	0	0X, 0Y	cx, bx, ax
0	0	0	1	1	1X, 1Y	cx, bx, ay
0	0	1	0	2	2X, 2Y	cx, by, ax
0	0	1	1	3	3X, 3Y	cx, by, ay
0	1	0	0	4		cy, bx, ax
0	1	0	1	5		cy, bx, ay
0	1	1	0	6		cy, by, ax
0	1	1	1	7		cy, by, ay
1	*	*	*	NONE	NONE	NONE

CMOS OR Gate

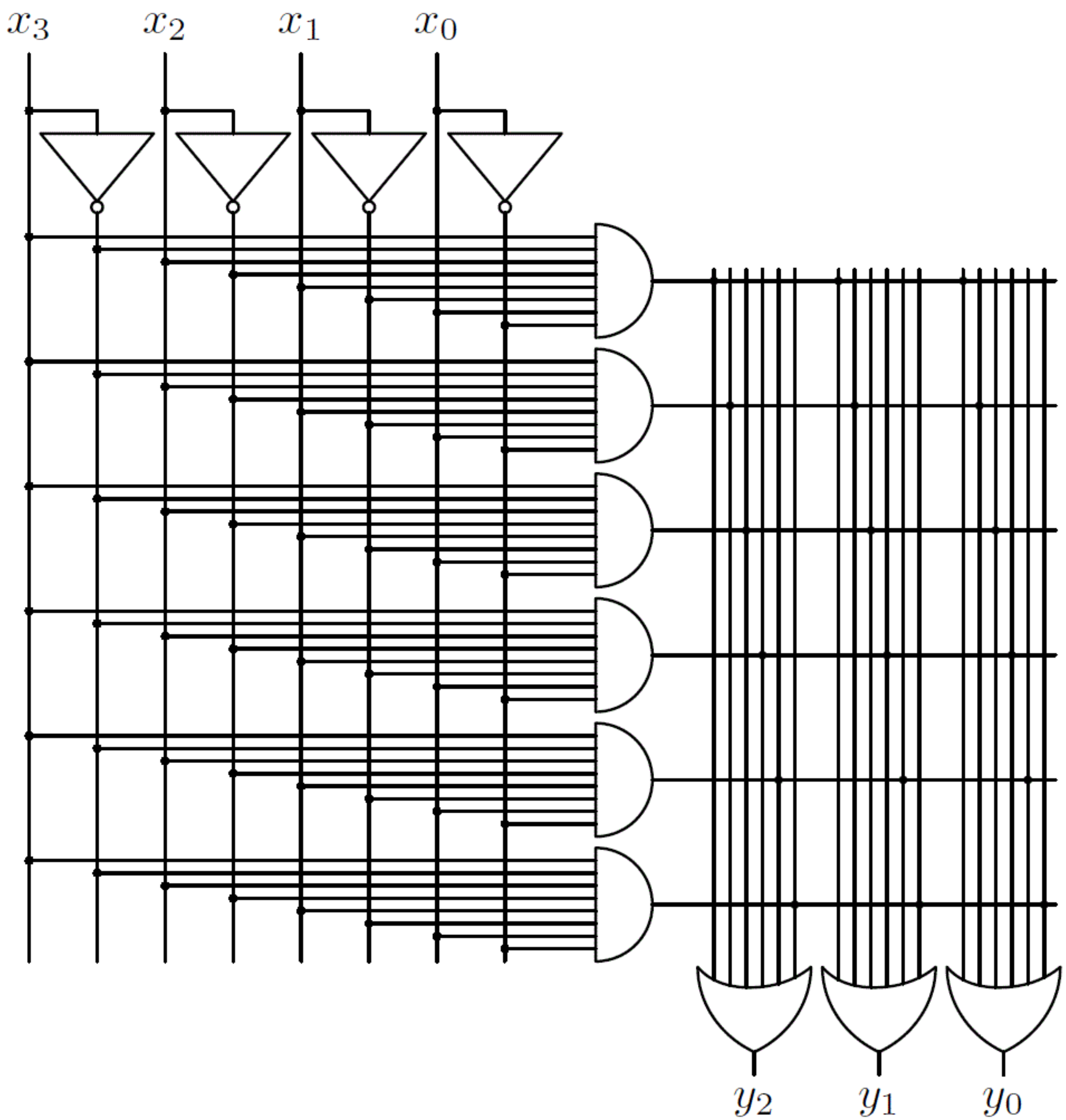


Application Specific Integrated Circuits



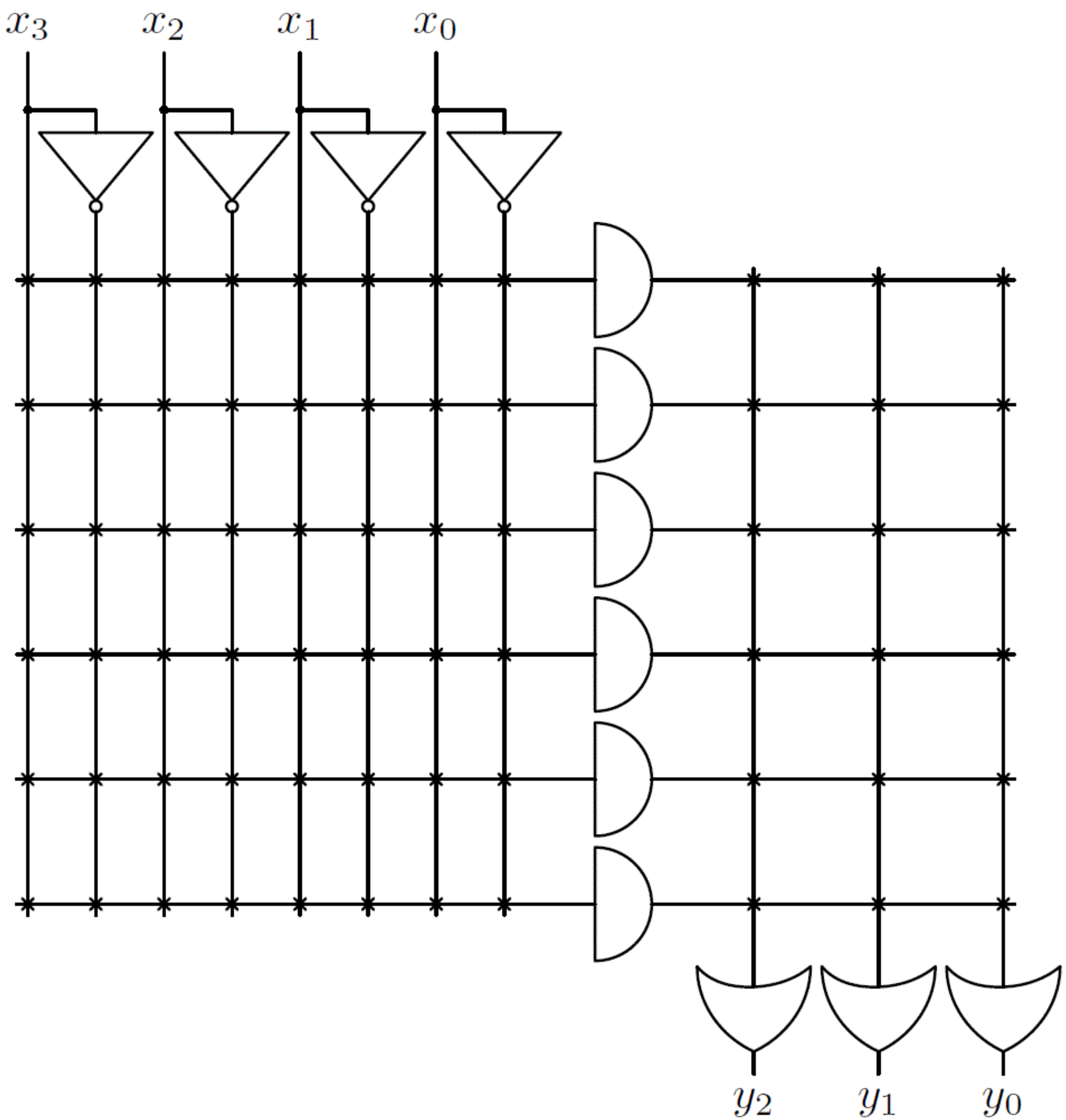
PLD – Programmable Logic Device
PLA – Programmable Logic Array
PAL – Programmable Array Logic
GAL – Generic Array Logic
PGA – Programmable Gate Array
FPGA – Field Programmable Gate Array

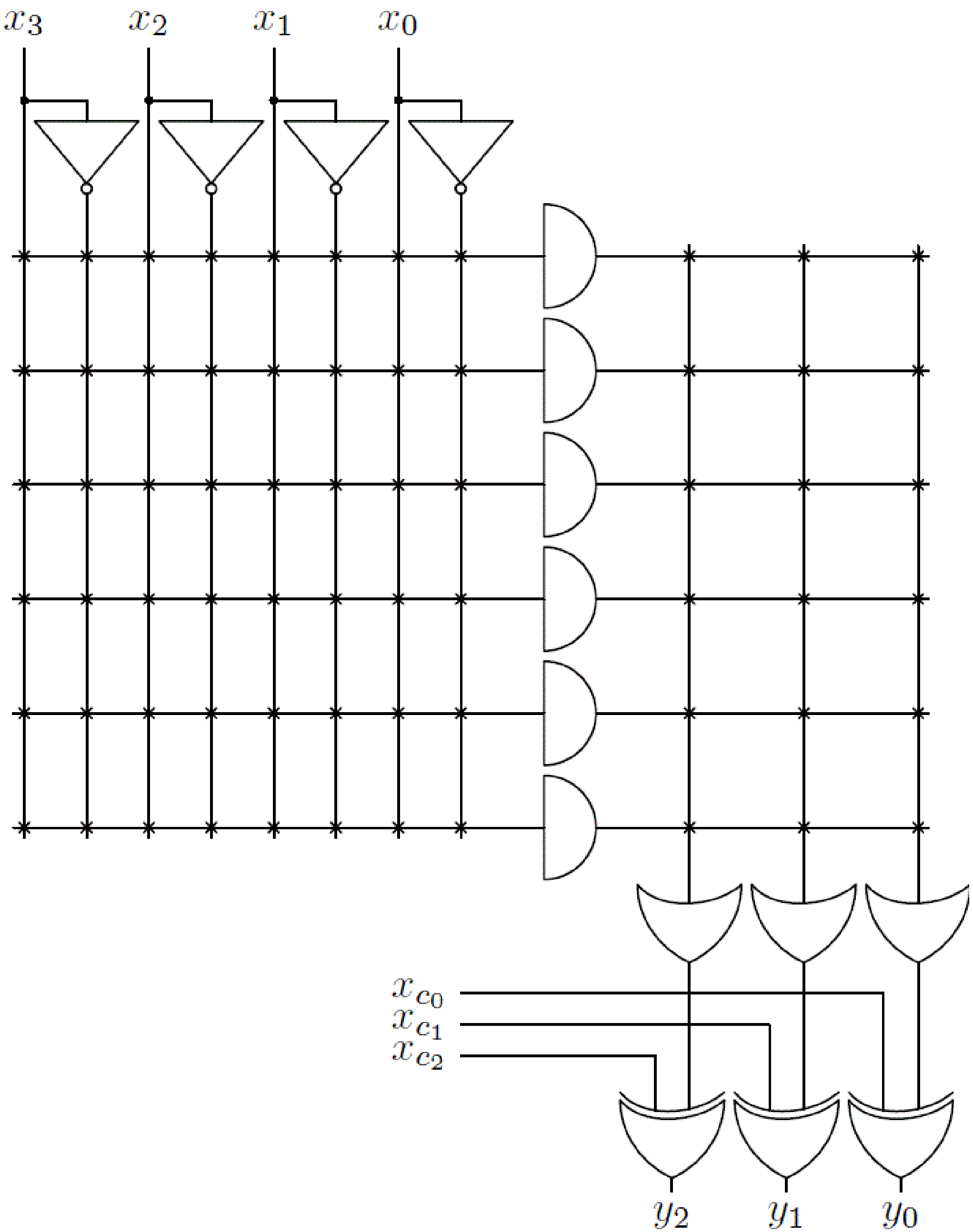
PLD – Programmable Logic Device
EPLD – Erasable PLD (UV light)
EEPLD – Electrically Erasable PLD



PLA:

4 inputs
3 outputs
6
products


x_3
x_2
x_1
x_0
y_2
y_1
y_0



Programming:
burning the initially
present fusible links

$$\begin{cases} y_0 &= \sum(3, 6, 7, 10, 11, 12, 13) \\ y_1 &= \sum(3, 6, 7, 11, 15) \\ y_2 &= \sum(0, 1, 2, 3, 4, 8, 9, 10, 11, 12, 14) \end{cases}$$

$$\begin{cases} y_0 &= \overline{x}_3x_2x_1 + \overline{x}_3x_1x_0 + x_3x_2\overline{x}_1 + x_3\overline{x}_2x_1 \\ y_1 &= \overline{x}_3x_2x_1 + x_1x_0 \\ \overline{y}_2 &= \overline{x}_3x_2x_1 + x_2x_0 \end{cases}$$

$x_3x_2 \backslash x_1x_0$	00	01	11	10
00	0	0	1	0
01	0	0	1	1
11	1	1	0	0
10	0	0	1	1

y_0

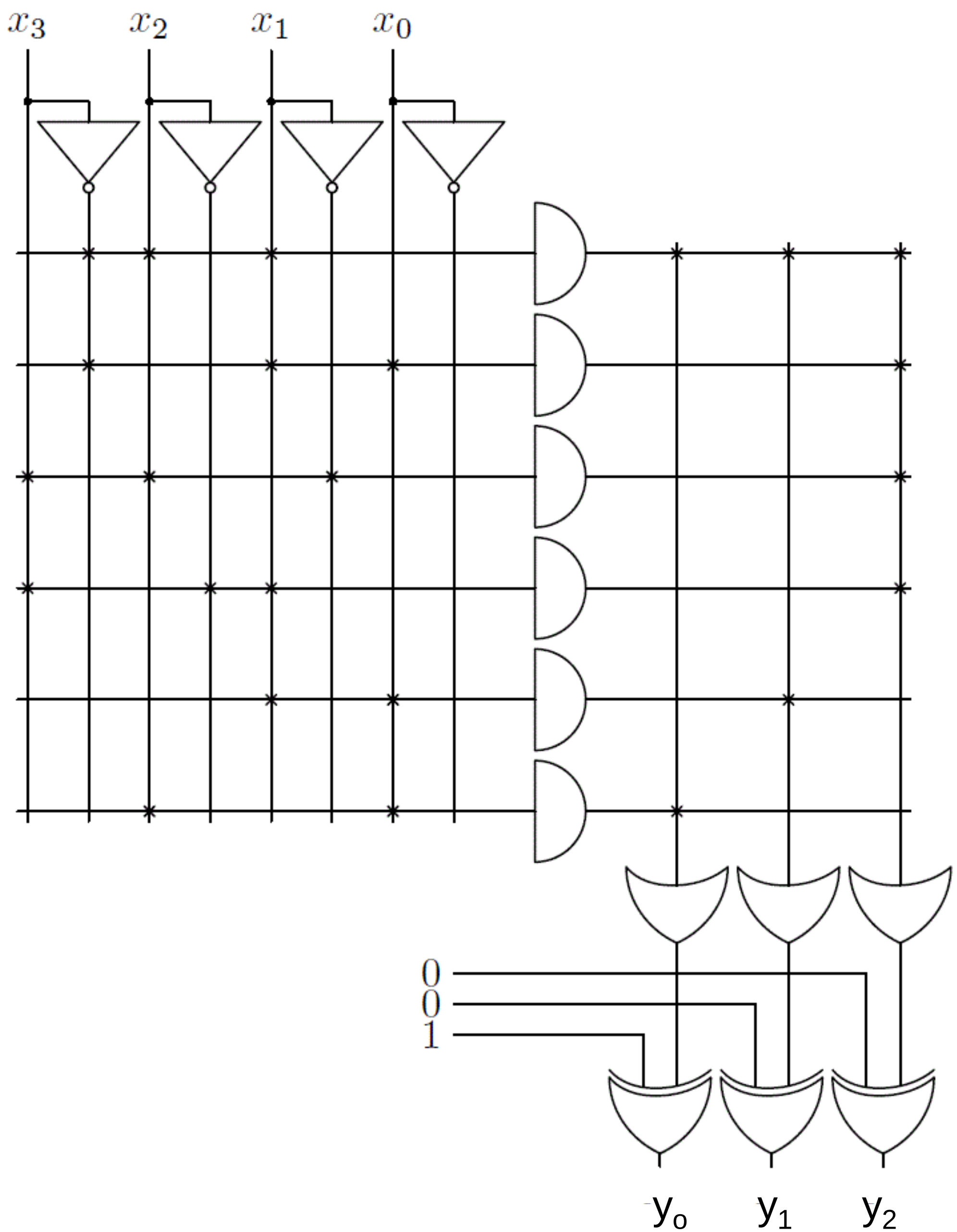
$x_3x_2 \backslash x_1x_0$	00	01	11	10
00	0	0	1	0
01	0	0	1	1
11	0	0	1	0
10	0	0	1	0

y_1

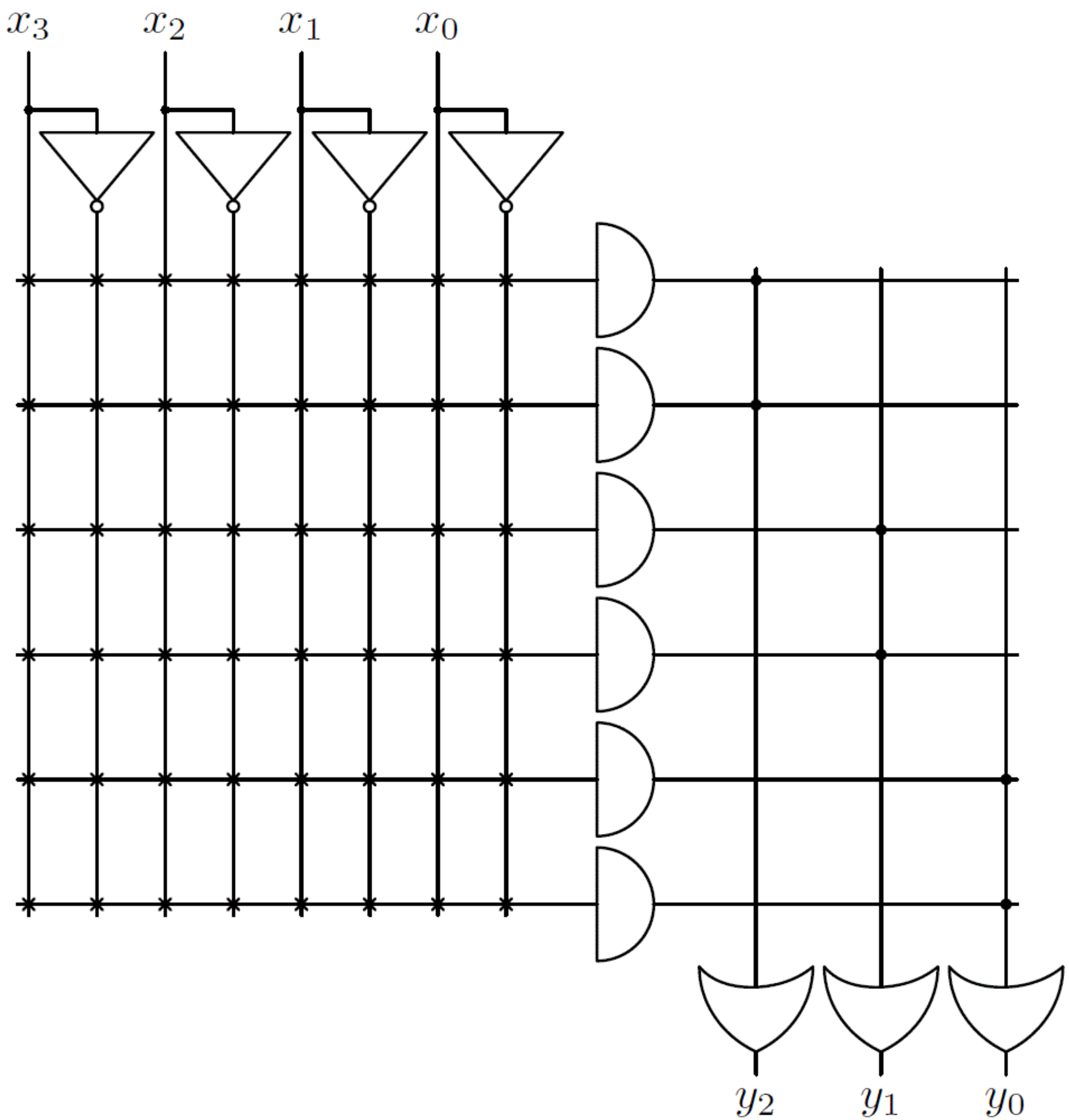
$x_3x_2 \backslash x_1x_0$	00	01	11	10
00	1	1	1	1
01	1	0	0	0
11	1	0	0	1
10	1	1	1	1

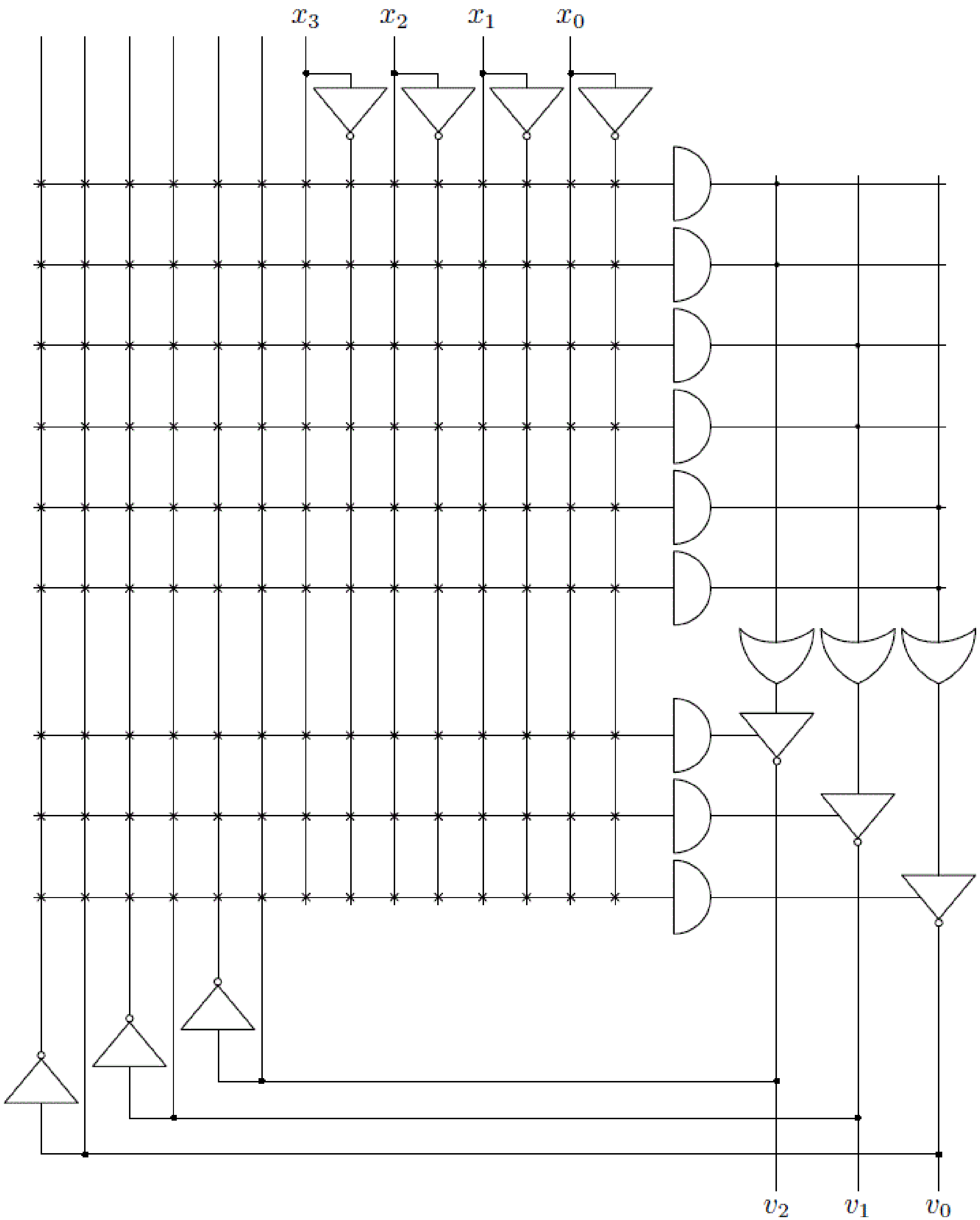
$x_3x_2 \backslash x_1x_0$	00	01	11	10
00	0	0	0	0
01	0	1	1	1
11	0	1	1	0
10	0	0	0	0

Resulting PLA circuit diagram



PAL: principle of operation





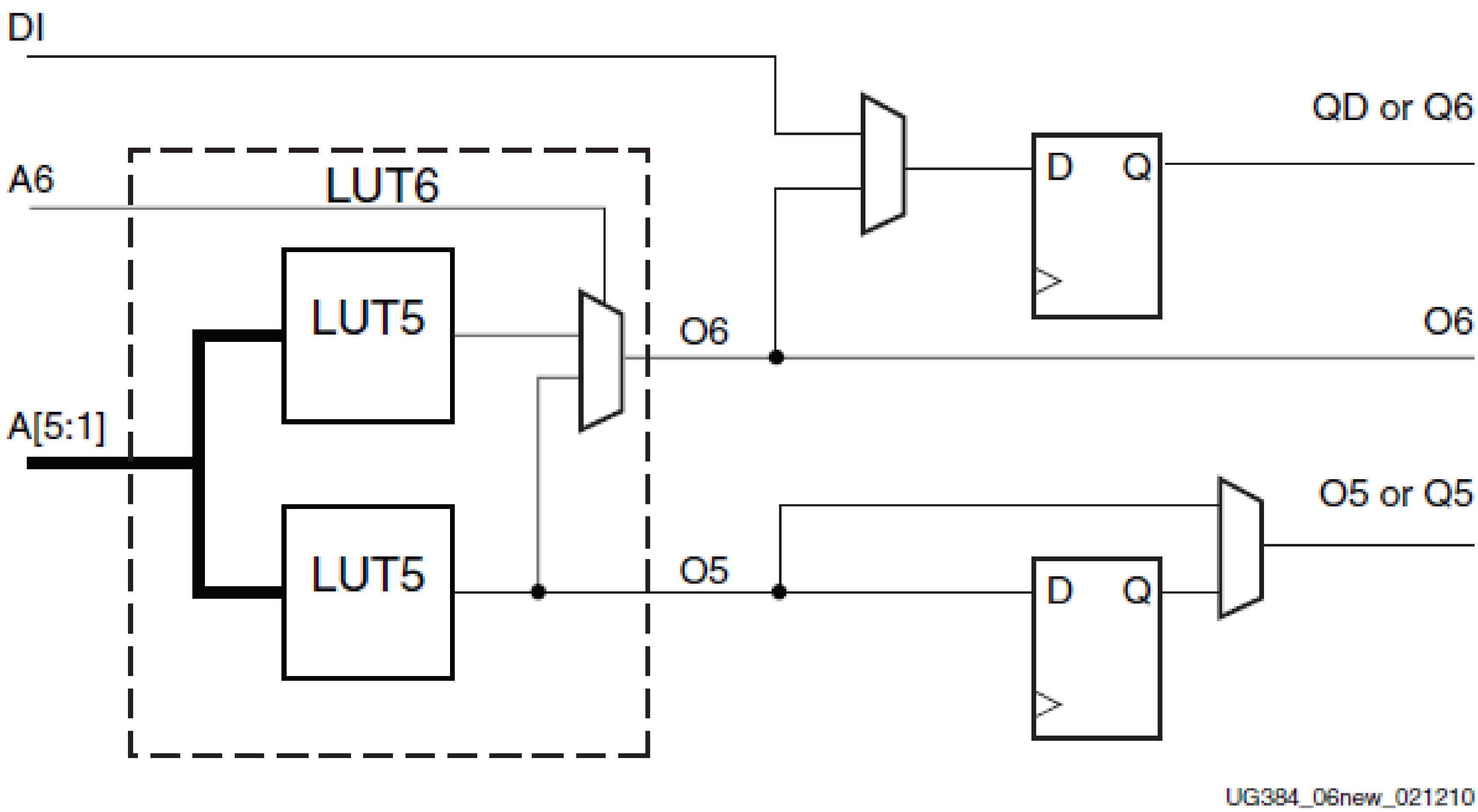
PAL: real structure

- Fixex OR array
- Bidirectional input-output pins (v_i, i = 0,1,2)
- Three-state gates

Spartan-6 FPGA Logic Resources

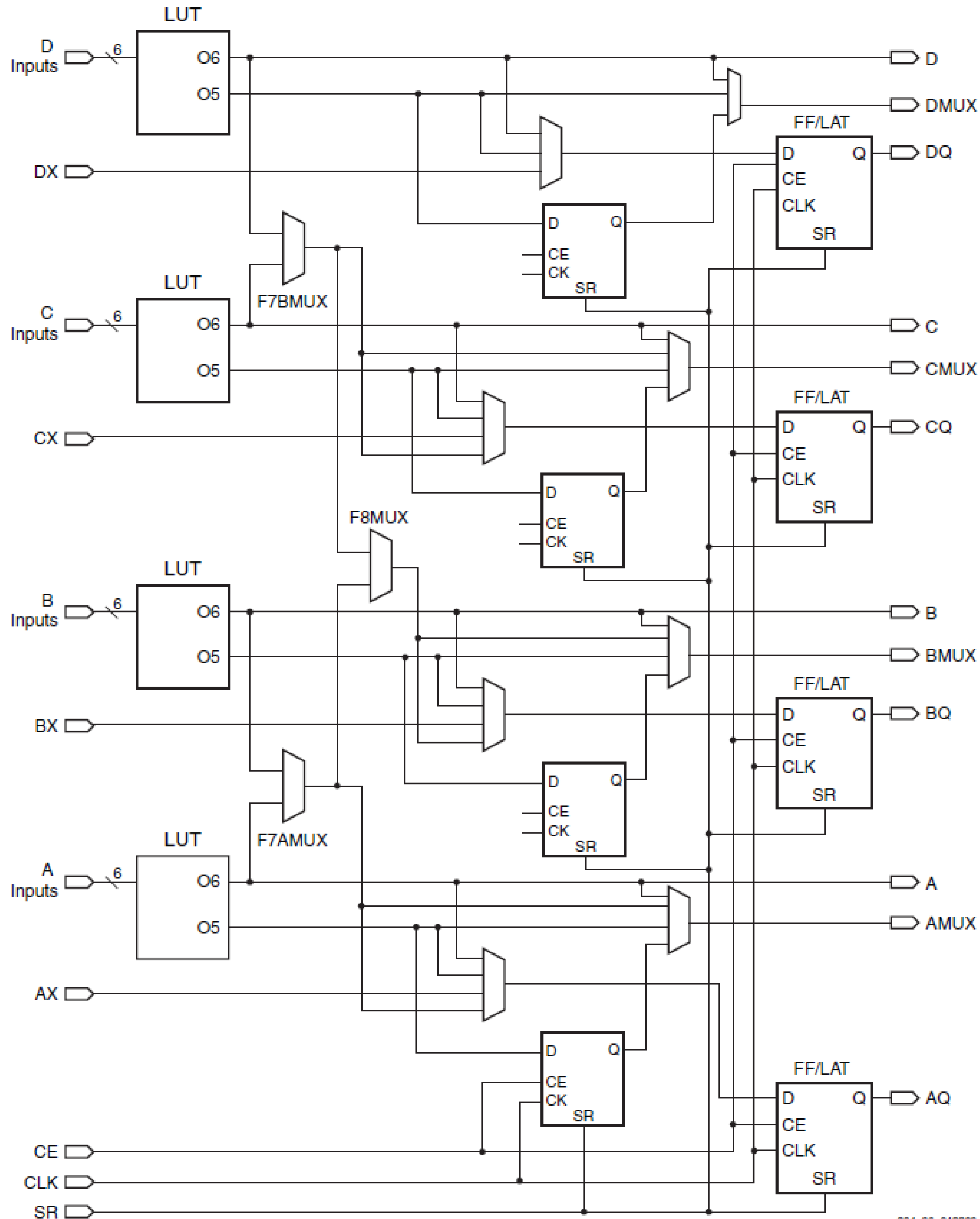
Device	Logic Cells	Total Slices	SLICEMs	SLICELs	SLICEXs	Number of 6-Input LUTs	Maximum Distributed RAM (Kb)	Shift Registers (Kb)	Number of Flip-Flops
XC6SLX4	3,840	600	300	0	300	2,400	75	38	4,800
XC6SLX9	9,152	1,430	360	355	715	5,720	90	45	11,440
XC6SLX16	14,579	2,278	544	595	1,139	9,112	136	68	18,224
XC6SLX25	24,051	3,758	916	963	1,879	15,032	229	115	30,064
XC6SLX45	43,661	6,822	1,602	1,809	3,411	27,288	401	200	54,576
XC6SLX75	74,637	11,662	2,768	3,063	5,831	46,648	692	346	93,296
XC6SLX100	101,261	15,822	3,904	4,007	7,911	63,288	976	488	126,576
XC6SLX150	147,443	23,038	5,420	6,099	11,519	92,152	1,355	678	184,304
XC6SLX25T	24,051	3,758	916	963	1,879	15,032	229	115	30,064
XC6SLX45T	43,661	6,822	1,602	1,809	3,411	27,288	401	200	54,576
XC6SLX75T	74,637	11,662	2,768	3,063	5,831	46,648	692	346	93,296
XC6SLX100T	101,261	15,822	3,904	4,007	7,911	63,288	976	488	126,576
XC6SLX150T	147,443	23,038	5,420	6,099	11,519	92,152	1,355	678	184,304

Simplified Structure of LUT6

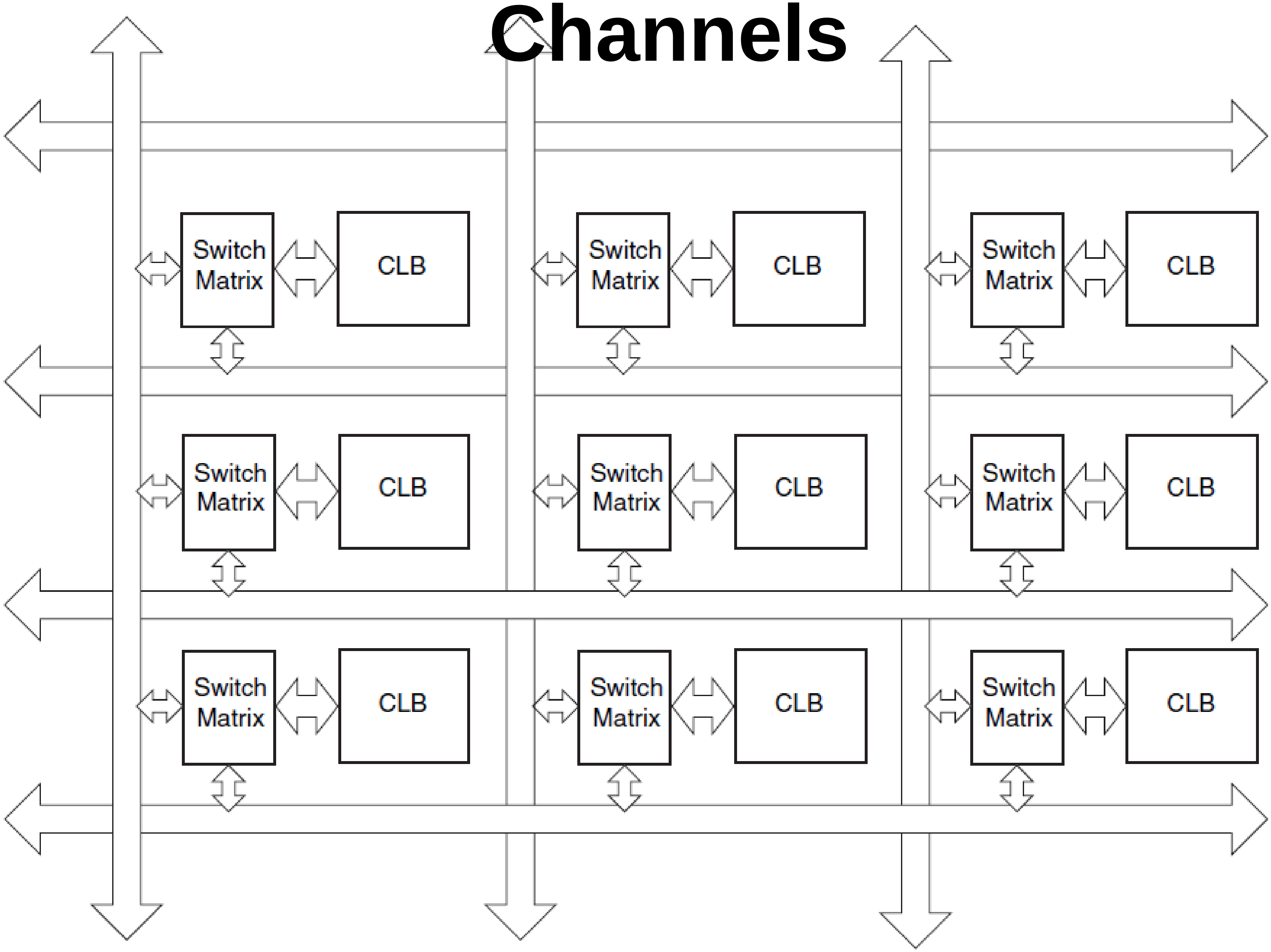


WARSAW UNIVERSITY OF TECHNOLOGY
DEVELOPMENT PROGRAMME

Simplified FPGA Slice



CLB Array and Interconnect Channels

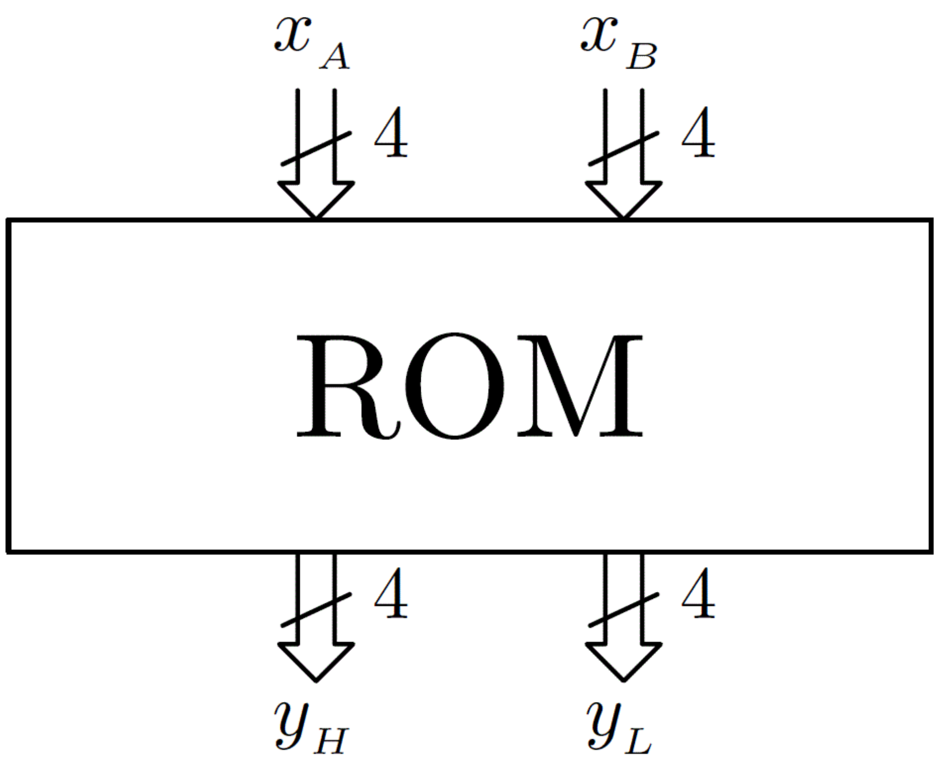


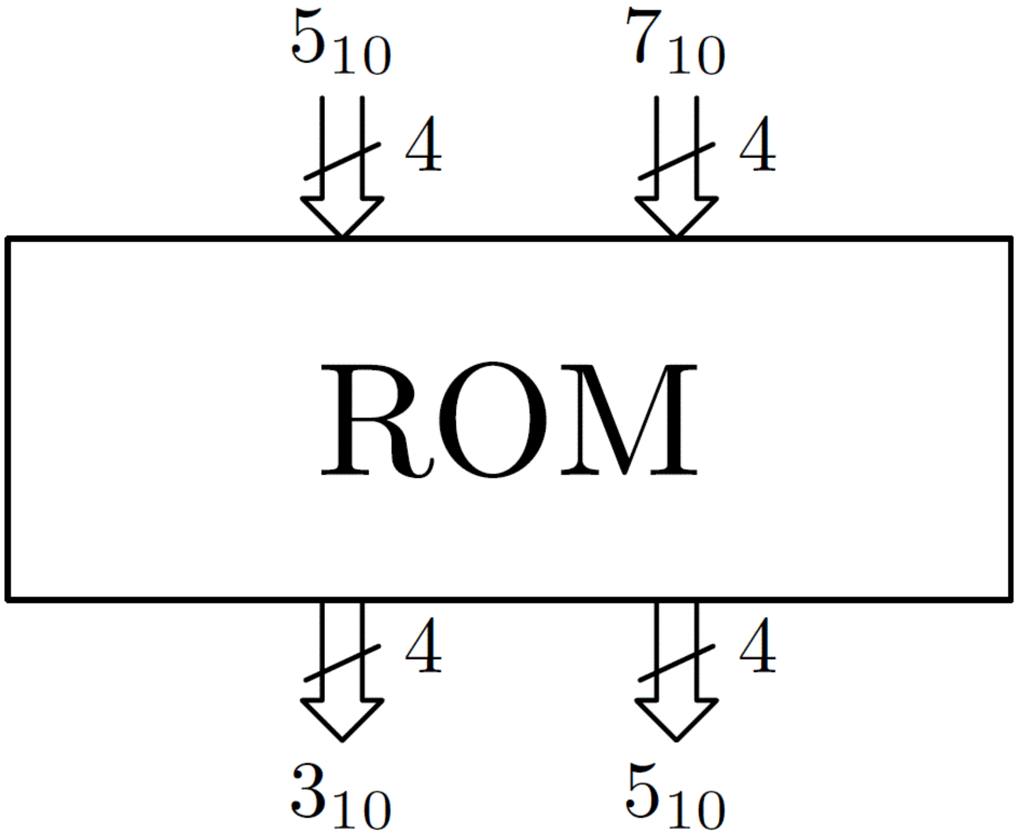
LVDS DC Specifications, V_{dd} = 2.5 V

DC Parameter	Conditions	MIN	TYP	MAX	Units
Output High Voltage for Q and $\overline{Q}$	R_T = 100 Ω across Q and $\overline{Q}$ signals	-	1.38	1.6	V
Output Low Voltage for Q and $\overline{Q}$	R_T = 100 Ω across Q and $\overline{Q}$ signals	0.90	1.03	-	V
Differential Output Voltage (Q - $\overline{Q}$), Q = High ($\overline{Q}$ - Q), $\overline{Q}$ = High	R_T = 100 Ω across Q and $\overline{Q}$ signals	250	350	450	mV
Output Common-Mode Voltage (Q + $\overline{Q}$) / 2	R_T = 100 Ω across Q and $\overline{Q}$ signals	1.125	1.25	1.375	V
Differential Input Voltage (Q - $\overline{Q}$), Q = High ($\overline{Q}$ - Q), $\overline{Q}$ = High	Common-mode input voltage = 1.25 V	100	350	-	mV
Input Common-Mode Voltage (Q + $\overline{Q}$) / 2	Differential input voltage = ±350 mV	0.25	1.25	2.25	V

ROM

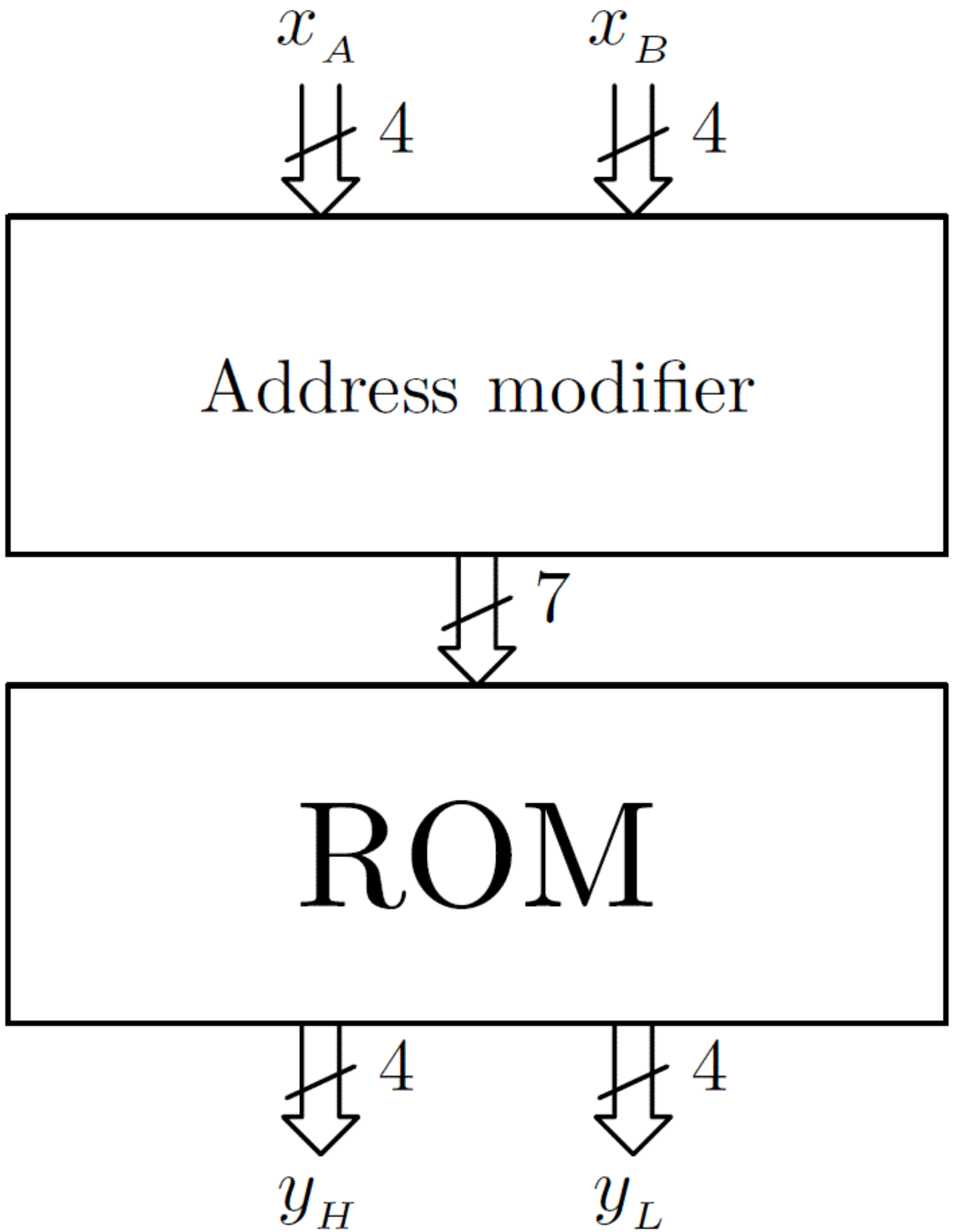
Example: BCD digit multiplier: $y_H \circ y_L = x_A * x_B$





e.g. $35_{10} = 5_{10} * 7_{10}$

- BCD digits: $x_A, x_B \in \{0, \ldots, 9\} \Rightarrow 4$ bits
- BCD digits: $y_H, y_L \in \{0, \ldots, 9\} \Rightarrow 4$ bits
- $4 + 4$ address lines $\Rightarrow 2^8 = 256$ words of $4 + 4$ bits
- ROM size: 256×8 bits
- ROM size needed: $(10 * 10) \times 8$ bits $\Rightarrow 100 \times 8$ bits
- Real ROM size: 128×8 bits, but an address modifier is needed


x_A
4
x_B
4
Address modifier
7
ROM
4
4
y_H
y_L

WARSAW UNIVERSITY OF TECHNOLOGY
DEVELOPMENT PROGRAMME

HUMAN CAPITAL
HUMAN – BEST INVESTMENT!

EUROPEAN UNION
EUROPEAN
SOCIAL FUND

Project is co-financed by European Union within European Social Fund