# Series & Parallel Resistor Networks

## Objective

The focus of this exercise is the examination of circuits with series and parallel resistor sub-networks. In analyzing circuits with combination of series and parallel sub-networks, one needs to remember and apply Kirchhoff's Voltage and Current Laws (KVL & KCL) as well as our good friend Ohm's Law.

## Theory Overview

In identifying series and parallel sub-networks, one needs to recall that several components with single nodes in between them constitute a series sub-network. A parallel circuit, on the other hand, is defined by the fact that all components share two common nodes. Several components branch out from a single node and eventually merge back into another common node.

One way of determining the sub-networks of a circuit is by starting at the source and traversing the circuit to the next node

- If the node encountered has a single component attached to it, this component is in series with the source (or the previous component). In this case, one would continue traversing the circuit after the component that was just encountered.
- However, if the node has multiple components attached to it, then the starting node of a parallel network has been encountered. In this case, each branch splitting from this node needs to be traversed individually.
  - o Each branch is traversed individually where it could contain a single series sub-network, another parallel sub-network or a combination thereof.
  - o As each branch is traversed if a node is encountered with several branches merging in, this node would indicate the ending of the parallel sub-network.
- The above procedures are repeated until one arrives back at the source.
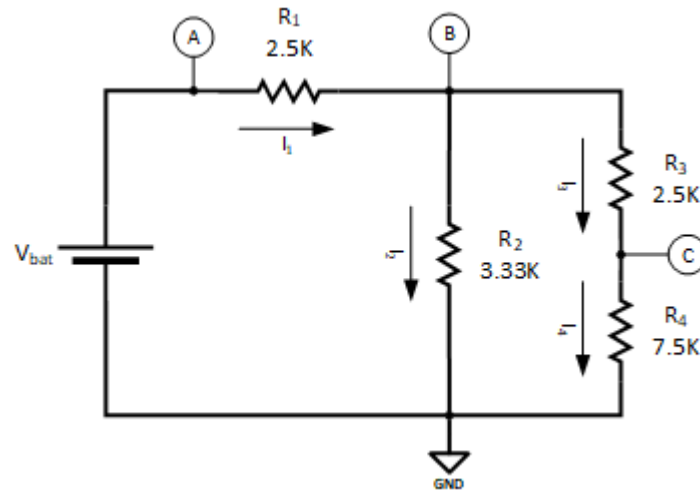
## Schematics



*Figure 1 – Sereis & Parallel Resistor Network*

## Procedure

A. Given the circuit shown in Figure 1, analyze the circuit and determine inner most resistor network.

    a. Determine the equivalent resistance for this innermost sub-network and record it below:

$$R_{eq1} = \underline{\hspace{3cm}}$$

    b. Redraw the circuit in Figure 1 below with the innermost sub-network replaced with $R_{eq1}$.

B. Given the equivalent circuit of step A, analyze the circuit and determine inner most resistor network.

    a. Determine the equivalent resistance for this innermost sub-network and record it below:

$$R_{eq2} = \text{_____}$$

    b. Redraw the circuit from step A below with the innermost sub-network replaced with $R_{eq2}$.

C. Given the equivalent circuit of step B, analyze the circuit and determine inner most resistor network.

    a. Determine the equivalent resistance for this innermost sub-network and record it below:

$$R_{eq3} = \text{_____}$$

    b. Redraw the circuit from step B below with the innermost sub-network replaced with $R_{eq3}$.

D. Given the equivalent circuit of step C, determine the voltage at point A with respect to ground and current $I_{eq3}$ in the circuit and record them below:

$V_A =$ _____

$I_{eq3} =$ _____

E. Given the equivalent circuit of step B, determine currents $I_1$ and $I_{eq2}$ and the voltage at point B with respect to ground and record them below:

$I_1 =$ _____

$I_{eq2} =$ _____

$V_B =$ _____

F. Given the equivalent circuit of step A, determine the voltage at point B with respect to ground and the currents $I_2$ and $I_{eq1}$ and record them below:

$V_B =$ _____

$I_2 =$ _____

$I_{eq1} =$ _____

G. Given the circuit shown in Figure 1, determine currents $I_3$ and $I_4$ and the voltage at point C with respect to ground and record them below:

$I_3 =$ _____

$I_4 =$ _____

$V_C =$ _____

# SPICE

A.  Enter the schematic for the circuit in Figure 1 in LTSpice as shown below
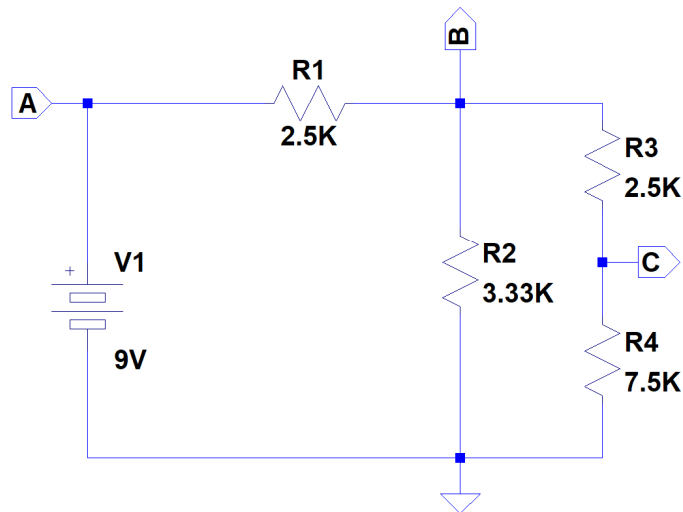


*Figure 2 – Sereis & Parallel Resistor Network LTSpice Schematic*

a.  Enter a SPICE directive to run a transient (time) simulation from 0 to 1ms stepping at 1us. The initial voltage value should be set to 0.  (Recall that this was done by adding the "startup" parameter to the .tran SPICE directive.)
b.  Run the simulation, and record the values listed in Table 1 below.

*Table 1 – Sereis & Parallel Resistor Network SPICE Simulation Results*

| $V_A$ | $V_B$ | $V_C$ | $I_{R1}$ | $I_{R2}$ | $I_{R3}$ | $I_{R4}$ |
|-------|-------|-------|----------|----------|----------|----------|
|       |       |       |          |          |          |          |

# Questions

A.  Do the simulation results match those calculated in the "Procedure" section?

B.  What could contribute to the numbers being different?

C. If you were to simulate the equivalent circuit of step C in the "Procedure" section, what values would you expect for $V_A$ and $I_{eq3}$? Record them below.

$V_A = $ _____

$I_{eq3} = $ _____