ECSE 534 Analog Microelectronics – Course Project (Phase II)

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***Abstract*—The final course project is presented in this paper. A 1-bit first order low-pass $\triangle\Sigma$ modulator (DSM) is designed in this project featuring the switched-capacitor technology. The design is first implemented in Matlab Simulink to test the algorithm feasibility. Then the respective architecture is mapped to the circuit level by using Cadence Virtuoso, with IBM 130nm CMOS technology. Finally, the circuit layout schematic and post-layout simulations are also given for cross-checking. In this paper, both Matlab and Cadence Virtuoso simulations will be discussed, and the latter will include the pre-layout simulation (PreLS) and post-layout simulation (PLS) results. With all these specifications presented, readers can find out that the design finally meets the project requirement by achieving a SNR 82dB in the Simulink model, 63dB in the Cadence circuit implementation, and 61.37dB in the extracted circuit layout with all parasitic effects considered, all above 60dB.**

***Keywords*—IBM 130nm, $\triangle\Sigma$ Modulator (DSM), Analog CMOS Circuits, A/D Circuits**

I. Introduction

$\triangle\Sigma$ modulator (DSM) is commonly used for analog-digital conversion (A/D). Particularly, for a 1-bit first-order low-pass DSM its high-level block-diagram is given in *Fig. 1*.

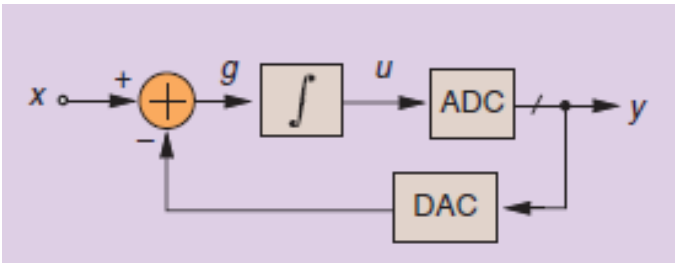

Figure 1: Block diagram of 1-bit first-order low-pass DSM [1]

The philosophy behinds 1-bit DSM is as follow: it converts the analog signal to the digital signal by the pulse density of digital "1", and digital "0"; using 1-bit conversion can maximally mitigate the distortion effects from the electronics, thereby maintain the linearity of transfer characteristics of analog inputs and digital outputs. However, in order to increase signal-to-noise-ratio (SNR) of the system, we need to introduce the noise-shaping scheme and over-sampling technique. Since majorly the noise is coming from the quantization error who has a uniform distribution over the time, the noise shaping can be achieved by the negative feedback by using digital-analog-conversion (DAC). Oversampling is the technique to wide-spread the power-spectral-density (PSD) of the noise through sampling the signal at way higher frequency rate that Nyquist-sampling frequency. This can be visualized in *Fig. 2*.

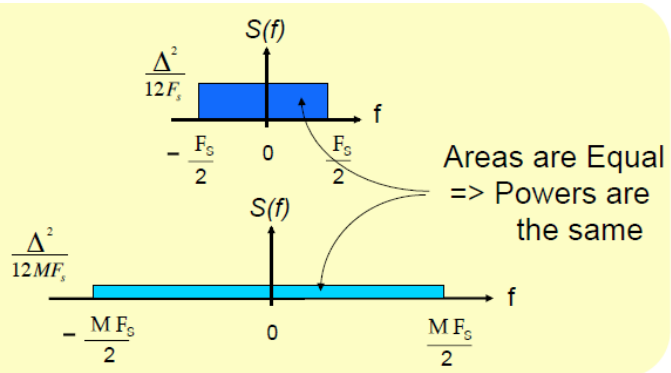

Figure 2: Spreading PSD of quantization noise through oversampling [2]

With these concepts, one is able to model this architecture in Matlab simulation, which will be then mapped to the silicons by using Cadence Virtuoso.

This report is the final phase of the project, so all simulation results, including the Simulink model, the Cadence PreLS model, as well as the Cadence PLS model, will be discussed entirely. Matlab simulation results are presented in *Section II* and Cadence PreLS simulations will be discussed in *Section III*. Cadence PLS simulations will be demonstrated in *Section V*. The final comparisons among these three and the conclusion will be made in *Section VI*.

II. Simulink Model for 1-bit DSM A/D

Guided by the the block diagram given in *Fig. 1*, the corresponding Simulink model is constructed and shown in *Fig. 3*.

The input is a sin-wave whose fundamental frequency $f_{sin} = 10kHz$. Its amplitude swings from $0.2V - 1V$, whose lower and upper margin correspond to V_{ref-} and V_{ref+} of the 1-bit DAC in the negative feedback, respectively. The bandwidth of the system is determined by the following equation:

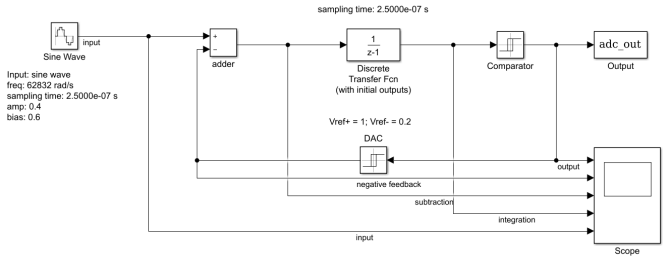

Figure 3: Simulink model of 1-bit DSM A/D

$$f_{bandwidth} = (1+\alpha) \times 20kHz = 23.58kHz$$
$$\alpha = \frac{179}{1000} = 0.179 \quad (1)$$

Where 179 is the last 3 digits of the writer's student ID number. The oversampling ratio OSR for first-order, 1-bit DSM is calculated by the following equation [2]:

$$OSR = 10^{\frac{SNR-2.61}{30}} \quad (2)$$

In this project, the desired minimum SNR is defined as 60dB; by substituting this value back to *Eq. 2*, the corresponding OSR is calculated as 81.846. The oversampling frequency can thereby be calculated using the following identity [2]:

$$f_{oversampling} = 2 \times f_{bandwidth} \times OSR \quad (3)$$

Which gives $f_{oversampling} \approx 4MHz$. This ensures that by sampling the input signal at this frequency rate, the minimum SNR value should be larger than 60dB.

These calculations are verified by the Simulink model in *Fig. 3*. The PSD of the output signal is plotted in *Fig. 4*.

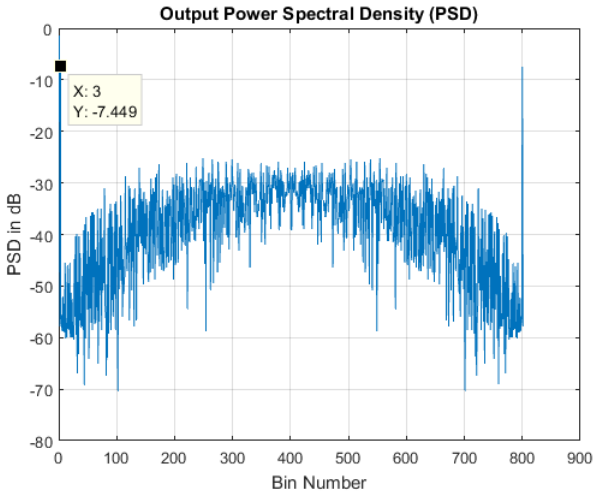

Figure 4: PSD of the Simulink model of 1-bit DSM A/D

In *Fig. 4*, the labelled spike corresponds to the input signal's fundamental frequency that is 10kHz, whose respective bin number is 3. Since the interested bandwidth is given by *Eq. 1*, the respective bin number of $f_{bandwidth}$ is calculated as 7. The following equation can thereby be used to calculate SNR of the output signal.

$$SNR = \frac{Power_{i=3}}{\sum_{i=2, i\neq 3}^{7} Power_i} \quad (4)$$

Here the first point from PSD is skipped since it is a redundant value. The calculated SNR value is equal to 82.49dB, which is larger than the minimum requirement.

The plot of SNR over different input amplitudes where the reference voltage of DAC V_{ref+} and V_{ref-} are fixed at 1V and 0.2V, is presented in *Fig. 5*. As one can see, SNR increases with the up scaling of the input amplitude until it reaches around 0.4V to 0.45V.

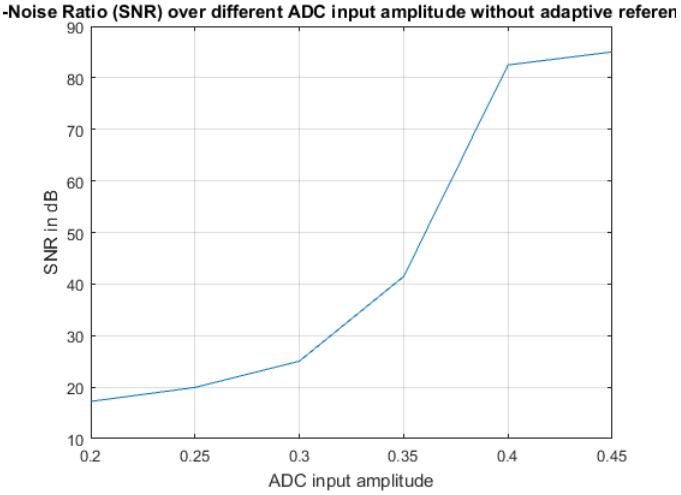

Figure 5: SNR vs. diff. input amplitude of the Simulink model of 1-bit DSM A/D with $V_{ref+} = 1.0V$ and $V_{ref-} = 0.2V$

When the reference voltages of DAC are self-adaptive with the change of the input voltage amplitudes, the larger the input swing, the better SNR will be obtained, which is shown in *Fig. 6*. Biased at 0.6V, the feedback reference voltages are tracking the amplitude of the input signal, since higher amplitude brings higher input signal power, SNR will be therefore higher. Since from assignment 2 one can see that the maximum input swing for the amplifier in unity-gain configuration to reach the total-harmonic distortion less than 0.2% is about 0.4V, it is selected here as the input amplitude.

Finally, the plot of the input signal with respect to the output quantized signal is given in *Fig. 7*. As the picture illustrates, the pulse density is very coarse when the input sin-wave reaches either the minimal or maximal, whose corresponding digital value is 0 and 1, respectively; when the signal is in the transient stage between these two digital states, the density of digital pulses is very dense. This justifies the mechanism of pulse-density-modulation (PDM), the working principle behinds this 1-bit DSM.

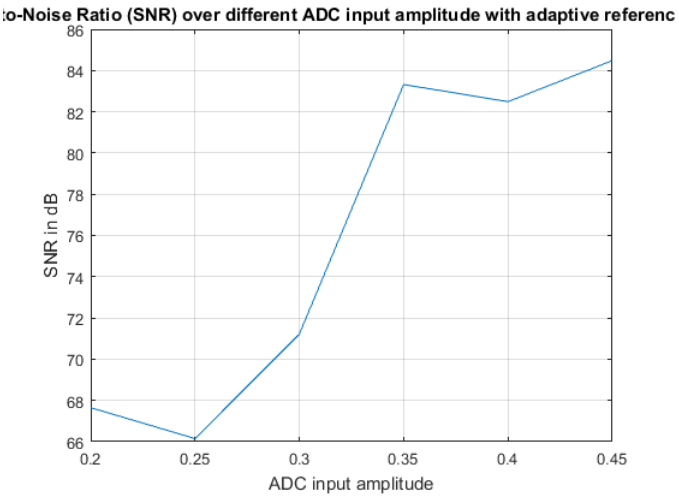

Figure 6: SNR vs. diff. input amplitude of the Simulink model of 1-bit DSM A/D with V_{ref+} and V_{ref-} with self-adaptive DAC reference voltages

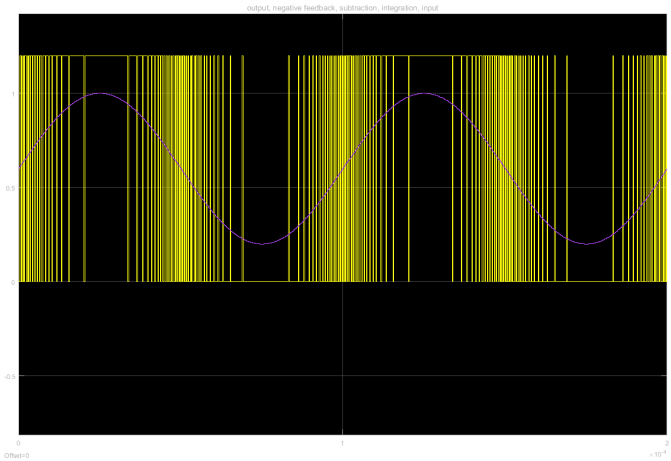

Figure 7: Input (pink) vs. output (yellow) of the Simulink model of 1-bit DSM A/D, given two completed duty cycles, with two cycles

All the above calculated values as well as some other specifications are summarized in the following table for readers' convenience.

The waveform probed at input, output, feedback, subtraction, and integration are given the *Fig. 8*.

III. Cadence PreLS Simulations of 1-bit DSM A/D

After the verification in Maltab, the algorithm can be therefore mapped to the silicon with confidence. The corresponding circuit is constructed in Cadence Virtuoso, whose schematic is shown in *Fig. 9*.

As highlighted in the plot, there are six major portions of this 1-bit DSM A/D, which are: switched capacitor (SC), integrator,

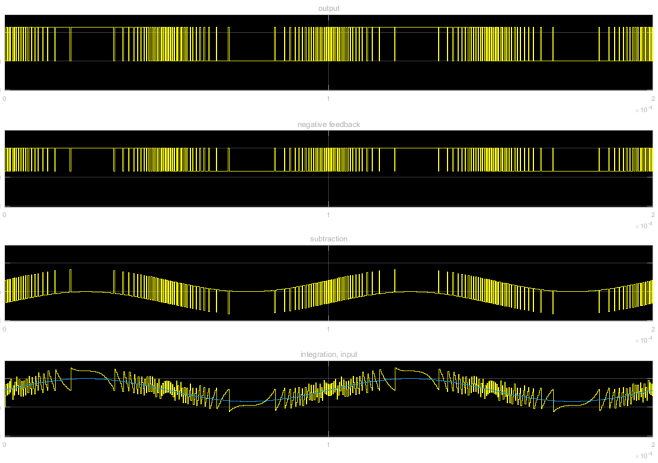

Figure 8: From top to bottom: output, feedback, subtraction, integration and input sin-wave

Table I: Pre-Cadence calculations of some critical parameters of 1-bit DSM A/D

Power supply	1.2V
Analog ground	0.6V
Input voltage range	0.2-1.0V
$f_{bandwidth}$	23.58kHz
$f_{sinwave}$	10kHz
$f_{oversampling}$	4MHz
Minimum OSR	81.84
Simulated OSR	443
Minimum SNR	60dB
Simulated SNR	82.49

1-bit comparator (A/D), D-latch, feedback 1-bit D/A, and a 4-phase clock circuit. The next couple of sub-sections will be talking about these circuit blocks individually. The PreLS simulated results are summarized by the end of this section.

A. Switched Capacitor

Switched capacitor, or SC in short, is an important circuitry of this DSM, who is essentially performing as a resistor by periodic switching on and off [2], which together with the integrator forms a low pass filter (Miller integrator). The resistance of this SC can be calculated by *Eq. 5*.

$$R_C = \frac{1}{f_C C} \tag{5}$$

Where f_C is the switching frequency of the SC, and C is the capacitance of the capacitor. Here, the capacitance is selected as 0.1 pF and the switching frequency f_C is equal to 4MHz, identical to the sampling frequency, but with four different clock phases. These four switching signals will control the triggering of SC.

A closer look of the SC is provided in *Fig. 10*. SC consists of four transmission gates and a capacitor. The transmission gate consists of a pair of PMOS and NMOS and the negative

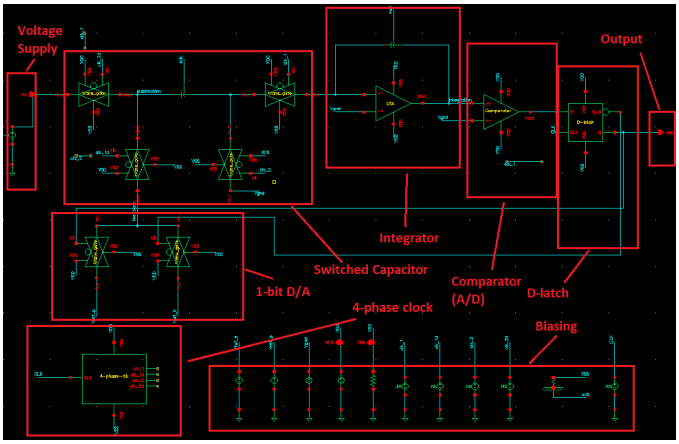

Figure 9: Circuits Schematic of 1-bit DSM

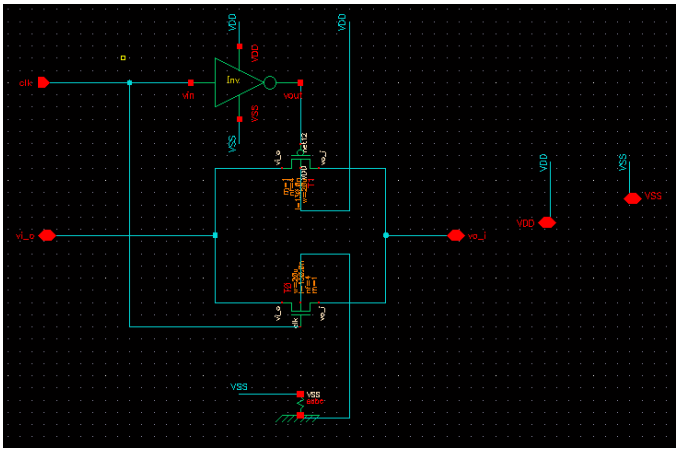

Figure 11: Schematic of transmission gate

clocking signal is feed to PMOS whereas the positive goes to NMOS. This is revealed in *Fig. 11*. The reason why transmission gate here is used is because it can mitigate the charge injection phenomena happens in SC, which is also the motivation of using four-phase clock. The four-phase clock circuit generates four triggering signals for SC with different phases, and they are fed to different transmission gate of SC. The mapping in between transmission gate and clocking signals with different phases is illustrated in *Fig. 12*. The detail timing of the clocking signals will be discussed in the section of four-phase clock circuit. By the configuration in *Fig. 12*, the charge injection effect should be largely in-sensitized.

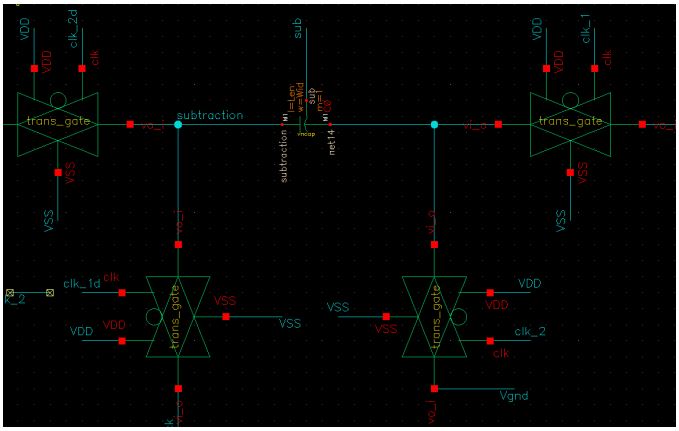

Figure 10: Schematic of SC

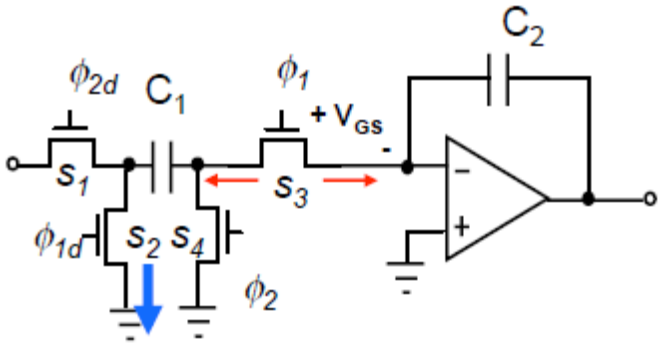

Figure 12: Diagram of the mapping in between different clocking signals with the gates of SC [2]

B. Integrator

The integrator will do the integration of the signal coming from SC, whose circuit diagram is shown in *Fig 13*. This integrator consists of an OTA designed from assignment 2 (whose schematic is neglected here) and a Miller capacitor. The integration signal will be passed to the input of the comparator, doing the analog-to-digital conversion. The integrator together with SC forms a classic low-pass RC filter, and the Miller capacitor here is 0.1pF, yielding about 13ns for the time constant τ ($\tau = RC$).

C. Comparator

Comparator functions as an analog-to-digital converter in this DSM. The analog ground is set as 0.6 V, acting as the threshold for the A/D conversion: if the integration signal is larger than 0.6V, the output signal will be 1.2V; whereas if it is smaller than 0.6V, the output signal will be 0V. The comparator is nothing but an OTA that has the Miller feedback be removed, whose transistor-level diagram can be viewed in *Fig. 14*.

The comparator here is using the non-inverting configuration, and the output signal should be sampled at $f_{oversampling}$ since it is still a continuous time signal; this brings the next circuitry into the picture, the D-latch.

D. D-latch

The purpose of the D-latch is clear: sampling the output signal from comparator and feeding back the signals to the

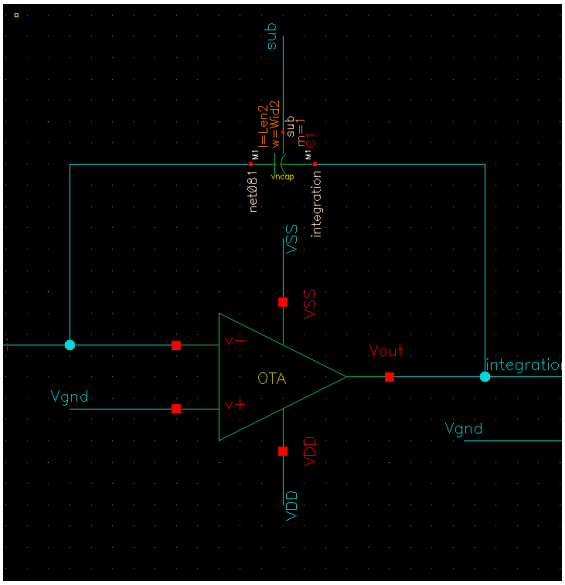

Figure 13: Schematic of integrator

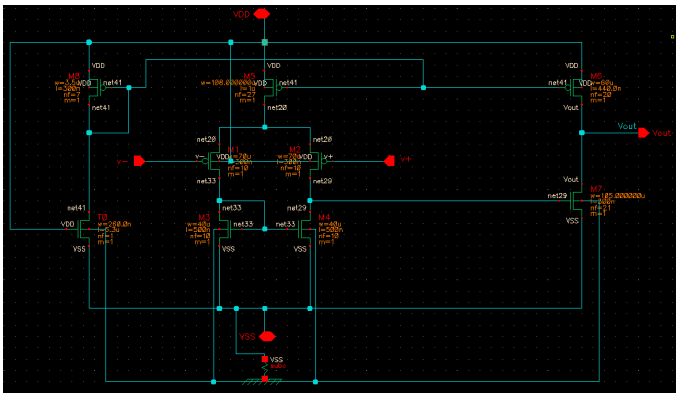

Figure 14: Schematic of comparator

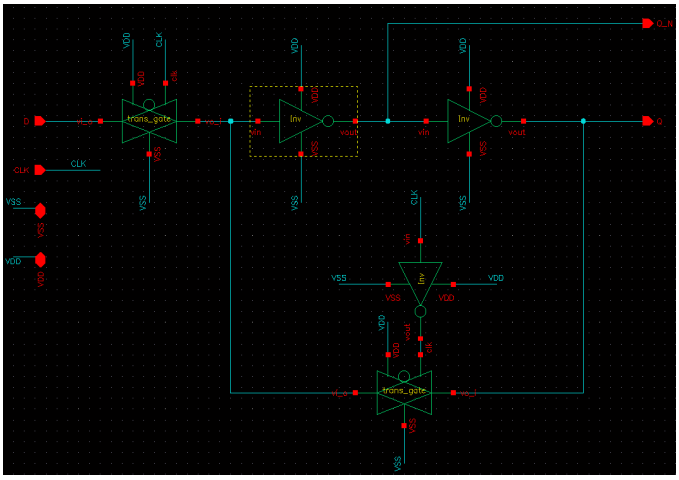

Figure 15: Schematic of D-latch

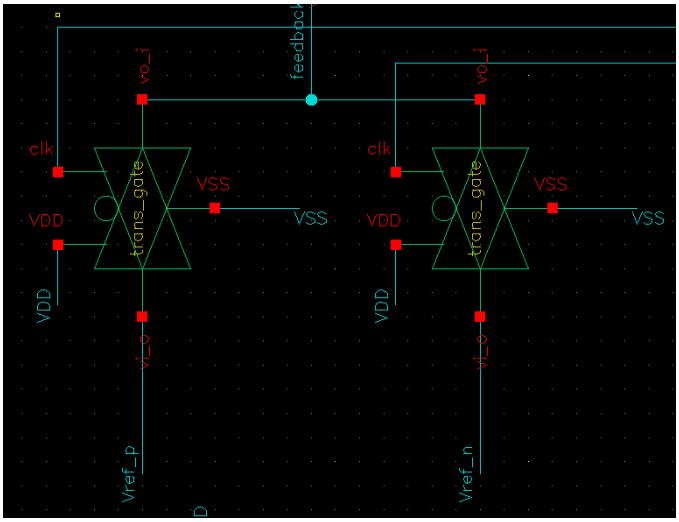

Figure 16: Schematic of 1-bit D/A

D/A circuitry. The schematic diagram of the D-latch is shown in *Fig. 15*. The D-latch consists of three inverters and two transmission gates. There are two inputs to the D-latch, and one of them is the sampling clock signal. There are two outputs which are complementary to each other: the signal coming from the positive pin will be feedback to the positive reference voltage $V_{ref,p}$ of the D/A, and the signal coming from the negative pin will be driven to the negative reference voltage $V_{ref,n}$ of the D/A. The signal comes from the positive pin is also the output of this DSM.

E. 1-bit D/A

The 1-bit D/A functions as the feedback block of this DSM, as seen in *Fig. 16*. The mechanism of this 1-bit D/A is straightforward: feeding $V_{ref,p}$ back to SC for the charge subtraction if the output signal from DSM is digital 1, and feeding $V_{ref,n}$ back to the system if the output is digital 0.

This block is very critical as the performance of the negative feedback will dominant the performance of this DSM. Here since the input signal swings from 0.2-1V, the positive reference voltage is therefore selected as 1V, and negative reference voltage is picked as 0.2V. However, these two values might be optimized later as the numerical simulated results may not match to the circuit level simulation outputs. As noted, the negative feedback in SC-based DSM is achieved by the subtraction is charge domain, rather than the voltage or current signal subtractions.

F. Four-phase Clock

As discussed in the section of SC, a four-phase clock scheme can mitigate the charge injection effect, thereby improving the performance. The schematic of the four-phase clock circuit is presented in *Fig. 17*. As one can see, the four-phase clock

consist of two NOR gate and a couple of inverters that setup the delay of the clock signals. Four clock signals coming out from the circuit has different timing, which is shown in *Fig. 18*. In *Fig. 18*, there are four signals generated, ϕ_1, ϕ_{1d}, ϕ_2 and ϕ_{2d}, which correspond to the clock signals of SC in *Fig. 12*.

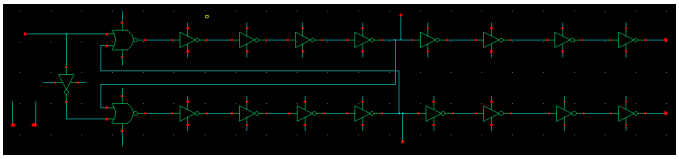

Figure 17: Schematic of four-phase clock circuit

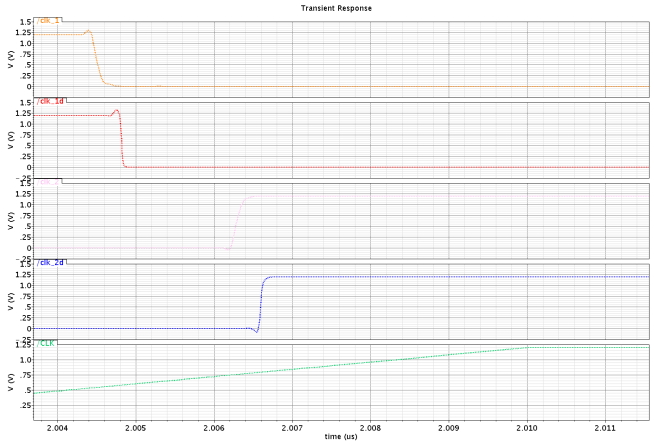

Figure 18: Timing diagram of four clock signals with different phases; from top to bottom: ϕ_1, ϕ_{1d}, ϕ_2, ϕ_{2d}, and input oversampling clock signal $f_{oversampling}$

G. Results and Discussions of PreLS

By revising the signal processing approach employed last time, the writer found out the issue that has majorly caused the negative PSD plot and SNR calculations, and this will be clarified in this paragraph. As summarized in *Table I*, the identical parameters will be used to guide the circuit level implementation in Cadence, and the corresponding PreLS simulated results are plotted in *Fig. 19*, together with the input signal as well as the integration signal. As one can see, the output signal generated by DSM does relatively match the simulations from Matlab

However, as pointed out last time in the Phase I report, the PSD plot of the output signal gives negative results in terms of noise-shaping performance. The writer then realizes the issue behind is the forgetting of re-sampling of the output data when it is imported to Matlab for post-processing. Since the Cadence simulated output signal is essentially still a time-continuous signal, it has to be re-sampled again, with the same oversampling frequency $f_{oversampling}$ provided in *Table I*. This can be done by either re-scripting the Matlab code, or simply defining the time interval of data-sampling in the Cadence built-in calculator function. By doing so, the writer successfully reconstructs the correct PSD plot whose time interval equals to two complete cycles of the input sin-wave signal. This is shown in *Fig. 20*. Clearly, the noise-shaping phenomena is illustrated in this picture, by achieving a SNR 63dB, which is apparently above the required minimum value, 60dB.

Nevertheless, there are some points are worth to be clarified regrading the discrepancies in between Matlab and Cadence PreLS results; first, a two-phase clock, instead of four-phase clock, is used for this test, namely only ϕ_1 and ϕ_2; this is due to the reason of the degrading of the SNR by the clock signal feeding to the transmission gate when four-clock scheme is used. More careful designs on the four-phase clock circuit should be given, as well as the transmission gate, which can be upgraded by utilizing dummy switches to mitigate clock signal injection effect. Second, by referring to *Fig. 19*, it can be seen that when the input signal reaches its minimal value, the integrator does not function very well, causing the output signal has not great pulse density accuracy around 0.2V. By solving these issues, one should be able to achieve higher SNR.

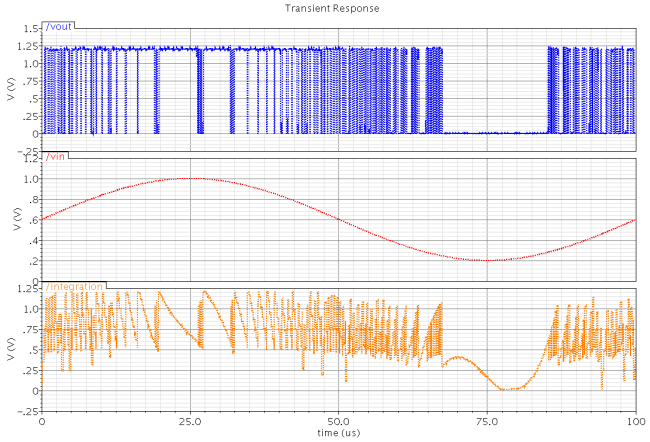

Figure 19: Output waveform (one cycle) from DSM circuit; from top to bottom: output signal, input signal, and integration signal

IV. Cadence PLS Simulations of 1-bit DSM A/D

As the continuous of Cadence PreLS, the respective circuit layout is constructed in Virtuoso environment. The circuit layout has successfully passed the Layout-versus-Schematic (LVS) test and has been extracted eventually for PLS purposes, which should contain all parasitic resistance and capacitance effects contributed by all silicon elements. The LVS result is shown in *Fig. 21* and the corresponding extracted circuit layout is demonstrated in *fig. 22*.

As noted, the circuit layout only contains the 1-bit DSM A/D module, as it is the main interest of this project. Another reason

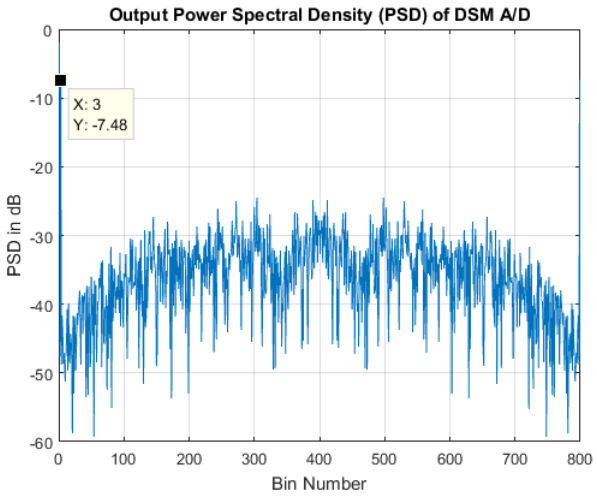

Figure 20: PSD of the output signal from DSM circuit

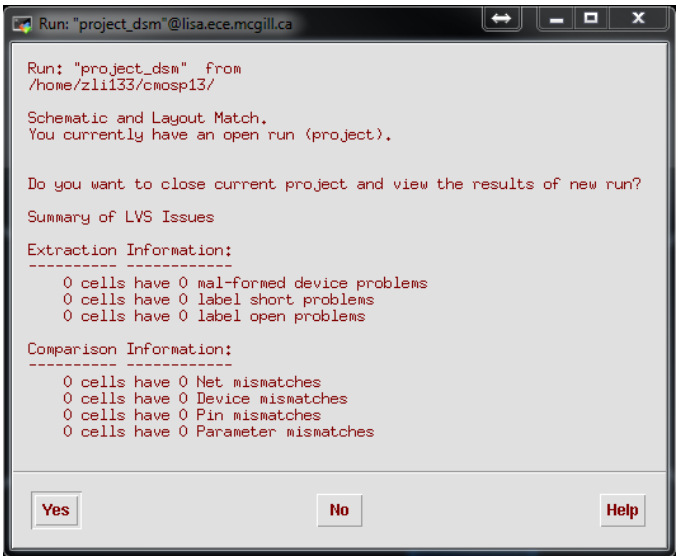

Figure 21: LVS result

is the uncertain robustness of the designed four-phase clock circuit in this project, which makes the necessity of approaching its layout design questionable. Also, as the confession made by the writer, the time limitation is also a critical factor.

Special care here should be given to the layout. For instance, as pointed in [3] and [4], for *vncap*, which means vertical (coplanar interdigitated) n-type capacitor, its best performance can be achieved by having 1:1 ratio of its length to width, which is the reason why the capacitor in *Fig. 22* are all in square shape. Another care should be given to the multi-substrate-contact network when one is conducting the LVS testing. Multiple substrate contacts, or *subc*, can lead to shorting problem in LVS if one does not explicit define the substrate boundaries. By consulting [5], a dummy layer called "SXCUT" and its

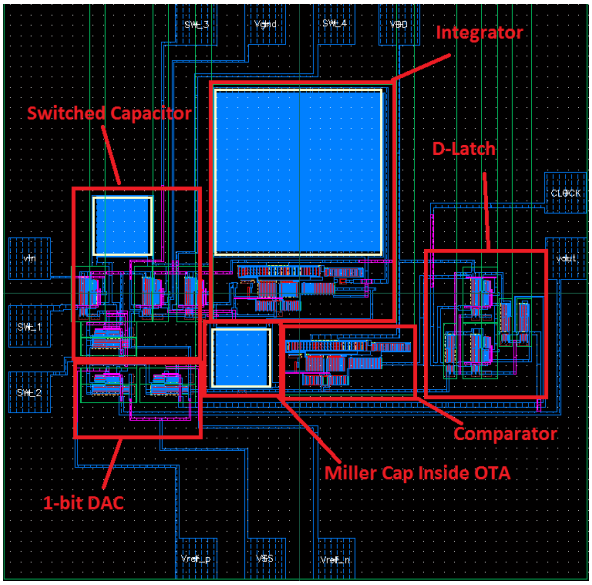

Figure 22: Extracted 1-bit DSM A/D circuit with all parasitic effects included

labels can be used to remove the above issue.

The testing setup is exactly the same as *Section V*, a two-phase clock instead of four-phase is employed to provide triggering signal to SC (ϕ_1 to S_1 and S_4, ϕ_2 to S_2 and S_3, refer to *Fig. 12*). The output signal from extracted circuit is plotted in *Fig. 23* together with its respective PSD in *Fig. 24*.

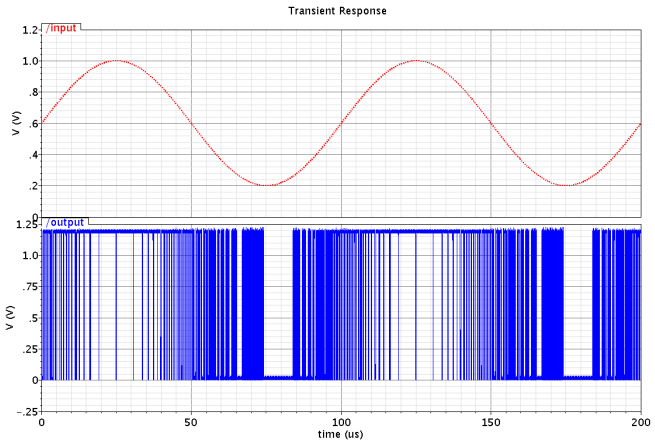

Figure 23: PLS of extracted 1-bit DSM A/D circuit with all parasitic effects included; from top to bottom: input sin-wave (two cycles) and output output PDM signal

Since in all PSD plots (*Fig. 4, Fig. 20* and *Fig. 24*), the interested time intervals are identical (two cycles), with also the same sampling frequency $f_{oversampling}$, therefore the same amount of bin number is obtained (800), and the labeling for the input signal spike in these three figures is the same as well.

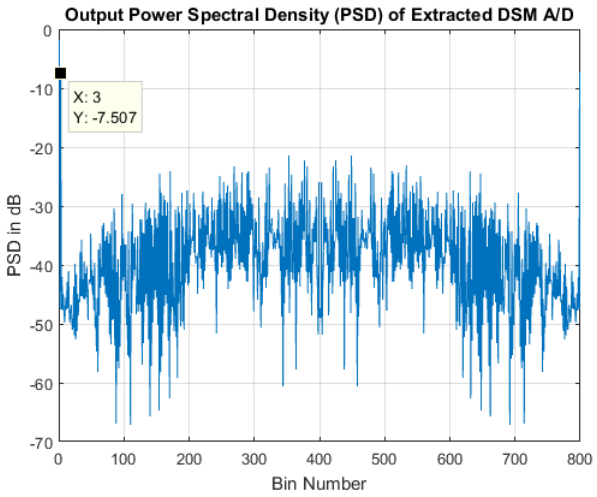

Figure 24: PSD of the extracted 1-bit DSM A/D circuit with all parasitic effects included

The extracted circuit achieves a SNR 61.37dB, which is also above the minimum design specification. This is also justified by simply comparing these three PSD plots: the noise-shaping indeed increases SNR performance quite obviously by shifting the power spectrum of noises to higher frequency domain.

For readers' intrests, the static power consumption is also measured, whose average value is calculated as $595\mu W$.

V. Conclusion

The conclusion of this project is presented in this section. A 1-bit low-pass first-order DSM A/D is designed in this project. The project starts with the algorithm feasibility testing via the Simulink simulations, which is covered in *Section II*; then the corresponding architecture is mapped to the circuit level with the help of Cadence Virtuoso, where is PreLS tests are conducted, which has been discussed in *Section III*. After the discussion of all circuit blocks be used, the whole DSM module layout is constructed who includes all parasitic effects; and PreLS results are presented and discussed in *Section V*.

Some testing constrains are applied to the simulations to achieve better performance, for instance, using two-phase clock scheme instead of four-phase to mitigate clock feeding issues. The clock circuit issues can be possibly solved by increasing some delay time among those clock signals. Due to the limited time of the writer, this path is not deeply investigated. Another method is to refine the transmission gate by introducing dummy gates to thereby reduce clock feeding issues. The third concern will be the Miller integrator problem happens when the input signal reaches around its minimal voltage value. In the future work, these issues should be solved to improve the SNR performance.

As a summary, all the resulted values are condensed in *Table II*. With these provided information, one can conclude that the design meets all the requirements in the system level. As noted, the power consumption is not explicitly restricted, and the frequency bandwidth, oversampling frequency, and input signal fundamental frequency, are all related to the provided algorithm that differentiates different designs, therefore those numbers will be altering by people.

Table II: Specifications summary of 1-bit DSM A/D

Specifications	Matlab	Cadence PreLS	Cadence PLS	Requirement
Power supply (V)	1.2	1.2	1.2	1.2
$f_{bandwidth}$ (kHz)	23.58	23.58	23.58	-
SNR (dB)	82.49	63	61.27	≥ 60
Analog ground	0.6V	0.6V	0.6V	0-0.6V
Input voltage range (V)	± 0.4	± 0.4	± 0.4	$\geq \pm 0.2$
$f_{sinwave}$ (kHz)	10	10	10	-
OSR	443	103	90.92	≥ 81.84
$f_{oversampling}$ (MHz)	4	4	4	-
Power (μW)	-	-	595	-

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Appendix

The structure of the project workspace is as follow. There are in total 11 folders are related to the design that all start with the prefix *project*. The table below lists all the directories that contain project content. All these folders are under the directory: "/home/zli133/cmosp13/ecse534/".

Table III: Project workspace navigator

Folder name	Content
project_4phase_clk	four-phase clock circuit
project_backup	backup folder for the project
project_D-latch	D-latch circuit
project_dsm	1-bit DSM A/D
project_inv	inverter
project_nor	NOR gate
project_ota	OTA circuit
project_comp	comparator circuit
project_trans_gate	transmission gate
project_tb	testbench for individual components
project_tb2	testbench for extracted DSM

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