ECSE 536 RF Microelectronics – Assignment 3

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***Abstract*—This is the report for the third assignment.**

***Keywords*—Assignment, CMOS Mixer, Gilbert Cell**

I. Design Methodology

A doubly-balanced CMOS Gilbert Cell mixer is designed in this project, whose basic circuit diagram has been given in the assignment handout, which is shown in Fig. 1. A certain specifications are asked to meet. Before starting the design, it is very important to make sure that all MOSFET transistors are biased at the saturation region to make sure the largest linearity can be achieved. Here, the V_{LO} and V_{RF} will be fed to the Gilber cell using balun to provide differential input, where the balun circuit schematic is presented in Fig. 2. R_{CPL} provides an isolation from the V_{in+} and V_{in-} to the DC biasing configured by the M_{BIAS}, and C_{CPL} is responsible for filtering out low frequency components.

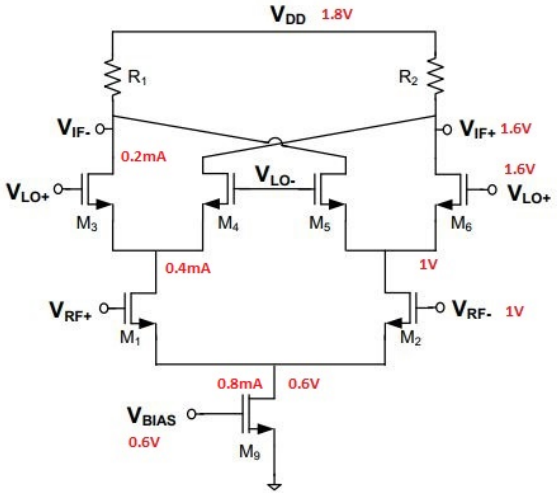

Figure 1: A doubly-balanced Gilbert Cell mixer with the ideal voltage and current biasing plan (in red)

Again, since it is desired to bias all transistors in saturation mode, with the fact that the required power consumption is less than 15mV, with a 1.8V power supply, which means the total DC current should be around 8.33mA. Here, the same transistor model (threshold voltage $V_T = 0.35V$) from the last assignment is employed, whose channel length L is selected as $0.18\mu m$ since it has a balanced performance as we investigated by parameter sweeping from the last assignment; the channel width W has a degree of freedom from $1 - 400\mu m$. In order

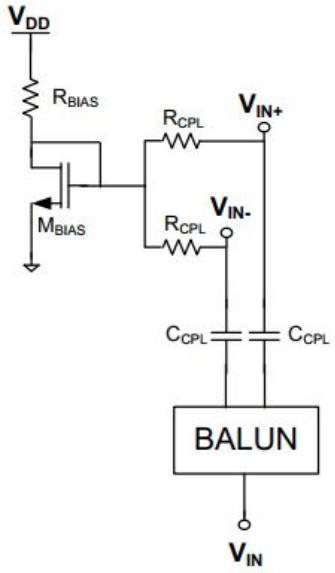

Figure 2: A balun circuit to provide differential output from single ended signal

to have a clear design methodology of the whole circuit, the following algorithm is proposed (refer to Fig. 1 and Fig. 2):

First, set $V_{BIAS} = 0.6V$, do the parametric sweeping of W_{BIAS} of M_9 so that $I_{D,M9} \approx 0.8mA$ and $V_{D,M9} \approx 0.6V$;

Second, set $V_{RF,DC} = 1V$, and do the parametric sweeping of W_{RF} of both M_1 and M_2 so that $I_{D,M1} = I_{D,M2} \approx 0.4mA$ and $V_{D,M1} = V_{D,M2} \approx 1V$;

Third, set $V_{LO,DC} = 1.6V$, and do the parametric sweeping of W_{LO} of both M_3, M_4, M_5 and M_6 so that $I_{D,M3} = I_{D,M4} = I_{D,M5} = I_{D,M6} \approx 0.2mA$ and $V_{IF} \approx 1.6V$;

Fourth, calculate the value for R_1 and R_2;

Fifth, configuring the balun DC biasing networks by properly selecting R_{BIAS} for RF and LO separately, and sweeping both $W_{RF,BIAS}$ and $W_{LO,BIAS}$ simultaneously so that $V_{RF,DC} = 1V$ and $V_{LO,DC} = 1.6V$;

Sixth, testing the circuit to see if it meets the desired specifications, if the gain and linearity do not meet the specifications, go back to step *First* to *Fifth* to either increase $I_{D,M9}$, alter W or decrease $V_{DC,BIAS}$.

By following this algorithm, after some iterations and parameter sweepings, the following component values have been selected (Table I) that are all within the given interval. The voltage and current at every single node are also summarized in Table II.

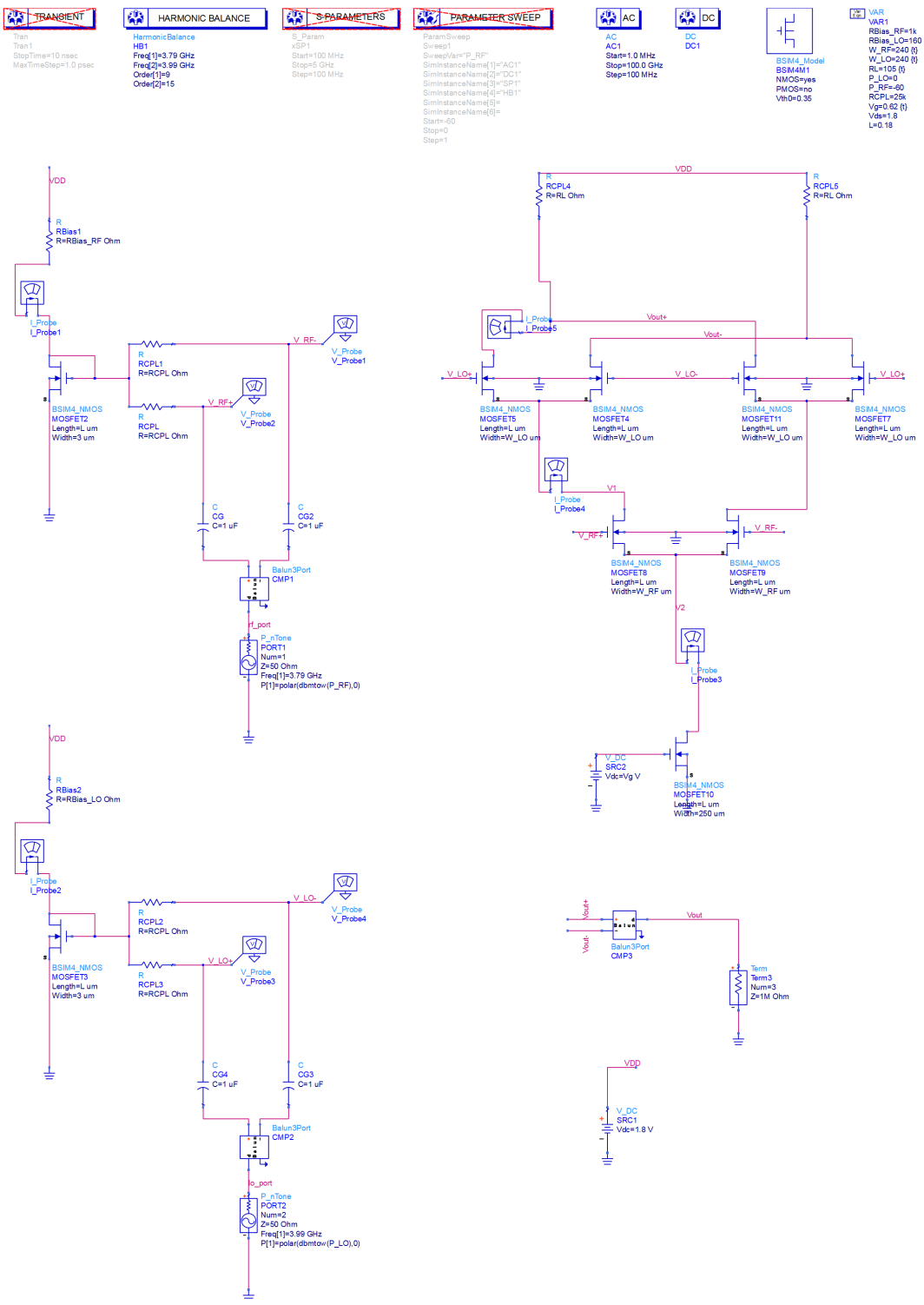

Figure 3: The entire doubly-balanced mixer design; the RF/LO terminal ports are 50Ω, and the load impedance is $1M\Omega$

Table I: CMOS mixer component values

L	W_9	W_1 - W_6	R_1 - R_2	C_{CPL}	R_{CPL}	$W_{LO,BIAS}$ and $W_{RF,BIAS}$	$R_{LO,BIAS}$	$R_{RF,BIAS}$
$0.18\mu m$	$250\mu m$	$240\mu m$	105Ω	$1\mu C$	$25k\Omega$	$3\mu m$	160Ω	$1k\Omega$

Table II: Voltage and current value at every single critical node

V_{BIAS}	$V_{RF,DC}$	$V_{LO,DC}$	$V_{IF,DC}$	$V_{D,M9}$	$V_{D,M1}$	$I_{D,M9}$	$I_{D,M1}$	$I_{D,M3}$
0.62V	1.037V	1.509V	1.368V	0.425V	0.9V	8.23mA	4.116mA	2.058mA

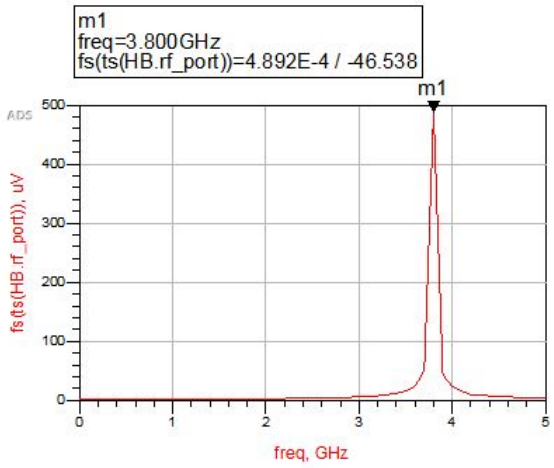

Figure 4: RF input signal when $P_{RF} = -60dBm$

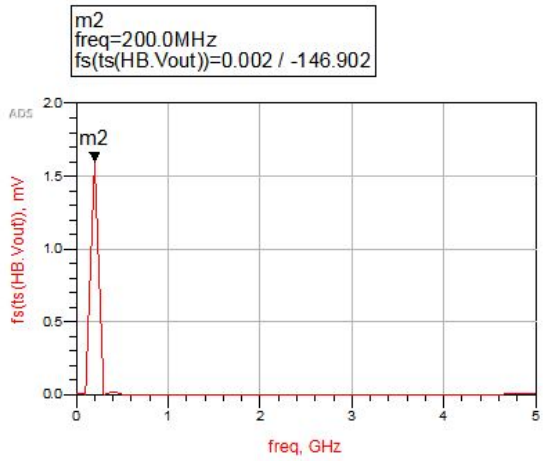

Figure 5: IF output signal when $P_{RF} = -60dBm$

It is clear that for every transistor they are in saturation mode since $V_D > V_G - V_t$ is valid for all of them. The whole circuit schematic is given in Fig. 3 for reference. Now each specification is measured.

II. Specification Checking

Before the simulation setup, it is worth to note that the order number that the author defined for RF signal is 9 and for LO signal is 15 for the harmonic balance simulation configurations in order to obtain reasonable results, which is very important when considering $IIP2$ and $IIP3$ specifications.

A. Voltage Gain

Since the mixer is not matched, we care more about the conversion gain by the voltage rather than the power gain. Given the RF signal's frequency $f_{RF} = 3.79GHz$ and local oscillator's frequency $f_{LO} = 3.99GHz$, which means $f_{IF} = 200MHz$; also the power for RF signal is $P_{RF} = -60dBm$ and the power for local oscillator's signal is $P_{LO} = 0dBm$. The input and output signal in the frequency domain in terms of voltage are presented in Fig. 4 and Fig. 5, where the gain is about $20log_{10}(1.6mV/488\mu V) = 10.45dB$, which is larger than $10dB$.

noisefreq	nf		
	nf(1)	nf(2)	nf(3)
200.0 MHz	0.000	0.000	5.936

Figure 6: SSB noise figure

B. SSB Noise Figure

The single-side-band noise figure is found by harmonic balance in between RF port and IF port at $f_{IF} = 200MHz$, which is defined as $nf(3)$ in ADS, whose value is given in Fig. 6. Again, 5.936dB is smaller than 10dB, meeting the specification.

C. 1-dB Compression

As noted by the assignment handout, finding 1-dB compression point in voltage domain requires a simple conversion from power to voltage as the mixer is not matched. If one increased the input RF power from -60dBm to 0, the output signal power versus the input RF power is illustrated in Fig. 7, where the 1-dB compression point in power fashion is about -11dBm at the RF input port. Then we defined $P_{RF} = -11dBm$ and

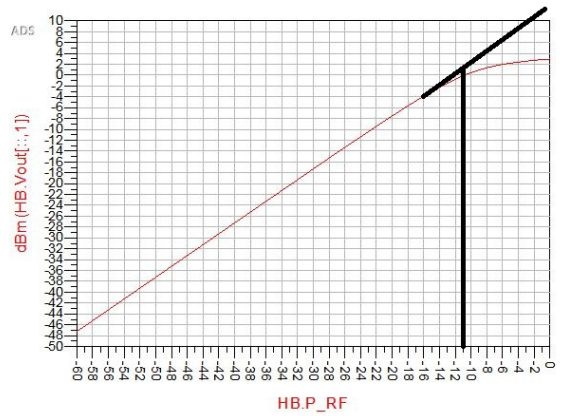

Figure 7: Harmonic balance simulation for 1-dB compression point in power fashion; the input RF power increased from -60dBm to 0 and the output power is tracked; when the input power source is about -11dBm, a -1dB compression happens

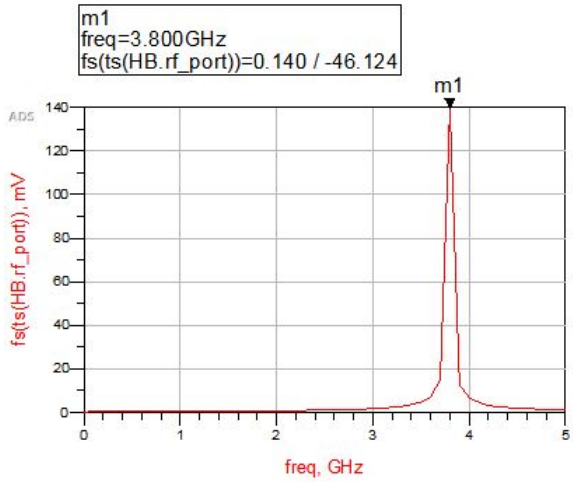

Figure 8: The voltage of the corresponding -11dBm power from the RF input source when it is -11dBm

conducted the *Fourier Transform* at IF port, the output voltage signal in frequency domain is given in Fig. 8, whose peak value is 140mV that is the 1-dB compression point for this unmatched mixer, which is way larger than 100mV that is given as the required specification, meaning it is a positive result.

D. IIP2 Test

The IIP2 test is a bit tricky. First, two RF tones that are symmetric to the 3.79GHz that is f_{RF} has been picked, which are $f_{1,IIP2} = 3.70GHz$ and $f_{1,IIP2} = 3.88GHz$, 180MHz apart from each other. The reason of selecting these two tones is because since $f_{IF} = 200MHz$ and for the low-side second harmonic IM2:

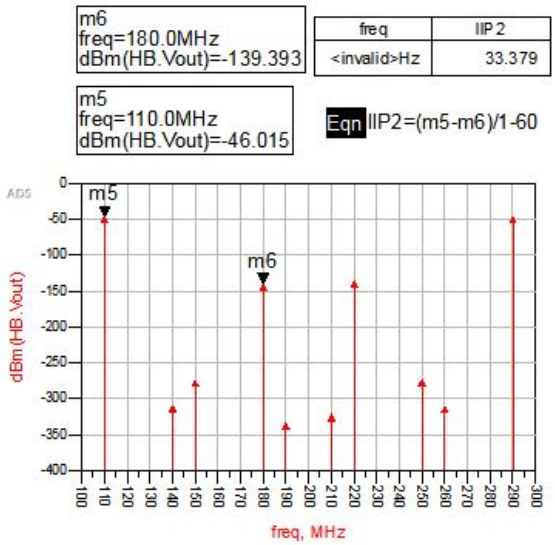

Figure 9: IIP2 harmonic balance simulation

$$f_{IM2} = f_{1,IIP2} - f_{2,IIP2} = 180MHz \quad (1)$$

Which is very close to f_{IF}. Therefore, this tone selection can better reflect how IM2 influence the IF signal sitting at 200MHz. Be reminded that here the order defined for RF signal is 9 and for LO signal is 15 so that an accurate result will be achieved. Fig. 9 shows the harmonic balance simulation of IIP2, where by looking at the tone at 180MHz ($m6$) and 110MHz ($m5$) where the later is the fundamental signal after the mixing ($f_{LO} - F_{1,IIP2} = 3.99 - 3.70 = 180MHz$), the IIP2 is calculated by:

$$IIP2 = \frac{-46.015 + 139.393}{2 - 1} - 60 = 33.379dBm \quad (2)$$

Which is also shown in Fig. 9. We then defined the input RF power as this number and do the conversion of the time mode signal to the frequency spectrum at *rf_port* in Fig. 3 to see its corresponding peak voltage, which is shown in Fig. 10, suggesting that the peak IIP2 is 24.935V, and it is larger than 10V, suggesting that it meets the IIP2 requirement.

E. IIP3 Test

For IIP3 test that is exactly like what we did in previous assignment, a two-tone test that is 20MHz apart with each other by symmetric with respect to f_{RF} have been selected, which are $f_{1,IIP3} = 3.791GHz$ and $f_{2,IIP3} = 3.889GHz$, respectively. After the mixer, the fundamental frequency tone will be located at 197MHz ($f_{LO} - f_{1,IIP3} = 3.99 - 3.791 = 199MHz$), and the Also by conducting harmonic balance simulation, the result is presented Fig. 11, where IIP3 is calculated by:

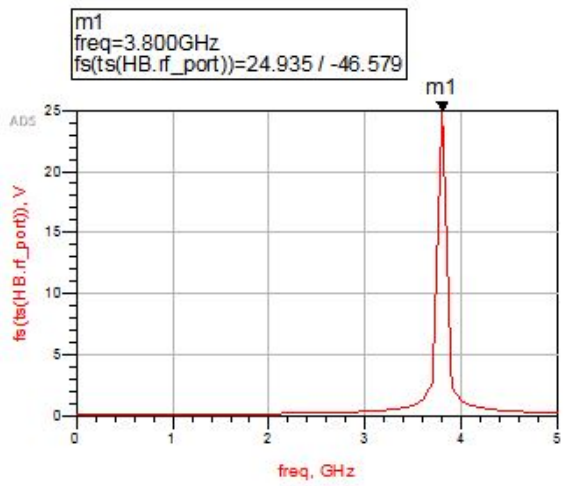

Figure 10: IIP2 peak voltage for $R_{RF} - 33.379dBm$

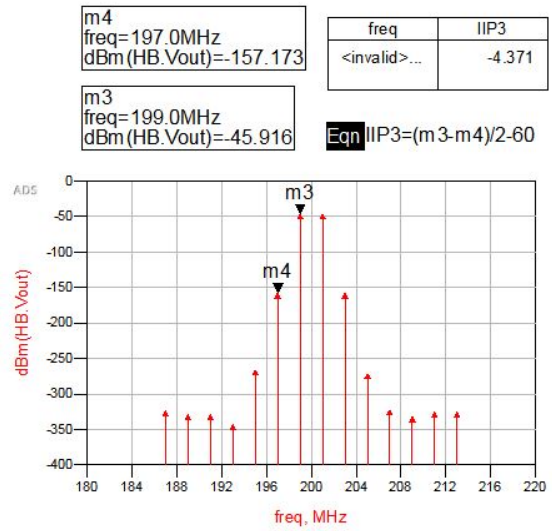

Figure 11: IIP3 harmonic balance simulation

$$IIP3 = \frac{-45.916 + 157.173}{3-1} - 60 = -4.371dBm \quad (3)$$

Similar to IIP2 test, We then defined $P_{RF} = -4.371dBm$ and probe the RF input port *rf_port* for retriving its voltage, which is shown in Fig. 12 that is 318mV, which is larger than 300mV and it also meets the specification.

F. Port-to-Port Isolation

Three kinds of port-to-port isolations are considered in this assignment, which are: RF-IF isolation, LO-IF isolation, and LO-RF isolation. For the RF-IF isolation, the harmonic balance is conducted at the *rf_port* in Fig. 3 and the result is shown

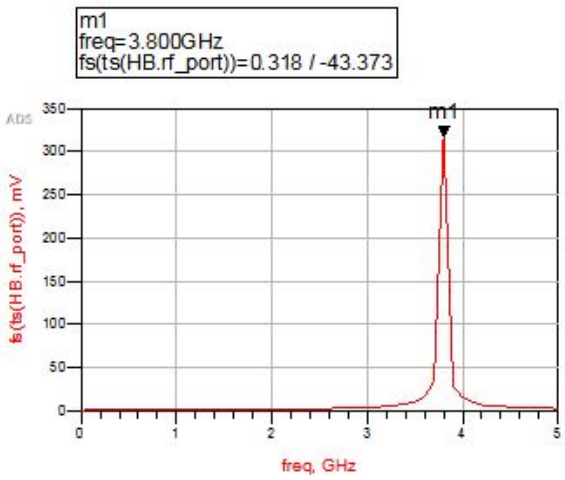

Figure 12: IIP3 IF port voltage when $P_{RF} = -4.371dBm$

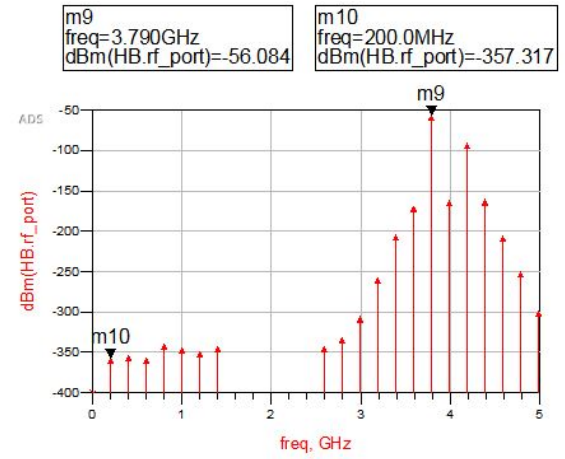

Figure 13: Harmonic balance simulation at *rf_port* in Fig. 3

in Fig. 13, where $m9$ is the RF signal and $m10$ is the IF signal, where the RF-IF isolation is calculated as $-56.084 - (-357.317) = 301.23dB$, and it meets the 100dB isolation specification.

Similarly, the LO-IF isolation is found by doing harmonic balance simulation and probing *lo_port*, whose result is shown in Fig. 14, where $m11$ is the LO signal and $m13$ is the IF signal, which suggests $3.811 - (-348.521) = 352.332dB$.

By looking at the same figure, for the calculation of LO-RF isolation, $m12$ is the RF signal, which gives a $3.811 - (-115.318) = 119.129dB$ LO-RF isolation. Therefore, both LO-IF and LO-RF isolation meet the specification.

III. Conclusion

We conclude this assignment report by summarizing the specifications obtained from the actual design compared with

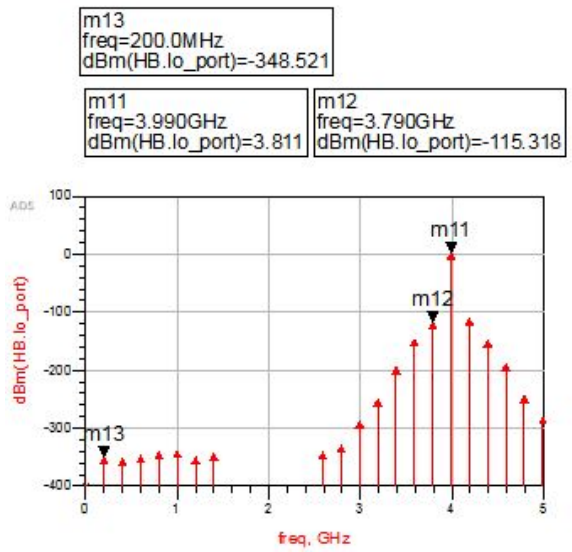

Figure 14: Harmonic balance simulation at *lo_port* in Fig. 3

Table III: Some critical specifications of the design

Parameters	Desired specs.	design specs.	Meet the specs.?
Voltage gain	$> 10dB$	10.45dB	Yes
SSB noise figure	$< 10dB$	5.93dB	Yes
1-dB compression point	$> 100mV(peak)$	140mV	Yes
IIP2	$> 10V(peak)$	24.935V	Yes
IIP3	$> 300mV(peak)$	318mV	Yes
RF to IF isolation	$> 100dB$	$301.23dB$	Yes
LO to IF isolation	$> 100dB$	$352.332dB$	Yes
LO to RF isolation	$> 100dB$	$119.129dB$	Yes
Supply voltage	1.8V	1.8V	Yes
Power consumption	$< 15mV$	14.84mV	Yes

the desire values, which is presented in Table III. It is shown that the design sucessfully meets all the specifications.

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