ECSE 536 RF Microelectronics – Assignment 2

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***Abstract*—This is the report for the second assignment.**

Keywords*—*Assignment

I. Part I

A. Question 1

Question: Explain the shape of the curves obtained in question 1, parts (b) and (c). Why do both the DC gain and the unity gain frequency have such a weak dependence on W?
Answer:

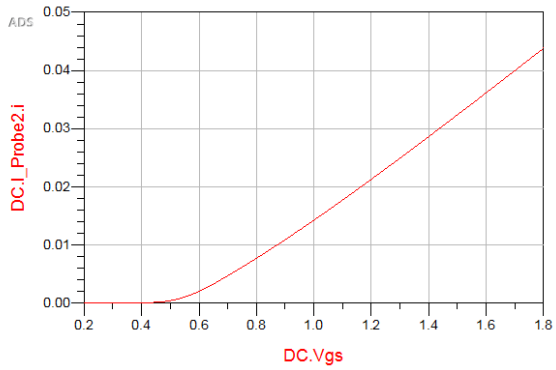

Figure 1: Drain current vs. sweeping of V_{gs}

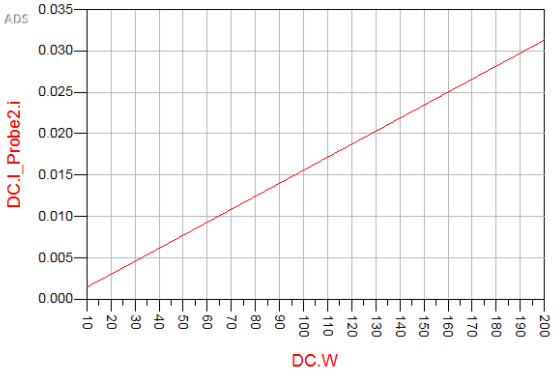

Figure 2: Drain current vs. sweeping of W

All the pictures collected from (a)-(e) from question 1 in part 1 are plotted in Fig. 1 - Fig. 15, and Fig. 16 is the circuit schematic for the measurement. For (a) - (c) the output port

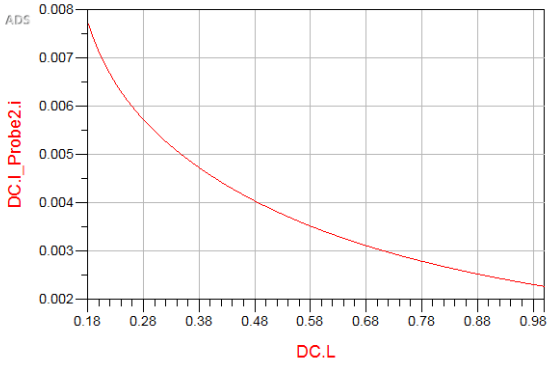

Figure 3: Drain current vs. sweeping of L

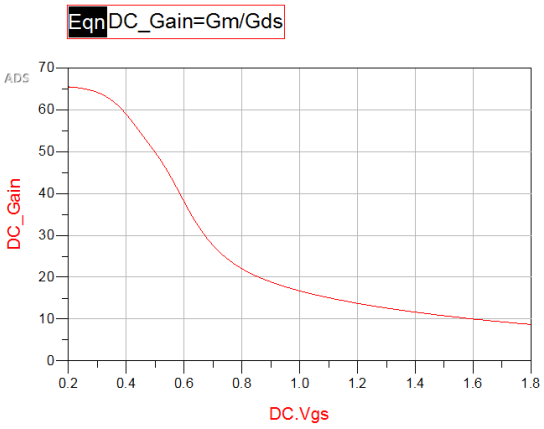

Figure 4: Intrinsic DC voltage gain vs. sweeping of Vgs

is shorted. For S_{21} and noise figure test, the signal source is set with center frequency as 5.79GHz, determined by the algorithm on the assignment. The current meter "I_Probe2" is measuring the drain current "coming out from the NMOS" since the connection is reversed.

It can be seen from Fig. 4 - Fig. 6 that the increase of transistor L will increase the DC intrinsic gain, whereas the increase of V_{gs} and W will decrease the DC intrinsic gain. However, in Fig. 7 - Fig. 9, the increase of L cause the decrease of the unity gain frequency f_T whereas the increase of V_{gs} and W will increase f_T. This phenomena reveals the property of constant gain-bandwidth product: the trade-off in-between the gain and bandwidth.

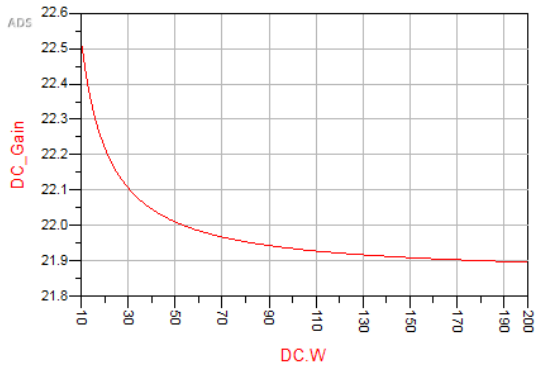

Figure 5: Intrinsic DC voltage gain vs. sweeping of W

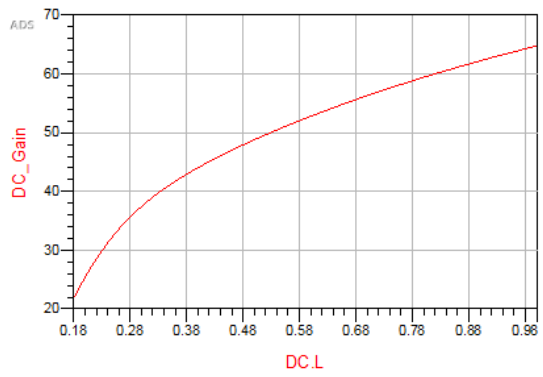

Figure 6: Intrinsic DC voltage gain vs. sweeping of L

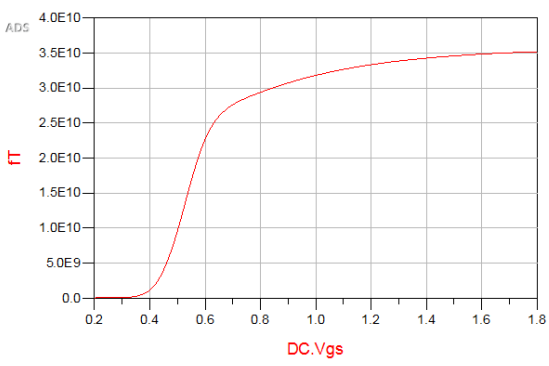

Figure 7: Unity-gain frequency f_T vs. sweeping of V_{gs}

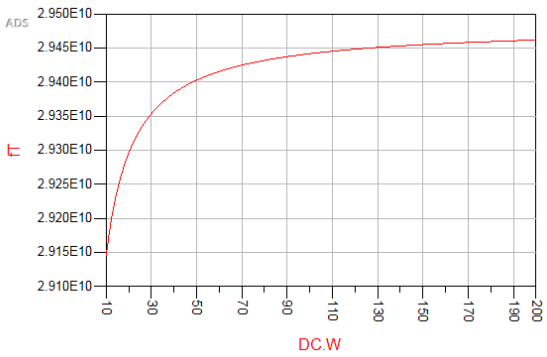

Figure 8: Unity-gain frequency f_T vs. sweeping of W

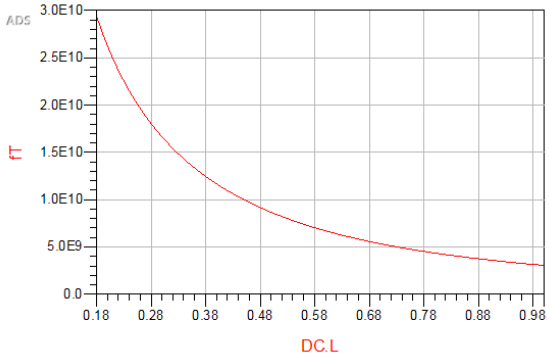

Figure 9: Unity-gain frequency f_T vs. sweeping of L

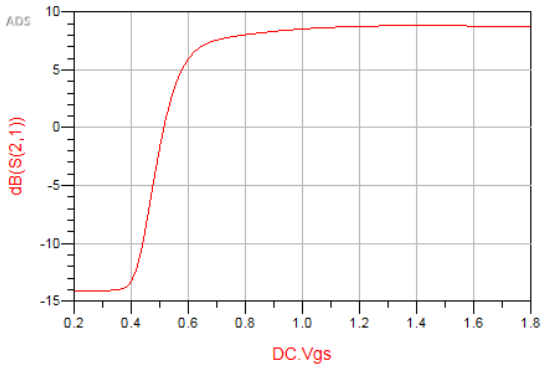

Figure 10: $|S_{21}|$ (dB) vs. sweeping of V_{gs}

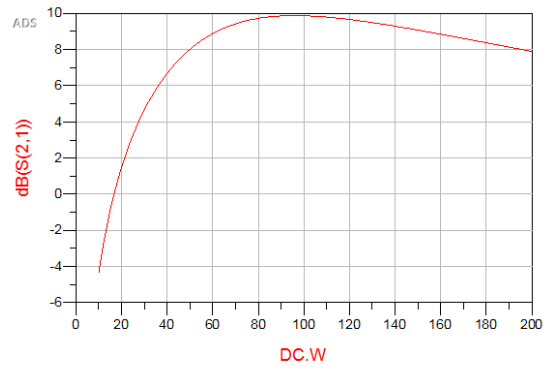

Figure 11: $|S_{21}|$ (dB) vs. sweeping of W

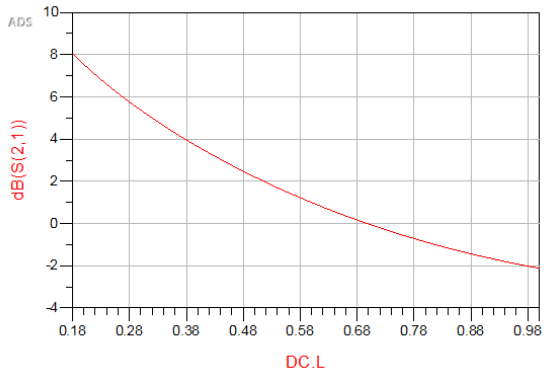

Figure 12: $|S_{21}|$ (dB) vs. sweeping of L

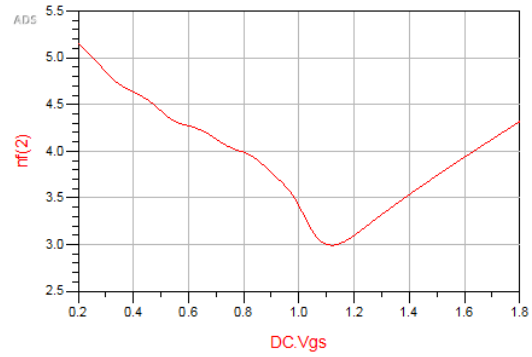

Figure 13: Noise figure (dB) vs. sweeping of V_{gs}

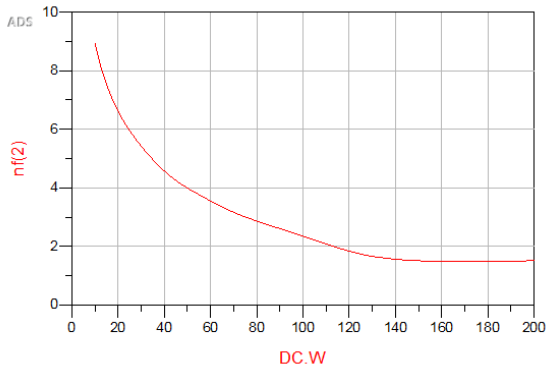

Figure 14: Noise figure (dB) vs. sweeping of W

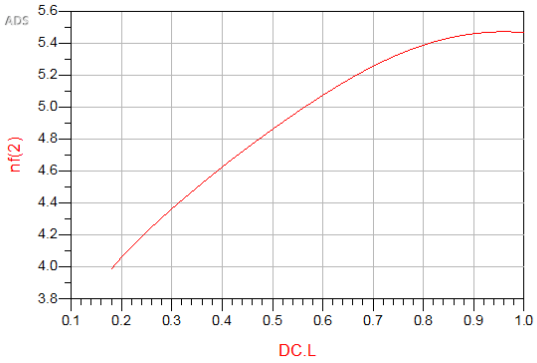

Figure 15: Noise figure (dB) vs. sweeping of L

The DC intrinsic voltage gain is defined as:

$$|Gain| = \frac{g_m}{g_0} = g_m r_0 \tag{1}$$

And the transconductance g_m is defined as (where V_{gs} represents large signal model; all analyses are done in saturation region):

$$g_m = \left.\frac{\partial I_d}{\partial V_{gs}}\right|_{V_{ds}=constant} \approx \mu_n C_{ox} \frac{W}{L} V_{ov} \tag{2}$$

Where mu_n is the n-type MOSFET charge mobility, C_{ox} is the gate oxide capacitance, and $V_{ov} = V_{gs} - V_{th}$. The similar analysis goes for g_0:

$$g_0 = \frac{1}{r_0} = \left.\frac{\partial I_d}{\partial V_{ds}}\right|_{V_{gs}=constant} \approx \frac{\mu_n C_{ox}}{2} \frac{W}{L} \frac{\lambda_n}{L} V_{ov}^2 \tag{3}$$

Where λ_n is the slope of $I_d - V_{gs}$ characteristic in saturation region caused by the Early effect, which is a constant. If one use Eq. 2 divided by Eq. 3:

$$|Gain| = \frac{g_m}{g_0} = g_m r_0 = \frac{2L}{\lambda_n V_{ov}} \tag{4}$$

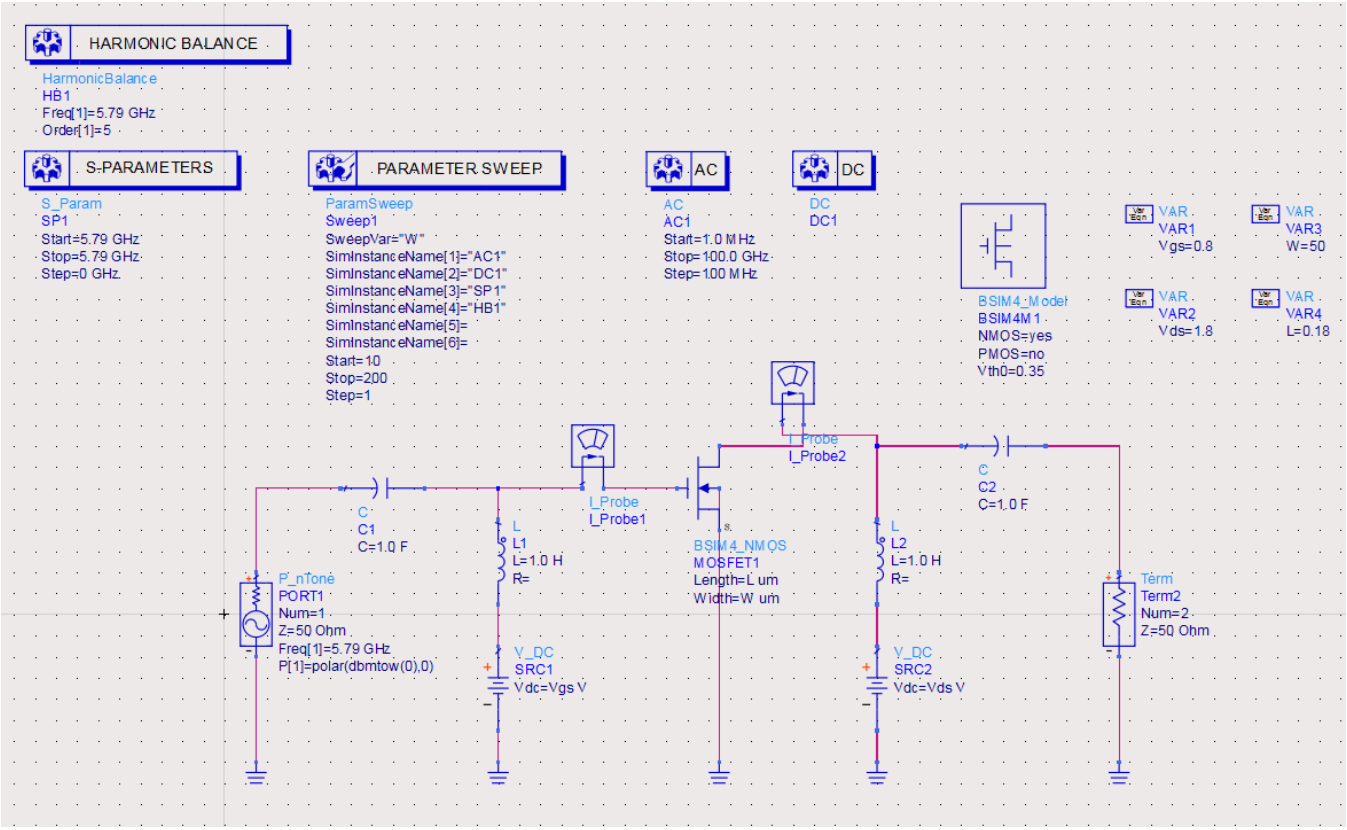

Figure 16: Circuit schematic for part 1.

So from Eq. 4 one can see that the intrinsic gain has the correlation to the length L os the transistor as well as the overdriven voltage V_{ov}, or essentially, V_{gs} since the threshold voltage of a transistor is constant at the constant temperature.

The unity frequency is defined as the frequency point where the short circuit current gain (NOT DC intrinsic voltage gain) is unity, which can be found as:

$$f_T = \frac{g_m}{2\pi(C_{gs}+C_{gd})} = \frac{g_m}{2\pi C_g} \approx \frac{g_m}{2\pi C_{ox} W L} \tag{5}$$

Where C_{gs} and C_{gd} is the gate-to-source and gate-to-drain capacitance, respectively, and $C_g = C_{ox}WL$. Substituting Eq. 2 to Eq. 5 one can find that:

$$f_T = \frac{\mu_n V_{ov}}{2\pi L^2} \tag{6}$$

Therefore, f_T correlates strongly with L and V_{gs} than W. Eq. 4 and Eq. 6 explain the phenonema seen from Fig. 4 - Fig. 9.

B. Question 2

Question: Explain the shape of the curves obtained in question 1, parts (d) and (e).

Answer: Many of these phenomena will be related to their physical properties, therefore it is hard to find analytical mathematical expressions to explain individual picture here. For Fig. 10, the transistor is off when $V_{gs} < V_{th}$ and there is almost no gain (S_{21}); when it increases until larger than V_{th}, the gain drastically boost since it enters the saturation region of the VTC of a MOSFET, and then it quickly saturates as the gain becomes a constant.

The increasing of W manipulates the input resistance of the transistor and when W is around $100\mu m$ a maximum insertion gain S_{21} is achieved since the network is matched, then further increasing W will decreases the gain. The same analogy is applicable for L, where the gain keeps decreasing.

Regarding the noise figure (NF) of this common-source configuration amplifier under the test, it has been shown in [1] that

$$NF = \frac{\gamma}{g_m R_s} + 1 \tag{7}$$

where γ is technology dependent parameter of a MOSFET, and R_s is the source resistance. If substituting Eq. 2 to Eq. 7, therefore:

$$NF = \frac{\gamma}{(\mu_n C_{ox} \frac{W}{L} V_{ov}) R_s} + 1 \tag{8}$$

Based on this equation, it is easy to tell that NF is inversely proportional to W and proportional to L; this justifies the shape

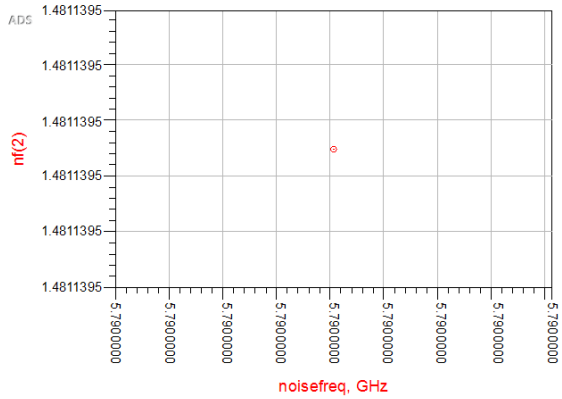

Figure 17: Noise figure for $V_{gs} = 0.8V$, $W = 180\mu m$, and $L = 0.18\mu m$

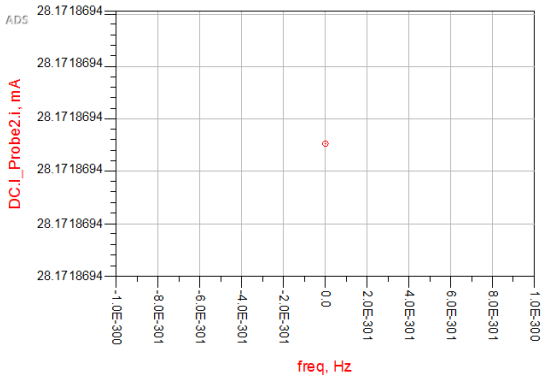

Figure 18: Drain current consumption for $V_{gs} = 0.8V$, $W = 180\mu m$, and $L = 0.18\mu m$

of the curve in Fig. 14 and Fig. 15; regarding the correlation of NF to V_{gs}, V_{gs} should be also inversely proportional to NF when $V_{gs} > V_{th}$. In Fig. 13, however, NF starts to increases after about $V_{gs} \approx 1.1V$, which might be caused by the non-linearity issue.

C. Question 3

Question: What is the maximum usable frequency of this transistor? What values for V_{GS}, W, and L would you use to obtain this frequency?

Answer: It can been seen from Fig. 7 - Fig. 9 that: $V_{gs} = 1.8V$, $W = 200\mu m$, and $L = 0.18\mu m$ should yield the highest $f_T = 3.5 * 10^{10} Hz$ (Fig. 7).

D. Question 5

Question: Based on the above plots, what values for V_{gs}, W, and L would you pick to obtain the minimum noise figure at your design center frequency? What would the current consumption be?

Answer:At center frequency $f_0 = 5.79GHz$, when: $V_{gs} = 0.8V$, $W = 200\mu m$, and $L = 0.18\mu m$ should yield the best NF performance $NF = 1.48$ (Fig. 17). The resulted drain current consumption is reported in Fig. 18 as about 28.17mA. This configuration will be used for Part II.

II. Part II

A. Finding Γ_S, Γ_{in}, Γ_L, and Γ_{out}

The source/load stability circle, constant noise-figure circle, and constant available gain G_A circle are all plotted in Fig. 19. Here it is very important to clarify the design methodology to meet the expect specifications. Table I summaries the goal of this design in this part. It is also noted that the device is not unconditionally stable.

Rather than directly establishing a correlation on meeting NF and power gain requirement while having both input and output stable, instead, fixing one condition while finding the

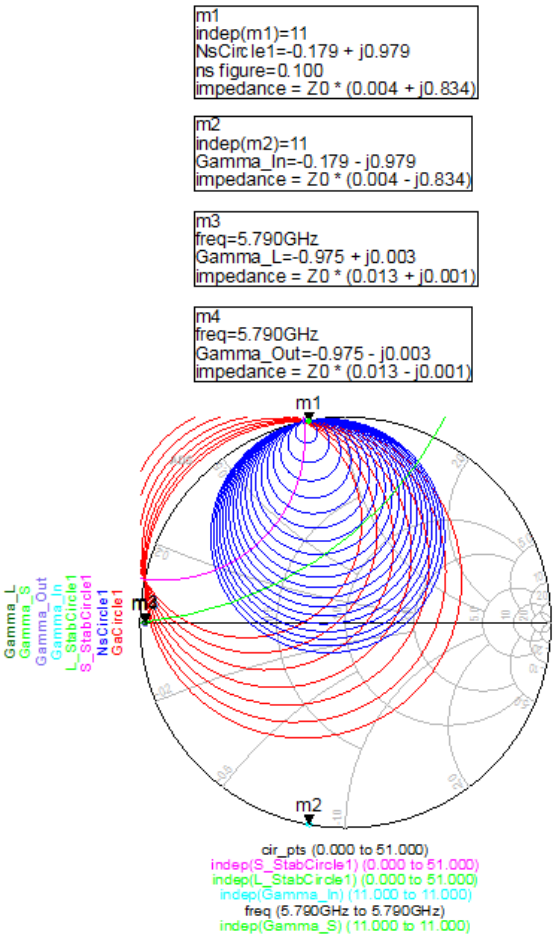

Figure 19: Source/load stability circle (pink/green), constant noise-figure (0-2dB) circle (blue), and constant available gain (5-11dB) G_A circle (red). $m1$: Γ_S, $m2$: Γ_{in}, $m3$: Γ_L, and $m4$: Γ_{out}

Table I: Desired specifications at 5.79GHz

Specifications	Goal
Stability	Conditionally stable
Noise figure (NF)	$<$ 0.15dB
Power gain $20log_{10}S_{21}$	$>$ 9dB

Table II: S-parameters at 5.79GHz

S-Parameter	Mag/Deg
S_{11}	0.18/-139.8
S_{12}	0.173/9.48
S_{21}	2.622/94.11
S_{22}	0.514/-134.86

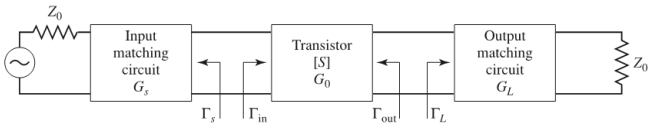

Figure 20: A general impedance matching network

way to meet another specification is a good strategy. Here, NF is fixed at about 0.1dB. G_A can be determined by the following formula:

$$G_A = \frac{1-|\Gamma_S|^2}{|1-S_{11}\Gamma S|^2}|S_{21}|^2\frac{1}{1-|\Gamma_{out}|^2} \tag{9}$$

Where Γ_{out} is:

$$\Gamma_{out} = S_{22} + \frac{S_{12}S_{21}\Gamma_S}{1-S_{11}\Gamma_S} \tag{10}$$

If one substitute Eq. 10 to Eq. 9:

$$G_A = \frac{1-|\Gamma_S|^2}{|1-S_{11}\Gamma S|^2}|S_{21}|^2\frac{1}{1-|S_{22}+\frac{S_{12}S_{21}\Gamma_S}{1-S_{11}\Gamma_S}|^2} \tag{11}$$

Therefore, G_A is a function of only Γ_S. On the other hand, it is also possible to correlate Γ_L with Γ_S. For conjugate matching, Γ_L is calculated by:

$$\Gamma_L = \Gamma_{out}^* \tag{12}$$

Substituting Eq. 10 to Eq. 12 one can also relate Γ_L with Γ_S, under conjugate matching. After finding out Γ_L, Γ_{in} can be calculated as:

$$\Gamma_{in} = S_{11} + \frac{S_{12}S_{21}\Gamma_L}{1-S_{22}\Gamma_L} \tag{13}$$

Therefore, essentially there is only one parameter. Γ_S, that determines all specifications. In order to have input and output stable for conjugate matching, Γ_S should be outside the source stability circle, and Γ_L should be outside the load stability circle so that it is conditionally stable, with the condition that $|S_{11}| < 1$ and $|S_{22}| < 1$. Therefore, it is proposed that:

- *Zeroth*, check if $|S_{11}| < 1$ and $|S_{22}| < 1$.
- *First*, choose a marker on the smith chart that meets the NF specifications as Γ_S that is outside the source stability circle.
- *Second*, retrieve G_A using Eq. 11 (or G_A circles in Fig. 19) and also find out the value of $20log_{10}S_{21}$ to see if it meets the requirement.
- *Third*, using the relationship derived in Eq. 12 to find Γ_L that should be outside the input load circle. If not, go back to first step. If everything meets the specifications, Γ_S and Γ_L are determined.

By following this approach, the S parameters are summarized in Table II, where S_{11} and S_{22} are both smaller than 1. All the reflection coefficients are labelled in Fig. 19, where marker $m1$ and $m3$ that correspond to Γ_S and Γ_L are indeed outside the source and load stability circle, which is highlighted in pink and green colour, respectively.

Therefore, by selecting $\Gamma_S = 0.938/98.403$ at marker $m1$ in Fig. 19, a $G_A = 11dB$, $20log_{10}S_{21} = 8.372dB$, $NF = 0.1dB$, and $\Gamma_L = 0.933/176.338$ has been achieved, where both Γ_S and Γ_L are within the stable region. Using the following formula to convert from reflection coefficient to normalized impedance:

$$\begin{aligned} \bar{z_L} &= \frac{1+\Gamma_L}{1-\Gamma_L} \\ \bar{z_S} &= \frac{1+\Gamma_S}{1-\Gamma_S} \end{aligned} \tag{14}$$

The normalized loading impedance is $\bar{z_S} = 0.004 + j0.834$ and $\bar{z_L} = 0.013 + j0.001$ in linear scale.

B. Impedance Matching

A general impedance matching network can be summarized in Fig. 20, where the characteristic impedance is 50 Ω here. We will do the output matching first and then do the input matching. In order to finish the impedance matching (conjugate matching), we will match $Z_S = Z_{in}^*$ and $Z_L = Z_{out}^*$.

1) Output Matching Network: To complete the output matching, one can refer to Fig. 19, and we need to make the following condition satisfy: the origin of the smith chart should be shifted to $m3$ for matching $Z_L = Z_{out}^*$ to make the load impedance to be $Z_0 \times (0.013 + j0.001)$. Therefore, conceptionally, a shunt inductor then a series capacitor should do the job. There are some options to do so, either using manual calculations, built-in ADS Smith chart matching wizard, or manual parameter tuning. Here the built-in Smith chart utility is used. By doing so, the following matching circuit is constructed with the serial capacitance $C = 4.81pF$ and shunt inductance $L = 157.33nH$. The corresponding Smith chart is in Fig. 21.

2) Input Matching Network: The input matching will be similar as the output matching. Here we need to matching Z_{in} to 50Ω, which means we need to shift $m2$ to the origin of smith chart in Fig. 19. By looking at a Smith chart, a series

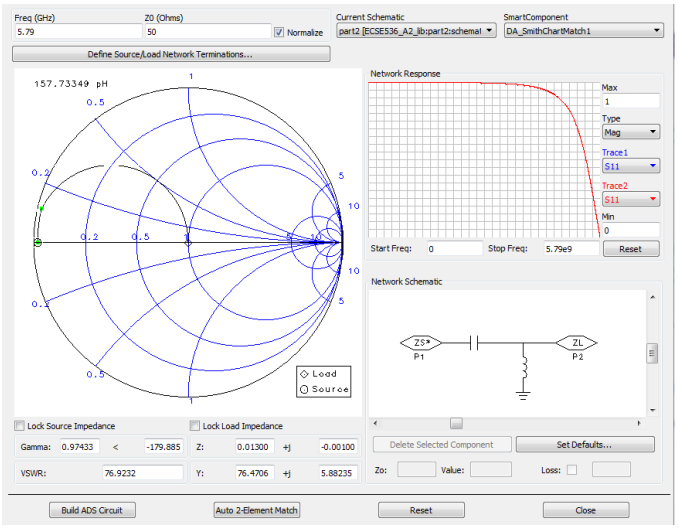

Figure 21: Smith chart for completing the matching. A series capacitor with a shunt inductor does the matching; The matching is done from load to source, where Z_0 is the load, and Z_{in} is the source; for conjugate matching, Z_L=Z_{in}^*

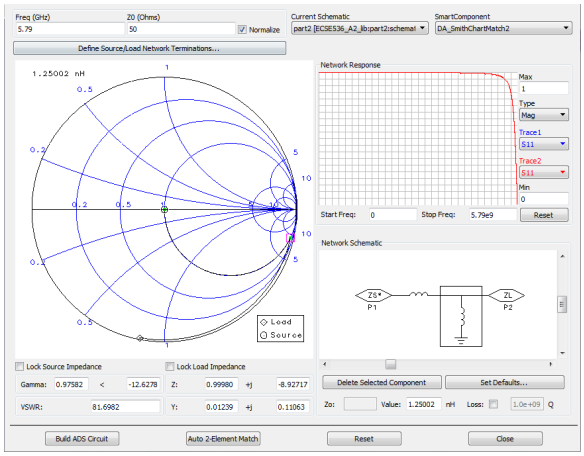

Figure 22: Smith chart for the input matching, which contains a shunt inductor and a series conductor. The matching is done from load to source, where Z_{in} is the load and Z_0 is the source

inductor and a shunt inductor should do the job. The Smith chart utility is used again and the matching diagram is shown in Fig. 22, where the series inductor has a $L = 12.70nH$, and a shunt inductor with a $L = 1.25nH$. Practically, the shunt inductor in the load matching network will be hard to make within the chip as its inductance is relatively large.

C. Result Summary

After the matching network finished, the S-parameters are summarized in Table III, and the NF is in Fig. 23, which is $NF = 0.097dB$, the power gain $20log_{10}S_{21} =$

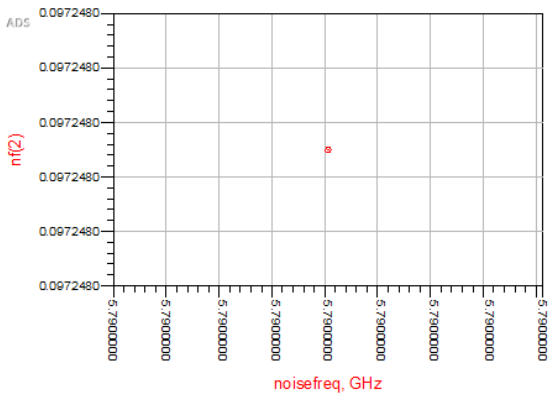

Figure 23: Noise figure of the matched amplifier (dB)

$20log_{10}(|3.105|) = 9.84dB$, all meet the specifications. The input and output impedance can be found by:

$$Z_{in} = Z_0\frac{1+\Gamma_{in}}{1-\Gamma_{in}}$$
$$Z_{out} = Z_0\frac{1+\Gamma_{out}}{1-\Gamma_{out}} \quad (15)$$

Where a $Z_{in} = 28.508 - j57.955$ and a $Z_{out} = 49.878 + j9.697$ are found. The matching network for both input and output is summarized in Table IV. The whole matching network is presented in Fig. 24, and the corresponding Smith chart is in Fig. 25, where the markers are the same as Fig. 19. $m1$ and $m3$ that is Γ_S and Γ_L are still outside the source and load stability circle (pink and green circle), so the circuit operates in stable region.

Table III: S parameters at 5.79GHz for matched network

S-Parameter	Mag/Deg
S_{11}	0.941/44.832
S_{12}	0.205/21.503
S_{21}	3.105/106.125
S_{22}	0.369/53.645

Table IV: Desired specifications at 5.79GHz

Component	Input matching	Output matching
Series L	12.27nH	-
Shunt L	1.25nH	-
Series C	-	4.81pF
Shunt L	-	157.73nH

III. Part III

The design goal here is to implement a inductor source-degenerated LNA biased by a current mirror. The prototype circuit schematic is given in the assignment handout and is

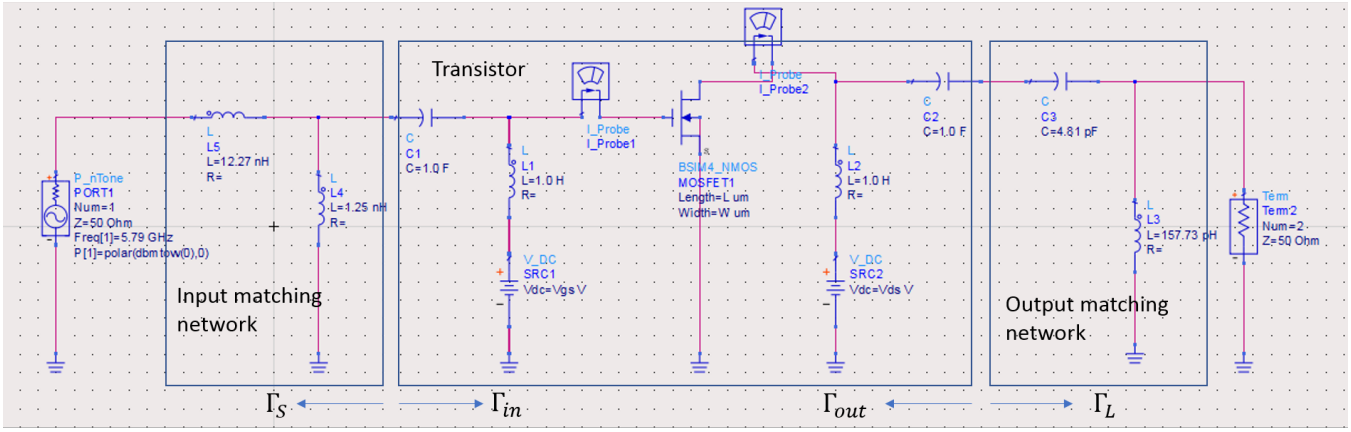

Figure 24: The whole matching network, where the corresponding input matching network, transistor block, and output matching network are highlighted in this picture for comparison to Fig. 19

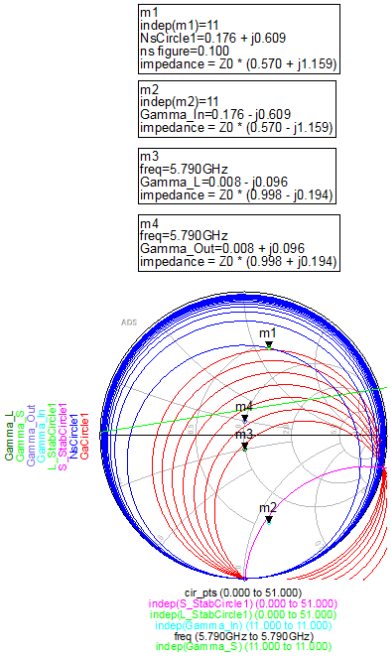

Figure 25: Smith chart for the matched network in Fig. 24

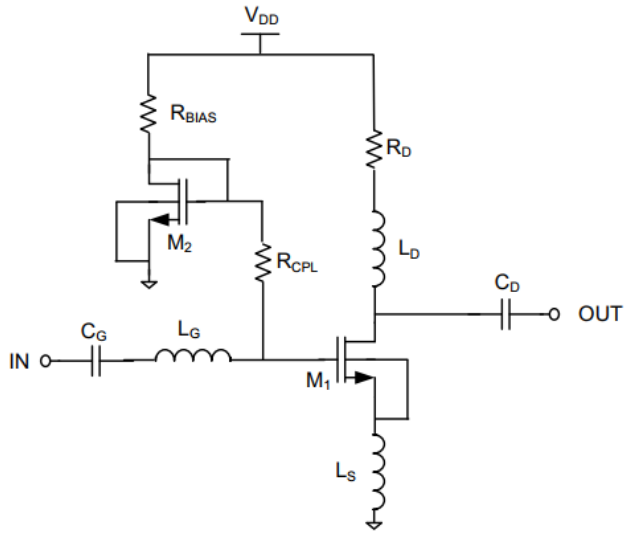

Figure 26: Inductor source-degenerated MOSFET LNA

given in Fig. 24. The targeted specifications of the design in outlined in Table V.

We will start by designing the biasing circuit first, then will illustrate the approach to design the actual LNA circuit part.

A. Biasing Network

If one refers to Fig. 26, the biasing method here is done by using a simple current mirror that consists of a CS MOSFET M_1, R_{bias}, and a noise isolation resistor R_{cpl}. Under this situation, the question that how much the biasing drain current pumped to M_1 and how much the biasing voltage given to the gate of M_1 should be provided by M_2 in order to meet the specifications plays the steering role in the design of the biasing network. Apparently, simply using the transistor designed in $part1$ and $part2$ will not satisfy the power requirement since the drain current of the old transistor is about $23mA$, which will result in an about $41.4mW$, which is way larger than $6mW$. In order to meet this power consumption requirement, an about $3.3mA$ drain current should be appeared at the drain of M_1. Also, the drain current of M_1 is directly proportional to W/L and also V_{ov}^2 by the following famous

Table V: Desired specifications at 5.79GHz

Specifications	Value
Central frequency	5.79 GHz
Bandwidth	$300MHz < BW < 900MHz$
Gain(S_{21})	$> 6dB$ over the designed bandwidth
Return Loss(S_{11})	$< -15dB$ over the designed bandwidth
Noise figure	$< 1dB$
IIP3	$5dBm$
1dB compression point	$> -5dBm$
Power consumption	$< 6mW$
Supply voltage	1.8V
I/O impedance	$50/Omega$
Stability	Stable over the interested bandwidth

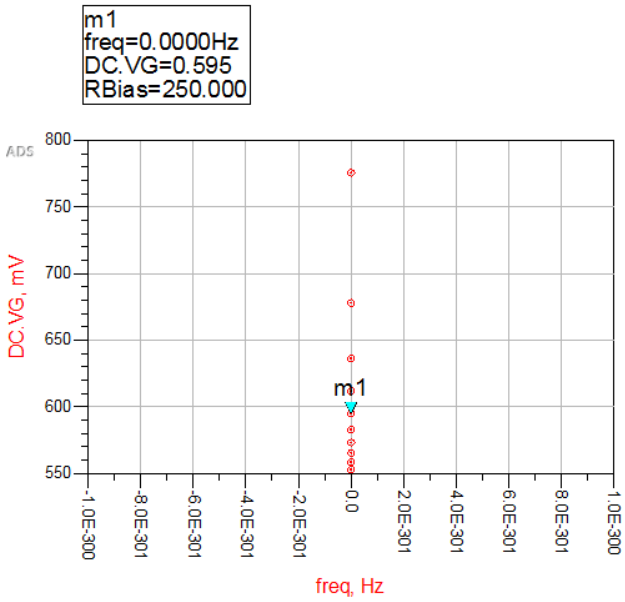

Figure 27: Sweeping R_{bias} to find the $V_G = 0.6V$

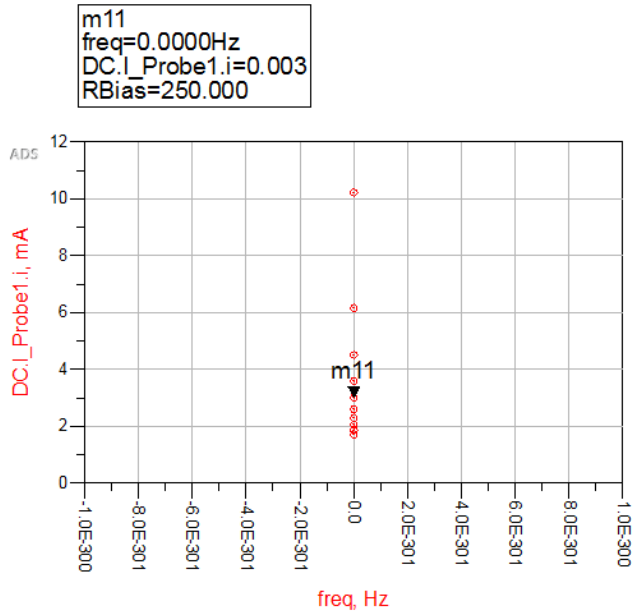

Figure 28: Sweeping R_{bias} to find the $I_{D,M_1} = 3mA$

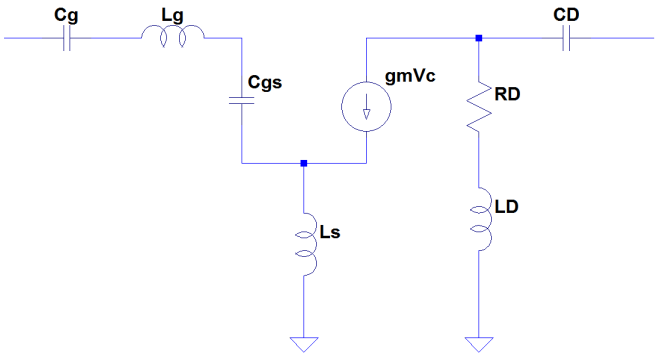

Figure 29: Small signal model of the LNA

correlation in saturation region, which is forced by the diode connection in M_2:

$$I_{D,M_1} = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}V_{ov}^2 \tag{16}$$

So scaling down V_G and W of M_1 will drop down the drain current. By doing the sweeping of these two parameters, to meet a $3.3mA$ drain current from M_1, a width of $80\mu m$ and a $V_G = 0.6V$ are found, which will trade off the noise figure based on the sweeping result from $part1$.

The same transistor as $part1$ and $part2$ will be used for the biasing network transistor M_2. The biasing resistor R_{bias} is swept to find the appropriate V_G and I_{D,M_1}. The sweeping result is given in Fig. 27 and Fig. 28. Based on these sweeping results, $R_{bias} = 250\Omega$ is selected. For the noise isolation resistor R_{CPL}, it has been selected as the highest resistance allowed in the design, which is equal to $25k\Omega$.

B. LNA Design

To approach this design like $part2$ is not very straightforward as here the matched network is also functioning as the load of the amplifier. In this senario, it will be beneficial to understand how the inductor and capacitor affect the input and output impedance of the LNA. For the inductor source-degenerated LNA given in Fig. 26, its small signal model is given in Fig. 29, where the feedback capacitance is neglected here, which will cause some error in the calculation, but for the first-order analysis this is acceptable.

It should be easy to first calculate the output impedance Z_{out} that consists of C_D, R_D, and L_D.

$$Z_{out} = R_D + j\omega(L_D - \frac{1}{\omega^2 C_D}) \tag{17}$$

And the input impedance Z_{in} needs some algebric manipulation, which will lead to:

$$Z_{in} = \frac{g_m L_S}{C_{gs}} + j\omega[(L_g + L_s) - \frac{1}{\omega^2}(\frac{1}{Cg} + \frac{1}{C_{gs}})] \quad (18)$$

Let us take a closer look to the above two equations. For Z_{out}, the real part is governed by the drain resistor R_D, and the imaginary part is self-cancelled by L_D and C_D if appropriate inductance and capacitance are selected. The center frequency here is 5.79GHz. To match with 50Ω load impedance, R_D is selected also as 50Ω. For a good cancellation of the imaginary part of the output impedance but meanwhile the value of the inductance and capacitance are appropriate numbers, after some parameter tinning in ADS (compensate some overlook parasitic capacitance and resistance), $L_D = 5nH$ and $C_D = 6pF$ are picked.

The selections of L_s, L_g, and C_g are tricky. Looking at the equation for Z_{in}, the real part is $\frac{g_m L_S}{C_{gs}}$, which is dependent to three parameters, and the real part should be equal to also 50Ω to match a 50Ω input resistance. Therefore, one needs to find g_m and C_{gs}.

Recall what we did in $part1$, using output-shorted circuit is capable for finding both unity-gain frequency f_T and g_m; but be reminded that the transistor M_1 has a different dimension and biasing condition compared with the old transistor, so the same test is conducted again, and a $f_T = 12.57GHz$ and $g_m = 0.037A/V$ are found.

The following method is used to find C_{gs}. A very short period current step function is applied to the gate of the interested transistor M_1 with the desired drain voltage biasing (1.8V), and the gate voltage is plotted with the time. The transient response of the gate voltage can be used to calculate C_{gs} by using the slope of the gate voltage transient response over the magnitude of the current step response. Fig. 30 illustrate this idea. Using $m1$ and $m2$ in Fig. 31 that is the transient voltage response of a $1nA$ current step input with $1nA$, the slope can be calculated as $4715V/sec$. Thus, the parasitic gate-source capacitance C_{gs} is approximated as:

$$C_{gs} = \frac{1nA}{4715V/sec} \approx 0.21pF \quad (19)$$

After collecting all the parameters that is required, from the equation:

$$Z_{in,real} = \frac{g_m L_S}{C_{gs}} = 50\Omega \longrightarrow L_S \approx 0.3nH \quad (20)$$

Which is not the actual available value as required from the assignment handout, the smallest inductance available is $0.5nH$. The value for C_g has been selected as $2pF$ initially since in order for C_{gs} to be the dominant capacitor in Eq. 18, it should be at least 10 times larger, which lead to the value of L_g to be about $2nH$. After some more tuning for C_g, L_g, and L_s, their values are finally determined as $2.5pF$, $2nH$, and $0.6nH$, respectively. The whole circuit schematic is given in Fig. 32.

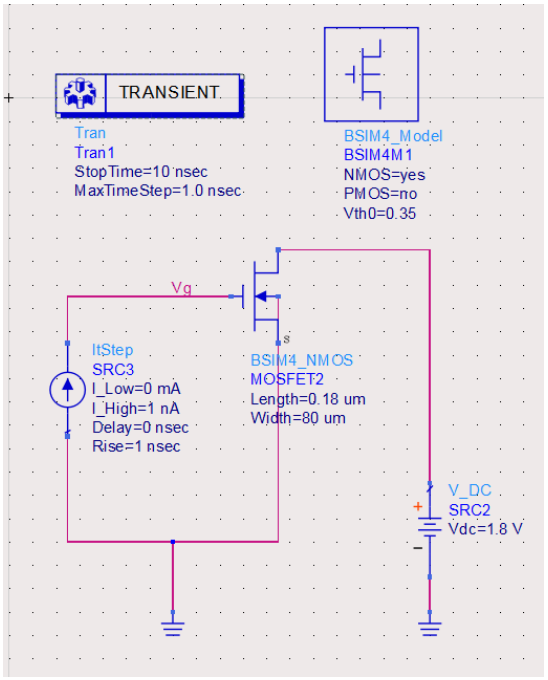

Figure 30: Transient simulation setup for finding C_{gs}

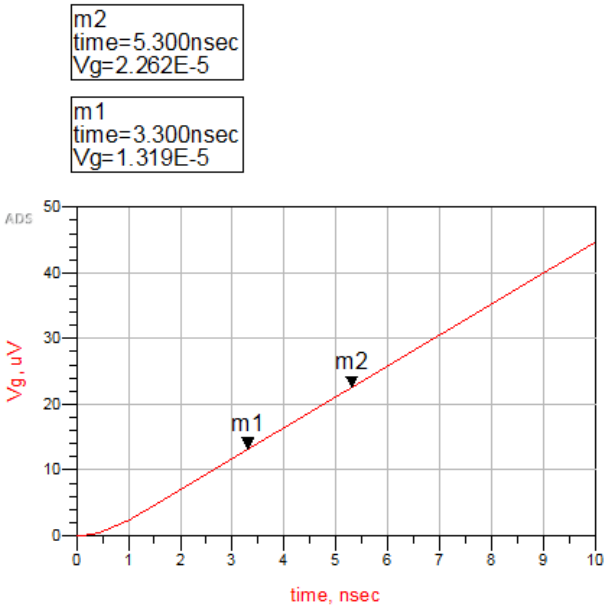

Figure 31: Transient gate voltage response of transistor M_1

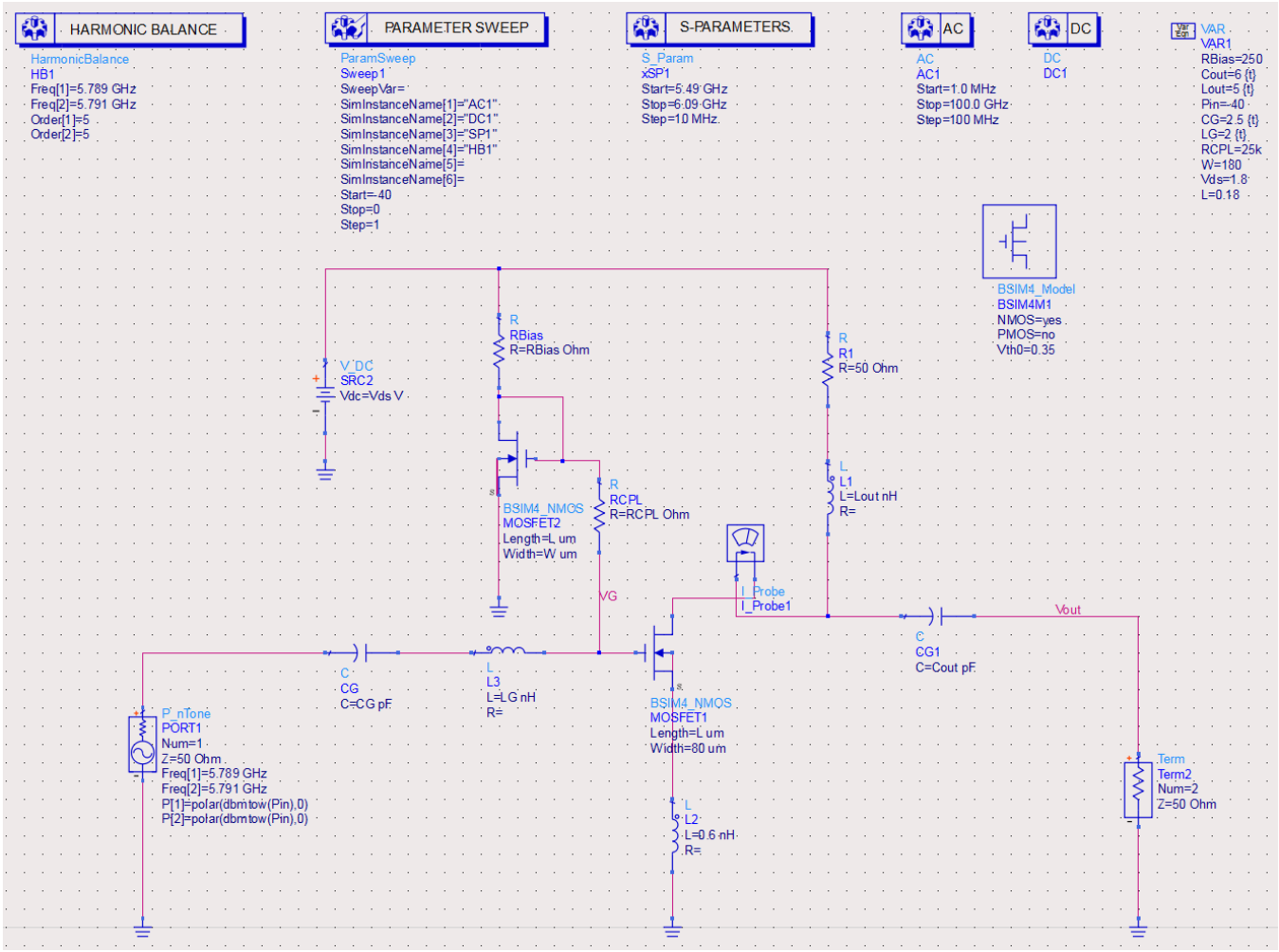

Figure 32: The inductor source-degenerated LNA

C. Performance Testing

1) S11 Measurement: The interested bandwidth is selected as 600MHz, which satisfies the specification requirement, which means from 5.49-6.09GHz S_{11} should be smaller than -15dB with the fact that the center frequency is 5.79GHz. The S-parameter simulation is conducted and the result is plotted in Fig. 33, where two markers indicate the S_{11} value at 5.49GHz and 6.09GHz, respectively. Apparently, the S_{11} over the interested bandwidth is smaller than -15dB, which implies that this specification is met.

2) S21 Measurement: Another important specification requirement is within the operating frequency bandwidth the forwarding gain should be larger than 6dB. Similar as the S_{11} simulation, the same simulation setup is applied to S_{21} measurement and the result is shown in Fig. 34, which suggests that the design also meets the S_{21} requirement.

3) Noise Figure Measurement: Noise figure measurement can also be done using S-parameter simulation if the interested operating mode is a frequency band rather than single tone. The NF result is given in Fig. 35 and over this bandwidth, the noise figure is smaller than 1dB, which means this specification is also met.

4) IIP3 Test: The third-harmonic intercept point power is also measured by using a two-tone test. IIP3 is calculated by using the formula given in assignment 1 handout, which is neglected here for simplicity. Two signals that locate at 5.789 and 5.791GHz who are separated by 1MHz with each other that each one signal has -40dBm RF power are injected from the input port. The harmonic balancing test is used in this simulation, and the power spectral detected at the output (V_{out} in Fig. 32) are plotted in Fig. 36, and IIP3 is calculated as 3dBm, which does not meet the required specification, but very close.

5) 1dB Compression Point: A single tone test with a variable RF power input whose center frequency is 5.79GHz is given at the input, and the output power that is plotted with the sweeping of the input power (it is swept from -10 to 10dBm) is given in Fig. 37, which suggests the 1-dB compression point

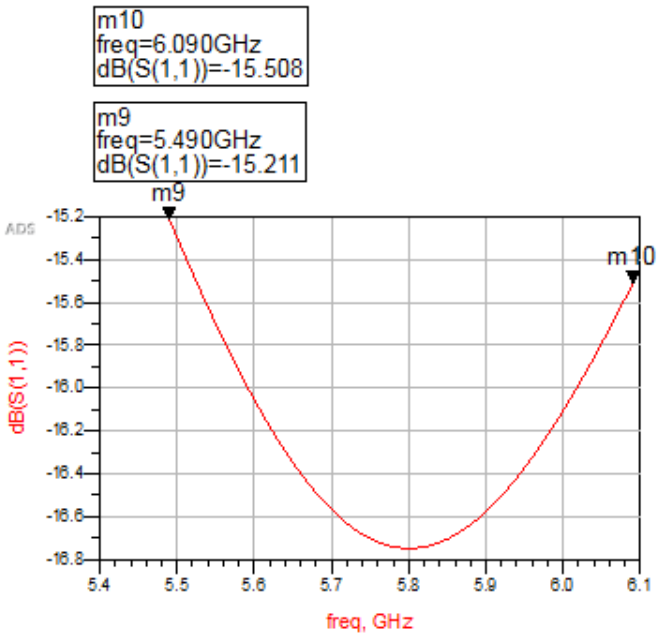

Figure 33: S_{11} response of the designed LNA over the interested operating bandwidth

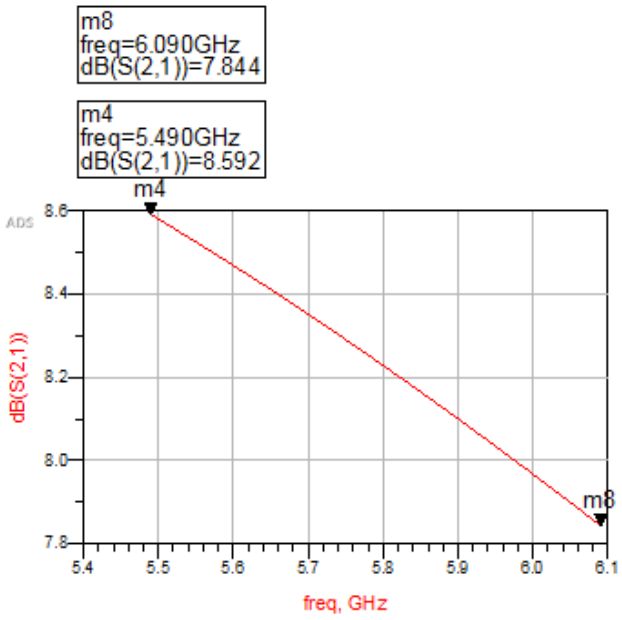

Figure 34: S_{21} response of the designed LNA over the interested operating bandwidth

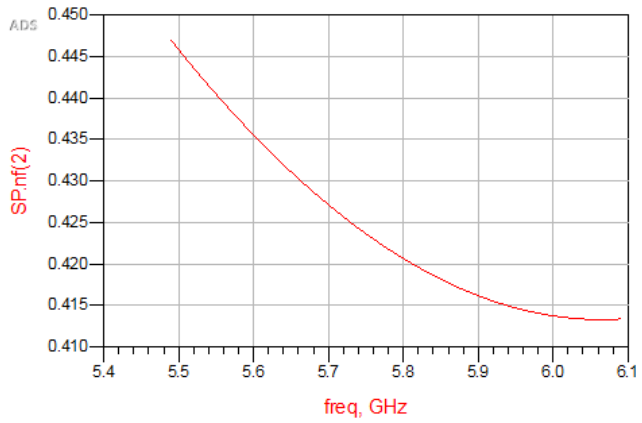

Figure 35: Noise figure result of the designed LNA over the interested operating bandwidth

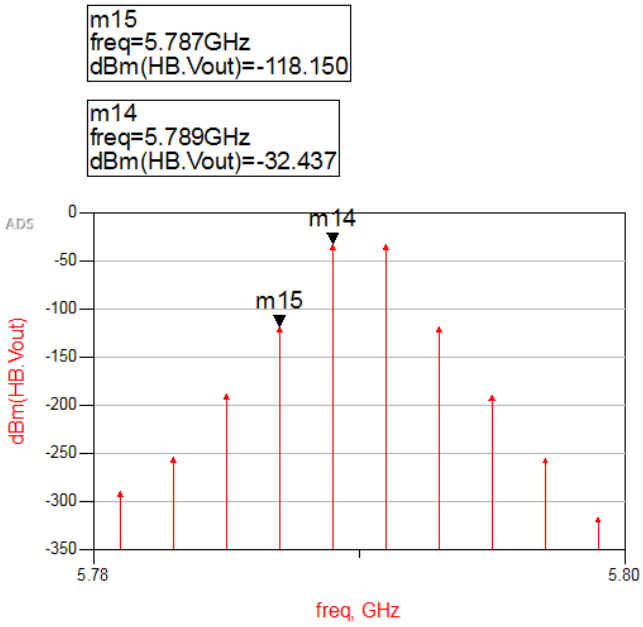

Figure 36: IIP3 result given by the two-tone test

is at about 4dBm that is larger than -5dBm. Therefore, this specification is also satisfied.

6) Stability: It is very important to verify that within the interested frequency bandwidth the LNA operates stably. In order to verify its stability, Rollet's stability principle is employed here, which suggests that if:

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12}S_{21}|} 1 \qquad (21)$$
$$|\Delta| = |S_{11}S_{22} - S_{12}S_{21}| < 1$$

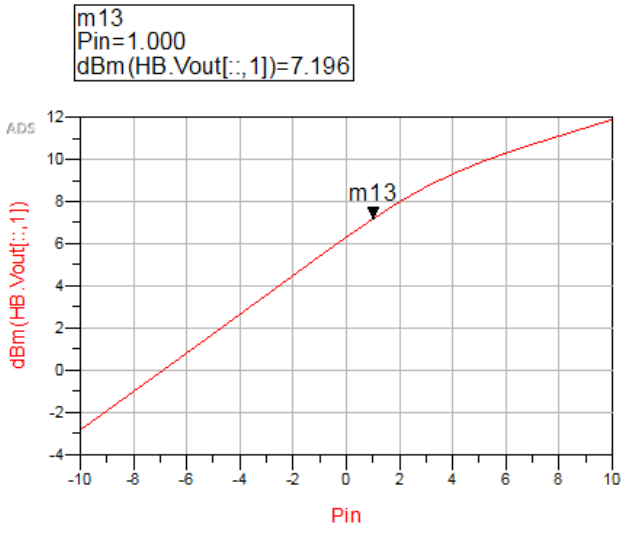

Figure 37: 1-dB compression point plot

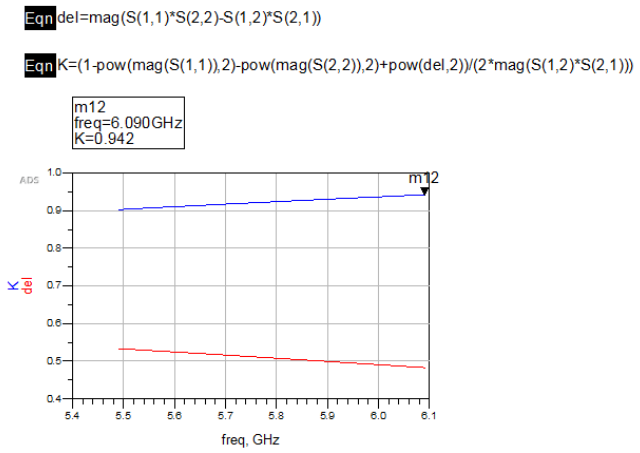

Figure 38: Rollet's stability criteria plot over the operating frequency bandwidth; the blue curve is K, and the red curve is Δ

are satisfied, then the device is unconditionally stable [2]. Therefore, K and Δ are both plotted over the interested frequency bandwidth in ADS and it is given in Fig. 38. Thankfully, Rollet's stability criteria is met, which means the designed LNA will be unconditionally stable.

7) Power Consumption: The power consumption specification is firstly used to decide the biasing network as well as the drain current of M_1; referring back to FIg. 28, the static power consumption (no AC signal is loaded) is calculated as $(1.8V)(0.003A) = 5.4mW$, which is smaller than 6mW, meeting the desired specification.

D. Summary of the Design

The specifications of the design compared with the desired specifications are summarized in Table VI, where one can see that except for the IIP3 parameter, all others are met nicely. Still, IIP3 is achieved as about 3dBm, which is very close to the desired value.

Table VI: Actual designed LNA's specifications vs. desired specifications

Specifications	Desired specs.	Design results	Meet specs.?
Central frequency	5.79GHz	5.79GHz	Yes
Bandwidth	[300MHz, 900Mhz]	600MHz	Yes
Gain(S_{21})	$> 6dB$	$> 7.8dB$	Yes
Return Loss(S_{11})	$< -15dB$	$< -15.2dB$	Yes
Noise figure	$< 1dB$	$< 0.45dB$	Yes
IIP3	$5dBm$	$3dBm$	No
1dB compression point	$> -5dBm$	4dBm	Yes
Power consumption	$< 6mW$	5.4mW	Yes
Supply voltage	1.8V	1.8V	Yes
I/O impedance	50Ω	50Ω	Yes
Stability	Stable	Stable	Yes

IV. Part IV

Question: In our LNA design we used an inductor to generate the real part of the input impedance. Why was this used instead of a resistor?

Answer: By swapping the source degenerated inductor L_s in Fig. 29 with a resistor R_s, the input impedance can be derived as:

$$Z_{in} = R_s + j\omega[L_g - \frac{1}{\omega^2}(\frac{g_m R_s}{C_{gs}} + \frac{1}{C_{gs}} + \frac{1}{C_g})] \qquad (22)$$

From matching point of view, it is totally fine to use resistor for matching, which will be $R_s = 50\Omega$ in this case. So here using inductor rather than using resistor is for reducing the noise generated by the resistor; also usually resistor has larger variations.

Question: In our design we used inductors with an infinite Q. (i.e., no internal series resistance). What would change if the inductors available had a maximum Q of 10?

Answer: Essentially limited quality factor of inductor means adding ESR (effective series resistance), so the impedance of an inductor has a real part. Therefore, inductor will also add the real part to the input matching network, adding thermal noise, adding more energy loss, and therefore dropping down the gain and shifting the resonances by creating mismatching.

Question: In the inductively degenerated common-source LNA used here, you may have noticed that the input matching network affects the output matching network and vice versa. Give a common method of reducing this feed-through effect, and briefly state how it works.

Answer: Parasitic feedback capacitance C_{ds} is the major contribution of the feed-through effect. A common gate MOSFET may be used as a current buffer at the output of a common source stage, forming a cascode. This will typically reduce the Miller effect and increase the bandwidth of the amplifier

and mitigate the parasitic effect. Alternatively, a voltage buffer may be used before the amplifier input, reducing the effective source impedance seen by the input terminals. This lowers the RC time constant of the circuit and typically increases the bandwidth and decrease the parasitic effect as well.

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[2] David Pozar, *Microwave Engineering, Fourth Edition*, John Wiley & Sons, Inc., 2012.

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