ECSE 536 RF Microelectronics – Assignment 1

Zonghao Li 260787179
M.Eng. Student, McGill University
zonghao.li@mail.mcgill.ca

***Abstract*—This is the report for the first assignment**

***Keywords*—Assignment**

I. Part I

A. Question 1

Question: Why is the 3^{rd} harmonic stronger than the 2^{nd} harmonic? Is tehre any way to find IIP3 and IIP2 of the amplifier by doing only single tone analysis? Explain.

Answer: Please also refer to *Fig. 1* for the explanations. As studied in [2], the third inter-modulation intercept point (IIP3) can be calculated by *Eq. 1*

$$IIP3|_{dBm} = P_{in}|_{dBm} + \frac{1}{2}\delta y_3|_{dB} \tag{1}$$

With the similar approach, one is able to calculate the second inter-modulation intercept point (IIP2) by *Eq. 2*:

$$IIP2|_{dBm} = P_{in}|_{dBm} + \delta y_2|_{dB} \tag{2}$$

Where P_{in} is the input power of the signal. The above two equations can be modified in the functions of δy:

$$\begin{aligned}\delta y_3|_{dB} &= -20dBm - 2P_{in}|_{dBm} = 60dBm \\ &\approx (-25dBm + 94dBm) = 69dBm\end{aligned} \tag{3}$$

$$\begin{aligned}\delta y_2|_{dB} &= 50dBm - P_{in}|_{dBm} = 90dBm \\ &\approx (-25dBm + 121dBm) = 96dBm\end{aligned} \tag{4}$$

Where the value of IIP2 and IIP3 are given in [1], which are 50dBm and -10dBm. Therefore, it should be obvious to see that:

$$\delta y_2 > \delta y_3 \tag{5}$$

This can be visualized in *Fig. 1*. It explains why is the 3^{rd} harmonic stronger than the 2^{nd} harmonic.

It is also viable to use single tone test to calculate IIP2 and IIP3 of a amplifier. First, assume the input test signal is a cosine function:

$$x(t) = Acos(\omega t) \tag{6}$$

Where A is the amplitude of the input signal and ω is its fundamental frequency. Through trigonometric expansion, its output signal can be formulated as [2]:

$$\begin{aligned}y(t) = \frac{\alpha_2 A^2}{2} + (\alpha_1 A)cos(\omega t) + \\ (\frac{\alpha_2 A^2}{2})cos(2\omega t) + (\frac{\alpha_3 A^3}{4})cos(3\omega t) + ...\end{aligned} \tag{7}$$

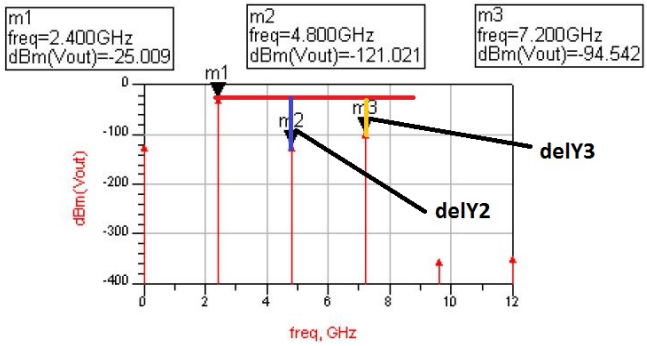

Figure 1: PSD of LNA (m1: fundamental frequency harmonic; m2: second-order harmonic; m3: third-order harmonic; "delY2" corresponds to δy_2; "delY3" corresponds to δy_3) [1]

Where in *Eq. 7* the first term is the DC component, the first, second, and third term are the first, second, and third harmonic, respectively, without the concern of gain compression; α_1, α_2, and α_3 are the gain of the first, second, and third harmonic, respectively. By equating the coefficient of the fundamental frequency component to the second and third component in *Eq. 7*, the following equations will be derived:

$$\alpha_1 A = \frac{\alpha_2 A^2}{2} \rightarrow A_{IIP2,one-tone} = 2|\frac{\alpha_1}{\alpha_2}| \tag{8}$$

$$\alpha_1 A = \frac{\alpha_3 A^3}{4} \rightarrow A_{IIP3,one-tone} = 2\sqrt{\frac{\alpha_1}{\alpha_3}} \tag{9}$$

Similarly, by equalizing the coefficients of first harmonic to the second and the third harmonic in the intermodulation equation for two-tone test in *Eq. 2.40* given in *section 2.2* in Razavi's book [3], one should be able to calculate the amplitude of IIP2 and IIP3 by:

$$\alpha_1 A = \alpha_2 A^2 \rightarrow A_{IIP2,two-tone} = |\frac{\alpha_1}{\alpha_2}| \tag{10}$$

$$\alpha_1 A = \frac{3}{4}\alpha_3 A^3 \rightarrow A_{IIP3,two-tone} = \sqrt{\frac{4}{3}|\frac{\alpha_1}{\alpha_3}|} \tag{11}$$

In this manner, one can relate the actual IIP2 and IIP3 of two-tine testing to one-tone testing. For $IIP2_{one-tone}$ and $IIP3_{one-tone}$, *Eq. 1* and *Eq. 2* are still valid. Then the

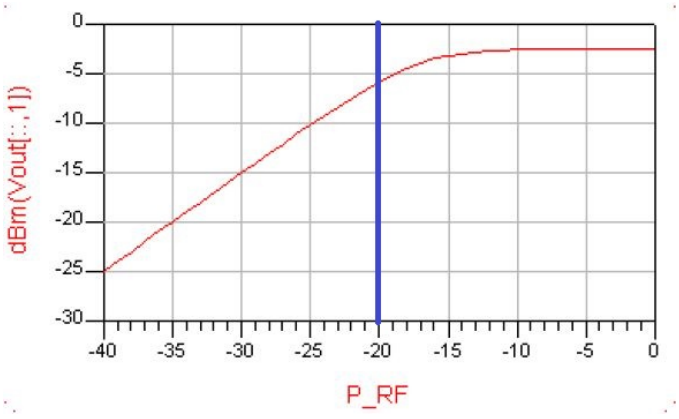

Figure 2: Amplifier gain vs. RF input power [1]

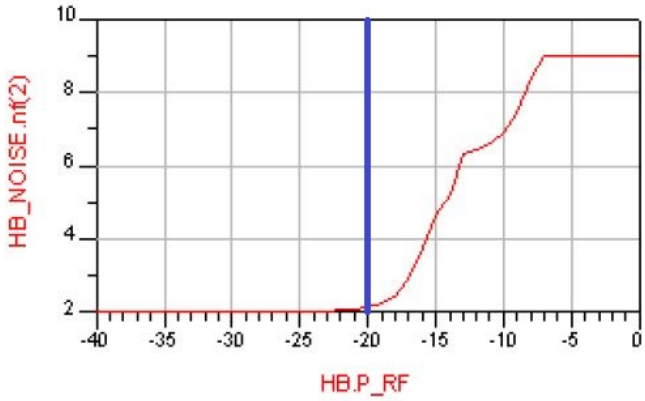

Figure 3: PSD of LNA (Noise figure vs. input power [1]

following relationship between one-tone and two-tone test is established:

$$IIP2_{two-tone}|_{dBm} = IIP2_{one-tone}|_{dBm} - 3dB \quad (12)$$

$$IIP3_{two-tone}|_{dBm} = IIP3_{one-tone}|_{dBm} - 2.38dB \quad (13)$$

Where: $10log_{10}(2) = 3dB$; and $10log_{10}(\frac{2}{\sqrt{\frac{4}{3}}}) = 2.38dB$. In this manner, one can use one-tone test to find IIP2 and IIP3 for two-tone test.

B. Question 2

Question: Why is the noise figure (NF) changing with the RF input power?

Answer: the initial NF is defined as 2dB [1]. The NF of the amplifier does not change until it reaches around -1dB point, where the linearity starts to distort. This phenomena can be illustrated in *Fig. 2* and *Fig. 3*. Ideally, if there is no gain compression, the NF of the amplifier should be constant as in the simulation things are ideal. When the input power reaches around -20dB (blue line) in both *Fig. 2* and *Fig. 3*, the gain compression occurs and it gradually decreases. Therefore NF starts to increase. When the input RF power is around 10dBm, the third harmonic IIP3 is dominant the signal power and thereby further distort the linearity. When the gain of the amplifier also reaches zero, which means now it is a zero order system, the NF is then back to a constant as again the NF function is now independent of the amplifier's gain.

C. Question 3

Question: Explain why the value of S21 is -31dB at 2.4GHz. Also, explain why the value of S21 is -221dB at 100 MHz when our Harmonic Balance simulation tells us that the gain is 19dB. Make a general comment on the usefulness of S-Parameter simulations.

Answer: The gain from port 1 to port 2 (S21) has a gain value of -31dB at 2.4GHz that can be characterized by the following equation:

$$\begin{aligned} S21|_{dB} = Gain_{LNA}|_{dB} + \\ IL_{Filter}|_{dB} + \\ S21_{Mixer}|_{dB} \\ = 15dB - 6dB - 40dB = -31dB \end{aligned} \quad (14)$$

However, for the mixer there is another gain called "conversion gain" (ConvGain) that S21 does not capture, which will give the gain as:

$$\begin{aligned} S21|_{dB} = Gain_{LNA}|_{dB} + \\ IL_{Filter}|_{dB} + \\ ConvGain_{Mixer}|_{dB} \\ = 15dB - 6dB + 10dB = 19dB \end{aligned} \quad (15)$$

Therefore, for a three-port network, for example, mixers are involved, S21 is not an accurate reflection of the gain of a system; whereas for regular two-port networks, S21 is still valid.

II. Part II

A dual IF-filter receiver design question is given in this part. The desired specifications and the topology of the receiver is given in *Table I* and *Fig. 4*, respectively. The available amplifiers, mixers, and filters are provided in *Table II*, *Table III*, and *Table IV*, correspondingly, which are all provided in [1]. Here, the author selects the following order for the receiver design: *Amplifier5* $\rightarrow$ *Mixer1* $\rightarrow$ *Amplifier3* $\rightarrow$ *Mixer2* $\rightarrow$ *Amplifier2*. The reasons are explained as the followings. First, it is obvious that *Amplifier5* is the LNA since its NF is the smallest among these options. The cascaded NF is dominated by the first stage at the RF front-end, which is formulated by the Friis' Formula for noise factor (linear scale):

$$F_{total} = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + ... \quad (16)$$

Where G_n is the available power gain at stage n. Then the order of the mixers should be *Mixer1* $\rightarrow$ *Mixer2* from the standing point of IIP3. The cascaded IIP3 is calculated by the following formula:

$$\frac{1}{IIP3_{total}} = \frac{1}{IIP3_1} + \frac{G_1}{IIP3_2} + \frac{G_1G_2}{IIP3_3} + ... \tag{17}$$

Therefore, the last term will dominant the performance of IIP3, and the larger the left-hand-side of *Eq. 17*, the smaller $IIP3_{total}$ will be, thereby the worse distortion. In order to have large $IIP3_{total}$ in total, stages with large IIP3 should be put at the later.

The selection of the rest two amplifiers are very dependent on the trade off among NF, IIP3, and gain. The amplifier sequence that author chooses is for the sake of meeting amplification specification but also maintain the balance between NF and IIP3. Also, it should be noted that in order to avoid the gain compression occurrence, before the stage of the second mixer (*Mixer2*), if the second amplifier is chose as the ones that have the gain S21 larger than 30dB, gain compression is happening on the second mixer and the the whole design is essentially wasting the gain provided by the second amplifier, which is found based on the author's simulation trials and errors. To avoid this situation but meanwhile provide enough gain, *Amplifier3* is chosen as the second IF amplifier that has 30dB gain, and the third amplifier is chosen as *Amplifier2* since it has larger IIP3 than *Amplifier1* although its gain is 10dB smaller, which trades for better IIP3 performance as IIP3 for the last stage is very critical and if *Amplifier1* is chosen, its low IIP3 will degrade the IIP3 of the whole design, which is very unwanted. The *ADS* schematic for this design is provided in *Fig. 5*. The rough calculations for this design is calculated by (in dB):

$$\begin{aligned} Gain_{total} = Gain_{Amp5} + IL_{Filter} + \\ ConvGain_{Mixer1} + IL_{Filter} + \\ Gain_{Amp3} + ConvGain_{Mixer2} \\ + IL_{Filter} + Gain_{Amp1} \\ = 15 - 6 + 10 - 6 + 30 - 10 - 6 + 40 = 67dB \end{aligned} \tag{18}$$

The above calculation should be valid if it is ideal and no gain compression situation happens. In this simulation, a testing signal whose RF poser is -40dBm located at f_{fund} = 2.4GHz is analyzed. The following subsections will be about the image rejection, IIP3, 1-dB compression point, receiver gain, and noise figure measurement, respectively.

Since the desired output signal bandwidth is 2MHz and the maximum quality factor of filters is 10, therefore the center frequency for the second IF-filter is 20MHz.

A. Image Rejection Test

It is recommended that for dual-IF filter receiver, the first LO-frequency (f_{LO1}) is high so that the image tone can be filtered out nicely by the image rejection filter. Therefore, *Mixer2* is selected to have f_{LO1} equals to 5GHz, thus the image signal will be located:

$$f_{image} = f_{LO1} + (f_{LO1} - f_{fund}) = 7.6GHz \tag{19}$$

Which will be the testing image signal at the input in addition to the received signal at 2.4GHz. The two tone test is thereby conducted and the PSD plot of f_{LO1} component (marker *m3*) versus f_{image} component (marker *m4*) is presented in *Fig. 6*. The image rejection ratio (IR) is calculated as:

$$IR = -30.936 - (-145.722) = 114.786dB \tag{20}$$

Which is above the specifications (65dB).

B. IIP3 Test

A two-tone signal whose fundamental frequencies are 2.399GHz and 2.401GHz and the power is -40dBm is imported to the design, and the IIP3 plot is demonstrated in *Fig. 7*. Since the signal is down-converted to 20MHz via the second mixer $Mixer2$ whose f_{LO2} is 2.62GHz so that a 2MHz bandwidth is achieved at the output, the IIP3 test conducted here will focus on the tones at 21MHz (marker *m5*) and 23MHz (marker *m6*), which corresponds to one of the two-tone testing signals that is at 2.399GHz, and its IM3 tone. The IIP3 is calculated by:

$$\begin{aligned} IIP3 = \frac{P_{test,out} - P_{IM3}}{2} + P_{test,in} = \\ \frac{24.924 + 47.474}{2} - 40 = -3.801dBm \end{aligned} \tag{21}$$

Which meets the required specification of IIP3.

C. -1dB Compression Point Test

The single tone test is used in this measurement that f_{fund}=2.4GHz again. The input power P_{in} of the testing signal is swept from -40dBm to 30dBm, and the output-power versus input power of the design is plotted in *Fig. 8*, where the blue line is the extrapolated linear line if the gain compression is not occurred. The -1dB compression point can be eyeballed around -24dBm, which is smaller than the -30dBm, also meets the specification.

D. Received Gain Test

The same single tone testing signal is used and the output signal plotted at the down-converted frequency 20MHz is shown in *Fig. 8*. The output signal (marker *m7*) The actual gain of the receiver is about 66.957dB, which is close to the calculation given in *Eq. 18* that is the ideal case.

E. Noise Figure Test

The noise figure plot is shown in *Fig. 9*, measured at 20MHz where the received signal is located. It is detected as about 10dB, which meets the specification

Table I: Desired specifications

Image Rejection	$\geq$ 70dB
IIP3	$\geq$ -20dBm
1-dB Compression Point	$\geq$ -30dBm
Receiver Gain	$\geq$ 65dB
Noise Figure	$\geq$ 11dB
Signal Bandwidth at End of Receiver	2MHz

Table II: Available amplifiers

Parameters	S11 (dB)	S21 (dB)	S12 (dB)	S22 (dB)	NF (dB)	IIP3 (dBm)	IIP2 (dBm)
Amp1	-15	50	-40	-15	10	5	70
Amp2	-15	40	-40	-15	10	20	70
Amp3	-15	30	-40	-15	12	30	70
Amp4	-15	20	-40	-15	14	40	70
Amp5	-15	15	-40	-15	2	-10	50

Table III: Available mixers

Parameters	Conversion Gain (dB)	Port-to-Port Isolation (dB)	NF (dB)	IIP3 (dBm)	IIP2 (dBm)
Mixer1	10	40	12	5	60
Mixer2	-10	40	13	25	60

Table IV: Available filters

Type = 4^{th} Order Butterworth
Maximum Quality Factor = 10
Insertion Loss = 6dB

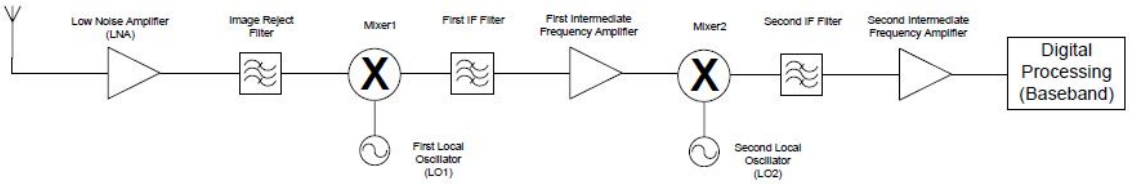

Figure 4: Schematic of a dual-IF filter receiver [1]

Table V: Summary of specifications

Parameters	Desired	Actual	Meet the spec?
Image Rejection	$\geq$ 70dB	114.786dB	Yes
IIP3	$\geq$ -20dBm	-3.8dBm	Yes
1-dB Compression Point	$\geq$ -30dBm	about -24dBm	Yes
Receiver Gain	$\geq$ 65dB	67dB	Yes
Noise Figure	$\geq$ 11dB	10dB	Yes
Signal Bandwidth at End of Receiver	2MHz	2MHz	Yes
f_{LO1}	-	5GHz	-
f_{LO2}	-	2.62GHz	-

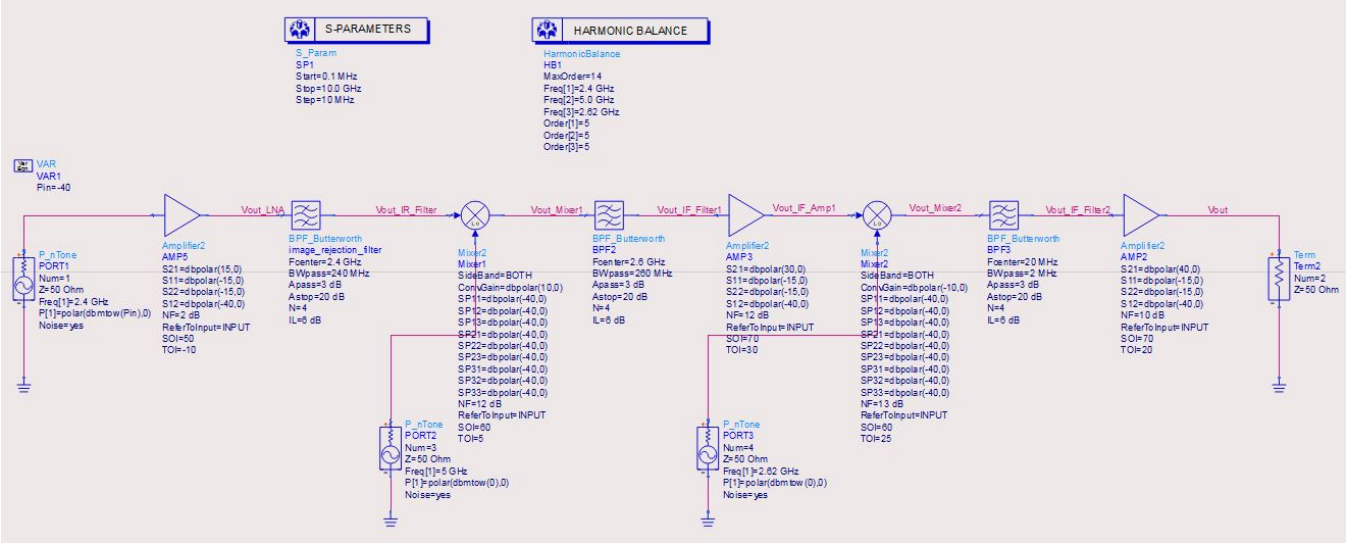

Figure 5: ADS schematic of the dual-if filter receiver design (*Amplifier5* → *Mixer1* → *Amplifier3* → *Mixer2* → *Amplifier2*)

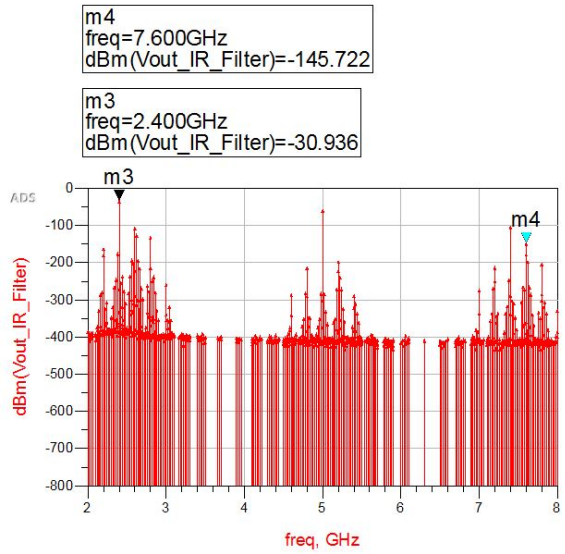

Figure 6: Image signal vs received signal plot

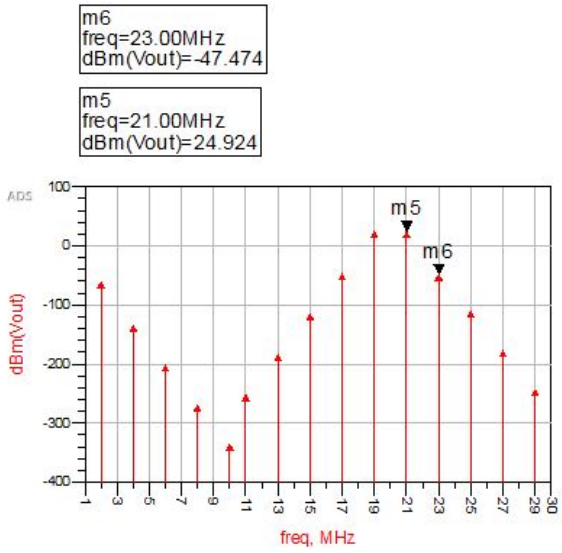

Figure 7: IIP3 vs received signal plot

F. Summary of Part II

The overall design specifications compared with the desired ones are listed in *Table V*. As one can see, the designed dual-IF filter receiver meet all the specifications.

III. Part III

In this part a Hartley receiver is designed, whose ADS schematic is in *Fig. 11*. Two mixers are both *Mixer1* from *Table III*, and two amplifiers from left to right are *Amplifier5* and *Amplifier1*, respectively, to provide enough gain. Idealy, the gain of the system will be calculated as (power spliter/combiner and phase shifter are ideal):

$$\begin{aligned} Gain_{total} &= Gain_{Amp5} + ConvGain_{Mixer1} + \\ &\quad IL_{Filter} + Gain_{Amp1} \\ &= 15 + 10 - 6 + 50 = 69dB \end{aligned} \tag{22}$$

So approximately a 69dB gain should be expected from this Hartley receiver. The reason of choosing this sequence is the same as the one explained in *Section II*. Here, special attentions are given to the local oscillators' frequency. It should be noted

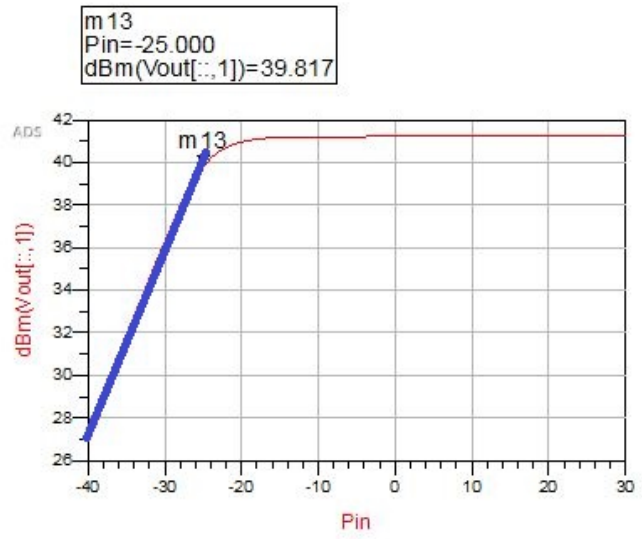

Figure 8: -1dB compression point plot (output power vs. input power)

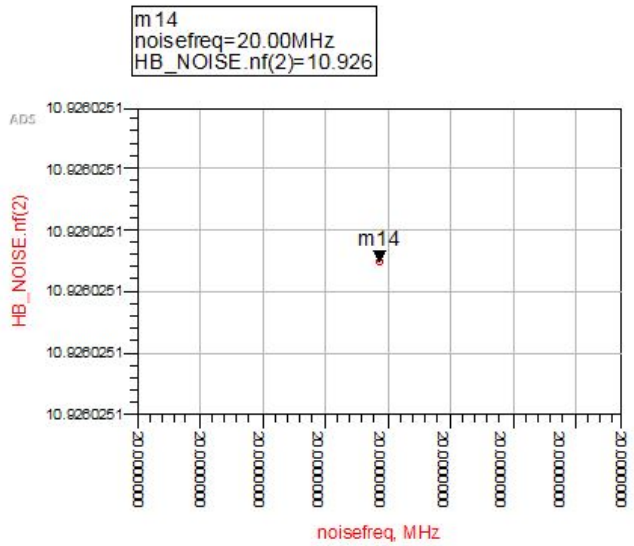

Figure 10: Noise figure of the receiver

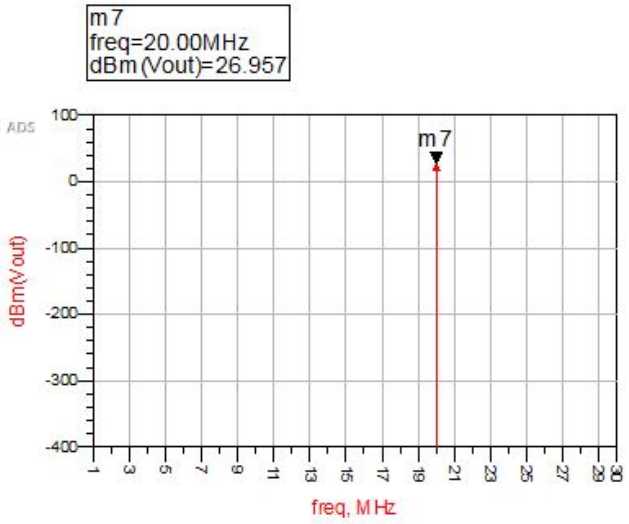

Figure 9: Output signal from the receiver

that in order to achieve image rejection mechanism through quadrature modulation, Hilbert transform is utilized to rotate the real part of the signal 90 degree counterclockwise and imaginary part of the signal 90 degree clockwise, which the summation of two quadrature signals at the power combiner should eliminate the image part of the signal. In [3] Behzad Razavi explained that in order to do so, low-side injection instead of high-side injection is applied at the local oscillators, which means $w_{LO} < w_{fund}$ has to be valid. Therefore, to meet the specification of the output signal bandwidth (2MHz), f_{LO} is selected as 2.38GHz instead of 2.42GHz to realize low-side injection. Besides, two phase shifters on one path are associate 45 degree phase shifting, and another two phase shifting on the another signal path are both associated with -45 degree phase shifting, to achieve 90 degree phase differentiation on two the local oscillators' signals ($sin(2\pi f_{LO})$ and $cos(2\pi f_{LO})$), and also 90 degree phase differentiation between the signals on two paths.

A. *Image Rejection Test*

Different to *Section II*, the IR test will be conducted at the output of the receiver because of the down-converting and the mechanism of Hartley receiver: image is not filtered but self-cancelled. The oscillators do the down-converting of the received signal and the IR test is done at 20MHz, which is shown in *Fig. 12*. Notice that the image and the received signals are at the same frequency. The image rejection is calculated as 87.279dB, above the specification (70dB).

B. *IIP3 Test*

The same as *Section II*, two tone test is conducted (2.399GHz and 2.401GHz) and the result is plot in *Fig. 13*. Utilizing the same equation in *Eq. 21*, the IIP3 is calculated as -12.13dBm, larger than the specification therefore meets the specification.

C. *-1dB Compression Test*

The output power versus input power is plotted in *Fig. 14*. It is obvious that the linear region extends beyond -30dBm: the -1dB compression point is about -21dBm, which is larger -30dBm in the specification.

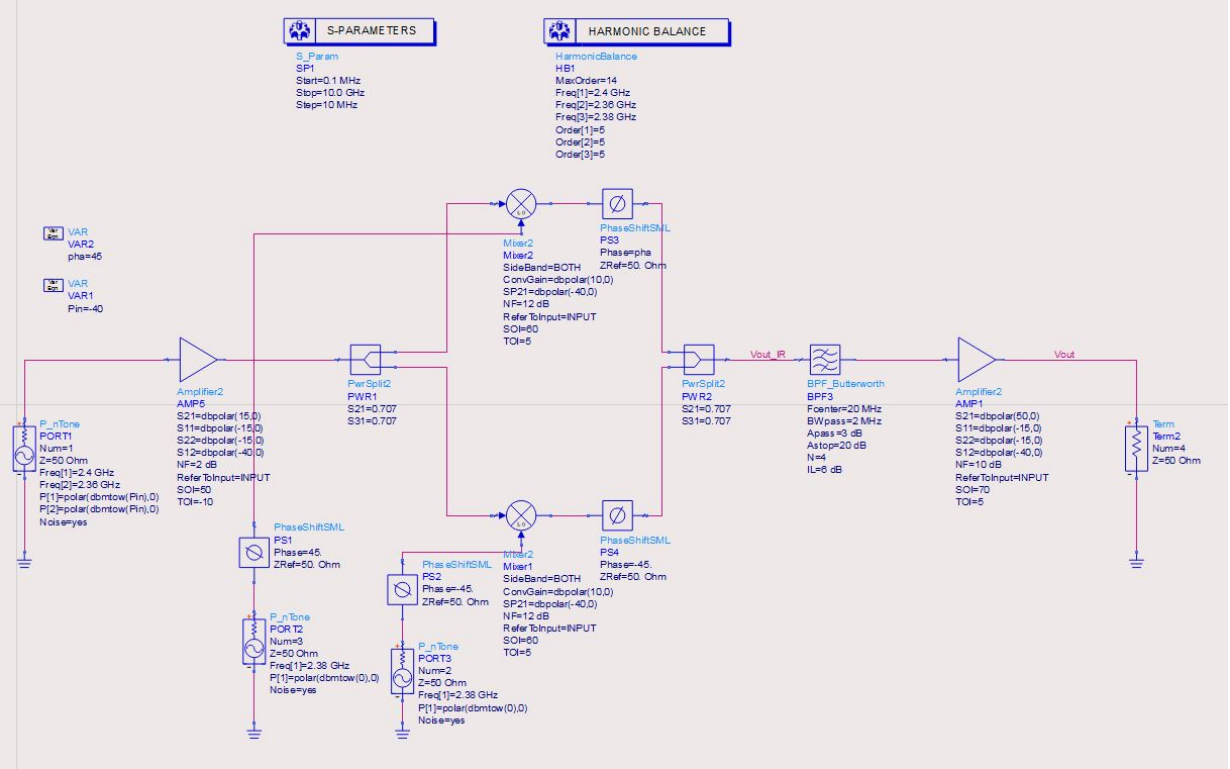

Figure 11: Schematic of a Hartley receiver (*Amplifier5* → *Mixer1 (top) & Mixer1 (bottom)* → *Amplifier1*))

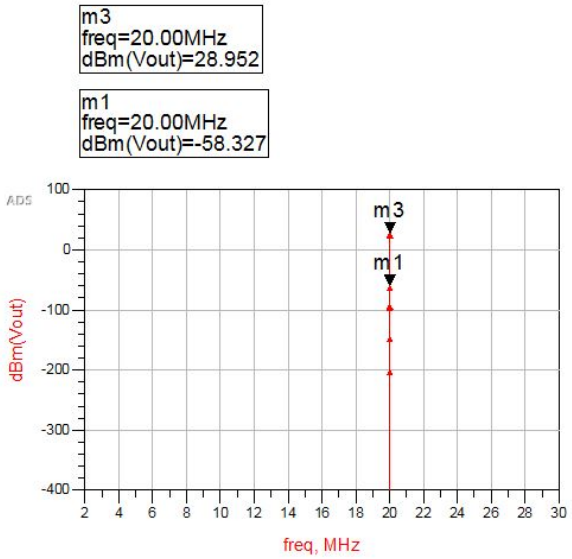

Figure 12: Image rejection test of Hartley receiver

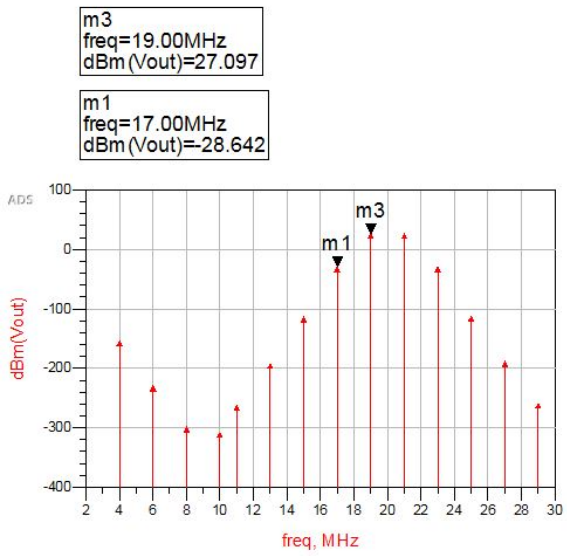

Figure 13: IIP3 test plot

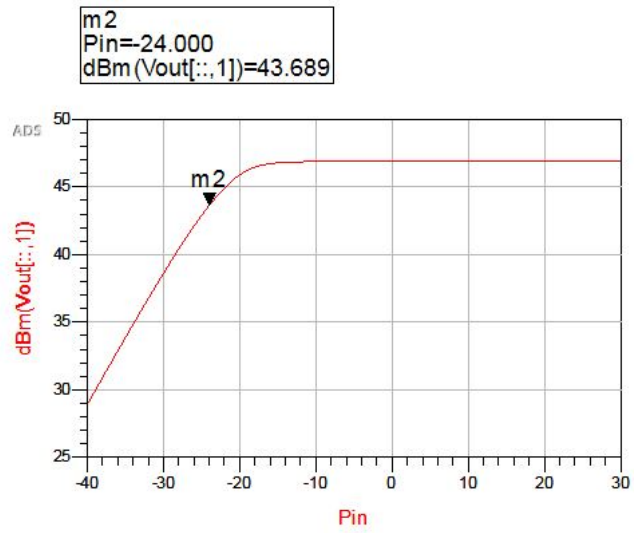

Figure 14: -1dB compression plot

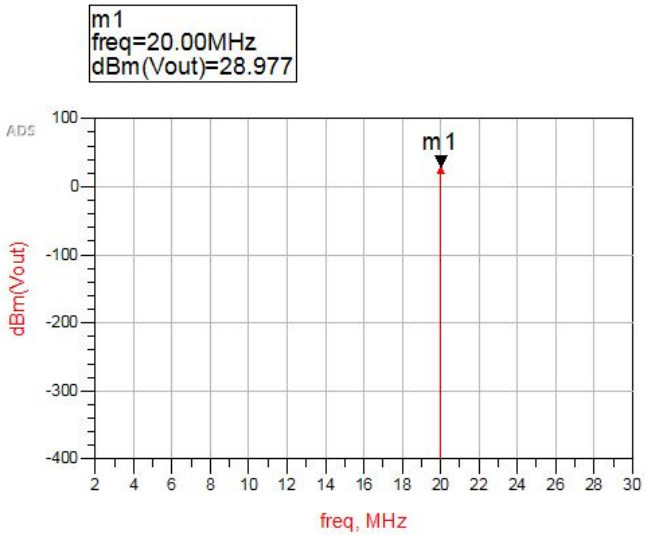

Figure 15: Output signal power of Hartley receiver

D. Gain Test

The output signal power at frequency 200MHz at the receiver's output is measured as 28.9dBm, which results in a 69dB gain. Therefore it also meets the specification (larger than 65dB), which is close to the result obtained in *Section III A* analytically.

E. Noise Figure Test

The NF does not really meet the specification that is about 21dB (*Fig. 15*), larger than the desired NF value (11dB). Some

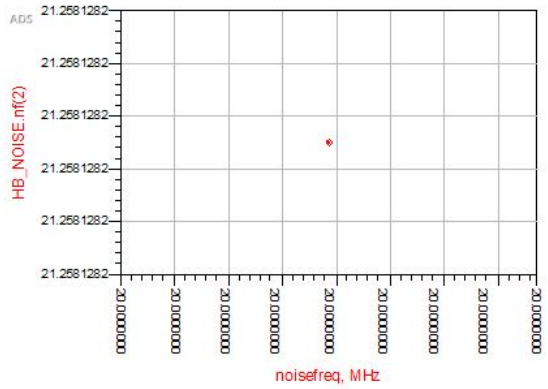

Figure 16: Noise Figure of Hartley receiver

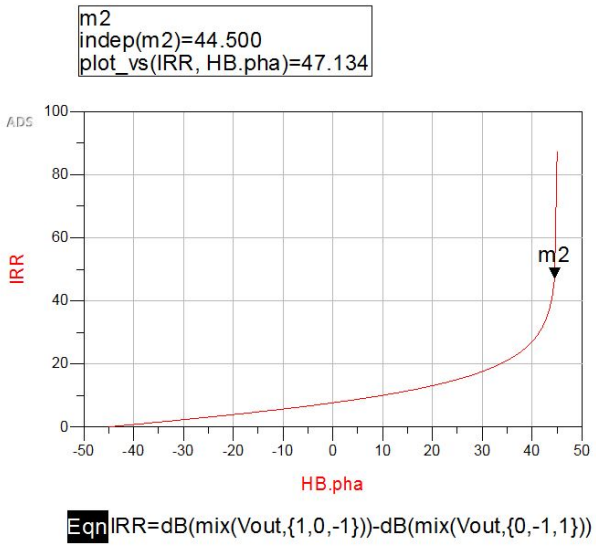

Figure 17: IIR degrading with the mismatching of phase

noise figure improvement should be applied to the design.

F. Phase Sensitivity

As pointed in [3], Hartley receiver is very sensitivity to the deviation of the phase shifter since image overlapping has to be perfect in order to reject the image. The sensitivity of the receiver to the deviation of the phase shifter is studied by varying the phase of one phase shifter and the IIR is plotted versus the shift deviation. The calculation is also done in ADS via equation utility, which is also shown in *Fig. 17*. When the phase is 45, phase shifters are matched and image rejection is achieved nicely. However, with just 0.5 degree phase mismatch (marker *m2* in *Fig. 17*), IRR drastically degrades from above 70dB to 44.5dB.

Table VI: Summary of specifications of Hartley receiver

Parameters	Desired	Actual	Meet the spec?
Image Rejection	$\geq$ 70dB	87.279dB	Yes
IIP3	$\geq$ -20dBm	-12.13dBm	Yes
1-dB Compression Point	$\geq$ -30dBm	about -21dBm	Yes
Receiver Gain	$\geq$ 65dB	69dB	Yes
Noise Figure	$\geq$ 11dB	21dB	No
Signal Bandwidth at End of Receiver	2MHz	2MHz	Yes
Sensitivity to the phase mismatch $\leq$ 70dB	-	0.5 degree	-
f_{LO1}	-	5GHz	-
f_{LO2}	-	2.62GHz	-

G. Summary of Hartley Receiver

The specifications achieved from the designed Hartley receiver are summarized in `Table VI`, where only the NF does not meet the desired value, which is majorly contributed by the high gain and high NF of the last stage. Hartley receiver is intrinsically sensitive to the phase mismatch from the phase shifters, therefore in hardware implementations temperature and manufacture of the circuit will dominant the performance of the receiver.

IV. Conclusion

In this assignment three types of RF receivers are studies, which are: simple heterodyne architecture, dual-IF architecture, and Hartley image reject architecture. They have their own pros and cons:

Simple heterodyne architecture as the name suggests, it is a very simple receiver architecture and therefore for the actual circuit implementation, it will consume less silicon area and also less power consumption; however, it suffers from low image rejection performance and low gain.

Dual IF-filter receiver is the modified version of simple heterodyne architecture. It employs two local oscillators with two different frequencies. The first mixers will mix the received signal and up-convert to the higher frequency so that the image reject filter can reject the image signal nicely; then the second mixer will down convert the signal to let the following filter to reject intermodulation signals. This design has good results in all specifications, but the power consumption as well as the silicon area will be the two major concerns. Also, making a very high-frequency oscillator needs special care on the phase-lock-loop (PLL) design that makes the implementations challenging.

Hartley receiver is a smart design that utilize Hilbert transform property to reject the image via the quadreture modulation architecture. It has less components and robust image rejection performance. However, the high NF and sensitivity of the phase shifter make the actual implementations of this receiver questionable.

With these conclusions, dual IF-filter receiver has the best robustness.

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Zonghao Li Zonghao Li is a first year Master of Engineering student at McGill University.