ECE1396H Assignment 1

Zonghao Li #1003843148

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A. Op-amp integrator simulation

1) a: Fig. 1 shows the small signal response of the integrator given in the assignment, from 1 kHz to 20 GHz. The general bilinear transfer function is given by $H(s) = \frac{k_1 s + k_0}{s + w_0}$. For a first-order low pass response in Fig. 1, $k_1 = 0$. At $s = 0$, the DC gain is about 0 dB, therefore $k_0 = w_0$. From the simulation, w_0 is the -3 dB frequency at 746.4 MHz, therefore $k_0 = w_0 = 2\pi \times 746.4 \times 10^6 = 4.7 \times 10^9$ rad/s.

2) b: Fig. 2 (left) shows the input sinusoidal signal at 1 MHz with 1 mV, Fig. 2 (right) shows the output signal from the given testbench, and Fig. 4 (left) shows the DFT of Fig. 2 (right) (output signal), with a sampling frequency $f_s = 64$ MHz, N = 1024 and simulation time 16 μs. A DC component equals to 3.75 dB is found, and a -60.09 dB is found at the fundamental frequency of the signal that is 1 MHz. If we only look at the small signal, a noise floor at -171.6 dB is found across the frequency range, so a SDR = 111.5 dB is achieved by the circuit. An output THD = 1.05% is found.

3) c: Fig. 3 (left) shows the input sinusoidal signal at 1 MHz with 100 mV, Fig 3 (right) shows the output signal from the given testbench from the assignment, and Fig. 4 (right) shows the DFT of Fig. 3 (right) (output signal), with a sampling frequency $f_s = 64$ MHz, N = 1024 and simulation time 16 μs. A DC component equals to 3.75 dB is found, and a -20.09 dB is found at the fundamental frequency of the signal that is 1 MHz. If we only look at the small signal, a noise floor at -131.6 dB is found across the frequency range, so a SDR = 111.5 dB is achieved by the circuit. A THD = 1.05% is found at the output. To remove the DC component, it is required to have fully differential topology.

4) d: The resistor was changed to a NMOS in the testbench. Fig. 5 (left) shows the frequency response by sweeping the NMOS gate voltage from 0 to 1.1 V with 0.1 V increment per step. Fig. 5 (right) shows the 3 dB bandwidth change with respect to the above gate voltage variation. Fig. 6 shows the frequency response of the gain when the gate voltage of the NMOS is 0.7 V.

B. Second Order Bandpass filter

A second-order bandpass filter with a unity gain centered at 200 MHz is designed. From the lecture, for a given general second-order bandpass filter topology with the given specifications, the transconductance of each cell is calculated as: G_{m1} = G_{m2} = 0.2512 mS, G_{m3} = G_{m5} = 50.21 μS. The transconductor topology was selected as Fig. 7 (left), where Q1 and Q2 are in active region and Q3 and Q4 are in triode region. For Q1 and Q2, $W = 1.2$ μm and $L = 0.06$ μm, and for Q3 and Q4, $W = 0.12$ μm and $L = 0.06$ μm. The common-mode voltage is set to 0.55 V to give enough headroom for the signal swing ($V_{cc} = 1.1$ V). The input signal voltage is 250 mV. The small signal transconductance with different biasing current I_1 are given in Fig. 8, where when I_1 = 4.4 μA, G_{m3} = G_{m5} = 50.27 μS, and when I_1 = 34 μA, G_{m1} = G_{m2} = 0.249 μS. These values are close to the given calculated value from the lecture.

The second-order bandpass filter implementation is in Fig. 7 (right). Fig. 9 (left) shows the output transient response with slow and fast corners. For nominal case, an 227.3 mV amplitude is found at the output, which is larger than the slow corner (204.7 mV) but smaller than the fast corner (228.5 mV). $|H(s)_{dB}|$ is shown in Fig. 9 (right), where at f_0 = 199.5 MHz, the gain is around 0 dB for all three cases (nominal, slow and fast corners). Fig. 10 shows the DFT of the bandpass filter output, with a $\text{SDR}_{nominal}$ = 44.72 dB (M0 and M3), SDR_{slow} = 44.69 dB (M1 and M4), and SDR_{fast} = 46.02 dB (M2 and M5) achieved. For DFT plotting, f_s = 1024 MHz, N = 1024, and simulation time is 1 μs. The quality factor Q = 19 for this filter, which is higher than the value given in the lecture, but it can be done by moving the zero of the filter towards lower frequency to decrease the quality factor and increase the bandwidth. After some tuning for the biasing currents, the final biasing currents for G_{m1} and G_{m2} is 200 μA, and for G_{m3} is 1 μA, and for G_{m5} is 50 μA. With a power supply 1.1 V, the total static power consumption is 1.1 V $\times$ ((200 μA) $\times$ 2 $\times$ 2 + 1 μA $\times$ 2 + 50 μA $\times$ 2) = 991.1 μW.

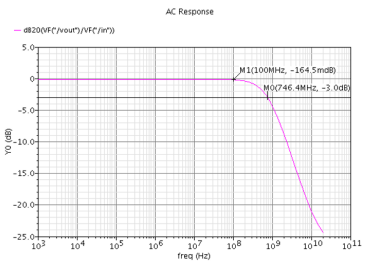

Fig. 1: Gain plot of the small signal response of the integrator from 1 KHz to 20 GHz.

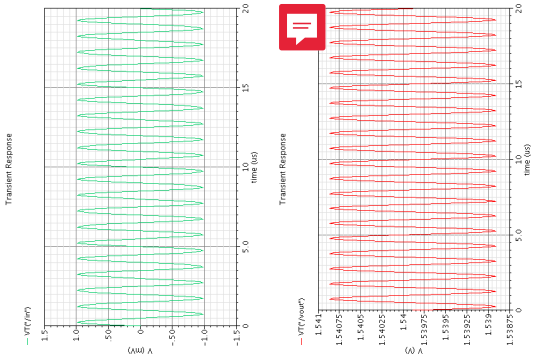

Fig. 2: 1 MHz, 1 mV amplitude input signal (left), and output (right) from the testbench.

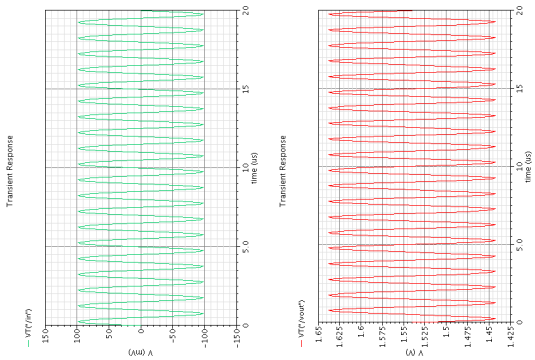

Fig. 3: 1 MHz, 100 mV amplitude input signal (left), and output (right) from the testbench.

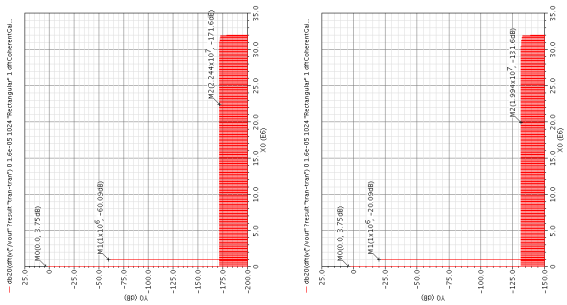

Fig. 4: DFT of the output signal from Fig. 2 (left) and Fig. 3 (right).

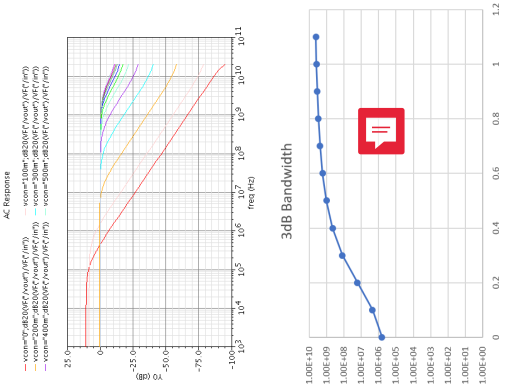

Fig. 5: Frequency response of the testbench over different gate voltage across the NMOS (left), and the change of 3 dB bandwidth (right).

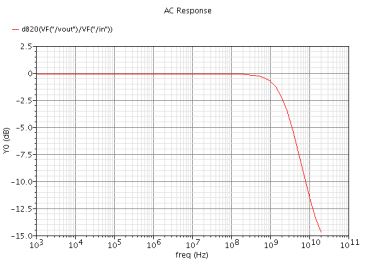

Fig. 6: Frequency response of the testbench when the gate voltage of NMOS is 0.7 V

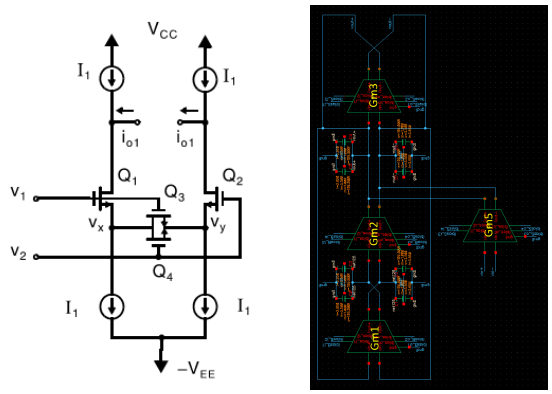

Fig. 7: Transconductor using varying bias-triode transistors (left); fully differential second-order bandpass filter (right).

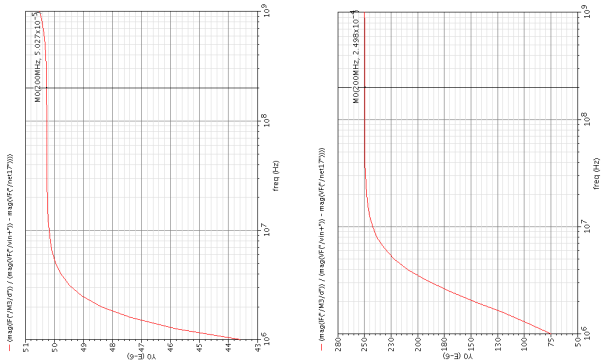

Fig. 8: Transconductance of the transconductor with I_1 = 4.4 μA. G_m = 50.27 μS (left); transconductance of the transconductor with I_1 = 34 μA. G_m = 0.249 mS at 200 MHz (right).

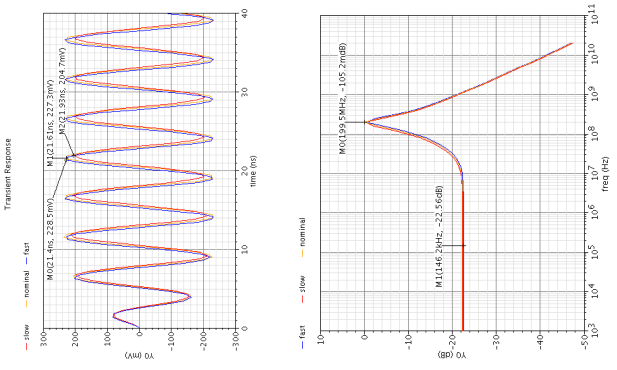

Fig. 9: Transient response of the bandpass filter output with slow and fast corners (left); frequency response of $|H_{dB}|$ of the bandpass filter with slow and fast corners (right).

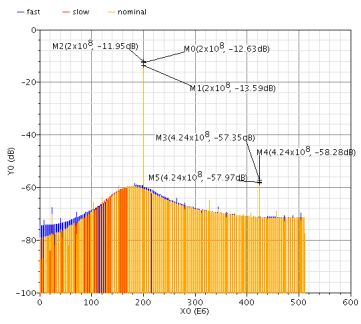

Fig. 10: DFT of the bandpass filter output with slow and fast corners.