

## 22.1 A 90GS/s 8b 667mW 64× Interleaved SAR ADC in 32nm Digital SOI CMOS

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Forthcoming optical communication standards such as ITU OTU-4 and 100/400Gb/s Ethernet require ADCs with more than 50GS/s and at least 5 ENOB to enable complex equalization in the digital domain. SAR ADCs and interleaved ADCs made impressive progress in recent years. First CMOS ADCs with at least 6b and conversion rates exceeding 20GS/s were presented [1-3], proving that interleaved SAR ADCs are an optimal choice for high-speed ADCs with moderate resolution. We present an interleaved CMOS ADC architecture based on an asynchronous redundant SAR ADC core element. It was measured up to a sampling rate of 100GS/s and can be operated from a single supply voltage. At 90GS/s, the measured SNDR stays above 36.0dB SNDR up to 6.1GHz and 33.0dB up to 19.9GHz input frequency while consuming 667mW. The ADC is implemented in 32nm digital SOI CMOS and occupies 0.45mm<sup>2</sup>.

Figure 22.1.1 shows a top-level overview of the ADC. The differential input is terminated by  $2 \times 50\Omega$ , protected with reduced ESD-diodes and directly connected to the 4 sampling and interleaving slices that feed buffered samples to 16 sub-ADCs. Therefore a total of 64 sub-ADCs convert the analog samples. The aggregated digital output is captured by a large high-speed memory block storing 8192 digitized samples. The architecture requires only 4 timing-critical clock phases, namely those connected to the first input sampling switches. These critical phases are derived from a half-rate differential clock  $ck2$  of up to 50GHz, which is divided by 2 in CML and converted to CMOS levels. An externally controlled digital signal  $dskew$  serves to adjust the skew between the 4 phases with a step size of less than 30fs. A separate sub-clock generation block receives the 4 clock phases and generates all non-timing-critical sub-clocks for the interleaver and sub-ADCs.

The core of the ADC consists of the sampling stage and interleaving architecture, as shown in Fig. 22.1.2. Sampling is implemented in voltage mode. Each of the 4 sampling switches  $M_1$  is connected in series with a 1 by 4 demux stage, formed by transistors  $M_2$ , before connecting to the sampling capacitors  $C_s$ . Implementing 4 interleaved sampling switches and a 1:4 demux stage proved to be optimum for highest bandwidth while still providing sufficient hold time on the sampling capacitor to buffer the sampled voltage. Single NMOS sampling switches are fast and provide sufficient linearity for an 8b ADC. Size and operating point of the sampling transistors are optimized for high bandwidth and high linearity across corners, with operating temperatures up to 100°C. One of the 4 demux switches is enabled by  $en16$  before the rising edge of  $ck4$  and disabled after the falling edge of  $ck4$  to eliminate influences of  $en16$  on the sampling window. The sampling capacitor  $C_s$  is reset shortly before the sampling window by  $res16$ . The signal  $en16$  is enabled before  $res16$  is disabled to eliminate ISI by canceling remaining charges on transistor  $M_1$  from the preceding sampling phase. This leaves about 120ps hold time of the sampled voltage on  $C_s$ . A source follower ( $M_3$  and  $M_4$ ) is chosen to buffer the sampled voltage because of its superior speed, noise figure and linearity. For high linearity, the source follower is operated with an output common mode of close to half the supply voltage. Its output common mode also defines the common mode of the sub-ADC and therefore the comparator. Control of the comparator common mode enables a good trade-off between conversion speed and comparator input-referred noise [4]. The buffered voltage is connected through a second demux stage ( $M_5$ ) controlled by  $en64$  to the capacitive DAC of a SAR ADC. Signal  $en64$  is also used to trigger the conversion of the asynchronous SAR ADC. Both demux stages in the interleaver feature cross-coupled NMOS switches, with gates connected to GND to cancel signal feed-through.

The asynchronous SAR ADC shown in Fig. 22.1.3 features a redundant capacitive DAC with a constant common mode and alternate comparators for enhanced speed. The SAR ADC is described in detail in [4]. A falling edge on  $en64$  starts the asynchronous conversion and a rising edge of  $en64$  resets the ADC if it did not finish. The alternate comparators eliminate the reset phase of the comparator from the critical path, thus increasing speed by about 30%. While one comparator is active, the other comparator resides in reset state, and

vice versa. The capacitive DAC is reset at the end of the conversion to eliminate ISI and zero the offset of the comparators. A low-power switch-capacitor reference buffer [5] is controlled with  $V_{gain}$  from an R-3R ladder to adjust the gain of each SAR ADC. The digital input  $dgain$  is set externally and enables per-channel gain calibration.

The ADC is manufactured in a 32nm SOI CMOS process with an area of 470x960μm<sup>2</sup>. The interleaver/sampler and 64 SAR ADCs occupy 370x960μm<sup>2</sup> and the clock divider 90x100μm<sup>2</sup>. The ADC supply on the interleaver, including sampler, CML clock divider and CML to CMOS stages ( $V_{DI}$ ), is 1.2V for 90GS/s, and the SAR ADC supply ( $V_{DA}$ ) is set to the same level for 90GS/s. To save power,  $V_{DA}$  can be lower than  $V_{DI}$  for lower conversion rates. At 1.2V and 90GS/s, the measured total power consumption of 667mW consists of 56mW for the CML clock divider and CML to CMOS stages, 112mW for the interleaver/sampler and sub-clock generation, and 499mW for the SAR ADCs including drivers for the memory block.

Gain calibration is performed off-chip with on-chip fine-grain adjustment on the R-3R ladders of each SAR ADC. The internal offset of the comparators is corrected in background in each SAR ADC, whereas the residual offset between the ADC channels is subtracted off-chip. For each supply voltage and conversion rate, gain and offset are calibrated only once at 2.1GHz input frequency. For better sensitivity, skew is calibrated once at a higher input frequency of 19.9GHz. Bandwidth mismatch is not calibrated.

Figure 22.1.4(a) shows SNDR vs. input frequency. More than 36.0dB is achieved up to 6.1GHz and 33.0dB up to 19.9GHz. The measurement series at 100GS/s is taken with skew calibration disabled, therefore the SNDR at higher input frequencies is limited by phase mismatch of the 4 input clock phases. With skew calibrated, lower SNDR at higher input frequencies mainly stem from the reduced amplitude due to the limited bandwidth, as shown in Fig. 22.1.4(b). Total jitter of individual measurements (8192 samples), including the external clock and input signal generators, is estimated to approx. 60fs based on modulo-time plot analysis and SNR comparison at different input frequencies at 90GS/s. This is in good agreement with jitter simulations that depending on corners, predict 30 to 50fs jitter. The ADC is measured with sampling frequencies from 56GHz to 100GHz (see Fig. 22.1.5(a)). Owing to the asynchronous design of the sub-ADC, the SNDR decreases gradually when some SAR cycles are no longer completed. Figure 22.1.5(b) shows the power consumption vs. sampling frequency. As can be seen at 70GS/s, power consumption highly depends on  $V_{DA}$ . 100GS/s was achieved at 1.27V on  $V_{DI}$  and  $V_{DA}$  with a reduced reset time of the capacitive DAC inside the SAR ADCs at the end of the conversion cycle. Best FoM is achieved at 70GS/s with 121fJ/conversion-step. FOM at 90GS/s is higher with 203fJ/conversion-step, mainly because of the increased voltage on the SAR ADCs.

SFDR of 41.4dB at 19.9GHz input frequency and full-scale input amplitude is limited by 3<sup>rd</sup>-order harmonic distortion (see Fig. 22.1.6(a)). Figure 22.1.6(b) compares the performance of high-speed CMOS ADCs with at least 6b resolution. As shown in the comparison table, this design exhibits the highest sampling frequency of previously reported 6b+ CMOS ADCs. The FoM is more than 50% lower and the technology-adjusted area is 4 times smaller than other 6b+, >20GS/s ADCs [1,7].

### References:

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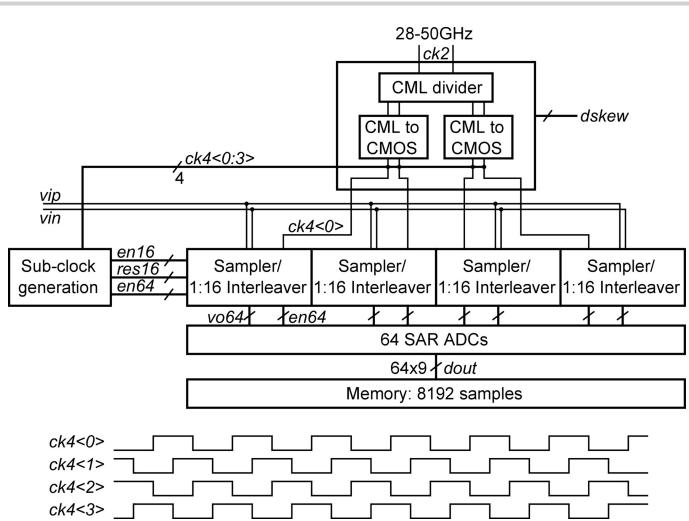


Figure 22.1.1: Architecture of the highly interleaved SAR ADC with a timing diagram of the clock signals defining the sampling time.

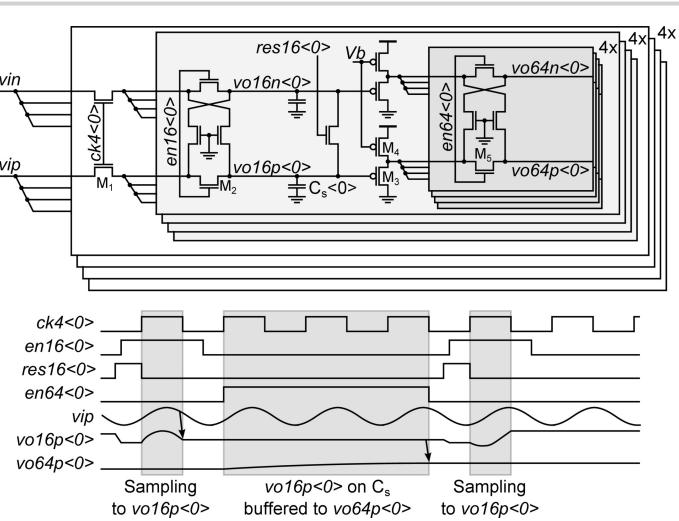


Figure 22.1.2: Schematic details of the differentially implemented 1:64 interleaver.

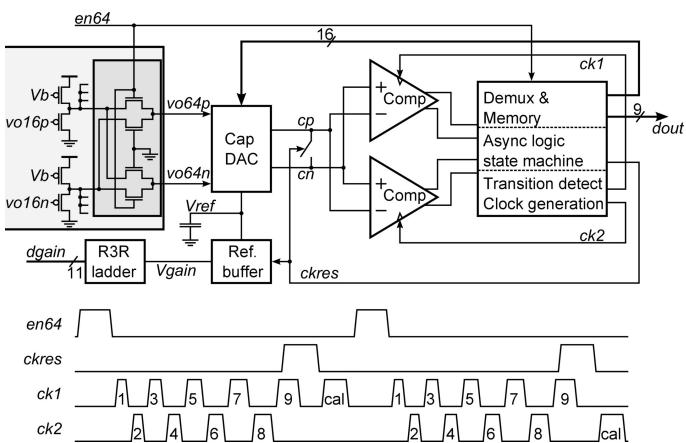


Figure 22.1.3: SAR ADC architecture [4] with last demux stage of the interleaver and corresponding timing diagram.

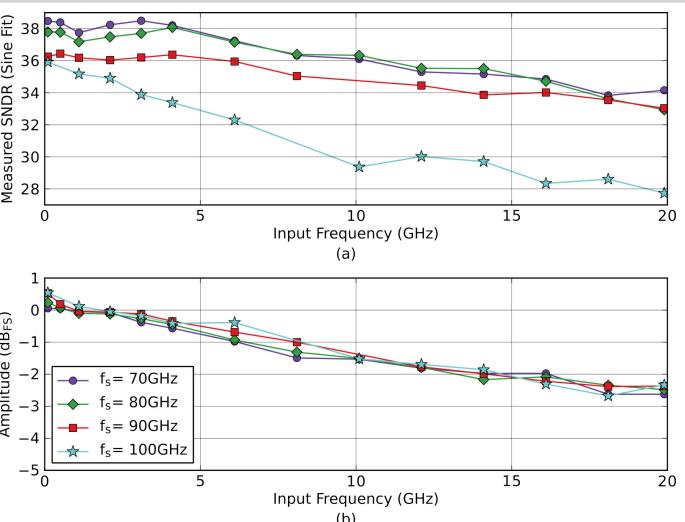


Figure 22.1.4: Measured SNDR and amplitude vs. input sine frequency for different sampling frequencies referred to 2.1GHz input frequency.

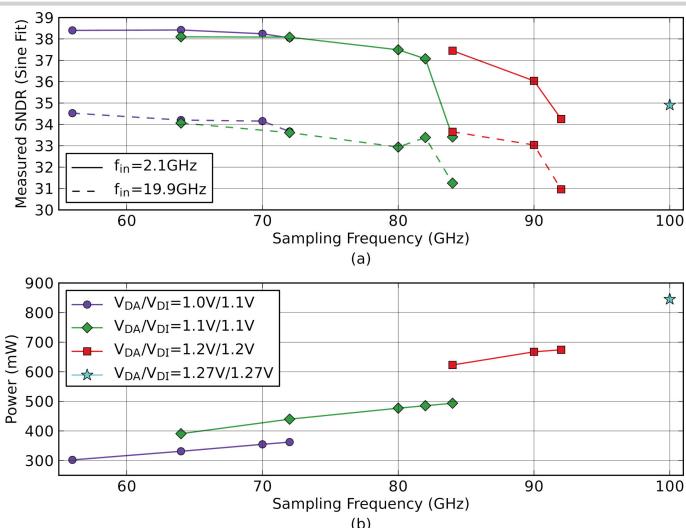


Figure 22.1.5: SNDR and power vs. sampling frequency for different supply voltages.

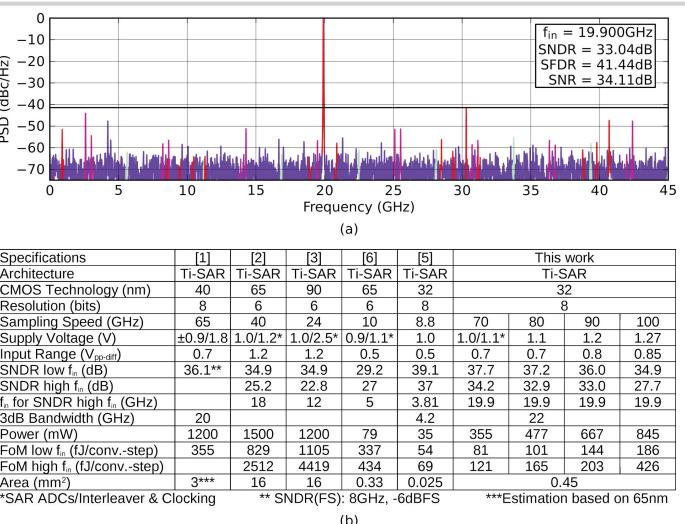


Figure 22.1.6: Spectrum of a 19.9GHz full-scale input signal and performance comparison table.

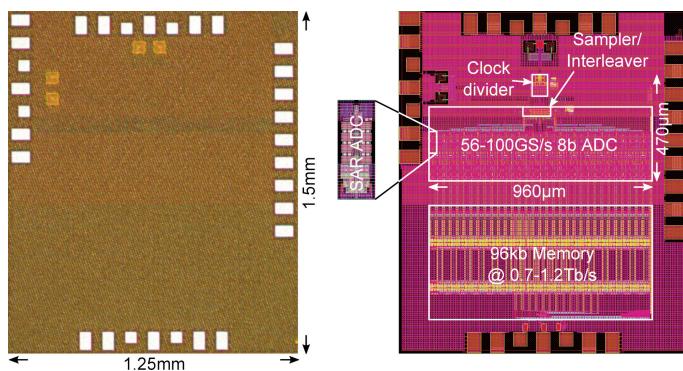


Figure 22.1.7: Chip micrograph and layout. The 96kb memory block stores 8192 samples with Hamming encoding.