Assignment 6: 8-bit Time-Interleaved ADC Simulation and Characterization

Objectives

- To simulate the static and dynamic performance of an 8-bit ADC using a verilog_A model that accounts for comparator mismatch and finite rise and fall time.
- To simulate the static and dynamic performance of a 2x time-interleaved 8-bit ADC using a verilog_A model that accounts for comparator mismatch and finite rise and fall time.

1. Preparation:

Study Chapters 17 in the textbook, the associated course slides.

You will use Cadence Analog Artist with the cmos65nm design kit with the *adc_8bit* cell and the *dac_8bit_ideal* cell from the *ahdl* library in all simulations. The properties of the 8-bit adc and ideal 8-bit DAC cells are shown in ***Fig*.1**.

2. 8-bit ADC Simulation and Characterization (10 points)

Consider a single 8-bit ADC driven by a clock signal with 5ps rise and fall times. The logic swing is 0 to 1.1V, representative of the *cmos65nm* CMOS technology. The ADC drives an ideal 8-bit DAC whose output is used to monitor the static and dynamic

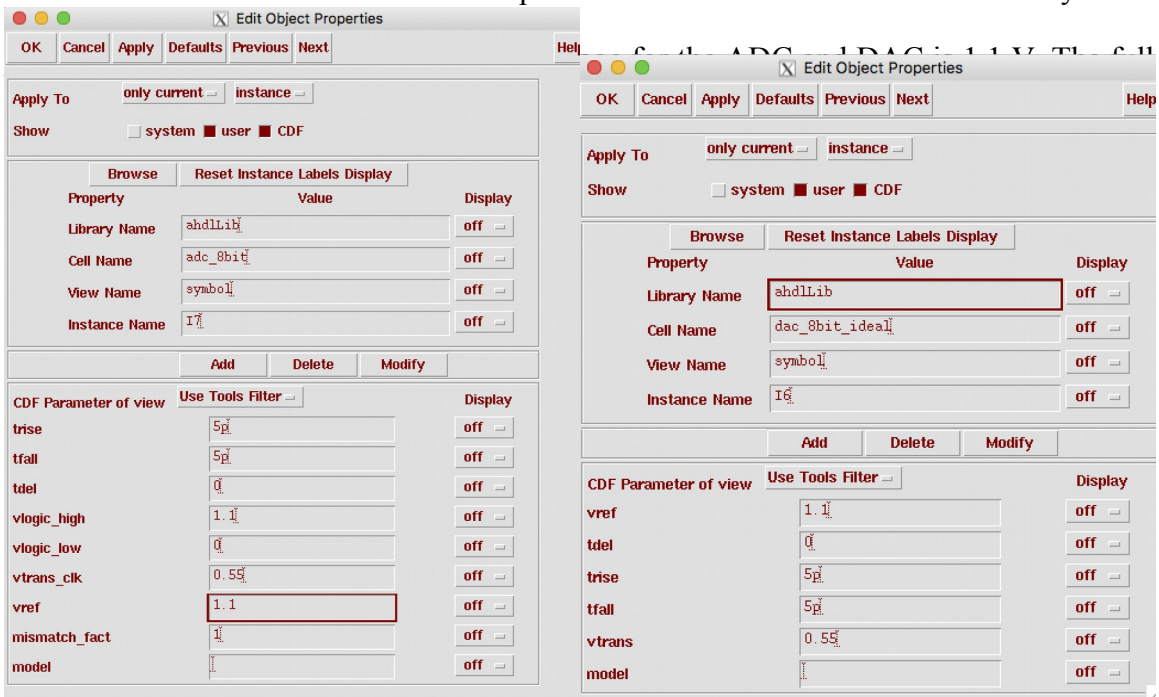

Fig.1 a) 8-bit ADC properties form and b) 8-bit ideal DAC properties form.

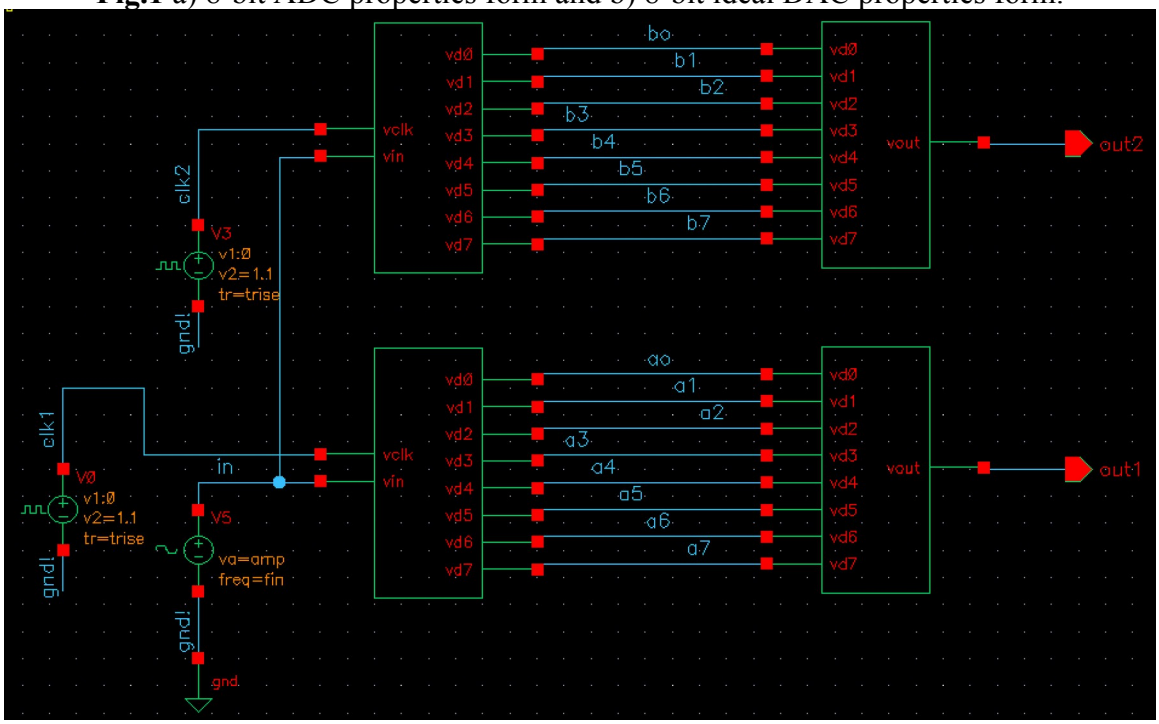

Fig.2 2x Time-Interleaved ADC test bench

a) Simulate the ***DNL*** of a single 8-bit ADC at the clock frequency specified in **Table 1** with the mismatch factor set to 0%. Plot the ***DNL*** as a function of output digital code **(2 points).**

b) Repeat **a)** above with the ***mismatch factor*** set to 1%. Explain the results **(3 points).**

c) With the ***mismatch factor*** set to 1%, simulate and plot the ***SNDR*** as a function of the input signal amplitude from 2.5 mV to 550 mV for an input sinusoid at 100 MHz. Plot the ***SNDR*** as a function of the input signal amplitude in dB. What is the ***ENOB***? (**2** points).

d) With the ***mismatch factor*** set to 1%, simulate and plot the ***SNDR*** and ***ENOB*** as a function of frequency for a full scale input sinusoid at 100 MHz, 1.1 GHz, 2.1 GHz, 3.1

GHz,, 4.1 GHz, 5.1 GHz, and 6.1 GHz. What is the effective resolution bandwidth at each sampling frequency? (**3 points**).

3. 2x, Time-Interleaved 8-bit ADC Simulation and Characterization (10 points)

Consider the time-interleaved ADC test bench in ***Fig*.2** consisting of two 8-bit ADCs, both driven by the same input sinusoidal signal source and by non-overlapping clock signals with 25% duty cycle and 5ps rise and fall times. The logic swing is 0 to 1.1V, representative of the *cmos65nm* CMOS technology. Each ADC drives an ideal 8-bit DAC whose output is used to monitor the static and dynamic performance of the ADC. The reference voltage for the ADCs and DACs is 1.1 V. The full range of the ADCs and DACs is 1.1 V.

a) Simulate the ***DNL*** of the time-interleaved 8-bit ADC at the clock frequency specified in Table 1 with the ***mismatch factor*** set to 1%. Plot the ***DNL*** as a function of output digital code. Note that you must combine the outputs from both DACs or use a digital MUX **(3 points).**

b) With the ***mismatch factor*** set to 1%, simulate and plot the ***SNDR*** and ***ENOB*** as a function of frequency for a full scale input sinusoid at 100 MHz, 1.1 GHz, 2.1 GHz, 3.1 GHz,, 4.1 GHz, 5.1 GHz, and 6.1 GHz.

What is the ***effective resolution bandwidth*** at each sampling frequency?

Compare the spectra at the combined outputs of the two DACs with those of a single DAC. Explain the results.

Are the ***effective resolution bandwidth*** and ***ENOB*** improved by time interleaving?

Do the results match theory?

What is the effective ***sampling rate*** of the time-interleaved ADC? (7 **points**).

Table 1

Surname starts with	Non-overlapping, 25% duty cycle, clock frequency, f_S
A, B, C, D	6 GHz
E, F, G, H,	6.5 GHz
I, J, K, L	7 GHz
M, N, O, P	7.5 GHz
Q, R, S, T	8 GHz
U,V,X,Y,Z	8.5 GHz