CPLATE CAPACITOR MODEL

CROLLES2 ALLIANCE

CMOS65nm TECHNOLOGY

DEVICE MODELLING TEAM (SALIM EL GHOULI)

CONTENTS

FIGURES INDEX

OVERVIEW

The Cplate device model is a physical model. The results of Quickcap[1] simulations (or measurements) are used to calculate specific and fringe capacitance. The capacitance value is calculated using the expression:

$$C = ca \times Area + cf0 \times Perimeter \qquad (1)$$

where

ca : specific capacitance (F/m2)

cf0 : perimeter (fringe) capacitance coefficient (F/m)

❑ Pins

Cplate capacitor is a 2 pins device: first and second terminal for main capacitance.

This elementary parallel metal plate capacitor consists of two plates (with an overlap: Area of top plate < Area of bottom plate) in two consecutive metal layer, which, from the layout point of view, must obey several marker layer design rules.

This elementary device thus represents a vertical capacitor, between two plates in two consecutive metal layers:

- front end simulation model is provided

- post layout simulation must accurately process such devices inside their actual context.

❑ Model nomenclature

At the moment, Cplate capacitor model is available only for metal types: 1, X and Z.

Cplate 2 pin capacitor model names are: **cm1mx**, **cmxmx, cmxmz** and **cmzmz**.

The name includes the right configuration of metals used to perform the capacitor: metal 1, metal X and metal Z.

1. QuickCap is a parasitic capacitance extraction tool. It is used in applications that demand high 3D-extraction accuracy, such as process analysis, library cell characterization, parameter extraction and modeling, correlation studies, critical block design, and critical net analysis. QuickCap provides the high accuracy parasitic data required for accurate delay and signal integrity analysis, verification, and post-layout simulation.

NOTE: It is important that the name contains information on the metal type. Capacitance value depends on it.

cm1mx	plate capacitor between metal1 and metal2 (X)
cmxmx	plate capacitor between two metal X
cmxmz	plate capacitor between metal X and metal Z
cmzmz	plate capacitor between two metal Z

DEVICE INSTANTIATION PARAMETERS

❑ Model CALL for the elementary plate capacitor:

Xname **Plus_Pin** **Minus_Pin** **ModelName** carea=**capacitor_area** cperi=**capacitor_perimeter** mismatch=**mismatch_flag** mult=**MULT_value** lpe=**LPE_Value** tometer=**microns_to_meter** c=**capacitance_value**[1]

Plus_Pin	is the first capacitor terminal
Minus_Pin	is the second capacitor terminal
ModelName	cm1mx, cmxmx, cmxmz or cmzmz (string)
carea	is the desired area of the capacitor (float)
cperi	is the desired perimeter of the capacitor (float)
mismatch	flag: to activate the mismatch effect for the device (0=disable, 1=enable)
mult	is the multiplication factor (parallel devices)
lpe	flag: is a user option to take into account the post-layout extraction mode (0,1, 2 or 3)
tometer	parameter used to transform distances in microns to meters unit (1 or 10e-6)
c	capacitance value (not used in the model)

1. The value specified here is not used in the model.

PCELL & LAYOUT

Three metal types are used to build the core of cplate capacitor. The metal level is 1, x or z type, that's why the Cplate family is composed of four different models depending on used metals. The models are named: cm1mx, cmxmx, cmxmz and cmzmz.

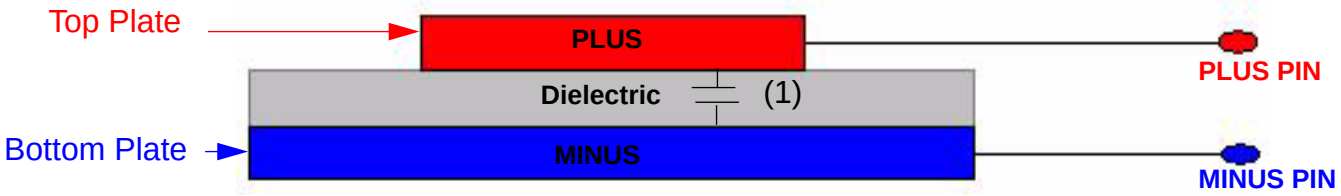

Figure 1 - Side view of cplate Pcell (A-A': next figure)

The main capacitance (1) is between the two terminals (Plus and Minus).

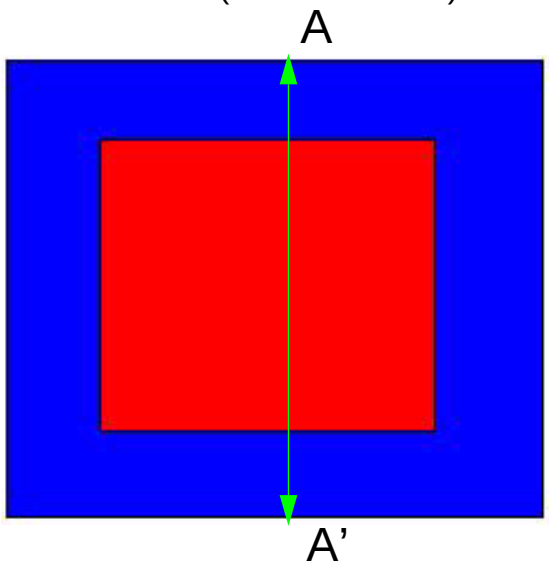

Figure 2 - Top view of the cplate Pcell (Layout)

EQUIVALENT CIRCUIT SCHEMATICS

Cplate capacitor model calculates the main capacitance which is accounted between the Plus/Minus terminals. No parasitics are evaluated in this model (Figure 1 and 3):

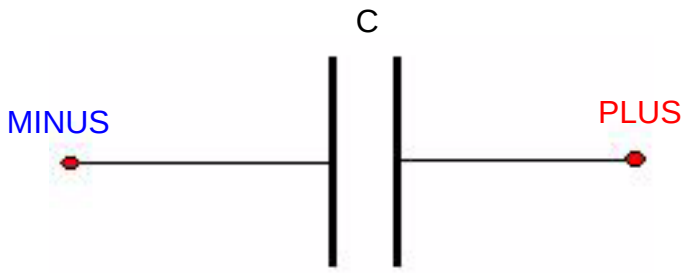

Figure 3 - Circuit diagram of cplate device

- c : the intrinsic (main) capacitor between the Plus/Minus terminals.

NOTE: This model is a simplified one.

MODELED EFFECTS

GEOMETRY SCALING

The capacitance value of the device is calculated using the expression:

$$C = ca \times Area + cf0 \times Perimeter \qquad (1)$$

where

ca : specific capacitance (F/m2)

cf0 : perimeter (fringe) capacitance coefficient (F/m)

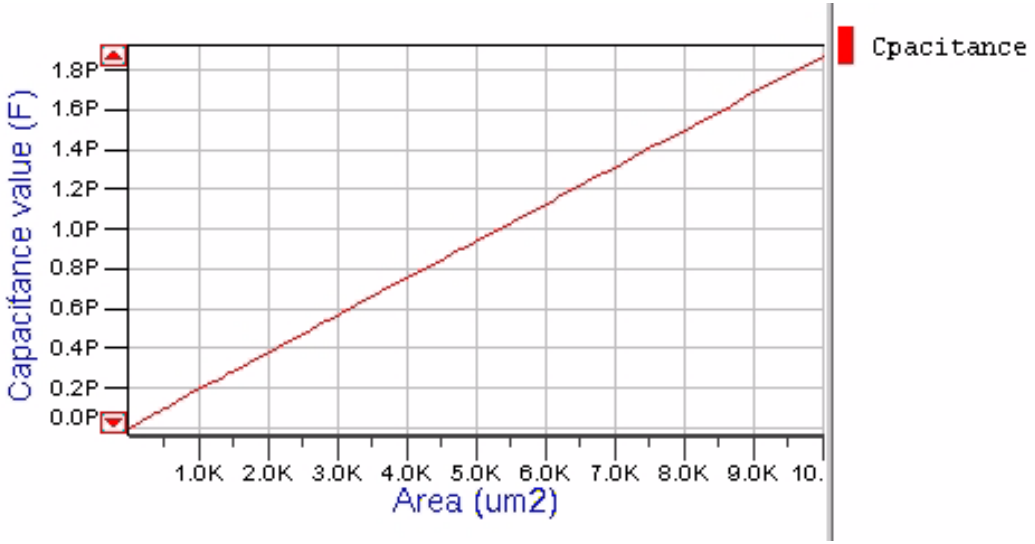

Figure 4 - Capacitance value versus Area (square cplate capacitor)

Variation of specific capacitance is shown in figure below:

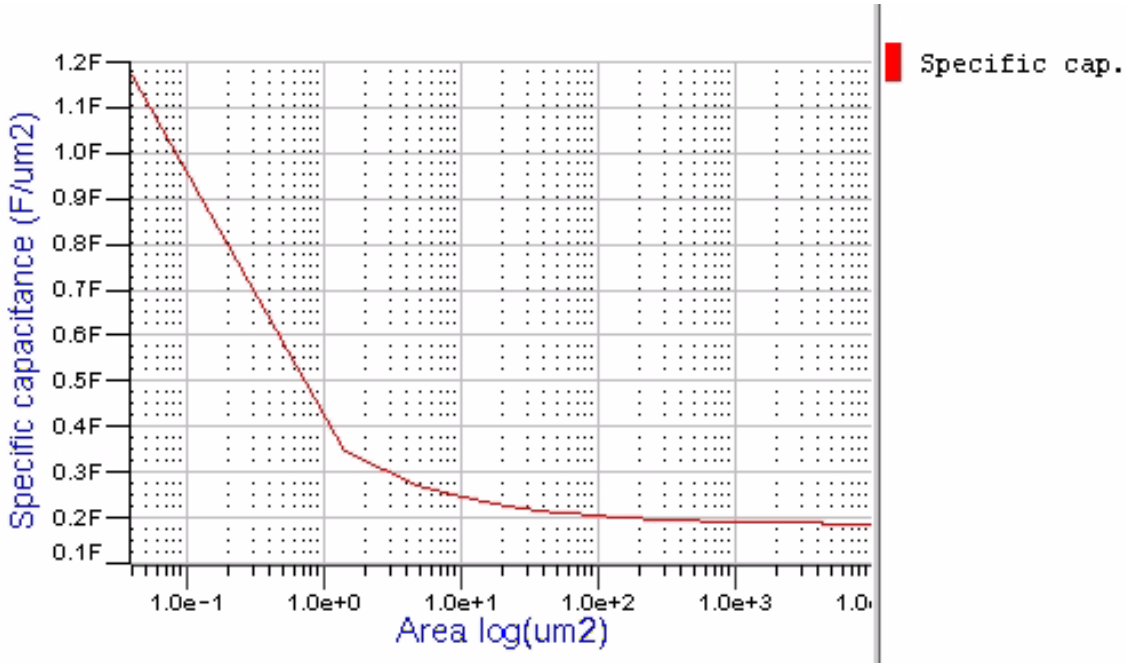

Figure 5 - Specific capacitance versus Area (square cplate capacitor)

MISMATCH MODEL

A normal distribution is used to estimate the expected main capacitance value:

$$capacitance = c0 \times (1 + \varepsilon)$$

where

- c0 : is the mean capacitance value given by the equation (1)
- ε : is a normal distribution with a standard deviation given by:

$$\sigma = \frac{c\_A}{\sqrt{2 \times c0}}$$

where

c_A : is the mismatch coefficient given by measurement values.

When c_A parameter is not specified no distribution is used and capacitance value is equal to c0.

The normal distribution is provided using the Eldo function: gauss

$$\varepsilon = 0 \qquad dev/gauss = 'fudge \times c\_A/(\sqrt{2 \times c0})'$$

where

fudge is a security parameter. It is used to be sure that the capacitance range covers measurements.

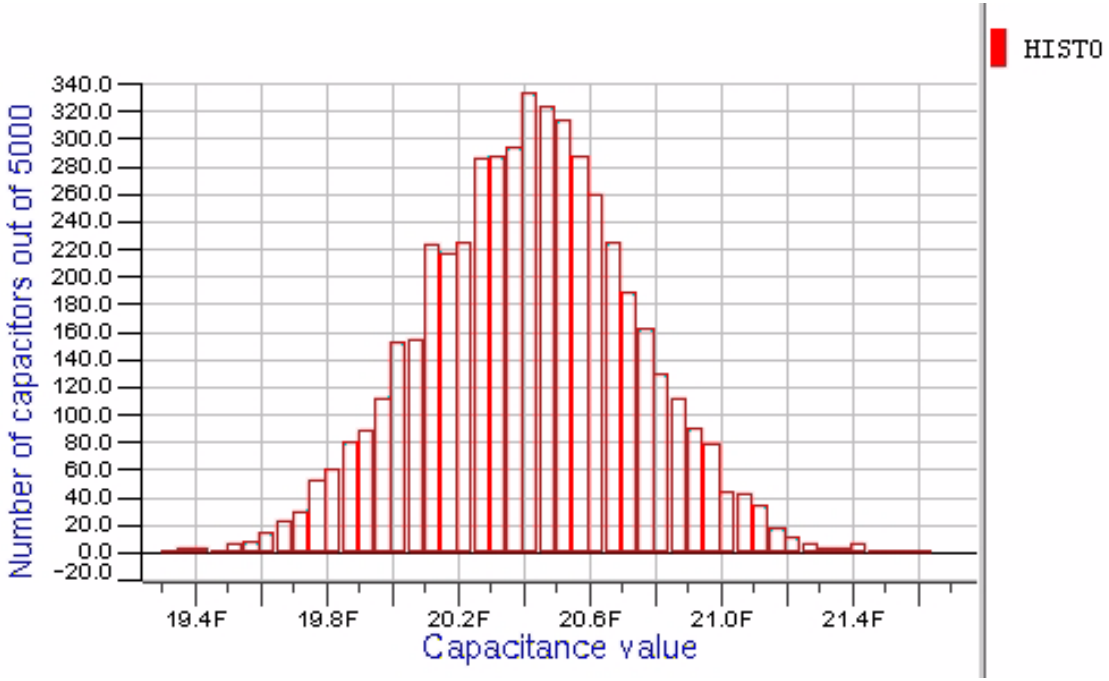

Figure 6 - Number of capacitors out of 5000 versus capacitance value

Example above is done for one cm1mx cplate capacitor (W = 10µm ; L = 10µm) simulation gives roughly: 20.417fF as capacitance value.

Realative[1] Standard Deviation specified: 15.59M

Realative Standard Deviation simulated (5000 random selection using a Monte Carlo Analysis): 15.73M

1. Standard deviation = Relative Standard deviation * Capacitance value.

POST LAYOUT SIMULATION

Each model (cm1mx, cmxmx, cmxmz and cmzmz) is managed by the LPE flag option, which permits to select the Capacitor access modeling mode. See the following table depicting the proposed options :

LPE	Body	Access_R[a]	Access_C	Extraction_mode
0	yes	yes	yes	--
1	yes	yes	no	C
2	yes	no	yes	R
3	yes	no	no	RC

a. at the moment no parasitic resistors are implemented.

The Front-End Models (F-E) :

name, a simple model which contains intrinsic capacitance (between the Plus and Minus terminals)

The Back-End Models (B-E) :

The **name** B-E model is identical to the **name** F-E model concerning the main capacitance.

CORNERS CONSTRUCTION

❑ Simulation parameters

Model coefficients ca and cf0 are extracted using Quickcap simulations and the expressions below:

$$C\_TYP = ca\_TYP \times Area + cf0\_TYP \times Perimeter$$

$$C\_MAX = ca\_MAX \times Area + cf0\_MAX \times Perimeter$$

$$C\_MIN = ca\_MIN \times Area + cf0\_MIN \times Perimeter$$

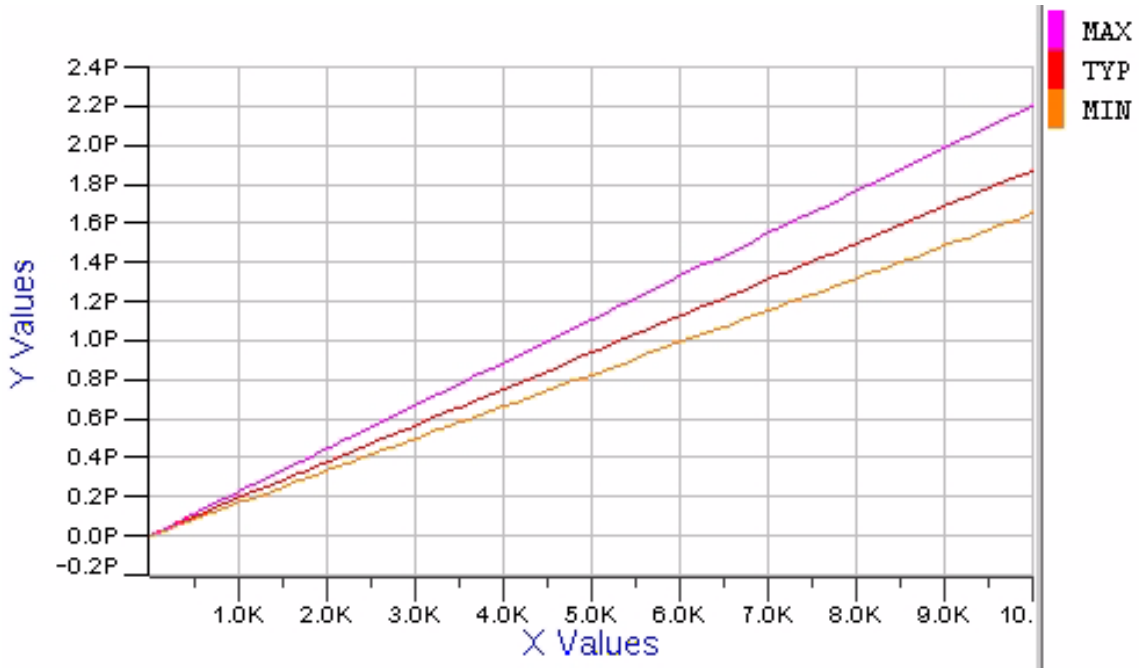

Figure 7 - Example of capacitance corners simulation (MAX and MIN)

MODEL PARAMETER LIST

areamin	(m2) Minimal area of the capacitor
careamax	(m2) Maximal area of the capacitor
careadef	(m2) Area by default of the capacitor
cperimin	(m) Minimal perimeter of the capacitor
perimax	(m) Maximal perimeter of the capacitor
cperidef	(m) Perimeter by default of the capacitor
wmin	(m) Minimal Width = sqrt(careamin)
wmax	(m) Maximal Width
wdef	(m) Width by default
lmin	(m) Minimal Length = sqrt(careamin)
lmax	(m) Maximal Length
ldef	(m) Length by default
c_A	(sqrt(F)) for capacitor mismatch effect
fudge	() security margin to cover measurements
ca[a]	(F/m2) specific capacitance
cf0	(F/m) fringe capacitance

a. In blue: parameters with specified MIN and MAX corners (see paragraph before)