Parasitic Capacitance and Mismatch Flag Settings

CMOS065 MOS Modeling Team

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Parasitic Capacitance and Mismatch flag settings

Modeling Issue	Simulation Condition	Methodology recommanded by ALLIANCE
Parasitic Capacitances	Pre-Layout simulations	Default configuration or LPE = 0 in the instance line
Parasitic Capacitances	Post-Layout simulations (VIACAP=YES)	LPE = 1 in the instance line
Corner Modeling	Predefined Corners	« mismatch_no » library selected in the « mismatch.lib » file
Mismatch	Monte-Carlo Simulations (.MC in ELDO)	« mismatch_corner » library selected in the « mismatch.lib » file + mismatch = 1 in the instance line

- Further information is available in the pdf files “mismatch.pdf” and “parasitic_capacitances.pdf”.