Assignment 4: CMOS Sample and Hold Circuit Simulation and Design

Objectives

- To simulate the operation and non-idealities of CMOS S/H circuits using a state-of-the art design kit and 65nm CMOS technology.
- To design the analog-front end of a 6-bit time-interleaved SAR ADC using Cadence Analog Artist.

1. Preparation:

Study Chapters 10 and 11 in the textbook, the associated course slides, and read the two reference papers posted with the assignment [1],[2].

You will use Cadence Analog Artist with the cmos65nm design kit and the *svt* MOSFETs from the *cmos065* library in all simulations, as in Assignments 1 and 3. You may use the circuit schematics in the two papers above. The supply voltage for all circuits is V_{DD}=1.1V.

2. CMOS T/H and S/H simulation (13 points)

Consider the CMOS S/H circuit test bench in *Fig*.1. The amplifier is an ideal buffer from the *ahdlLib* with a gain of 1, infinite bandwidth, and infinite linearity, as shown in *Fig*.2. The *vpulse* signals *clk1* and *clk2* are non-overlapping, 25% duty cycle, 2-GHz clocks with 5ps rise and fall times, as illustrated in *Fig*.3. Both capacitors have a value of 200 fF. The *n*- and *p*-MOSFETs have minimum gate length (60 nm) , N_f=5 and W=20 um.

a) Using the *vsin* cell from *analogLib,* simulate the 3-dB bandwidth in tracking mode from the input to the first hold capacitor and to the second hold capacitor. Compare these values with those obtained from hand analysis based on the switch model from

Assignment 3. Make sure that the switches are fully turned on during the AC simulation.

Plot the transfer function in dB from the input to the T/H and S/H nodes. **(2 points)**

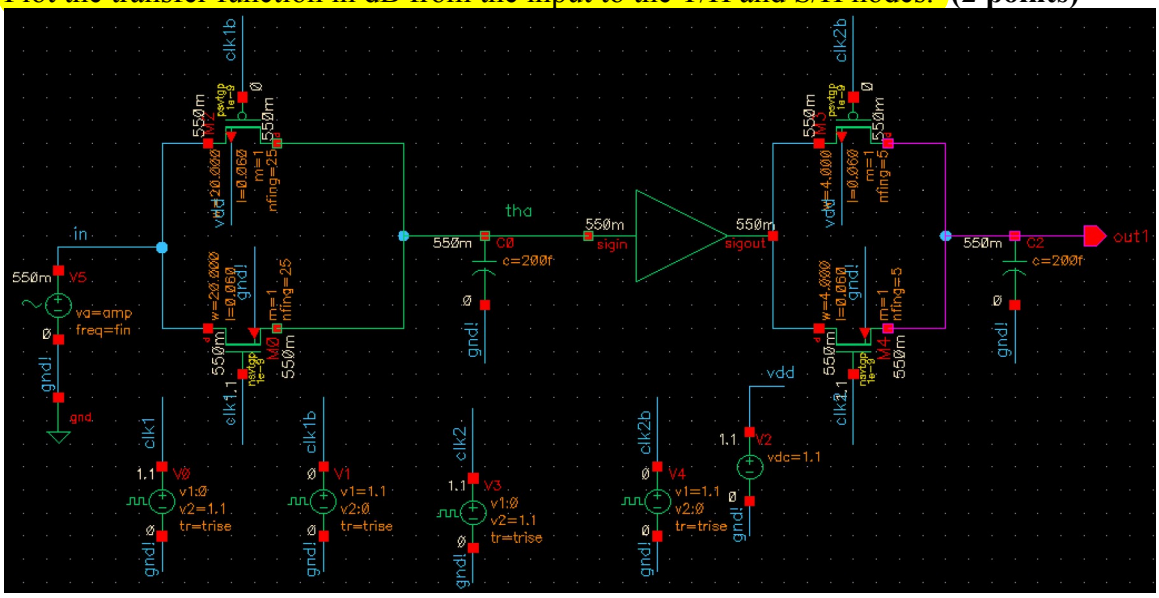

Fig.1 CMOS S/H circuit testbench schematics.

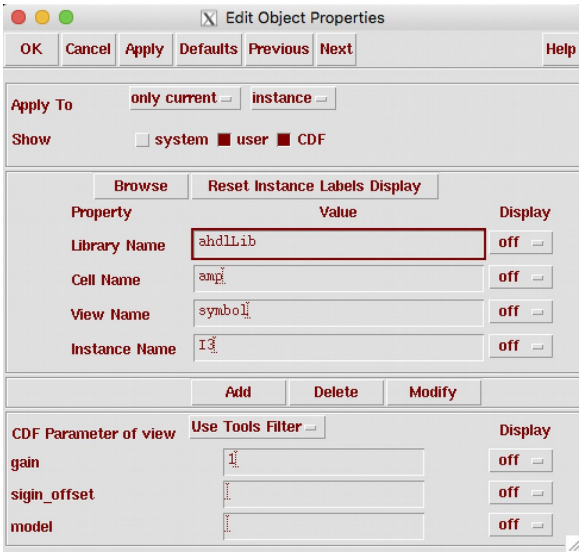

Fig.2 Buffer property form.

Fig.3 Clock *vpulse* property form a) *clk1*, b) *clk2*.

b) Apply a 50-MHz sinusoidal input signal with 500mV amplitude and simulate and plot the signal waveforms at the input node, at the T/H node, and at the S/H output node. Is the pedestal at the T/H node signal-dependent? What is the pedestal value? Simulate the spectrum (Fourier transform) at the input node and at the output node. What is the cause of the linearity (SDR) degradation? Use the difference in dB of the power of the fundamental signal and that of the largest harmonic or intermodulation product below $f_{clk}/2$ as the measure of linearity **(3 points**).

c) Repeat **c)** above for a 50-MHz sinusoidal signal with 5mV input amplitude. (**2 points**)

d) What is the IIP3? (**3 points**)

e) Simulate and plot the SDR (defined as in **a)** above) as a function of frequency at 500mV input amplitude with 100 MHz frequency steps. What is the large signal bandwidth of the SHA? The large signal bandwidth is defined as the input signal frequency at which the SDR decreases by 3 dB from its low-frequency value. (**3 points**)

3. 4x Time-interleaved S/H ADC front-end (7 points)

Design a 4x time-interleaved two-stage SH front-end using the schematic in Fig. 4 of [1] with the f_{clk} non-overlapping master clocks and $f_{clk}/4$ sub-sampling non-overlapping clocks specified in **Table 1**. Assume both sets of capacitors are 64 fF. Indicate the chosen size of the MOSFETs in the sampling and sub-sampling switches and the rational for that choice. Simulate the small-signal bandwidth from the input to $C_{s,ADC}$ and the SFDR as a function of input frequency at 500mV input amplitude. Plot the signal waveforms at the input and at the 16 capacitor outputs of the ADC front-end. Sum or multiplex the 16

outputs, plot the resulting waveform and perform a Fourier transform on it to determine the SDR (as defined earlier) of the entire front-end. How does it compare with the SDR at a single output. Explain the results.

Table 1

Surname starts with	f_{clk} (GHz)
A, B, C, D	10 GHz
E, F, G, H,	9.5 GHz
I, J, K, L	9 GHz
M, N, O, P	8.5 MHz
Q, R, S, T	8 MHz
U,V,X,Y,Z	7.5 MHz

[1] L. Kull et al., "CMOS ADCs towards 100 GS/s and beyond," IEEE CSICS, Oct. 2016

[2] S. Le Tual et al., "A 20GHz-BW 6b 10GS/s 32 mW Time-Interleaved SAR ADC with Master T&H in 28nm UTBB FDSOI Technology," IEEE ISSCC, pp.382-383, Feb.2014.