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Problem with SepctreHDL and ahdl.def

riccart *over 10 years ago*

Hi everyone,

Does anyone can help me to fix this problem.

I am trying to simulate my A2D and I am using the verilog file ''dac_10bit_ideal'' and ''sah_ideal'' from library ''ahdlLib'', but I have this Error.

FATAL (VACOMP-2095): File 'ahdl.def' does not appear to be a valid
Verilog-A file. In previous releases, 'ahdl.def' was a typical file name
for the SpectreHDL view of a component in the Virtuoso Analog Design Environment
but the software no longer supports SpectreHDL.
Thanks for your help !!

Offline Andrew Beckett *over 10 years ago*

SpectreHDL has been obsolete for many years now, and eventually MMSIM dropped support for altogether (to avoid having to maintain the obsolete code).

Use the veriloga views in ahdlLib instead of the ahdl views. That will work - and will have worked for many, many, years.

Regards,

Andrew.

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riccart *over 10 years ago*

Thanks, but could you please explain me more.

First of all, in attachment, you will see the set up of my design.
I am using the symbol for bloc dac_10bit_ideal and sah_ideal. Of course, I took it from Library ahdlLib.
In your response, you said that I have to use veriloga views instead of the views. But when I get a symbol, How can I know if this

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Here is the ahdl code for a sample and hold.

```
// $Date: 1995/08/12 01:54:14 $
// $Revision: 1.8 $
```

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```
//
// The sample SpectreHDL library is unsupported and subject to change
// without notice. Future versions of SpectreHDL may not be compatible
// with this library.

//------------------------------------------
// sah_ideal
//
//- ideal sample and hold amplifier
//
// vin:      [V,A]
// vclk:    [V,A]
// vout:    [V,A]
//
// INSTANCE parameters
//    vtrans_clk = transition voltage of the clock [V]
//
// MODEL parameters
// (none)

module sah_ideal(vin, vout, vclk) (vtrans_clk)
node [V,I] vin, vout, vclk;
parameter real vtrans_clk=2.5;
{
real vout_val = 0 ;

    analog{
        if ($threshold(V(vclk) - vtrans_clk, 1.0))
            vout_val = V(vin) ;
            V(vout) <- vout_val ;
            }
}
```

Here is the veriloga for a sample and Hold

```
include "discipline.h"
include "constants.h"

// $Date: 1997/08/28 05:54:39 $
// $Revision: 1.1 $
//
//.
// Based on the OVI Verilog-A Language Reference Manuel, version 1.0 1996
//
//
```

```
//------------------------------------------
// sah_ideal
//
//- ideal sample and hold amplifier
//
// vin:      [V,A]
// vclk:   [V,A]
// vout:    [V,A]
//
// INSTANCE parameters
//    vtrans_clk = transition voltage of the clock [V]
//
// MODEL parameters
// (none)

module sah_ideal(vin, vout, vclk);
input vin,vclk;
output vout;
electrical vin, vout, vclk;
parameter real vtrans_clk=2.5;
real vout_val;

   analog begin
      @ (cross(V(vclk) - vtrans_clk, 1.0))
         vout_val = V(vin) ;
         V(vout) <+ vout_val ;
   end

endmodule
```

Both come from ahdlLib.

P.S. I'm a new on Cadence.

Thanks again.

Offline Andrew Beckett   *over 10 years ago*

It sounds as if you could do with some basic training, or at least read some of the documentation.

Each cell has (potentially) multiple views. For example, a cell might have a symbol, a schematic, a veriloga, an ahdl view, a layout view, etc, etc. When you netlist for simulation, it needs to pick a
particular view to simulate from each cell it finds in your design hierarchy. It's not a matter of the
symbol being generated by the veriloga or ahdl view.

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Netlisters in the Cadence IC tools work by a concept called "view switching". When it finds an instance of a symbol in your design, it will then descend the hierarchy by switching into another view alongside the symbol. In a pure schematic based design, this is controlled in ADE by the Switch List and Stop List on the Setup->Environment form in the Analog Design Environment. This might be something like:

Switch View List: spectre cmos_sch cmos.sch schematic veriloga
Stop View List: spectre

The idea is that it tries each of the views in the switch list in turn, and if that view exists for a particular cell, it will switch into it and use it. Having switched into it, it then checks to see if that view was in the stop list, in which case it stops expanding the hierarchy during netlisting.

Maybe you have "ahdl" in your switch view list, and have it listed before veriloga? If you remove ahdl (and ensure that veriloga is there), or even just put veriloga before ahdl, it would pick up the veriloga view in preference to the ahdl view for simulation.

If instead of a simple schematic based design, you're using the hierarchy editor to create a config view, and are then simulating with that, you have finer control over which views are picked for which blocks. However, I doubt you can be doing that, because otherwise I would have been very surprised that you would have asked this question - you can't really use the hierarchy editor unless you understand the basics of simulating with different views.

Regards,

Andrew.

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