PROCESS	DRM REVISION	DK REVISION	ELDO VERSION
DIGITAL CMOS065	D	4.2.1	AMS 2005.2.p0274

✓ Maturity Definition

Maturity	Definition	Model revision format
Tentative (mat 5)	Prediction models based on early silicon results, TCAD simulation and previous technology models	0.0x
Preliminary (mat 10)	Based silicon model representative of mat 10 technology	0.x
Pre-production (mat 20)	Based silicon model representative of mat 20 technology	1.x
Production (mat 30)	Based silicon model representative of mat 30 technology	2.x

✓ Common Files

Common Files	Revision	Previous revision in DK4.2
common_active_cd.lib	0.1	0.1
common_active_res.lib	0.1	0.1
common_poly_cd.lib	0.2	0.2
common_poly_res.lib	0.2	0.2
common_go1.lib	0.1	0.1
common_go2.lib	0.1	0.1
common_be.lib	0.1	0.1
common_well.lib	0.1	0.1

✓ GP SVT MOS Transistors

DEVICES	DEVICE NAME IN OPUS	MODEL or SUBCKT NAME IN MODEL LIBRARIES	STANDARD MODEL CODE VERSION	COMMENTS	MODEL REVISION	MODEL FEATURES									Previous model revision in DK4.2	CHANGES VERSUS LAST DK DK4.2	DOCUMENTATIONS	LAST UPDATE
						Ipe	Well-proximity effect	pre-defined corners	User-corners	Statistical models (Global variation)	Mismatch (local varaition)	SOA	HCI	NBTI				
NMOS SVT	nsvtgp	nsvtgp	BSIM4.4	.subckt MOS Model	0.12_st1	√		√	√	√	√	√		--	0.11.a_st1	ngcon activated	GPmos_bsim4_svt.pdf RPO.pdf Mechanical_Stress.pdf GuidelinesDK_NBTI_HCI.pdf mismatch.pdf parasitic_capacitances.pdf flag_settings.pdf UserCorner_model.pdf	06/2006
	nsvtgprpo	nsvtgprpo		MOS unsilicided: .subckt MOS Model + Rgate+ External S/D resistances														
PMOS SVT	psvtgp	psvtgp		.subckt MOS Model										0.1				
	psvtgprpo	psvtgprpo		MOS unsilicided: .subckt MOS Model + Rgate+ External S/D resistances														

✓ GP HVT MOS Transistors

DEVICES	DEVICE NAME IN OPUS	MODEL or SUBCKT NAME IN MODEL LIBRARIES	STANDARD MODEL CODE VERSION	COMMENTS	MODEL REVISION	MODEL FEATURES									Previous model revision in DK4.2	CHANGES VERSUS LAST DK DK4.2	DOCUMENTATIONS	LAST UPDATE
						Ipe	Well-proximity effect	pre-defined corners	User-corners	Statistical models (Global variation)	Mismatch (local varaition)	SOA	HCI	NBTI				
NMOS HVT	nhvtgp	nhvtgp	BSIM4.4	.subckt MOS Model	0.12_st1	√		√	√	√	√	√		-	0.11.a_st1	bugfix on STI stress model + ngcon activated	GPmos_bsim4_hvt.pdf RPO.pdf Mechanical_Stress.pdf GuidelinesDK_NBTI_HCI.pdf mismatch.pdf parasitic_capacitances.pdf flag_settings.pdf UserCorner_model.pdf	06/2006
	nhvtgprpo	nhvtgprpo		MOS unsilicided: .subckt MOS Model + Rgate+ External S/D resistances														
PMOS HVT	phvtgp	phvtgp		.subckt MOS Model										0.1				
	phvtgprpo	phvtgprpo		MOS unsilicided: .subckt MOS Model + Rgate+ External S/D resistances														

✓ GP HVT MOS Transistors for Double Port SRAM cell

DEVICES	DEVICE NAME IN OPUS	MODEL or SUBCKT NAME IN MODEL LIBRARIES	STANDARD MODEL CODE VERSION	COMMENTS	MODEL REVISION	MODEL FEATURES									Previous model revision in DK4.2	CHANGES VERSUS LAST DK DK4.2	DOCUMENTATIONS	LAST UPDATE
						lpe	Well-proximity effect	pre-defined corners	User-corners	Statistical models (Global variation)	Mismatch (local varaition)	SOA	HCI	NBTI				
NMOS HVT PULL-DOWN	nhvtgppddp	nhvtgppddp	BSIM4.4	.subckt MOS Model	0.06.a_st1	√		√	√	√	√			-	0.06.a_st1	no change	Mechanical_Stress.pdf mismatch.pdf parasitic_capacitances.pdf fllag_settings.pdf UserCorner_model.pdf	05/2006
NMOS HVT PASS_GATE	nhvtgppgdp	nhvtgppgdp																
PMOS HVT PULL-UP	phvtgppudp	phvtgppudp												0.1				

✓ GP HVT MOS Transistors for Single Port SRAM cell (0.620 um^2)

DEVICES	DEVICE NAME IN OPUS	MODEL or SUBCKT NAME IN MODEL LIBRARIES	STANDARD MODEL CODE VERSION	COMMENTS	MODEL REVISION	MODEL FEATURES									Previous model revision in DK4.2	CHANGES VERSUS LAST DK DK4.2	DOCUMENTATIONS	LAST UPDATE
						Ipe	Well-proximity effect	pre-defined corners	User-corners	Statistical models (Global variation)	Mismatch (local varaition)	SOA	HCI	NBTI				
NMOS HVT PULL-DOWN	nhvtgppdsp620	nhvtgppdsp620	BSIM4.4	.subckt MOS Model	0.06.a_st1	√		√	√	√	√			-	0.06.a_st1	no change	Mechanical_Stress.pdf mismatch.pdf parasitic_capacitances.pdf fllag_settings.pdf UserCorner_model.pdf	05/2006
NMOS HVT PASS_GATE	nhvtgppgsp620	nhvtgppgsp620																
PMOS HVT PULL-UP	phvtgppusp620	phvtgppusp620												0.1				

✓ LP HPA MOS TransistorsGP HVT MOS Transistors

DEVICES	DEVICE NAME IN OPUS	MODEL or SUBCKT NAME IN MODEL LIBRARIES	STANDARD MODEL CODE VERSION	COMMENTS	MODEL REVISION	MODEL FEATURES									Previous model revision in DK4.2	CHANGES VERSUS LAST DK DK4.2	DOCUMENTATIONS	LAST UPDATE
						Ipe	Well-proximity effect	pre-defined corners	User-corners	Statistical models (Global variation)	Mismatch (local varaition)	SOA	HCI	NBTI				
NMOS HPA	nhpap	nhpalp	BSIM4.4	.subckt MOS Model	0.1.a	√		√	√	√	√	√		-	0.1.a	no change	LPmos_bsim4_hpa.pdf Mechanical_Stress.pdf GuidelinesDK_NBTI_HCI.pdf mismatch.pdf parasitic_capacitances.pdf flag_settings.pdf UserCorner_model.pdf	05/2006
PMOS HPA	phpalp	phpalp		.subckt MOS Model														

✓ LP LVT MOS Transistors

DEVICES	DEVICE NAME IN OPUS	MODEL or SUBCKT NAME IN MODEL LIBRARIES	STANDARD MODEL CODE VERSION	COMMENTS	MODEL REVISION	MODEL FEATURES									Previous model revision in DK4.2	CHANGES VERSUS LAST DK DK4.2	DOCUMENTATIONS	LAST UPDATE
						Ipe	Well-proximity effect	pre-defined corners	User-corners	Statistical models (Global variation)	Mismatch (local varaition)	SOA	HCI	NBTI				
NMOS LVT	nlvtlp	nlvtlp	BSIM4.4	.subckt MOS Model	0.9.d_st1	√		√	√	√	√	√		-	0.9.d_st1	no change	LPmos_bsim4_lvt.pdf Mechanical_Stress.pdf GuidelinesDK_NBTI_HCI.pdf mismatch.pdf parasitic_capacitances.pdf flag_settings.pdf UserCorner_model.pdf	05/2006
PMOS LVT	plvtlp	plvtlp		.subckt MOS Model										0.1				

✓ LP SVT MOS Transistors

DEVICES	DEVICE NAME IN OPUS	MODEL or SUBCKT NAME IN MODEL LIBRARIES	STANDARD MODEL CODE VERSION	COMMENTS	MODEL REVISION	MODEL FEATURES									Previous model revision in DK4.2	CHANGES VERSUS LAST DK DK4.2	DOCUMENTATIONS	LAST UPDATE
						Ipe	Well-proximity effect	pre-defined corners	User-corners	Statistical models (Global variation)	Mismatch (local varaition)	SOA	HCI	NBTI				
NMOS SVT	nsvtlp	nsvtlp	BSIM4.4	.subckt MOS Model	1.1.d_st1	√		√	√	√	√	√		-	1.1.d_st1	no change	LPmos_bsim4_svt.pdf RPO.pdf Mechanical_Stress.pdf GuidelinesDK_NBTI_HCI.pdf mismatch.pdf parasitic_capacitances.pdf flag_settings.pdf UserCorner_model.pdf	05/2006
	nsvtlprpo	nsvtlprpo		MOS unsilicided: .subckt MOS Model + Rgate+ External S/D resistances														
PMOS SVT	psvtlp	psvtlp		.subckt MOS Model										0.1				
	psvtlprpo	psvtlprpo		MOS unsilicided: .subckt MOS Model + Rgate+ External S/D resistances														

✓ LP HVT MOS Transistors

DEVICES	DEVICE NAME IN OPUS	MODEL or SUBCKT NAME IN MODEL LIBRARIES	STANDARD MODEL CODE VERSION	COMMENTS	MODEL REVISION	MODEL FEATURES									Previous model revision in DK4.2	CHANGES VERSUS LAST DK DK4.2	DOCUMENTATIONS	LAST UPDATE
						Ipe	Well-proximity effect	pre-defined corners	User-corners	Statistical models (Global variation)	Mismatch (local varaition)	SOA	HCI	NBTI				
NMOS HVT	nhvtlp	nhvtlp	BSIM4.4	.subckt MOS Model	1.1.d_st1	√		√	√	√	√	√		-	1.1.d_st1	no change	LPmos_bsim4_svt.pdf RPO.pdf Mechanical_Stress.pdf GuidelinesDK_NBTI_HCI.pdf mismatch.pdf parasitic_capacitances.pdf flag_settings.pdf UserCorner_model.pdf	05/2006
	nhvtlprpo	nhvtlprpo		MOS unsilicided: .subckt MOS Model + Rgate+ External S/D resistances														
PMOS HVT	phvtlp	phvtlp		.subckt MOS Model										0.1				
	phvtlprpo	phvtlprpo		MOS unsilicided: .subckt MOS Model + Rgate+ External S/D resistances														

✓ LP SVT and HVT MOS Transistors for Single Port SRAM cell (0.525 um^2)

DEVICES	DEVICE NAME IN OPUS	MODEL or SUBCKT NAME IN MODEL LIBRARIES	STANDARD MODEL CODE VERSION	COMMENTS	MODEL REVISION	MODEL FEATURES									Previous model revision in DK4.2	CHANGES VERSUS LAST DK DK4.2	DOCUMENTATIONS	LAST UPDATE
						lpe	Well-proximity effect	pre-defined corners	User-corners	Statistical models (Global variation)	Mismatch (local varaition)	SOA	HCI	NBTI				
NMOS SVT PULL-DOWN	nsvtlppdsp	nsvtlppdsp	BSIM4.4	.subckt MOS Model	0.22_st1	√		√	√	√	√			--	0.21.a_st1	rrecentering (VTH+matching)	Mechanical_Stress.pdf mismatch.pdf parasitic_capacitances.pdf fllag_settings.pdf UserCorner_model.pdf	06/2006
NMOS SVT PASS_GATE	nsvtlppgsp	nsvtlppgsp																
PMOS SVT PULL-UP	psvtlppusp	psvtlppusp												0.1				
NMOS HVT PULL-DOWN	nhvtlppdsp	nhvtlppdsp												-				
NMOS HVT PASS_GATE	nhvtlppgsp	nhvtlppgsp																
PMOS HVT PULL-UP	phvtlppusp	phvtlppusp												0.1				

✓ LP SVT and HVT MOS Transistors for Single Port SRAM cell (0.620 um^2)

DEVICES	DEVICE NAME IN OPUS	MODEL or SUBCKT NAME IN MODEL LIBRARIES	STANDARD MODEL CODE VERSION	COMMENTS	MODEL REVISION	MODEL FEATURES									Previous model revision in DK4.2	CHANGES VERSUS LAST DK DK4.2	DOCUMENTATIONS	LAST UPDATE
						lpe	Well-proximity effect	pre-defined corners	User-corners	Statistical models (Global variation)	Mismatch (local varaition)	SOA	HCI	NBTI				
NMOS SVT PULL-DOWN	nsvtlppdsp620	nsvtlppdsp620	BSIM4.4	.subckt MOS Model	0.22_st1	√		√	√	√	√			--	0.21.a_st1	recentering (VTH+matching)	Mechanical_Stress.pdf mismatch.pdf parasitic_capacitances.pdf fllag_settings.pdf UserCorner_model.pdf	06/2006
NMOS SVT PASS_GATE	nsvtlppgsp620	nsvtlppgsp620																
PMOS SVT PULL-UP	psvtlppusp620	psvtlppusp620												0.1				
NMOS HVT PULL-DOWN	nhvtlppdsp620	nhvtlppdsp620												-				
NMOS HVT PASS_GATE	nhvtlppgsp620	nhvtlppgsp620																
PMOS HVT PULL-UP	phvtlppusp620	phvtlppusp620												0.1				

✓ LP SVT and HVT MOS Transistors for Double Port SRAM cell (0.97um^2)

DEVICES	DEVICE NAME IN OPUS	MODEL or SUBCKT NAME IN MODEL LIBRARIES	STANDARD MODEL CODE VERSION	COMMENTS	MODEL REVISION	MODEL FEATURES									Previous model revision in DK4.2	CHANGES VERSUS LAST DK DK4.2	DOCUMENTATIONS	LAST UPDATE
						lpe	Well-proximity effect	pre-defined corners	User-corners	Statistical models (Global variation)	Mismatch (local varaition)	SOA	HCI	NBTI				
NMOS SVT PULL-DOWN	nsvtlppddp	nsvtlppddp	BSIM4.4	.subckt MOS Model	0.22_st1	√		√	√	√	√			--	0.21.a_st1	recentering (VTH+matching)	Mechanical_Stress.pdf mismatch.pdf parasitic_capacitances.pdf fllag_settings.pdf UserCorner_model.pdf	06/2006
NMOS SVT PASS_GATE	nsvtlppgdp	nsvtlppgdp																
PMOS SVT PULL-UP	psvtlppudp	psvtlppudp												0.1				
NMOS HVT PULL-DOWN	nhvtlppddp	nhvtlppddp												-				
NMOS HVT PASS_GATE	nhvtlppgdp	nhvtlppgdp																
PMOS HVT PULL-UP	phvtlppudp	phvtlppudp												0.1				

✓ Double Gate Oxide (50 Angst.) MOS Transistors

DEVICES	DEVICE NAME IN OPUS	MODEL or SUBCKT NAME IN MODEL LIBRARIES	STANDARD MODEL CODE VERSION	COMMENTS	MODEL REVISION	MODEL FEATURES									Previous model revision in DK4.2	CHANGES VERSUS LAST DK DK4.2	DOCUMENTATIONS	LAST UPDATE
						Ipe	Well-proximity effect	pre-defined corners	User-corners	Statistical models (Global variation)	Mismatch (local varaition)	SOA	HCI	NBTI				
NMOS SVT 2V5	nsvt25	nsvt25	BSIM4.4	.SUBCKT MOS Model with Juncap model for S/D junction diodes	0.1.f_st1	√		√	√	√	√	√		-	0.1.f_st1	no change	mos_bsim4_svt25.pdf RPO.pdf Mechanical_Stress.pdf GuidelinesDK_NBTI_HCI.pdf mismatch.pdf parasitic_capacitances.pdf flag_settings.pdf UserCorner_model.pdf	05/2006
	nsvt25rpo	nsvt25rpo		MOS unsilicided: .standard model + Rgate+ External S/D resistances														
	nsvt25rpo noldd	nsvt25rponoldd		MOS no-ldd unsilicided: .subckt MOS Model + Rgate+ External S/D resistances														
PMOS SVT 2V5	psvt25	psvt25		.subckt MOS Model with Juncap model for S/D junction diodes										0.1				
	psvt25rpo	psvt25rpo		MOS unsilicided: standard model + Rgate+ External S/D resistances														

✓ Double Gate Oxide (50 Angst.) DriftMOS Transistors

DEVICES	DEVICE NAME IN OPUS	MODEL or SUBCKT NAME IN MODEL LIBRARIES	STANDARD MODEL CODE VERSION	COMMENTS	MODEL REVISION	MODEL FEATURES									Previous model revision in DK4.2	CHANGES VERSUS LAST DK DK4.2	DOCUMENTATIONS	LAST UPDATE
						Ipe	Well-proximity effect	pre-defined corners	User-corners	Statistical models (Global variation)	Mismatch (local varaition)	SOA	HCI	NBTI				
NDRMOS2V5	ndr25	ndr25	BSIM3 Version 3.24 + ST solution	.subckt MOS Model + juncap diode models + specific CGD capa	0.02.a_st2			√	√	√	√	√		-	0.02.a_st2	no change	mos_bsim3_dr25.pdf UserCorner_model.pdf	06/03/06
		ndr25_leak	BSIM3 Version 3.24 + ST solution	.subckt MOS Model + juncap diode models + specific CGD capa														
NDRMOS2V5 for OTP	ndr25otp	ndr25otp	BSIM4.4+ ST solution	.subckt MOS Model + juncap diode models + specific CGD capa	0.1.c_st1			√	√	√	√				0.1.c_st1		mismatch.pdf + flag_setting UserCorner_model.pdf	04/06
PDRMOS2V5	pdr25	pdr25	BSIM3 Version 3.24 + ST solution	.subckt MOS Model + juncap diode models + specific CGD capa	0.02.a_st2							√		0.1	0.02.a_st2		mos_bsim3_dr25.pdf UserCorner_model.pdf	06/03/06
		pdr25_leak	BSIM3 Version 3.24 + ST solution	.subckt MOS Model + juncap diode models + specific CGD capa														

✓ Double Gate Oxide (50 Angst.) transistors for DRAM applications

DEVICES	DEVICE NAME IN OPUS	MODEL or SUBCKT NAME IN MODEL LIBRARIES	STANDARD MODEL CODE VERSION	COMMENTS	MODEL REVISION	MODEL FEATURES									Previous model revision in DK4.2	CHANGES VERSUS LAST DK DK4.2	DOCUMENTATIONS	LAST UPDATE
						Ipe	Well-proximity effect	pre-defined corners	User-corners	Statistical models (Global variation)	Mismatch (local varaition)	SOA	HCI	NBTI				
NMOS SVT-DRAM 2V5	nsvt25dram	nsvt25dram	BSIM4.2.1	.subckt MOS Model + Juncap model for S/D junction diodes + specific CGD capa	0.01.j			√	√	√	√			-	0.01.j	no change	mismatch.pdf + flag_setting UserCorner_model.pdf	05/06

✓ Double Gate Oxide (28 Angst.) MOS Transistors

DEVICES	DEVICE NAME IN OPUS	MODEL or SUBCKT NAME IN MODEL LIBRARIES	STANDARD MODEL CODE VERSION	COMMENTS	MODEL REVISION	MODEL FEATURES									Previous model revision in DK4.2	CHANGES VERSUS LAST DK DK4.2	DOCUMENTATIONS	LAST UPDATE
						Ipe	Well-proximity effect	pre-defined corners	User-corners	Statistical models (Global variation)	Mismatch (local varaition)	SOA	HCI	NBTI				
NMOS SVT 1V8	nsvt18	nsvt18	BSIM4.2.1	.subckt MOS Modell with Juncap model for S/D junction diodes	0.03.f_st1	√		√	√	√	√	√		-	0.03.f_st1	no change	mos_bsim4_svt18.pdf RPO.pdf Mechanical_Stress.pdf GuidelinesDK_NBTI_HCI.pdf mismatch.pdf parasitic_capacitances.pdf flag_settings.pdf UserCorner_model.pdf	05/2006
	nsvt18rpo	nsvt18rpo		MOS unsilicided: standard model + Rgate+ External S/D resistances														
	nsvt18rpo noldd	nsvt18rponoldd		MOS no-ldd unsilicided: ..subckt MOS Model with Juncap model + Rgate+ External S/D resistances														
PMOS SVT 1V8	psvt18	psvt18		.subckt MOS Model with Juncap model for S/D junction diodes														
	psvt18rpo	psvt18rpo		MOS unsilicided: standard model + Rgate+ External S/D resistances														

✓ Double Gate Oxide (28 Angst.) DriftMOS Transistors

DEVICES	DEVICE NAME IN OPUS	MODEL or SUBCKT NAME IN MODEL LIBRARIES	STANDARD MODEL CODE VERSION	COMMENTS	MODEL REVISION	MODEL FEATURES									Previous model revision in DK4.2	CHANGES VERSUS LAST DK DK4.2	DOCUMENTATIONS	LAST UPDATE
						Ipe	Well-proximity effect	pre-defined corners	User-corners	Statistical models (Global variation)	Mismatch (local varaition)	SOA	HCI	NBTI				
NDRMOS 1V8 for OTP	ndr18otp	ndr18otp	BSIM4.2.1+ ST solution	.subckt MOS Model + juncap diode models + specific CGD capa	0.01.b_st1			√	√	√	√			-	0.01.b_st1	no change	mismatch.pdf + flag_setting + UserCorner_model.pdf	05/06

✓ Diodes for thin Oxide MOS transistors

DEVICES	DEVICE NAME IN OPUS	MODEL or SUBCKT NAME IN MODEL LIBRARIES	STANDARD MODEL CODE VERSION	COMMENTS	MODEL REVISION	LPE	PRE-DEFINED CORNER MODELS	STATISTIC MODELS		Previous model revision in DK4.2	CHANGES VERSUS LAST DK4.2	DOCUMENTATIONS	LAST UPDATE
								PROCESS VARIATION (global variation)	MATCHING (local variation)				
GP SVT N+ / Pwell	dnsvtgp	dnsvtgp	juncap	Junction diode for thin Oxide MOS transistor	0.03		√			0.03	no change		09/2004
GP SVT P+ / Nwell	dpsvtgp	dpsvtgp											
GP HVT N+ / Pwell	dnhvtgp	dnhvtgp											
GP HVT P+ / Nwell	dphvtgp	dphvtgp											
LP LVT N+ / Pwell	dnlvtlp	dnlvtlp											
LP LVT P+ / Nwell	dplvtlp	dplvtlp											
LP SVT N+ / Pwell	dnsvtlp	dnsvtlp											
LP SVT P+ / Nwell	dpsvtlp	dpsvtlp											
LP HVT N+ / Pwell	dnhvtlp	dnhvtlp											
LP HVT P+ / Nwell	dphvtlp	dphvtlp											
Nwell / Psub	dnwps	dnwps			0.03a					0.03a			10/05/05
Pwell / Niso	ddnwpw	ddnwpw											
Niso / Psub	ddnwps	ddnwps			0.03					0.03			09/2004

✓ Diodes for double gate Oxide MOS transistors

DEVICES	DEVICE NAME IN OPUS	MODEL or SUBCKT NAME IN MODEL LIBRARIES	STANDARD MODEL CODE VERSION	COMMENTS	MODEL REVISION	LPE	PRE-DEFINED CORNER MODELS	STATISTIC MODELS		Previous model revision in DK4.2	CHANGES VERSUS LAST DK4.2	DOCUMENTATIONS	LAST UPDATE
								PROCESS VARIATION (global variation)	MATCHING (local variation)				
SVT25 N+ / Pwell	dnsvt25	dnsvt25	juncap	Junction diode for double gate Oxide (50 Angst.) MOS transistor	0.03		√			0.03	no change		10/05/05
SVT25 P+ / Nwell	dpsvt25	dpsvt25											
SVT18 N+ / Pwell	dnsvt18	dnsvt18		Junction diode for double gate Oxide (28 Angst.) MOS transistor	0.01					0.01			06/03/2006
SVT18 P+ / Nwell	dpsvt18	dpsvt18											

✓ 2V5 and 1V8 Gated-Diodes

DEVICES	DEVICE NAME IN OPUS	MODEL or SUBCKT NAME IN MODEL LIBRARIES	STANDARD MODEL CODE VERSION	COMMENTS	MODEL REVISION	LPE	PRE-DEFINED CORNER MODELS	STATISTIC MODELS		Previous model revision in DK4.2	CHANGES VERSUS LAST DK4.2	DOCUMENTATIONS	LAST UPDATE
								PROCESS VARIATION (global variation)	MATCHING (local variation)				
N+ / Pwell 2V5 - 5.0 nm	dgnsvt25	dgnsvt25	BSIM4.4 + juncap	Gated diode for I/O application	0.04.b	√	√	√		0.04.b	no change		05/2006
P+ / Nwell 2V5 - 5.0 nm	dgpsvt25	dgpsvt25											
N+ / Pwell 1V8- 2.8 nm	dgnsvt18	dgnsvt18	BSIM4.2.1 + juncap	Gated diode for I/O application	0.02.g					0.02.g	no change		05/2006
P+ / Nwell 1V8 - 2.8 nm	dgpsvt18	dgpsvt18											

✓ Bipolar Transistors

DEVICES	DEVICE NAME IN OPUS	MODEL or SUBCKT NAME IN MODEL LIBRARIES	STANDARD MODEL CODE VERSION	COMMENTS	MODEL REVISION	DATA MATURITY	CORNER MODELS	STATISTIC MODELS		SOA LIMITS	Previous model revision in DK4.2	CHANGES VERSUS LAST DK4.2	DOCUMENTATIONS	LAST UPDATE
								PROCESS VARIATION	MATCHING					
N+ / Pwell / Niso bipolar - (E:5x5)	npniso25	npniso25	ST_compact	Band-Gap applications M1 : compact model	0.11	Preliminary	yes	no	no	no	**0.1**	tnom specified in model card		24/08/2005 (Q513RDZ)
P+ / Nwell / Psub vertical bipolar (E:5x5)	pnps25	pnps25		Band-Gap applications M1 : compact model										
N+ / Pwell / Niso bipolar - (E:2x2)	npniso4	npniso4		Band-Gap applications M1 : compact model										
P+ / Nwell / Psub vertical bipolar (E:2x2)	pnps4	pnps4		Band-Gap applications M1 : compact model										

✓ Resistors

DEVICES	DEVICE NAME IN OPUS	MODEL or SUBCKT NAME IN MODEL LIBRARIES	STANDARD MODEL CODE VERSION	COMMENTS	MODEL REVISION	CORNER MODELS	STATISTIC MODELS		SOA	Previous model revision in DK4.1.2	CHANGES VERSUS LAST DK 4.1.2	DOCUMENTATIONS	LAST UPDATE
							PROCESS VARIATION	MATCHING					
N+ Poly silicided resistor	rnpo	rnpo		Silicide N+ Poly Resistor + flicker noise (ANALOG)	0.2	yes	yes	yes	no	0.2	no change	resistor_model.pdf	05/05/06
		rnpo_acc		Silicide N+ Poly Resistor including flicker noise (ANALOG) + no-linearities									
P+ OD non-silicided resistor	rpodrpo	rpodrpo		Unsilicided P+ Active Resistor + flicker noise (ANALOG)	0.2					0.2	no change		
		rpodrpo_acc		Unsilicided P+ Active Resistor including flicker noise (ANALOG) + no-linearities									
P+ Poly non-silicided resistor	rpporpo	rpporpo		Unsilicided P+ Poly Resistor + flicker noise (ANALOG)	0.2					0.2	no change		
		rpporpo_acc		Unsilicided P+ Poly Resistor including flicker noise (ANALOG) + no-linearities									
N+ Poly non-silicided resistor	rnporpo	rnporpo		Unsilicided N+ Poly Resistor + flicker noise (ANALOG)	0.2					0.2	no change		
		rnporpo_acc		Unsilicided N+ Poly Resistor including flicker noise (ANALOG) + no-linearities									
HIPO resistor (High Resistive Poly)	rhiporpo	rhiporpo		Hipo Resistor + flicker noise (ANALOG)	0.02					0.02	no change		
		rhiporpo_acc		Hipo Resistor including flicker noise (ANALOG) + no-linearities									
M1 resistor	rm1	rm1		Metal 1 Resistor + Temperature no-linearity Effect	0.06			no		0.06	no change		05/05/06
Mx resistor	rmx	rmx		Metal x Resistor + Temperature no-linearity Effect									
Mz resistor	rmz	rmz		Metal z Resistor + Temperature no-linearity Effect									
AP resistor	rap	rap		Alucap Resistor + Temperature no-linearity Effect									
N+ Poly resistor	rnpoi	rnpoi		N+ poly silicided intrinsic resistor	0.05					0.05	no change		05/05/06
P+ Poly resistor	rppoi	rppoi		P+ poly silicided intrinsic resistor									

✓ Poly Capacitors

DEVICES	DEVICE NAME IN OPUS	MODEL or SUBCKT NAME IN MODEL LIBRARIES	STANDARD MODEL CODE VERSION	COMMENTS	MODEL REVISION	CORNER MODELS	STATISTIC MODELS		SOA LIMITS	Previous model revision in DK4.1.2	CHANGES VERSUS LAST DK 4.1.2	DOCUMENTATIONS	LAST UPDATE
							PROCESS VARIATION	MATCHING					
N+ Poly / 50A Gox / Nwell	cpo25nw	cpo25nw	--		0.12.c	yes	yes	no	no	0.12.b	no change on simulation	cpoly25_silicon_st.pdf	06/06
P+ Poly / 50A Gox / Pwell	cpo25pw	cpo25pw											
N+ Poly / 28A Gox / Nwell	cpo18nw	cpo18nw			0.01.a	yes	yes	no	no	0.01	no change on simulation		06/06
N+ Poly / 21A Gox / Nwell	cpolpnw	cpolpnw		mm11 based model	0.12	yes	yes	no	no	0.11	improvement on derivative		-06/06
P+ Poly / 21A Gox / Pwell	cpolppw	cpolppw		mm11 based model		yes	yes	no	no				

✓ Strip Capacitors

DEVICES	DEVICE NAME IN OPUS	MODEL or SUBCKT NAME IN MODEL LIBRARIES	STANDARD MODEL CODE VERSION	COMMENTS	MODEL REVISION	CORNER MODELS	STATISTIC MODELS		SOA LIMITS	Previous model revision in DK4.1.2	CHANGES VERSUS LAST DK 4.1.2	DOCUMENTATIONS	LAST UPDATE
							PROCESS VARIATION	MATCHING					
strip capacitor	cmstrstk	cmstrstk	--	Strip Stacked Metal Capacitor (M1 to M5 stacked)	0.03	yes	yes	yes	no	0.03	no change	cstrip_model.pdf	03/01/06

✓ Fringe Capacitors

DEVICES	DEVICE NAME IN OPUS	MODEL or SUBCKT NAME IN MODEL LIBRARIES	STD. MODEL CODE VERSION	COMMENTS	MODEL REVISION	CORNER MODELS	STATISTIC MODELS		SOA LIMITS	Previous model revision in DK4.1.2	CHANGES VERSUS LAST DK 4.1.2	DOCUMENTATIONS	LAST UPDATE
							PROCESS VARIATION	MATCHING					
M1-M5 Fringe capacitor for ShZ option technology (FMOM)	cfrm1m5shz	cfrm1m5shz		Model containing intrinsic and parasitic capa. and isolated diode	0.1_st1	yes	yes	yes	no	0.1_st1	-no change	cfrringe_model.pdf	03/01/06
		cfrm1m5shz_acc		Complete model with intrinsic and parasitic capa. and RS									
M1-M5 Fringe capacitor for ShZ option technology- **without substrate pin**	cfrm1m5shznosub	cfrm1m5shznosub		Model containing intrinsic and parasitic capa. and isolated diode									
		cfrm1m5shznosub_acc		Complete model with intrinsic and parasitic capa. and RS									
M1 Fringe capacitor	cfrm1	cfrm1		Ideal fringe capa for Metal 1	0.02	no	no	no		0.02	no change	-	01/03/05
Mx Fringe capacitor	cfrmx	cfrmx		Ideal fringe capa for Metal x									
Mz Fringe capacitor	cfrmz	cfrz		Ideal fringe capa for Metal z									

✓ Plate Capacitors

DEVICES	DEVICE NAME IN OPUS	MODEL or SUBCKT NAME IN MODEL LIBRARIES	STANDARD MODEL CODE VERSION	COMMENTS	MODEL REVISION	CORNER MODELS	STATISTIC MODELS		SOA LIMITS	Previous model revision in DK4.1.2	CHANGES VERSUS LAST DK 4.1.2	DOCUMENTATIONS	LAST UPDATE
							PROCESS VARIATION	MATCHING					
M1/Mx Plate Capacitor	cm1mx	cm1mx	-	Metal1/Metalx Plate Capacitor	0.03	yes	yes	yes	no	0.03	no change	cplate_model.pdf	03/01/06
Mx/Mx Plate Capacitor	cmxmx	cmxmx		Metalx/Metalx Plate Capacitor									
Mx/Mz Plate Capacitor	cmxmz	cmxmz		Metalx/Metalz Plate Capacitor									
Mz/Mz Plate Capacitor	cmzmz	cmzmz		Metalz/Metalz Plate Capacitor									

