Parasitic Capacitance Modeling description

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Goals

• A new methodology has been developed to take into account parasitic capacitance contributions such as poly-contact coupling and corner capacitances which can not be neglected since cmos090 technology.

• These parasitic capacitance contributions depend strongly on the layout. Therefore, it is desirable to extract these contributions with a LPE tool. At the same time, these contributions are important in pre-layout simulations, and have to be included in Spice models.

• To avoid double counting, LPE-flags were introduced. Depending on the LPE extraction option chosen by the designer, components which are extracted by the LPE tool are automatically desactivated in the Spice model through LPE-flags.

• To validate the new methodology, cmos065 LP Silicon was used as an example. The new methodology will be applied to all technologies from cmos065 onward.

LPE Flag included in SPICE models: Convention

1. Pre-layout simulations: lpe flag set to "0"
   * No capacitances and no resistances extraction with LPE tool,
   * Parasitic capacitances in SPICE models,
   * Contact resistances of Source/Drain in SPICE models.

2. Post-layout simulations using "C + VIACAP=YES" option in StarRCXT: lpe flag set to "1"
   * No resistances extraction with LPE tool,
   * C3ext, C5, C6, C7m, C7c parasitic capacitances (please see slide 7) extraction with LPE tool,
   * Remaining parasitic capacitances in SPICE models,
   * Contact resistances of Source/Drain in SPICE models.

3. Post-layout simulations using "R" option in StarRCXT: lpe flag set to "2"
   * No capacitances extraction with LPE tool,
   * Parasitic capacitances in SPICE models,
   * Contact resistances of Source, Drain and Gate extraction with LPE tool,
   * Contact resistances of Source/Drain desactivated in SPICE models (BSIM only, MM11 under evaluation).

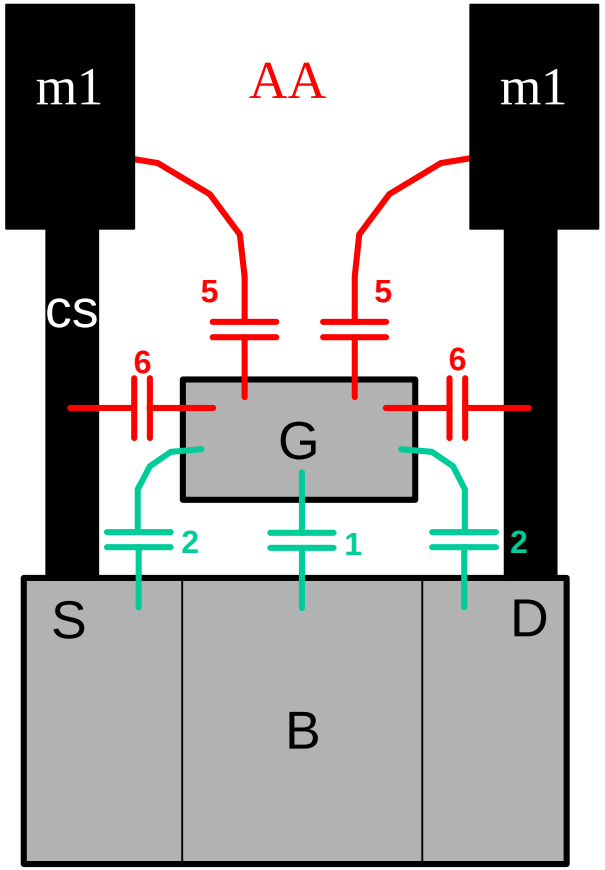
4. Post-layout simulations using "RC + VIACAP=YES " option in StarRCXT: lpe flag set to "3"
   * C3ext, C5, C6, C7m, C7c parasitic capacitances extraction with LPE tool,
   * Remaining parasitic capacitances in SPICE models,
   * Contact resistances of Source, Drain and Gate extraction with LPE tool,
   * Contact resistances of Source/Drain desactivated in SPICE models (BSIM only, MM11 under evaluation).

Summary of LPE Flag Implications

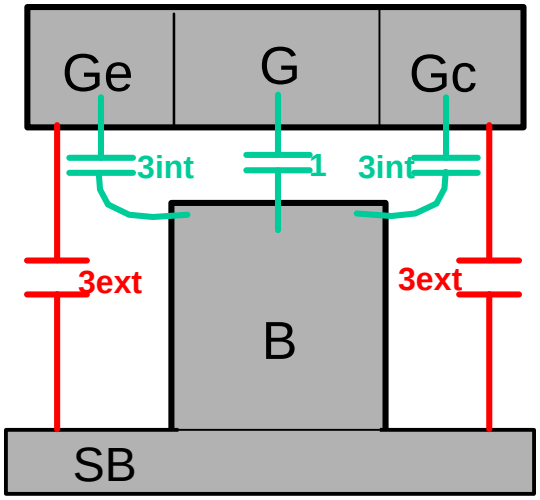
Crolles Model	v0.02	lpe=0,2, DEFAULT	lpe=1,3
StarRCXT setting	N/A, Pre-layout	N/A, Pre-layout	VIACAP=YES, DEFAULT
Capacitance			
C1	Model	Model	Model
C2	Model	Model	Model
C3int	-	Model	Model
C3ext	-	Model	Extracted
C4	-	Model	Model
C5 + C6	-	Model	Extracted
C7c	-	Model	Extracted
C7m	-	Model	Model and Extracted *

* Note: For the moment C7m is double counted. In future releases this will be corrected. The double counting contribution is however minor.

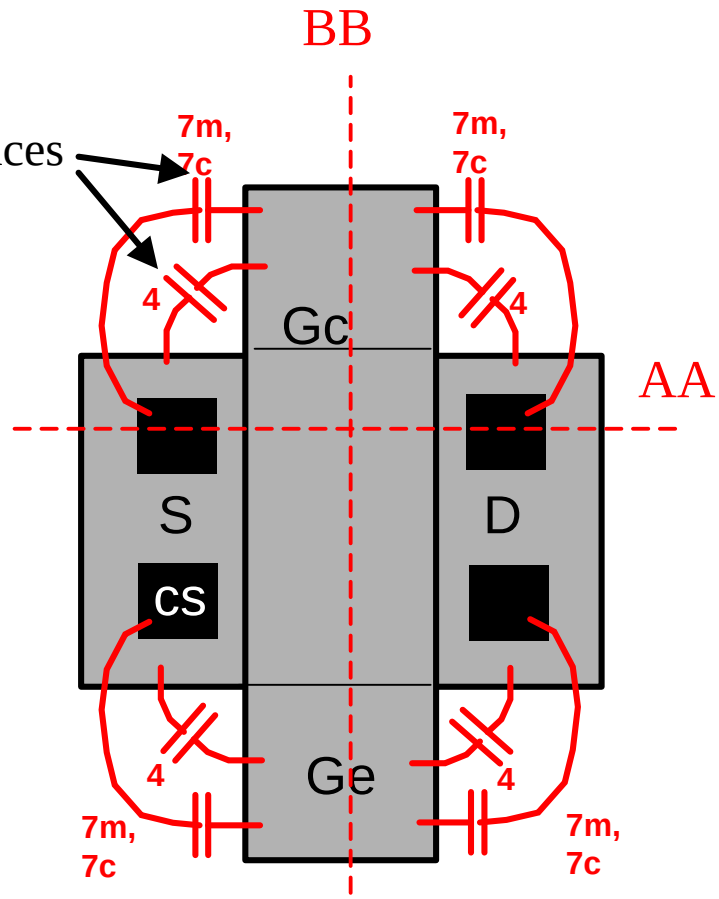
MOS Capacitance Overview (Pre-Layout, lpe = 0 or 2)



C's scaling with W



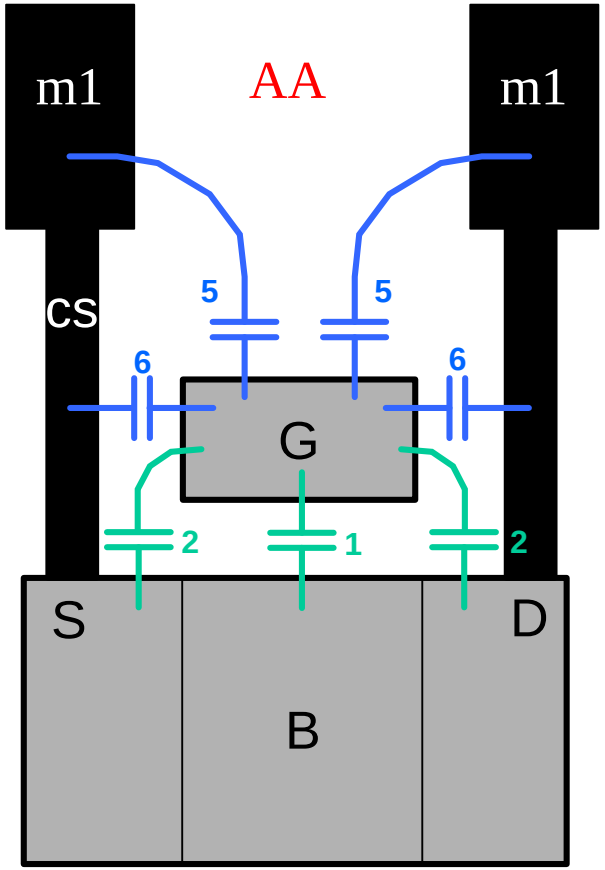
C's scaling with L

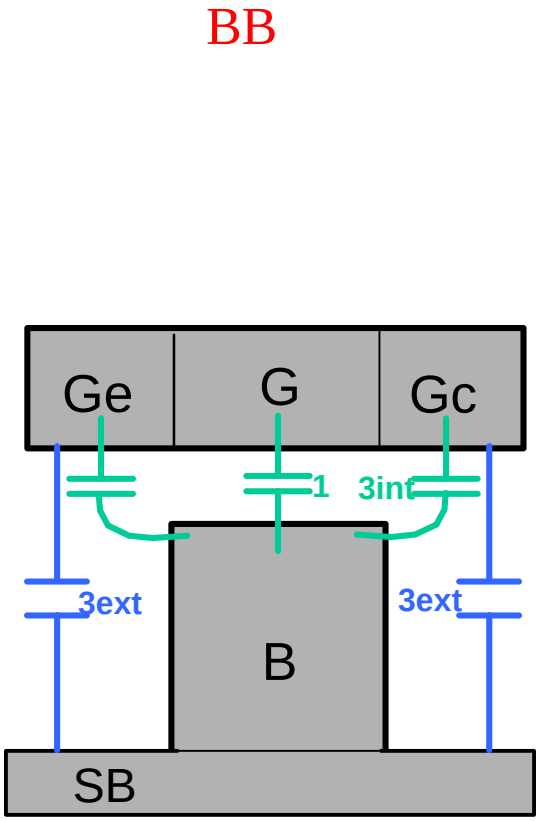


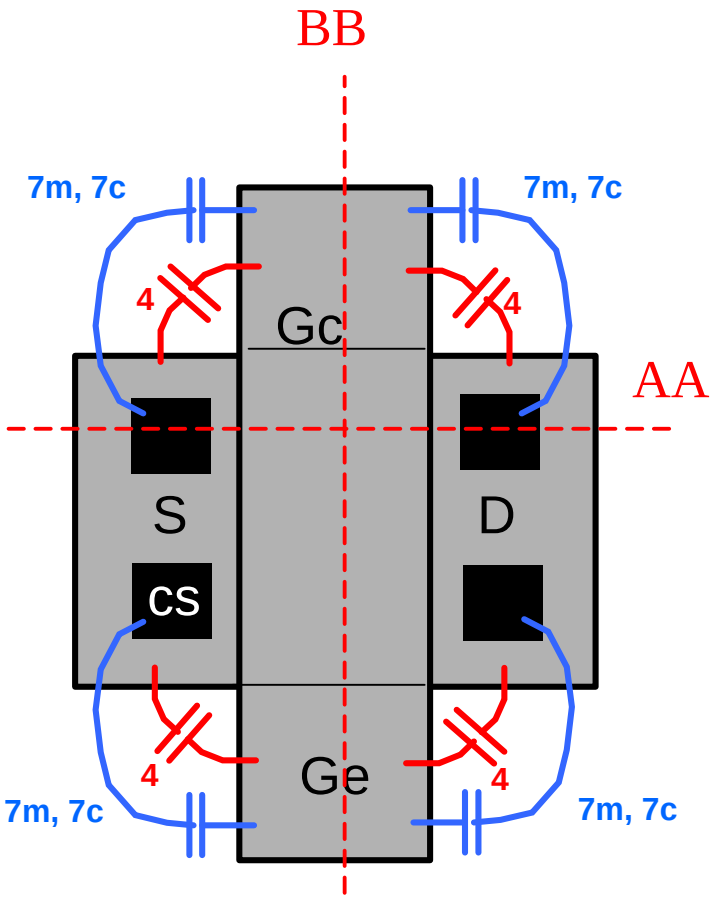
Corner Capacitance contributions

Capacitance drawn in green: Intrinsic capacitance included in SPICE model,
Capacitance drawn in red: Parasitic capacitance included in SPICE model.

MOS Capacitance Overview (Post-Layout, lpe = 1 or 3)







C's scaling with W

C's scaling with L

Corner Capacitance contributions

Capacitance drawn in green: Intrinsic capacitance included in SPICE model,
Capacitance drawn in red: Parasitic capacitance included in SPICE model,
Capacitance drawn in blue: Parasitic capacitance extracted using LPE tool.

Parasitic Capacitances: Scaling versus W and L for dogbone structures

- C2 = fudge_factor*[C20 + C2w*WOD]
- C3int = fudge_factor_c3*[C3int0 + C3intl*LPOLY]
- C3ext = C3ext0 + C3extl*LPOLY
- C4 = C40 + C4l*LPOLY + C4w*WOD
- C7 = C7m + C7c = C70 + C7l*LPOLY + C7w*WOD
- C56 = C5 + C6
  = C560 + C56l*log10(1+LPOLY/(2*co2po)) + C56w*WOD
  + C56wl*WOD*log10(1+LPOLY/(2*co2po))

  where co2po is the distance between Source (or Drain) contact and Poly Gate edge.

Fudge: factor to correct for depletion in Silicon. The simulations were performed with Raphael which considers only metals and dielectrics. The fudge factor was determined using TCAD simulations:

- fudge_factor = 0.75
- fudge_factor_c3 = 0.3

Parasitic Capacitances: Scaling versus W and L for standard structures

- C2 = fudge_factor*[C20 + C2w*WOD]
- C3int = fudge_factor_c3*[C3int0 + C3intl*LPOLY]
- C3ext = C3ext0 + C3extl*LPOLY
- C4 = C40 + C4l*LPOLY + C4w*WOD
- C7 = C7m + C7c = C70 + C7l*TANH(LPOLY/C7l0) + C7w*TANH(WOD/C7w0)
- C56 = C5 + C6
  = C560 + C56l*WOD*TANH(LPOLY/C56l0) + C56w*WOD.

Fudge: factor to correct for depletion in Silicon. The simulations were performed with Raphael which considers only metals and dielectrics. The fudge factor was determined using TCAD simulations

- fudge_factor = 0.75
- fudge_factor_c3 = 0.3