DR25 MODELS (NDR25, PDR25)

1. CONDITIONS OF EXTRACTION

- Maturity: Tentative
- Model parameters extraction based on lot :
- Geometrical extraction domain:
  - Drawn gate length : 0.5 ≥ L ≥ 0.5 µm
  - Drawn transistor width : 10 ≥ W ≥ 1 µm
- Temperature extraction domain: -40 ˚C to 150 ˚C
- Bias extraction domain:
  - Gate bias: 0 ≤ |VGS| ≤ 2.75 V (VDD + 10%)
  - Drain bias: 0 ≤ |VDS| ≤ 2.75 V (VDD + 10%)
  - Bulk bias: 0 ≤ |VBS| ≤ 2.75 V (VDD + 10%)

2. CONDITIONS OF SIMULATION

- Temperature: 25 ˚C
- Currents:

  IDLIN = Ids at Vgs = 2.5 V, Vds = 100 mV and Vbs = 0 V

  ION = Ids at Vgs = 2.5 V, Vds = 8 V and Vbs = 0 V

  IOFF = Ids at Vgs = 0 V, Vds = 8 V and Vbs = 0 V

  IG_ON = Igs at Vgs = 2.5 V and Vd= Vs = Vb = 0 V

  IG_OFF = Igs at Vgs =Vbs = 0 V and Vds = 8 V
- Threshold voltage in linear and saturation regime

  VTLIN is Vgs value at Vds = 100 mV, Vbs = 0 V and Ids=100*W/L nA.

  VTSAT is Vgs value at Vds = 8 V, Vbs = 0 V and Ids=100*W/L nA.
- Current derivatives:

$$Gm = \frac{\partial}{\partial V_{gs}} Ids$$ at Vgs = VTLIN + 0.2 V, Vds = 1.25 V and Vbs = 0 V

$$Gd = \frac{\partial}{\partial V_{ds}} Ids$$ at Vgs = VTLIN + 0.2 V, Vds = 1.25 V and Vbs = 0 V

Analog gain = Gm/Gd

- Gate Capacitances:

  CGGINV = CGG at Vgs = 2.5 V, Vds = 0 V and Vbs = 0 V

  CGD_0V = CGD at Vgs = 0 V, Vds = 0 V and Vbs = 0 V

  $$CGGMEAN = \frac{1}{VDD} \cdot \int_{0}^{VDD} CGG \times dVgs$$ with VDD = 2.5 V and Vbs = 0 V

  TAU = CGGMEAN*VDD/ION

- Diode Capacitances:

  CBD OFF = CBD at Vgs = 0 V, Vds = 8 V and Vbs = 0 V

  Note: the area and perimiters of source/drain junction diodes used for simulation are defined with the the minimum poly-to-active distance specified in the DRM.

- Transition frequency:

  FT = frequency for which the small signal current gain H_{21} is 0 dB (i.e. $\left|\frac{I_d}{I_g}\right|$ = 0 dB).

3. MAIN ELECTRICAL CHARACTERISTICS OF NMOS DR25 TRANSISTORS

PARAMETERS	DR25_SSA	DR25_TT	DR25_FFA	units
N-channel transistors (ndr25)				
VTLIN W=10/L=0.5	641	587	512	mV
IDLIN W=10/L=0.5	1.22e-04	1.77e-04	2.85e-04	A
VTSAT W=10/L=0.5	635	582	507	mV
ION W=10/L=0.5	1.72e-03	2.45e-03	3.62e-03	A
VTLIN W=10/L=0.5	641	587	512	mV
IDLIN W=10/L=0.5	1.22e-04	1.77e-04	2.85e-04	A
VTSAT W=10/L=0.5	635	582	507	mV
ION W=10/L=0.5	1.72e-03	2.45e-03	3.62e-03	A
IOFF W=10/L=0.5	6.11e-14	1.61e-13	8.84e-13	A
IG_ON W=10/L=0.5	0.00e+00	0.00e+00	0.00e+00	A
IG_OFF W=10/L=0.5	0.00e+00	0.00e+00	0.00e+00	A
FT W=10/L=0.5	6.39e+09	8.17e+09	1.29e+10	Hz
CGGinv W=10/L=0.5	4.48e-14	4.67e-14	4.89e-14	F
CGGmean W=10/L=0.5	3.80e-14	4.14e-14	4.54e-14	F
CGD 0V W=10/L=0.5	3.07e-15	1.18e-14	2.14e-14	F
CBD OFF[a] W=10/L=0.5	1.74e-14	1.81e-14	1.88e-14	F
Tau W=10/L=0.5	55.1	42.2	31.3	ps
Gm W=10/L=0.5	2.94e-04	4.08e-04	5.93e-04	S
Gd W=10/L=0.5	2.28e-07	3.24e-07	5.27e-07	S
Gain W=10/L=0.5	1.29e+03	1.26e+03	1.13e+03	
VTLIN W=1/L=0.5	632	578	507	mV
IDLIN W=1/L=0.5	1.12e-05	1.65e-05	2.70e-05	A
VTSAT W=1/L=0.5	626	573	502	mV
ION W=1/L=0.5	1.54e-04	2.25e-04	3.42e-04	A
IOFF W=1/L=0.5	9.28e-15	2.33e-14	1.10e-13	A
FT W=1/L=0.5	6.20e+09	7.68e+09	1.19e+10	Hz

Table 1: Main electrical characteristics for NMOS

a. Value coresponding to the minimum poly-to-acvtive distance specified in the DRM

4. MAIN ELECTRICAL CHARACTERISTICS OF PMOS DR25 TRANSISTORS

PARAMETERS	DR25_SSA	DR25_TT	DR25_FFA	units
P-channel transistors (pdr25)				
VTLIN W=10/L=0.5	692	609	516	mV
IDLIN W=10/L=0.5	3.05e-05	4.67e-05	8.51e-05	A
VTSAT W=10/L=0.5	684	604	510	mV
ION W=10/L=0.5	4.81e-04	7.89e-04	1.41e-03	A
VTLIN W=10/L=0.5	692	609	516	mV
IDLIN W=10/L=0.5	3.05e-05	4.67e-05	8.51e-05	A
VTSAT W=10/L=0.5	684	604	510	mV
ION W=10/L=0.5	4.81e-04	7.89e-04	1.41e-03	A
IOFF W=10/L=0.5	4.01e-14	2.18e-13	1.95e-12	A
IG_ON W=10/L=0.5	0.00e+00	0.00e+00	0.00e+00	A
IG_OFF W=10/L=0.5	0.00e+00	0.00e+00	0.00e+00	A
FT W=10/L=0.5	1.74e+09	2.54e+09	4.78e+09	Hz
CGGinv W=10/L=0.5	4.47e-14	4.64e-14	4.86e-14	F
CGGmean W=10/L=0.5	3.77e-14	4.09e-14	4.44e-14	F
CGD 0V W=10/L=0.5	2.82e-15	9.77e-15	1.71e-14	F
CBD OFF[a] W=10/L=0.5	2.43e-14	2.72e-14	3.00e-14	F
Tau W=10/L=0.5	196.0	129.6	78.6	ps
Gm W=10/L=0.5	9.86e-05	1.42e-04	2.22e-04	S
Gd W=10/L=0.5	8.91e-08	1.33e-07	2.81e-07	S
Gain W=10/L=0.5	1.11e+03	1.06e+03	7.87e+02	
VTLIN W=1/L=0.5	699	614	520	mV
IDLIN W=1/L=0.5	2.94e-06	4.57e-06	8.43e-06	A
VTSAT W=1/L=0.5	690	608	514	mV
ION W=1/L=0.5	4.51e-05	7.50e-05	1.36e-04	A
IOFF W=1/L=0.5	3.79e-15	2.00e-14	1.80e-13	A
FT W=1/L=0.5	1.72e+09	2.45e+09	4.59e+09	Hz

Table 2: Main electrical characteristics for PMOS

a. Value coresponding to the minimum poly-to-acvtive distance specified in the DRM

5. ION, IOFF, VT BEHAVIOR VERSUS GATE LENGTH AND CHANNEL WIDTH FOR NMOS DR25 TRANSISTORS

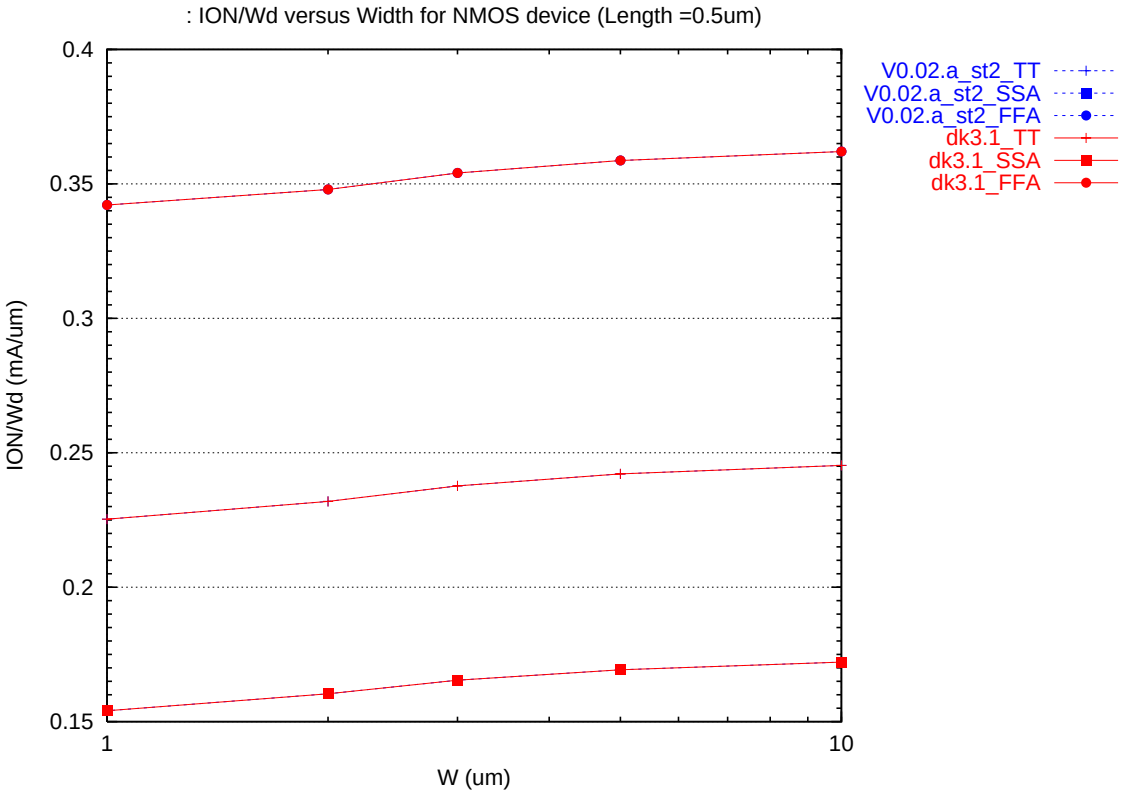

Figure 1 : ION versus drawn channel width for NMOS DR25 transistors (L = 0.5 µm)

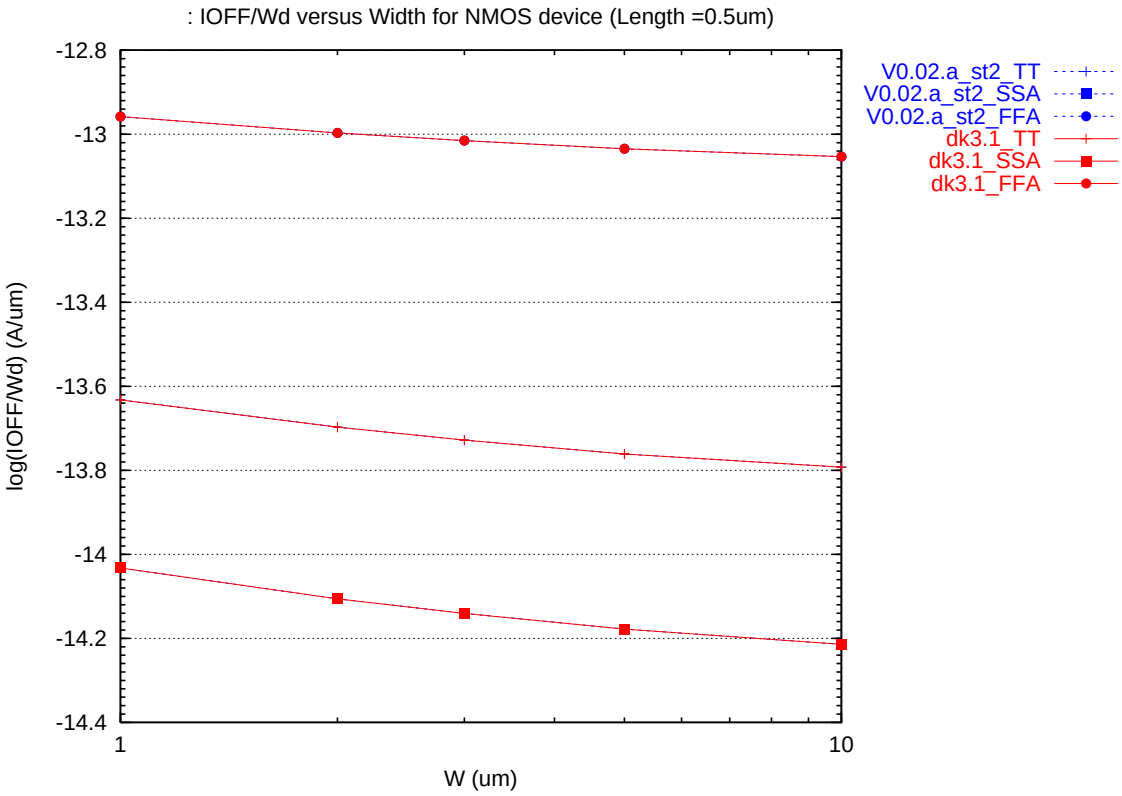

Figure 2 : IOFF versus drawn channel width for NMOS DR25 transistors (L = 0.5 µm)

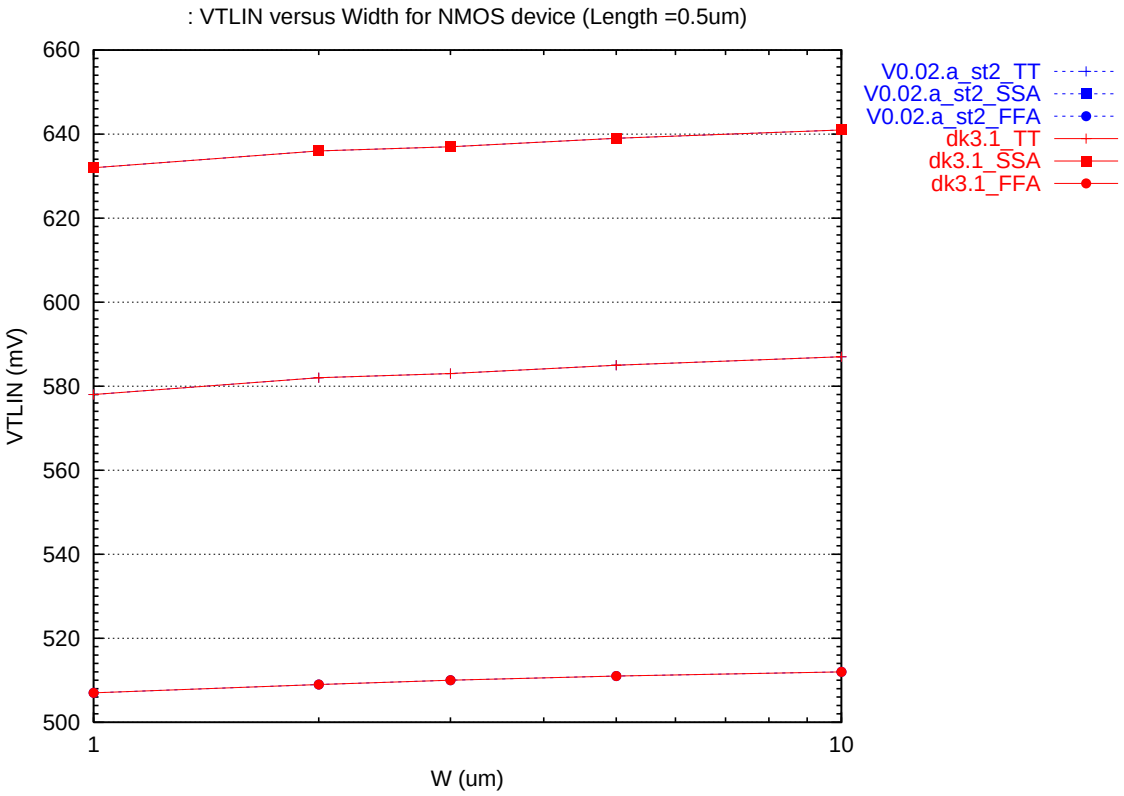

Figure 3 : Threshold voltage VTLIN versus drawn channel width for NMOS DR25 transistors (L = 0.5 µm)

6. ION, IOFF, VT BEHAVIOR VERSUS GATE LENGTH AND CHANNEL WIDTH FOR PMOS DR25 TRANSISTORS

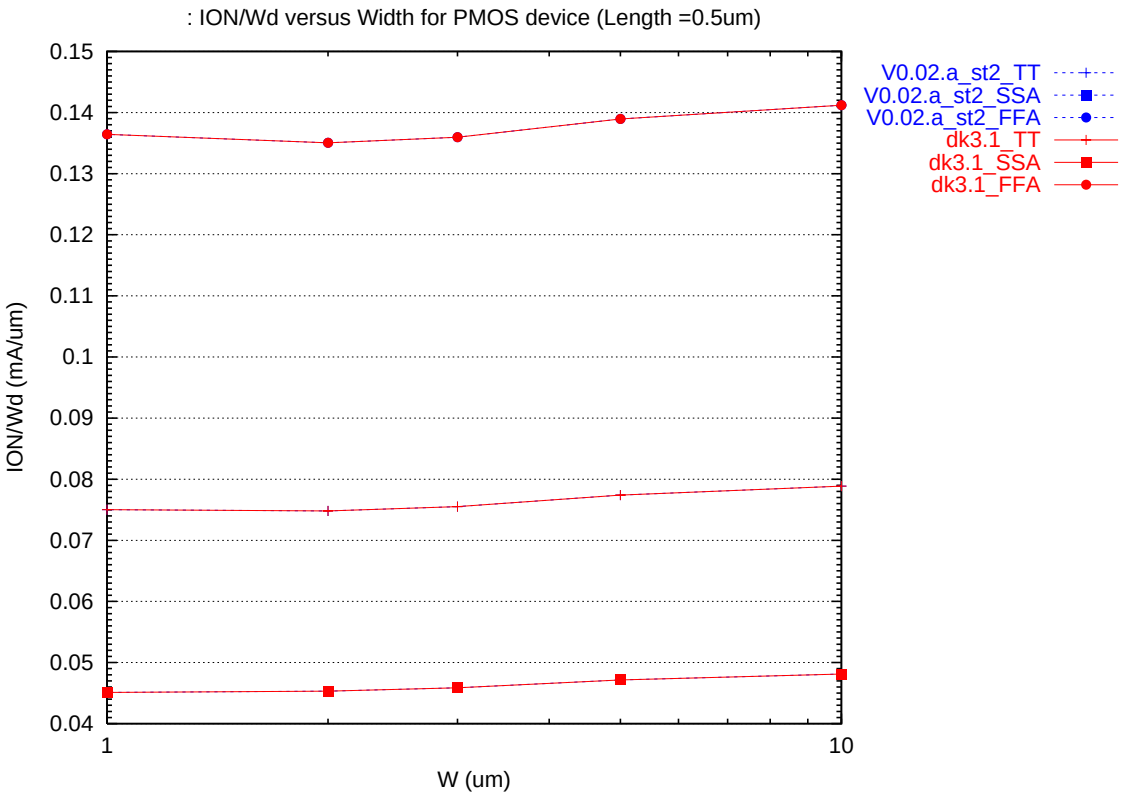

Figure 4 : ION versus drawn channel width for PMOS DR25 transistors (L = 0.5 µm)

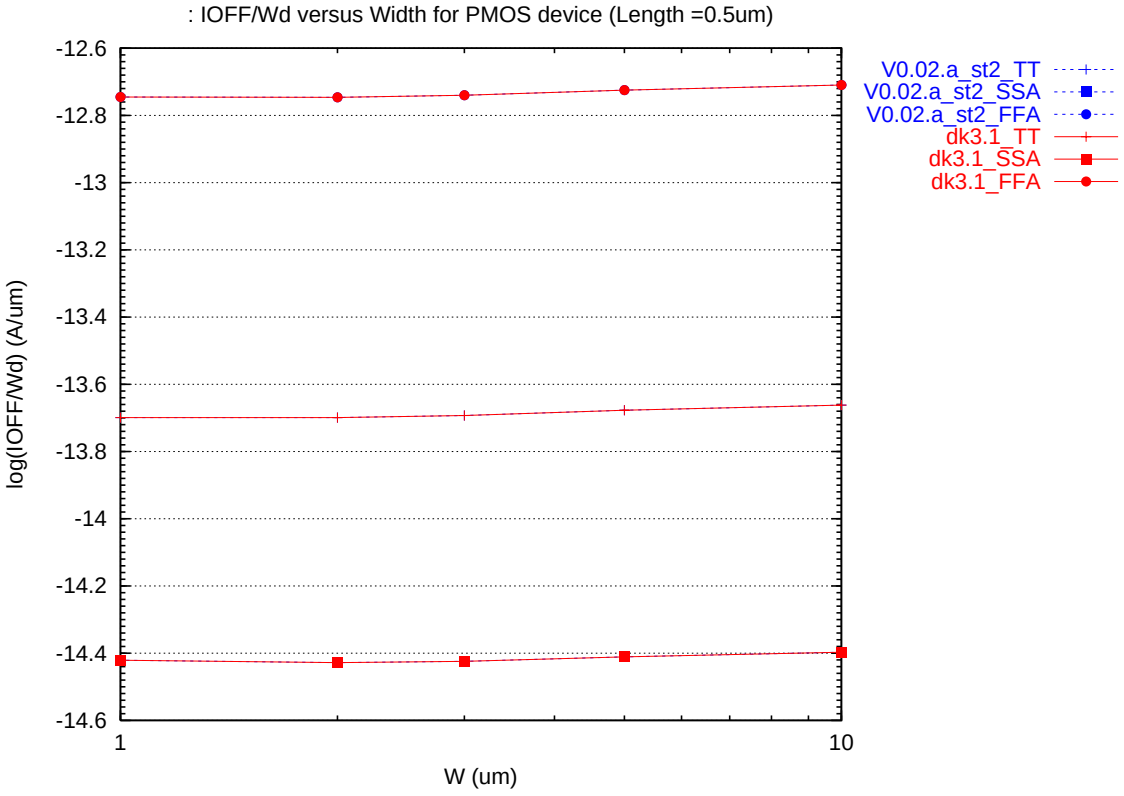

Figure 5 : IOFF versus drawn channel width for PMOS DR25 transistors (L = 0.5 µm)

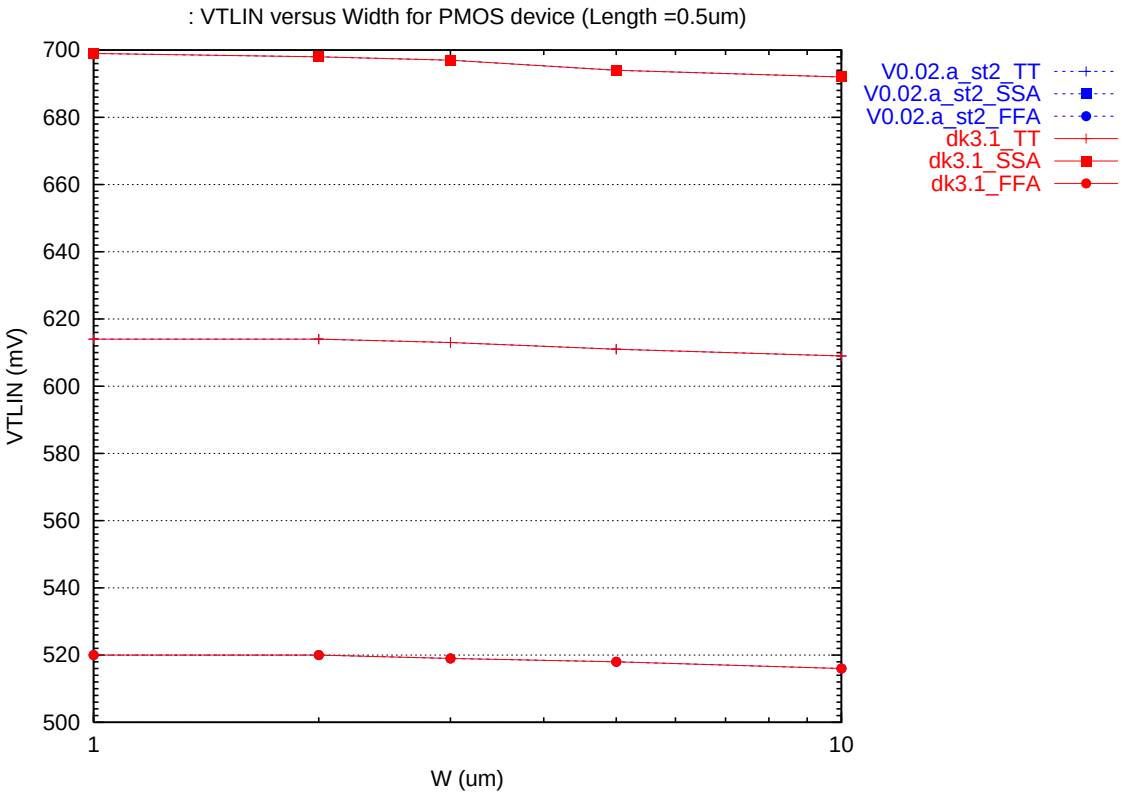

Figure 6 : Threshold voltage VTLIN versus drawn channel width for PMOS DR25 transistors (L = 0.5 µm)