FTM – Central Cad & Design Solution

CALIBRE MODULE SWITCH DOCUMENTATION

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Team: **Layout Verification Team**

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1 - INTRODUCTION

This documentation aims to present the **Calibre Module Switch Documentation**.

- Technology : cmos065lpgp_RF_7m4x0y2z_50A28A
- Design Kit version : 4.2
- Calibre release : 2006.1_19.20
- CMOS065 ANALOG & RF DESIGN RULES MANUAL - 65NM CMOS PROCESS revB ADCS 7855274-
- Design rule manual : DRM 65 nm Bulk CMOS Process ADCS #7683821 RevD (29 Dec 2005)
- Document named "ANTICIPATED CHANGES TO CMOS065 Design Rule Manual 65nm Bulk CMOS Process" (Version revD draft1 dated 7 July 2005)
- EWS, Assembly and reliability design Rules Manual, Rev Y (ADCS Doc # 0018063)
- EWS, Advanced Assembly and reliability design Rules Manual, Rev E (ADCS Doc # 7114456)
- Flip Chip, Design guide for solder bumped wafers Manual Rev F (ADCS Doc # 7158281)

2 - CALIBRE SWITCHES

2.1 DRC Switches

- **INVISIBLE SWITCHES:**
  - INTERACTIVE

The default is set to "YES" when in an interactive window.
This is an invisible switch, that allows to get a default configuration when Calibre is used in batch mode.

  - ALLIANCE

The default is set to "NO", which means that specific ST modifications are used. When set to "YES", one can only use the TKIT file (available with $U2TK_CALIBRETKITdrc.

- **DENSITY CHECKS MANAGEMENT**
  - density_CHECKS

"Check Density Rules". Allows to turn ON or OFF density checks. The default is set to "YES". THIS IS DRM MANDATORY FOR CIRCUIT FINISHING.

In the early phases of the layout of a design/cell/block, it may be more user friendly to turn OFF the density checks as it is known that, becuase the layout is not yet finished, minimum density may not be reached on all layers.

By default, all minimum density checks are performed; this corresponds to the following list of design rules: OD.DEN.1 OD.DEN.2 OD.DEN.3 PO.DEN.2 PO.DEN.3 AP.DEN.2 I_DUM.DEN.1 I_DUM.DEN.2 M1.DEN.1 M1.DEN.3.1 M2X.DEN.1 M2X.DEN.3.1 M3X.DEN.1 M3X.DEN.3.1 M4X.DEN.1 M4X.DEN.3.1 M5X.DEN.1 M5X.DEN.3.1 M6Z.DEN.1 M6Z.DEN.3.1 M7Z.DEN.1 M7Z.DEN.3.1 CTM.DEN.1

These checks can be turned OFF by undefining the DENSITY_CHECK variable.
Note that Maximum density checks are always performed (not possible to turn them OFF).

- **SEALRING AND LOGO CHECKS MANAGEMENT**
  - BEOL_SEALRING

" Check metalization ID marker if ...". The default is set to "NO".

Design rule ID.BEOL.1 requires presence on a design to be taped out of marker layers indicating which metal option is used.

If a sealring has been placed around the design, the metallization marker layers must be placed with respect to the seal ring boundary ; this is the default behaviour of the tkit DRC techfile.
In some cases, it can occur that a design is taped out without seal ring: in such a case, the calibre variable BEOL_SEALRING must be defined so that the check is performed, not with respect to the sealring boundary, but rather with respect to the design boundary itself.

+ COMPANY_MKR_SEALRING

"Check company marker if ...". The default is set to "NO".

Design rule ID.IP.1 requires presence on a design to be taped out of marker layers indicating which company this design belongs to.

If a sealring has been placed around the design, the company marker layers must be placed with respect to the seal ring boundary ; this is the default behaviour of the tkit DRC techfile.

In some cases, it can occur that a design is taped out without seal ring: in such a case, the calibre variable COMPANY_MKR_SEALRING must be defined so that the check is performed, not with respect to the sealring boundary, but rather with respect to the design boundary itself (OD and PO layers used to compute cell boundary)

- **DATA SIZE and PF CHECKS MANAGEMENT**

+ DATA_SIZE_SEALRING

Check size of extent of data if it is a design submission without sealring. Design rule ID.W.1 requires, on a design to be taped out, that the extent of the data is a rectangle with edge's lenght multiple of 2.

If a sealring has been placed around the design, check is done with respect to the seal ring boundary by default.

In some cases, it can occur that a design is taped out without seal ring: in such a case, the calibre variable DATA_SIZE_SEALRING must be defined so that the check is performed, not with respect to the sealring boundary, but rather with respect to the design boundary itself (CHIP).

+ PF

Check rules for Poly Fuses. Allows to turn ON or OFF design rules PF.?
By default, they are not checked. This check can be turned ON by defining the PF calibre variable.

- **SRAM MEMORIES MANAGEMENT**
  - EXCLUDE_SRAMDMY_ONLY

"Use SRAMDMY only as DRC exclusion layer...". The default is set to "NO".

Present in tkit DRC file to "mimic" TSMC DRC on SRAMs:

Allows to determine which layer(s) should be used to exclude from DRCed database, a set of layers in the "3rd party" SRAM memories. Such memories have been designed using TSMC DRC which removes from the DRCed database a set of layers (from DNW to VIA1).

In TSMC DRC, two layers can be used to remove these layers from the DRCed database: (SRM, drawing) and (MKR, sramdmy)

By default, the OR of (SRM, drawing) and (MKR, sramdmy) is used. If EXCLUDE_SRAMDMY_ONLY is set to TRUE (for ex. by clikcing on the corresponding button in the calibre interactive customization form), only the layer (MKR. sramdmy) is used.

- **PADS MANAGEMENT**
  - classPAD

It is possible that one has to enlarge the customization window to see all the possibilities.

"ClassPAD". The default is set to "classH1".

If an other class is used for the circuit, please select the corresponding class in the menu to the right. Selects all specific class rules.

  - CHECK_PAD_ASSEMBLY

"Check PAD_ASSEMBLY rules". The default is set to "YES".

This switch checks the pad assembly rules corresponding to the selected class.

- **RECOMMENDED RULES**
  - RECOMMENDED_RULES

"Check recommended rules on Poly / Well capacitors". The default is set to "NO".

Check specific recommended ST rules on poly / well capacitors (cpo25nw / cpo25pw / cpo18nw & cpo18pw) : Maximum area / maximum number of contact is checked. It is possible to get a not DRC clean layout with the Pcell about the number of contacts.

- **SPLIT GEN.5 RULE**
  - GEN5SPLIT

"Get GEN.5 rule splitted for each layer to easier correction". The default is set to "NO".

All GEN.x rules have been splitted by “layer checked”. However, the rule GEN.5 could not be directly splitted for backward compatibility with memory cuts. This switch enables one to split the rule to help designers to debug it. However, some fake errors can appear on memory cuts. Please do not try to correct or report bug on these layouts.

- **MEMORIES CHECKS MANAGEMENT**
  - EXCLUDE_SRAMDMY_ONLY

Use SRAMDMY only as DRC exclusion layer for non alliance memories. The default is set to "NO".

Present in tkit DRC file to "mimic" TSMC DRC on SRAMs:
Allows to determine which layer(s) should be used to exclude from DRCed database, a set of layers in the "3rd party" SRAM memories. Such memories have been designed using TSMC DRC which removes from the DRCed database a set of layers (from DNW to VIA1). In TSMC DRC, two layers can be used to remove these layers from the DRCed database:|
- (SRM, drawing)
- (MKR, sramdmy)

By default, the OR of (SRM, drawing) and (MKR, sramdmy) is used If EXCLUDE_SRAMDMY_ONLY is set to TRUE (for ex. by clikcing on the corresponding button in the calibre interactive customization form), only the layer (MKR. sramdmy) is used.

2.2 LVS Switches

- **INVISIBLE SWITCHES:**
  - INTERACTIVE

The default is set to "YES" when in an interactive window.

This is an invisible switch, that allows to get a default configuration when Calibre is used in batch mode.

  - ALLIANCE

The default is set to "NO", which means that specific ST modifications are used. When set to

"YES", one can only use the TKIT file (available with $U2TK_CALIBRETKITlvs).

- **ERC rules management**

  + NOERC1_TO_NOERC12

"Skip ERC1 to ERC12 rules check (Wells biasing)". The default is set to "NO"

When **not** selected, it checks Wells biasing (Pwell, nwell or substrat not correctly connected).

  + ERC13_AND_ERC14

"Check ERC13 and ERC14 rules check...". The default is set to "NO".

When selected, it checks there is no wiring connection througth poly or active.

  + ERC15

"Check ERC15 rules check (Floating OD-PO intersection)". The default is set to "NO".

When selected, it checks floating gates (Active + poly intersection) not connected to a fixed voltage node (other device or well strap).

- **SENSE parameter**

  + SENSE

"Sense extraction and comparison". The default is set to "NO".

Switch to extract sensitive components (diods / mos /resistors that have a "SENSE" property). There is no wiring metal{1 to sense number} over sensitive component, so less parasistic effects on the device.

- **Parallel or series reduction**

  + ANALOG

"Analog mode (no parallel/series reduction performed)". The default is set to "NO".

When selected, no parralel or series reduction are done. Longer... Enables device / device (or 1:1) checks.

- **PW / DNW diods**

  + LVS_DDNWPW_PARAMS

"Compare area & perimeter of isolated PW to DNW diods". The default is set to "YES".

Switch to extract and to check values of DNW/PW diods, checking area and perimeter of these diods.

- **Tolerance on resistors**

  + SWI_TOLER_RES_W

"Tolerance for resistor width comparison (%)". The default is set to 0.

Tolerance allowed for the width of resistors during *layout vs schematic* comparison.

+ SWI_TOLER_RES_L

"Tolerance for resistor length comparison (%)". The default is set to 0.

Tolerance allowed for the length of resistors during *layout vs schematic* comparison.

+ SWI_TOLER_RES_R

"Tolerance for resistor length comparison (%)". The default is set to 1.

Tolerance allowed for the resistance of resistors during *layout vs schematic* comparison. (only in electrical mode)

- **Tolerance on capacitors**

+ SWI_TOLER_CAP_A

"Tolerance for capacitor ara comparison (%)". The default is set to 0.

Tolerance allowed for the area of capacitors during *layout vs schematic* comparison.

+ SWI_TOLER_CAP_P

"Tolerance for capacitor perimeter comparison (%)". The default is set to 0.

Tolerance allowed for the perim of capacitors during *layout vs schematic* comparison.

+ SWI_TOLER_CAP_C

"Tolerance for capacitor capacitance comparison (%)". The default is set to 5.

Tolerance allowed for the capacitance of the capacitor (only when ELECT is selected).

- **Tolerance on MOS & RF MOS**

+ SWI_TOLER_MOS_W

The default is set to 1. Tolerance allowed for the width of all standard and SRAM mos.

+ SWI_TOLER_MOS_L

The default is set to 0. Tolerance allowed for the length of all standard and SRAM mos.

+ SWI_TOLER_MOSRF_W

The default is set to 1. Tolerance allowed for the width of all RF mos.

+ SWI_TOLER_MOSRF_L

The default is set to 0. Tolerance allowed for the length of all RF mos.

- **Electrical extraction**

  + ELECT

"Enable electrical comparison (default = sign-off)"

Enables to switch from geometrical comparaison to electrical comparaison.
On capacitors: capacitance C is compared instead of Carea and Cperi values ;
On resistors: Resistance R is compared instead of width W.

- **LVS_DONOTCOMPARE_ESU_EDU CHECKS MANAGEMENT :**

Do not compare ESU and EDU of non salicided MOS transistors.

  + LVS_DONOTCOMPARE_ESU_EDU

The switch LVS_DONOTCOMPARE_ESU_EDU allows to turn ON or OFF the comparison of esu/edu parameters.

- if LVS_DONOTCOMPARE_ESU_EDU is not defined, compare ESU and EDU of non salicided MOS transistors. (this is the default behaviour)

- if LVS_DONOTCOMPARE_ESU_EDU is defined, Do not compare ESU and EDU of non salicided MOS transistors.

- **LVSEXTASADPSPDPAR / LVSEXTSTIPAR CHECKS MANAGEMENT :**

  + LVSEXTASADPSPDPAR

If LVSEXTASADPSPDPAR is defined, for MOS transistors, values for AS AD PS & PD are computed from layout and written in output netlist (no comparison to schematic) (this is the default behaviour for LPE).

If LVSEXTASADPSPDPAR is not defined, for MOS transistors, values for AS AD PS & PD are not computed from layout and written in output netlist (no comparison to schematic) (this is the default behaviour for LVS)

  + LVSEXTSTIPAR

If LVSEXTSTIPAR defined, for MOS transistors, values for the parameter used for "STI stress" modeling are computed from layout and written in output netlist (no comparison to schematic) (this is the default behaviour for LPE)

If LVSEXTSTIPAR not defined, for MOS transistors, values for the parameter used for "STI

stress" modeling are not computed from layout and written in output netlist (no comparison to schematic) (this is the default behaviour for LVS)

- **DDNWPW PARAMETERS CHECKS MANAGEMENT :**

Checks comparaison of DDNWPW parameters.

+ LVS_DDNWPW_PARAMS

In case of usage of layer DNW (isolation of Pwell regions), the tkit calibre LVS techfiles extract from the layout a diode ddnwpw between the isolated PWell region and the DNW region: this is to check the correct biasing of the DNW isolation zone. Also the diode parameters (area and peri) are computed from layout and compared to schematic.

This corresponds to the default behaviour.

It may be necessary not to compare the diode parameters between schematic and layout: to do so, the user must undefine the calibre variable LVS_DDNWPW_PARAMS.

- **LVSEXTPARADIODE / LVSEXTPROBE CHECKS MANAGEMENT :**

Extract from layout Well/sub diode for simulation (LPE). Checks extraction and comparaison of probe devices.

+ LVSEXTPARADIODE

If LVSEXTPARADIODE is defined, extracts parasitic diodes between NW and substrate (dnwps) and between DNW and substrate (ddnwps) are performed (this is the default behaviour for LPE)

If LVSEXTPARADIODE is not defined, extracts parasitic diodes between NW and substrate (dnwps) and between DNW and substrate (ddnwps) are not performed (this is the default behaviour for LVS)

+ LVSEXTPROBE

the tkit product includes support of so called ebeam and micro probes.

By default these devices are "recognized" from layout and their connectivity is compared to schematic; for designs including such probes, the schematic database must thus contain instances of the ebeamprobe or microprobe cells (with correct value settings for their parameters area and peri).

In some situations, it may be necessary to desactivate this extraction from layout and

corresponding comparison to schemetaic; this can be done by undefining the calibre variable LVSEXTPROBE.

Note: this is the case for the LPE flow (calibre starrcxt) because these devicves do not have corresponding simulation models: they are thus not present in the device level simulation netlists extracted from layout.

- **LVSNOFILTERUNUSEDDEVICE CHECKS MANAGEMENT :**

Do not filter unused devices (O AB RC RG)

If LVSNOFILTERUNUSEDDEVICE is defined, filter unused devices (O AB RC RG) is performed (this is the default behaviour for LVS)

If LVS_BIP_PARAMS is not defined, filter unused devices is not performed.

Signification of option (O AB RC RG) for the filtering of unused devices (O AB RC RG):

O : Repeats all unused device filtering until no more devices can be filtered. Also repeats series and parallel reduction of capacitor, resistor, diode, and MOS devices, split gate reduction, and semi-series MOS reduction.

AB : Filters MOS devices with source, drain, and gate pins tied together.

RC : Filters resistors with POS and NEG pins tied together.

RG : Filters diodes with POS and NEG pins tied together.

- **PORT/ TEXT DEPTH CHECKS MANAGEMENT :**

Select the level of hierarchy of the port or text depth.

+ SWI_PORT_DEPTH

This calibre variable is used to specifiy where (in the layout hierarchy) to look for labels to be processed by calibre LVS as ports.

By default, the labels are searched only at the primary level of the layout hierarchy of the processed cell.

To look deeper in the hierarchy the variable SWI_PORT_DEPTH can be set to 1 (two levels of layout hierachy), 2 (three levels) or 3 (four levels).

+ SWI_TEXT_DEPTH

This calibre variable is used to specifiy where (in the layout hierarchy) to look for labels to be

processed by calibre LVS as text information.

By default, the texts are searched only at the primary level of the layout hierarchy of the processed cell.

To look deeper in the hierarchy the variable SWI_TEXT_DEPTH can be set to 1 (two levels of layout hierachy), 2 (three levels) or 3 (four levels).

2.3 Dummies Generation Switches

The Tkit Calibre Tiling techfiles contain different switches,refer to cmos065 calibre_tiling_userdoc tkit for more details.

Tiling scripts are provided as independent calibre DRC type techfiles, allowing generating from a design layout the cells including all tiles (all layers as described in DRM) for this design. The output of this procedure is a GDS file that needs to be assembled with the overall design.

It must be possible for the user:

- to generate tiles on a layer per layer basis
- to choose tiles orientation in case of metal layers
- to "block" tiles insertion on parts of the design on a layer per layer basis; this is done by marking these regions with specific marker layers (purpose tileNot of corresponding layers). (MKR, tileNot) blocks all tiles.

In addition, there exists a specific marker layer (MKR, tile) which allows generating RPO shapes on top of OD tiles.

- **DENSITY CHECKS MANAGEMENT : Check minimum density rules after.**

MEASURE_DENSITY_AFTER_TILING

Minimum density DRC checks added inside tiling procedure (OD,M1,MiX,MiY,MiZ and AP); it is now possible to generate, in the calibre run corresponding to tiling, density res

The output results are:

- calibre DRC database which can be viewed with calibre RVE hilighting design locations with too low density (with respect to corresponding density design rule defined in D

- ascii files containing density figures for all windows in the design (density "statistics") (file name is the same as the one generated by standard DRC).

This feature can be switched on or off thanks to a calibre variable named MEASURE_DENSITY_AFTER_TILING:

- if MEASURE_DENSITY_AFTER_TILING is defined: the density design rule check after tiling is performed

- if MEASURE_DENSITY_AFTER_TILING is not defined (this is the default situation): density checks after tiling are not performed (same behaviour as in previous tkit releases

- **FIRST PASS TILES OD CHECKS MANAGEMENT : Enable first pass OD tiling (1.99x1.99um2 squares).**

SWI_FIRST_PASS_DUM_OD

This feature can be switched on or off thanks to a calibre variable named SWI_FIRST_PASS_DUM_OD

- if SWI_FIRST_PASS_DUM_OD is not defined : In the first OD tiling pass, square shaped (1.99 x 1.99 um2) OD tiles are not inserted.

- if SWI_FIRST_PASS_DUM_OD is defined : In the first OD tiling pass, square shaped (1.99 x 1.99 um2) OD tiles are inserted. (this is the default behaviour)

- **FIRST PASS TILES OD SPACE TO OD/PO SHAPES MANAGEMENT : Distance between first pass OD tiles and OD PO shapes.**

SWI_FIRST_PASS_DUM_OD_S

The user can specify at which distance the OD tiles should be placed with respect to the actual design OD PO shapes, whose default value is 1.5.

- **FIRST PASS TILES OD DENSITY MANAGEMENT : Density threshold below which first pass OD tiles are inserted**

SWI_FIRST_PASS_DUM_OD_T

The user can specify which is the OD density below which OD tiles should be inserted (local density on shifted windows), whose default value is 30.

- **SECOND PASS TILES OD CHECKS MANAGEMENT : Enable second pass OD tiling (rectangles, w=0.5um)**

SWI_SECOND_PASS_DUM_OD

This feature can be switched on or off thanks to a calibre variable named SWI_SECOND_PASS_DUM_OD,it allows to increase OD density after the first pass.

- if SWI_SECOND_PASS_DUM_OD is not defined : In the second OD tiling pass, smaller (rectangles, w=0.5um) OD tiles are not inserted.

- if SWI_SECOND_PASS_DUM_OD is defined : In the second OD tiling pass, smaller (rectangles, w=0.5um) OD tiles are inserted. (this is the default behaviour)
The user can also specify in this switch, the orientation of OD tiles (VERTICAL or HORIZONTAL) (the default is VERTICAL).

- **SECOND PASS TILES OD SPACE MANAGEMENT : Space second pass OD tiles**

SWI_SECOND_PASS_DUM_OD_D

The user can specify the space between inserting OD tiles, whose default value is 1.1.

- **SECOND PASS TILES OD SPACE TO OD/PO SHAPES MANAGEMENT : Distance between second pass OD tiles and OD PO shapes**

SWI_SECOND_PASS_DUM_OD_S

The user can specify at which distance the OD tiles should be placed with respect to the actual design OD PO shapes, whose default value is 0.6.

- **SECOND PASS TILES OD DENSITY MANAGEMENT : Density threshold below which second pass OD tiles are inserted**

SWI_SECOND_PASS_DUM_OD_T

The user can specify which is the OD density below which rectangular OD tiles should be inserted (local density on shifted windows, after first pass OD tiling) in case of difficulties to reach minimum OD density process requirements, it is possible to set a threshold value higher than the minimum specified in DRM, in order to "force" more tiles insertion, whose default

value is 25.

- **THIRD PASS TILES OD DENSITY MANAGEMENT : Density threshold below which third pass OD tiles are inserted**

SWI_THIRD_PASS_DUM_OD_T

This option is set to false by default: time consuming. It will generate OD dummies in 20x20um windows that contain no OD (in order to be conform with the rule OD.DEN.3.

- **TILES PO CHECKS MANAGEMENT : Enable PO tiling**

SWI_DUM_POLY
Note: As mentioned in the doc calibre_tiling_userdoc , zones where PO tiles can be inserted in a design are derived from the OD tiling algorithm. Note that PO tiles will be inserted even if OD tiling is not enabled.
This feature can be switched on or off thanks to a calibre variable named SWI_DUM_POLY

- if SWI_DUM_POLY is not defined : PO tiles are not inserted.

- if SWI_DUM_POLY is defined : PO tiles are inserted. (this is the default behaviour)

Note: In all the switch description below Mi can be M1, MX2, ...(Metal tiling; M1, thin or intermediate metals) Name of the variable varies accordingly

- **FIRST PASS TILES Mi CHECKS MANAGEMENT : Enable first pass Mi tiling (0.9x0.90um2 squares).**

SWI_FIRST_PASS_DUM_Mi

This feature can be switched on or off thanks to a calibre variable named SWI_FIRST_PASS_DUM_Mi

- if SWI_FIRST_PASS_DUM_Mi is not defined : In the first Mi tiling pass, square shaped (0.9x0.90um2 squares) Mi tiles are not inserted.

- if SWI_FIRST_PASS_DUM_Mi is defined : In the first Mi tiling pass, square shaped (0.9x0.90um2 squares) Mi tiles are inserted. (this is the default behaviour)

- **FIRST PASS TILES Mi SPACE TO Mi SHAPES MANAGEMENT : Distance between first pass Mi tiles and Mi shapes.**

SWI_FIRST_PASS_DUM_Mi_S

The user can specify at which distance the Mi tiles should be placed with respect to the actual design Mi shapes, whose default value is 1.5.

- **FIRST PASS TILES Mi DENSITY MANAGEMENT : Density threshold below which first pass Mi tiles are inserted**

SWI_FIRST_PASS_DUM_Mi_T

The user can specify which is the Mi density below which Mi tiles should be inserted (local density on shifted windows), whose default value is 10.

- **SECOND PASS TILES Mi CHECKS MANAGEMENT : Enable second pass Mi tiling (rectangles, w=0.4um)**

SWI_SECOND_PASS_DUM_Mi

This feature can be switched on or off thanks to a calibre variable named SWI_SECOND_PASS_DUM_Mi,it allows to increase Mi density after the first pass.

- if SWI_SECOND_PASS_DUM_Mi is not defined : In the second Mi tiling pass, smaller (rectangles, w=0.4um) Mi tiles are not inserted.

- if SWI_SECOND_PASS_DUM_Mi is defined : In the second Mi tiling pass, smaller (rectangles, w=0.4um) Mi tiles are inserted. (this is the default behaviour)

The user can also specify in this switch, the orientation of Mi tiles (VERTICAL or HORIZONTAL) (the default is VERTICAL).

- **SECOND PASS TILES Mi WIDTH MANAGEMENT : Width second pass Mi tiles**

SWI_SECOND_PASS_DUM_Mi_W

The user can specify the width between inserting Mi tiles, whose default value is 0.4.

- **SECOND PASS TILES Mi SPACE TO Mi SHAPES MANAGEMENT : Distance between second pass Mi tiles and Mi shapes**

SWI_SECOND_PASS_DUM_Mi_S

The user can specify at which distance the Mi tiles should be placed with respect to the actual design Mi shapes, whose default value is 0.6.

- **SECOND PASS TILES Mi DENSITY MANAGEMENT : Density threshold below which second pass Mi tiles are inserted**

SWI_SECOND_PASS_DUM_Mi_T

The user can specify which is the Mi density below which rectangular Mi tiles should be inserted (local density on shifted windows, after first pass Mi tiling)

in case of difficulties to reach minimum Mi density process requirements, it is possible to set a threshold value higher than the minimum specified in DRM, in

order to "force" more tiles insertion, whose default value is 25.

- **THIRD PASS TILES Mi CHECKS MANAGEMENT : Enable third pass Mi tiling (rectangles, w=0.4um)**

SWI_THIRD_PASS_DUM_Mi

This feature can be switched on or off thanks to a calibre variable named SWI_THIRD_PASS_DUM_Mi,it allows to increase Mi density after the second or first pass.

- if SWI_THIRD_PASS_DUM_Mi is not defined : In the third Mi tiling pass, smaller (rectangles, w=0.4um) Mi tiles are not inserted.

- if SWI_THIRD_PASS_DUM_Mi is defined : In the third Mi tiling pass, smaller (rectangles, w=0.4um) Mi tiles are inserted. (this is the default behaviour)

The user can also specify in this switch, the orientation of Mi tiles (VERTICAL or HORIZONTAL) (the default is HORIZONTAL).

- **THIRD PASS TILES Mi WIDTH MANAGEMENT : Width third pass Mi tiles**

SWI_THIRD_PASS_DUM_Mi_W

The user can specify the width between inserting Mi tiles, whose default value is 0.4.

- **THIRD PASS TILES Mi SPACE TO Mi SHAPES MANAGEMENT : Distance between third pass Mi tiles and Mi shapes**

SWI_THIRD_PASS_DUM_Mi_S

The user can specify at which distance the Mi tiles should be placed with respect to the actual design Mi shapes, whose default value is 0.6.

- **THIRD PASS TILES Mi DENSITY MANAGEMENT : Density threshold below which third pass Mi tiles are inserted**

SWI_THIRD_PASS_DUM_Mi_T

The user can specify which is the Mi density below which rectangular Mi tiles should be inserted (local density on shifted windows, after second or first pass Mi tiling)

in case of difficulties to reach minimum Mi density process requirements, it is possible to set a threshold value higher than the minimum specified in DRM, in

order to "force" more tiles insertion, whose default value is 25.

THIRD PASS TILES Mi CHECKS MANAGEMENT : Enable third pass Mi tiling (rectangles, w=0.4um)

SWI_THIRD_PASS_DUM_Mi

This feature can be switched on or off thanks to a calibre variable named SWI_THIRD_PASS_DUM_Mi,it allows to increase Mi density after the second or first pass.

- if SWI_THIRD_PASS_DUM_Mi is not defined : In the third Mi tiling pass, smaller (rectangles, w=0.4um) Mi tiles are not inserted.

- if SWI_THIRD_PASS_DUM_Mi is defined : In the third Mi tiling pass, smaller (rectangles, w=0.4um) Mi tiles are inserted. (this is the default behaviour)

The user can also specify in this switch, the orientation of Mi tiles (VERTICAL or HORIZONTAL) (the default is HORIZONTAL).

- **THIRD PASS TILES Mi WIDTH MANAGEMENT : Width third pass Mi tiles**

SWI_THIRD_PASS_DUM_Mi_W

The user can specify the width between inserting Mi tiles, whose default value is 0.4.

- **THIRD PASS TILES Mi SPACE TO Mi SHAPES MANAGEMENT : Distance between third pass Mi tiles and Mi shapes**

SWI_THIRD_PASS_DUM_Mi_S

The user can specify at which distance the Mi tiles should be placed with respect to the actual design Mi shapes, whose default value is 0.6.

- **THIRD PASS TILES Mi DENSITY MANAGEMENT : Density threshold below which third pass Mi tiles are inserted**

SWI_THIRD_PASS_DUM_Mi_T

The user can specify which is the Mi density below which rectangular Mi tiles should be inserted (local density on shifted windows, after second or first pass Mi tiling)

in case of difficulties to reach minimum Mi density process requirements, it is possible to set a threshold value higher than the minimum specified in DRM, in

order to "force" more tiles insertion, whose default value is 25.

- **FOURTH PASS TILESO Mi CHECKS MANAGEMENT : Enable fourth pass Mi tilingO (rectangles, w=0.14um)**

SWI_FOURTH_PASS_DUM_Mi

This feature can be switched on or off thanks to a calibre variable named SWI_FOURTH_PASS_DUM_Mi,it allows to increase Mi density after third, second or first pass.

- if SWI_FOURTH_PASS_DUM_Mi is not defined : In the fourth Mi tilingO pass, smaller (rectangles, w=0.14um) Mi tilesO are not inserted.

- if SWI_FOURTH_PASS_DUM_Mi is defined : In the fourth Mi tilingO pass, smaller (rectangles, w=0.14um) Mi tilesO are inserted. (this is the default behaviour)

The user can also specify in this switch, the orientation of Mi tilesO (VERTICAL or HORIZONTAL) (the default is VERTICAL).

- **FOURTH PASS TILESO Mi WIDTH MANAGEMENT : Width fourth pass Mi tilesO**

SWI_FOURTH_PASS_DUM_Mi_W

The user can specify the width between inserting Mi tilesO, whose default value is 0.1.

- **FOURTH PASS TILESO Mi SPACE TO Mi SHAPES MANAGEMENT : Distance between fourth pass Mi tilesO and Mi shapes**

SWI_FOURTH_PASS_DUM_Mi_S

The user can specify at which distance the Mi tilesO should be placed with respect to the actual design Mi shapes, whose default value is 0.1.

- **FOURTH PASS TILESO Mi DENSITY MANAGEMENT : Density threshold below which fourth pass Mi tilesO are inserted**

SWI_FOURTH_PASS_DUM_Mi_T

The user can specify which is the Mi density below which rectangular Mi tilesO should be inserted (local density on shifted windows, after third, second or first pass Mi tiling)

in case of difficulties to reach minimum Mi density process requirements, it is possible to set a threshold value higher than the minimum specified in DRM, in

order to "force" more tiles insertion, whose default value is 25.

- **FOURTH PASS TILESO Mi DENSITY MANAGEMENT UNDER BOND PAD : Density threshold below which fourth pass Mi tilesO are inserted under Bond Pad**

SWI_FOURTH_PASS_DUM_Mi_T_BOA

The user can specify which is the Mi density below which rectangular Mi tilesO should be inserted under Bond Pad (local density on shifted windows, after third, second or first pass Mi tiling)

in case of difficulties to reach minimum Mi density process requirements, it is possible to set a threshold value higher than the minimum specified in DRM, in

order to "force" more tiles insertion, whose default value is 25.

- **FIFTH PASS TILESO Mi CHECKS MANAGEMENT : Enable fifth pass Mi tilingO (rectangles, w=0.1um)**

SWI_FIFTH_PASS_DUM_Mi

This feature can be switched on or off thanks to a calibre variable named SWI_FIFTH_PASS_DUM_Mi,it allows to increase Mi density after fourth, third, second or first pass.

- if SWI_FIFTH_PASS_DUM_Mi is not defined : In the fifth Mi tilingO pass, smaller (rectangles, w=0.1um) Mi tilesO are not inserted.

- if SWI_FIFTH_PASS_DUM_Mi is defined : In the fifth Mi tilingO pass, smaller (rectangles, w=0.1um) Mi tilesO are inserted. (this is the default behaviour)

The user can also specify in this switch, the orientation of Mi tilesO (VERTICAL or HORIZONTAL) (the default is VERTICAL).

- **FIFTH PASS TILESO Mi WIDTH MANAGEMENT : Width fifth pass Mi tilesO**

SWI_FIFTH_PASS_DUM_Mi_W

The user can specify the width between inserting Mi tilesO, whose default value is 0.1.

- **FIFTH PASS TILESO Mi SPACE TO Mi SHAPES MANAGEMENT : Distance between fifth pass Mi tilesO and Mi shapes**

SWI_FIFTH_PASS_DUM_Mi_S

The user can specify at which distance the Mi tilesO should be placed with respect to the actual design Mi shapes, whose default value is 0.1.

- **FIFTH PASS TILESO Mi DENSITY MANAGEMENT : Density threshold below which fifth pass Mi tilesO are inserted**

SWI_FIFTH_PASS_DUM_Mi_T

The user can specify which is the Mi density below which rectangular Mi tilesO should be inserted (local density on shifted windows, after fourth, third, second or first pass Mi tiling)

in case of difficulties to reach minimum Mi density process requirements, it is possible to set a threshold value higher than the minimum specified in DRM, in

order to "force" more tiles insertion, whose default value is 25.

- **FIFTH PASS TILESO Mi DENSITY MANAGEMENT UNDER BOND PAD : Density threshold below which fifth pass Mi tilesO are inserted under Bond Pad**

SWI_FIFTH_PASS_DUM_Mi_T_BOA

The user can specify which is the Mi density below which rectangular Mi tilesO should be inserted under Bond Pad (local density on shifted windows, after fourth, third, second or first pass Mi tiling)

in case of difficulties to reach minimum Mi density process requirements, it is possible to set a threshold value higher than the minimum specified in DRM, in

order to "force" more tiles insertion, whose default value is 25.

Note: In all the switch description below Mi can be MZ6,MZ7, ...(Metal tiling; thick metals) Name of the variable varies accordingly

- **FIRST PASS TILES Mi CHECKS MANAGEMENT : Enable first pass Mi tiling (0.9x0.90um2 squares).**

SWI_FIRST_PASS_DUM_Mi

This feature can be switched on or off thanks to a calibre variable named SWI_FIRST_PASS_DUM_Mi

- if SWI_FIRST_PASS_DUM_Mi is not defined : In the first Mi tiling pass, square shaped (0.9x0.90um2 squares) Mi tiles are not inserted.

- if SWI_FIRST_PASS_DUM_Mi is defined : In the first Mi tiling pass, square shaped (0.9x0.90um2 squares) Mi tiles are inserted. (this is the default behaviour)

- **FIRST PASS TILES Mi WIDTH MANAGEMENT : Width third pass Mi tiles (min=0.78 to respect the rule DMi.A.1)**

SWI_FIRST_PASS_DUM_Mi_W

The user can specify the width between inserting Mi tiles, whose default value is 0.9.

- **FIRST PASS TILES Mi SPACE TO Mi SHAPES MANAGEMENT : Distance between first pass Mi tiles and Mi shapes.**

SWI_FIRST_PASS_DUM_Mi_S

The user can specify at which distance the Mi tiles should be placed with respect to the actual design Mi shapes, whose default value is 1.5.

- **FIRST PASS TILES Mi DENSITY MANAGEMENT : Density threshold below which first pass Mi tiles are inserted**

SWI_FIRST_PASS_DUM_Mi_T

The user can specify which is the Mi density below which Mi tiles should be inserted (local density on shifted windows), whose default value is 25.

- **TILES ALUCAP CHECKS MANAGEMENT : Enable AP tiling.**

SWI_DUM_ALUCAP

This feature can be switched on or off thanks to a calibre variable named SWI_DUM_ALUCAP

- if SWI_DUM_ALUCAP is not defined : AP tiles are not inserted.

- if SWI_DUM_ALUCAP is defined : AP tiles are inserted. (this is the default behaviour)

- **TILES ALUCAP DENSITY MANAGEMENT : Density threshold below which L shaped AP tiles are inserted.**

SWI_DUM_ALUCAP_T

The user can specify which is the AP density below which AP tiles should be inserted (local density on shifted windows), whose default value is 15.

- **INDUCTOR TILING MANAGEMENT :**

SWI_FIRST_PASS_DUM_IND

A procedure to generate dummies in the density transtion ring of all inductors from OD level to

last metal. (Only available in RF DKs).

2.4 Antenna Switches

- **RECOMMENDED RULES**
  - \+ RECOMMEND

"Check Poly / Well capacitors specific recommended rules." The default is set to "NO".

This switch checks a specific rule on Poly / Well capactitors: poly plate of a Poly / Well capacitor should be connected to an effective diod at Metal1 level.

3 - RULES ABREVIATION MEANING

The default DRC functionality will include the support of the sense layer, which will define a DRC violation for any metal (defined by sense layer per metal) which is overlapping the sense layer (and PO and OD layers). The devices that are marked in schematic with the sense option will be required to LVS the sense layer(s) to ensure their presence for the specific device. This check is intended to block metal routing over sensitive analog devices.

The DRM specified rules will be placed in one deck and the antenna rules will be placed in separate decks.

As far as density checks:

- minimum density checks will be managed by a switch (name : DENSITY_CHECK) so that tkit user can turn on or off the design rule checks corresponding to minimum density requirements,

- maximum density checks are not included in this switch.

MRC (methodology) checks are supported; they are aimed at checking design rules which are related to masks but are not explicitly referenced in DRM (example: layers usage)

CAD checks are supported: they are aimed at checking design rules related to CAD tools/ features usage. They can be easily switched off for in coming controls at fab

ERC (electrical) checks are included in LVS deck.

MRC, CAD and ERC rules are intended to check rules that are not considered hard design rules but aimed at highlighting not good practice designs.

NOTE: As far as SRAM memories designed in TSMC environment (non alliance memories) and that cmos065 common technology kit users want to include in their design, the common technology kit must provide a feature by which all waived design rule violations inside memory array do not produce DRC errors. On the other hand for those memories which have been designed with the common technology kit (Alliance memories), the Alliance standard waiving mechanism is used (no exclusion from DRC).

For the non Alliance memories, an exclusion scheme similar to the one proposed in TSMC DRC rule files is used. Criterion for identification of non Alliance memories: Presence of (SRM, drawing) layer or (MKR, sramdmy) layer and absence of (MKR, waiver) layer.

When this criterion is fulfilled an "exclusion window" is created (no DRC checks done inside this window) for all mask layers where "known" design rules violations are present.

4 - DEVICE PROPERTIES

Device	Terminals	Parameters Checked [%variation allowed]	Merging Definition	Recognition Shape Required
MOS Devices	d, g, s, b	w[1 grid or 1%] l [0 grid, 0%] sense (on/off) (esu, edu for non silicided MOS: 1%)	Default: add all widths with same l (and esu, edu for non silicided MOS) that are in parallel	
DIODES	plus, minus	a [1%] p[1%]	add all areas and peris for parallel diodes	Optional DIODMY layer. This layer optional for all diodes (they should extract w/ or w/o layer)
nmos in DEEP NWEL (IPW)				NOTE: This device will LVS as base MOS device + DEEP NWELL diode. This diode should be placed at the level in hierarchy that matches between layout and schematic... The parameters of this diode can be LVSed or not (switch in LVS)
diode between isolated Pwell and DNW	plus, minus	a [1%, extracted in LPE] p [1%, extracted in LPE] Switch to disable area and peri comparison		Device parameter comparison during LVS can be turned ON or OFF
RESISTORS	plus, minus, minus,	w [0 grid or 0%] l [0 grid or 0%] sense (on/off)	Series: Add all l values for devices that have same w value. Parallel: add all w values for devices that have same w and same l values	rpo resistors do not require layer (rpo defines resistor body)
Metal RESISTORS	plus, minus	width [0 grid or 0%] length [0 grid or 0%] metal [0%]	Series: dd all l values for devices that have same w value. Parallel: add all w values for devices that have same w and same l values	Purpose res drawn to define body of resistor... (metal layer with purpose res over metal layer)
Stacked metal fringe capacitor	a_po, b_od, shod, shop, sub	nf [0%] l [1%]	Series: NONE Parallel: NONE	Recognition layer : use of fringeC purpose

Device	Terminals	Parameters Checked [%variation allowed]	Merging Definition	Recognition Shape Required
elementary fringe capacitor (mono layer fringe)	Plus minus	l [1%] fs [1%] metal [0%]	Series: NONE Parallel: add all l values if same l , metal and fs	Recognition layer : use of fringeC purpose
Striped stacked metal	Plus minus	carea [1%] cperi [1%] toplayer [0%] botlayer [0%]	Series: NONE Parallel: add all carea, cperi values if same toplayer and botlayer	Recognition layer : use of plateC purpose
elementary plate capacitor(two consecutive metal layers)	Plus minus	carea [1%] cperi [1%] toplayer [0%]	Series: NONE Parallel: add all carea, cperi values if same toplayer	Recognition layer : use of plateC purpose
MOS oxide capacitor (Ex:N+ PO/ Nwell)	Plus minus bulk	carea [1%] cperi [1%] sense (on/off)	Series: NONE Parallel: add all carea, cperi values	No recognition layer required.
BIPOLARS	c b e (sub)	ae (1%) pe (1%) sense (on/off)	Series: None Parallel: add all ae and pe values	Use BJT layer. Substrate PNP has 3 pins Vertical NPN (using DNW) has 4 pins
TESTPOINTS	Probe	area [1%] peri[1%]	Not applicable	described in DRM