CMOS ADCs towards 100 GS/s and beyond

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***Abstract* — The implementation of a 64x time-interleaved ADC in 32nm CMOS SOI is analyzed. Measurement results confirm 33 dB SNDR up to 19.9 GHz at 90 GS/s and 1.2V supply. Architecture details and analysis show insights into limitations and potentials of the chosen architecture. In particular the input bandwidth is of concern for ADCs at more than 64 GS/s, as a larger number of sampling switches increases the parasitic load and reduces the input bandwidth. Insights on a simplified analysis of interleaver structures and existing solutions to bandwidth issues are highlighted and show a path to extend the sampling speed of CMOS ADCs beyond 100 GS/s.**

***Index Terms* — ADC, time-interleaving, inline demux sampling, SAR, successive approximation, IEEE 802.3bs, ITU-OTU5.**

I. Introduction

Time-interleaved analog-to-digital converters (ADCs) have been gaining popularity in the past few years for achieving high sampling speeds required by ever faster communication systems. Applications such as long-haul optical communication standards ITU-OTU4/5 and recent electrical communication standards such as 400 Gb/s Ethernet IEEE 802.3bs require high-performance ADCs.

Several designs have been shown to achieve more than 30 GS/s in CMOS [1−4], all of them combine time interleaving to achieve high sampling rates with a large array of power-efficient sub-ADCs. As these ADCs feature 6−8 bit resolution, the successive-approximation register (SAR) architecture showed to be well suited. SAR ADCs are generally simple in their architecture and often require little calibration while being very power efficient and suitable for digital CMOS process implementation. Their main drawback is a limited sampling speed as one conversion of a sample in a SAR ADC requires a number of conversion steps on the order of the designed resolution. Therefore pipelined ADCs are sometimes used when a low number of sub-ADCs are desired [5]. Techniques to improve conversion speeds of SAR ADCs have been shown [6−8], which result in a significant smaller number of sub-ADCs required for a given sampling speed. A smaller number of sub-ADCs facilitates calibration and saves significant silicon area, which simplifies the interleaving layout.

As technology trends show the need for sampling rates beyond 100 GS/s at 8 bit resolution, further improvement to current state of the art is necessary. Two of the main challenges at these speeds are the input bandwidth and sampling jitter. While it is relatively straightforward to boost the sampling rate, it is not easy to maintain a reasonable input bandwidth of at least a quarter of the sampling rate. Furthermore, sampling jitter needs to drop to below 50 fs RMS to maintain high SNDR at high input frequencies. High input bandwidth can only be achieved by optimizing the input sampling architecture and network, while sampling jitter can be reduced by increasing the power consumption of the clock driving circuitry.

Section II of this paper shows the implementation of a low-power ADC architecture that achieves 90 GS/s at 8-bit resolution. Design decisions and circuit details are outlined.

The following section outlines on-going work to increase the sampling speed beyond 100 GS/s with an increased input bandwidth.

II. 90 GS/s 8-bit Time-Interleaved SAR ADC

Figure 1 shows an overview of the ADC. The input to the ADC is differential (2×50 • terminated) and connected to the interleaver switches without buffers. Four clock

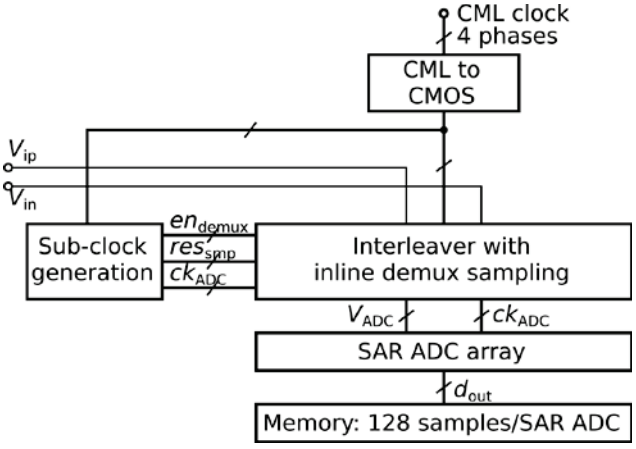

Fig. 1. Overview of the 64x interleaved SAR ADC running up to 90 GS/s [1].

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phases drive the interleaver, which have to be at a quarter of the sampling speed (f_s) and exhibit very low jitter. Lower speed clocks used in the sampler and sub-ADCs are derived from these four clock phases.

The sampled analog voltage outputs of the interleaver V_{ADC} are connected to an array of 64 SAR ADCs, each running at more than 1 GS/s. Due to limited silicon area, data is stored in a snapshot memory and not taken off chip in real time.

The sampling scheme used in this ADC is shown in Fig. 2 in a single-ended configuration. The input is connected to four sampling switches, each of them in series with a set of inline demux switches. During sampling, one of the inline demux switches connects the sampling switch to one of the sampling capacitors C_s. The use of inline demux switches increases the hold time of the sample by approx. a factor of four while keeping the number of high precision clocks low. During the hold phase, the sampled voltage on C_s is buffered and connected to the sampling capacitor of one of four SAR ADCs, $C_{s,ADC}$. The corresponding timing diagram is shown at the bottom of Fig. 2. It is important to note that the clocks on the inline demux switches, $\bullet_{xy}$, are rising before the active clock edge of $\bullet_x$ and falling after $\bullet_x$ in order to prevent any impact of $\bullet_{xy}$ on the sampling time, thus significantly relaxing the clock precision constraints on $\bullet_{xy}$.

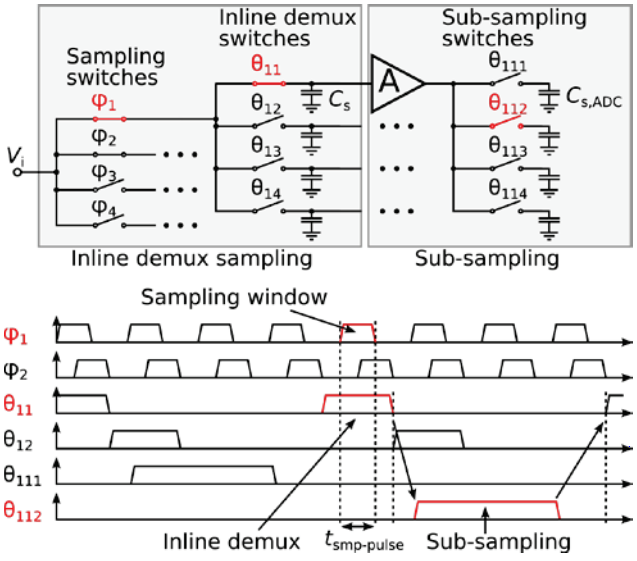

Fig. 2. Inline demux sampling, as used in the 90 GS/s ADC reduces the number of critical sampling clocks to four [1].

The choice of the input sampling architecture provides a hold time that is long enough to enable sub-sampling, reduces the critical clock phases to four with a 50% duty cycle and achieves a bandwidth of about one quarter of the sampling speed, as required by e.g. ITU-OTU4.

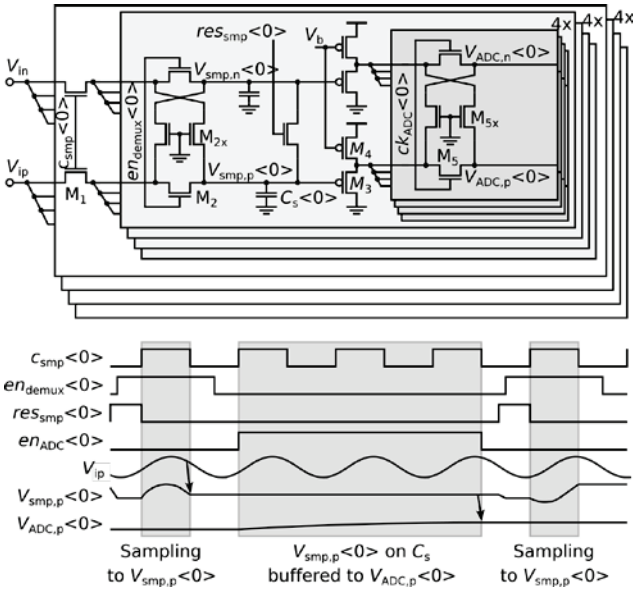

Fig. 3. Implementation of 64x interleaved sampling frontend with inline demux sampling [1].

The circuit schematic of the interleaver is depicted in Fig. 3. The inline demux switches (M_2) are implemented with feed-through compensation to prevent distortion of the sampled voltage during the hold time. No feed-through compensation is used in the sampling switches (M_1), as the additional transistors would increase parasitic capacitance and thus reduce the bandwidth. Source followers (M_3, M_4) are used to buffer the sampled voltage, as they provide high linearity and good bandwidth to enable fast sub-sampling.

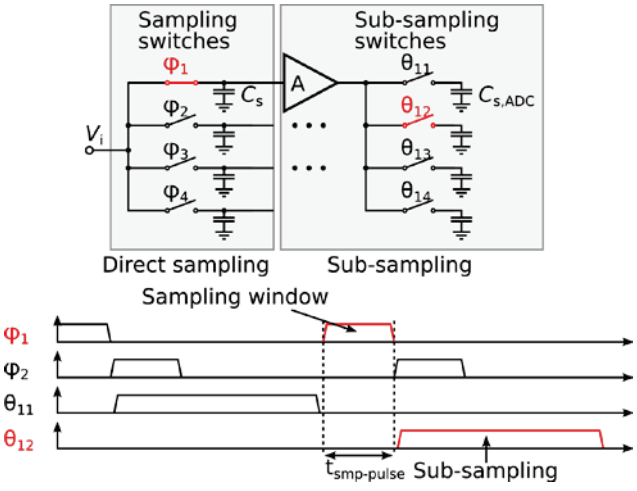

Fig. 4. Direct sampling, as e.g. used in [1].

Analyzing the bandwidth of different inline demux sampling configurations and direct sampling configurations, shown in Fig. 4, was conducted in [4]. The model simply replaces each switch with a model based on a capacitor at the input and output of the switch and a switch resistor, as shown in Fig. 5. Resistance and capacitance can be coupled to the f_T of the process, adjusting for parasitic capacitors and resistors. A detailed analysis is found in [4].

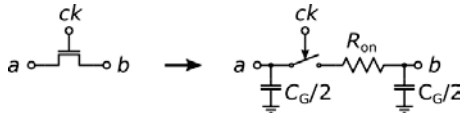

Fig. 5. Each transistor in the interleaver is replaced by parasitic capacitors and a channel resistor.

A comparison of direct and inline demux sampling with different numbers of switches for an implementation of a > 64 GS/s ADC with respect to hold time, analog input bandwidth and complexity of the input clocking is shown in Fig. 6. The analysis assumes feed-through compensation in the sampling switches directly connected to the sampling capacitors (Fig. 3).

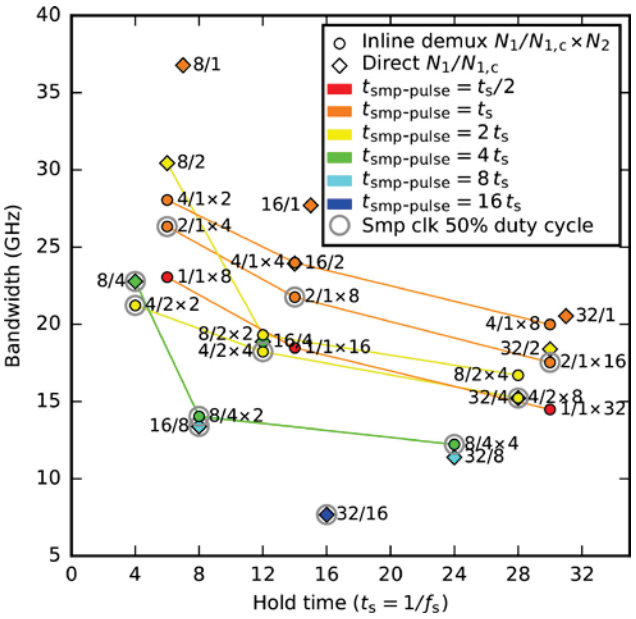

Fig. 6. Comparison of different interleaver architectures based on a simplified RC model of the sampling switches for a sampling capacitor of 32 fF, 50 • input resistance, an effective f_T of 210 GHz that includes the effects of parasitic capacitance for a process with f_T of 300 GHz. N_1 is the number of sampling switches, $N_{1,c}$ the number of activated sampling switches at each time and N_2 the number of inline demux switches. The hold time on the x-Axis is given in multiples of the sampling period t_s. [4].

The implementation in Fig. 3 is shown as the 4/2x4 design point, and results in the highest bandwidth for a $f_s/4$ sampling clock. Its 50% duty cycle clock relaxes complexity for the clock generation.

A photo of the chip is seen in Fig. 7. The ADC was implemented on 470 x 340 µm^2 in 32nm CMOS SOI. At 90 GS/s and 1.2 V supply it consumes 667 mW and achieves more than 36 dB up to 6.1 GHz and more than 33 dB up to 19.9 GHz. The 3 dB frequency was measured to be at approx. 22 GHz [4]. This is higher than predicted, but T-coils in the input path eliminate part of the input capacitance, resulting in higher bandwidth.

Simulation results based on extracted layout of a new SAR ADC with different architecture in 14nm FinFET technology show promising results; the same sampling speed as in 32nm CMOS SOI can be achieved at significantly more SNDR. Almost 2 ENOB more at approx. 3mW/GSps were simulated over corners at 0.8 V supply.

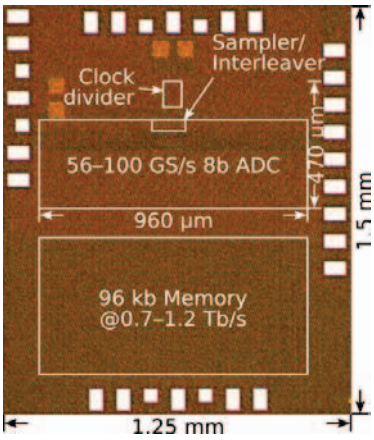

Fig. 7. Die photo of the 90 GS/s ADC implemented in 32nm CMOS SOI [4].

III. Strategies to Achieve >100 GS/s

If Fig. 6 is applied to an ADC with twice the nominal sampling frequency of [4], the hold time in t_s doubles as the hold time in seconds needs to remain the same to allow for sufficient sub-sampling. Furthermore, the maximum clock speed that can be achieved on-chip will remain the same, thus a solution with similar clock frequencies is desirable. These requirements restrict interleaver architectures to hold times above 24 t_s and with at least 4 concurrently active sampling switches (green and cyan). The highest shown 3-dB frequency based on the analysis above is found in the 32/4 configuration (hidden by the 4/2x8 configuration). This means 32 direct sampling switches in parallel, 4 of them active at each point in time. Not only is the 3 dB bandwidth too low for most applica-

tions, but also the clocking is harder to achieve. The latter could likely be solved with e.g. clock gating as applied in [9], but the former requires different approaches.

Given that the overall SNDR of the ADC in Fig. 1 is limited by the sub-ADC, an improved sub-ADC as simulated in 14nm FinFET can boost the SNDR of the interleaved ADC. This means that the same SNDR that was measured at the 3-dB frequency in the 32nm implementation will be measured at a much higher frequency and signal attenuation with a higher resolution sub-ADC.

Assuming that the higher resolution of the sub-ADC simulated in 14nm FinFET yields one additional bit of effective resolution (6 dB SNDR) if combined with an interleaver as depicted in Fig. 3 and that neither jitter nor bandwidth mismatch limits the ADC performance, one can look at the 9-dB frequency as a frequency band of interest instead of a 3-dB frequency band.

The same analysis as that which was used to predict the bandwidth in Fig. 6 can be applied for a 9-dB frequency point. The resulting plot is shown in Fig. 8.

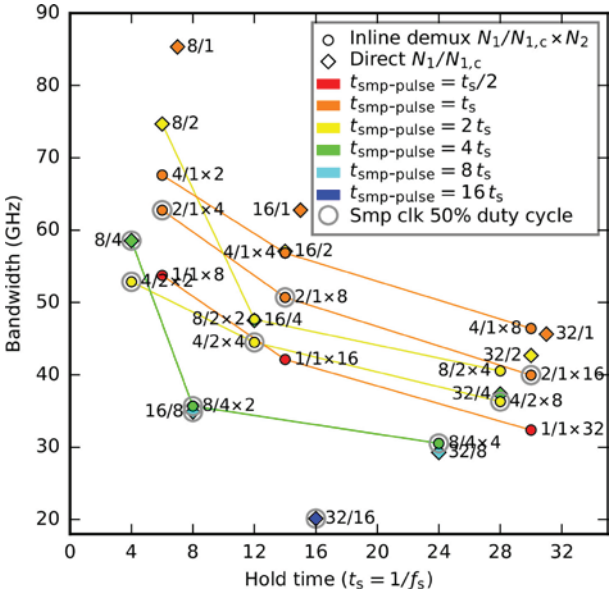

Fig. 8. Analysis of the 9-dB bandwidth for the same assumptions as in Fig. 6.

Not only can it be seen that a much higher virtual bandwidth of interest can be achieved with the ADC in its current configuration and with the current sampling speed, but also the 32/4 sampling configuration shows a 9-dB bandwidth of more than 35 GHz, which is sufficient for ADCs of approx. 128 GS/s if the signal of interest is between DC and $f_s/4$. Also the 8/4x4 configuration, which features a 50% duty cycle clock by doubling the structure seen in Fig. 3 with 8 instead of 4 sampling channels results in more than 30 GHz bandwidth. The 32/4 configuration yields a higher bandwidth compared to the 8/4x4 at the expense of more complex clocking, since 32 critical clock edges with 1/8 duty cycle are required. The 8/4x4 configuration trades lower, but potentially still sufficient bandwidth for much simpler clocking, as only 8 clock phases at 50% duty cycle are required. The additional bandwidth gained at -9dB is higher for the 32/4 configuration, because there is one switch less in the sampling path and therefore one pole less in the system, resulting in a less steep amplitude roll-off with higher input frequencies.

Further measures can be taken to boost the bandwidth: a front-end buffer can be used or the input resistor termination can be lowered to present a lower input impedance to the sampling switches [1].

IV. Conclusion

The paper analyzes a time-interleaved SAR ADC architecture for sampling rates of 64 GS/s and beyond with measured silicon in 32nm CMOS SOI. Insights into the architecture reveal potential to implement ADCs of more than 100 GS/s in 14nm FinFET with adequate bandwidth.

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