HPA_LP MODELS (NHPALP, PHPALP)

1. CONDITIONS OF EXTRACTION

- Maturity: Preliminary
- Model parameters extraction based on lot : Q552GKN
- Geometrical extraction domain:
  - Drawn gate length : 10.0 ≥ L ≥ 0.14 µm
  - Drawn transistor width : 10 ≥ W ≥ 0.15 µm
- Temperature extraction domain: -40 ˚C to 150 ˚C
- Bias extraction domain:
  - Gate bias: 0 ≤ |VGS| ≤ 1.32 V (VDD + 10%)
  - Drain bias: 0 ≤ |VDS| ≤ 1.32 V (VDD + 10%)
  - Bulk bias: 0 ≤ |VBS| ≤ 1.32 V (VDD + 10%)

2. CONDITIONS OF SIMULATION

- Temperature: 25 ˚C
- Currents:

  IDLIN = Ids at Vgs = 1.2 V, Vds = 50 mV and Vbs = 0 V

  ION = Ids at Vgs = 1.2 V, Vds = 1.2 V and Vbs = 0 V

  IOFF = Ids at Vgs = 0 V, Vds = 1.2 V and Vbs = 0 V

  IG_ON = Igs at Vgs = 1.2 V and Vd= Vs = Vb = 0 V

  IG_OFF = Igs at Vgs =Vbs = 0 V and Vds = 1.2 V
- Threshold voltage in linear and saturation regime

  VTLIN is Vgs value at Vds = 50 mV, Vbs = 0 V and Ids= 40*W/L nA.

  VTSAT is Vgs value at Vds = 1.2 V, Vbs = 0 V and Ids= 40*W/L nA.
- Current derivatives:

$$Gm = \frac{\partial}{\partial V_{gs}} Ids$$ at Vgs = VTLIN + 0.2 V, Vds = 0.6 V and Vbs = 0 V

$$Gd = \frac{\partial}{\partial V_{ds}} Ids$$ at Vgs = VTLIN + 0.2 V, Vds = 0.6 V and Vbs = 0 V

Analog gain = Gm/Gd

- Gate Capacitances:

  CGGINV = CGG at Vgs = 1.2 V, Vds = 0 V and Vbs = 0 V

  CGD_0V = CGD at Vgs = 0 V, Vds = 0 V and Vbs = 0 V

  $$CGGMEAN = \frac{1}{VDD} \cdot \int_{0}^{VDD} CGG \times dVgs$$ with VDD = 1.2 V and Vbs = 0 V

  TAU = CGGMEAN*VDD/ION

- Diode Capacitances:

  CBD OFF = CBD at Vgs = 0 V, Vds = 1.2 V and Vbs = 0 V

  Note: the area and perimiters of source/drain junction diodes used for simulation are defined with the the minimum poly-to-active distance specified in the DRM.

- Transition frequency:

  FT = frequency for which the small signal current gain H_{21} is 0 dB (i.e. $\left|\frac{I_d}{I_g}\right|$ = 0 dB).

3. MAIN ELECTRICAL CHARACTERISTICS OF NMOS HPA_LP TRANSISTORS

PARAMETERS	HPALP_TT	HPALP_SS	HPALP_FF	units
N-channel transistors (nhpalp)				
VTLIN W=1/L=10.0	91	110	71	mV
IDLIN W=1/L=10.0	1.54e-06	1.44e-06	1.64e-06	A
VTSAT W=1/L=10.0	87	107	68	mV
ION W=1/L=10.0	1.63e-05	1.50e-05	1.78e-05	A
VTLIN W=1/L=0.14	-16	16	-53	mV
IDLIN W=1/L=0.14	9.24e-05	8.33e-05	1.03e-04	A
VTSAT W=1/L=0.14	-101	-54	-162	mV
ION W=1/L=0.14	7.51e-04	6.94e-04	8.12e-04	A
IOFF W=1/L=0.14	2.79e-06	1.12e-06	6.64e-06	A
IG_ON W=1/L=0.14	3.68e-11	1.78e-11	7.69e-11	A
IG_OFF W=1/L=0.14	1.32e-12	6.35e-13	2.78e-12	A
FT W=1/L=0.14	6.33e+10	5.95e+10	6.77e+10	Hz
CGGinv W=1/L=0.14	2.39e-15	2.44e-15	2.35e-15	F
CGGmean W=1/L=0.14	2.29e-15	2.32e-15	2.27e-15	F
CGD 0V W=1/L=0.14	8.75e-16	7.90e-16	9.31e-16	F
CBD OFF[a] W=1/L=0.14	4.02e-16	4.42e-16	3.56e-16	F
Tau W=1/L=0.14	3.7	4.0	3.4	ps
Gm W=1/L=0.14	3.46e-04	3.11e-04	3.79e-04	S
Gd W=1/L=0.14	2.37e-05	1.98e-05	2.78e-05	S
Gain W=1/L=0.14	1.46e+01	1.57e+01	1.37e+01	
VTLIN W=0.15/L=0.14	52	86	18	mV
IDLIN W=0.15/L=0.14	1.46e-05	1.29e-05	1.66e-05	A
VTSAT W=0.15/L=0.14	-18	21	-63	mV
ION W=0.15/L=0.14	1.18e-04	1.06e-04	1.30e-04	A
IOFF W=0.15/L=0.14	7.19e-08	2.29e-08	2.25e-07	A
FT W=0.15/L=0.14	5.73e+10	5.36e+10	6.14e+10	Hz

Table 1: Main electrical characteristics for NMOS

a. Value coresponding to the minimum poly-to-acvtive distance specified in the DRM

4. MAIN ELECTRICAL CHARACTERISTICS OF PMOS HPA_LP TRANSISTORS

PARAMETERS	HPALP_TT	HPALP_SS	HPALP_FF	units
P-channel transistors (phpalp)				
VTLIN W=1/L=10.0	192	212	172	mV
IDLIN W=1/L=10.0	5.00e-07	4.66e-07	5.34e-07	A
VTSAT W=1/L=10.0	188	208	168	mV
ION W=1/L=10.0	5.07e-06	4.63e-06	5.55e-06	A
VTLIN W=1/L=0.14	85	117	52	mV
IDLIN W=1/L=0.14	3.08e-05	2.77e-05	3.42e-05	A
VTSAT W=1/L=0.14	-23	22	-74	mV
ION W=1/L=0.14	3.63e-04	3.17e-04	4.17e-04	A
IOFF W=1/L=0.14	4.68e-07	1.72e-07	1.23e-06	A
IG_ON W=1/L=0.14	3.51e-12	1.66e-12	7.45e-12	A
IG_OFF W=1/L=0.14	1.45e-13	6.80e-14	3.12e-13	A
FT W=1/L=0.14	3.60e+10	3.20e+10	4.06e+10	Hz
CGGinv W=1/L=0.14	2.33e-15	2.37e-15	2.28e-15	F
CGGmean W=1/L=0.14	2.06e-15	2.07e-15	2.04e-15	F
CGD 0V W=1/L=0.14	5.04e-16	4.53e-16	5.72e-16	F
CBD OFF[a] W=1/L=0.14	3.10e-16	3.42e-16	2.76e-16	F
Tau W=1/L=0.14	6.8	7.8	5.9	ps
Gm W=1/L=0.14	1.75e-04	1.57e-04	1.96e-04	S
Gd W=1/L=0.14	1.45e-05	1.18e-05	1.78e-05	S
Gain W=1/L=0.14	1.21e+01	1.33e+01	1.10e+01	
VTLIN W=0.15/L=0.14	121	155	86	mV
IDLIN W=0.15/L=0.14	5.35e-06	4.74e-06	6.04e-06	A
VTSAT W=0.15/L=0.14	20	65	-30	mV
ION W=0.15/L=0.14	6.18e-05	5.26e-05	7.27e-05	A
IOFF W=0.15/L=0.14	2.72e-08	8.87e-09	8.15e-08	A
FT W=0.15/L=0.14	3.24e+10	2.86e+10	3.68e+10	Hz

Table 2: Main electrical characteristics for PMOS

a. Value coresponding to the minimum poly-to-acvtive distance specified in the DRM

5. ELECTRICAL BEHAVIOR VERSUS GATE LENGTH AND CHANNEL WIDTH FOR NMOS HPA_LP TRANSISTORS

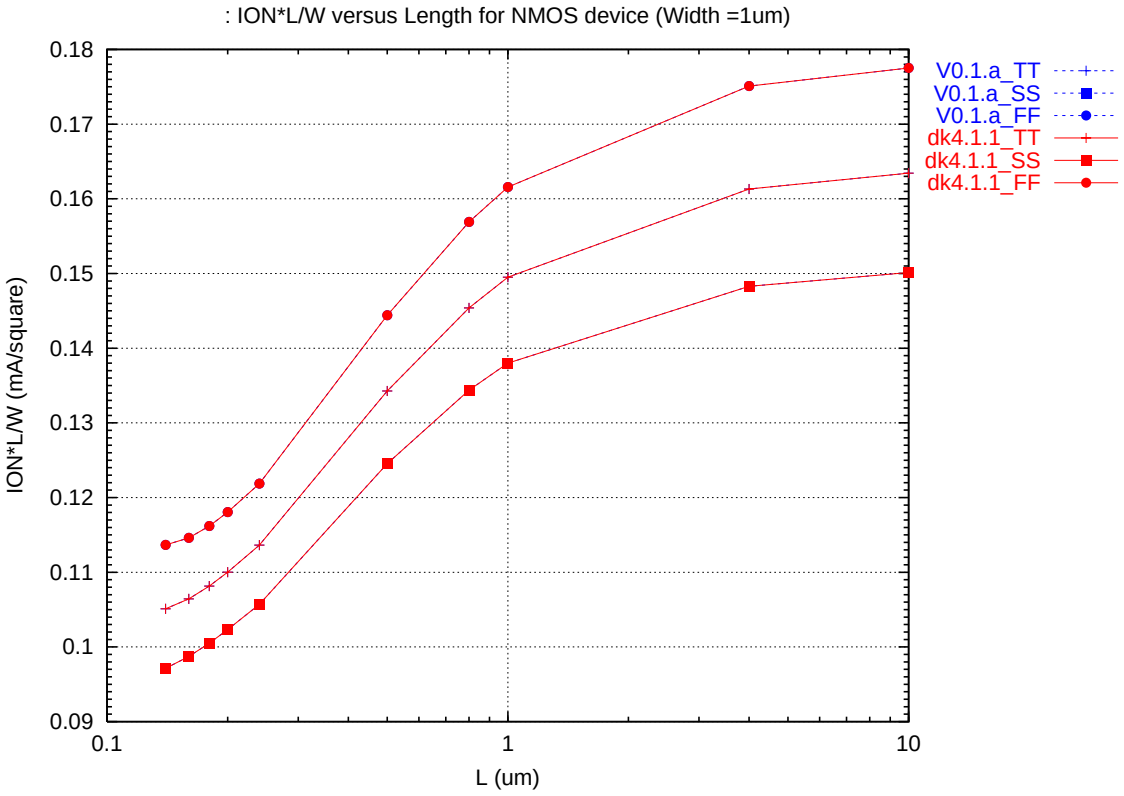

Figure 1 : ION/❑=ION*L/W versus drawn gate length for NMOS HPA_LP transistors (W = 1 µm)

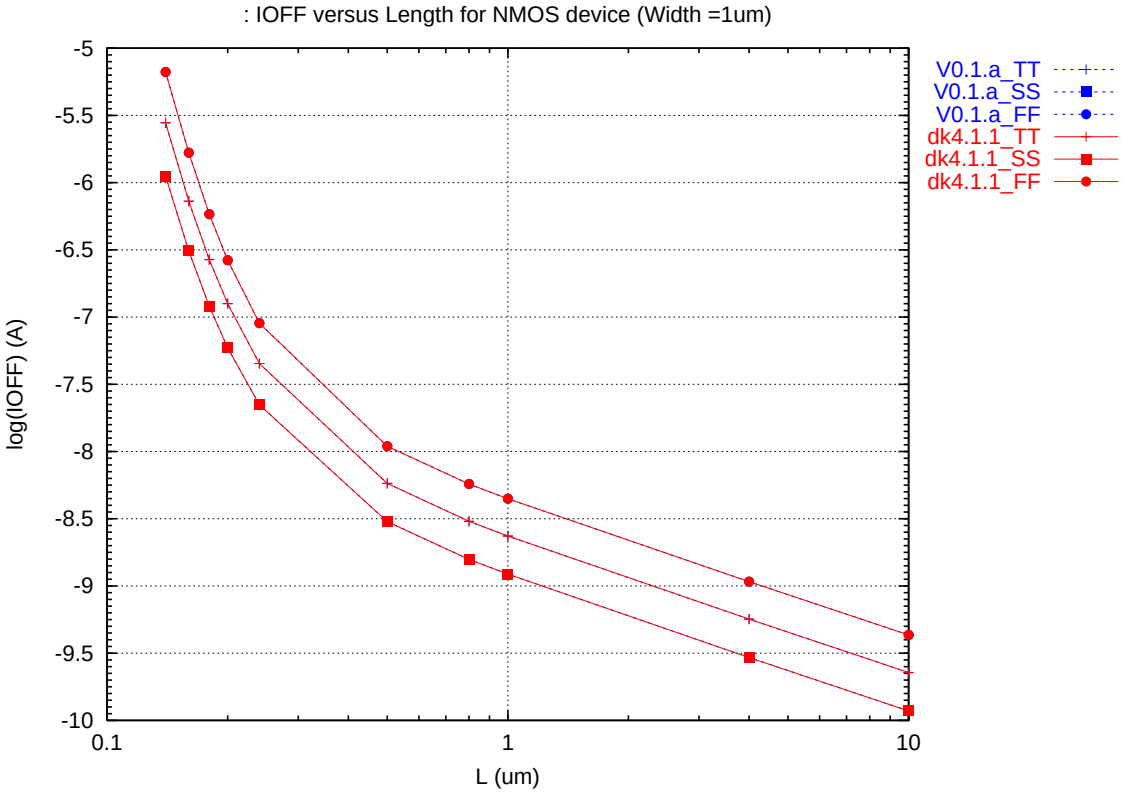

Figure 2 : IOFF versus drawn gate length for NMOS HPA_LP transistors (W = 1 µm)

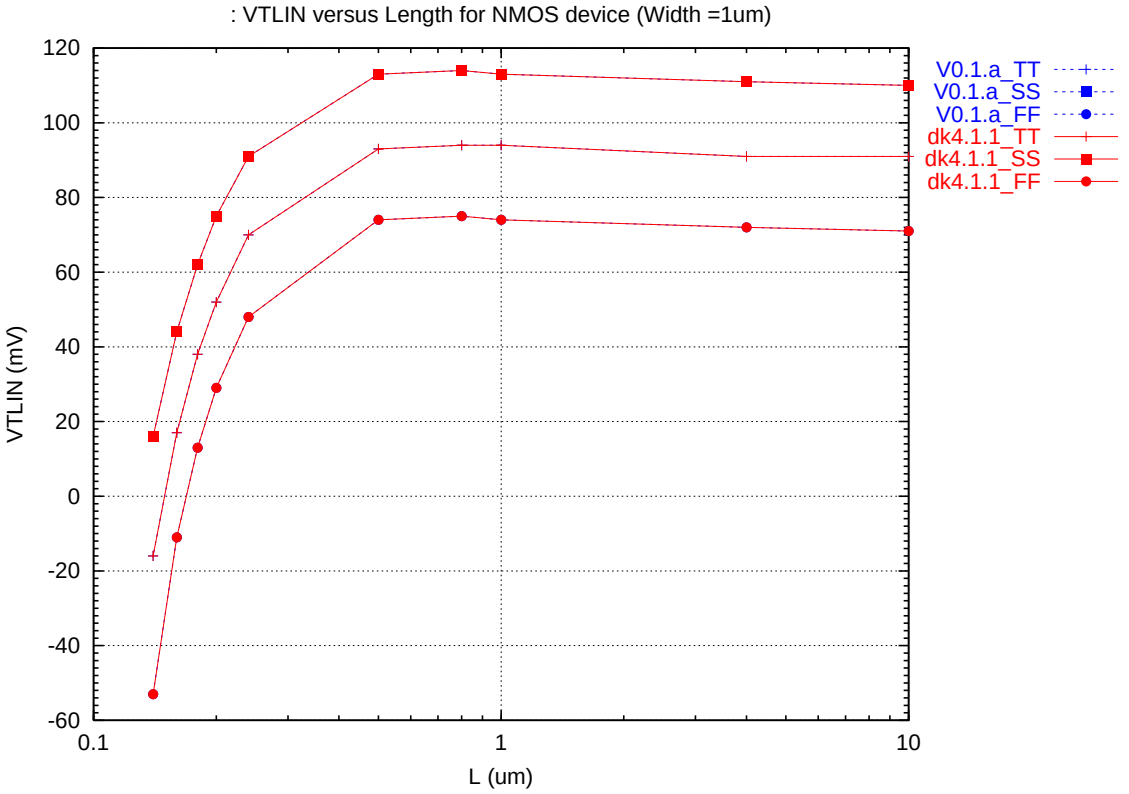

Figure 3 : Threshold voltage VTLIN versus drawn gate length for NMOS HPA_LP transistors (W = 1 µm)

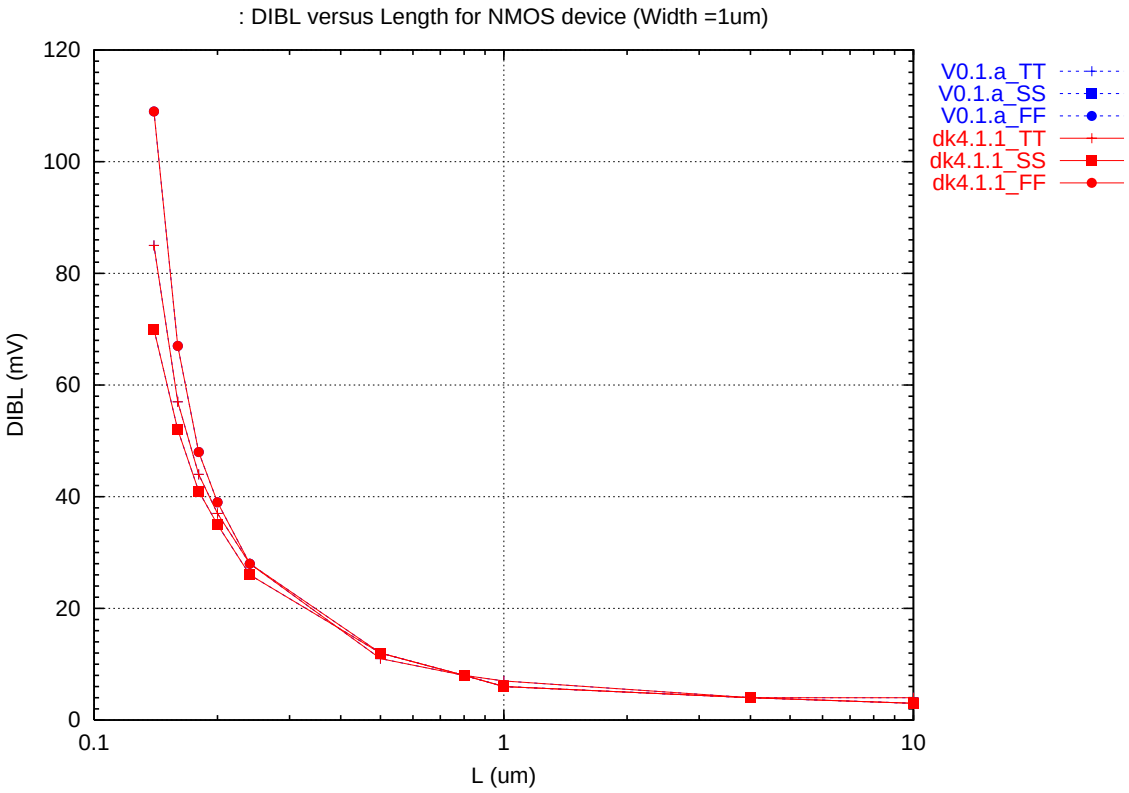

Figure 4 : DIBL= VTLIN-VTSAT versus drawn gate length for NMOS HPA_LP transistors (W = 1 µm)

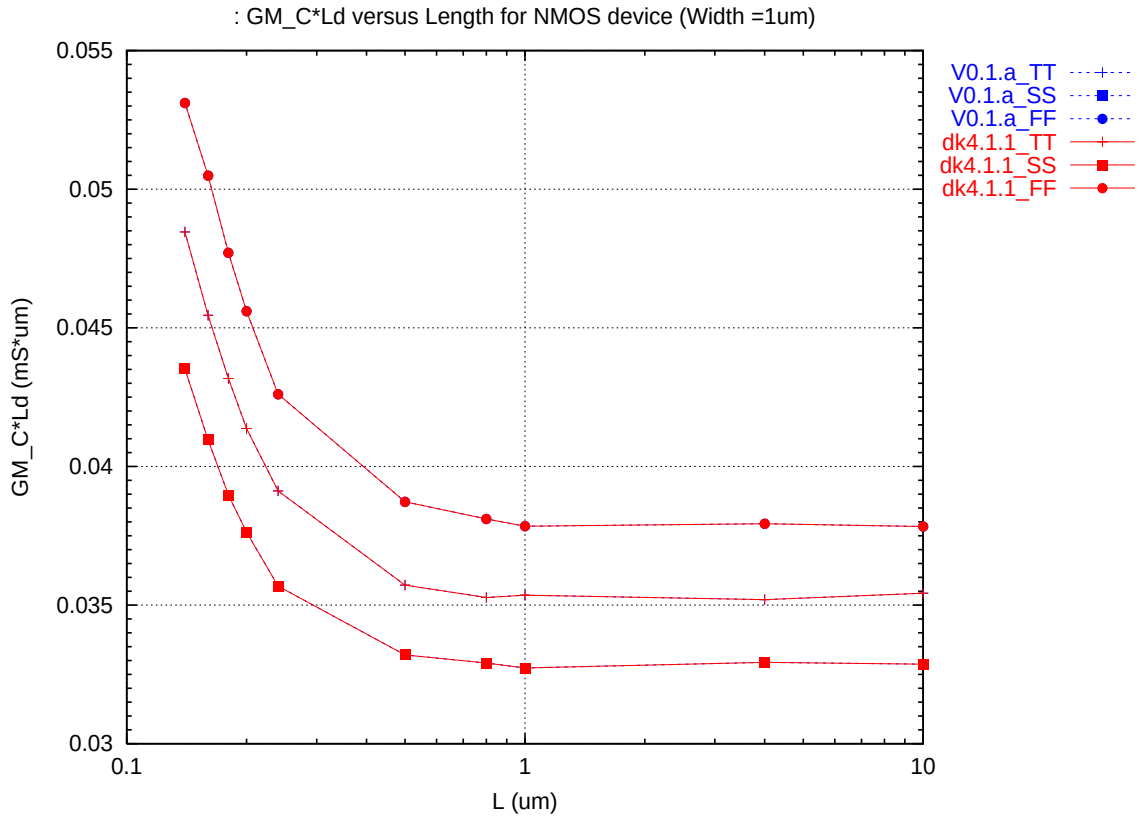

Figure 5 : GM*Ld versus drawn gate length for NMOS HPA_LP transistors (W = 1 µm)

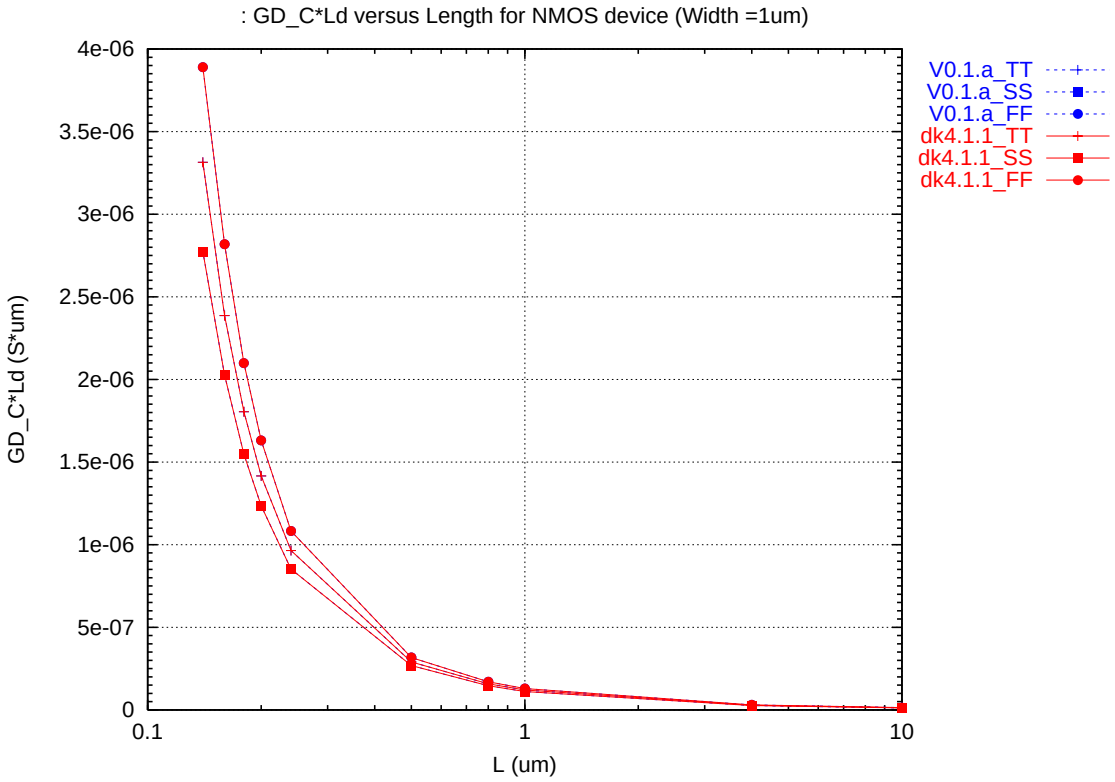

Figure 6 : GD*Ld versus drawn gate length for NMOS HPA_LP transistors (W = 1 µm)

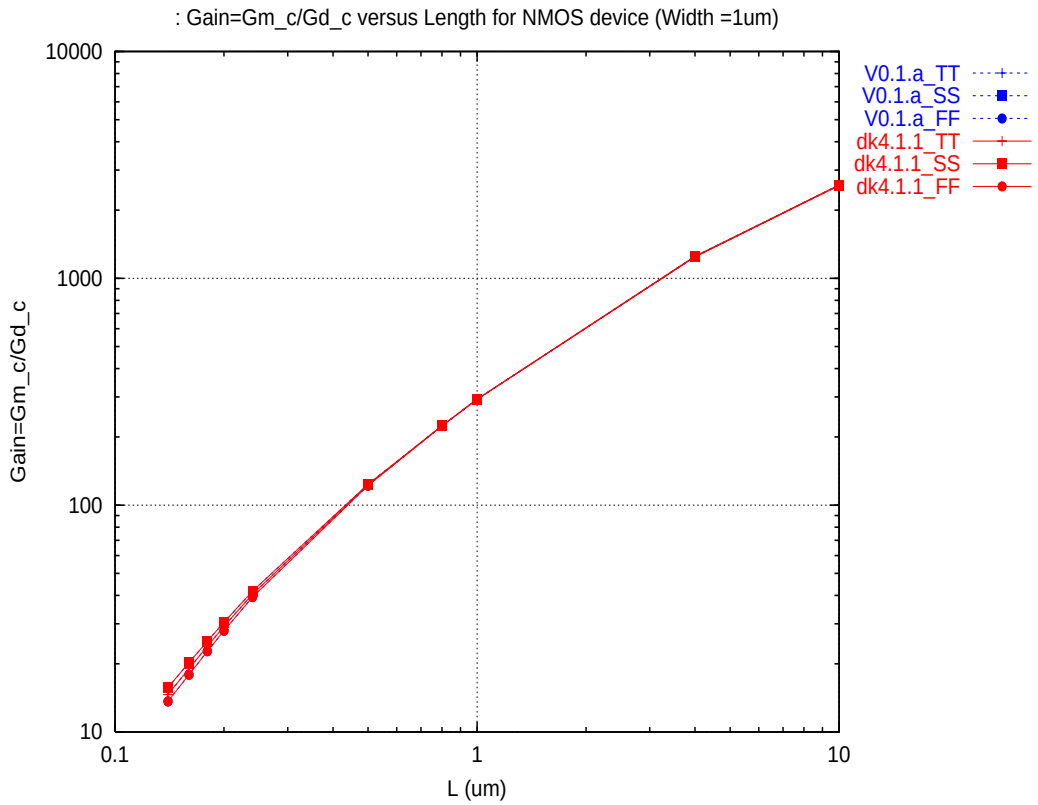

Figure 7 : GAIN versus drawn gate length for NMOS HPA_LP transistors (W = 1 µm)

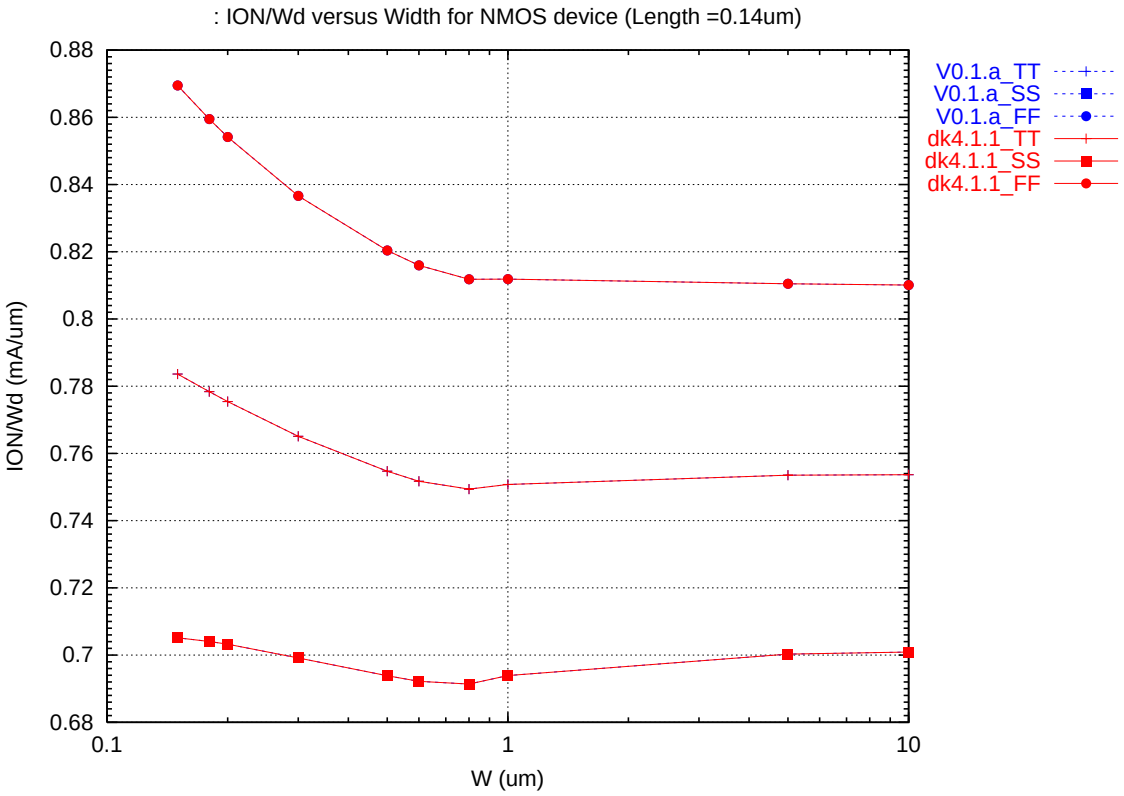

Figure 8 : ION versus drawn channel width for NMOS HPA_LP transistors (L = 0.14 µm)

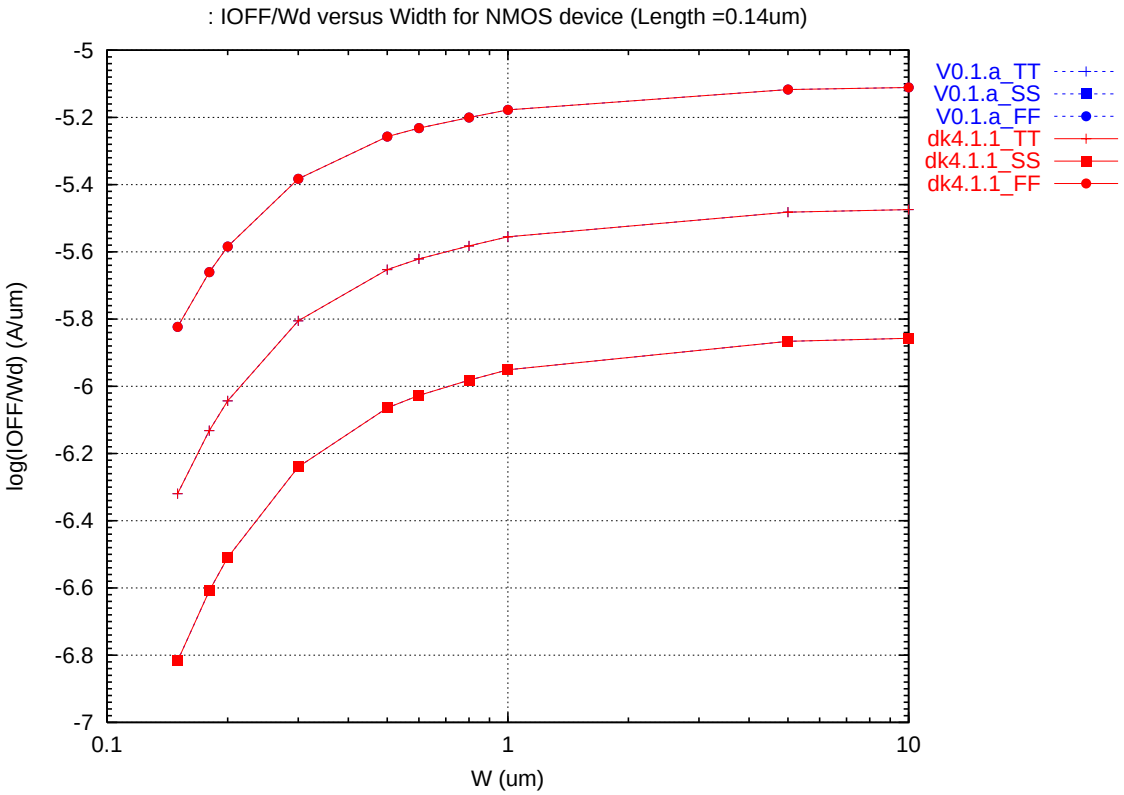

Figure 9 : IOFF versus drawn channel width for NMOS HPA_LP transistors (L = 0.14 µm)

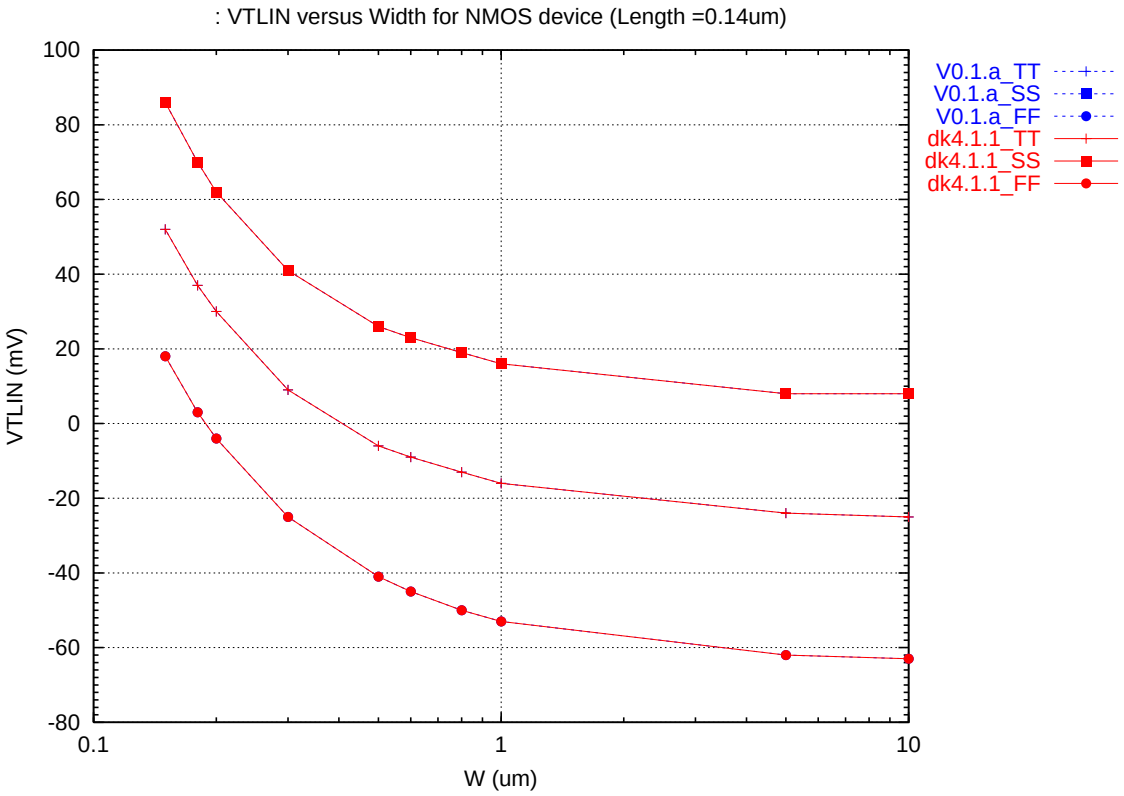

Figure 10 : Threshold voltage VTLIN versus drawn channel width for NMOS HPA_LP transistors (L = 0.14 µm)

6. ELECTRICAL BEHAVIOR VERSUS GATE LENGTH AND CHANNEL WIDTH FOR PMOS HPA_LP TRANSISTORS

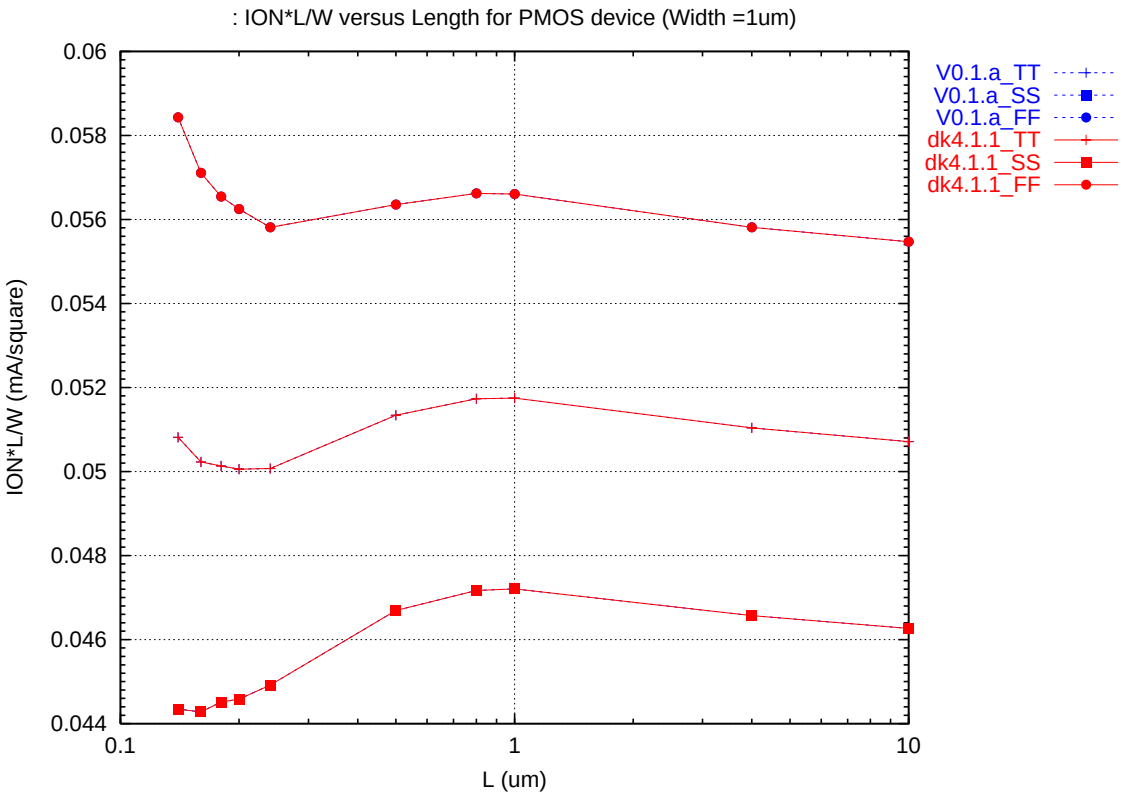

Figure 11 : ION versus drawn gate length for PMOS HPA_LP transistors (W = 1 µm)

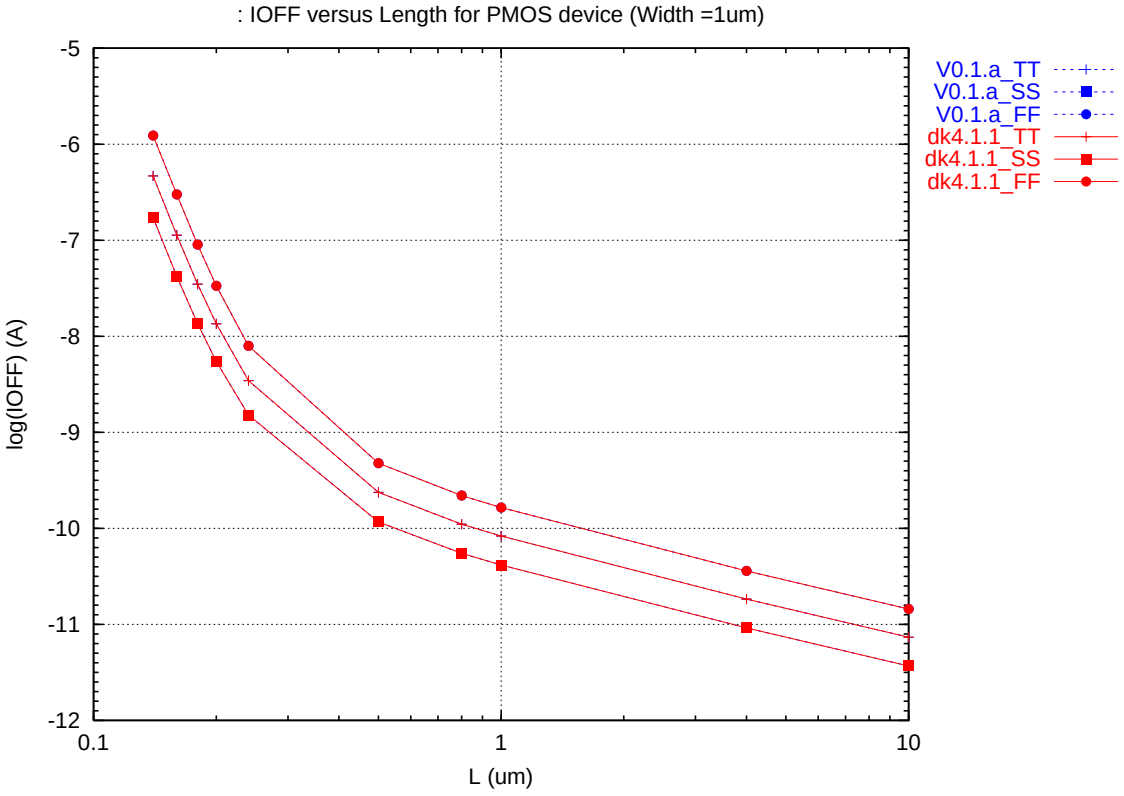

Figure 12 : IOFF versus drawn gate length for PMOS HPA_LP transistors (W = 1 µm)

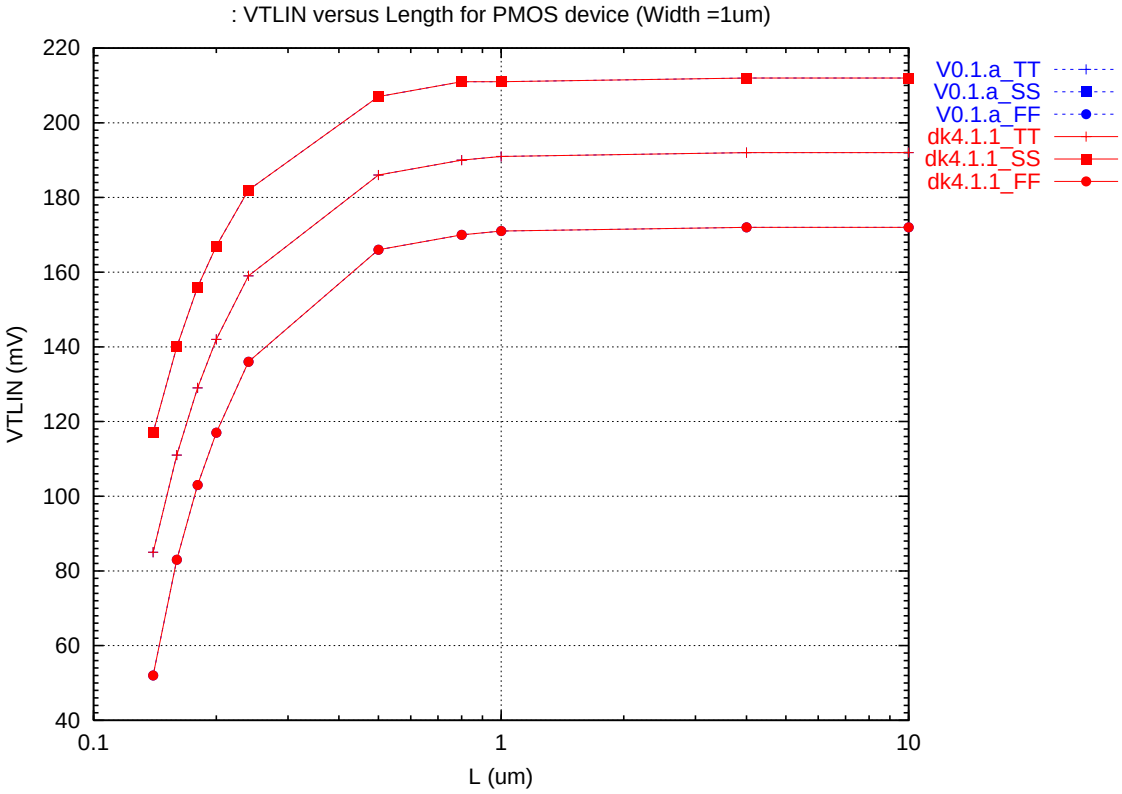

Figure 13 : Threshold voltage VTLIN versus drawn gate length for PMOS HPA_LP transistors (W = 1 µm)

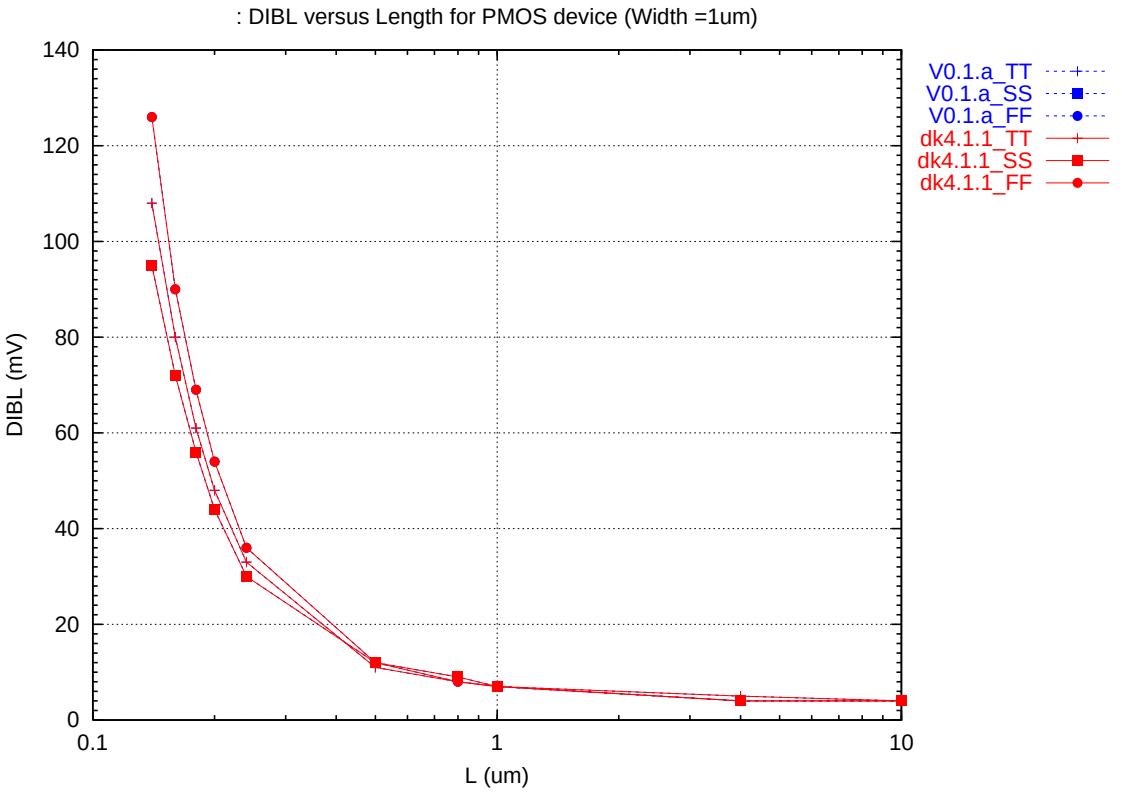

Figure 14 : DIBL= VTLIN-VTSAT versus drawn gate length for PMOS HPA_LP transistors (W = 1 µm)

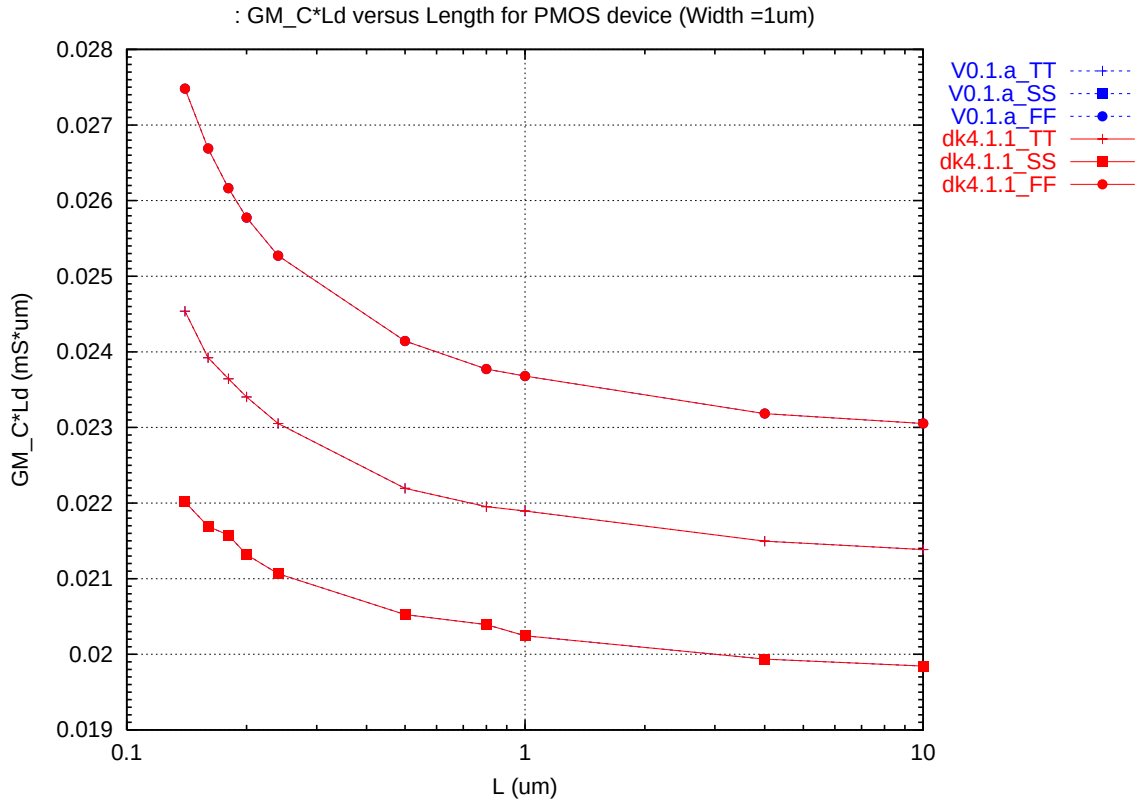

Figure 15 : GM*Ld versus drawn gate length for PMOS HPA_LP transistors (W = 1 µm)

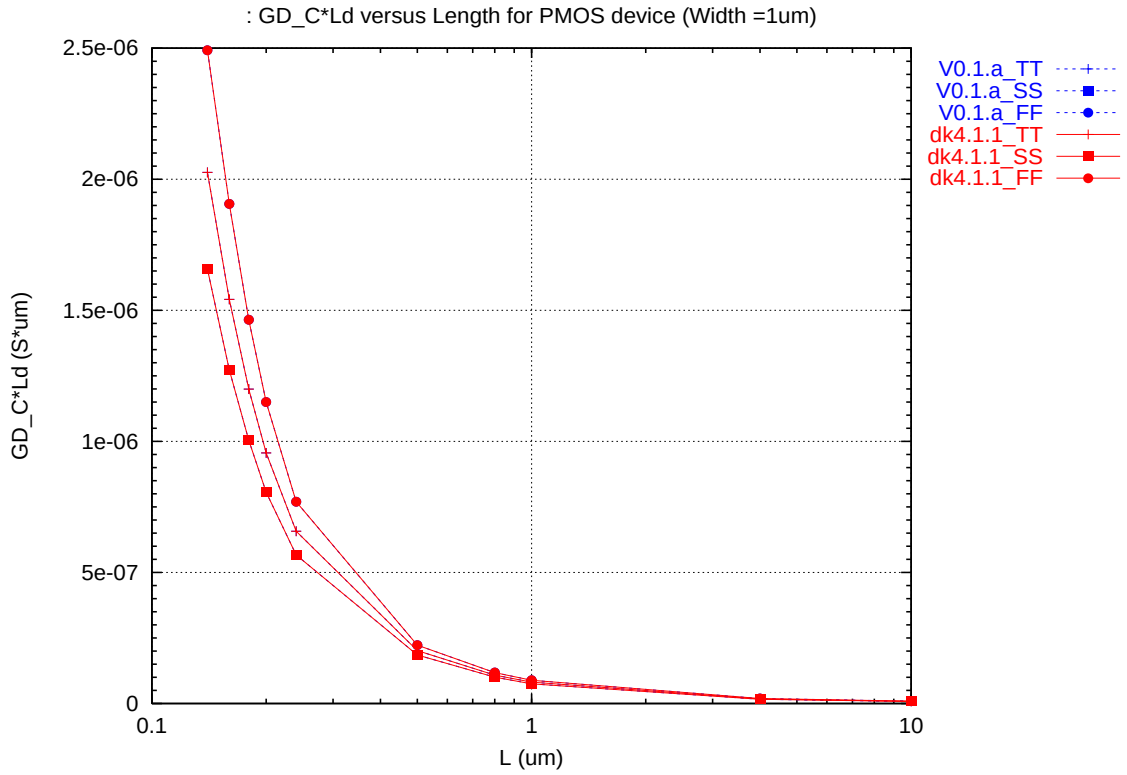

Figure 16 : GD*Ld versus drawn gate length for PMOS HPA_LP transistors (W = 1 µm)

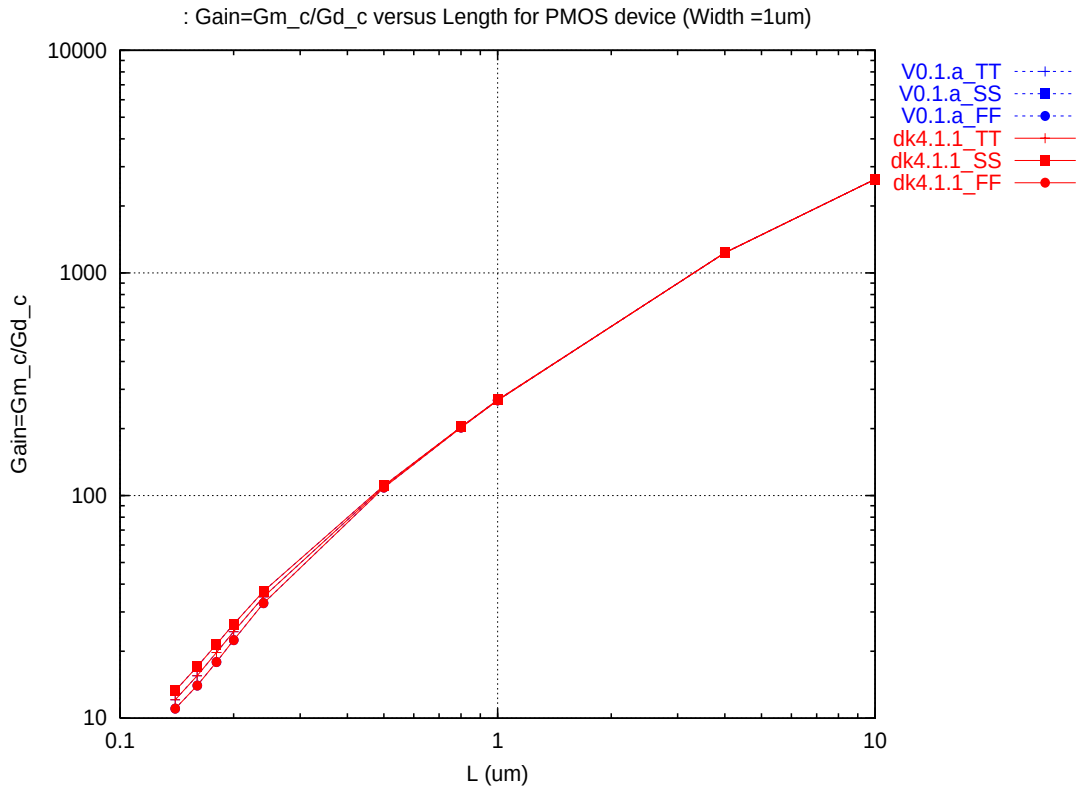

Figure 17 : GAIN versus drawn gate length for PMOS HPA_LP transistors (W = 1 µm)

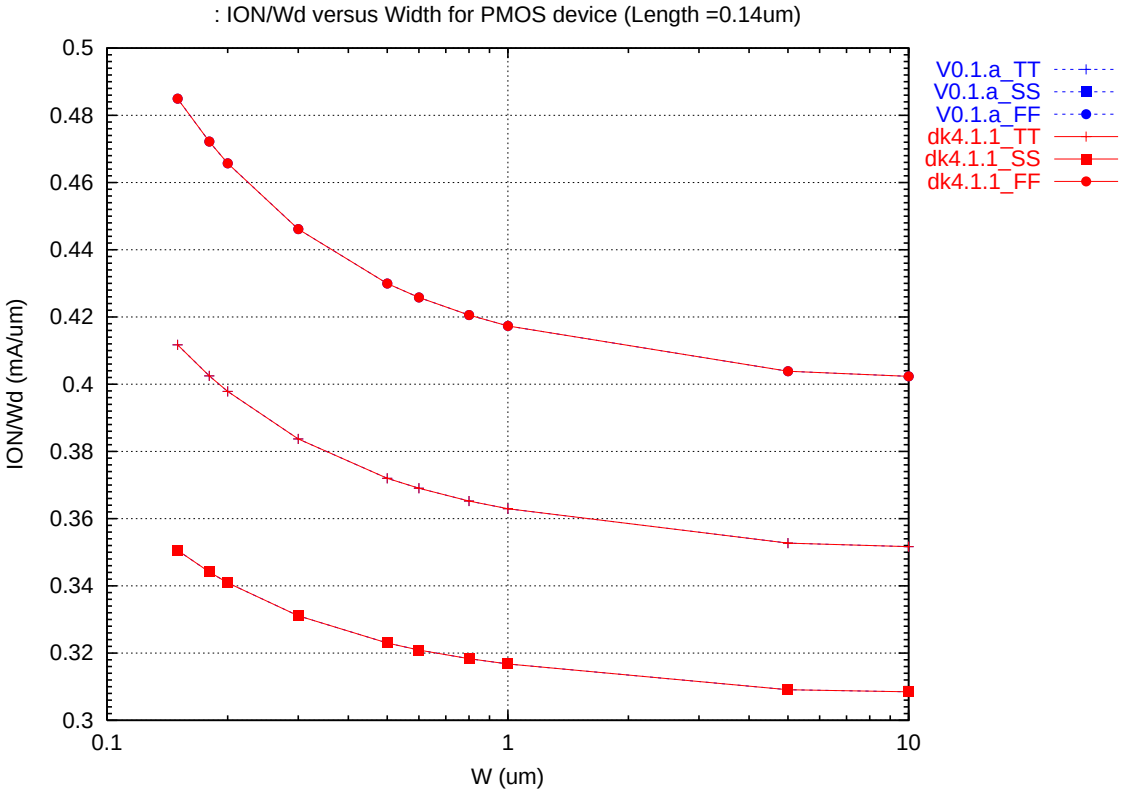

Figure 18 : ION versus drawn channel width for PMOS HPA_LP transistors (L = 0.14 µm)

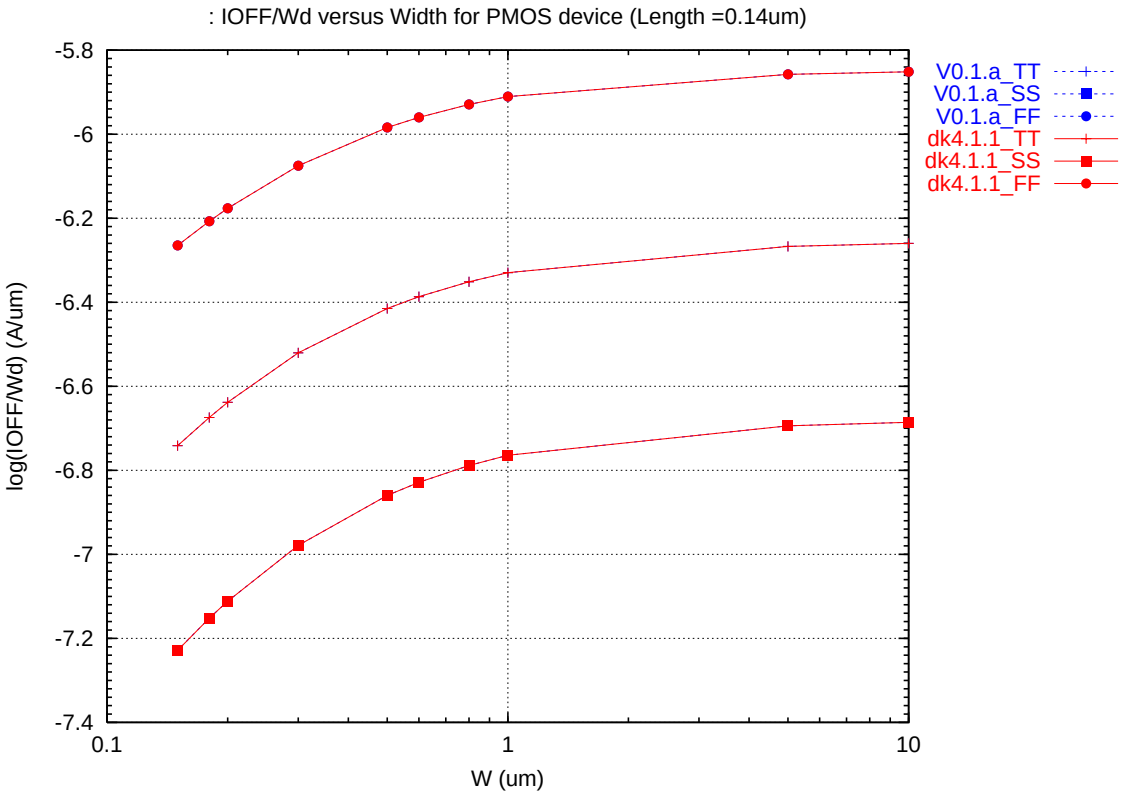

Figure 19 : IOFF versus drawn channel width for PMOS HPA_LP transistors (L = 0.14 µm)

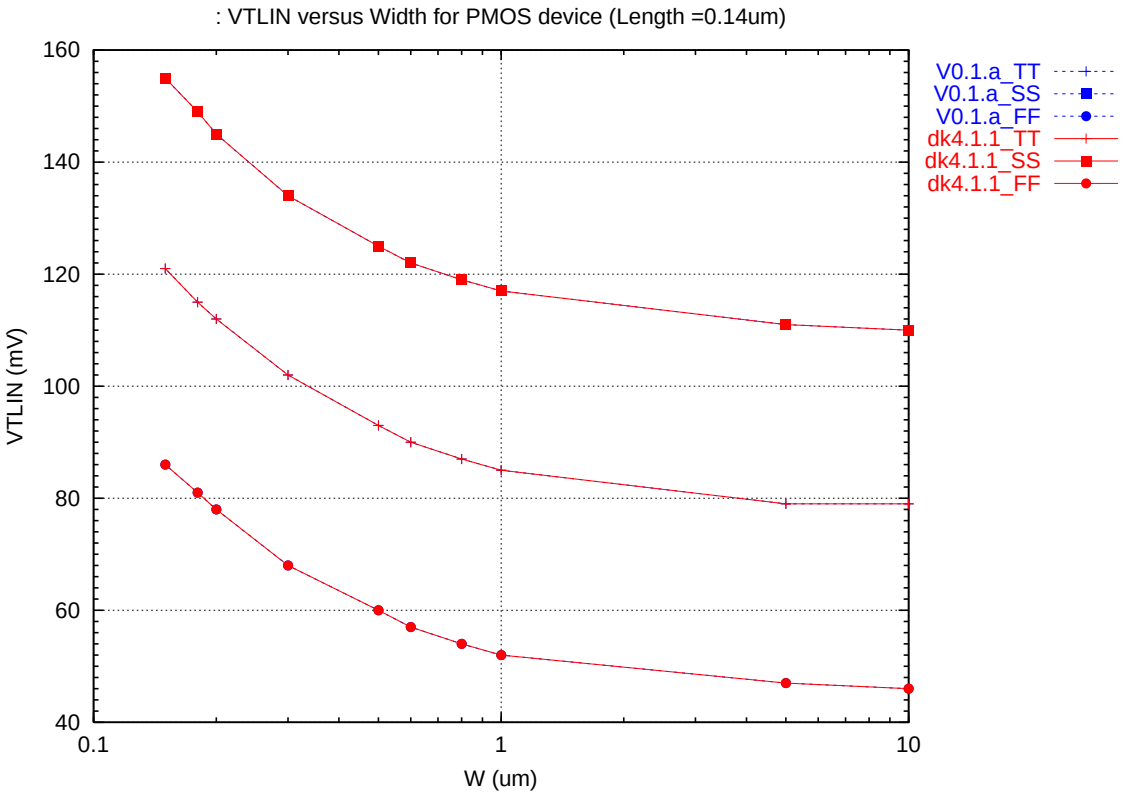

Figure 20 : Threshold voltage VTLIN versus drawn channel width for PMOS HPA_LP transistors (L = 0.14 µm)