PLS flow and solutions

Training Rev. 2006.01

STMicroelectronics

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Introduction

- PLS acronym for Post Layout Simulation
- Script built by CR&D to perform automatically the Interconnects parasitic (R&C) extraction flow
- Stand alone or Opus (cadence) Framework integrated interface
- Link to Simulation Environment based on *Cadence Analog Environment*

Products

- PLS integrated within Opus (cadence) Framework interface from PLSKit
- Supported in all Technologies from 0.35um with last release of Design Kit
- Supported extractors
  - StarRCXT (SYNOPSYS)
- Supported simulator netlist formats:
  - Eldo, EldoD (*Mentor Graphics) with Artist-Link*
  - Spectre (*Cadence) with Analog Artist*
  - hspiceS
  - ADS

Glossary

- Interconnects = Wires used to connect devices
  - Described as ideal connections at schematic level
  - Described as metal shapes in the layout
  - Interconnects present electrical losses that need to be taken into account during performances estimation

- Interconnects model
  - Electrical models based on resistances, capacitances and eventually inductances including coupling elements

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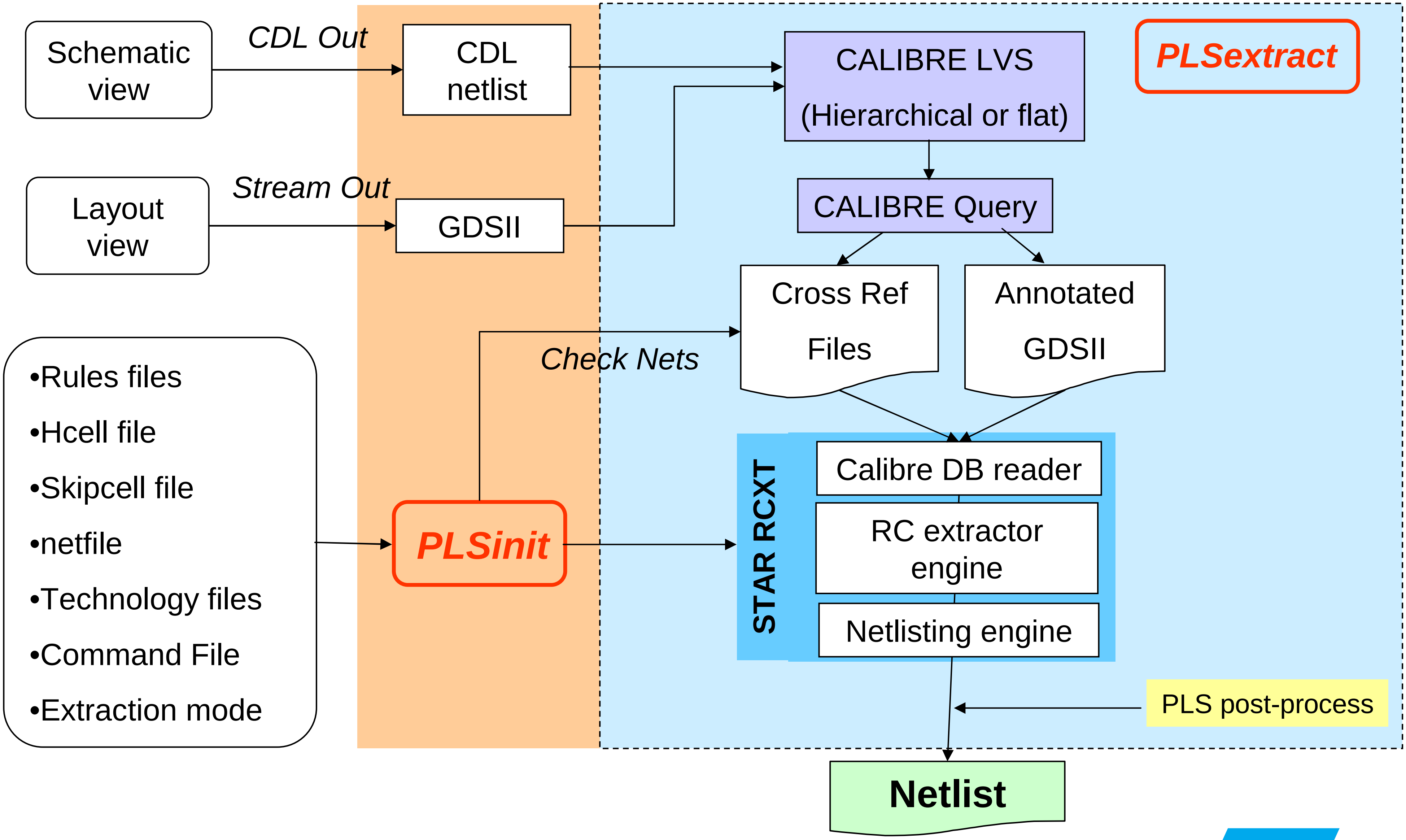
PLS Flow overview

- Post layout extraction flow based on Calibre (Mentor Graphics) and StarRCXT (Synopsys)

- 2 main steps:
  - ➢ PLSinit
    - ✓ Copy and customize data from design kit
    - ✓ Design information setup
  - ➢ PLSextract
    - ✓ Run LVS
    - ✓ RC extraction
    - ✓ Netlisting

PLS Flow overview



PLS flow Prerequisites

- Mandatory tools for PLS flow:
  - Calibre for LVS part
  - StarRCXT for extraction part
  - Opus to get all integrated features
  - PLSkit to get all PLS associated scripts and interface
  - ArtistKit for simulation tools integration
  - DesignKit for all techno dependant files
  - Simulator eldo/spectre/hspice/ADS
- Optionnal tools:
  - QuickCap if Field Solver extraction has to be used
- To run the PLS flow properly please check you are using the recommended tools in Design Kit. Please refer to release notes of the Design Kit.
- Correct DRC and no mismatch on Standard LVS (including ERC) is a mandatory prerequesite before any PLS run

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Full chip extraction

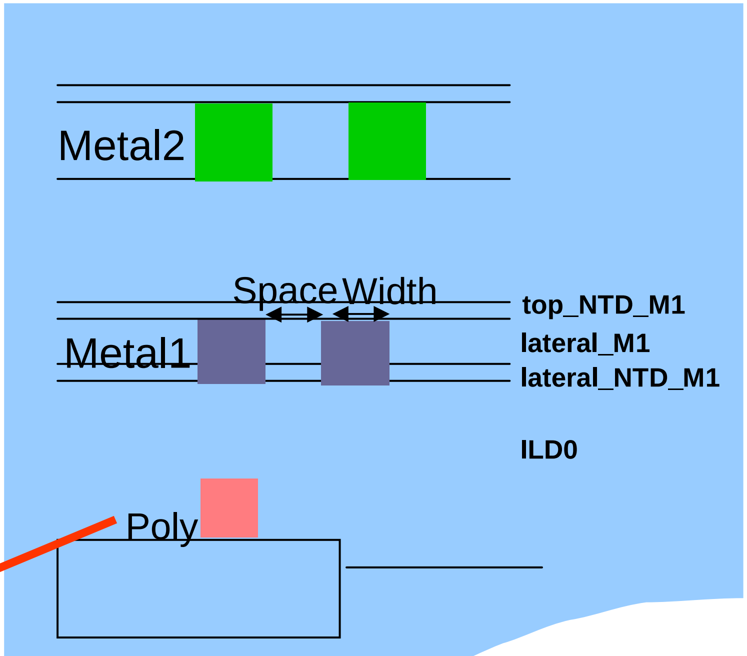
- Full chip extractors are based on **Pattern Matching** approach
  - Pre-computed analytical RCmodels on a proprietary library of basic patterns (such as crossing, bends…)
  - RC extraction starts by a design parsing step to identify basic patterns and apply the analytical models
  - Algorithm to correct models abutment
- RCmodels input
  - ITF = interconnect technology file
    - ✓ Cross-section of interconnects (z dimensions)
    - ✓ Material properties

Input parameters

➔ list of the drawn and technological parameters respectively used for capacitance and resistance computation.

- For capacitances computation
  - ➢ Line’s width, length and space (drawing)
  - ➢ Conductor thickness
  - ➢ Dielectric’s thickness and permittivity
- For resistances computation
  - ➢ Line’s width and length (drawing)
  - ➢ Conductor sheet resistance
  - ➢ Conductor temperature coefficient (if applicable)

ITF sample



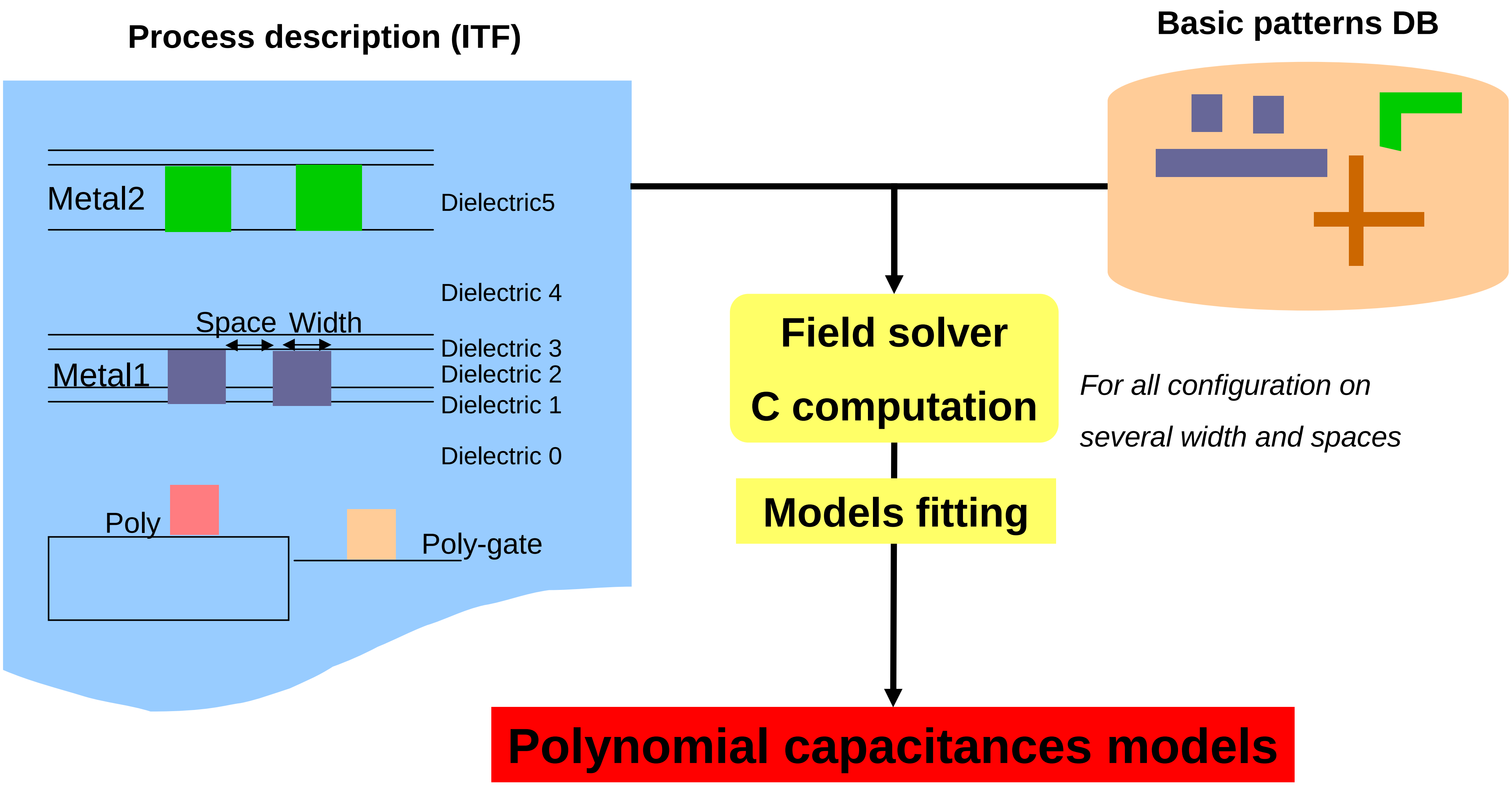
```
DIELECTRIC ILD2                 { THICKNESS=0.360  ER=3.7 }
DIELECTRIC top_NTD_M1           { THICKNESS=0.040  ER=8.1 }
DIELECTRIC lateral_M1           { THICKNESS=0.22  ER=3.7 }
DIELECTRIC lateral_NTD_M1  {THICKNESS=0.040  ER=8.1 }
CONDUCTOR  ME1_FINAL {     THICKNESS=0.260
                           WMIN=0.160
                           SMIN=0.180
                           RPSQ=75.0e-3
                           ETCH=0 }

DIELECTRIC ILD0                 { THICKNESS=0.59 MEASURED_FROM=Base_Dielectric ER=4.2 }
DIELECTRIC NTD_POLY             { THICKNESS=0.050  MEASURED_FROM=TOP_OF_CHIP SW_T=0.050 TW_T=0.050 ER=7 }
CONDUCTOR  IPOLY_FINAL  { THICKNESS=0.180
                            WMIN=0.130
                            SMIN=0.180
                            RPSQ=10.0
                            ETCH=0.01 }

DIELECTRIC Base_Dielectric {  THICKNESS=0.300 ER=4 }

VIA VI1_FINAL {                 FROM=ME1_FINAL              TO=ME2_FINAL  AREA=0.0361 RPV=1.0 }
VIA contact     {                FROM=IPOLY_FINAL            TO=ME1_FINAL                    AREA=0.0256 RPV=10.4237 }
```

Capacitances modeling



Process description (ITF)

Basic patterns DB

Field solver

C computation

For all configuration on several width and spaces

Models fitting

Polynomial capacitances models

Process corners

- RCTYP: typical values for all C's and R's
- RCMIN: best values for all C's and R's
- RCMAX: worst values for all C's and R's

- CMIN: best C's, worst R_{wire} and best R_{via}
- CMAX: worst C's, best R_{wire} and worst R_{via}
- XTLK: worst lateral C, best vertical C and best R's
- DLY: best lateral C, worst vertical C and worst R's

TECHNO	CORNER	METAL THICK.	METAL WIDTH	VIA THICK.	DIELEC K1	DIELEC K2	VIA RES.	METAL RES.	TEMP.
All	RCTYP	TYP	TYP	TYP	TYP	TYP	TYP	TYP	TYP
	RCMIN	MIN	MIN	MAX	MIN	MIN	MIN	MIN	TYP
	RCMAX	MAX	MAX	MIN	MAX	MAX	MAX	MAX	TYP
<= 90 nm	CMIN	MIN	MIN	MAX	MIN	MIN	MIN	MAX	MIN
	CMAX	MAX	MAX	MIN	MAX	MAX	MAX	MIN	MAX
	XTLK	MAX	MAX	MAX	MAX	MIN	MIN	MIN	MIN
	DLY	MIN	MIN	MIN	MIN	MAX	MAX	MAX	MAX

K1 = intra-layer dielectric K2 = inter-layer dielectric

Advanced process features

➔ Applicable to 90nm and below

- Sheet resistance function of Silicon width
- Isolated lines upsizing
  - ➢ Etching function of width and space
  - ➢ Different etching for R and C
- Temperature derating coefficient function of the width
- Poly spacer

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PLSkit main features

- 8 extraction modes: noRc; C; Cc; R; RC; RCc; Mixed/Cc_RCc; Field Solver
- Process corners:
  - 3 for techno > 90nm: RCMIN; RCTYP; RCMAX
  - 7 for techno<=90nm: RCMIN; RCTYP; RCMAX; CMIN; CMAX; DLY; XTLK
- 5 simulators supported: eldo; eldoD; Spectre; HspiceS; ADS
- 2 output netlist formats: Spice; DSPF
- Option for via capacitance extraction and temperature
- LPE flag
- Batch mode or opus/standalone integration
- Automatic netfile creation
- Prerequisites checker
- Run on SUN, HP or linux plateforms
- Flat or hierarchical LVS
- Based on calibre interactive
- Net Browser
- Extracted views

Extraction Modes (1/8)

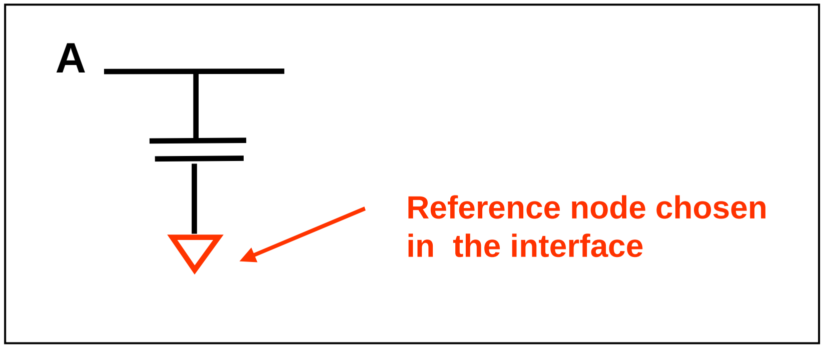
Note: Interconnects models are called extraction modes

- noRC extraction mode
  - **noRC** : allows to check devices netlist validity
  - Allows to evaluate impact of LVS netlist and to distinguish instance section and parasitics section
  - Due to LVS tolerance comparison, slight differences versus pre-layout simulation
  - Diode devices extracted by default with PLS; and not compared (can be changed in calibre LVS expert mode)
  - Impact of extra parameters : as;ad;ps;pd;po2act …
  - Recommended before any other extraction mode

Extraction Modes (2/8)

Capacitive only extraction modes

- **Mode C** : Net-to-ground coupling (suited for digital applications)



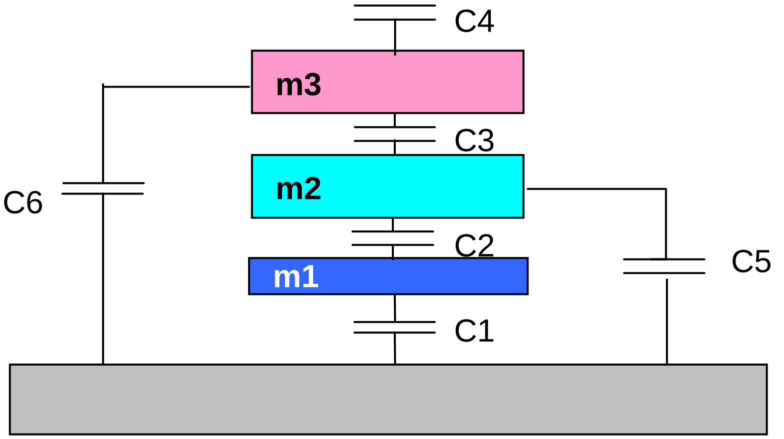
Reference node chosen in the interface

If net A is declared in the netfile :

associated lumped capacitance extracted

1 threshold: C threshold (post-processing)

If [C(A) < C threshold] **then** C(A) is ignored



If Ref = 0 :

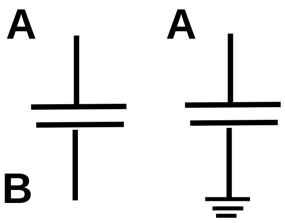
Metal1 : Clumped $C_{m1\text{-}0} = C1 + C2$

Metal2 : Clumped $C_{m2\text{-}0} = C2 + C3 + C5$

Metal3 : Clumped $C_{m3\text{-}0} = C3 + C4 + C6$

Extraction Modes (3/8)

- Capacitive only extraction modes
  - **Mode Cc** : Net-to-net coupling (best suited for RF applications)



If net A is declared in the netfile : extraction of all coupling capacitances between A and all nets Ni

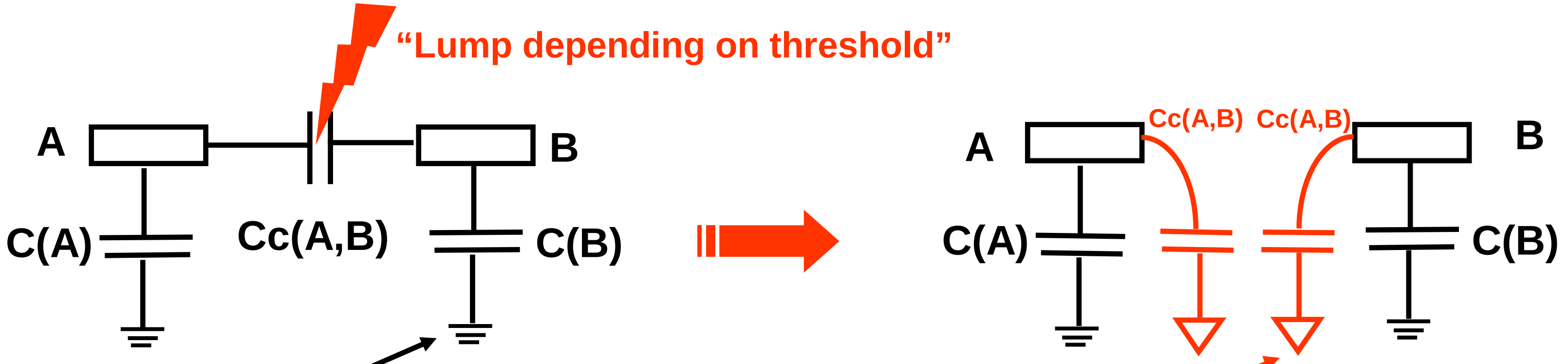
2 thresholds: Cc threshold ; Cc percentage

If { [Cc(A,B) < Cc threshold]

and [Cc(A,B)/C(A) < Cc percentage]

and [Cc(A,B)/C(B) < Cc percentage] }

then Cc(A,B) is lumped (not removed)



"Lump depending on threshold"

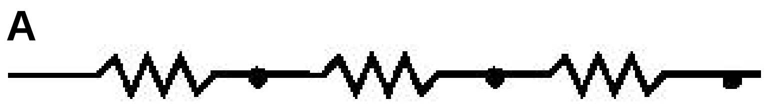
Extracted ground

Ground net name for Lumped parasitic capacitances (Node chosen in the interface)

➔ **Best Accuracy with "Cc threshold = 0" and Cc "percentage = 0"**

Extraction Modes (4/8)

- Resistance only extraction mode
  - **Mode R** : Net resistances



If net A is declared in the netfile :

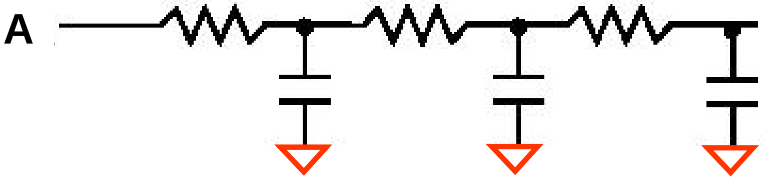
parasitic resistances extraction

This mode allows usage of reduction script proposed within the interface

PLS reduction is described in further slides

Extraction Modes (5/8)

- Resistive and Capacitive extraction modes
  - **Mode RC** : Sub node-to-ground coupling



If net A is declared in the netfile :

- parasitic resistances extraction

- lumped capacitances extraction

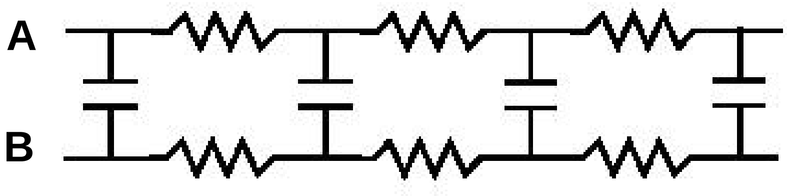
on each subnode of net A

This mode allows usage of reduction script proposed within the interface

PLS reduction is described in further slides

Extraction Modes (6/8)

- Resistive and Capacitive extraction modes
  - **Mode RCc** : Subnode-to-Subnode coupling



- parasitic resistances extraction on nets declared in the netfile

- coupling capacitances associated to each node declared in the netfile, even if the agresssor nets are not declared in the netfile.

2 thresholds: Cc threshold ; Cc percentage

If { [Cc(A,B) < Cc threshold]

or [Cc(A,B)/C(A) < Cc percentage]

or [Cc(A,B)/C(B) < Cc percentage] }

then Cc(A,B) is lumped (not removed)

Extraction Modes (7/8)

- Mixed extraction modes
  - **Mode Mixed**: 5 netfiles
    - **net_R** : parasitic resistances
    - **net_C** : lumped capacitances
    - **net_Cc** : coupling capacitances
    - **net_RC** : parasitic resistances and lumped capacitances
    - **net_RCc** : parasitic resistances and coupling capacitances

    - Same thresholds as mode RCc or Cc
    - User can specify from 1 to 5 netfiles
    - netfiles are exclusive (one net can be declared in only one of the 5 netfiles ; In mode Mixed; *all is forbidden)

Extraction Modes (7/8)

- Mixed extraction modes
  - **Mode Cc_RCc**: 1 netfile
    - **net_RCc** : parasitic resistances and coupling capacitances

    - Specific Mixed mode dedicated to RF most used applications
      - All nets are extracted with Cc mode
      - Resistor is extracted for the subset of nets given in netfile
    - Netfile concerns only nets where parasitic resistors are calculated
      - In framework: **"Res & net-to-net coupling"**
    - Same thresholds as mode RCc or Cc

Extraction Modes (8/8)

- Field solver extraction mode: **FS extract**
  - **<u>Coupling capacitances only</u>**
  - 2 netfiles:

  - **net_Std**: coupling cap. given by full chip extractor

  - **net_FSextract**: Very accurate capacitance extraction based on a field solver (Quickcap)

  - Dedicated to a very limited number of nets
  - 2 capa threshold + 3 options for convergence goals and runtime limit.
  - Accurate but slow!

Netfile

- Each extraction mode has associated netfile
  - C; Cc; R; RC; RCc; Cc_RCc: only one netfile needed
  - Mixed: 1 to 5 netfiles
  - FS extract: 1 standard netfile + 1 accuracy netfile
- PLS netfile generation
  - all nets
  - all nets but power and ground (as specified in lvs.ctrl)
  - only power and ground nets
- netfile syntax
  - *all
  - *schematic-net-name: select schematic net name for extraction
  - ~schematic-net-name: avoid extraction of selected net.

Threshold; filtering; reduction options

	Cc threshold & Cc percentage (Lumped capacitors)	Cg threshold for filtering (post-processing)	PLS reduce script (Only with PLS phase II)
C		X	
Cc	X		
R			X
RC			X
RCc CC_RCc	X		

Available threshold and filterings depending on extraction options

Reduction

- Aimed at reducing DSPF when netlist size is critical for simulation convergence
- PLSreduce script is a Tcl wrapper of a C program
- Reduction of the resistor network for R or RC modes
- Applies on DSPF netlist; only for nets containing more than 10 nodes
- Subnodes resistors are removed : remaining resistors for drivers/driven pins only
- Pre-processing :
  - replace device terminals by driver pins
  - Topcell pin is considered as driven pin
  - A resistor is computed between each pin and the topcell pin
- Resistor network represented by admitance matrix with I=YU
- Linear system resolution with Gauss-Jordan numerical method
- Lumped capacitors of deleted subnodes shared between kept nodes
- Option for selection of candidates nets for reduction
- When running reduction, result without reduction are still available:

The reduction switch allows to visualize both results in netbrowser

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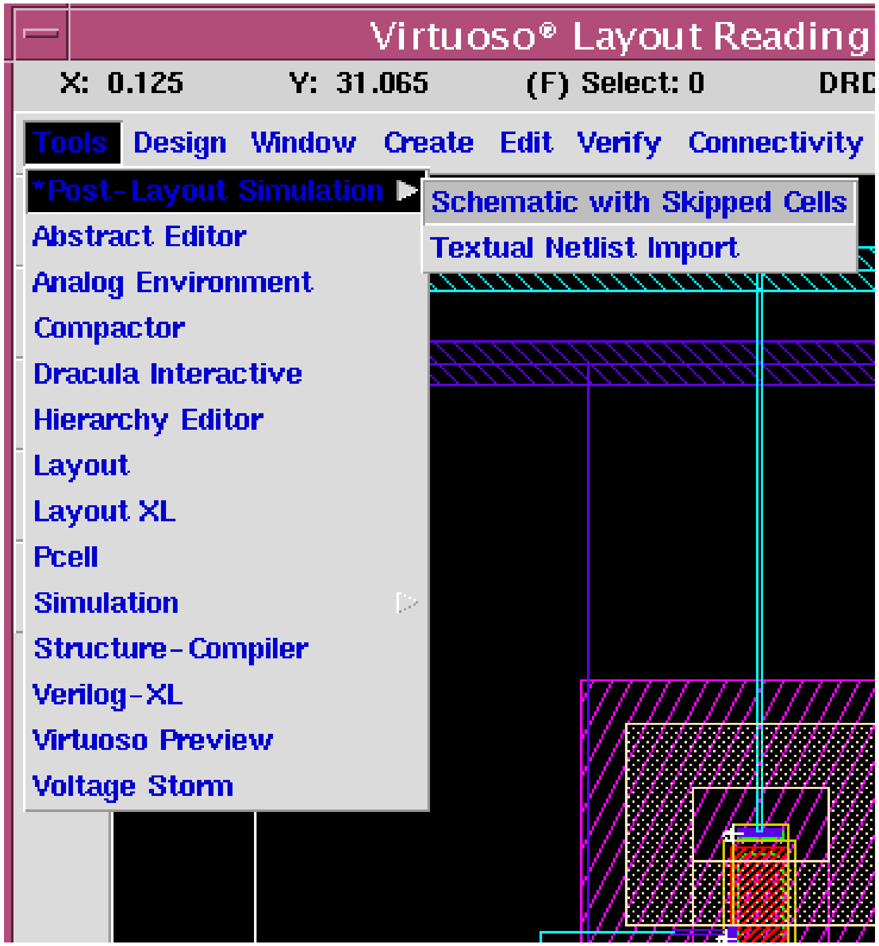
PLS flow choice



Select additional menu

Tools-> Post-Layout Simulation from the **schematic** menu banner or from the **layout** menu: 2 flows available:

•Schematic with Skipped Cells:

A true schematic with parasitics is built

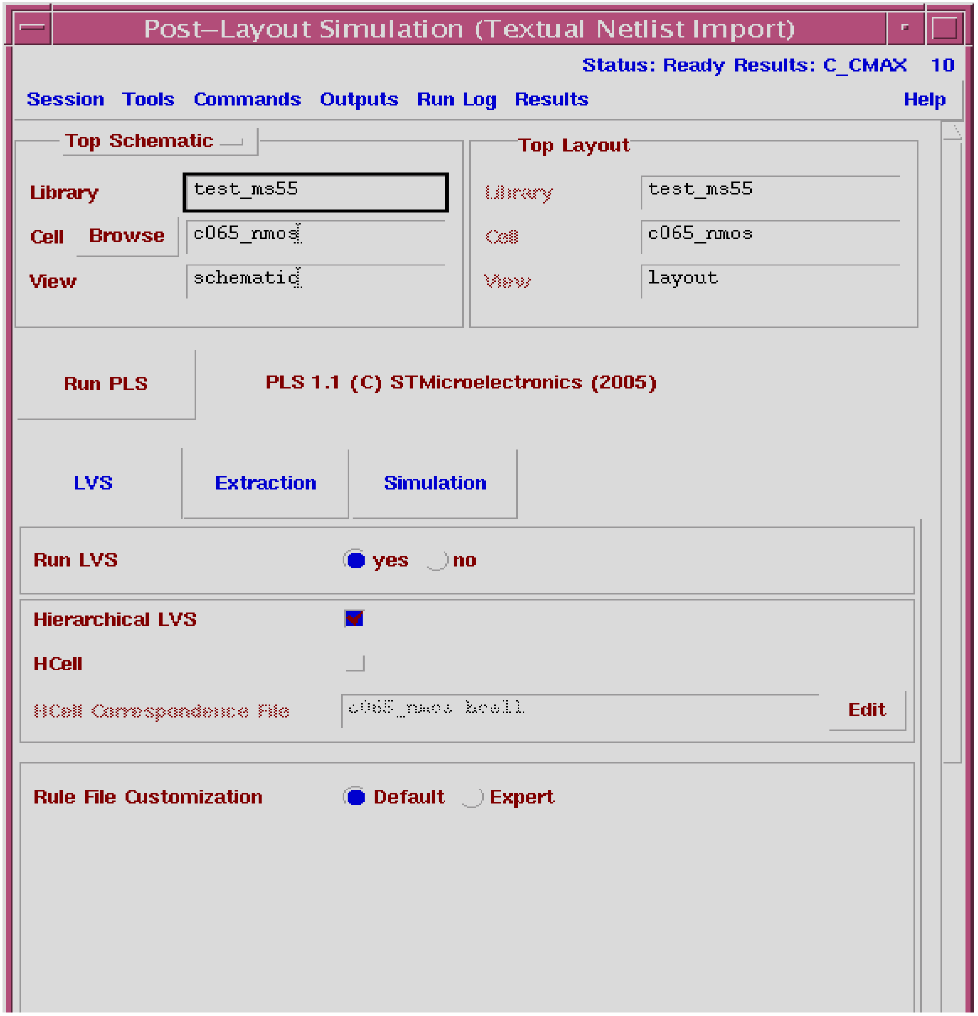
•Textual Netlist Import:

Only a textual netlist is obtained

Warning: the 2 flows cannot be run simultaneously on the same cadence cell (non compatible properties added in the cell)

For more informations please read PLSkit user manual

PLS Environment



Status: Ready Results: C_CMAX 10

Top Schematic

Library	test_ms55
Cell	c065_nmos
View	schematic

Top Layout

Library	test_ms55
Cell	c065_nmos
View	layout

PLS 1.1 (C) STMicroelectronics (2005)

Run LVS ● yes ○ no

Hierarchical LVS ☑

HCell □

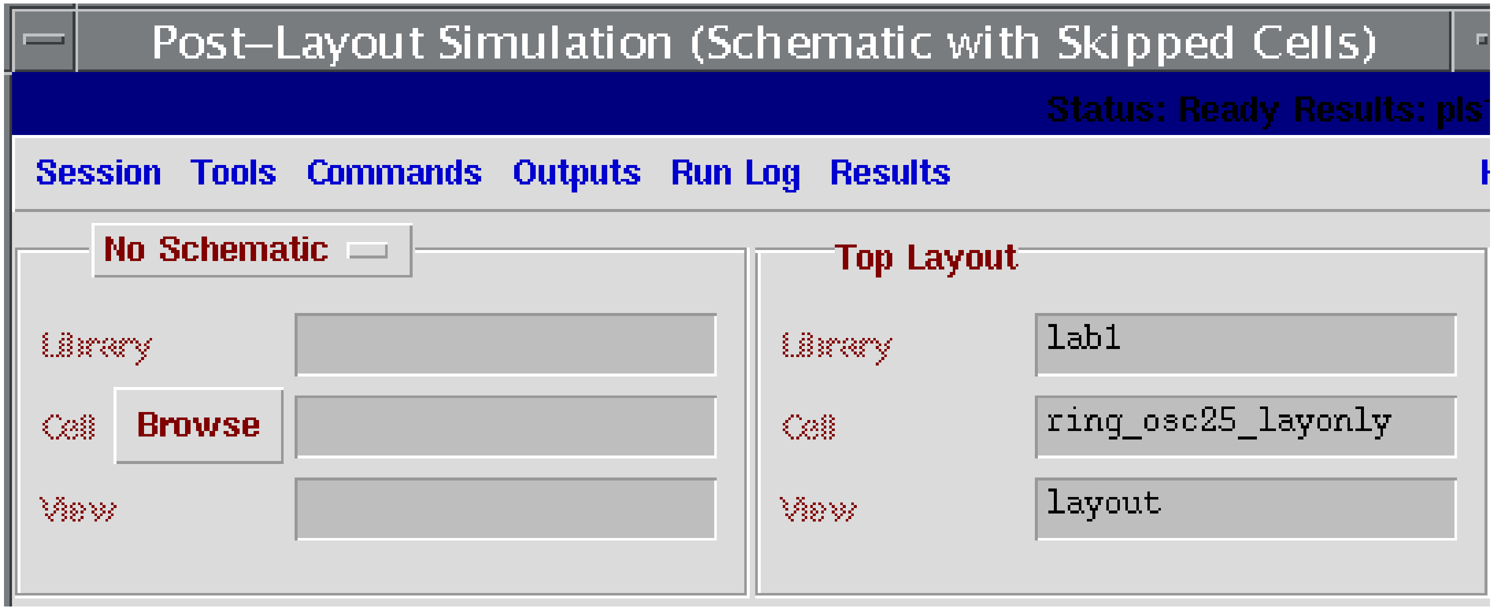
HCell Correspondence File c065_nmos.hcell

Rule File Customization ● Default ○ Expert

The interface is divided into 4 parts:

- The tool bar: for advanced options; logs and results viewing
- The Design information section: choice of cells and views to be used
- The PLS run section
- The option section: with tabular fields to set all desired extraction options

PLS Environment: Layout only case



Post–Layout Simulation (Schematic with Skipped Cells)
Status: Ready Results: pls
Session
Tools
Commands
Outputs
Run Log
Results
No Schematic
Browse
Top Layout

Library

Cell

View

Top Layout

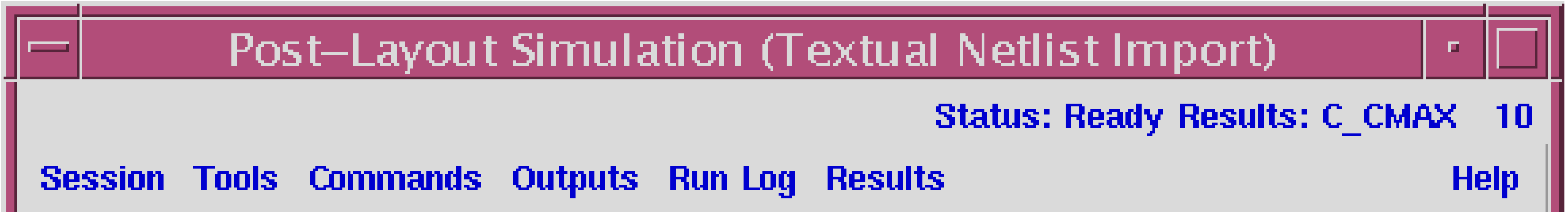
Library: lab1

Cell: ring_osc25_layonly

View: layout

- Layout view can be used if no schematic => “layout only flow”
- When launching interface from layout; auto-detection of blank schematic
- The lay.net netlist extracted by calibre serves as “cdl” netlist
- An other possibility is to select any other “top schematic”
- Only for quick analysis purpose; LVS based on schematic has to be done for signoff flow

PLS Environment menus

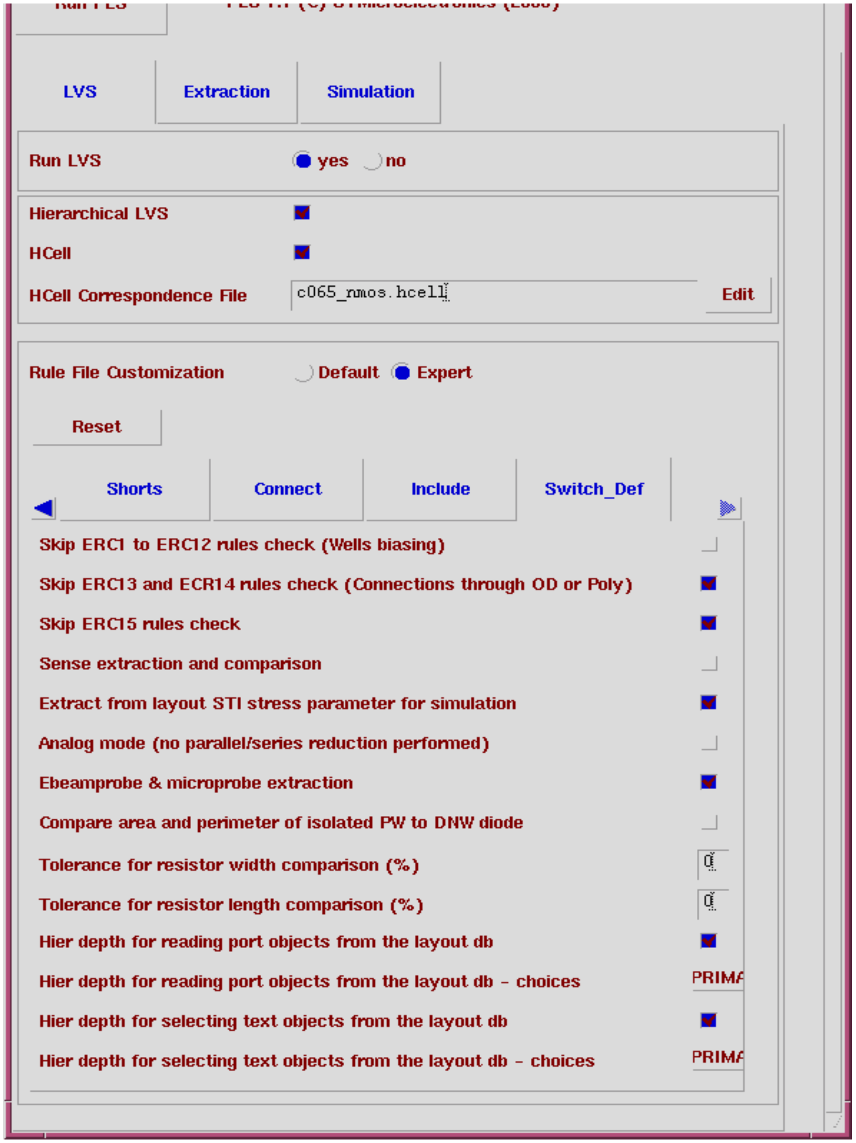


Post–Layout Simulation (Textual Netlist Import)

Status: Ready Results: C_CMAX 10

- **Session** menu allows you to customize your session
- **Tools** menu allows to run the program step by step
- **Commands** menu resumes main PLS commands
- **Outputs** menu allows you to look at important files & results
- **Run Log** menu allows you to see the log files
- **Results** menu allows you to store/delete different runs or reload previous one

PLS interface Window: LVS



Run LVS ● yes ○ no

Hierarchical LVS ☒

HCell ☒

HCell Correspondence File c065_nmos.hcell

Rule File Customization ○ Default ● Expert

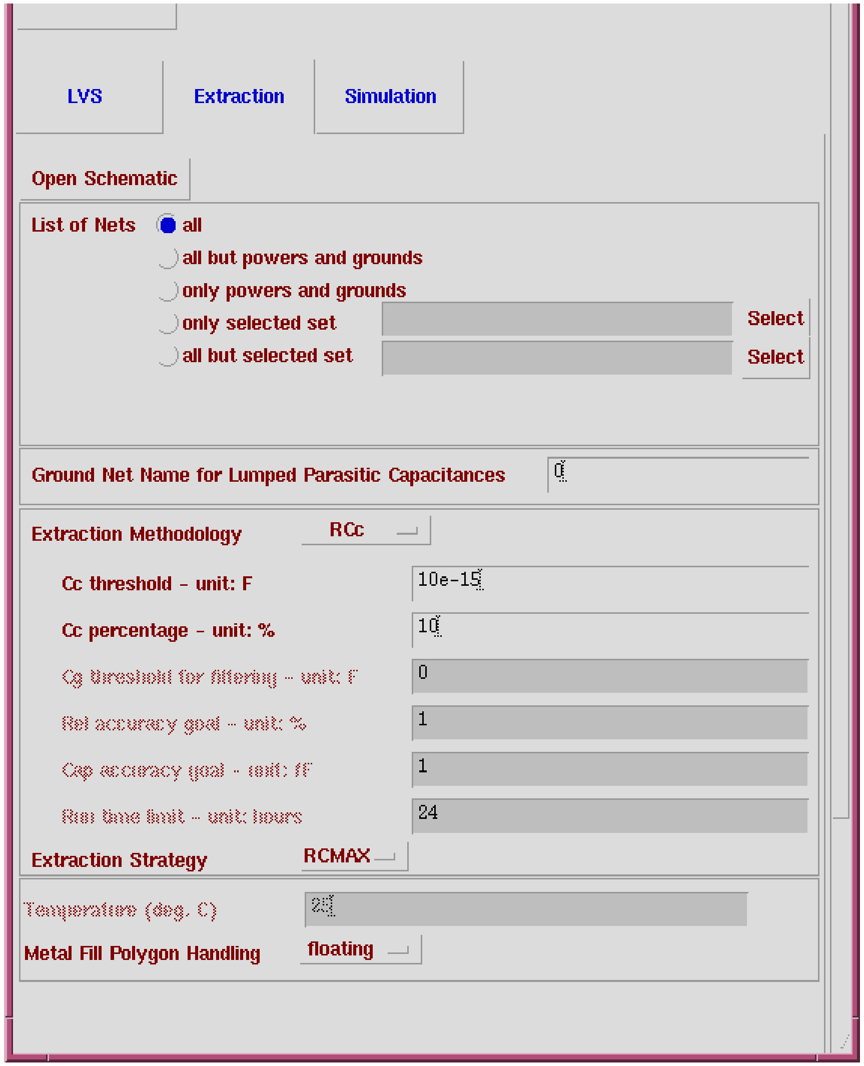
Skip ERC1 to ERC12 rules check (Wells biasing)	□
Skip ERC13 and ECR14 rules check (Connections through OD or Poly)	☒
Skip ERC15 rules check	☒
Sense extraction and comparison	□
Extract from layout STI stress parameter for simulation	☒
Analog mode (no parallel/series reduction performed)	□
Ebeamprobe & microprobe extraction	☒
Compare area and perimeter of isolated PW to DNW diode	□
Tolerance for resistor width comparison (%)	0
Tolerance for resistor length comparison (%)	0
Hier depth for reading port objects from the layout db	☒
Hier depth for reading port objects from the layout db - choices	PRIMA
Hier depth for selecting text objects from the layout db	☒
Hier depth for selecting text objects from the layout db - choices	PRIMA

From the window, with **Calibre LVS** Tab you can:

- Choose **not to run** the step (if already run(mandatory))
- Choose run **flat** or **hierarchical** LVS
- Define **Hcell List** (hierarchical)
- Choose customization level **default** or **expert**
- **If expert** Selected:

Many tab menus allow to use same option as for standard LVS (Precision of comparisons, virtual connections, diodes extractions…)

PLS interface Window: Extraction



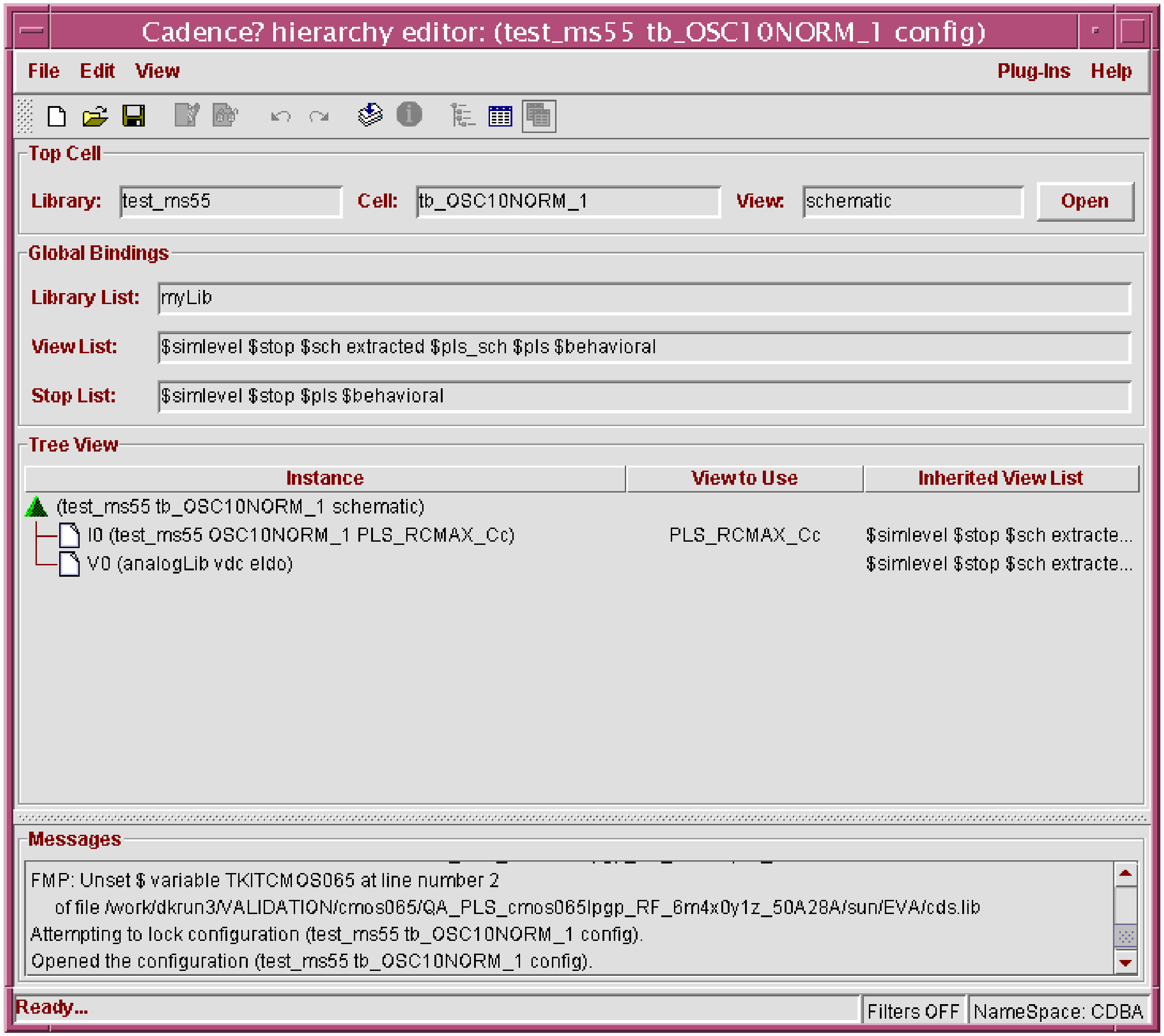
List of Nets
- ● all
- ○ all but powers and grounds
- ○ only powers and grounds
- ○ only selected set
- ○ all but selected set

Ground Net Name for Lumped Parasitic Capacitances	0
Extraction Methodology	RCc
Cc threshold - unit: F	10e-15
Cc percentage - unit: %	10
Cg threshold for filtering - unit: F	0
Rel accuracy goal - unit: %	1
Cap accuracy goal - unit: fF	1
Run time limit - unit: hours	24
Extraction Strategy	RCMAX
Temperature (deg. C)	25
Metal Fill Polygon Handling	floating

From **Extraction** Tab you can:

- **Generate automatically** a netfile with
  - ✓ all nets
  - ✓ all nets but power and ground nodes (as defined in LVS)
  - ✓ **select on schematic** the nets to be extracted or not
- Choose reference net for grounded capacitances (lumped modes C & RC)
- Select **extraction mode:** R, RC, Cc…
- Define filtering **Thresholds**
- Choose Corner **Strategy** (RCTYP, RCMAX…)
- Choose temperature and dummies management mode

Link to Simulation: CONFIG creation / HED



Library: test_ms55 Cell: tb_OSC10NORM_1 View: schematic

Library List: myLib

View List: $simlevel $stop $sch extracted $pls_sch $pls $behavioral

Stop List: $simlevel $stop $pls $behavioral

Instance	View to Use	Inherited View List
(test_ms55 tb_OSC10NORM_1 schematic)		
I0 (test_ms55 OSC10NORM_1 PLS_RCMAX_Cc)	PLS_RCMAX_Cc	$simlevel $stop $sch extracte...
V0 (analogLib vdc eldo)		$simlevel $stop $sch extracte...

```
FMP: Unset $ variable TKITCMOS065 at line number 2
    of file /work/dkrun3/VALIDATION/cmos065/QA_PLS_cmos065lpgp_RF_6m4x0y1z_50A28A/sun/EVA/cds.lib
Attempting to lock configuration (test_ms55 tb_OSC10NORM_1 config).
Opened the configuration (test_ms55 tb_OSC10NORM_1 config).
```

Ready... | Filters OFF | NameSpace: CDBA

To simulate view created by PLS, use hierarchy editor (HED) to create a config view.

Use the template adapted to your simulator

Choose the stop view of the cell you want to simulate (stop views are written uppercase)

Don’t forget to update the config view

Then you can simulate it as if it was a schematic.

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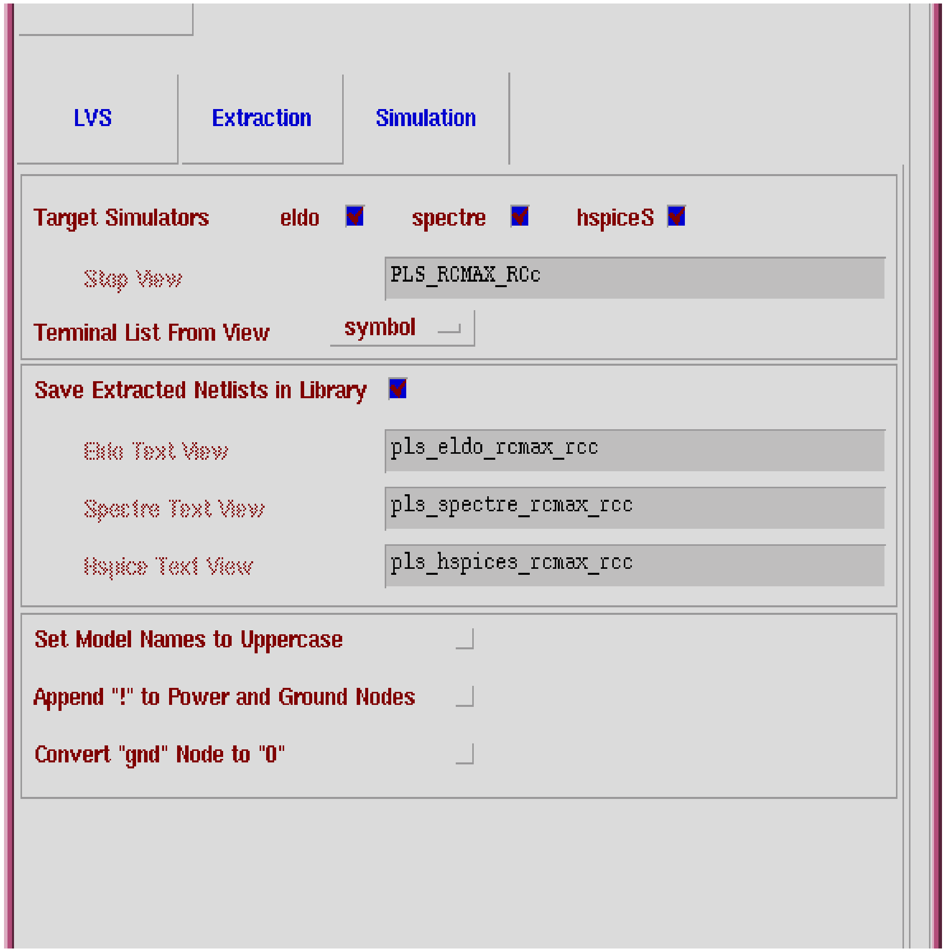
- **Advanced CAD features**

PLS interface Window: Simulation only for textual netlist import flow



Target Simulators eldo ☑ spectre ☑ hspiceS ☑

Stop View PLS_RCMAX_RCc

Terminal List From View symbol

Save Extracted Netlists in Library ☑

Eldo Text View pls_eldo_rcmax_rcc

Spectre Text View pls_spectre_rcmax_rcc

Hspice Text View pls_hspices_rcmax_rcc

Set Model Names to Uppercase ☐

Append "!" to Power and Ground Nodes ☐

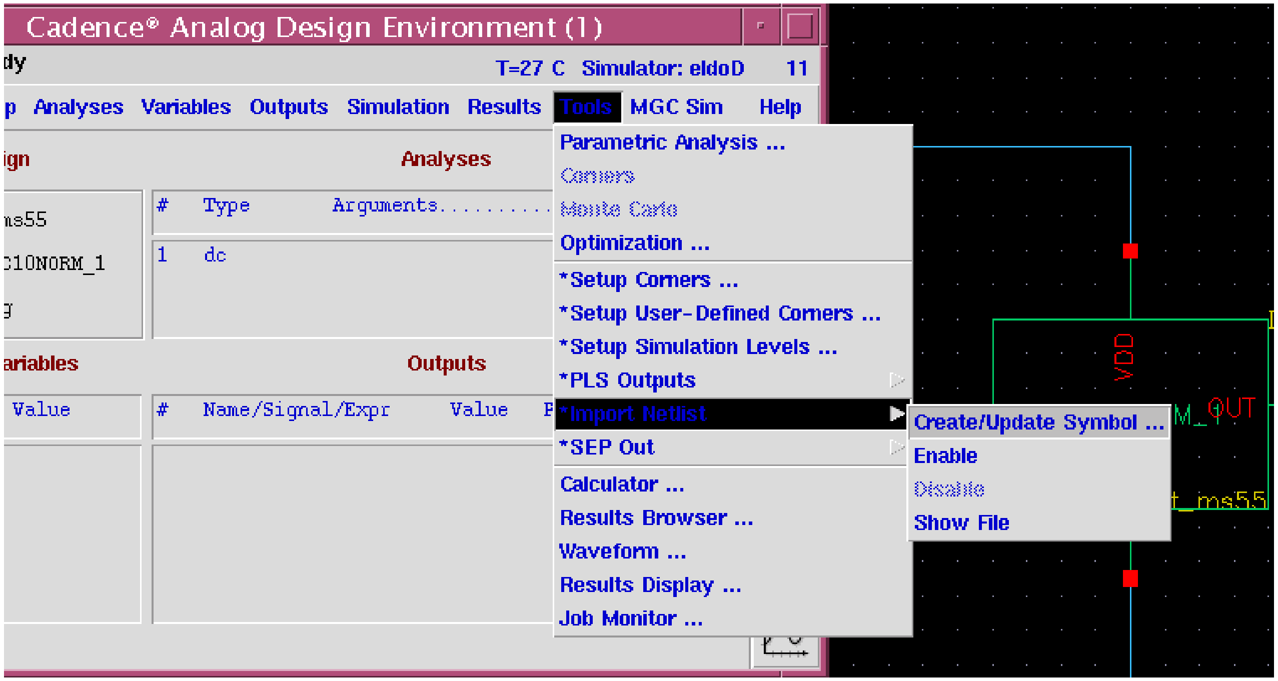
Convert "gnd" Node to "0" ☐

From **Simulation** Tab you can:

- Choose the target **simulator(s)** (Eldo, Spectre, hspiceS)
- Create **Stopviews** in library (<u>uppercase</u> PLS_STRATEGY_MODE)
- Create **netlists** in library (<u>lowercase</u> pls_simulator_strategy_mode)

To run the entire flow just click on <u>Run PLS</u> button.

Link to Simulation: “import netlist” only for textual netlist import flow



To perform the simulation, you need to activate the import netlist capability.

Then do a check and save of the config view.

The others simulation settings are the same as for a standard schematic

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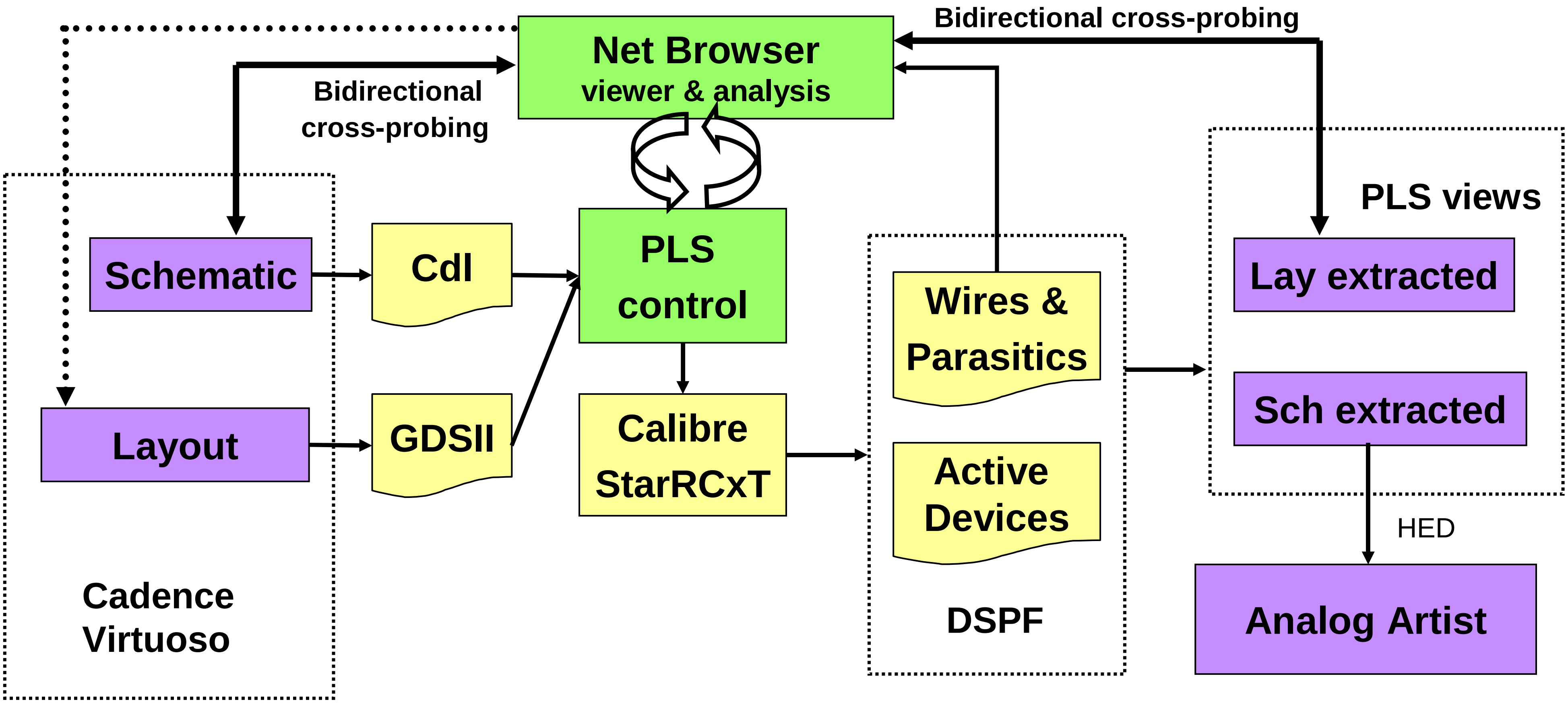
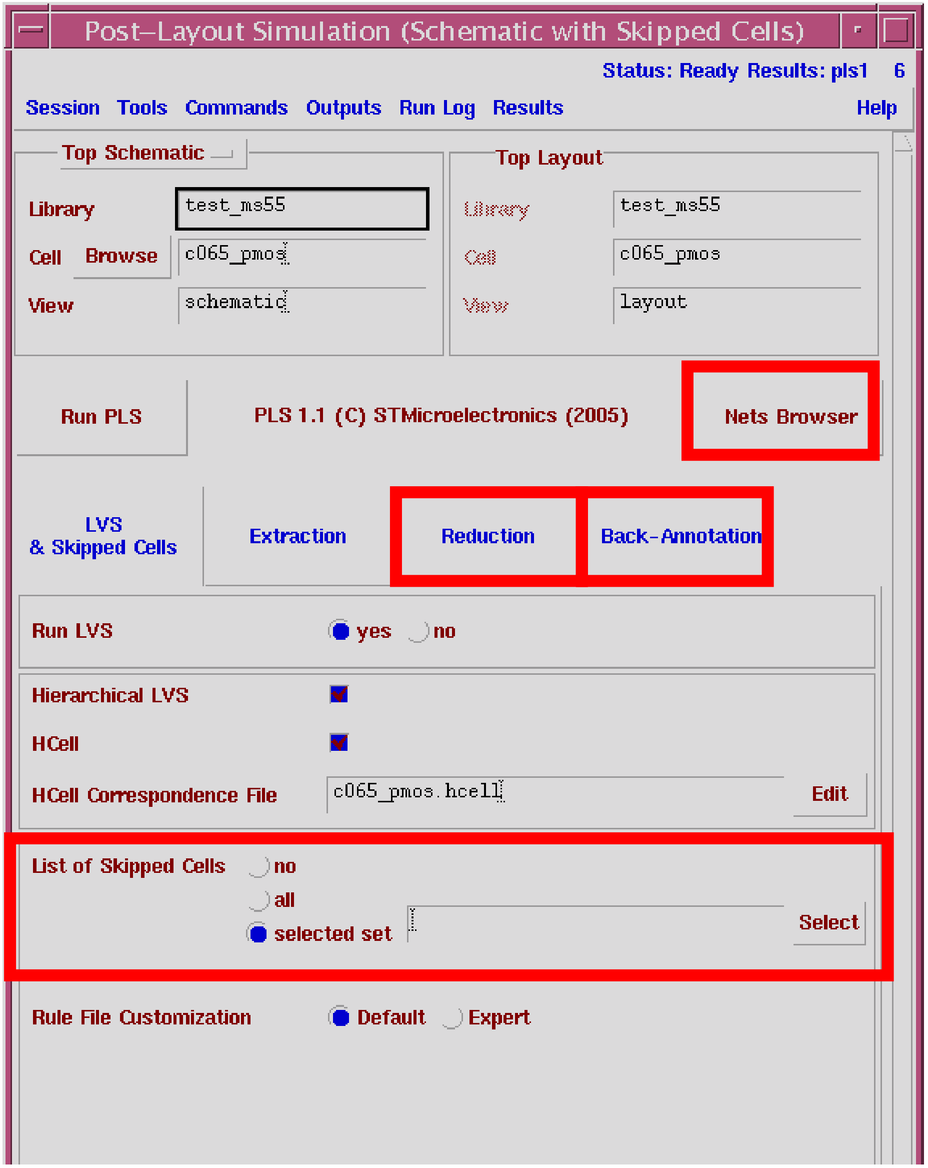
- **Advanced CAD features**

PLS Flow based on DSPF

Net selection / probing / highlighting



PLS Environment



Status: Ready Results: pls1 6

Top Schematic

Library test_ms55

Cell c065_pmos

View schematic

Top Layout

Library test_ms55

Cell c065_pmos

View layout

PLS 1.1 (C) STMicroelectronics (2005)

Run LVS ● yes ○ no

Hierarchical LVS ☑

HCell ☑

HCell Correspondence File c065_pmos.hcell

List of Skipped Cells ○ no ○ all ● selected set

Rule File Customization ● Default ○ Expert

Specific features for “DSPF Skipcells” flow :

Main changes:

•SkipCell option

•Net Browser button

•Reduction tab menu

•Back-Annotation options : extracted views

•Cross probing

Skipcell:

skip cells options for filtering a part of a design.

Warning: Skip Cells should be declared according to sub-set cells of the hcell list.

EXTRACTION TAB MENU: unchanged

PLS interface Window: Skipcell

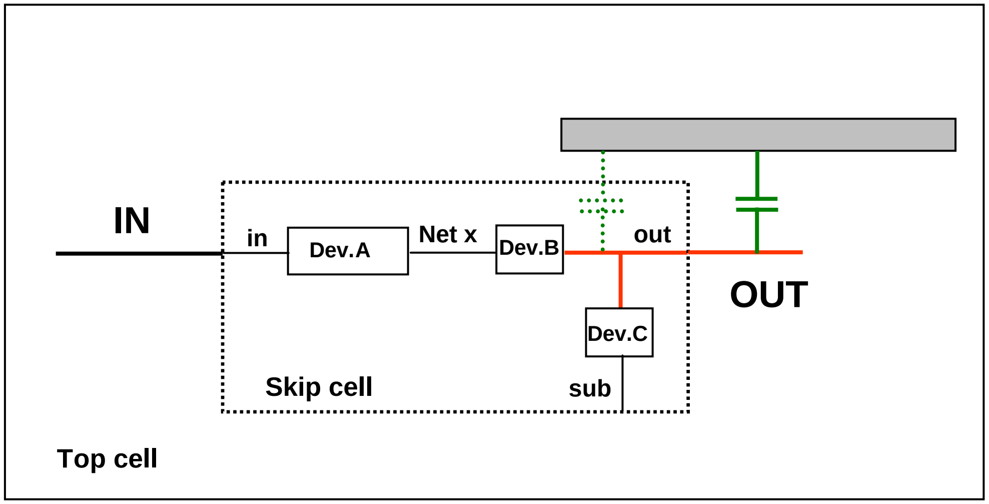
Skipcell:

skip cells options for filtering a part of a design.

-Capacitors from skipped cells will be lumped

-Resistors still extracted from top ports to devices terminals of the skipped cell. The device terminal is the stopping point of the extracted resistive path, not the pin of the cell. No resistor extraction for internal nets of the skipped cell nor for nets not declared in the netfile.

Warning: Skip Cells should be declared according to sub-set cells of the hcell list.



Netfile :
*schematic-net-name
OUT

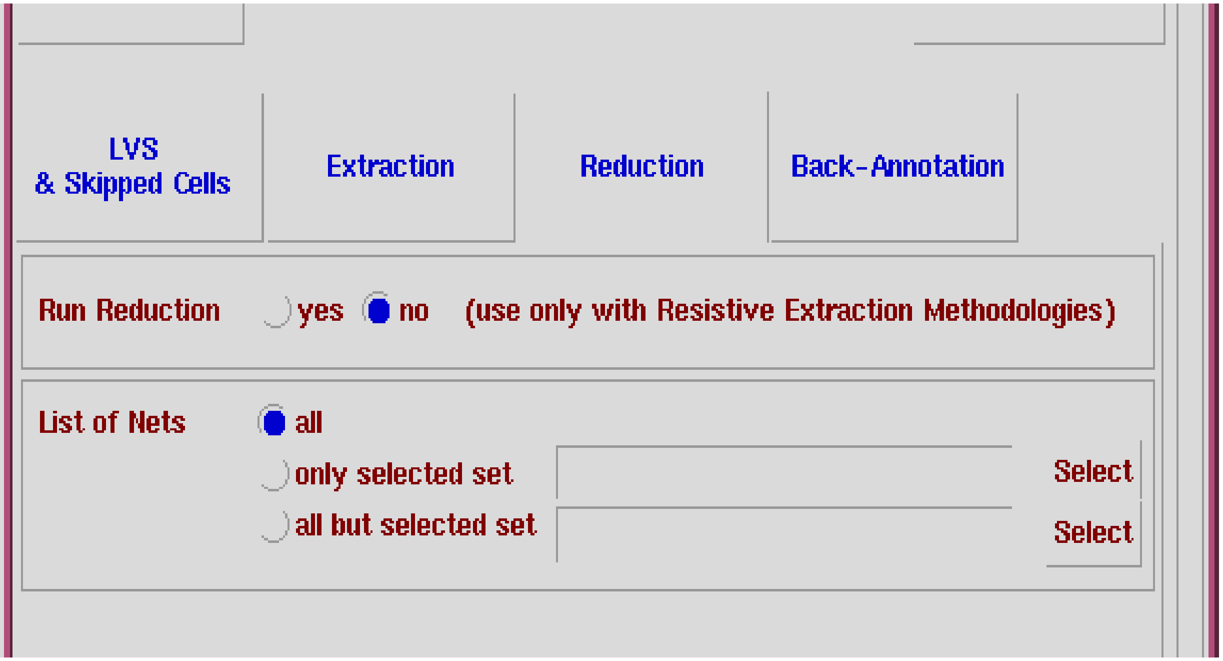
Lumped Capacitor

Extracted Capacitor

Resistor network extraction

No Resistor extraction

PLS interface Window: Reduction



Run Reduction ○ yes ● no (use only with Resistive Extraction Methodologies)

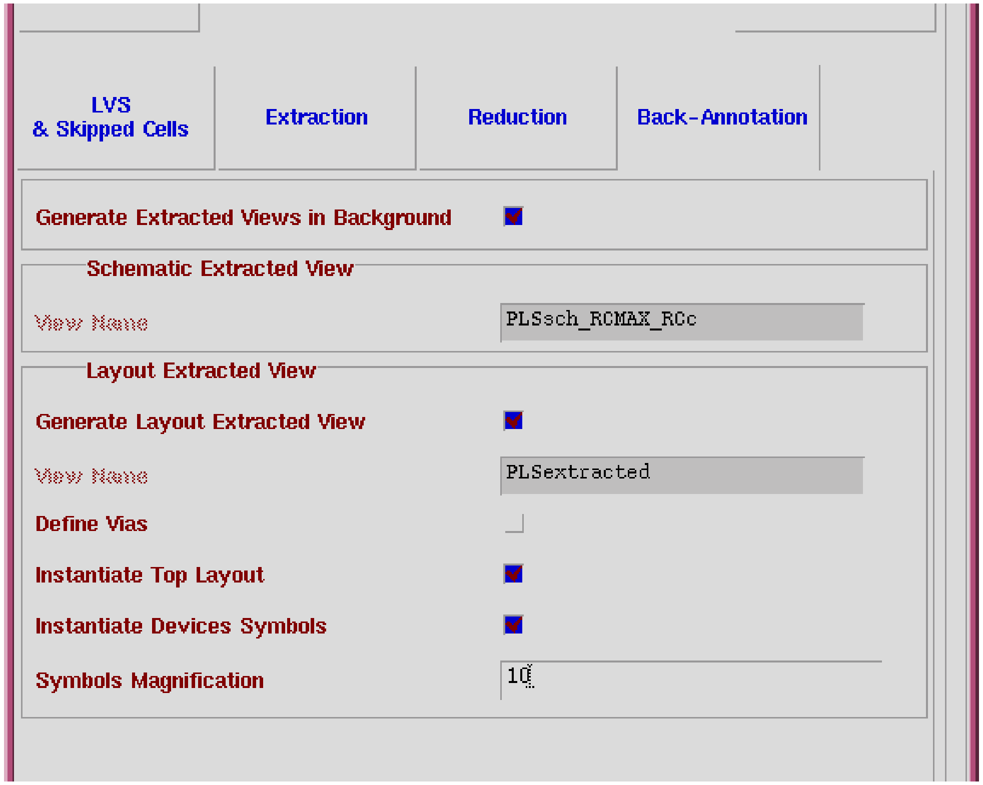
List of Nets ● all
○ only selected set
○ all but selected set

In **Reduction** Tab you can:

- Activate **Resistance network reduction**
- Choose list of nets where reduction has to be applied

Warning: Reduction is efficient only with R or RC extraction mode

PLS interface Window: Back-Annotation



Generate Extracted Views in Background ☑

Schematic Extracted View

View Name: PLSsch_RCMAX_RCc

Layout Extracted View

Generate Layout Extracted View ☑

View Name: PLSextracted

Define Vias □

Instantiate Top Layout ☑

Instantiate Devices Symbols ☑

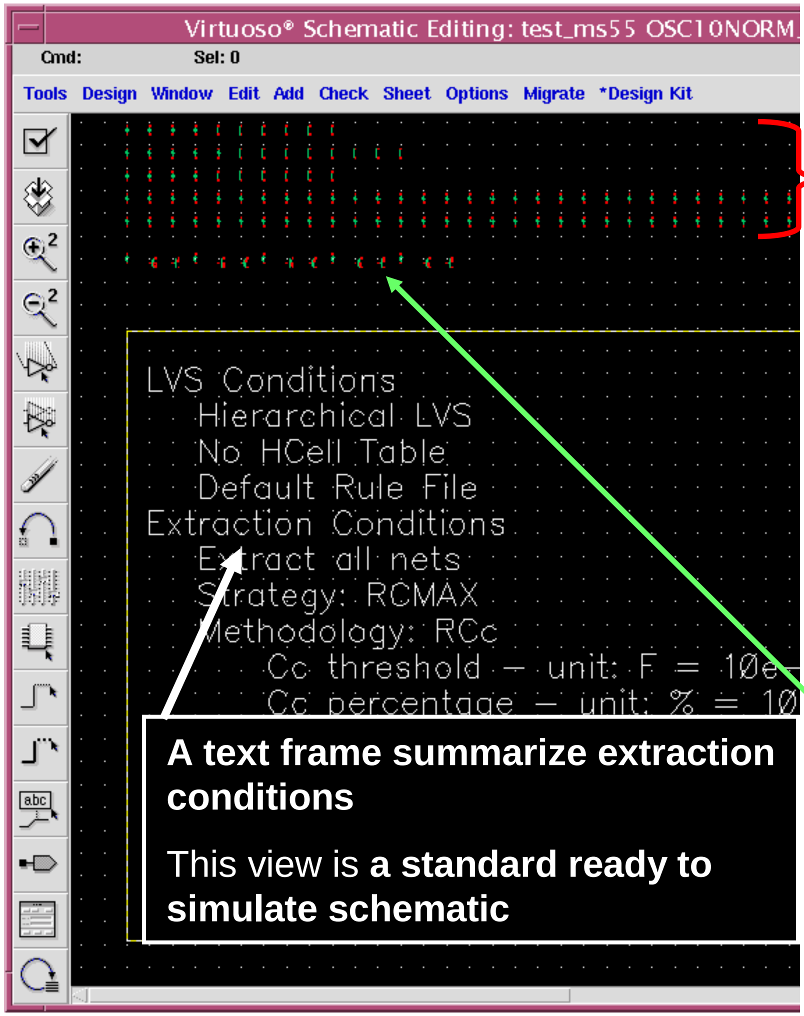
Symbols Magnification: 10

From **Back-Annotation** Tab you can:

- Choose to generate extracted views in a
  - foreground mode; better suited for small designs
  - background cadence session; for big designs (Warning : flow is closing library manager)
- Choose the name of the extracted schematic view: default is PLSsch_STRATEGY_MODE
- Choose to generate layout extracted view
- Choose option about this view
  - Include via
  - Instantiate top
  - Instantiate symbols with size option

To run the entire flow just click on <u>Run PLS</u> button

Extracted Schematic view



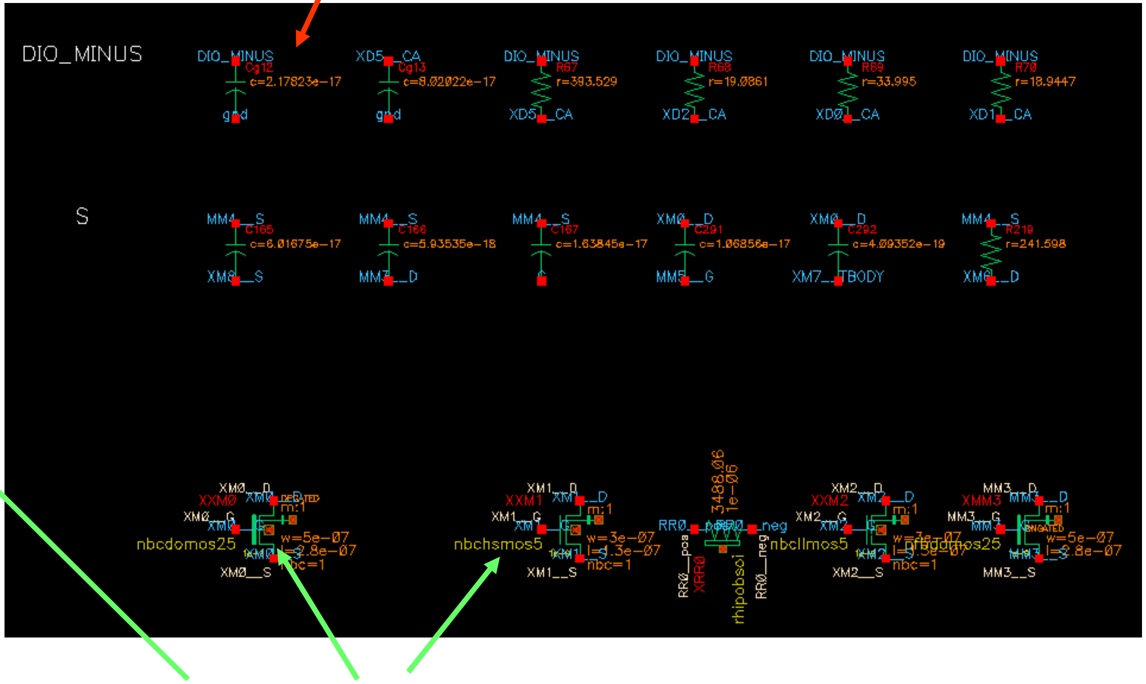
```
LVS Conditions
    Hierarchical LVS
    No HCell Table
    Default Rule File
Extraction Conditions
    Extract all nets
    Strategy: RCMAX
    Methodology: RCc
        Cc threshold – unit: F = 10e
        Cc percentage – unit: % = 10
```

A text frame summarize extraction conditions

This view is **a standard ready to simulate schematic**

On top of the schematic the **design ports** are gathered

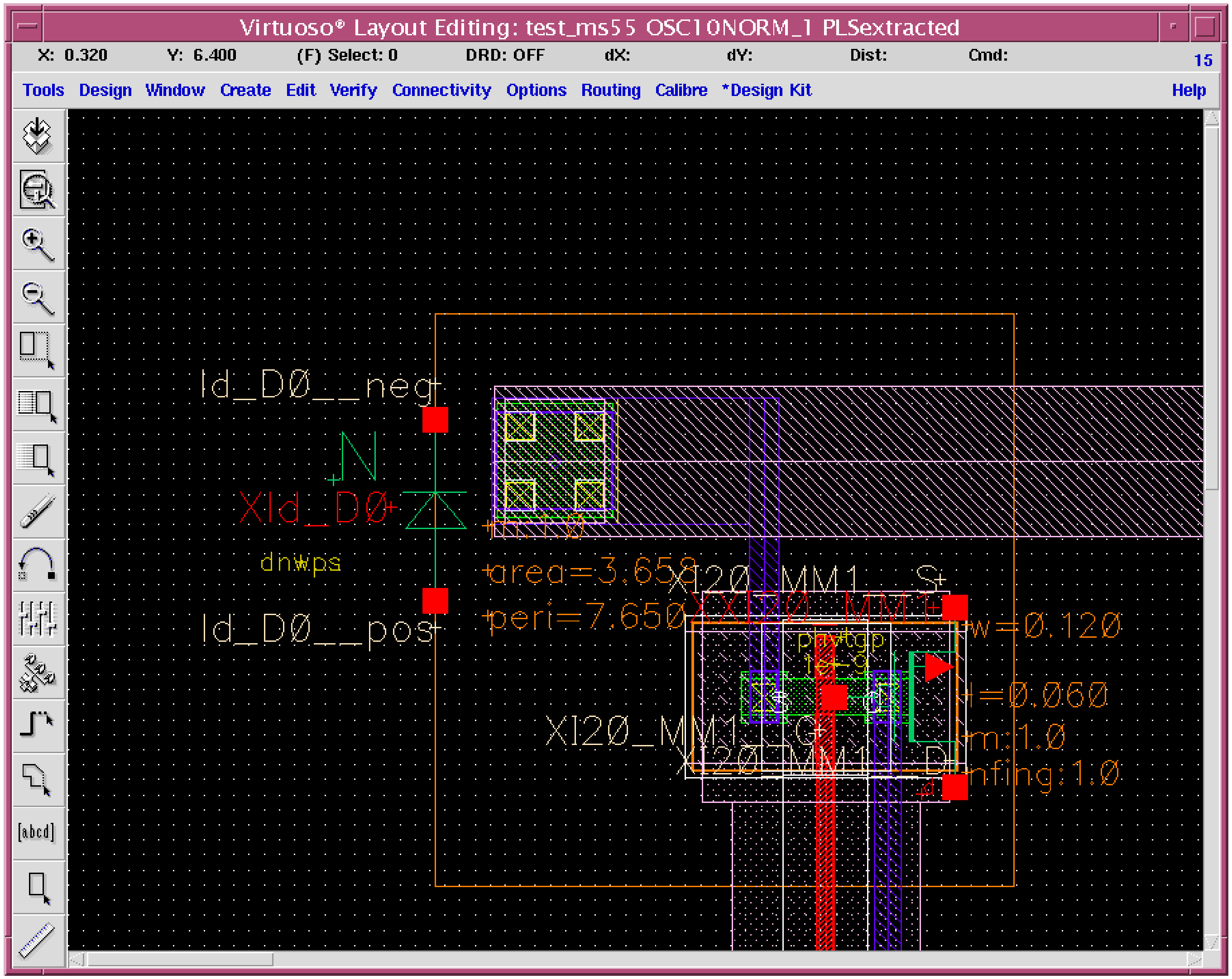
Parasitics elements are **sorted by net names,** one line for each net



Devices are gathered **at the end** of the schematic

All **connections** are made **by net labels**

Extracted Layout view



Virtuoso® Layout Editing: test_ms55 OSC10NORM_1 PLSextracted

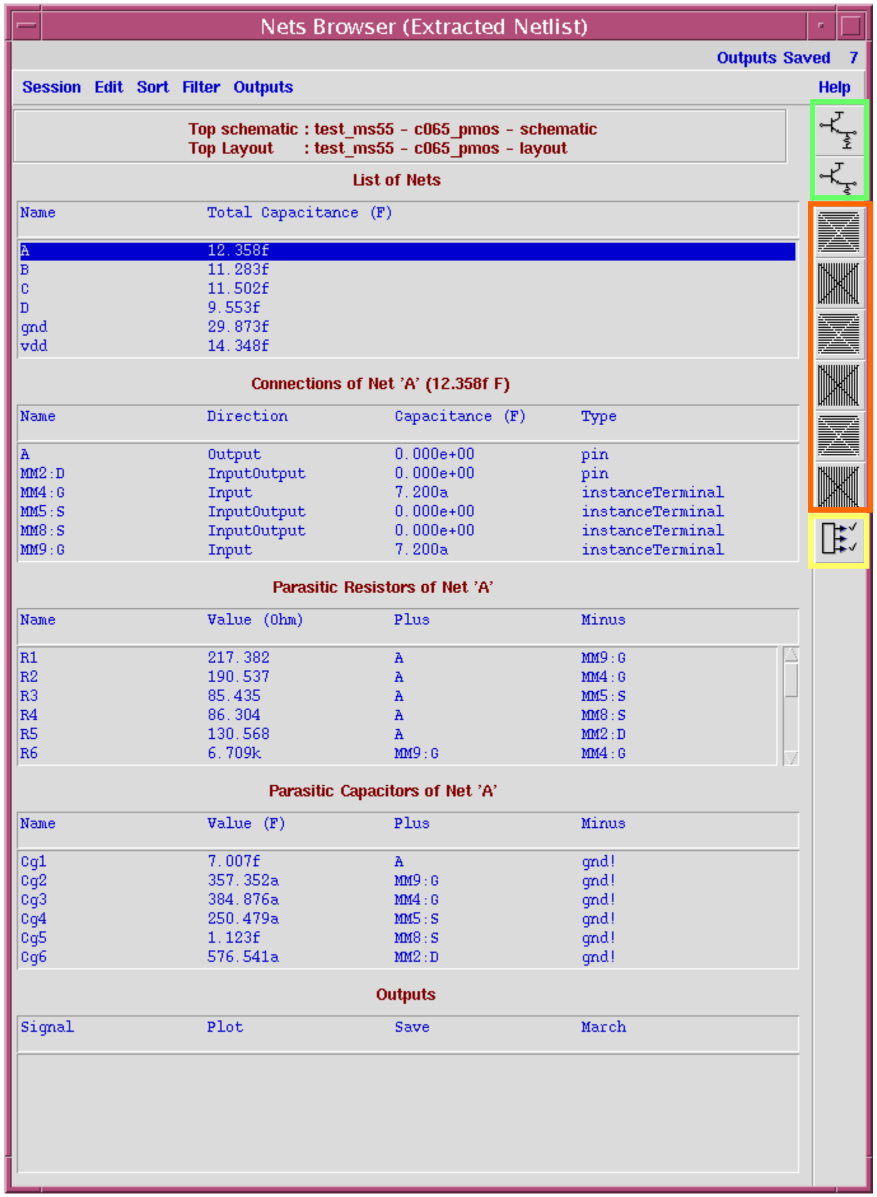
X: 0.320 Y: 6.400 (F) Select: 0 DRD: OFF dX: dY: Dist: Cmd: 15

Layout extracted view is a hierarchical layout view that includes:

- The design layout in a lower hierarchy
- The extracted connections
- the symbols and properties of extracted devices

This view gives an overview of what is really extracted by PLS flow.

Net Browser


Nets Browser (Extracted Netlist)
Outputs Saved 7
Session Edit Sort Filter Outputs
Help

Top schematic : test_ms55 – c065_pmos – schematic
Top Layout : test_ms55 – c065_pmos – layout

List of Nets

Name	Total Capacitance (F)
A	12.358f
B	11.283f
C	11.502f
D	9.553f
gnd	29.873f
vdd	14.348f

Connections of Net 'A' (12.358f F)

Name	Direction	Capacitance (F)	Type
A	Output	0.000e+00	pin
MM2:D	InputOutput	0.000e+00	pin
MM4:G	Input	7.200a	instanceTerminal
MM5:S	InputOutput	0.000e+00	instanceTerminal
MM8:S	InputOutput	0.000e+00	instanceTerminal
MM9:G	Input	7.200a	instanceTerminal

Parasitic Resistors of Net 'A'

Name	Value (Ohm)	Plus	Minus
R1	217.382	A	MM9:G
R2	190.537	A	MM4:G
R3	85.435	A	MM5:S
R4	86.304	A	MM8:S
R5	130.568	A	MM2:D
R6	6.709k	MM9:G	MM4:G

Parasitic Capacitors of Net 'A'

Name	Value (F)	Plus	Minus
Cg1	7.007f	A	gnd!
Cg2	357.352a	MM9:G	gnd!
Cg3	384.876a	MM4:G	gnd!
Cg4	250.479a	MM5:S	gnd!
Cg5	1.123f	MM8:S	gnd!
Cg6	576.541a	MM2:D	gnd!

Outputs

Signal	Plot	Save	March

Net Browser is a set of utilities to study and analyze RC networks in a design:

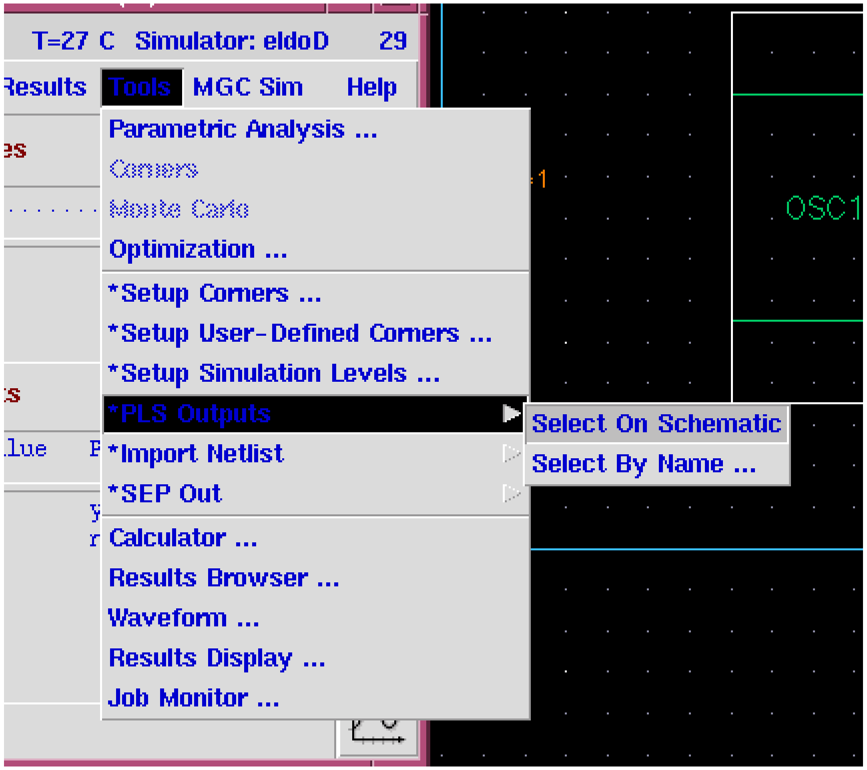
table tools:

- List all nets in design with their **total capacitances**
- When a net is selected, it gives all connections to the net (for R[C[c]] modes), the **coupling and grounded capacitance list** and **resistive network**
- Allows to save any internal **nodes to probe** in simulation (use outputs menu). These nodes can be used later with analog Artist. Current probing is also proposed with PLSKit 1.3 and above
- Results can be sorted according to different filters
- Link to PLSreduce option; to represent R mesh

Highlight tools / cross-probing for every net:

- Layout and schematic highlight from NetBrowser
- Net browser highlight from layout or schematic

Simulation



To run simulation with extracted schematic, a config view is also needed to switch between different PLS modes and corners

The import netlist option is not necessary.

To get nodes to analysed saved in Netlist Browser use the tools->PLS outputs menu

You can then select directly the cell containing the nodes to probe or give its name. All wanted nodes will be added in the probing list.

PLS flows comparison

	Netlist import	**DSPF skipcells**
Integration	☹ Cumbersome import netlist	☺ Schematic extracted view
Device Models management	☹ Only level std	☺ Through Hierarchy Editor
Multi-simulator	Netlist translation	Std netlisting
Net Browser	☹ No	☺ Yes
Probing	☹ Only pins	☺ Any internal connection
Top level extraction	☹ Flat	☺ Hierarchical with Skip Cell

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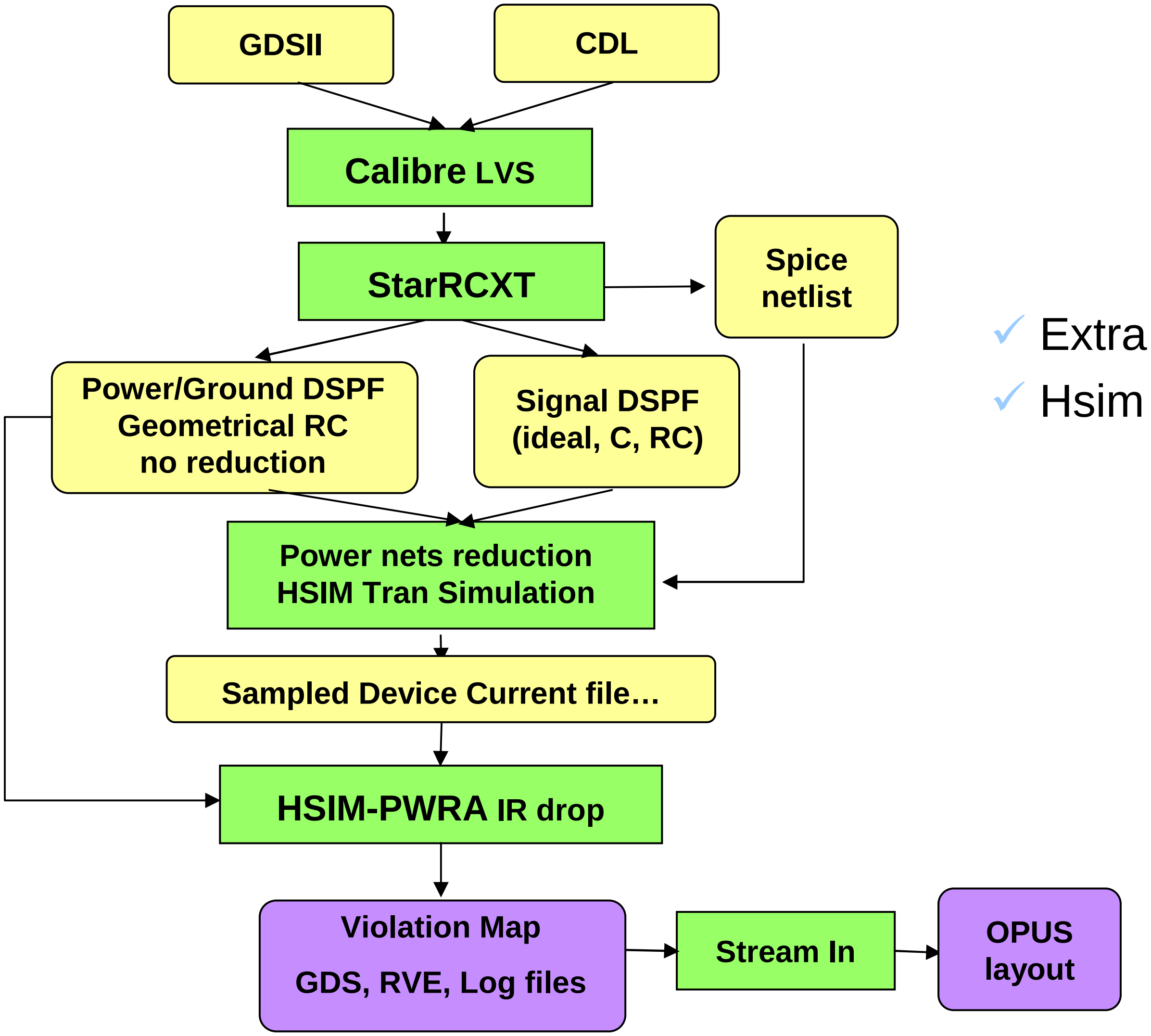
  - ➢ Opus integration
    - ✓ Textual Netlist Import
    - ✓ Schematic With Skip Cells
    - ✓ DSPF with IRdrop
  - ➢ Stand alone GUI
  - ➢ Batch mode
- **Advanced CAD features**

DSPF with IRdrop flow
Support of Hsim-PWRA

- PLSinit: independent signals and power net selection
- PLSextract: performs 2 StarRCXT extractions
  - **Signal nets**: C, Cc, RC, RCc extraction modes with reduction
  - **Power nets**: R, RC, RCc extraction modes without reduction
- Output files:
  - 2 DSPF files: one for signal and one for power/ground nets
  - a Spice Ideal netlist (IDEAL.SPI)
  - a DSPF_INCLUDE file with include Spice and DSPF commands
- Opus integration:
  - new DSPF with IRdrop flow (similar to Import Netlist)
  - new stop-view DSPF_INCLUDE in order to include all files
  - supports skipped cells
  - Signal Browser

Dynamic Transistor Level IR-Drop with HSIM-PWRA


GDSII
CDL
Calibre LVS
StarRCXT
Spice netlist
Power/Ground DSPF Geometrical RC no reduction
Signal DSPF (ideal, C, RC)
Power nets reduction HSIM Tran Simulation
Sampled Device Current file…
HSIM-PWRA IR drop
Violation Map
GDS, RVE, Log files
Stream In
OPUS layout

- ✓ Extra option of Hsim
- ✓ Hsim 5.0

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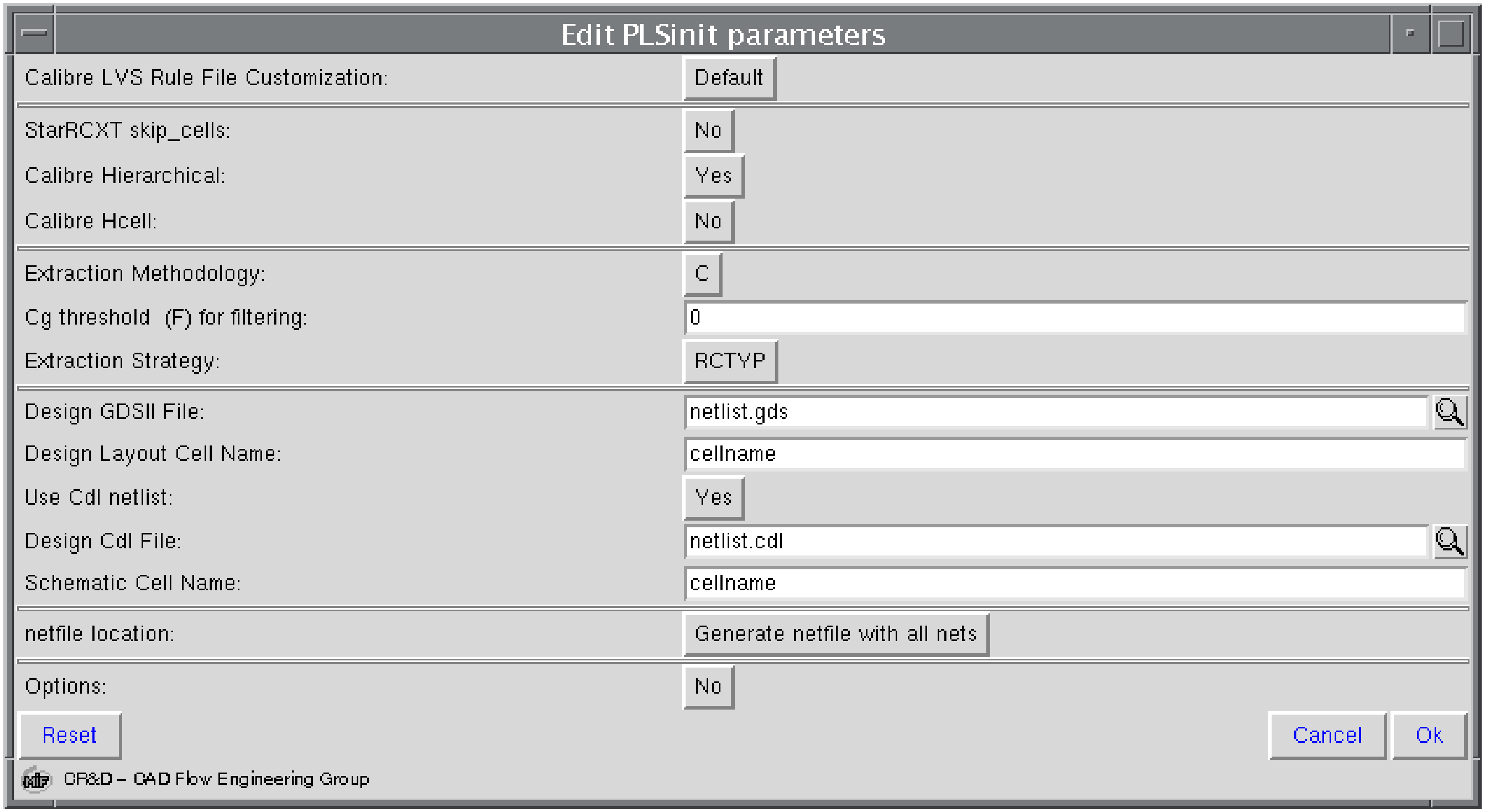
PLSinit Graphical User Interface

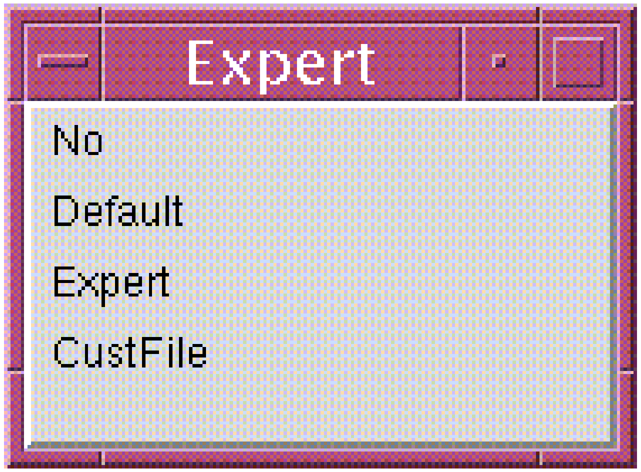
- PLSinit -gui



Calibre LVS Rule File Customization:	Default
StarRCXT skip_cells:	No
Calibre Hierarchical:	Yes
Calibre Hcell:	No
Extraction Methodology:	C
Cg threshold (F) for filtering:	0
Extraction Strategy:	RCTYP
Design GDSII File:	netlist.gds
Design Layout Cell Name:	cellname
Use Cdl netlist:	Yes
Design Cdl File:	netlist.cdl
Schematic Cell Name:	cellname
netfile location:	Generate netfile with all nets
Options:	No

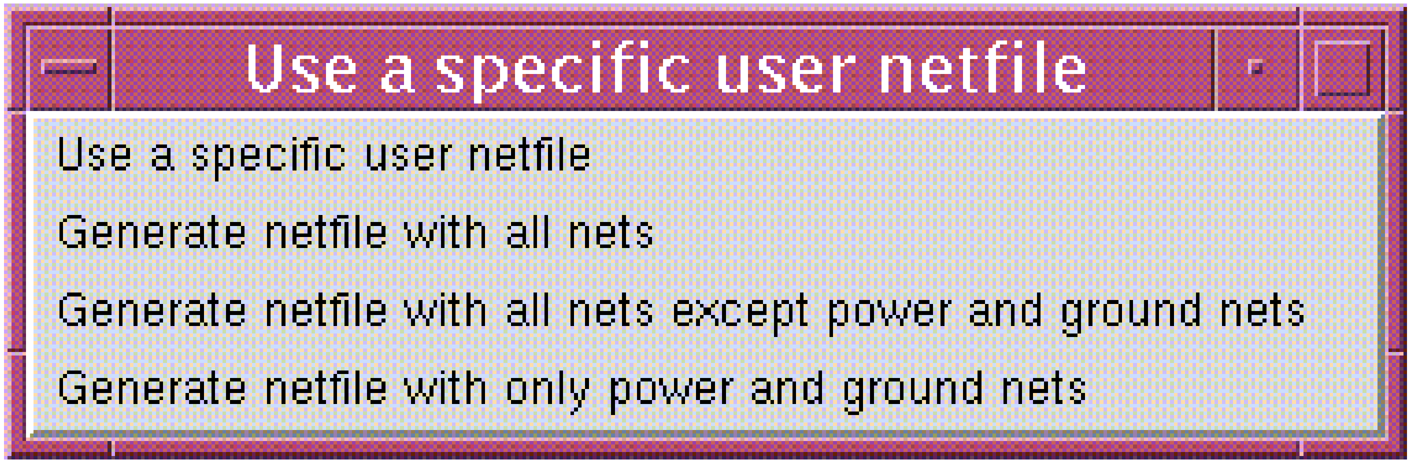
PLSinit: LVS customization

- PLSinit -gui : LVS Customization
  - Default: LVS default parameters
  - Expert: LVS customization such as
    - ✓ Hierarchical or flat LVS
    - ✓ Virtual connect names..
  - No: no new customization in case of new PLSinit run
  - Custfile: usage of an old customized lvs deck (batch mode application)



PLSinit: netfiles

- PLSinit -gui : netfiles
  - Use a specific user netfile -> **default**
  - Generate netfile with all nets
  - Generate netfile with all nets except power and ground nets
  - Generate netfile with only power and ground nets



Use a specific user netfile

Use a specific user netfile

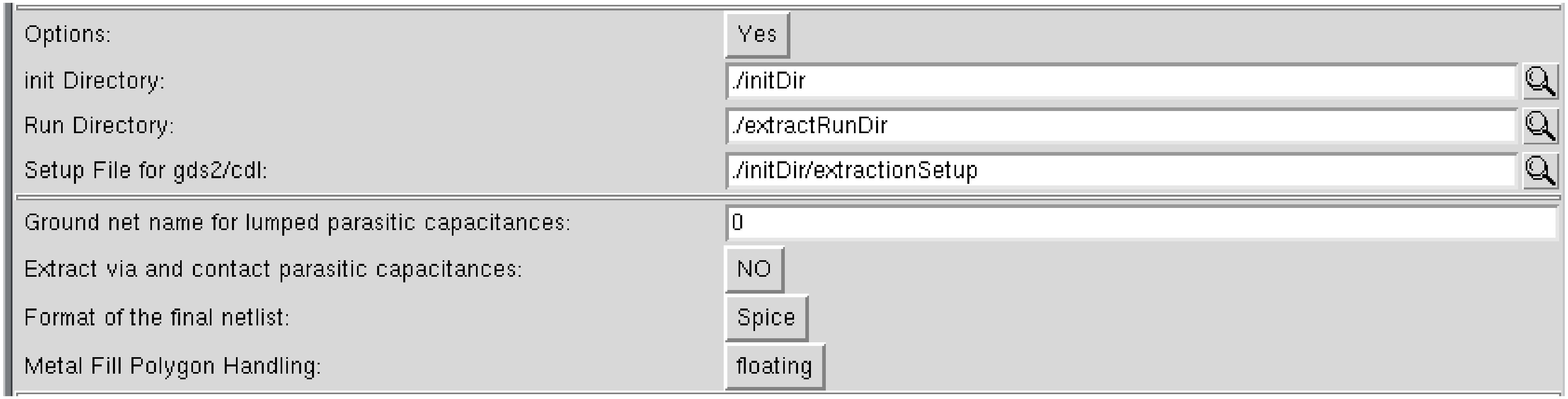
Generate netfile with all nets

Generate netfile with all nets except power and ground nets

Generate netfile with only power and ground nets

PLSinit: Options

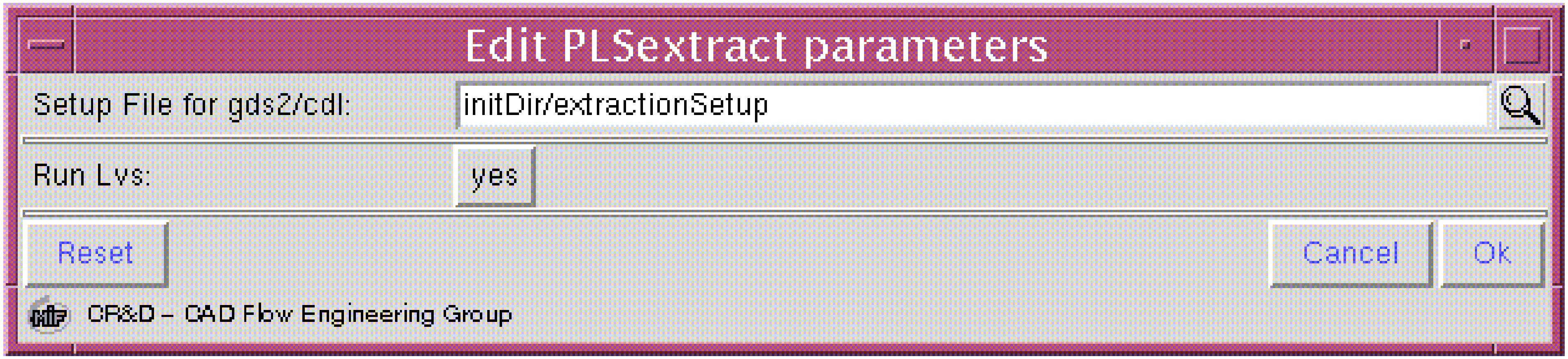
- PLSinit -gui : options
  - Init/Run directories setup
  - Ground Net name for lumped Capacitors
  - Extract via capacitances : YES / NO
  - Output format: Spice / DSPF
  - Metal Fill Polygon Handling : floating/ignore/grounded
  - Temperature (deg. C)



Options:	Yes
init Directory:	./initDir
Run Directory:	./extractRunDir
Setup File for gds2/cdl:	./initDir/extractionSetup
Ground net name for lumped parasitic capacitances:	0
Extract via and contact parasitic capacitances:	NO
Format of the final netlist:	Spice
Metal Fill Polygon Handling:	floating

PLS Graphical User Interface

- PLSextract -gui



Edit PLSextract parameters

Setup File for gds2/cdl: initDir/extractionSetup

Run Lvs: yes

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PLSinit batch mode

- PLSinit -h

```
 PLSinit [-custLvs <No|Default|Expert|CustFile>]
        [-custLvsFile <path>] [-skipcells <Yes|No>] [-skipcellsPath <path>]
        [-calibreHier <Yes|No>] [-calibreHcell <Yes|No>]
        [-calibreHcellPath <path>]
        [-extractionMethod <RCc|Cc|RC|C|R|Mixed|FSextract|NoRC>]
        [-conlythreshold <float>] [-ccthreshold <float>] [-ccpercentage <float>]
        [-fsOptPercentage <float>] [-fsOptCapacitance <float>]
        [-fsOptRunTime <float>] [-strategy <RCMAX|RCTYP|RCMIN>]
        [-gdsFile <path>] [-gdsCellName <string>] [-cdl <Yes|No>]
        [-cdlFile <path>] [-cdlCellName <string>] [-skipNetFile <path>]
        [-net <Use a specific user netfile|Generate netfile with all nets|Generate netfile with all nets except
power and ground nets|Generate netfile with only power and ground nets>]
        [-netFile <path>] [-net_C <path>] [-net_Cc <path>] [-net_R <path>]
        [-net_RC <path>] [-net_RCc <path>] [-net_Std <path>]
        [-net_FSextract <path>] [-options <Yes|No>] [-initDir <path>]
        [-runDir <path>] [-setupFile <path>] [-groundNetName <string>]
        [-extractViaCaps <YES|NO>] [-format <Spice|DSPF>]
        [-dspfinstsection <YES|NO>] [-dspfreliability <YES|NO>]
        [-dspfconversion <YES|NO>] [-dspfbacktype <extracted|schematic>]
        [-temperature <string>] [-metalfill <floating|grounded|ignore>]
        [-help|-h|-u|-U] [-gui] [-version]
```

PLSinit batch mode

- PLSinit -h

```
-custLvs          Calibre LVS Rule File Customiszation. Default is 'Default'.
-custLvsFile      Switches definition File for Calibre Customization.
-skipcells        StarRCXT skip_cells. Default is 'No'.
-skipcellsPath    StarRCXT skip_cells File Path. Default is 'skipcellsfile'.
-calibreHier      Calibre Hierarchical. Default is 'Yes'.
-calibreHcell     Calibre Hcell. Default is 'No'.
-calibreHcellPath Calibre Hcell File Path. Default is 'hcellfile'.
-extractionMethod Extraction Methodology. Default is 'Cc'.
-conlythreshold   Cg threshold  (F) for filtering. Default is '0'.
-ccthreshold      Cc threshold  (F) for filtering. Default is '10e-15'.
-ccpercentage     Cc percentage (%) for filtering. Default is '10'.
-fsOptPercentage  Relative accuracy goal (%). Default is '1'.
-fsOptCapacitance Capacitance accuracy goal (fF). Default is '1'.
-fsOptRunTime     Run time limit (Hours). Default is '24'.
-strategy         Extraction Strategy. Default is 'RCMAX'.
-gdsFile          Design GDSII File. Default is 'test.gds'.
-gdsCellName      Design Layout Cell Name. Default is 'test'.
-cdl              Enable selection of Cdl File. Default is 'Yes'.
-cdlFile          Design Cdl File. Default is 'test.cdl'.
-cdlCellName      Schematic Cell Name. Default is 'test'.
-skipNetFile      Skipped Cells Netlist File. Default is 'skip.cdl'.
-help|-h|-u|-U    Display the script usage.
-gui              Graphical user interface.
-version          Display the script version.
```

```
-net              netfile location. Default is 'Use a specific user netfile'.
-netFile          netfile path. Default is 'netfile'.
-net_C            Net-to-ground coupling netfile location. Default is 'net_C'.
-net_Cc           Net-to-net coupling netfile location. Default is 'net_Cc'.
-net_R            Resistance netfile location. Default is 'net_R'.
-net_RC           Resistance & net-to-ground coupling netfile location. Default is 'net_RC'.
-net_RCc          Resistance & net-to-net coupling netfile location. Default is 'net_RCc'.
-net_Std          Standard netfile path. Default is 'net_Std'.
-net_FSextract    FSextract netfile path. Default is 'net_FSextract'.
-options          Options. Default is 'No'.
-initDir          Init Directory for Rules and technology files. Default is './initDir'.
-runDir           Run Directory. Default is './extractRunDir'.
-setupFile        Setup File for gds2/cdl. Default is './initDir/extractionSetup'.
-groundNetName    Ground net name for lumped parasitic capacitances. Default is '0'.
-extractViaCaps   Extract via and contact parasitic capacitances. Default is 'NO'.
-format           Format of the final netlist. Default is 'Spice'.
-dspfinstsection  Generate a DSPF file with or without instance section. Default is 'YES'.
-dspfreliability  DSPF with geometrical information and no reduction. Default is 'NO'.
-dspfconversion   DSPF conversion is required for ELDO but not required for HSIM and
NANOSIM. Default is 'YES'.
-dspfbacktype     DSPF backannotation of ideal netlist either extracted or from schematic.
Default is 'extracted'.
-temperature      Temperature (deg. C).
-metalfill        Metal Fill Polygon Handling. Default is 'floating'.
```

PLSinit batch mode

- PLSinit -h

Extra conditions:

-custLvsFile If '$custLvs == "CustFile"'

-skipcellsPath If '$skipcells=="Yes"'

-calibreHier If '$skipcells=="No"'

-calibreHcell If '([info exists calibreHier] && ($calibreHier=="Yes")) && ($skipcells=="No")'

-calibreHcellPath If '(([info exists calibreHier] && ($calibreHier=="Yes")) && ([info exists calibreHcell] && ($calibreHcell=="Yes"))) || ($skipcells=="Yes")'

-conlythreshold If '$extractionMethod == "C"'

-ccthreshold If '($extractionMethod == "RCc") || ($extractionMethod == "Cc") || ($extractionMethod == "Mixed") || ($extractionMethod == "FSextract")'

-ccpercentage If '($extractionMethod == "RCc") || ($extractionMethod == "Cc") || ($extractionMethod == "Mixed") || ($extractionMethod == "FSextract")'

-fsOptPercentage If '($extractionMethod == "FSextract")'

-fsOptCapacitance If '($extractionMethod == "FSextract")'

-fsOptRunTime If '($extractionMethod == "FSextract")'

-cdlFile If '$cdl=="Yes"'

-cdlCellName If '$cdl=="Yes"'

-skipNetFile If '($cdl=="No") && ($skipcells=="Yes")'

-net If '($extractionMethod != "Mixed") && ($extractionMethod != "FSextract")'

-netFile If '($extractionMethod != "Mixed") && ($extractionMethod != "FSextract") && ($net == "Use a specific user netfile")

-net_C If '$extractionMethod == "Mixed"'

-net_Cc If '$extractionMethod == "Mixed"'

-net_R If '$extractionMethod == "Mixed"'

-net_RC If '$extractionMethod == "Mixed"'

-net_RCc If '$extractionMethod == "Mixed"'

-net_Std If '$extractionMethod == "FSextract"'

-net_FSextract If '$extractionMethod == "FSextract"'

-initDir If '$options == "Yes"'

-runDir If '$options == "Yes"'

-setupFile If '$options == "Yes"'

-groundNetName If '$options == "Yes"'

-extractViaCaps If '$options == "Yes"'

-format If '$options == "Yes"'

-dspfinstsection If '($options == "Yes") && ($format=="DSPF")'

-dspfreliability If '($options == "Yes") && ($format=="DSPF") && [regexp ^R $extractionMethod] && ($dspfinstsection=="NO")'

-dspfconversion If '($options == "Yes") && ($format=="DSPF") && ($dspfinstsection=="NO")'

-dspfbacktype If '($options == "Yes") && ($format=="DSPF") && ($dspfinstsection=="NO")'

-temperature If '($options == "Yes")&&0'

-metalfill If '($options == "Yes") && 1'

PLSextract batch mode

- PLSextract -h

```
Usage: PLSextract [-setupFile <path>]  [-lvs < yes | no >]  [-help | -h | -u | -U ]
               [-gui]

where:
       -setupFile          Setup File for gds2/cdl. Default is 'initDir/extractionSetup'.
       -lvs                Run Lvs. Default is 'yes'.
       -help|-h|-u|-U      Display the script usage.
       -gui                Graphical user interface.
```

Batch mode example

```
#!/bin/csh -f

set filelist = `ls design_*.gds | cut -f1 -d"."`

foreach filename ($filelist)

  echo "";echo "Extraction in progress on design : "$filename

  PLSinit -extractionMethod Cc -strategy RCTYP -gdsFile $filename.gds
    gdsCellName $filename -cdlFile $filename.spi -cdlCellName $filename >& PLSinit.log

  PLSextract >& PLSextract.log

  cp ./SPICE.SPI spi_${filename}_LCCTYP.cir

end
```

Table of contents

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- Parasitics extraction tool
  - PLS Flow overview
  - Parasitics computation
  - Main features
- PLS Flow Interface
  - Opus integration
  - Stand alone GUI
  - Batch mode
- Advanced CAD features

Advanced CAD features

- Layout Parasitic Extraction Flag (LPE)
  - ➢ Aimed to have an accurate control on interface between parasitic extraction and devices models
- Blackbox at device level
  - ➢ Management of user device models fully integrated in PLS flow
- StarRCXT files
  - ➢ Information related to main techno files / stress calculation
- Resistors network
  - ➢ resistors networks transformations
- Temperature management
- Tiling management

Advanced CAD features

- Layout Parasitic Extraction Flag (LPE)
- User Defined Devices
- Details on extraction
- Resistors network
- Temperature Management
- Tiling management

LPE: devices vs. interconnects

Problem:

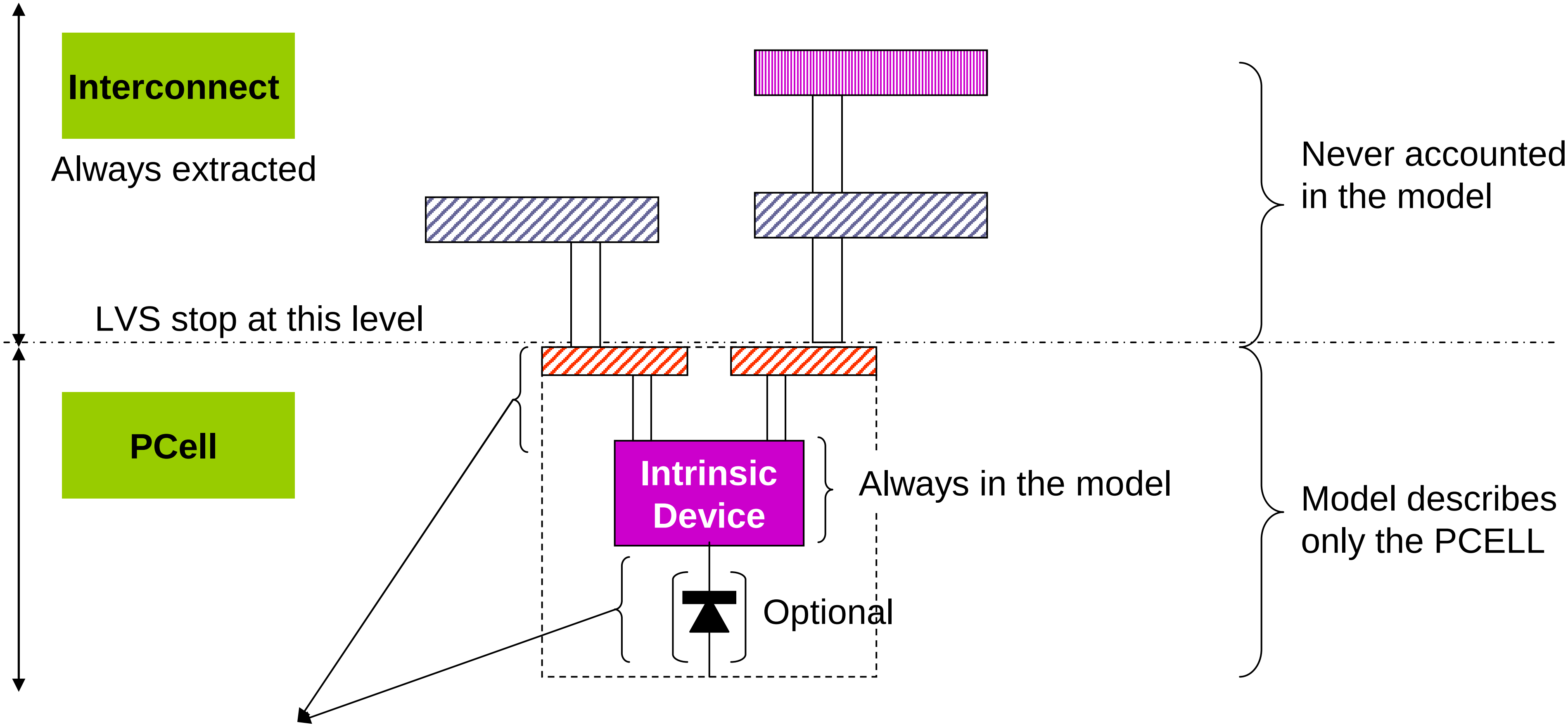
☞ To control the parasitic extraction in order to be consistent with devices models and pre-layout simulations

Solution:

☞ To develop LVS decks in respects with models and post layout extraction needs

☞ Implementation of LPE flag to well control the limit between the devices models and the parasitic network

FE/BE models definition



Interconnect

Always extracted

LVS stop at this level

PCell

Intrinsic Device

Always in the model

Optional

Never accounted in the model

Model describes only the PCELL

Access Parasitics Guessed by the model for Pre-layout accoding to PCell

Extracted in Post-Layout (→ removed from the model) to offer some flexibility to the user

LPE flag: goals

- ***Assumption:***
  - ➢ Devices models are built with the intrinsic device completed by parasitic elements which represent the closed environment (default pcell layout)

- ***Target:***
  - ➢ Allow pre-layout simulation including estimated parasitic elements of the device environment (I.e. full model)
  - ➢ control the interface between devices models and parasitic network (post-layout) I.e.avoid double-counting and “holes”

- ***Method:***
  - ➢ Non modifications on the “physical” model
  - ➢ Rewritten CAD model to support lpe flag
  - ➢ Post-processing of the Post layout netlist to set the lpe flag in respect with the “extraction mode” ➔ fully automated.

LPE flag: values vs. PLS extraction mode

lpe	Body	Access R	Access C	PLS Extraction Mode
0	yes	yes	yes	NoRC / schematic (Pre-layout)
1	yes	yes	no	C, Cc
2	yes	no	yes	R
3	yes	no	no	RC, RCc

- For pre-layout simulation, the default value is used I.e. lpe=0
- For the post-layout simulation, the flag is used as an additional model parameter such as: *XR in out gnd model_name w=1 l=2 lpe=1*

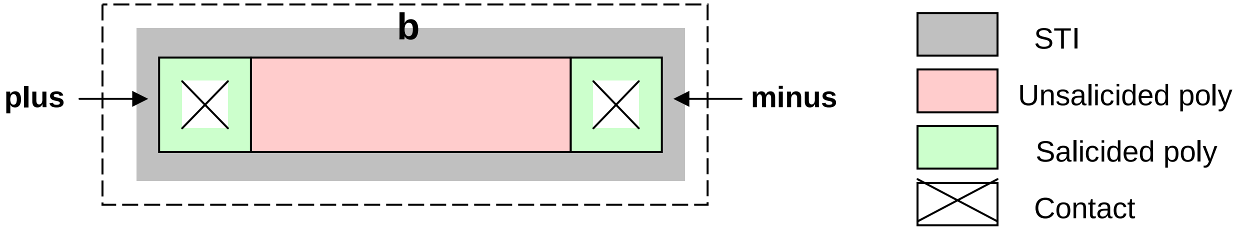
LPE flag: poly resistor model ex

- Model

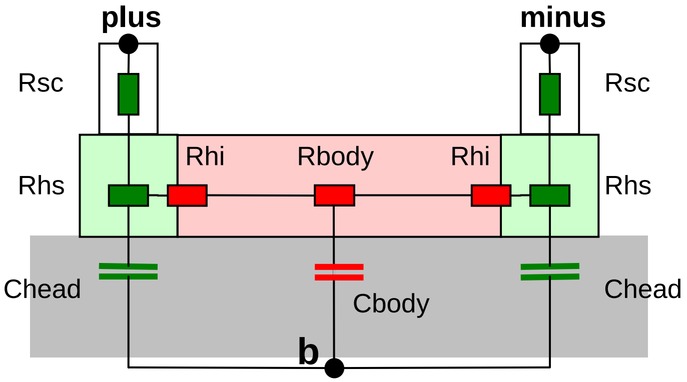
Model(rnpo) = [Rbody + Cbody + 2xRhi] + {2 x [Rsc + Rhs + Chead]} x lpe

Rhi = resistance due to interface between salicided and un-salicided poly

- Layout



- Cross-section



Parasitics :

🟥 always in the model

🟩 managed by LPE flag

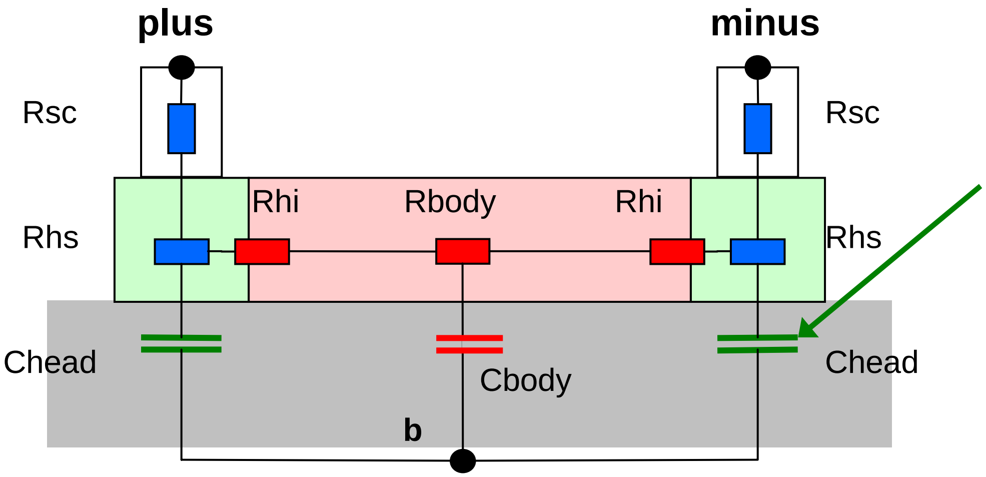
LPE flag: poly resistor extraction

Post layout extraction mode “C”

If we launch a post-layout simulation with a capacitive extraction (lpe = 1), the model will include :

- red resistors AND Rsc + Rhs,
- only the red capacitor Cbody.

Chead will be removed from the final equation of the total device capacitance and will be calculated by the extraction tool.



Chead added by Post-layout extraction

Parasitics :

- 🟥 always in the model
- 🟦 Counted in the model because not extracted
- 🟩 Extracted by the tool

XR plus minus b RPO1 w=x l=y lpe=1

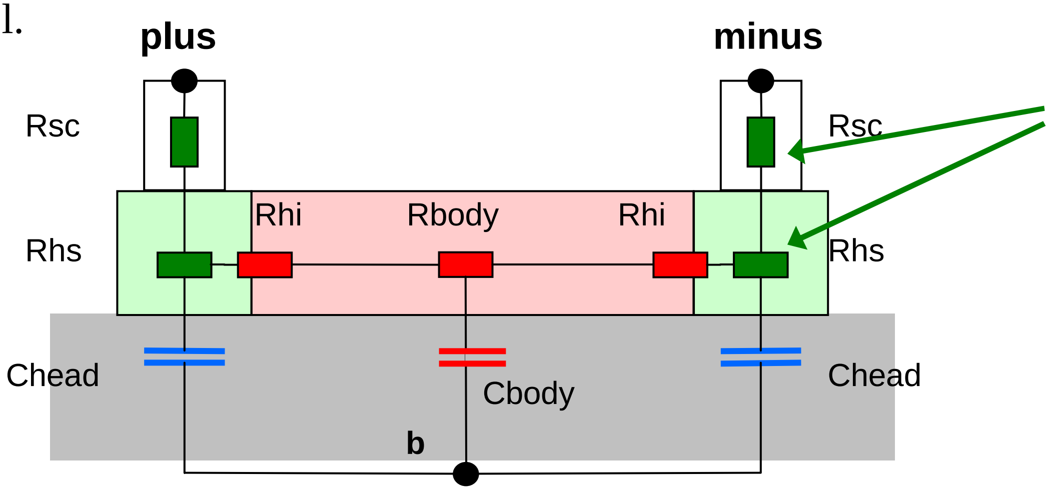
lpe=1 ➔ Model(RPO1)= [Rbody + Cbody + 2xRhi] + 2x[Rsc + Rhs]

LPE flag: poly resistor extraction
Post layout extraction mode “R”

If we launch a post-layout simulation with a resistive extraction (lpe = 2), the model will include :

- only the red resistors,
- the red capacitor Cbody AND Chead.

Rsc and Rhs will be removed from the final equation of the total device resistance and will be calculated by the extraction tool.



Rsc & Rhs added by Post-layout extraction

Parasitics :

🟥 always in the model

🟦 Counted in the model because not extracted

🟩 Extracted by the tool

XR plus minus b RPO1 w=x l=y lpe=2

lpe=2 ➔ Model(RPO1)= [Rbody + Cbody + 2xRhi] + 2 x [Chead]

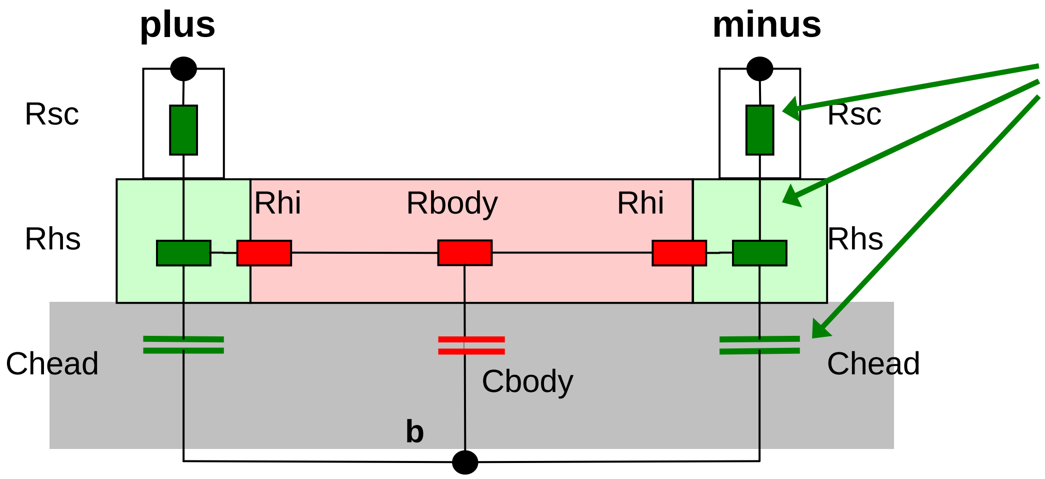
LPE flag: poly resistor extraction

Post layout extraction mode “RC”

If we launch a post-layout simulation with a R&C extraction (lpe = 3), the model will include :

- only the red resistors Rhi,
- only the red capacitor Cbody.

Rsc, Rhs and Chead will be removed from the final equation of the total device resistance and capacitance and will be calculated by the extraction tool.



Rsc & Rhs + Chead added by PLS

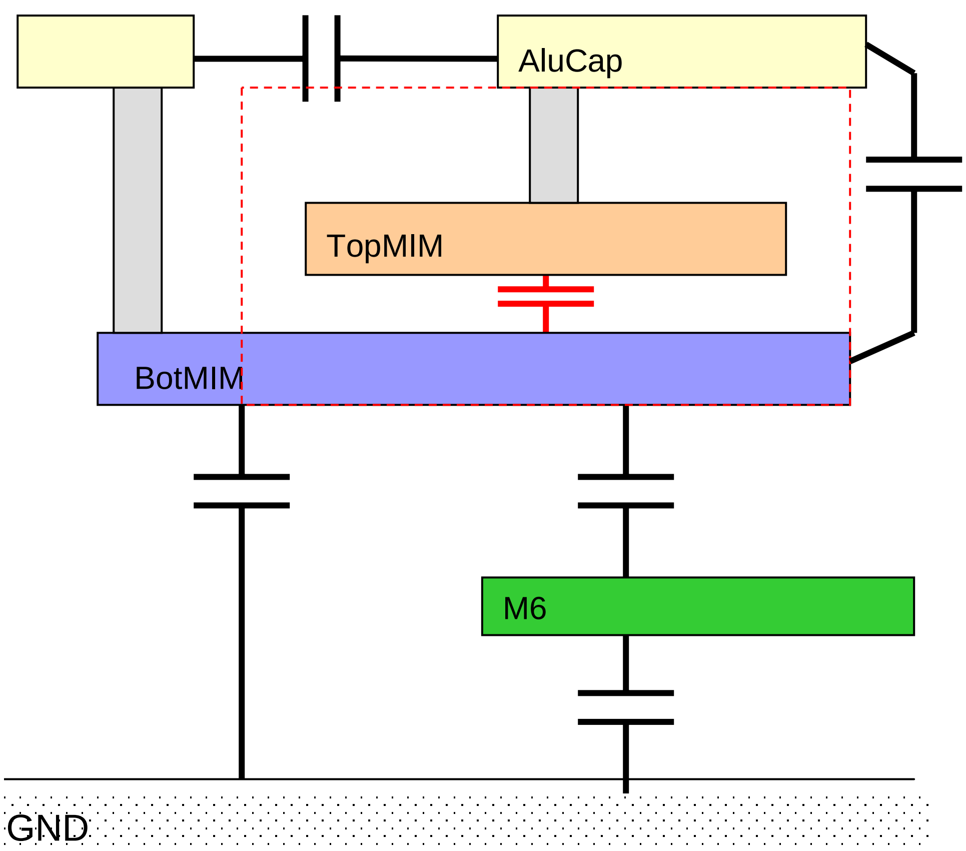
Parasitics :

- 🟥 always in the model
- 🟦 Counted in the model because not extracted
- 🟩 Extracted by the tool

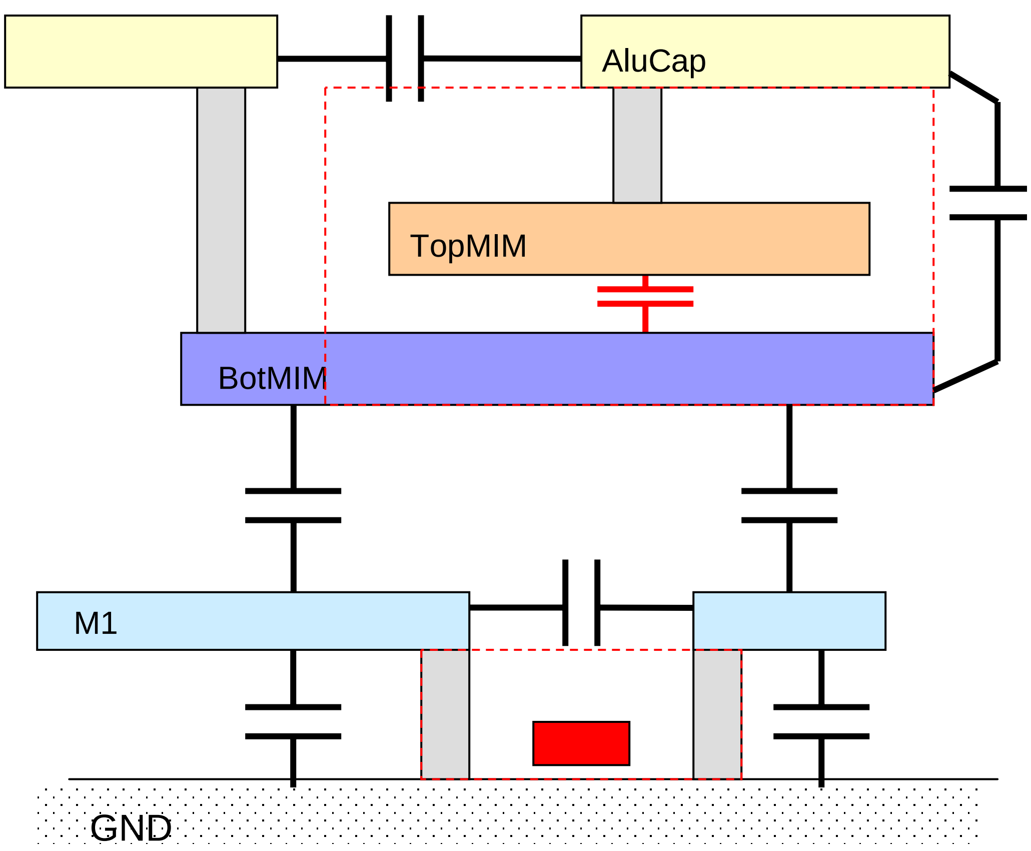
XR plus minus b RPO1 w=x l=y lpe=3

lpe=3 ➔ Model(RPO1)= [Rbody + Cbody + 2xRhi]

LPE flag: MIM capacitor (H9 case)



MIM over interconnects



MIM over Mos

LPE flag: Bipolar transistors

Parasitics :

🟥 always in the model

🟨 managed by LPE flag

🟧 always extracted

Example: BEC structure

Interconnections

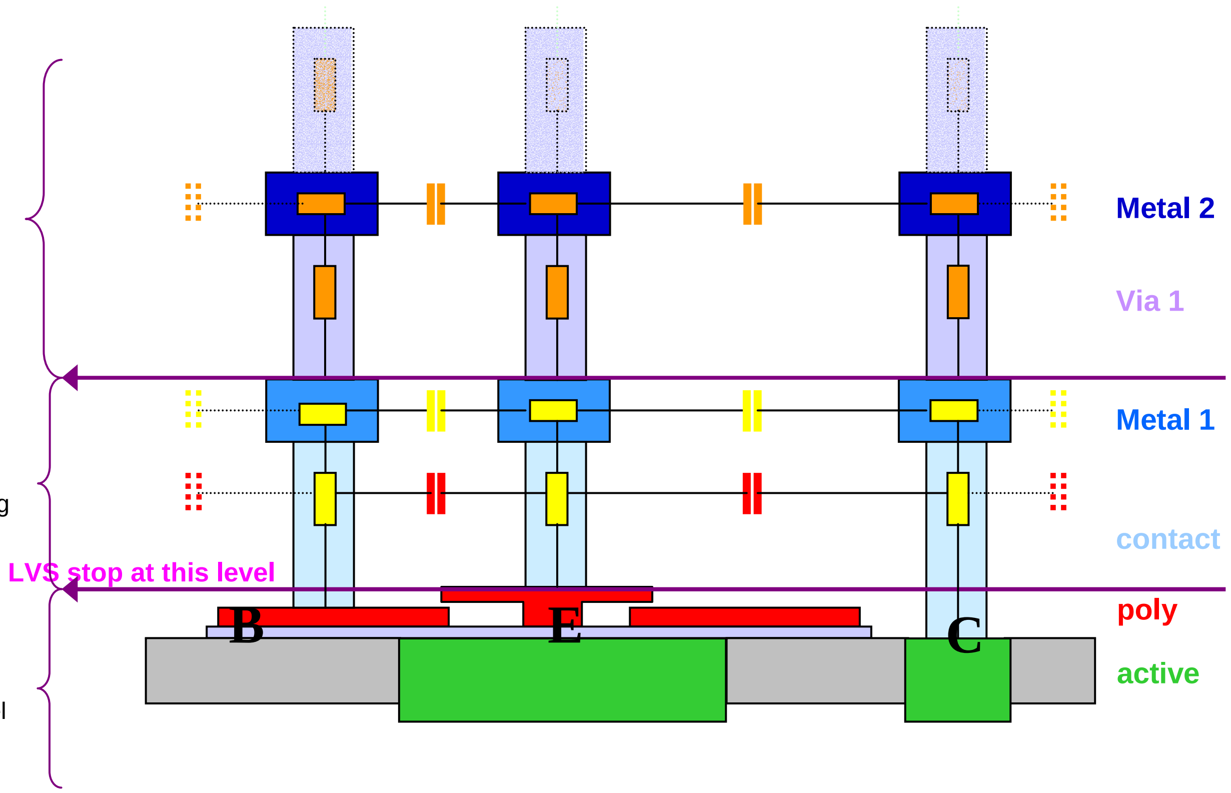
➔ never accounted in the model

Access

➔ managed by LPE flag

Intrinsec device

➔ always in the model



LPE flag processing

- **<u>netfile and strategy taken into account for each device</u>**

- DSPF format (star option “CONNECT SECTION:YES”) allows smart implementation of LPE flag to well control the presence of nets connected to a given device in the netfile. For device whose nets are not all declared in the netfile, lpe value remains 0.

- Post processing automated by a C program named “spfProcess”; no manual step is necessary.

- Limitation: this method is accurate only if all the nets connected to a device are extracted with the same strategy.
  - ➔ Devices models are considered as symetrical : the lpe value is the same for both edges of a resistor.
  - ➔ Specific processing applied for mixed mode

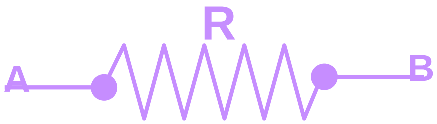
Mixed mode : LPE choice methodology (1/4)

The LPE value for a device is set according the extraction mode realized on nets connected to this device.

- Parsing of DSPF file,
- Storing each connection in spf_net_array table,
- Get extraction mode and list of nets depending on extraction type from StarRCXT command file,
- Set lpe value depending on extraction mode,
- Checking in order to cover the **worst case** (see following table, next page),
  (bulk node is filtered in addLpe function)
- Add "lpe=x" in some devices definitions :

Mixed mode : LPE choice methodology(2/4)

Assume the following resistor with 2 ports A & B and a connection to the bulk:

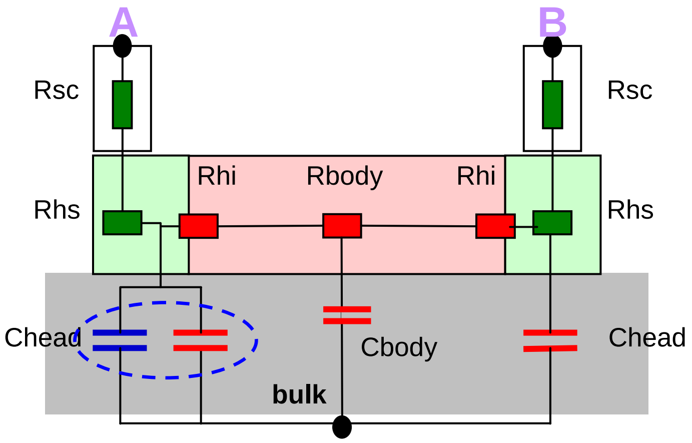


The following table summarizes the LPE value according the extraction mode of each net connected to the resistor :

extraction mode for net A	extraction mode for net B	Resistor LPE value
noRC	noRC	0
	C or Cc	0
	R	0
	RC or RCc	0
C or Cc	C or Cc	1
	R	0
	RC or RCc	1
R	R	2
	RC or RCc	2
RC or RCc	RC or RCc	3

The extraction mode of the bulk node is filtered in addLpe function.

Mixed mode : LPE choice methodology(3/4)



🟩 **extracted parasitics**

🟦 **extra parasitics**

🟥 **model**

RC extraction is performed on net A.

R extraction is performed on net B.

So, the LPE flag value for the resistor is set at 2.

As the LPE flag has been set at 2, no access resistor is taken account in the model, but capacitors remain in the equation.

We thus realize a double counting on Chead on the resistor side connected to the net A.

We simulate :

Model = [Rbody + Cbody + 2xRhi + Chead + Chead] + 2 x [Rsc + Rhs] + Chead

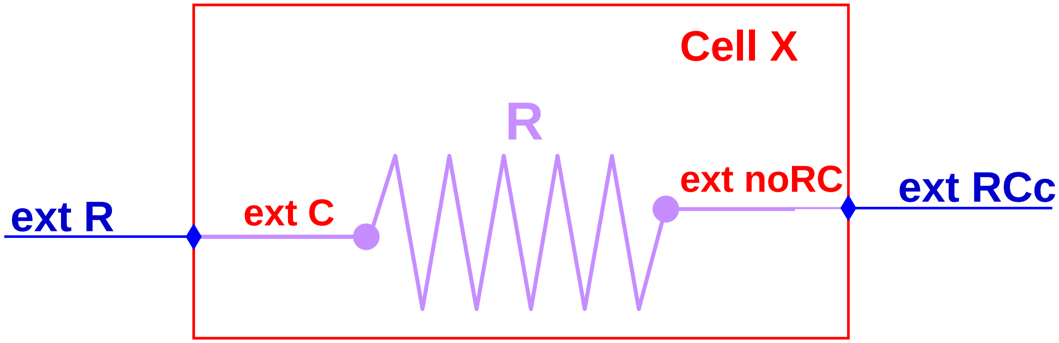
instead of :

Model = [Rbody + Cbody + 2xRhi + Chead] + 2 x [Rsc + Rhs] + Chead

Thus, we are much pessimistic than reality ➔ worst case.

Mixed mode : LPE choice methodology(4/4)

In the case of a devices in a hierarchy, the LPE flag value is set according the extraction mode of nets located at the top level of the design :



R extraction is performed to device pins and resistor LPE value is set at 2 (case R-RC).

Advanced CAD features

- Layout Parasitic Extraction Flag (LPE)
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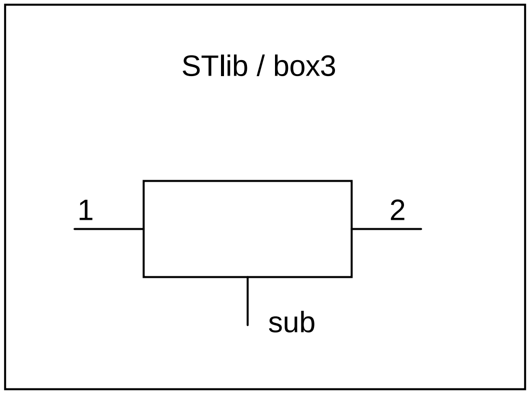
User Defined Devices : Blackbox at device level

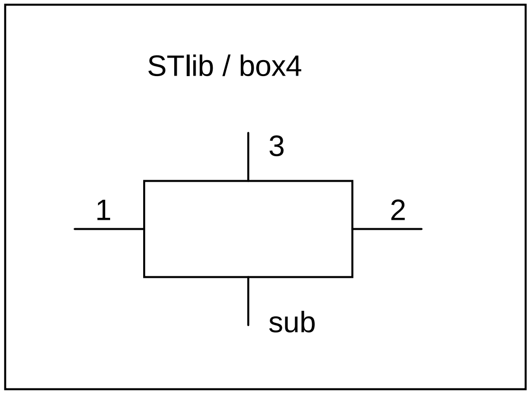
Design Kit main features

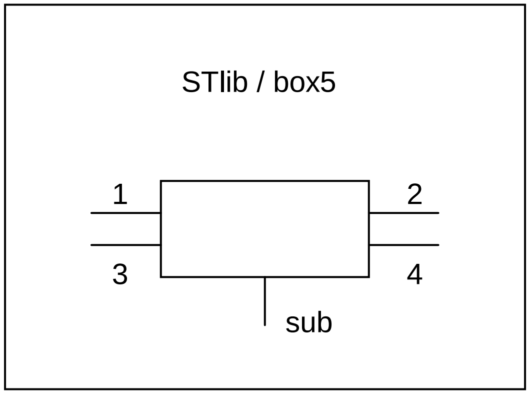
- box3 ; box4 ; box5; box6; box7 (1 pin for substrate) proposed in STLib
- CAD layers :
  - b7rf case :_mkr blackbox; mlabel drawing ;mkr userp1 -> mkr userp4
  - cmos065RF case : MKR blackbox; MKR label; MKR block;
    MKR drawing1 -> MKR drawing7
- layers ignored during LVS/PLS: all metal levels inside blackbox [+ active/poly grounshield inside ‘’MKR block’’]
- metalX connections ignored in blackbox
- DRC still applied
- LVS device type X: no auCdl; 1 schematic view; X device netlisting
- LVS code techno-independent ; metal level dependant.
- Warning: metal short or open are no more detected inside blackbox
- Warning: active layers are still taken into account during LVS step (mos; resistors; bipolar transistors still extracted without metal1)

Main Features (1/3)

- Symbols:
- Proposed in STLib
- Inputs/outputs pins of blackbox symbols correspond to the markers chosen in layout.
- Example: pin1 of a symbol must be associated to ‘mkr userp1 | MKR drawing1’ in layout

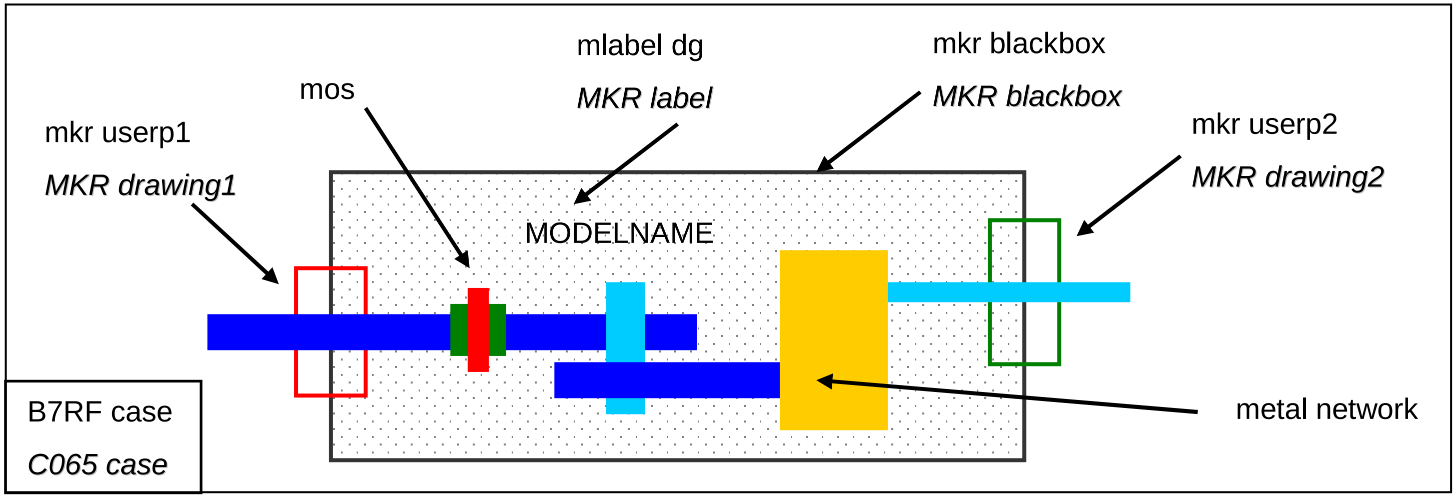






Main Features (2/3)

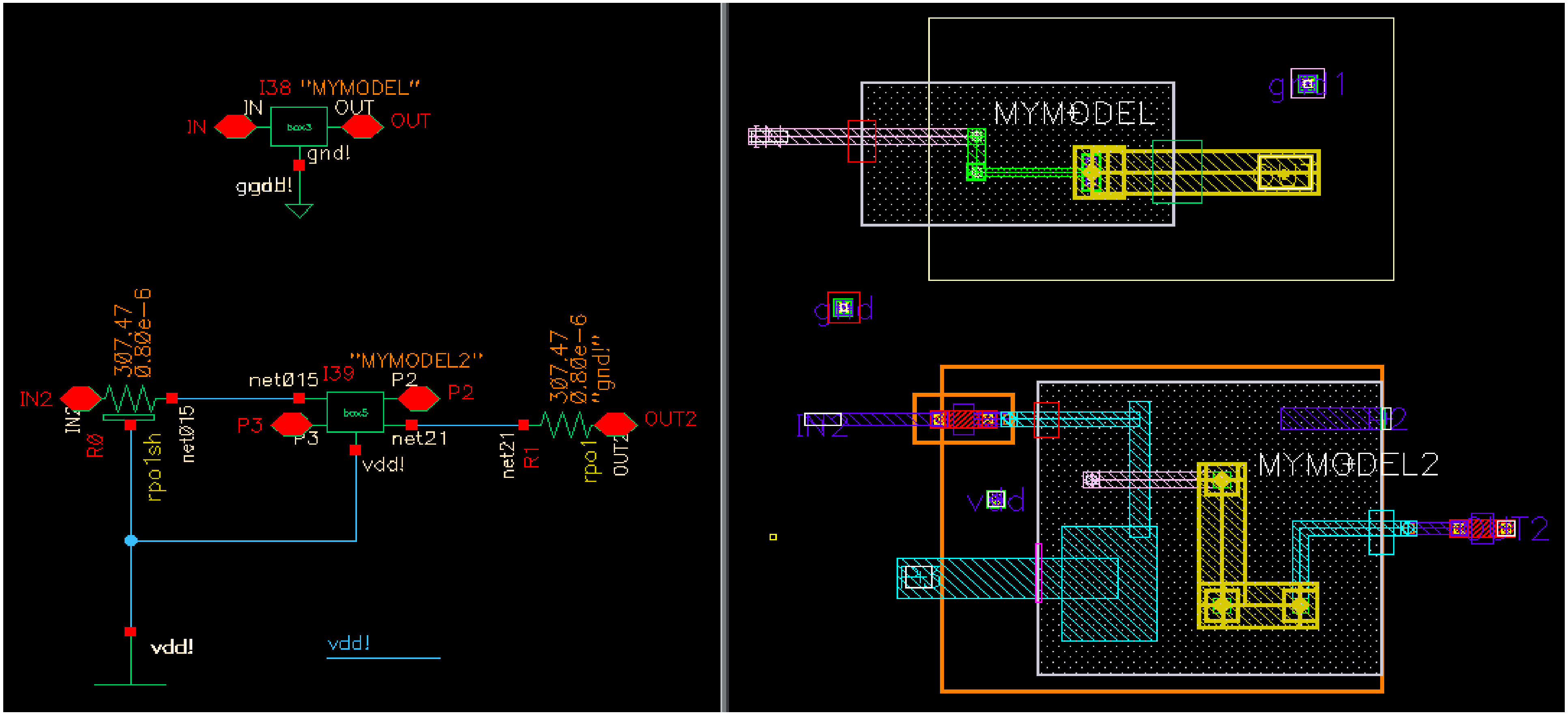
- Layout : methodology / markers placement
  - The blackbox area is delimited with marker {mkr blackbox | MKR blackbox}
  - Input/output pins are identified with {mkr userp1-5 | MKR drawing1-7}
  - Model name is labelled inside blackbox with marker {mlabel dg | MKR label}



PLS netlist will contain 1 floating mos + 1 device box3 with model “MODELNAME”

Main Features (3/3)

- Schematic versus Layout Views



Applications

- The aim of blackbox layer is to ignore metal parasitics in a limited area, it can be also used to extract user device with an associated user model (modified Pcell or 3D extracted model)

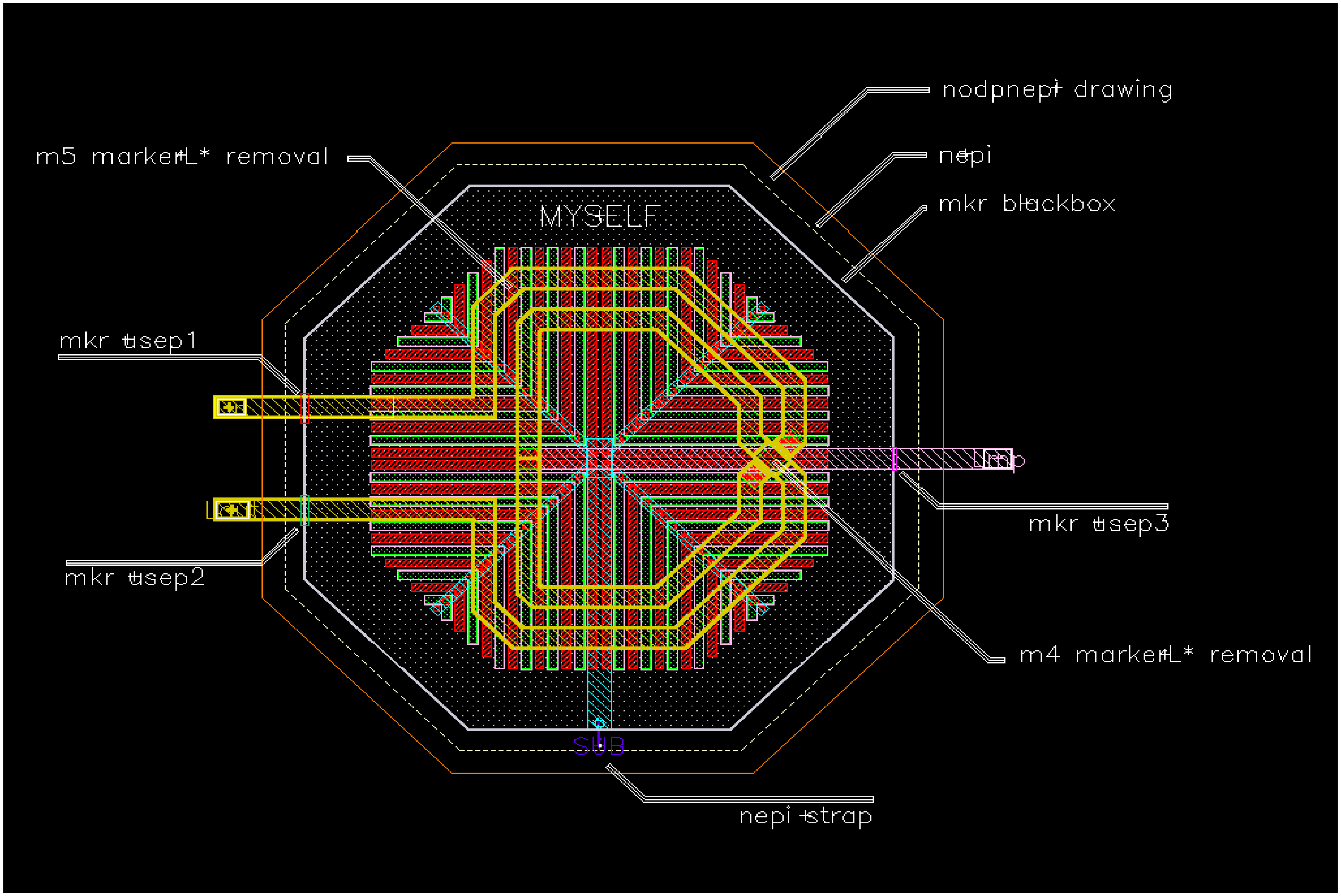
- A passive user device using metal layers can be extracted as a user device.

- This is not applicable for transistor devices; poly resistors devices; capacitor devices or substrate straps (only metalisation are ignored inside mkr blackbox).

- Some microstrip shapes can be handled by this CAD solution

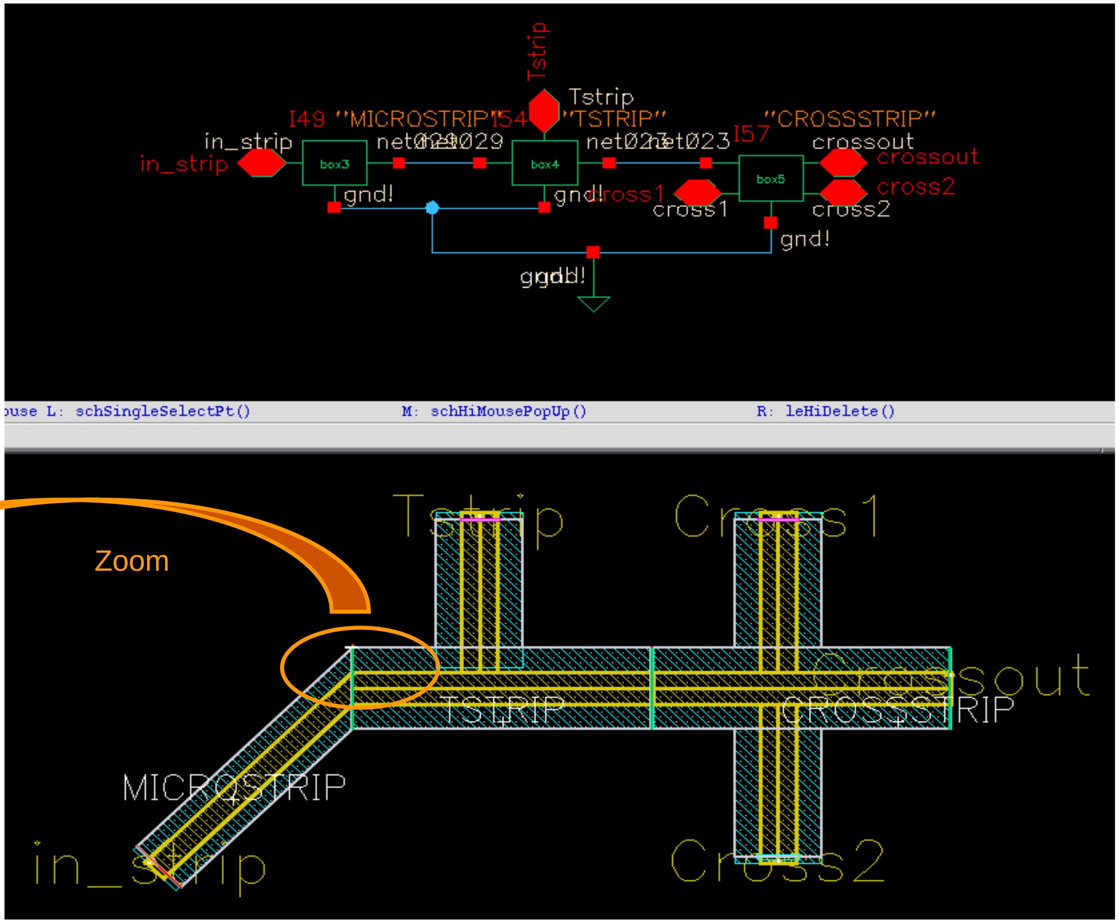
- Some user inductors can be extracted as user devices in a blackbox, if the classical recognition layers are removed : metalX markerL; metalX markerLS; metalX markerLA, metalX markerLC. To ignore pattern groundshield diodes inside N-epi, the marker “mkr nodpnepi’ must be used ; or “MKR block” for c065rf case.

Blackbox application example : user inductor device

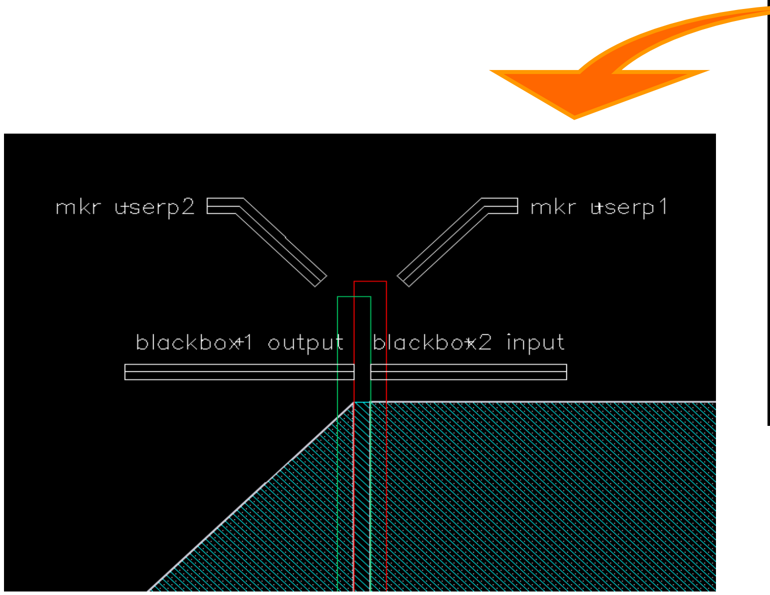


Blackbox application example : microstrip devices

- This example shows usage of different microstrip shapes between metal2 and metal5
- The limits between two blackboxes can be limited to one step of grid



```
ouse L: schSingleSelectPt()          M: schHiMousePopUp()          R: leHiDelete()
```



BlackBoxes and user models backannotation (1/2)

To perform backannotation step; the tool creates a symbol based on device name found in netlist

Therefore, any device included in the extracted netlist should have an associated symbol.

To complete a custom mapping for blackbox, the user have to declare the symbols to use with its own “user devices”

The backannotation will complain if this step is not done, with following message (plsintegrate_phase2.log):
“*Error model name has not been found for XRR0*”

The solution depends on the foreground/background choice from backannotation Tab

(see p.48, button “Generate extracted views”)

- BackAnnotation foreground mode :

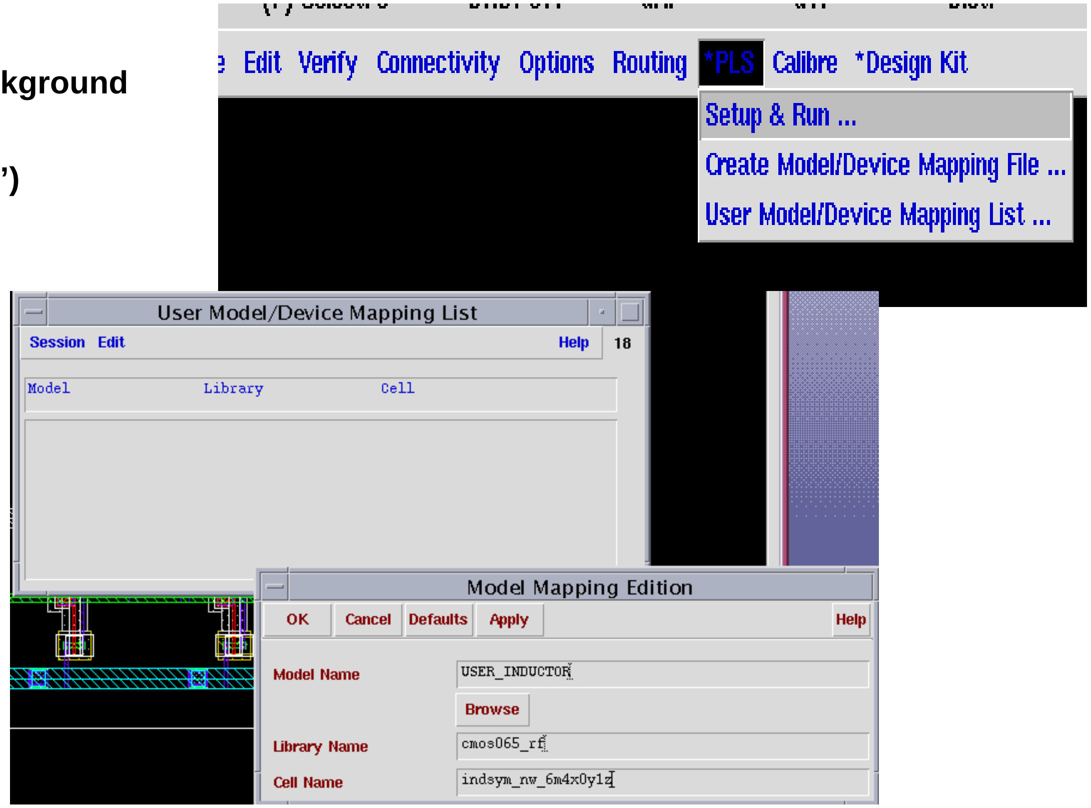
From PLS menu in layout window:

PLS->User Model/Device Mapping List

Edit the new model / Device mapping

Model Name is the text label used in layout

You can choose any existing/new cell having the same number of pins



Model Name USER_INDUCTOR

Library Name cmos065_rf

Cell Name indsym_nw_6m4x0y1z

BlackBoxes and user models backannotation (2/2)

- BackAnnotation background mode : An other Opus session is launched

In the case of a foreground run ("*Generate Extracted View in Background*" button of the Simulation menu is ticked), specific skill lines must be loaded through .cdsinit file for example.
Those lines can be retrieved by saving Mapping list from Model mapping editor described on previous slide

Example :

```
(let (local)
(setq local '(
("MYMODELNAME"
   libName "STlib"
   cellName "box5"
   termOrder ("box5p1" "box5p2" "box5p3" "box5p4" "box5sub")
   modelParameter ("macro" "MYMODELNAME")
   instParameters (("a") ("np"))
)
)
)
(if (boundp 'UARTPlsSpfModel2DeviceUserList)
    (setq UARTPlsSpfModel2DeviceUserList `(,@UARTPlsSpfModel2DeviceUserList ,@local))
   (setq UARTPlsSpfModel2DeviceUserList local)
)
)
```

In this example, we have a box5 from STLib and the model name chosen is "MYMODELNAME".
Be carefull to chose Model namse in upper case.

Advanced CAD features

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LVS for StarRCXt :

- The main differences between standard LVS and LVS for PLS are :
  - No ERC checks
  - Diode extraction
  - Stress effect calculation : po2act parameter
  - as, ad; ps; pd parameters calculation for mos devices
  - Segmentation of interconnect layers

- Calibre starrcxt lvs cgi file (1/2)

For **STANDARD** LVS calibre customized file, the MOS gate is defined with POLY of interconnection:
DEVICE MN(N) NGATE_FINAL IPOLY_FINAL(G) NDIFSI_FINAL(S) NDIFSI_FINAL(D) SUBS_FINAL(B)

Parasitics linked to POLY gate are already included in the Model or controlled via LPE flag.

To avoid double-counting in PLS, MOS gate is defined as a new layer which is extracted from the IPOLY :

```
NGATE_TERM_FINAL = IPOLY:i AND NGATE_FINAL

IPOLY:I+1  = IPOLY:I NOT NGATE_FINAL
```

Reconnection of the gate layer to the IPOLY in the “Connectivity Section” to avoid open circuit:

```
CONNECT IPOLY_FINAL NGATE_TERM_FINAL

ATTACH [L poly calnum pintext] NGATE_TERM_FINAL
```

In **STARRCXT** file, the gate is defined with this layer instead of IPOLY in the recognition section:
DEVICE MN(N) NGATE_FINAL NGATE_TERM_FINAL (G) NDIFSI_FINAL(S) NDIFSI_FINAL(D) SUBS_FINAL(B)

LVS for StarRCXt :

- Calibre starrcxt lvs cgi file (2/2)

The same treatment is realized for the plate of poly / nwell capacitors:

Standard :

DEVICE C(CPNW) CP1NW_FINAL IPOLY_FINAL NWELLC_FINAL SUBS_FINAL

StarRCXT :

DEVICE C(CPNW) CP1NW_FINAL CP1NW_TERM_FINAL NWELLC_FINAL SUBS_FINAL

and for the plate of METAL capacitors:

Standard :

DEVICE C(CMET) CAPMETAL3_FINAL ME3_FINAL ME2_FINAL SUBS_FINAL

StarRCXT :

DEVICE C(CMET) CAPMETAL3_FINAL M3_PLATE M2_PLATE SUBS_FINAL

M3PLATE = (ME3:i AND CAPMETAL3_FINAL) OR (ME3:i AND CAPMETAL4_FINAL)

ME3:i+1 = (ME3:i NOT CAPMETAL3_FINAL) NOT CAPMETAL4_FINAL

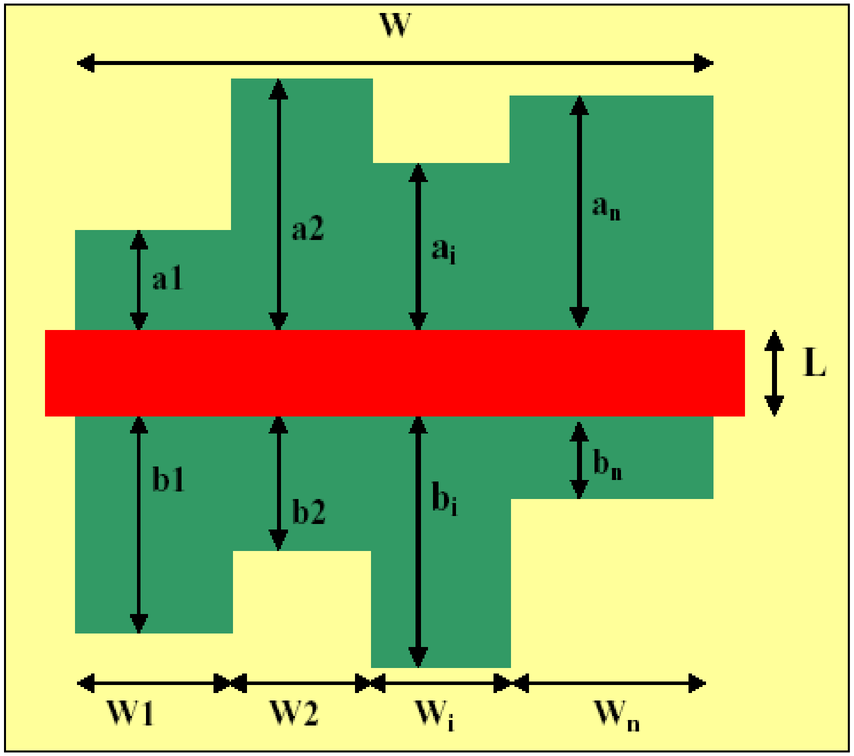
CONNECT ME3_FINAL M3PLATE

Stress effect handling (1/2)

Po2act parameter computation (single-finger)

- Example : XMP D G S B vdd epllgp_bs3ju w=2u l=0.13u ad=0.32p as=0.58p pd=0.33u ps=2.53u **po2act=**5.07467e-07 lpe=-1
- Starting from 0.13um technologies

$$po2act = \frac{1}{\sum_{i=1}^{n} \frac{W_i}{W}\left(\frac{1}{2a_i} + \frac{1}{2b_i}\right)}$$

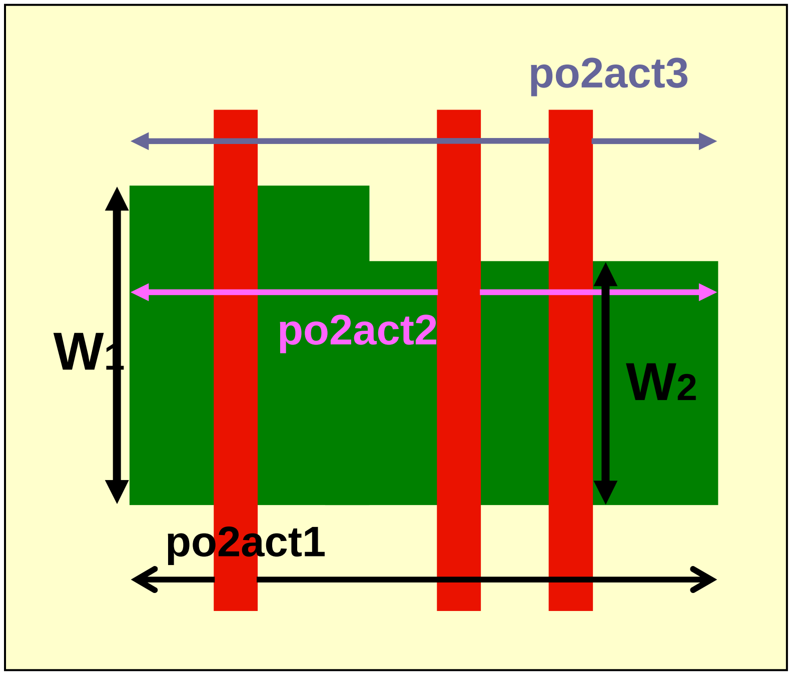


Approximations:

- a_i, b_i are limited values

Stress effect handling (2/2)

- Po2act parameter computation (multi-finger)



$$po2act_{eq} = \frac{\sum_{j=1}^{m} W_j}{\sum_{i=1}^{n} \frac{W_j}{po2act_j}}$$

Approximations:

- exact for a rectangular active area, and

fingers reguraly spaced.

StarRCXT main command files :

- starrcxt.map
  - ➢ mapping file between calibre and process tables for conductors and via layers

  example : NGATE_TERM_FINAL IPOLY_FINAL RPSQ=0.00001
  M3PLATE ME3_FINAL RPSQ=0.00001

  - ➢ To ignore capacitors between terminal layers

  example : ignore_cap_layers
  SALI_FINAL NGATE_TERM_FINAL
  M2PLATE M3PLATE

- starrcxt.cmd
  - ➢ setup of and options and files paths as specified in PLSinit
  - ➢ list of devices which need X prefix in Spice netlist.

- techno.cfg
  - ➢ PostProcessing of SPICE netlist
    - ✓ To add lpe flag
    - ✓ To cut too long .SUBCKT header before netlist awk conversion
    - ✓ To remove SHORT model name

Advanced CAD features

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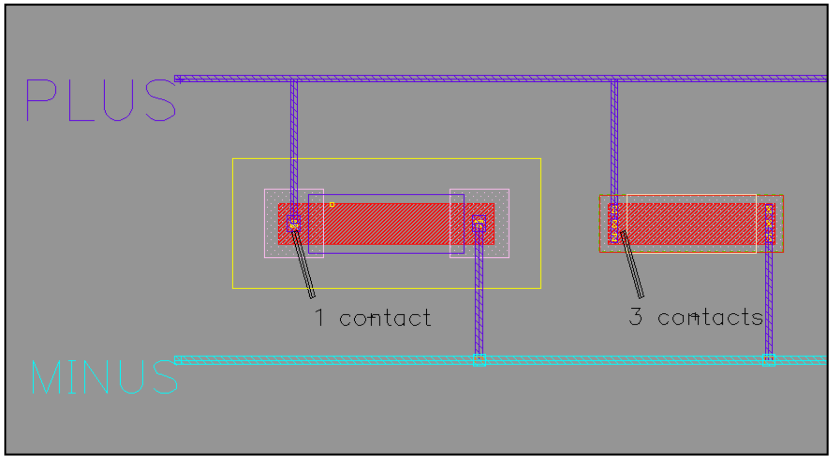
Resistor network

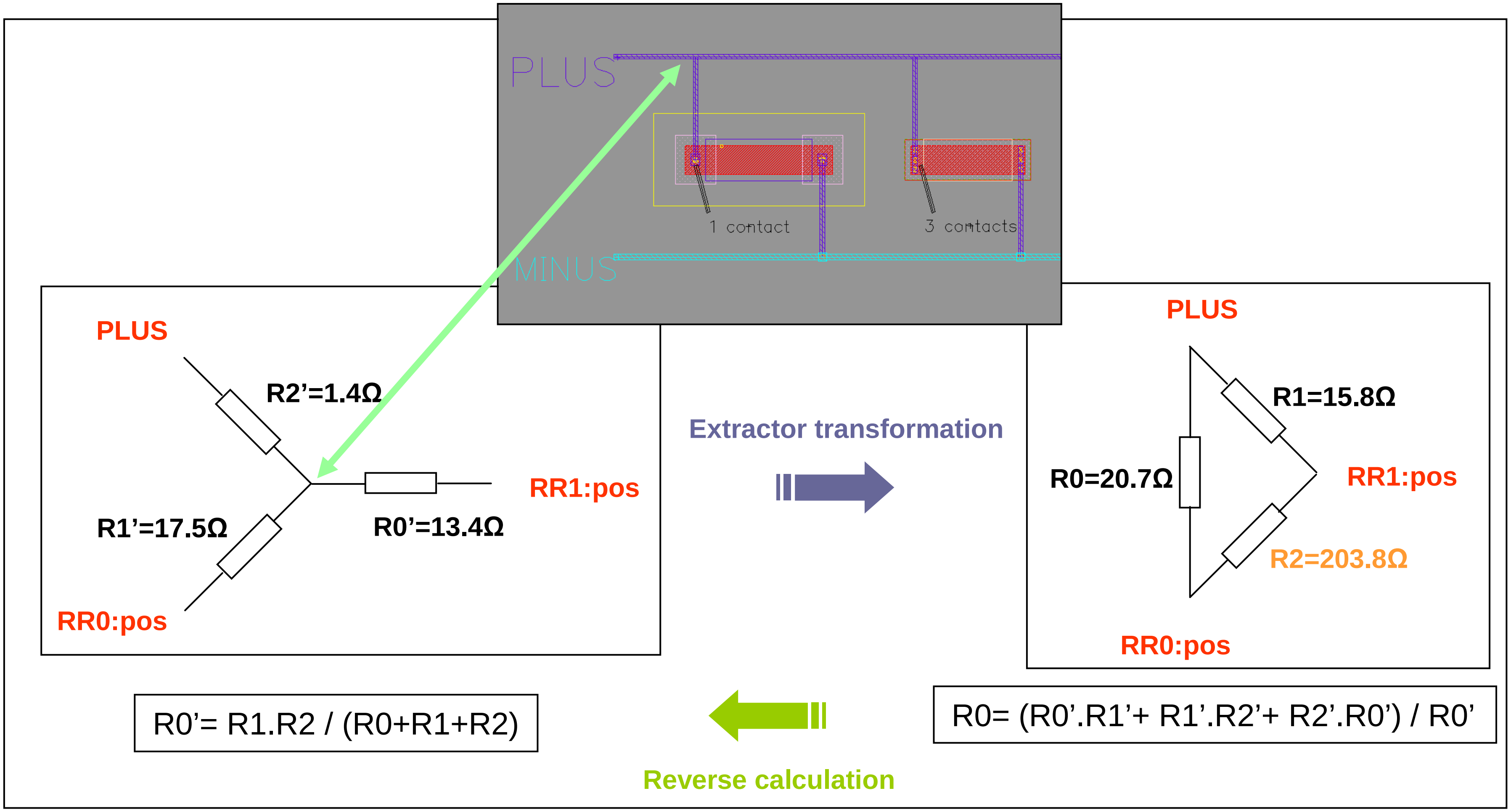
- triangle network in netlists for reduction purpose
- fully equivalent network with conversion Y to Δ (Kennely)
- Netlist is not direct image of interconnects
- High resistor values due to transformation
- To find out resistor localisation, Δ to Y must be applied
- Example :



```
.SUBCKT testr MINUS PLUS bulk
...
*|NET PLUS 0
R0 PLUS RR0:pos 20.751
R1 PLUS RR1:pos 15.7895
R2 RR1:pos RR0:pos 203.78
...
...
* Instance Section
XRR0 RR0:pos RR0:neg RR0:SUB rpo1hm1 W=1e-06 nc=1 r=3488.06
lpe=2
XRR1 RR1:pos RR1:neg RR1:SUB rpo1pm1 W=1e-06 nc=3 r=1200.01
lpe=2
```

Resistor network

- Y to Δ transformation example



$$R0' = R1.R2 / (R0+R1+R2)$$

$$R0 = (R0'.R1' + R1'.R2' + R2'.R0') / R0'$$

Advanced CAD features

- Layout Parasitic Extraction Flag (LPE)
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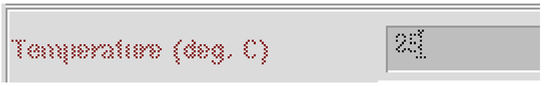
Temperature management

- Dedicated to parasitic resistances only
- Default temperature is set for each Process Corner
- Available within the interface
- For old design Kits temperature fixed @ 25 °C (All empirical tables compatible to fixed value)
- Editable with last DK releases (New empirical table format)
- T1 is the recommended operating temperature for a given corner
- CRT is temperature derating coefficient

$$R' = R_{25C} (1 + (T_1 - 25) . CRT_\alpha)$$

Where "CRT_α" is a first polynomial order given in ITF.



Temperature (deg. C) 25

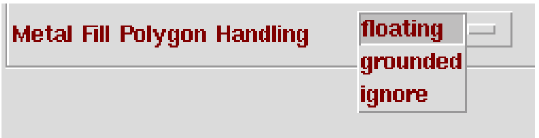
TECHNO	CORNER	TEMP.	T_1
All	RCTYP	TYP	25 °C
	RCMIN	TYP	25 °C
	RCMAX	TYP	25 °C
<= 90 nm	CMIN	MIN	-40 °C
	CMAX	MAX	105 °C
	XTLK	MIN	-40 °C
	DLY	MAX	105 °C

Advanced CAD features

- Layout Parasitic Extraction Flag (LPE)
- User Defined Devices
- Details on extraction
- Resistors network
- Temperature Management
- Tiling management

Tiling management (1/2)

- Based on dummy purpose recognition : “dummy” or “tile”
- 3 different options within the interface : floating/grounded/ignore
- Ignore :
  - ✓ dummies are not seen by the extractor engine; no impact in netlists
  - ✓ Equivalent to “no dummies drawn”
- Grounded :
  - ✓ Capacitor between dummies and active lines are lumped.
  - ✓ Equivalent to connect dummy @ reference node 0
- Floating :
  - ✓ Clear netlist / faster simulation; coupling calculation between net
  - ✓ The most accurate and recommended option
  - ✓ Physically equivalent to increase coupling between lines



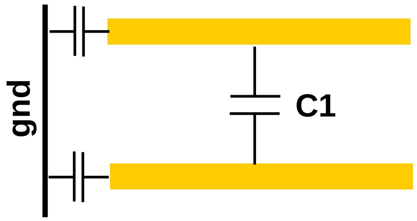
Metal Fill Polygon Handling

floating

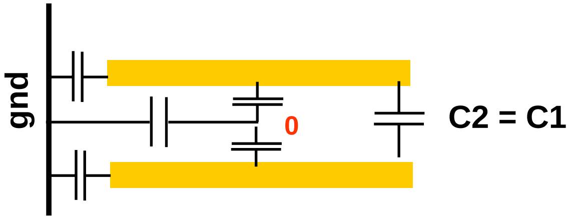
grounded

ignore

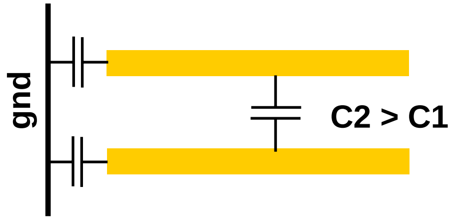
- Floating Net “*A*” drawn with purpose drawing is always seen as “grounded *In_A*”, unless pin A is present in schematic.



Ignore



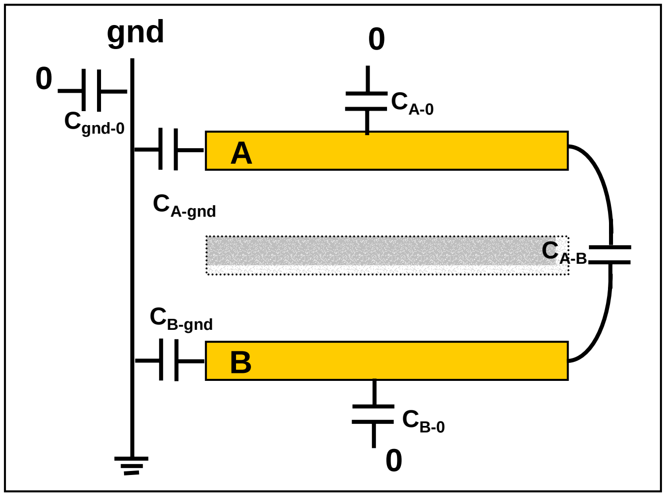
Grounded



Floating

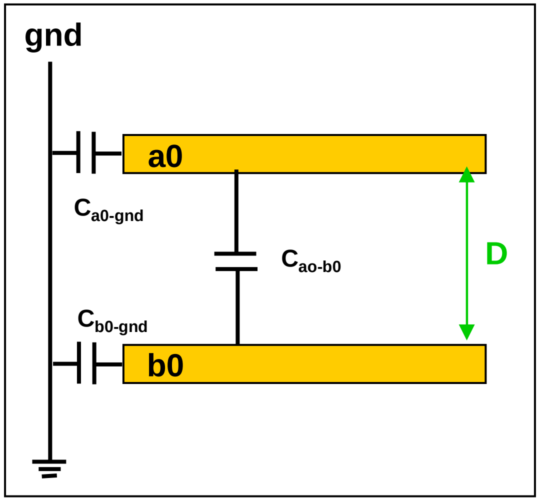
Tiling management (2/2)

Purpose dummy / tile

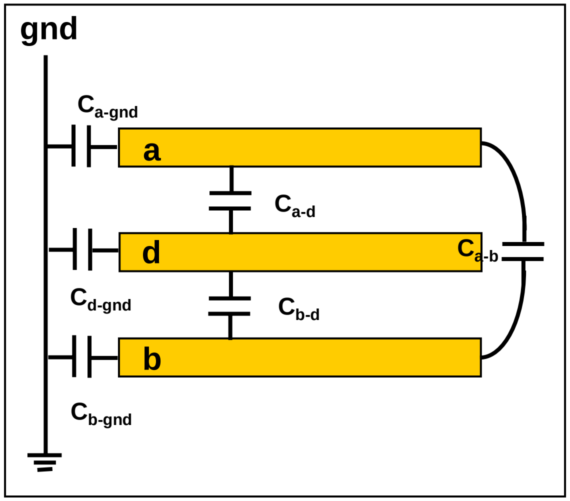


Drawn layout

Reference equivalent layouts



no dummy



dummy drawing

	C_{A-B}	C_{A-gnd}	C_{B-gnd}	C_{A-0}	C_{B-0}	C_{gnd-0}
IGNORE	$= C_{a0-b0}$	$= C_{a0-gnd}$	$= C_{b0-gnd}$	-	-	-
GROUNDED	$= C_{a-b}$	$= C_{a-gnd}$	$= C_{b-gnd}$	$= C_{a-d}$	$= C_{b-d}$	$= C_{d-gnd}$
FLOATING	$\approx C_{a-b} +$ $1/(1/C_{a-d}+1/C_{b-d})$	$\approx C_{a-gnd}$	$\approx C_{b-gnd}$	-	-	-

🟨	**metalX drawing**
▨	**metalX dummy**

Same distance D for all cases

0 is lumped reference

Personal Notes