HVT_LP MODELS (NHVTLP, PHVTLP)

1. CONDITIONS OF EXTRACTION

- Maturity: Pre-Production
- Model parameters extraction based on lot : Q539TVB
- Geometrical extraction domain:
  - Drawn gate length : 10.0 ≥ L ≥ 0.06 µm
  - Drawn transistor width : 10 ≥ W ≥ 0.12 µm
- Temperature extraction domain: -40 ˚C to 150 ˚C
- Bias extraction domain:
  - Gate bias: 0 ≤ |VGS| ≤ 1.32 V (VDD + 10%)
  - Drain bias: 0 ≤ |VDS| ≤ 1.32 V (VDD + 10%)
  - Bulk bias: 0 ≤ |VBS| ≤ 1.32 V (VDD + 10%)

2. CONDITIONS OF SIMULATION

- Temperature: 25 ˚C
- Currents:

  IDLIN = Ids at Vgs = 1.2 V, Vds = 50 mV and Vbs = 0 V

  ION = Ids at Vgs = 1.2 V, Vds = 1.2 V and Vbs = 0 V

  IOFF = Ids at Vgs = 0 V, Vds = 1.2 V and Vbs = 0 V

  IG_ON = Igs at Vgs = 1.2 V and Vd= Vs = Vb = 0 V

  IG_OFF = Igs at Vgs =Vbs = 0 V and Vds = 1.2 V
- Threshold voltage in linear and saturation regime

  VTLIN is Vgs value at Vds = 50 mV, Vbs = 0 V and Ids= 40*W/L nA.

  VTSAT is Vgs value at Vds = 1.2 V, Vbs = 0 V and Ids= 40*W/L nA.
- Current derivatives:

$$Gm = \frac{\partial}{\partial V_{gs}} Ids$$ at Vgs = VTLIN + 0.2 V, Vds = 0.6 V and Vbs = 0 V

$$Gd = \frac{\partial}{\partial V_{ds}} Ids$$ at Vgs = VTLIN + 0.2 V, Vds = 0.6 V and Vbs = 0 V

Analog gain = Gm/Gd

- Gate Capacitances:

  CGGINV = CGG at Vgs = 1.2 V, Vds = 0 V and Vbs = 0 V

  CGD_0V = CGD at Vgs = 0 V, Vds = 0 V and Vbs = 0 V

  $$CGGMEAN = \frac{1}{VDD} \cdot \int_{0}^{VDD} CGG \times dVgs$$ with VDD = 1.2 V and Vbs = 0 V

  TAU = CGGMEAN*VDD/ION

- Diode Capacitances:

  CBD OFF = CBD at Vgs = 0 V, Vds = 1.2 V and Vbs = 0 V

  Note: the area and perimiters of source/drain junction diodes used for simulation are defined with the the minimum poly-to-active distance specified in the DRM.

- Transition frequency:

  FT = frequency for which the small signal current gain H_{21} is 0 dB (i.e. $\left|\frac{I_d}{I_g}\right|$ = 0 dB).

3. MAIN ELECTRICAL CHARACTERISTICS OF NMOS HVT_LP TRANSISTORS

PARAMETERS	HVTLP_TT	HVTLP_SS	HVTLP_FF	units
N-channel transistors (nhvtlp)				
VTLIN W=1/L=10.0	438	459	417	mV
IDLIN W=1/L=10.0	8.26e-07	7.63e-07	8.93e-07	A
VTSAT W=1/L=10.0	429	450	407	mV
ION W=1/L=10.0	4.78e-06	4.26e-06	5.35e-06	A
VTLIN W=1/L=0.06	556	596	510	mV
IDLIN W=1/L=0.06	7.07e-05	5.93e-05	8.44e-05	A
VTSAT W=1/L=0.06	426	482	358	mV
ION W=1/L=0.06	4.22e-04	3.41e-04	5.24e-04	A
IOFF W=1/L=0.06	1.56e-11	4.20e-12	1.14e-10	A
IG_ON W=1/L=0.06	4.57e-12	2.36e-12	8.80e-12	A
IG_OFF W=1/L=0.06	9.30e-13	4.64e-13	1.87e-12	A
FT W=1/L=0.06	1.36e+11	1.19e+11	1.55e+11	Hz
CGGinv W=1/L=0.06	1.16e-15	1.22e-15	1.09e-15	F
CGGmean W=1/L=0.06	1.01e-15	1.04e-15	9.73e-16	F
CGD 0V W=1/L=0.06	3.80e-16	3.74e-16	3.87e-16	F
CBD OFF[a] W=1/L=0.06	4.87e-16	5.53e-16	4.19e-16	F
Tau W=1/L=0.06	2.9	3.6	2.2	ps
Gm W=1/L=0.06	3.63e-04	3.22e-04	4.14e-04	S
Gd W=1/L=0.06	4.51e-05	3.34e-05	6.35e-05	S
Gain W=1/L=0.06	8.06e+00	9.65e+00	6.52e+00	
VTLIN W=0.12/L=0.06	505	541	465	mV
IDLIN W=0.12/L=0.06	1.02e-05	8.46e-06	1.23e-05	A
VTSAT W=0.12/L=0.06	402	449	348	mV
ION W=0.12/L=0.06	6.02e-05	4.89e-05	7.42e-05	A
IOFF W=0.12/L=0.06	3.16e-12	8.44e-13	1.75e-11	A
FT W=0.12/L=0.06	1.10e+11	9.62e+10	1.25e+11	Hz

Table 1: Main electrical characteristics for NMOS

a. Value coresponding to the minimum poly-to-acvtive distance specified in the DRM

4. MAIN ELECTRICAL CHARACTERISTICS OF PMOS HVT_LP TRANSISTORS

PARAMETERS	HVTLP_TT	HVTLP_SS	HVTLP_FF	units
P-channel transistors (phvtlp)				
VTLIN W=1/L=10.0	528	550	506	mV
IDLIN W=1/L=10.0	2.48e-07	2.28e-07	2.68e-07	A
VTSAT W=1/L=10.0	521	543	499	mV
ION W=1/L=10.0	1.39e-06	1.23e-06	1.56e-06	A
VTLIN W=1/L=0.06	574	607	540	mV
IDLIN W=1/L=0.06	3.01e-05	2.56e-05	3.55e-05	A
VTSAT W=1/L=0.06	472	521	414	mV
ION W=1/L=0.06	2.10e-04	1.72e-04	2.57e-04	A
IOFF W=1/L=0.06	9.65e-12	2.98e-12	5.21e-11	A
IG_ON W=1/L=0.06	1.58e-12	7.90e-13	3.14e-12	A
IG_OFF W=1/L=0.06	4.36e-13	2.11e-13	9.08e-13	A
FT W=1/L=0.06	7.02e+10	6.08e+10	8.06e+10	Hz
CGGinv W=1/L=0.06	1.20e-15	1.26e-15	1.13e-15	F
CGGmean W=1/L=0.06	1.02e-15	1.05e-15	9.86e-16	F
CGD 0V W=1/L=0.06	3.60e-16	3.57e-16	3.65e-16	F
CBD OFF[a] W=1/L=0.06	4.77e-16	5.40e-16	4.12e-16	F
Tau W=1/L=0.06	5.8	7.3	4.6	ps
Gm W=1/L=0.06	2.15e-04	1.89e-04	2.47e-04	S
Gd W=1/L=0.06	2.02e-05	1.52e-05	2.82e-05	S
Gain W=1/L=0.06	1.07e+01	1.24e+01	8.75e+00	
VTLIN W=0.12/L=0.06	510	543	475	mV
IDLIN W=0.12/L=0.06	5.30e-06	4.46e-06	6.31e-06	A
VTSAT W=0.12/L=0.06	420	466	365	mV
ION W=0.12/L=0.06	3.53e-05	2.92e-05	4.26e-05	A
IOFF W=0.12/L=0.06	3.20e-12	8.57e-13	1.68e-11	A
FT W=0.12/L=0.06	6.09e+10	5.36e+10	6.87e+10	Hz

Table 2: Main electrical characteristics for PMOS

a. Value coresponding to the minimum poly-to-acvtive distance specified in the DRM

5. ELECTRICAL BEHAVIOR VERSUS GATE LENGTH AND CHANNEL WIDTH FOR NMOS HVT_LP TRANSISTORS

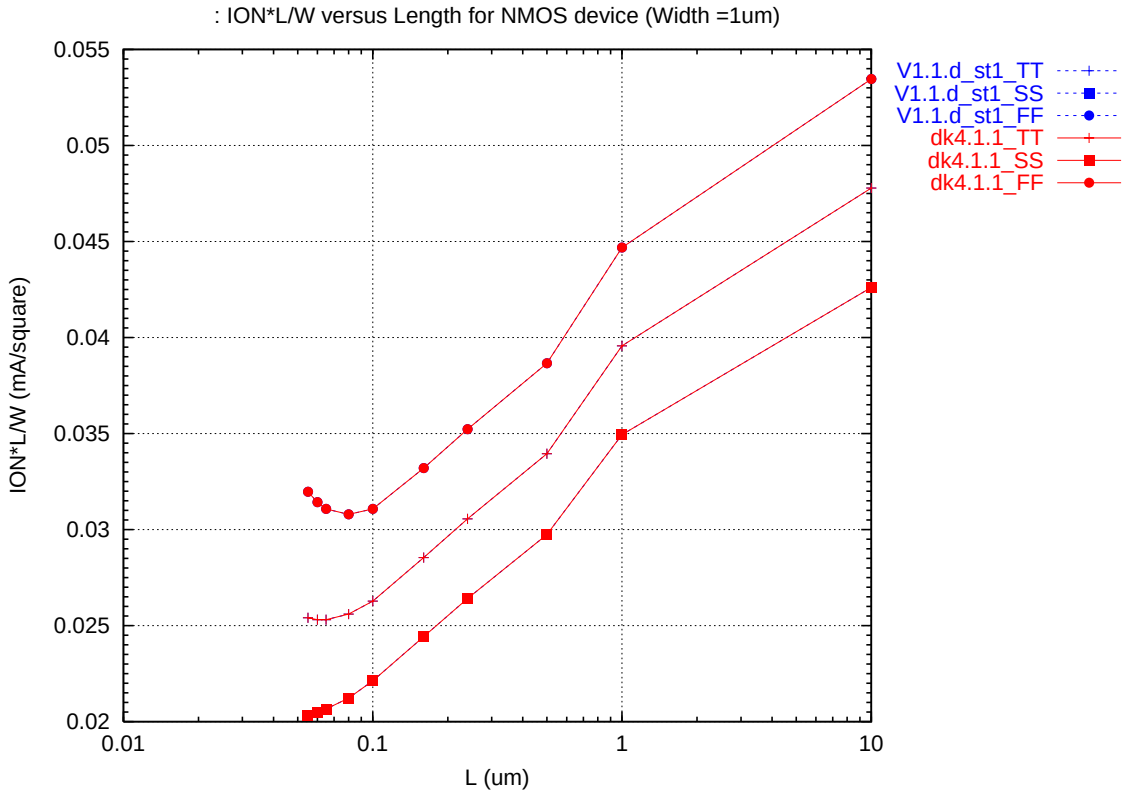

Figure 1 : ION/❑=ION*L/W versus drawn gate length for NMOS HVT_LP transistors (W = 1 µm)

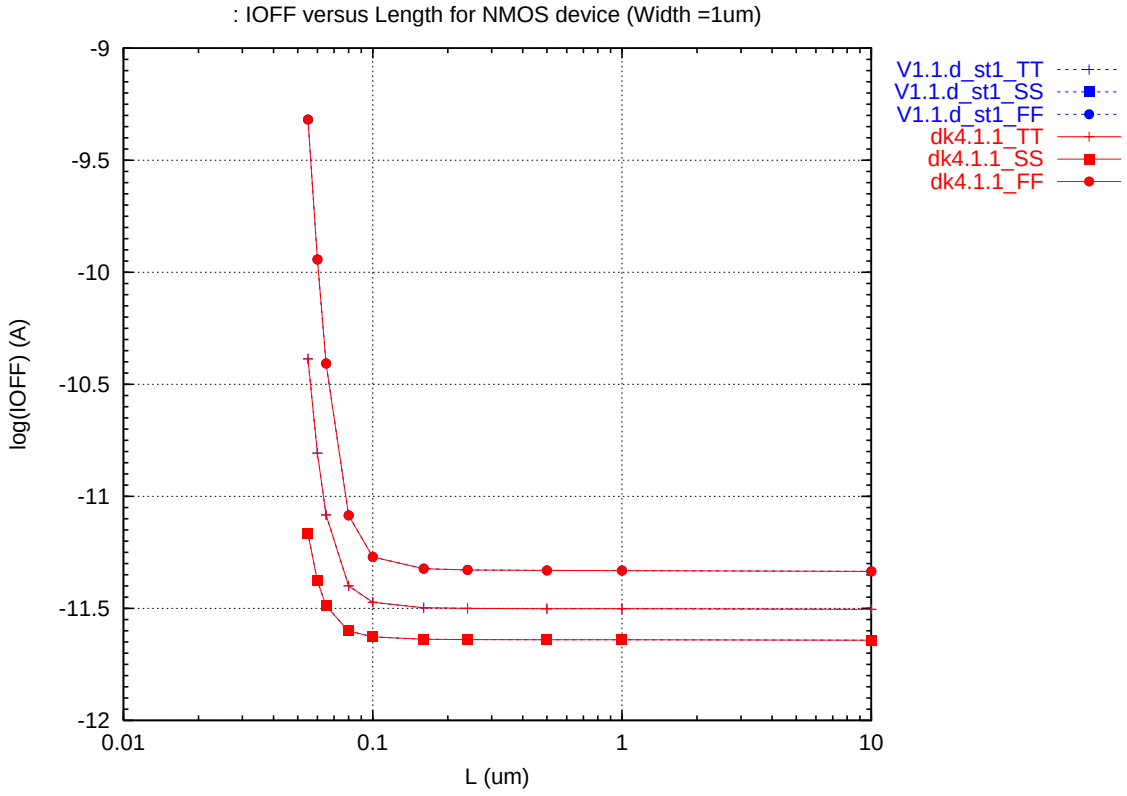

Figure 2 : IOFF versus drawn gate length for NMOS HVT_LP transistors (W = 1 µm)

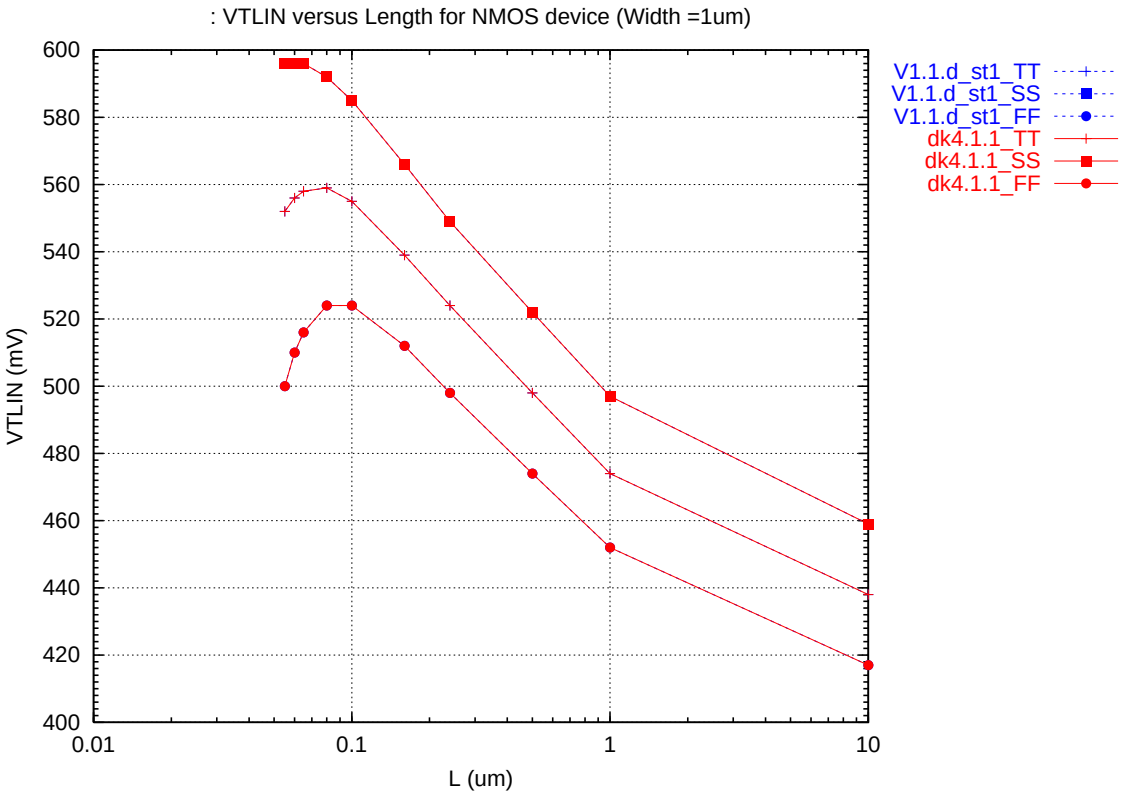

Figure 3 : Threshold voltage VTLIN versus drawn gate length for NMOS HVT_LP transistors (W = 1 µm)

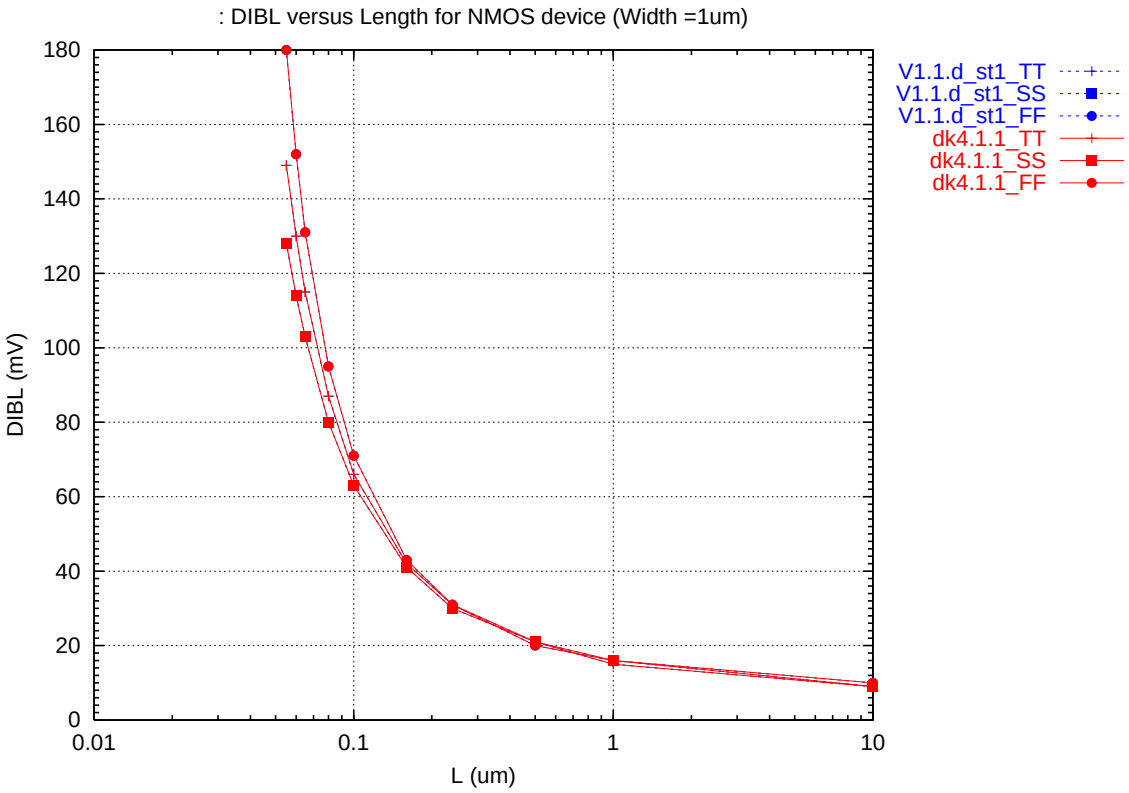

Figure 4 : DIBL= VTLIN-VTSAT versus drawn gate length for NMOS HVT_LP transistors (W = 1 µm)

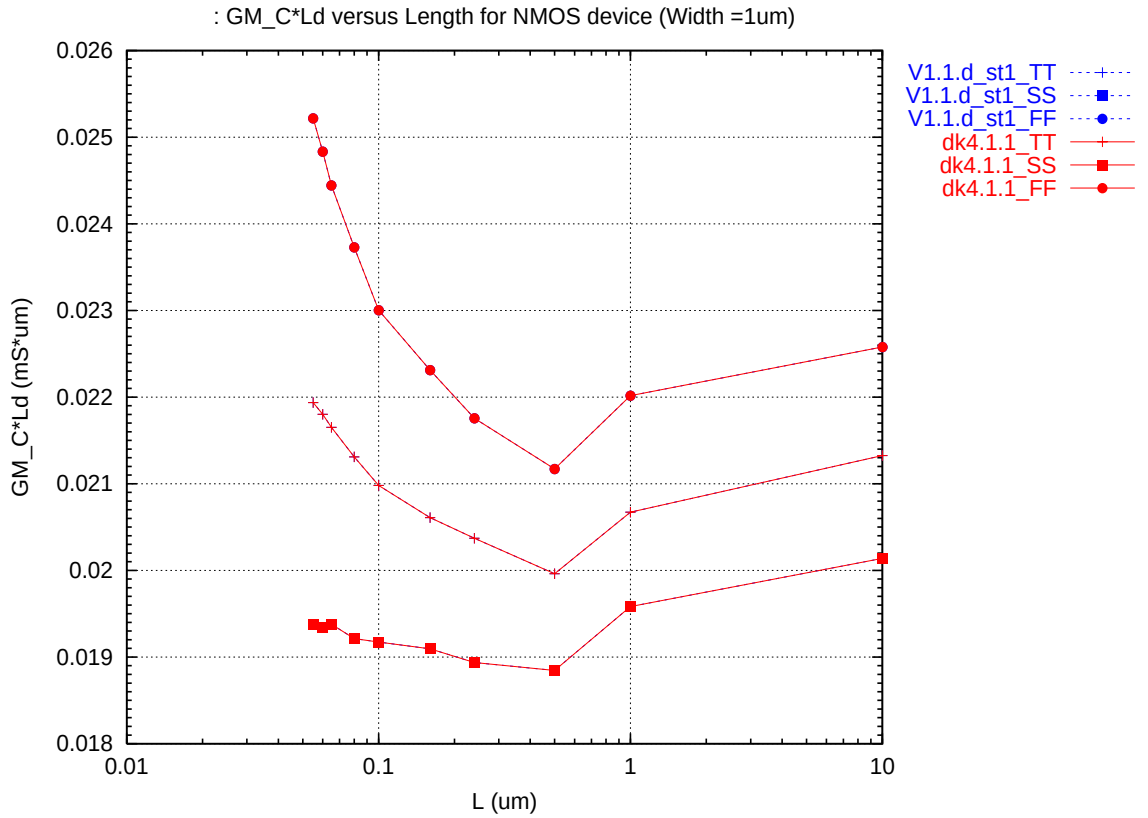

Figure 5 : GM*Ld versus drawn gate length for NMOS HVT_LP transistors (W = 1 µm)

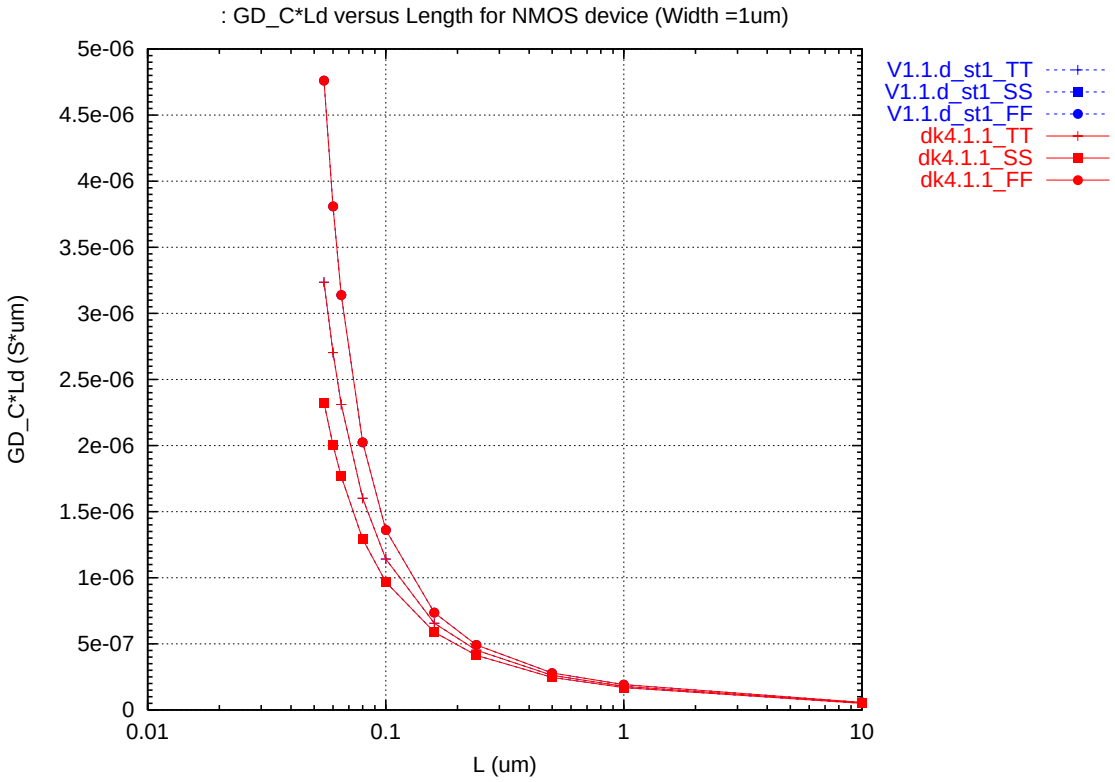

Figure 6 : GD*Ld versus drawn gate length for NMOS HVT_LP transistors (W = 1 µm)

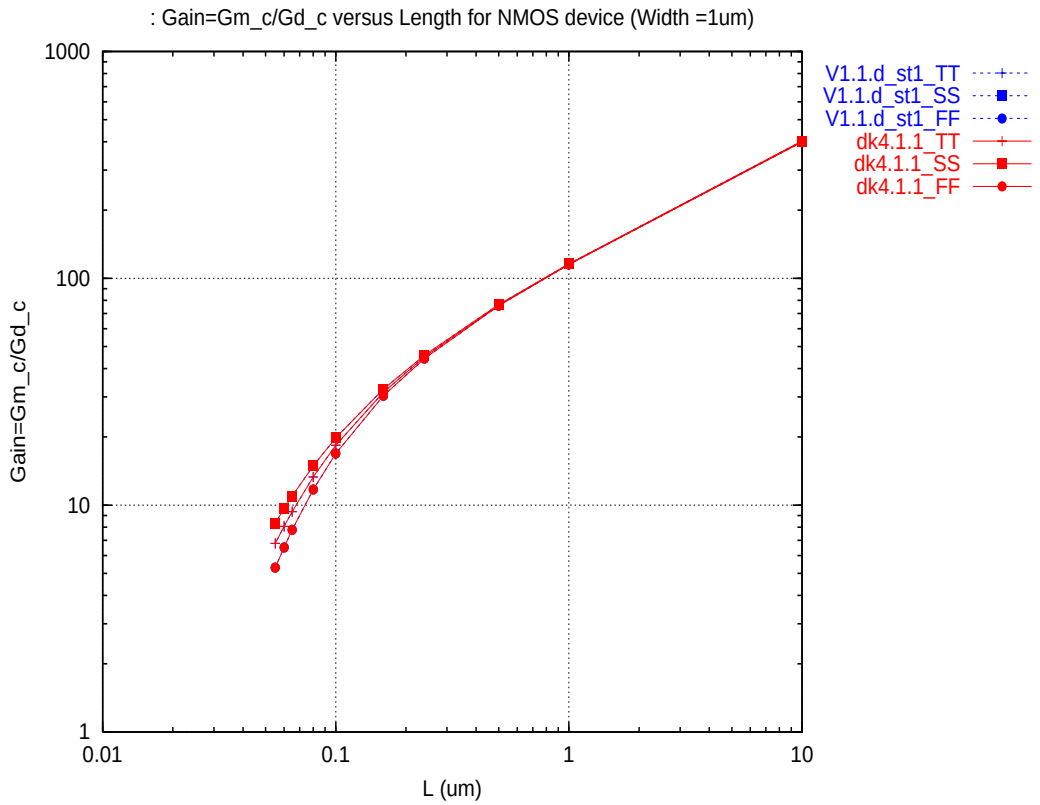

Figure 7 : GAIN versus drawn gate length for NMOS HVT_LP transistors (W = 1 µm)

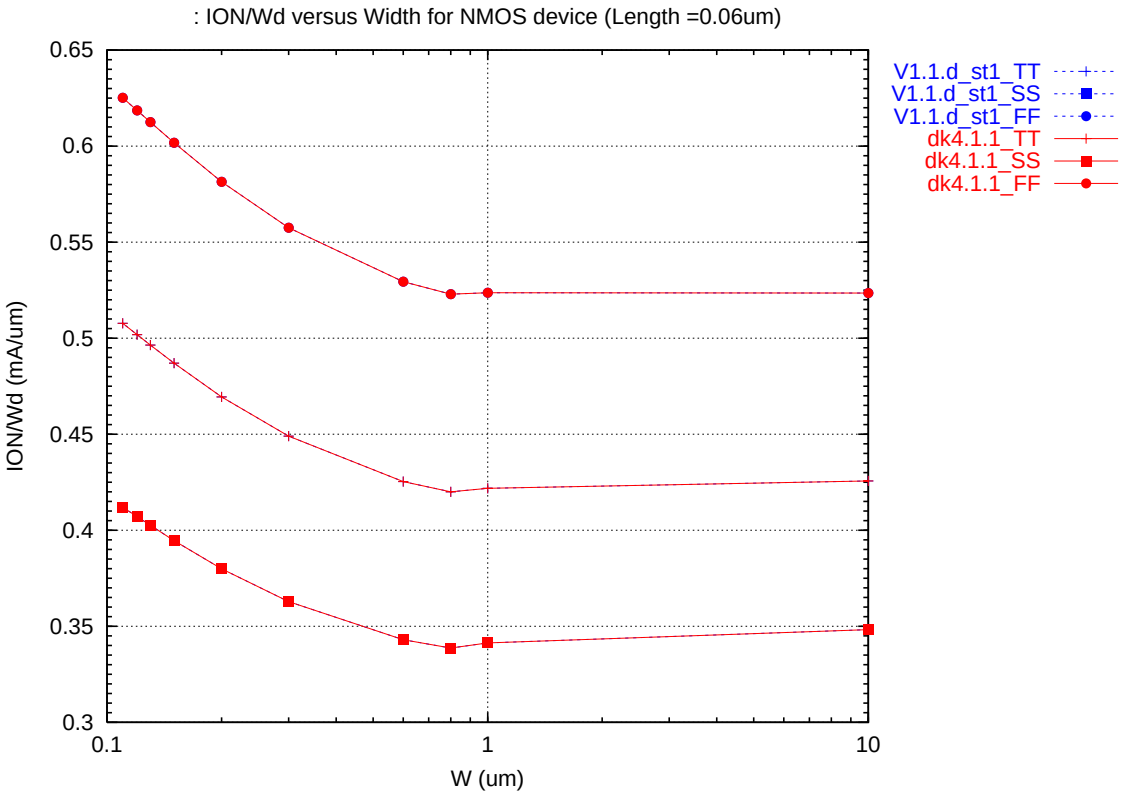

Figure 8 : ION versus drawn channel width for NMOS HVT_LP transistors (L = 0.06 µm)

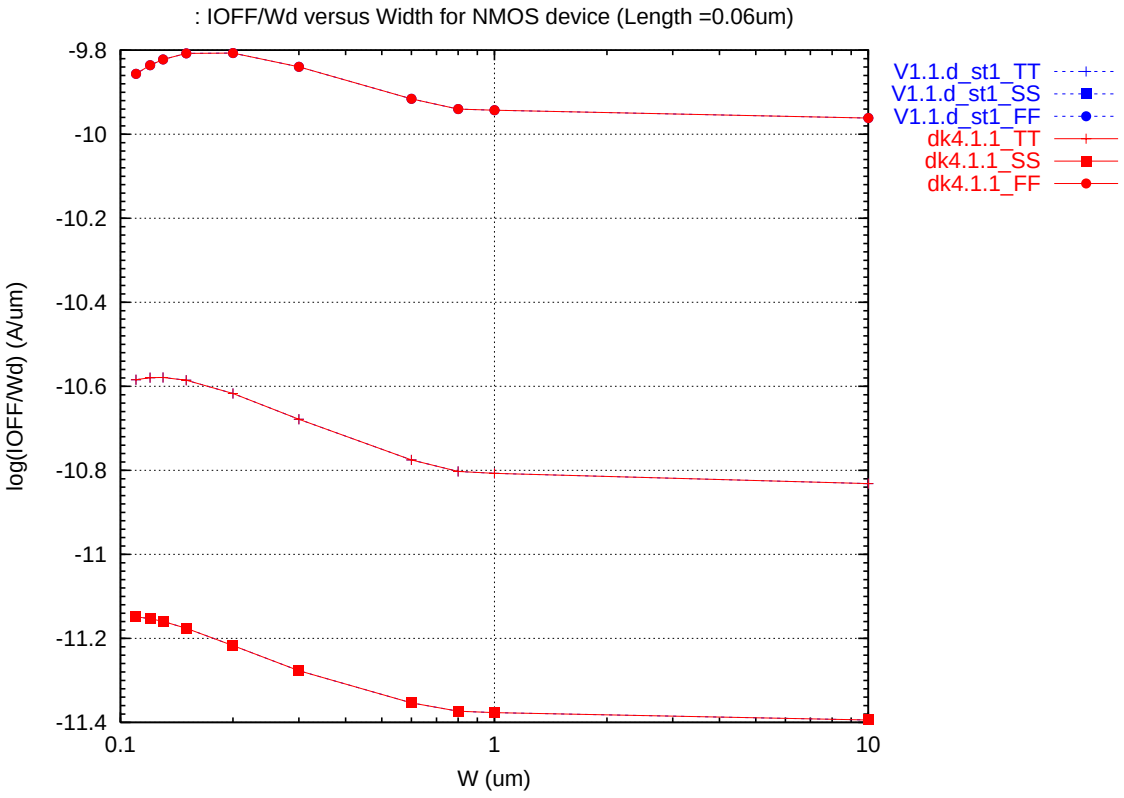

Figure 9 : IOFF versus drawn channel width for NMOS HVT_LP transistors (L = 0.06 µm)

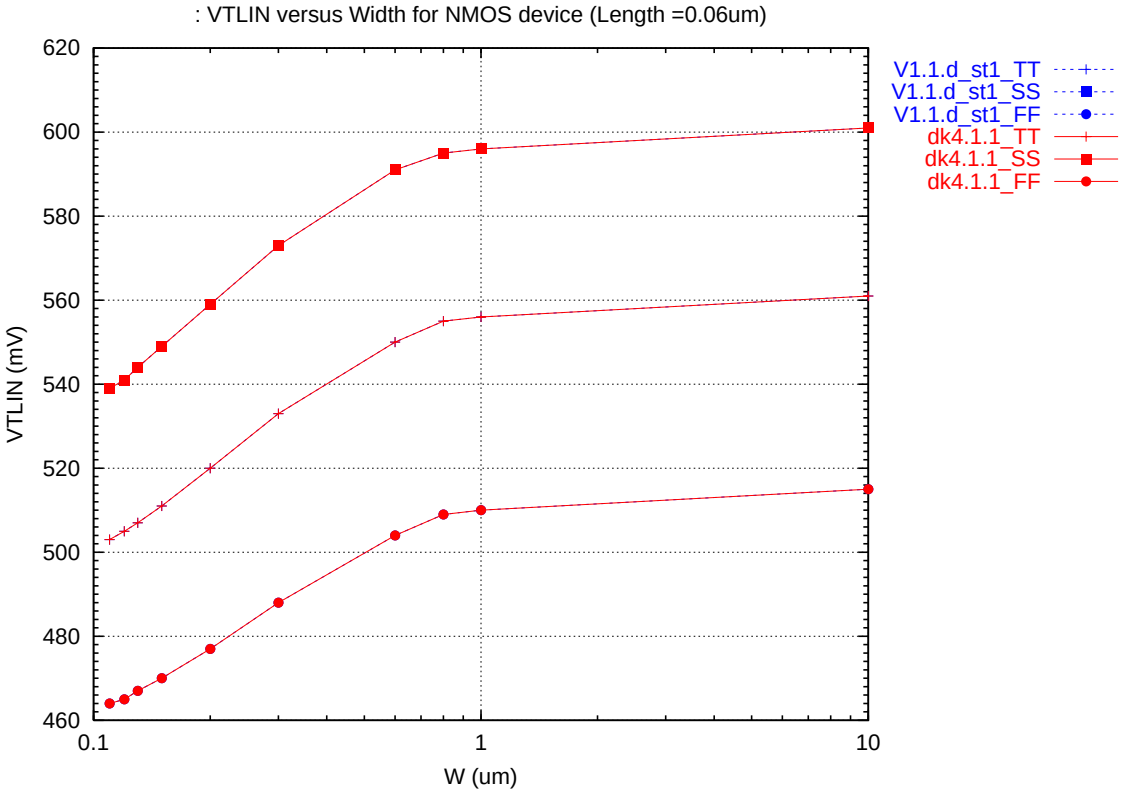

Figure 10 : Threshold voltage VTLIN versus drawn channel width for NMOS HVT_LP transistors (L = 0.06 µm)

6. ELECTRICAL BEHAVIOR VERSUS GATE LENGTH AND CHANNEL WIDTH FOR PMOS HVT_LP TRANSISTORS

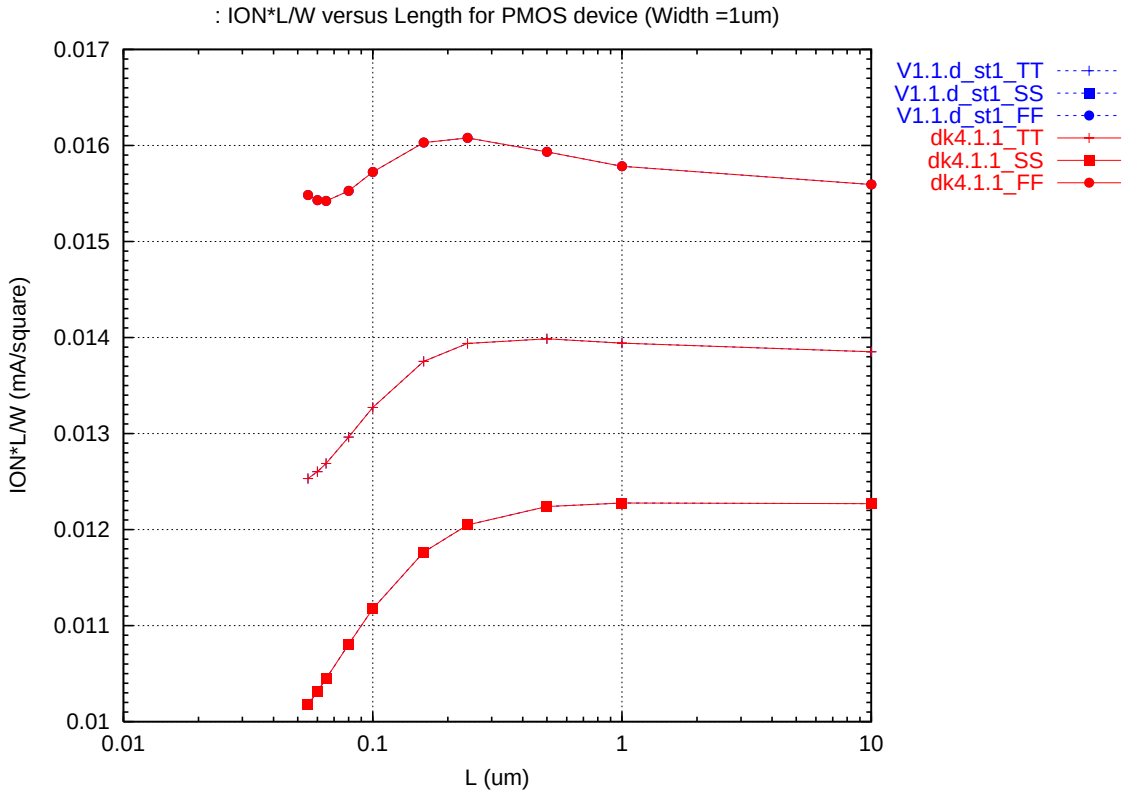

Figure 11 : ION versus drawn gate length for PMOS HVT_LP transistors (W = 1 µm)

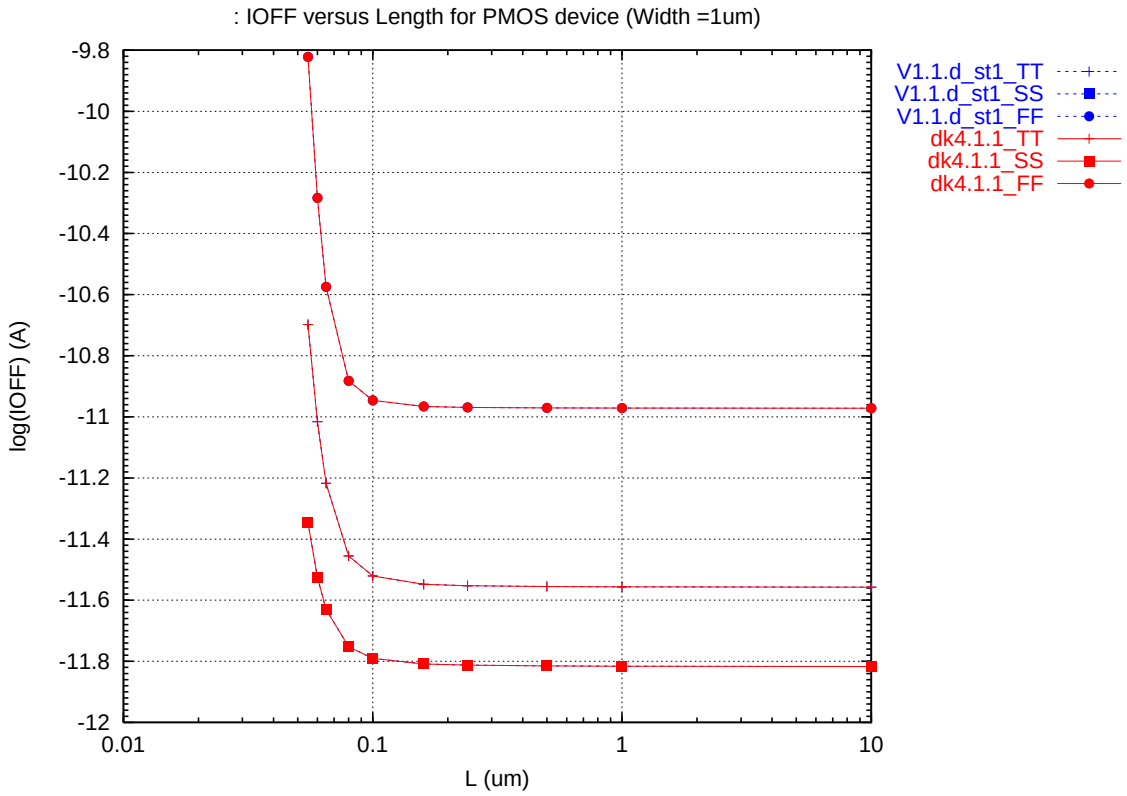

Figure 12 : IOFF versus drawn gate length for PMOS HVT_LP transistors (W = 1 µm)

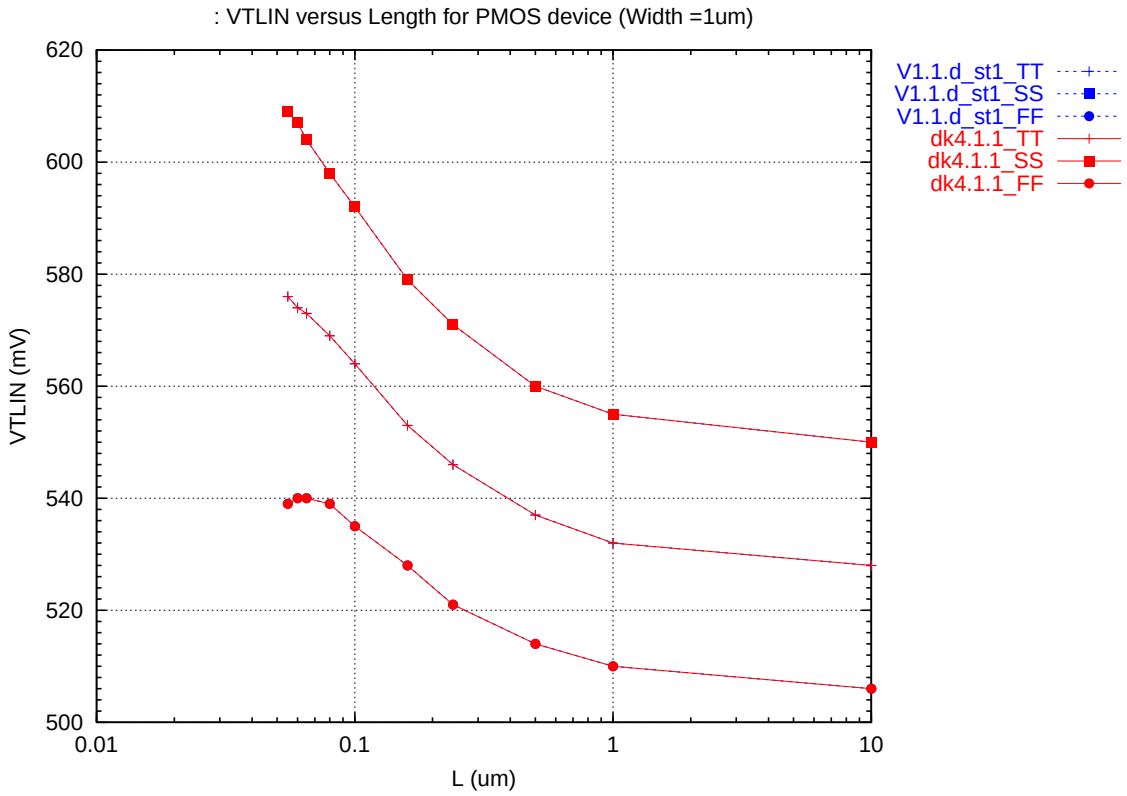

Figure 13 : Threshold voltage VTLIN versus drawn gate length for PMOS HVT_LP transistors (W = 1 µm)

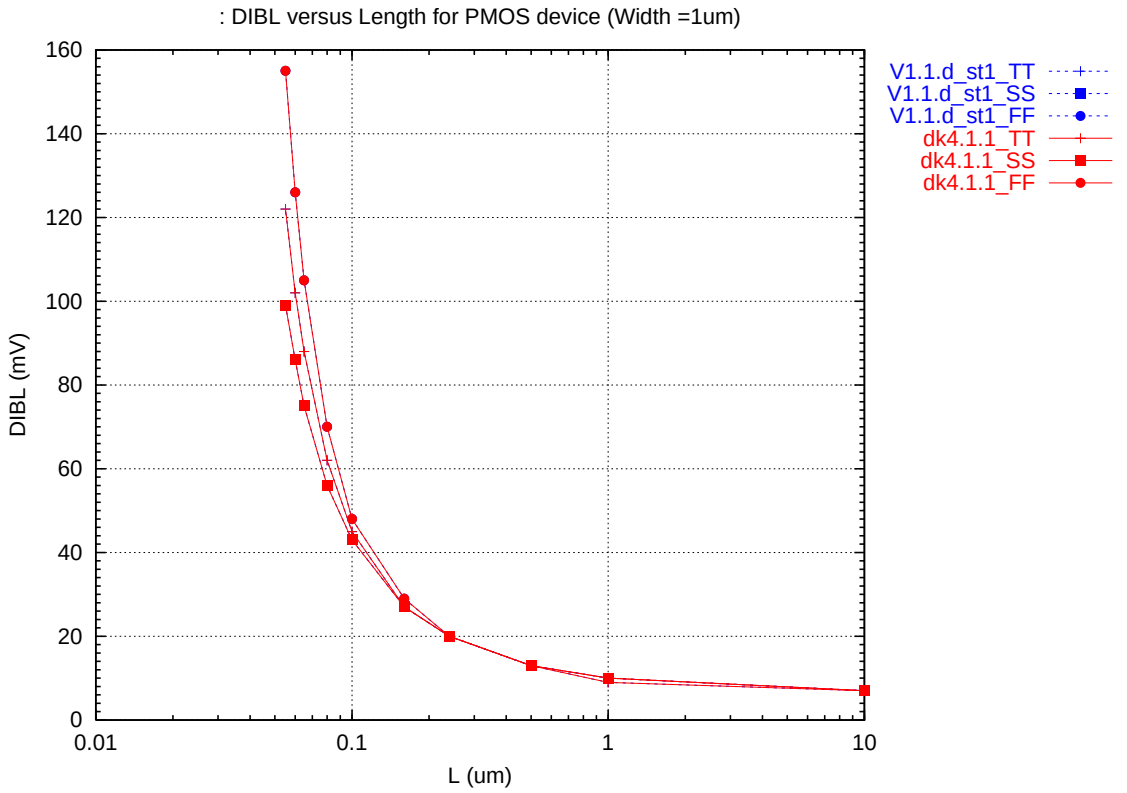

Figure 14 : DIBL= VTLIN-VTSAT versus drawn gate length for PMOS HVT_LP transistors (W = 1 µm)

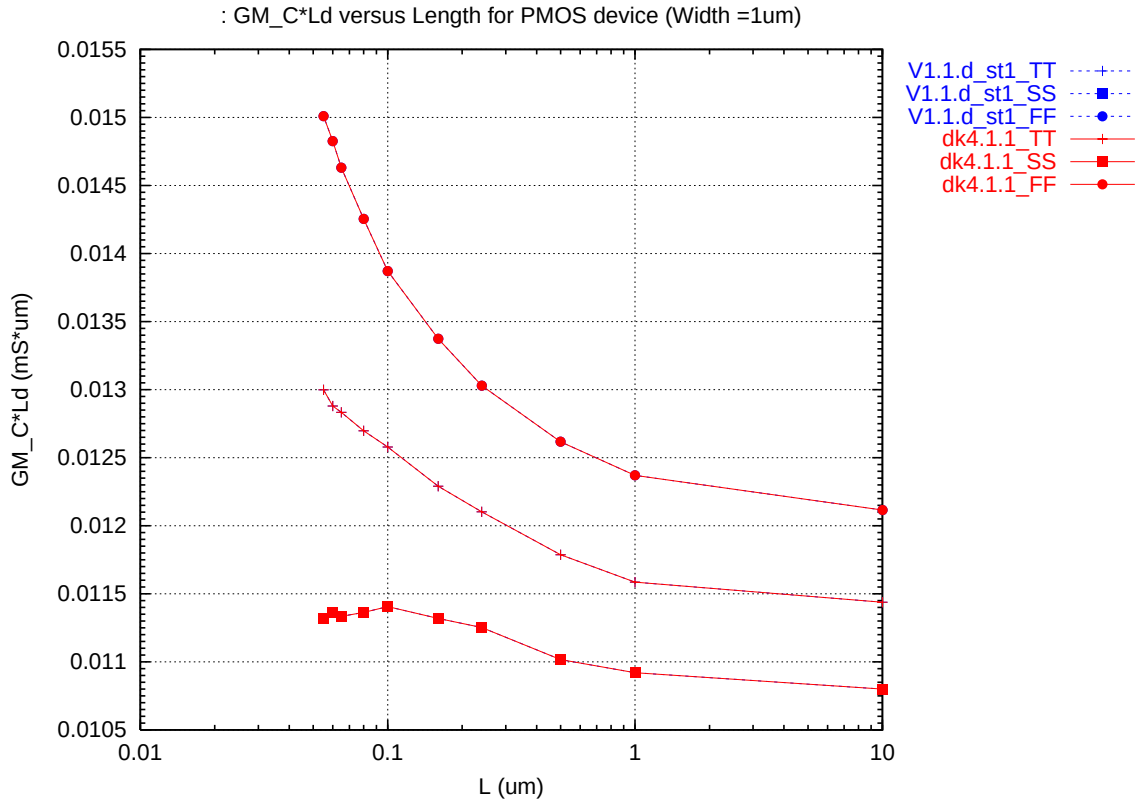

Figure 15 : GM*Ld versus drawn gate length for PMOS HVT_LP transistors (W = 1 µm)

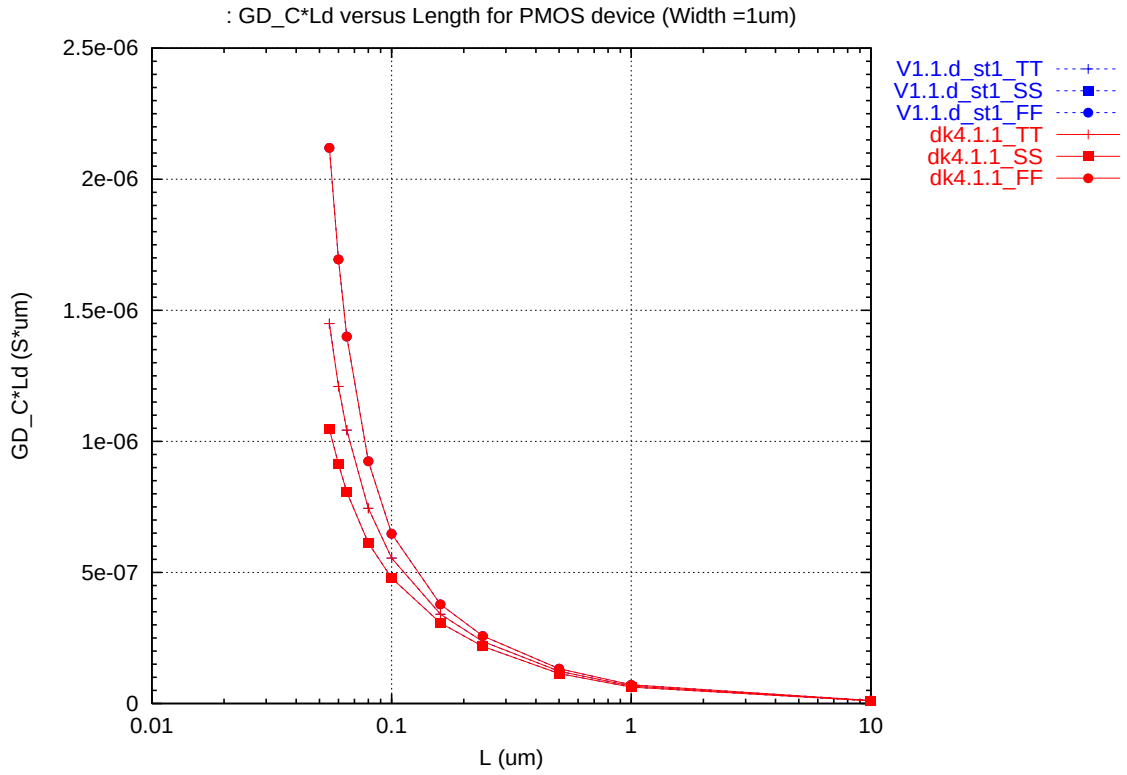

Figure 16 : GD*Ld versus drawn gate length for PMOS HVT_LP transistors (W = 1 µm)

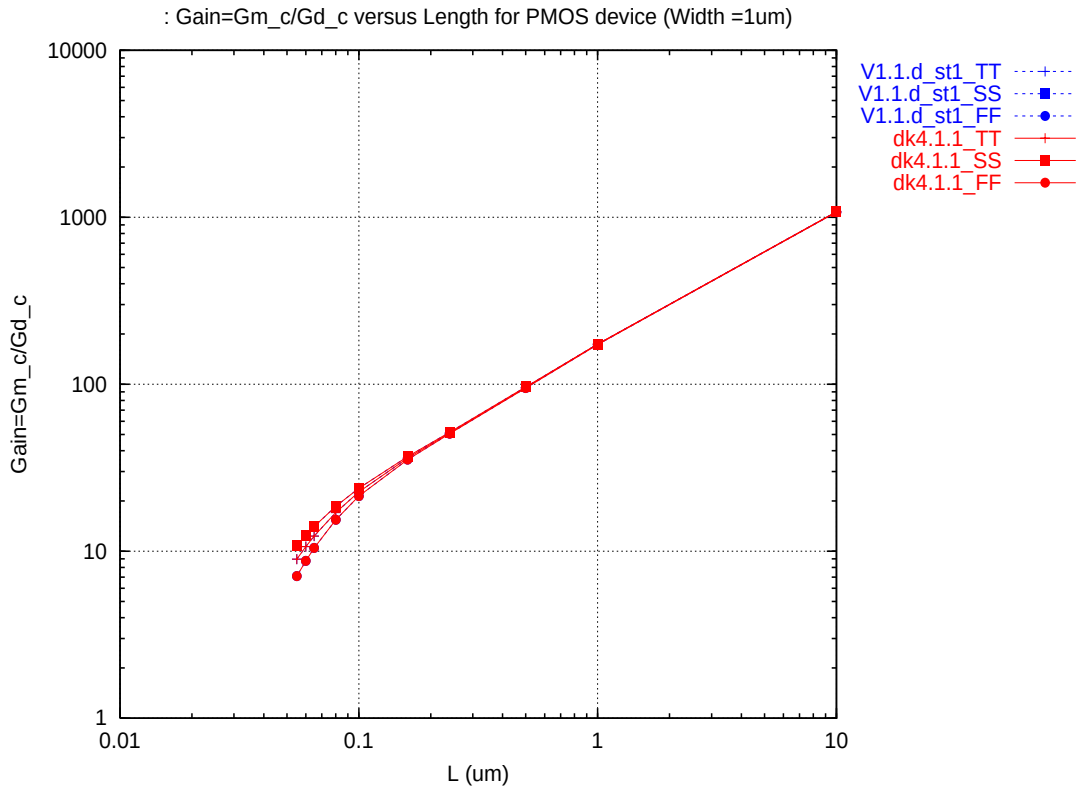

Figure 17 : GAIN versus drawn gate length for PMOS HVT_LP transistors (W = 1 µm)

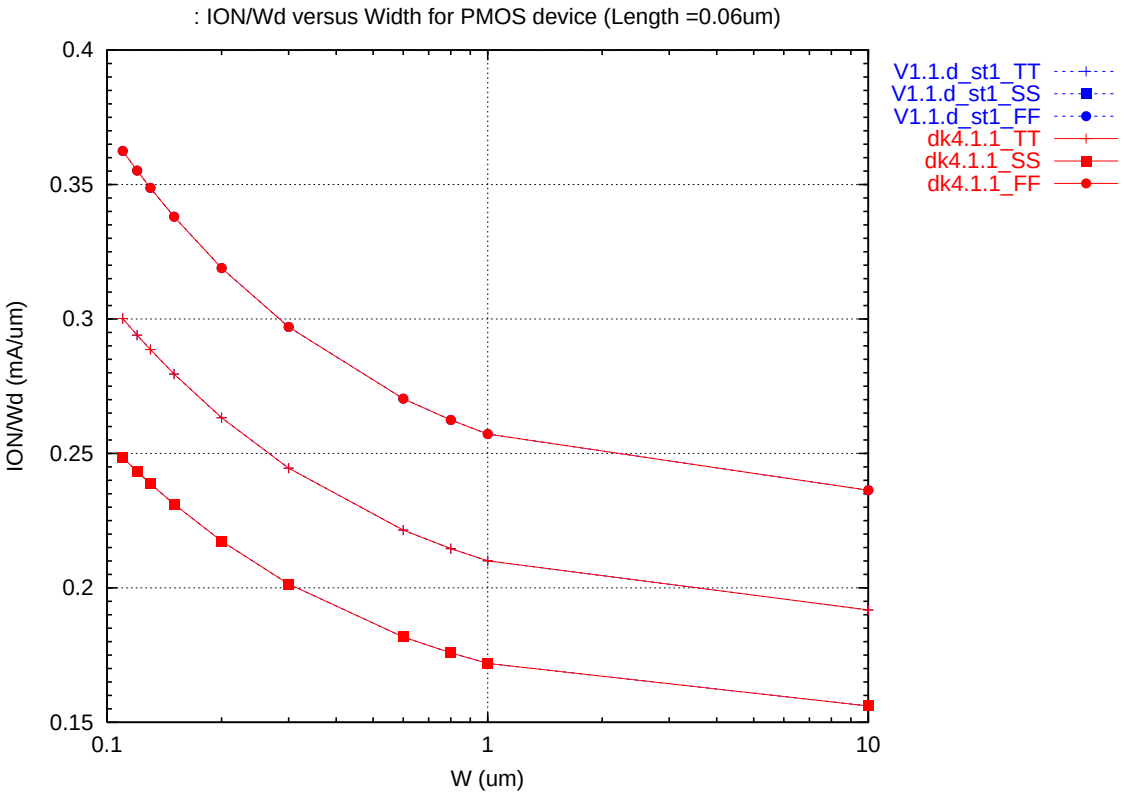

Figure 18 : ION versus drawn channel width for PMOS HVT_LP transistors (L = 0.06 µm)

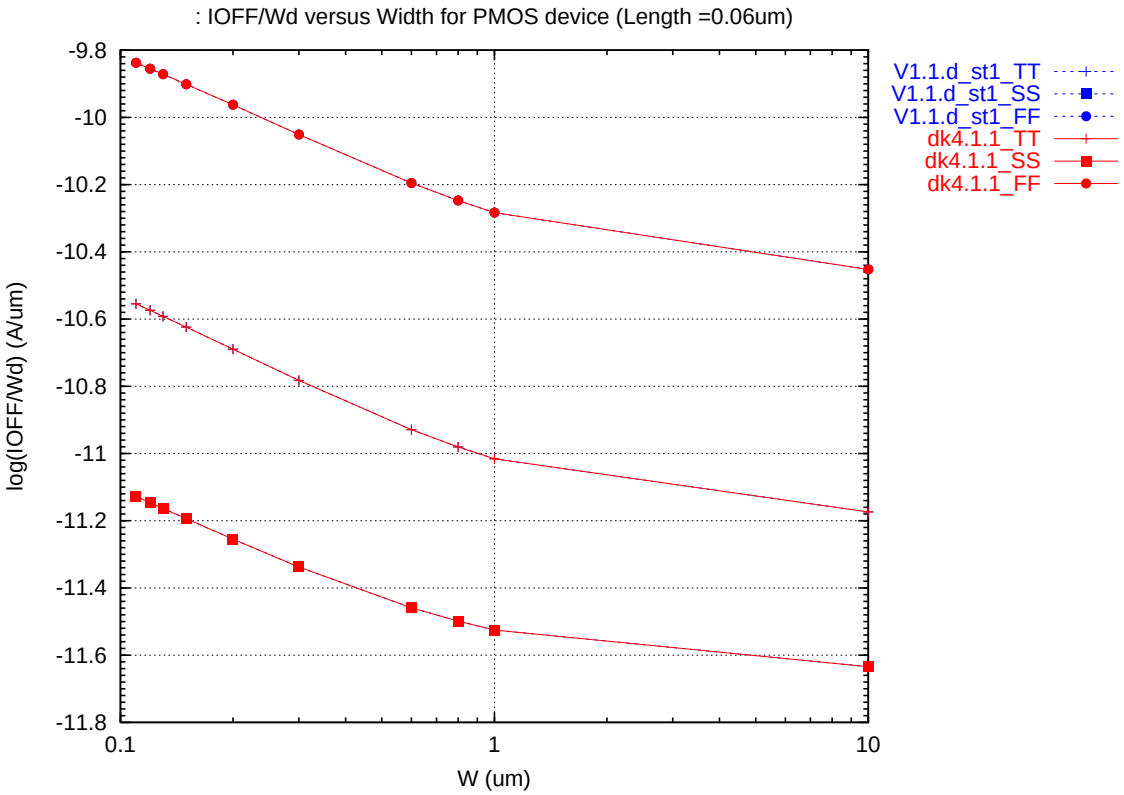

Figure 19 : IOFF versus drawn channel width for PMOS HVT_LP transistors (L = 0.06 µm)

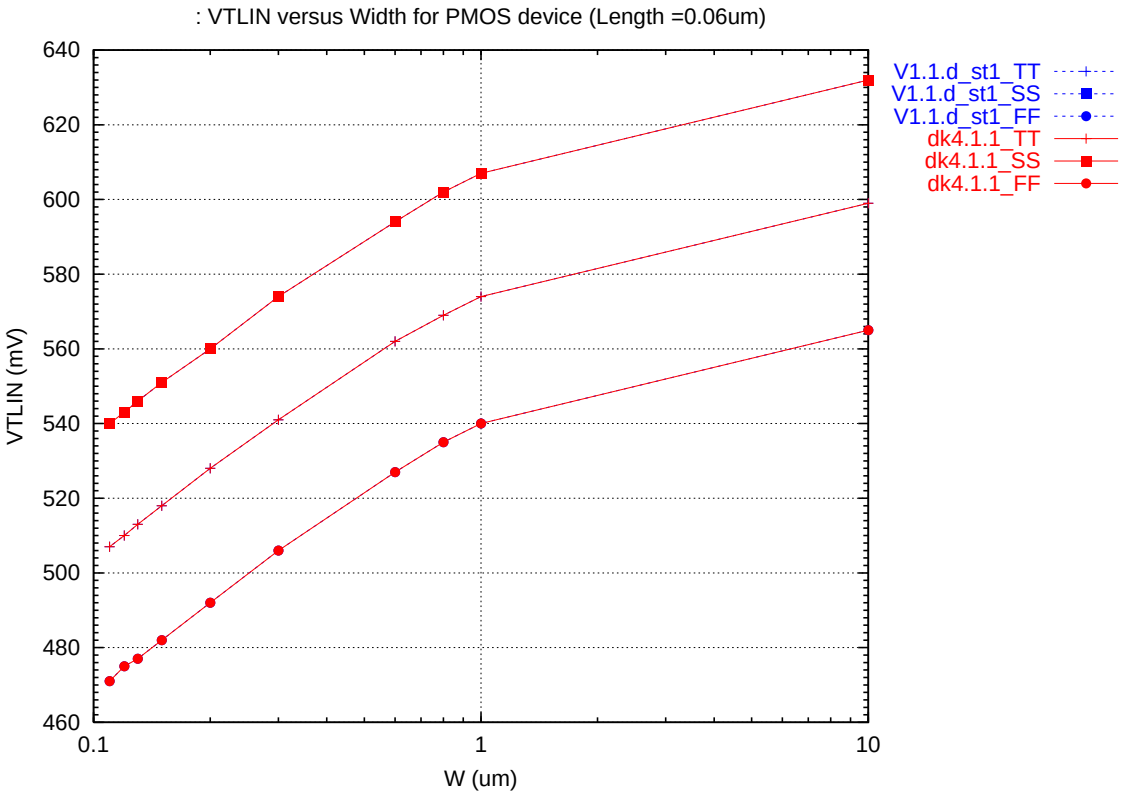

Figure 20 : Threshold voltage VTLIN versus drawn channel width for PMOS HVT_LP transistors (L = 0.06 µm)