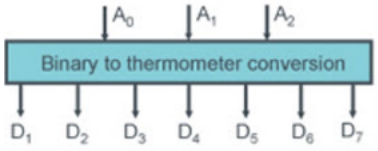
Binary to Thermometer Code Conversion Using If and Else Block Verilog

By G.Anitha 8:30 AM Verilog Program



Decimal	Binary			Thermometer code						
	A0	A1	A2	D1	D2	D3	D4	D5	D6	D7
0	0	0	0	0	0	0	0	0	0	0
1	0	0	1	0	0	0	0	0	0	1
2	0	1	0	0	0	0	0	0	1	1
3	0	1	1	0	0	0	0	1	1	1
4	1	0	0	0	0	0	1	1	1	1
5	1	0	1	0	0	1	1	1	1	1
6	1	1	0	0	1	1	1	1	1	1
7	1	1	1	1	1	1	1	1	1	1

```
`timescale 1ns / 1ps
//////////////////////////////////////////////////////////////////////////////////
// Company:
// Engineer: Manohar Mohanta
//
// Create Date:    07:31:52 08/10/2016
// Design Name:
// Module Name:    Btother
// Project Name:
// Target Devices:
// Tool versions:
// Description:
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
//////////////////////////////////////////////////////////////////////////////////
module Btother(
    input [2:0] b,
    output [6:0] t
    );
reg [6:0]t;
always @ (b)
begin
```

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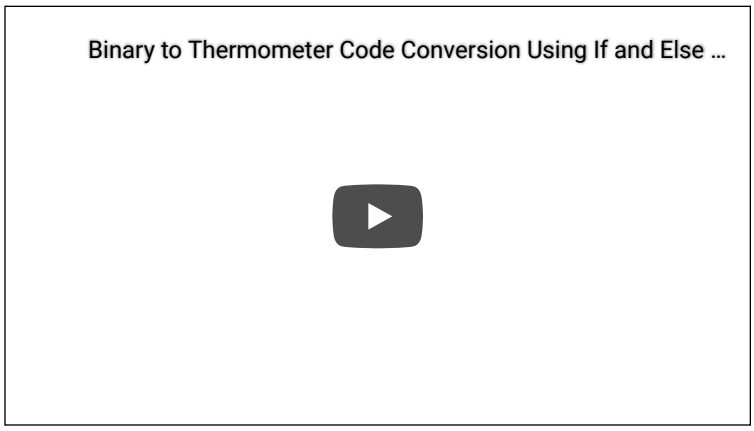
```
 if(b==3'b000)
  t=7'b0000000;
 else if(b==3'b001)
  t=7'b0000001;
 else if(b==3'b010)
  t=7'b0000011;
 else if(b==3'b011)
  t=7'b0000111;
 else if(b==3'b100)
  t=7'b0001111;
 else if(b==3'b101)
  t=7'b0011111;
 else if(b==3'b110)
  t=7'b0111111;
 else
  t=7'b1111111;
end
endmodule
```

Binary to Thermometer Code Conversion Using If and Else Block Verilog Test Bench

```
`timescale 1ns / 1ps

////////////////////////////////////////////////////////////////////////////////
// Company:
// Engineer: Manohar Mohanta
//
// Create Date:   07:43:23 08/10/2016
// Design Name:   Btother
// Module Name:   H:/Verilog/btother_tb.v
// Project Name:  Verilog
// Target Device:
// Tool versions:
// Description:
//
// Verilog Test Fixture created by ISE for module: Btother
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
////////////////////////////////////////////////////////////////////////////////

module btother_tb;

 // Inputs
 reg [2:0] b;

 // Outputs
```

```
wire [6:0] t;

// Instantiate the Unit Under Test (UUT)
Btother uut (
 .b(b),
 .t(t)
);

initial begin
 // Initialize Inputs
 b = 3'b000;#100;b = 3'b001;#100;
 b = 3'b010;#100;b = 3'b011;#100;
 b = 3'b100;#100;b = 3'b101;#100;
 b = 3'b110;#100;b = 3'b111;#100;
// Wait 100 ns for global reset to finish

 // Add stimulus here

end

endmodule
```



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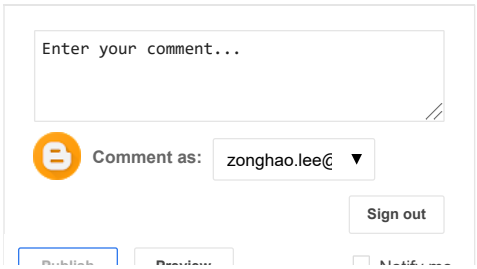

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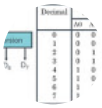

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