CSTRIP CAPACITOR MODEL

CROLLES2 ALLIANCE

CMOS65nm TECHNOLOGY

DEVICE MODELLING TEAM (SALIM EL GHOULI)

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OVERVIEW

The Cstrip device model is a physical model. The results of Quickcap[1] simulation (or measurements) are used to calculate the capacitance value of one elementary cross capacitor as well as specific and fringe capacitance between two consecutive metal layers. The capacitance value between two consecutive layers is calculated using the value of one elementary and repetitive shape taking into account parsitic capacitance contributions due to ring and access parts of the device[2].

The capacitive effect is mainly vertical. Compared to the equivalent device in the cmos090 technology kit product (cmsbe), the metal plates have been replaced by metal stripes.

❑ Pins

This device has two pins (plus and minus). PLUS pin is always surrounded by an upper and a lower stripes array (MINUS Pin) in upper and lower metal layers: consequently the number of metal layers required for this device is always an odd number (3 or 5). These metal layers can be:

- M1 (if bottom layer is Metal1)

- Thin metal (type X) layers available in the corresponding process option. This device does not involve the intermediate metal layers (type Y), nor the thick metal layers (type Z).

plus = plus (used as signal pin, it is the intermediate metal level)

minus = minus (shield around the plus pin, it is the top-layer and bottom-layer levels)

❑ Model nomenclature

Cstrip models are available only from metal1 to metal5 levels : M1-> M5

1. QuickCap is a parasitic capacitance extraction tool. It is used in applications that demand high 3D-extraction accuracy, such as process analysis, library cell characterization, parameter extraction and modeling, correlation studies, critical block design, and critical net analysis. QuickCap provides the high accuracy parasitic data required for accurate delay and signal integrity analysis, verification, and post-layout simulation.
2. See figure 2.

Cstrip 2 pin capacitor model name is: **cmstrstk** (for Capacitor Metal STRiped StacKed).

The device instantiation includes the right configuration of metals used to perform the capacitor: bottom metal to top metal (only thin metal is used). It is important to inform the model about the right metal configuration: capacitance value depends on it.

DEVICE INSTANTIATION PARAMETERS

❑ Model CALL for the 2 pin striped stacked capacitor:

Xname **Plus_Pin** **Minus_Pin** **ModelName** carea=**capacitor_area** cperi=**capacitor_perimeter** botlayer=**bottom_layer** toplayer=**top_layer** mismatch=**mismatch_flag** mult=**MULT_value** lpe=**LPE_Value** tometer=**microns_to_meter** c=**capacitance_value**[1]

Plus_Pin	is the first capacitor terminal
Minus_Pin	is the second capacitor terminal
ModelName	cmstrstk (string)
carea[a]	is the desired PLUS striped layer area of the capacitor (float)
cperi[b]	is the desired perimeter of the PLUS striped layer of the capacitor (see figure 2) (float)
botlayer	bottom metal layer used for the device (1, 2 or 3)
toplayer	top metal layer used for the device (3, 4 or 5)
mismatch	flag: to activate the mismatch effect for the device (0=disable, 1=enable)
mult	is the multiplication factor (parallel devices)
lpe	flag: is a user option to take into account the post-layout extraction mode (0,1, 2 or 3)
tometer	parameter used to transform distances in microns to meters unit (1 or 10e-6)
c	capacitance value (not used in the model)

a. takes discrete values as: $\text{Area} = (2 \cdot n - 1) \times (2 \cdot m - 1) \times W_S$ (1) where Ws is the stripe width and n,m are integer numbers.
b. takes discrete values as: $Peri = 4 \times (n + m - 1) \times W_S$ (2) where Ws is the stripe width and n,m are integer numbers.

1. The value specified here is not used in the model.

PCELL & LAYOUT

The layout of the striped stacked metal capacitor is a stack of parallel stripes, orthogonal from one metal level to the next one. Stripes have both their width and spacing predefined. These stripes are connected together with a metal ring, with the same width as stripes (figure 2).

The plus plate (between two minus plates) is underlaped w.r.t the side of the minus plate in order to be insensitive against outside perturbations. Metal allowed for this capacitor are only metal 1 and thin metal (Metal X). Only odd number of metal layers are allowed.

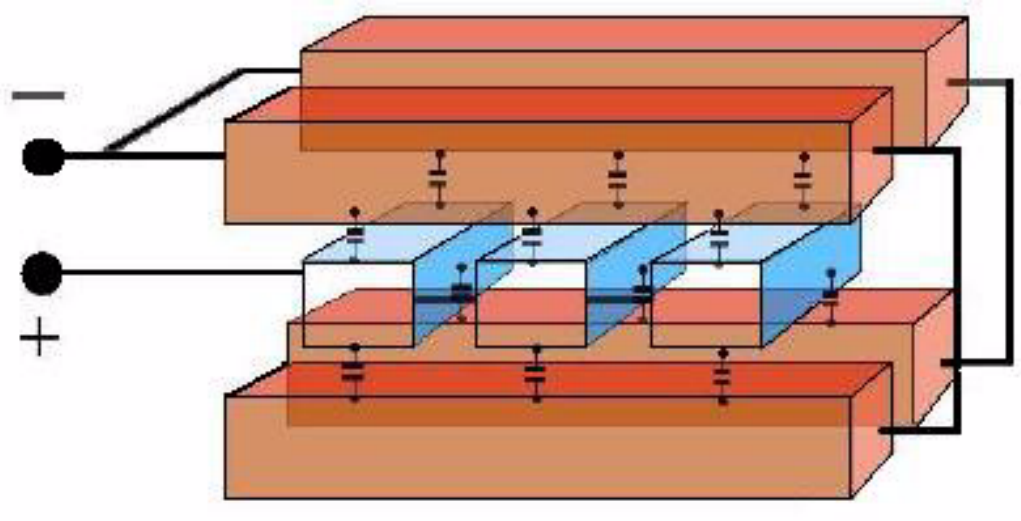

Figure 1 - 3D view of the core of cstrip Pcell

The main capacitance is between the two terminals (Plus and Minus).

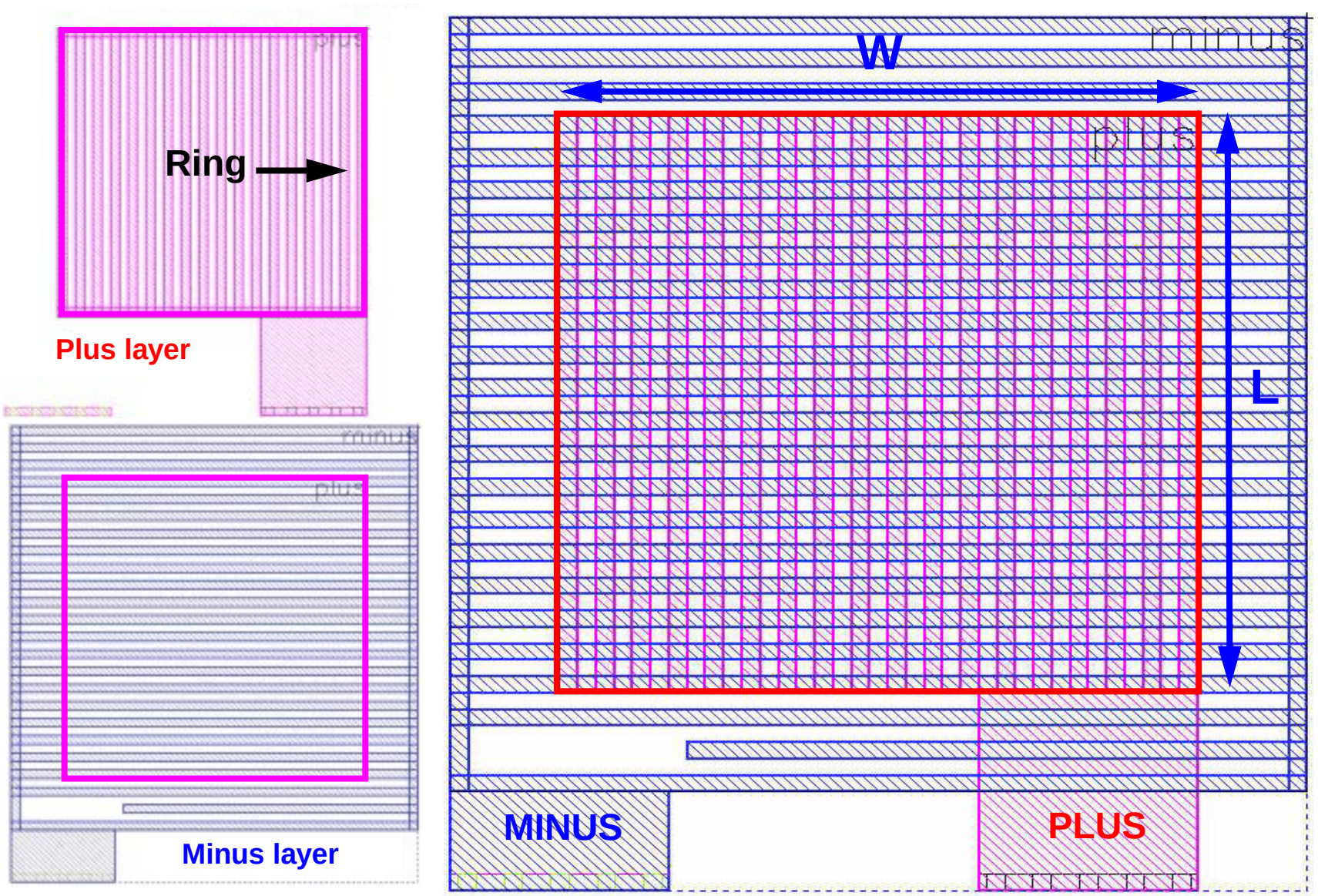

Figure 2 - Top view of cstrip Pcell (Layout)

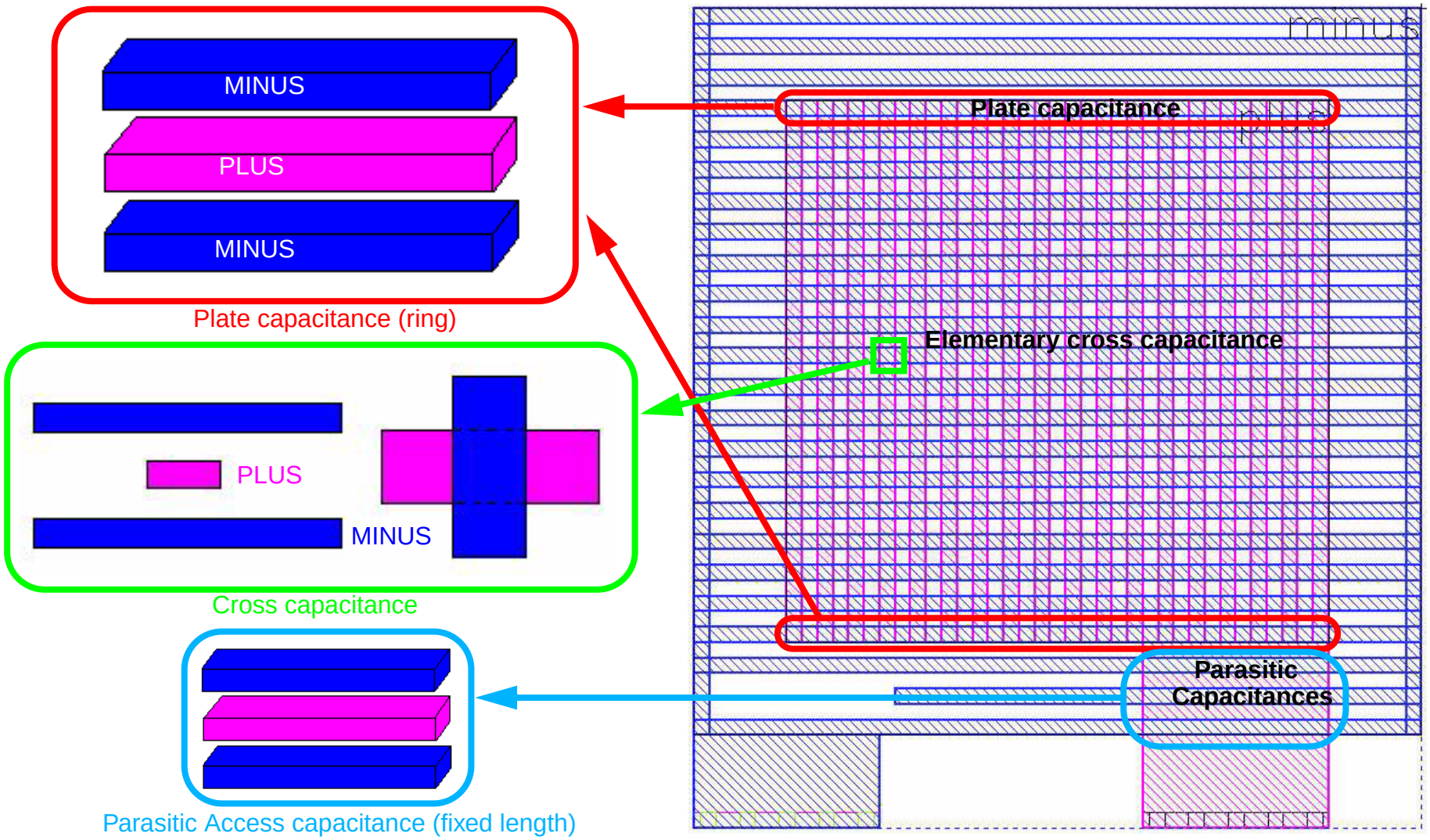

Figure 3 - Capacitance distribution

EQUIVALENT CIRCUIT SCHEMATICS

Capacitor model calculates the main capacitance which is accounted between the Plus/Minus terminals (Figure 1 and 3):

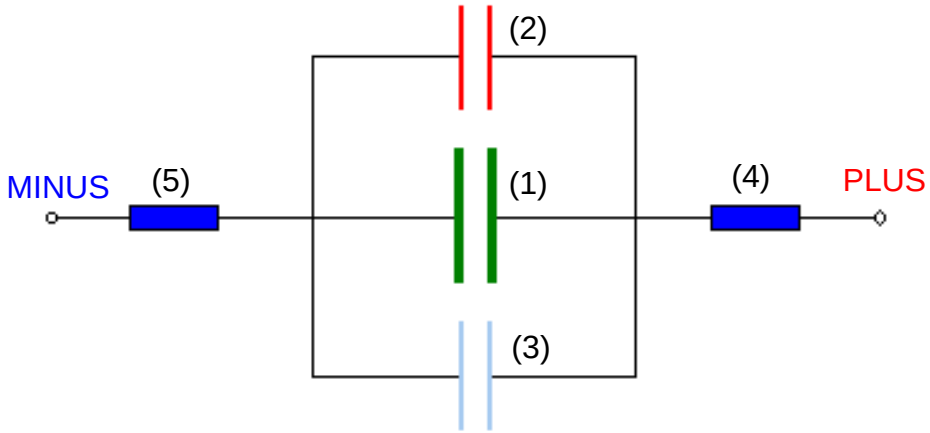

Figure 4 - Circuit diagram of cstrip device

- Cc (1): intrinsic (main) capacitor between the Plus/Minus terminals.
- Cplate (2): ring plate capacitance contribution (see figure 3).
- Cap_para (3): parasitic capacitor between the plus and minus terminals (due to acces to PLUS pin).

The model includes two series resistances: rvalp (4): for the plus terminal. It takes into account the vias (VIA1X, VIA2X, VIA3X, VIA4X or VIA5X) and the metal levels resistance belonging to the plus layer. rvalm (5): for the minus terminal. It takes into account the vias (VIA1X, VIA2X, VIA3X, VIA4X or VIA5X) and the metal levels resistance belonging to the minus layer.

CAPACITANCE CALCULATION

Capacitance value is written as (see figure 3):

$$\text{Capacitance} = n \times \text{Cm1mx} + m \times \text{Cmxmx} \qquad (3)$$

where:

n : is a number of m1-mx elementary vertical capacitors in a stacked device (0 or 1)

m : is a number of mx-mx elementary vertical capacitors in a stacked device (1, 2 or 3)

$$\text{Cm1mx} = \text{numcross} \times \text{Ccross1x} + 2 \times \text{C1xplate} + 3 \times \text{Cap1x\_para}$$

$$\text{Cmxmx} = \text{numcross} \times \text{Ccrossxx} + 2 \times \text{Cxxplate} + 3 \times \text{Capxx\_para}$$

where:

numcross : number of repetitive cross shapes in one level = number of plus stripes * (number of minus stripes - 2)

Ccross1x (Ccrossxx) : capacitance value of one cross elementary shape between metal layers type 1 - type x (type x - type x)

C1xplate (Cxxplate) : capacitance value of the plate region of internal ring (two stripes: see figures 2 and 3)

Cap1x_para (Capxx_para) : capacitance value (fixed) of parasitic access (3 stripes: see figure 3)

MODELED EFFECTS

GEOMETRY SCALING

Number of stripes for minus and plus terminals are calculated using expressions:

$$\text{nplus} = \frac{1}{2} \cdot \left(E\left[\frac{W}{Ws} \right] + 1 \right) \quad (4)$$

$$\text{nminus} = \frac{1}{2} \cdot \left(E\left[\frac{L}{Ws} \right] + 1 \right) \quad (5)$$

where:

nplus: is number of stripes in plus layer

nminus: is number of stripes in minus layer

W, L: are respectively width and length of the device

Ws: is a width of one stripe = space between two stripes.

The instantiation is done using area and perimeter. The length and the width are calculated using the system of equations:

$$Area = L \times W \quad \text{and} \quad \text{Perimeter} = 2 \times (L + W) \quad (6)$$

thus[1] : $L = \frac{Peri}{4} + \frac{1}{2}\sqrt{\left(\frac{Peri}{2}\right)^2 - 4 \times Area}$ and $W = \frac{Peri}{4} - \frac{1}{2}\sqrt{\left(\frac{Peri}{2}\right)^2 - 4 \times Area}$ (7)

The capacitance value contribution of one elementary capacitor is then calculated using the expression (1)

Nplus (and nminus) variations for a square[2] cstrip capacitor versus capacitor area see curves shown bellow (From L=W=10µm to 15µm):

1. Hypothesis: L > W (without this consideration we obtaine two different configurations)
2. nplus = nminus

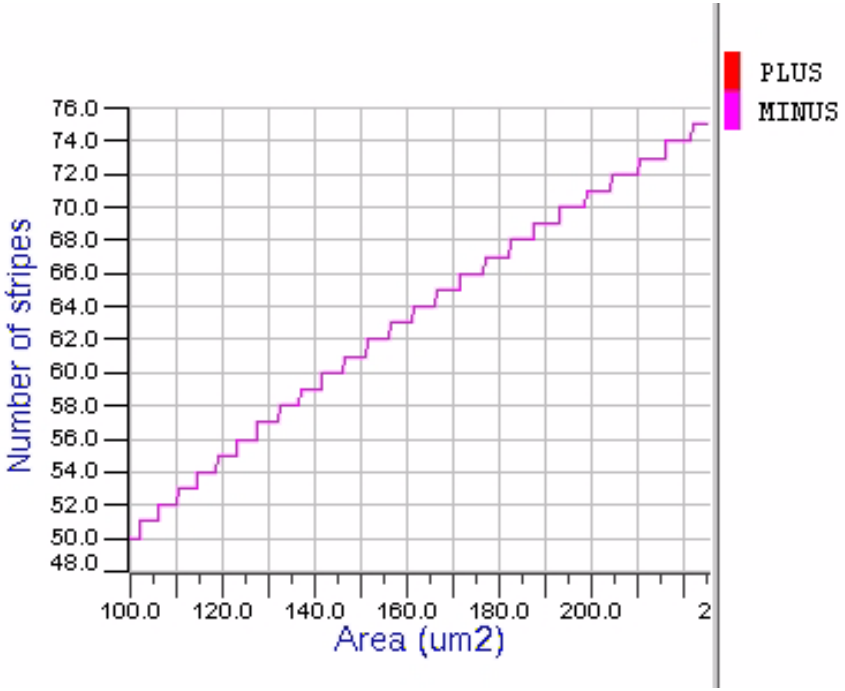

Figure 5 - Number of plus and minus stripes versus Area (square capacitor)

Variation of capacitance value for same geometry is shown in figure below:

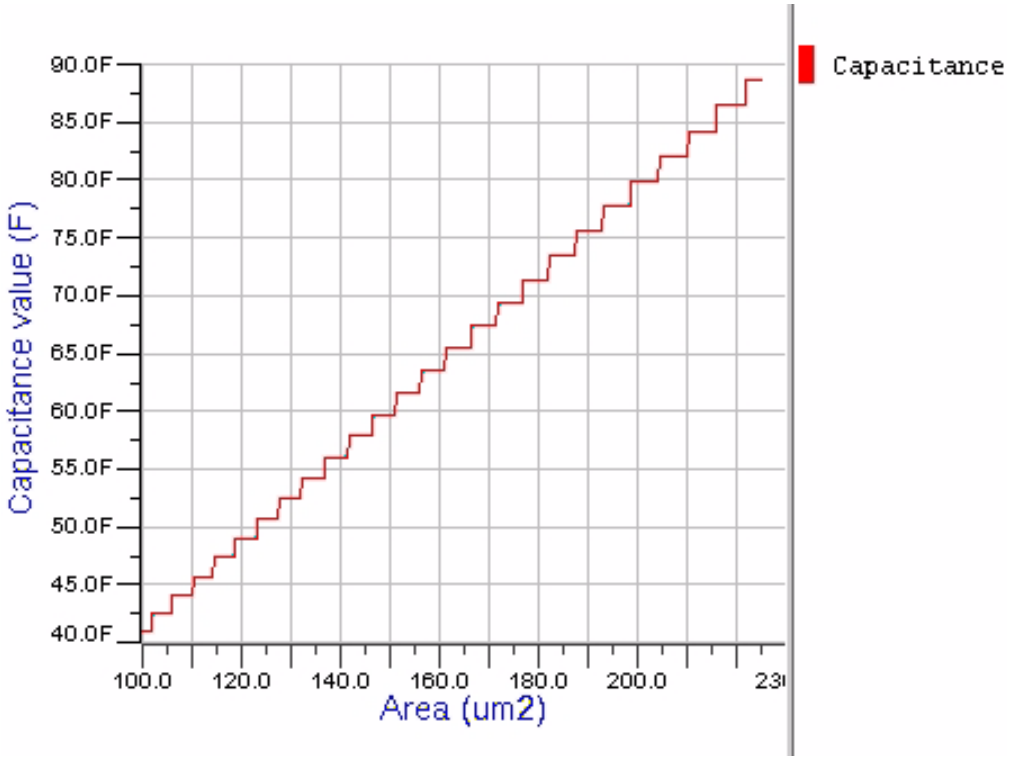

Figure 6 - Capacitance value versus Area (square capacitor)

Variation of specific capacitance for same geometry is shown in figure below:

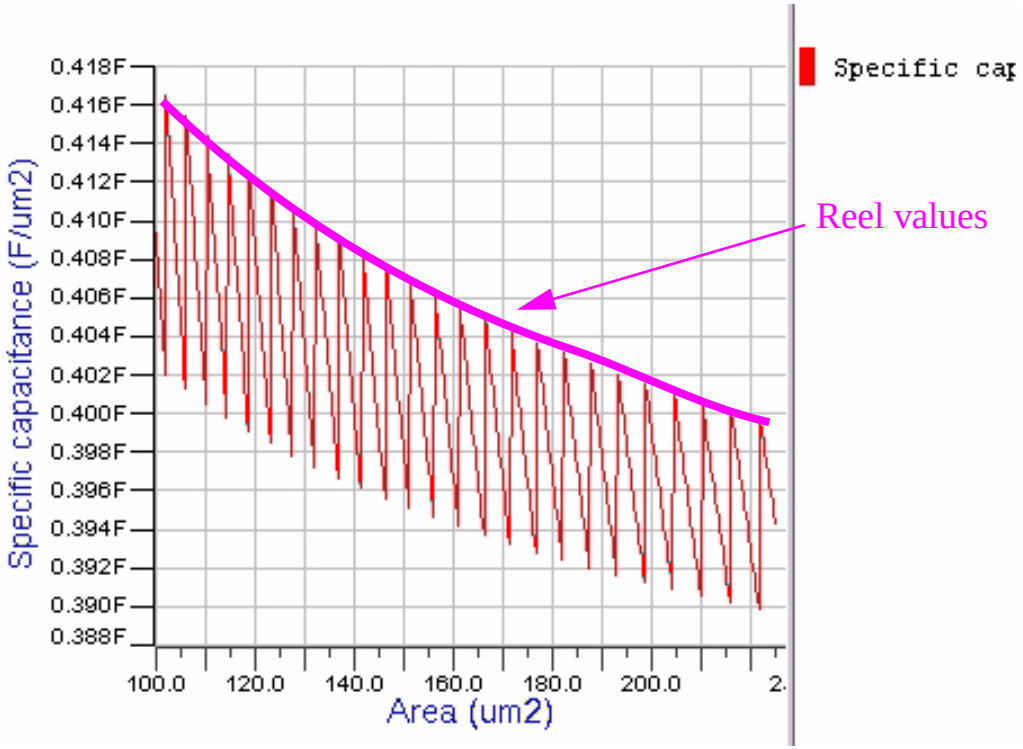

Figure 7 - Specific capacitance versus Area (square capacitor)[1]

1. Area of cstrip capacitor takes discrete values: thus capacitance value (specific capacitance) doesn't take all values shown in figures 6 and 7.

MISMATCH MODEL

A normal distribution is used to estimate the expected main capacitance value:

$$capacitance = c0 \times (1 + \varepsilon)$$

where

- c0 : is the mean capacitance value given by the equation (1)
- ε : is a normal distribution with a standard deviation given by:

$$\sigma = \frac{c\_A}{\sqrt{2 \times c0}}$$

where

c_A : is the mismatch coefficient given by measurement values.

When c_A parameter is not specified no distribution is used and capacitance value is equal to c0.

The normal distribution is provided using the Eldo function: gauss

$$\varepsilon = 0 \qquad dev/gauss = 'fudge \times c\_A/(\sqrt{2 \times c0})'$$

where

fudge is a security parameter. It is used to be sure that the capacitance range covers measurements.

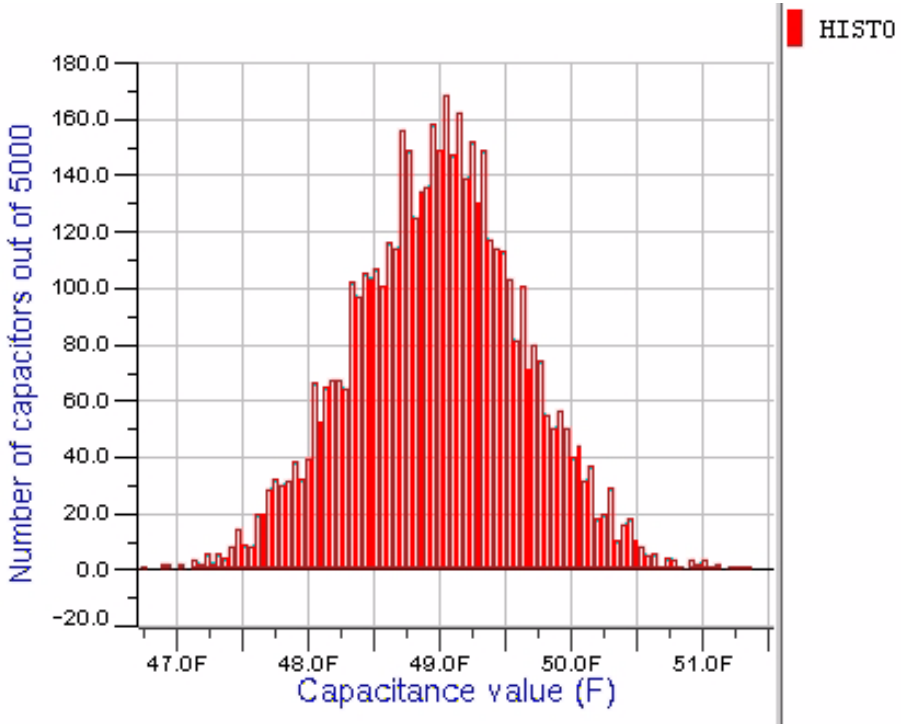

Figure 8 - Number of capacitors out of 5000 versus capacitance value

Example above is done for one cstrip capacitor (number of stripes plus = 55 ; number of stripes minus = 55) simulation gives roughly: 49fF as capacitance value.

Relative[1] Standard Deviation specified: 13.13M

Relative Standard Deviation simulated (5000 random selection using a Monte Carlo Analysis): 13.24M

1. Standard deviation = Relative Standard deviation * Capacitance value.

PARASITIC COMPONENTS

- **Series Resistors:**

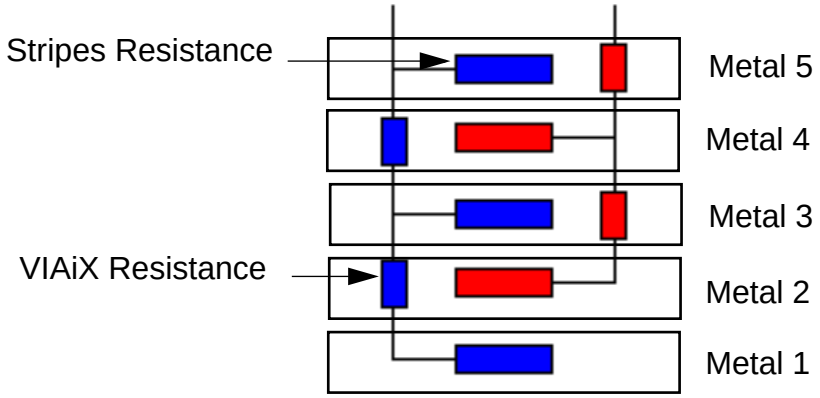

Figure 9 - Parasitic Resistors configuration for Pins: PLUS and MINUS

Stripes resistance: is the equivalent resistance of all one level layer stripes[1]

1. in calculation of this resistance we consider parallel stripe resistors (hypothesis)

POST LAYOUT SIMULATION

The cstrip model is managed by the LPE flag option, which permits to select the Resistor/Capacitor access modeling mode. See the following table depicting the proposed options :

LPE	Body	Access_R	Access_C	Extraction_mode
0	yes	yes	yes	--
1	yes	yes	no	C
2	yes	no	yes	R
3	yes	no	no	RC

The Front-End Models (F-E) :

cmstrstk, a complete model which contains intrinsic and parasitic capacitances (between the Plus/Minus terminals) and parasitic series resistances (LPE=0).

The Back-End Models (B-E) :

The **cmstrstk** B-E model is identical to the **cmstrstk** F-E model concerning the main capacitance (LPE=1,2 or 3 according to the user choice) but it excludes parasitic resistors (LPE=2, 3).

CORNERS CONSTRUCTION

❑ Design Rule Manual parameters

rsq_M1_t, rsq_M2_5_t, rsq_M1_l, rsq_M2_5_l and rviax parameter corners are given by DRM

❑ Simulation parameters

Model coefficients ca1x, caxx, cf01x and cf0xx are extracted using Quickcap simulations and the expressions below:

$$C\_TYP = ca\_TYP \times Area + cf0\_TYP \times Perimeter$$

$$C\_MAX = ca\_MAX \times Area + cf0\_MAX \times Perimeter$$

$$C\_MIN = ca\_MIN \times Area + cf0\_MIN \times Perimeter$$

Model coefficients ccross1x and ccrossxx are extracted using Quickcap simulations.

Figure below shows capacitance corners versus area. This result depends on the construction of MAX and MIN corners.

Simulations are done for a square cstrip capacitor: L=W=10µm -> L=W=15µm

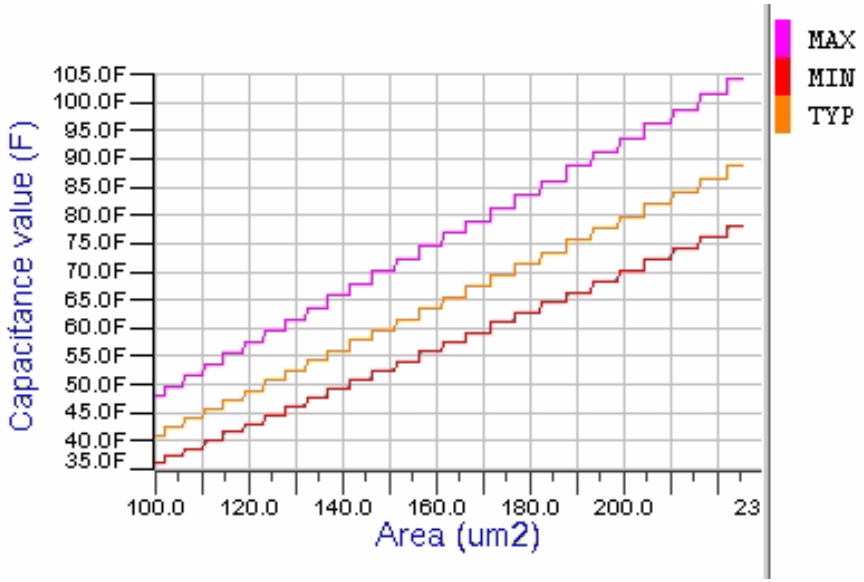

Figure 10 - Example of capacitance corners simulation (MAX and MIN)

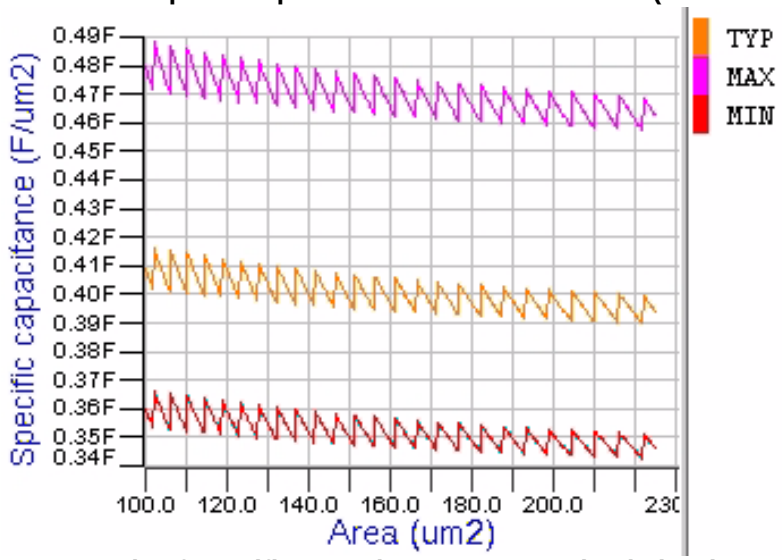

Figure 11 - Example of specific capacitance corners simulation (MAX and MIN)

MODEL PARAMETER LIST

careamin	(m2) Area min=lmin*wmin
careamax	(m2) Area max=lmax*wmax
careadef	(m2) Area def=ldef*wdef
cperimin	(m) Perm. mini= 2*(lmin+wmin)
cperimax	(m) Perim max= 2*(lmax+wmax)
cperidef	(m) Perim def= 2*(ldef+wdef)
wmin	(m) Minimal Width (Pcell)
wmax	(m) Maximal Width (square: 10pF)
wdef	(m) Width def (square: 100fF)
lmin	(m) Minimal Length doc1 (MiX.A.2)
lmax	(m) Maximal Length (10pF)
ldef	(m) Length def (square: 100fF)
nspmin	() number of stripes min for PLUS pin
nspmax	() number of stripes max for PLUS pin
nspdef	() number of stripes def for PLUS pin
nsmmin	()number of stripes min for MINUS pin
nsmmax	() number of stripes max for MINUS pin
nsmdef	() number of stripes def for MINUS pin
c_A	(sqrt(F)) for cap. mismatch

ws	(m) Width metaln for stripes
wsp	(m) Space between two stripes
wpar	(m) Width of parasitic block
lpar	(m) Length of parasitic block
nvia	() Number of contact vias
cdef	() botlayer=1 and toplayer=5
ccross1x	(F) Capacitance value of one cross (m1-mx)
ccrossxx	(F)Capacitance value of one cross (mx-mx)
ca1x	(F/m2) Specific capacitance (m1-mx)
caxx	(F/m2) Specific capacitance (mx-mx)
cf01x	(F/m) Fringe capacitance (m1-mx)
cf0xx	(F/m) Fringe capacitance (mx-mx)
rviax	(ohm) Rvia unit resistance X type
rsq_M1_t	(ohm/square) sheet Resistance of M1 (DOC1 7.6.3) small W
rsq_M2_5_t	(ohm/square) sheet Resistance of metals M2 to M5 (DOC1 7.6.3) small W
rsq_M1_l	(ohm/square) sheet Resistance of M1 (DOC1 7.6.3) large W
rsq_M2_5_l	(ohm/square) sheet Resistance of metals M2 to M5 (DOC1 7.6.3) large W