SPICE 50 ANG POLY/WELL CAPACITOR

CMOS065 CPOLY25 V0.1

CMOS065 MOS MODELLING TEAM

CONTENTS

INTRODUCTION

- **Based on silicon lot Q527AJA wafer , the models of 50Ang N+/Nwell and P+/PWell capacitors have been extracted.**
- **The extracted model has been centered with additionnal measurement data from Q536ZGV**
- **The 50Ang (P-Cell based) extrinsic capacitors have been added to the centered model, leading to the final model.**
- **The results of extracted, centered and final model are here presented.**

CORNER GENERATION

The corners of the V0.1 50A poly/well capacitor model are realized on the base of 3σ regarding the following technological tolerances:

Oxide thickness : +/- 2.5 Ang
Poly over-etch : +/- 10.5 nm
STI over-etch : +/- 15 nm
Vfb deviation: +/- 17.88 mV
Nsub deviation: x2 / x0.5
Oxide eps deviation: +/- 6%
Silicon eps deviation: +/- 6%
STI oxide thickness deviation: +/- 300 Ang

EXTRACTION CONDITIONS

- **Temperature: 25°C**

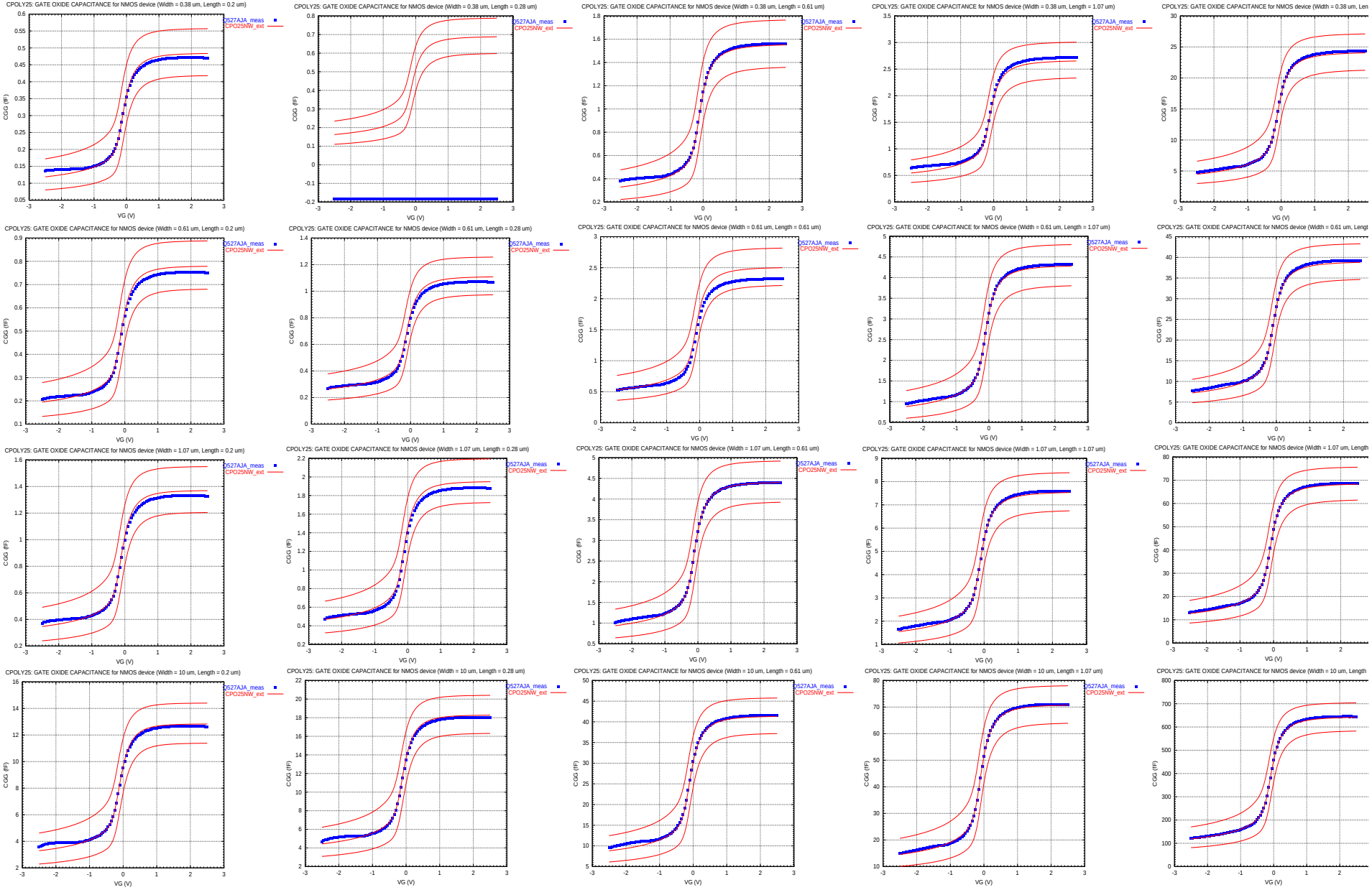
- **Capacitors used for extraction**

Width\Length	0.2 µm	0.28 µm	0.61 µm	1.07µm	10µm
Wd=0.38 µm	X	X	X	X	X
Wd=0.61 µm	X	X	X	X	X
Wd=1.07 µm	X	X	X	X	X
Wd=10 µm	X	X	X	X	X

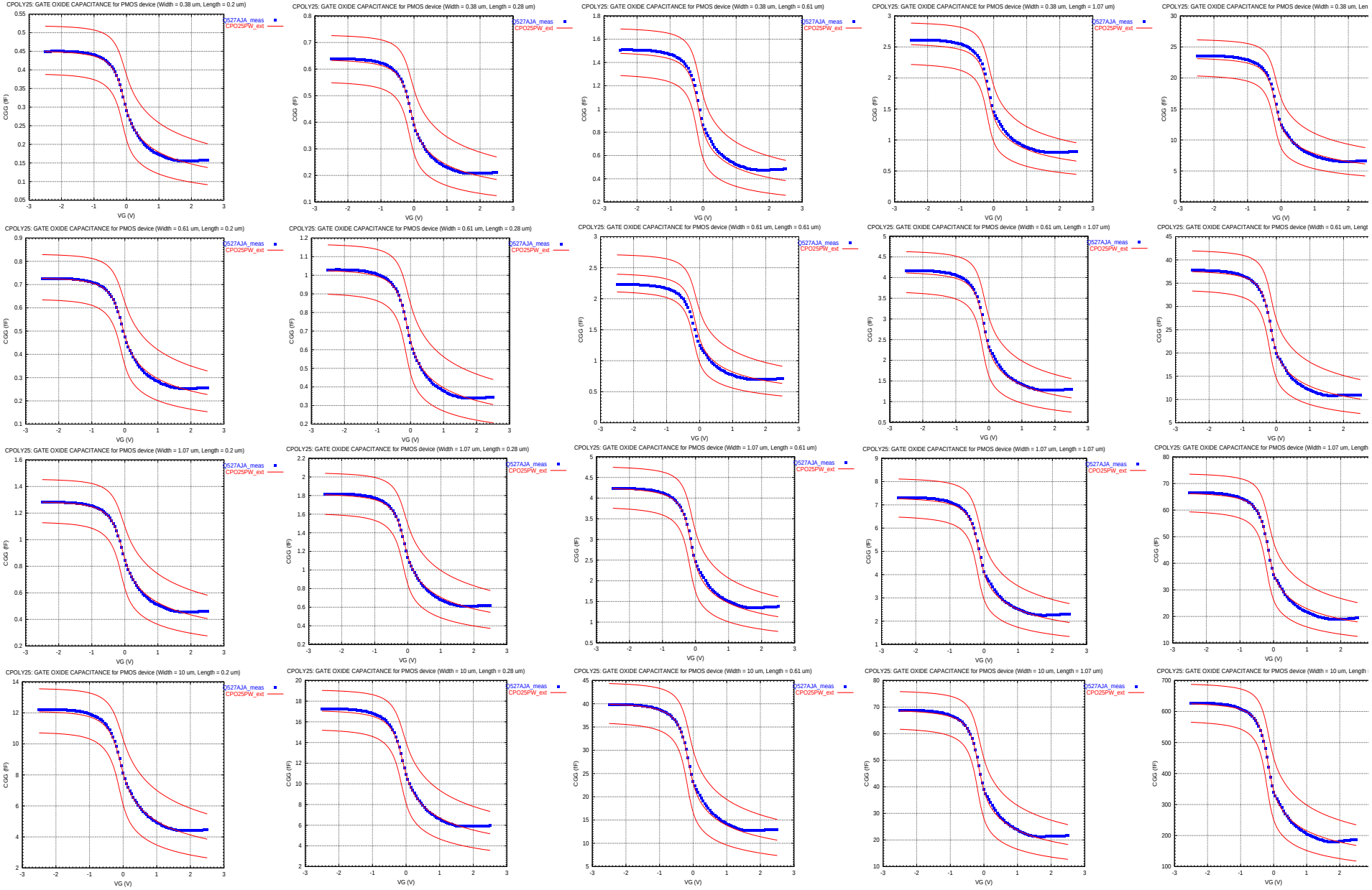
Table 1: Matrix of capacitors used for analysis

- **Method:**
  - C-V measurement on matrix of capacitors and calibration structures
  - Intrinsic capacitance calculation per device, including raphael calibration values
  - Modelisation of individual W,L devices
  - Parameter smoothing functions used for W,L scaling effects
  - Final model integrating P-cell parasitic capacitors

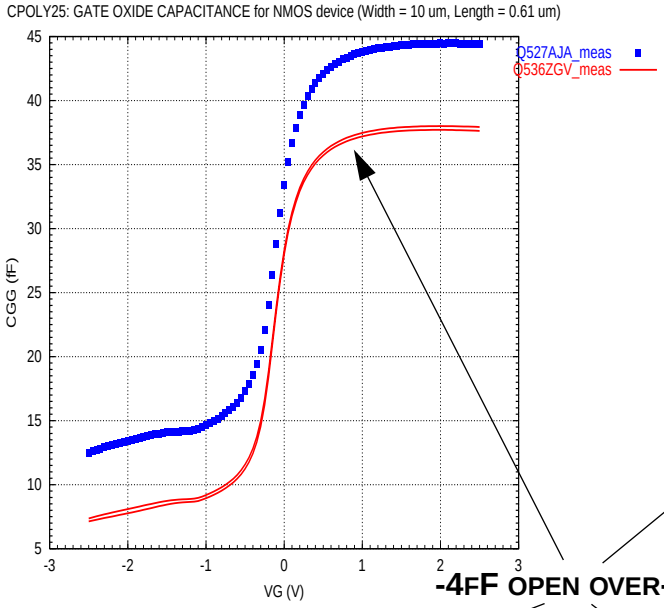
Ext N+/Nwell CPOLY25: intrinsic oxide capacitance

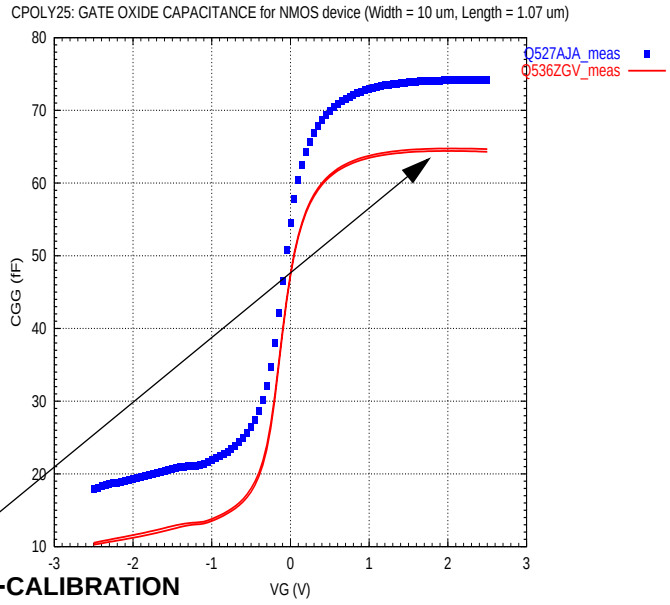


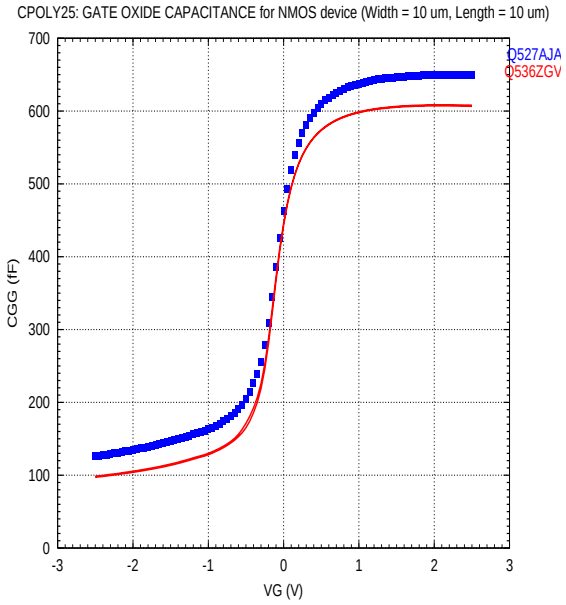
Ext P+/Pwell CPOLY25: intrinsic oxide capacitance



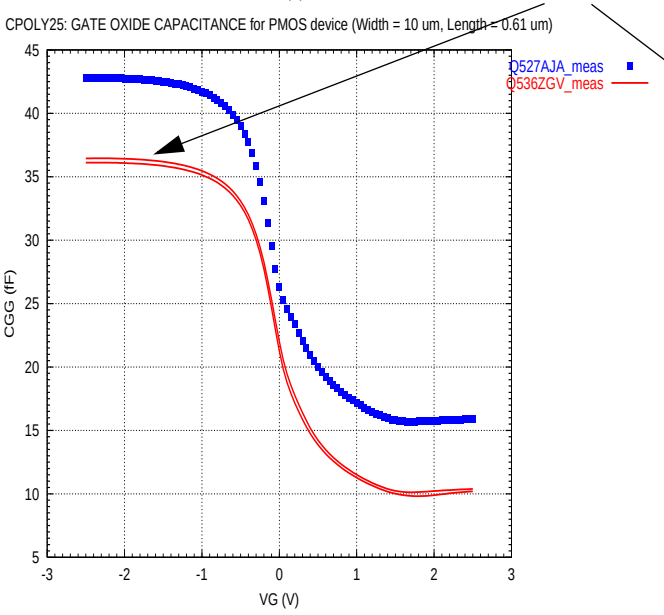
CPOLY25: Q527AJA vs Q536ZGV

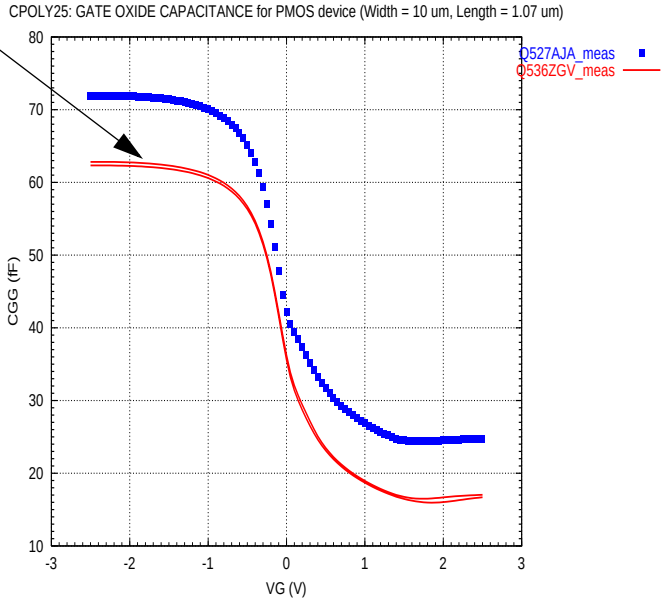


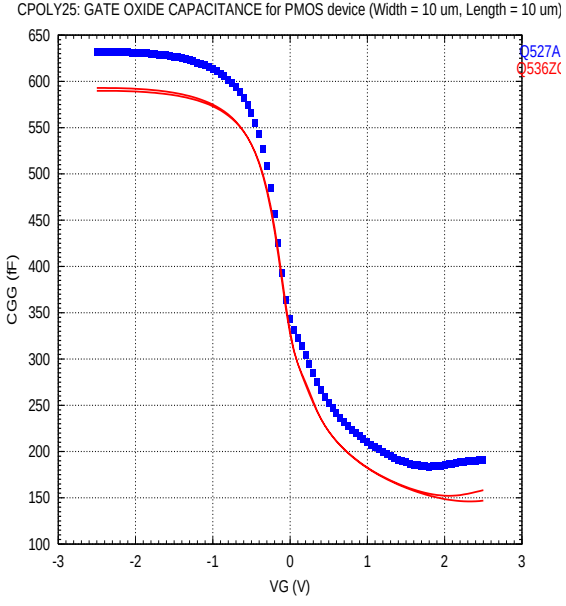




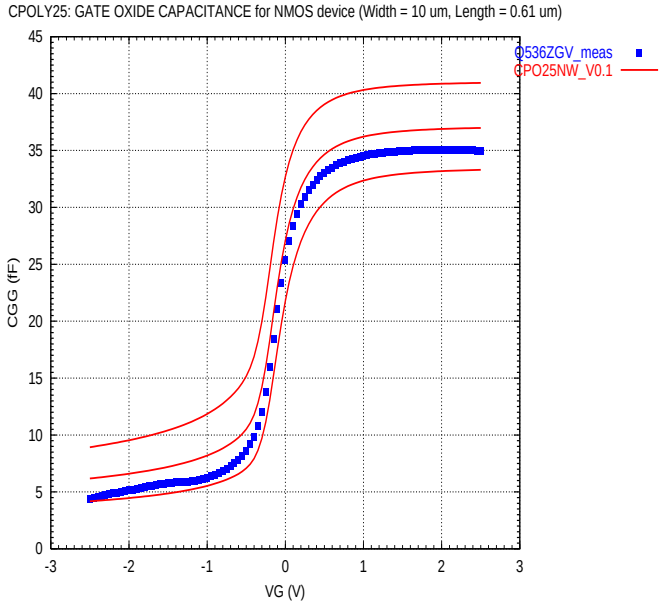
-4FF OPEN OVER-CALIBRATION

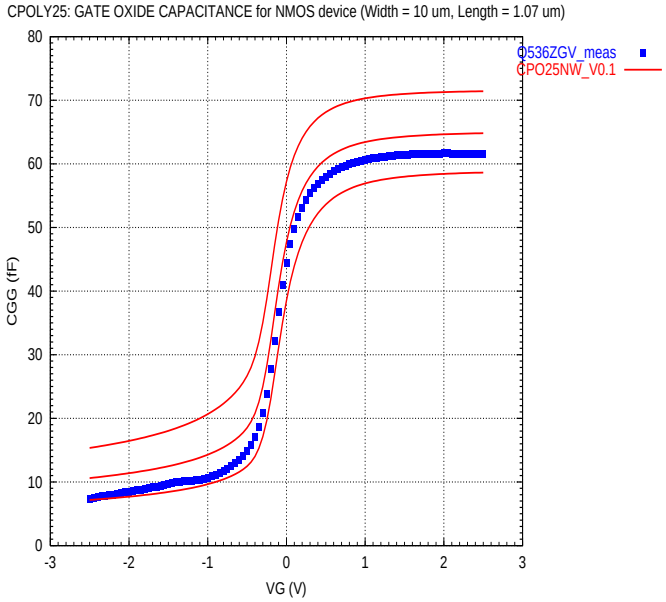


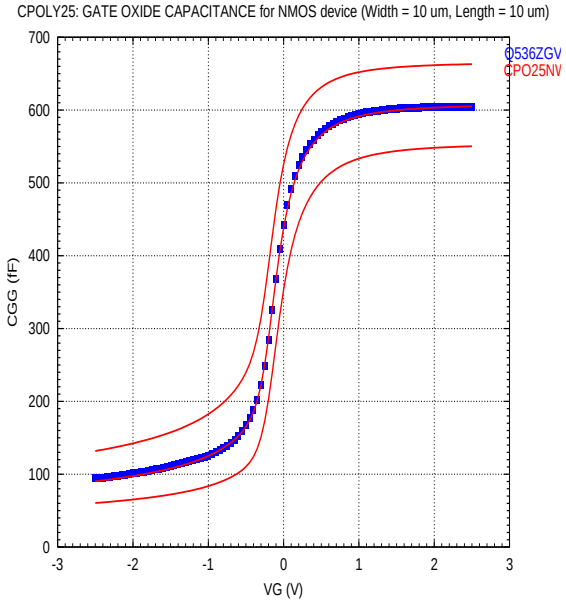


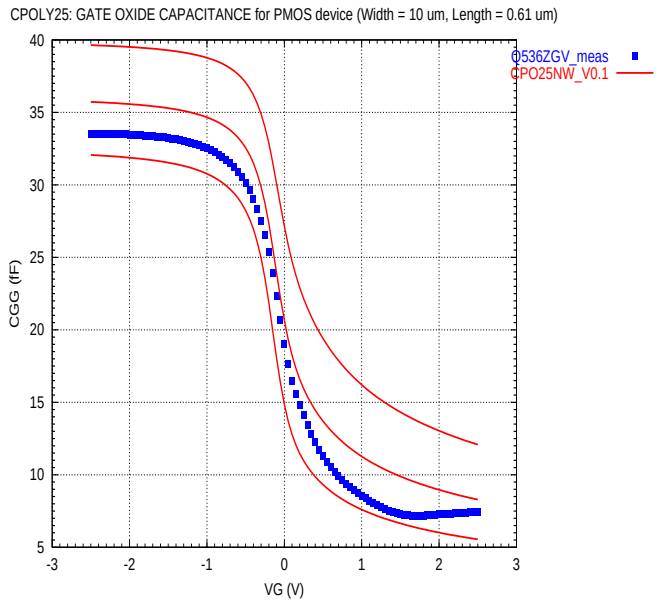


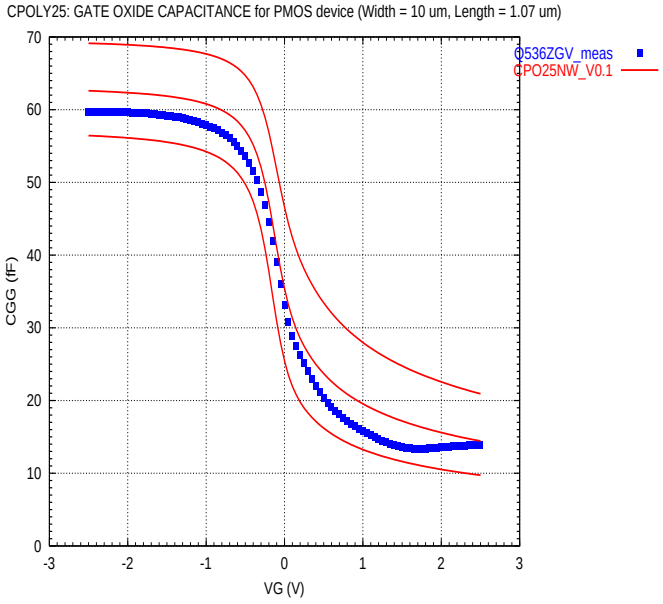
CPOLY25: CENTERED MODEL VS Q536ZGV - INTRINSIC

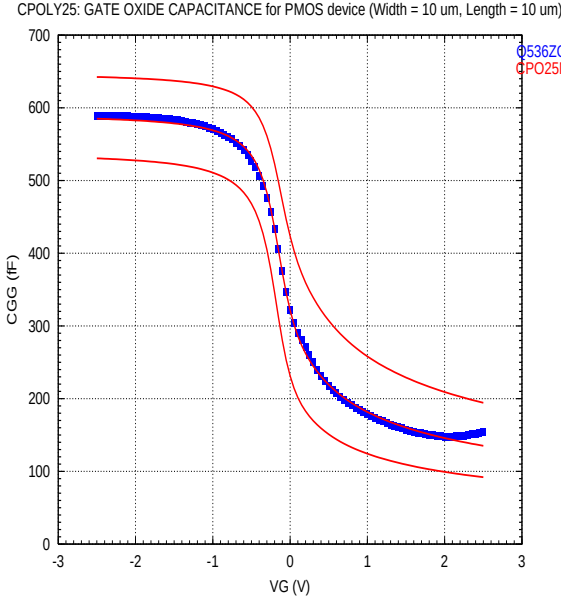




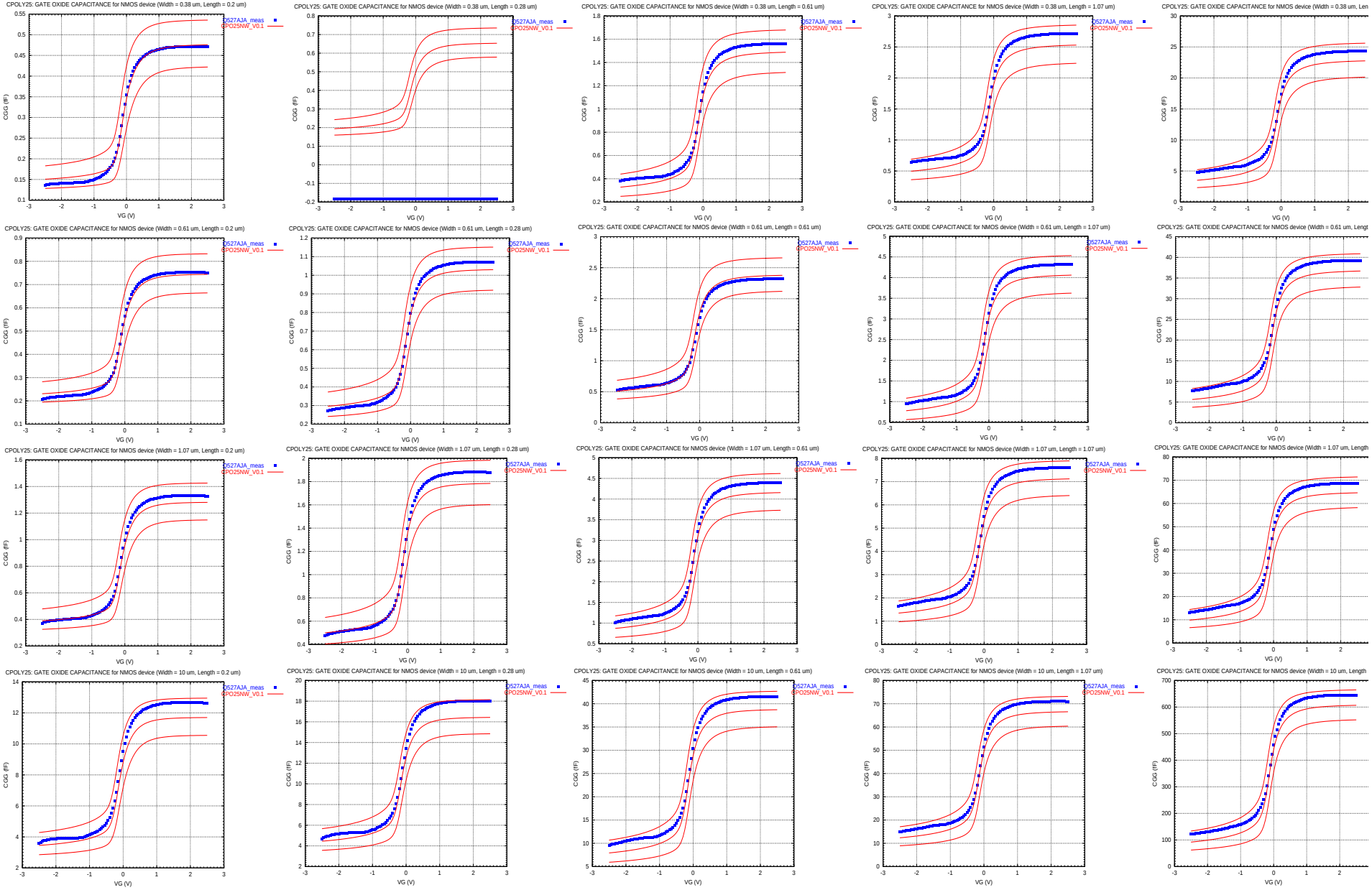




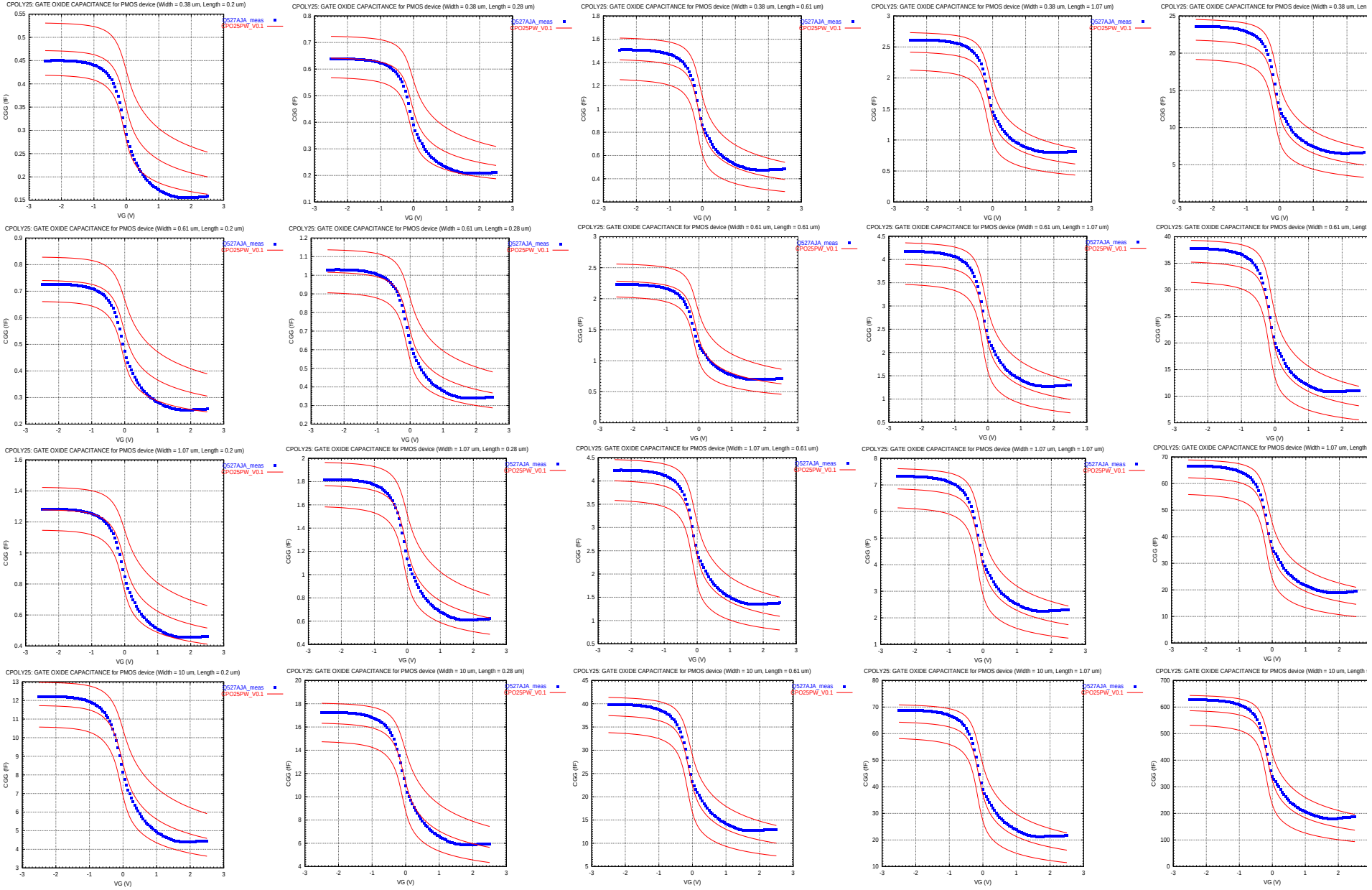




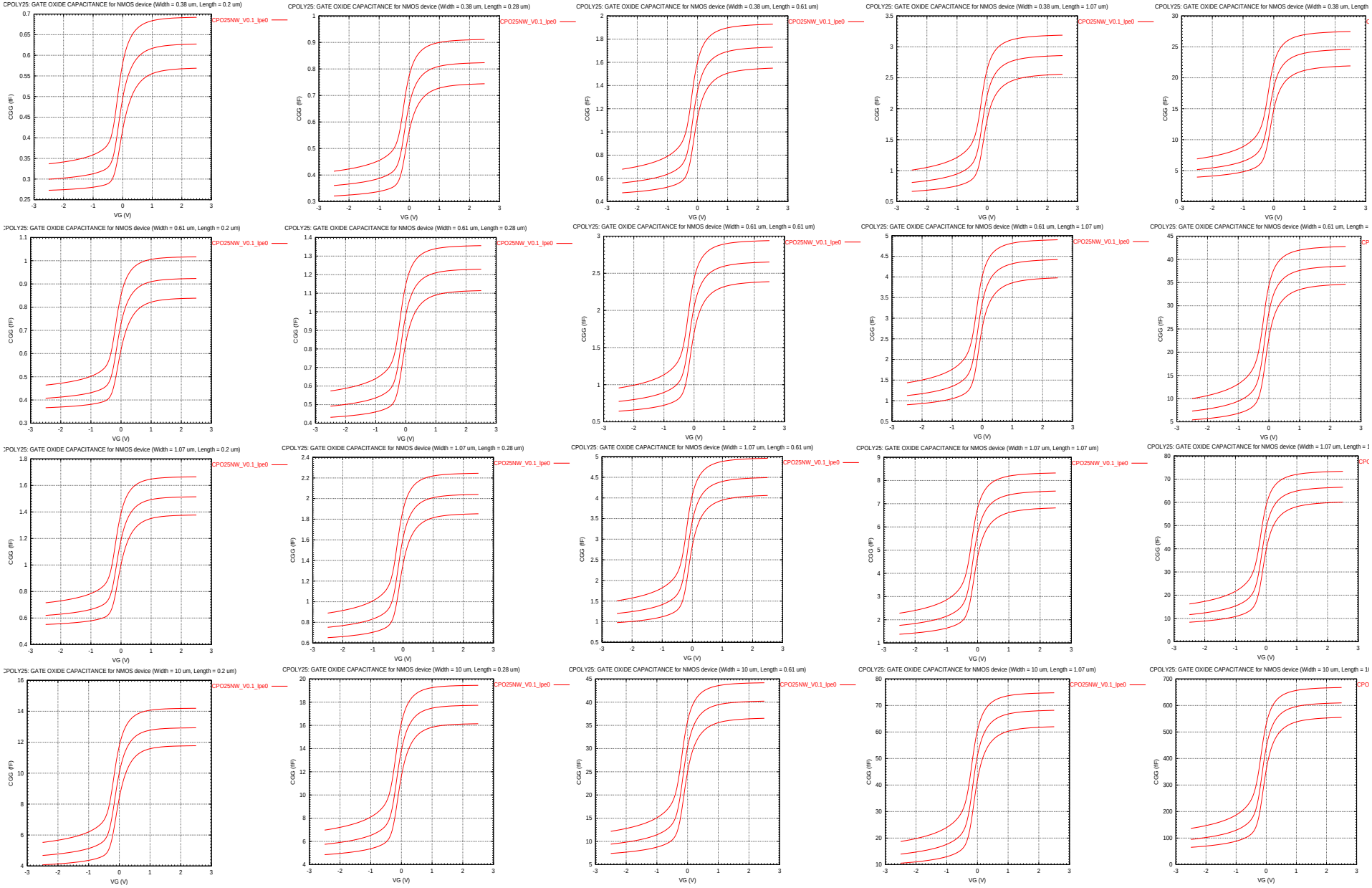
Centered N+/Nwell CPOLY25: intrinsic cap vs AJA



Centered P+/Pwell CPOLY25: intrinsic cap vs AJA



N+/Nwell CPOLY25 v0.1: lpe=0



P+/Pwell CPOLY25 v0.1: lpe=0