

VHDL/VERILOG CODING

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VHDL code for a 3-bit binary to thermomete r converter

june 21, 2017



Author :

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Platform : Xilinx

code : VHDL

```
//bit binary to  
thermometer  
converter//  
library IEEE;  
use  
IEEE.STD_LOGIC_11  
64.ALL;  
use  
ieee.numeric_std.all;  
entity bin2therm2bit  
is  
    port (  
  
        binary_input : in  
        std_logic_vector (1  
  
        downto 0);
```

```
therm_output : out  
std_logic_vector (6  
downto 0)  
    );  
end bin2therm6bit;
```

```
architecture  
Behavioral of  
bin2therm6bit is  
begin
```

```
    process  
(binary_input)  
    begin
```

```
label1 : case  
binary_input is
```

```
    when "000" =>  
therm_output <=  
"0000000";
```

```
    when "001" =>  
  
therm_output <=
```

```
"0000001";
```

```
    when "010" =>
```

```
therm_output <=
```

```
"0000011";
```

```
    when "011" =>
```

```
therm_output <=
```

```
"0000111";
```

```
    when "100" =>
```

```
therm_output <=
```

```
"0001111";
```

```
    when "101" =>
```

```
therm_output <=
```

```
"0011111";
```

```
    when "110" =>
```

```
therm_output <=
```

```
"0111111";
```

```
    when "111" =>
```

```
therm_output <=
```

```
"111111";  
  
        when others =>  
            therm_output <=  
                "xxxxxxx";  
  
        end case;  
    end  
process;  
end Behavioral;
```

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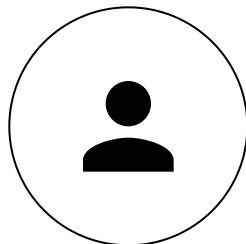
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