7. PROCEDURE

7.1 GENERAL CMOS065 TECHNOLOGY

7.1.1 STANDARD PROCESS

Standard processes:

- CMOS065_LP: Targeted as Low Power to serve battery operated and wireless applications. It is a single IO oxide + single core oxide dual Vt process. It gives access to standard Vt transistors (SVT), high Vt transistors (HVT), high density SRAM using LP core oxide, and IO transistors (one of: 1.8V or 2.5V) using IO oxide. It does not give access to GP devices (§7.1.5). It uses Copper metallization with 7 metal levels (5 thin + 2 thick) and low-K dielectrics.

- CMOS065_LPGP: Targeted as Low Power with access to General Purpose devices. It is a single IO oxide + dual core oxide dual Vt process. It gives access to standard Vt transistors (SVT), high Vt transistors (HVT), and high density SRAM in the LP core oxide. Additionally it gives access to standard Vt transistors (SVT), high Vt transistors (HVT), and high density SRAM in the GP oxide. It gives access to IO transistors (one of: 1.8V or 2.5V) using IO oxide (§7.1.5). It uses Copper metallization with 7 metal levels (5 thin + 2 thick) and low-K dielectrics.

The metallization choices are (see §7.3.3):
- 7M-4X-0Y-2Z (fully supported standard process)
- 6M-4X-0Y-1Z, 7M-4X-1Y-1Z~~, 8M-5X-0Y-2Z, 9M-6X-0Y-2Z, 9M-4X-2Y-2Z~~ (fully supported options)
- others feasible but currently not supported

where mM-xX-yY-zZ refers to a process with a total of m metal layers out of which x are fine pitch, y are intermediate pitch and z are thick metals (§7.3.3). Note that the product designs must contain markers to identify the metallization choice (§8.1).

7.1.2 TECHNOLOGY OPTIONS

For the standard process, the following add-on options are available:

- L (Low Vt): CMOS065~~_LP~~ + Low Vt transistor (LVT) option ~~[low Vt of CMOS065_LP only]~~.
- N (Native Vt): CMOS065 + Native Vt transistor (NT_N) option.
- F (Fuse): CMOS065 + Copper metal fuse option.

In Chapter 8 this document includes the description of process options which are specific to the Crolles fab:

- A (Analog): CMOS065 + HIPO resistor option.
- D (DRAM): CMOS065 + Embedded DRAM option.
- R (RF): CMOS065 + MIM Capacitor + Inductor option.
- B (Flip-Chip Bump): CMOS065 + Flip-Chip Bump option.

Thin Oxide MOSFETs						
Device	**Name in DK**	**Fully Supported**	**Specific Applic.**	**Process Option**	**Natural**	**Comment**
GP Core Oxide MOSFETs (LPGP process)						
GP NMOS 1.3nm 1.0V, SVT	nsvtgp	x				
GP PMOS 1.3nm 1.0V, SVT	psvtgp	x				
GP NMOS 1.3nm 1.0V, HVT	nhvtgp	x				
GP PMOS 1.3nm 1.0V, HVT	phvtgp	x				
GP NMOS 1.3nm 1.0V, SVT unsilicided	nsvtgprpo		x			IO application; model same as silicided device + series resistance
GP PMOS 1.3nm 1.0V, SVT unsilicided	psvtgprpo		x			IO application; model same as silicided device + series resistance
GP NMOS 1.3nm 1.0V, HVT unsilicided	nhvtgprpo		x			IO application; model same as silicided device + series resistance
GP PMOS 1.3nm 1.0V, HVT unsilicided	phvgptrpo		x			IO application; model same as silicided device + series resistance
LP Core Oxide MOSFETs (LP and LPGP processes)						
LP NMOS 1.8nm 1.2V, SVT	nsvtlp	x				
LP PMOS 1.8nm 1.2V, SVT	psvtlp	x				
LP NMOS 1.8nm 1.2V, HVT	nhvtlp	x				
LP PMOS 1.8nm 1.2V, HVT	phvtlp	x				
LP NMOS 1.8nm 1.2V, LVT	nlvtlp			x		~~option offered only for LP standalone process~~
LP PMOS 1.8nm 1.2V, LVT	plvtlp			x		~~option offered only for LP standalone process~~
LP NMOS 1.8nm 1.2V, Native Vt	nnvtlp			x		
LP NMOS 1.8nm 1.2V, SVT unsilicided	nsvtlprpo		x			IO application; model same as silicided device + series resistance
LP PMOS 1.8nm 1.2V, SVT unsilicided	psvtlprpo		x			IO application; model same as silicided device + series resistance
LP NMOS 1.8nm 1.2V, HVT unsilicided	nhvtlprpo		x			IO application; model same as silicided device + series resistance
LP PMOS 1.8nm 1.2V, HVT unsilicided	phvtlprpo		x			IO application; model same as silicided device + series resistance
LP SRAM Bitcell MOSFETs (LP and LPGP processes)						
LP NMOS 1.8nm 1.2V, SRAM	nsvtlppgsp nsvtlppgdp nsvtlppdsp nsvtlppddp nhvtlppgsp nhvtlppgdp nhvtlppdsp nhvtlppddp		x			SRAM specific
LP PMOS 1.8nm 1.2V, SRAM	psvtlppusp psvtlppudp phvtlppusp phvtlppudp		x			SRAM specific

Dummy Pattern CAD Levels		Dummy_O Pattern CAD Levels	
Name	**Number;datatype**	**Name**	**Number;datatype**
OD,dummy	6;1		
PO,dummy	17;1		
M1,dummy	31;1	M1;dummy_O	31;7
M2X,dummy	32;1	M2X;dummy_O	32;7
M3X,dummy	33;1	M3X;dummy_O	33;7
M4X,dummy	34;1	M4X;dummy_O	34;7
M5X,dummy	35;1	M5X;dummy_O	35;7
M6X,dummy	36;1	M6X;dummy_O	36;7
M6Y,dummy	36;21	M6Y;dummy_O	36;27
M6Z,dummy	36;41		
M7X,dummy	37;1	M7X;dummy_O	37;7
M7Y,dummy	37;21	M7Y;dummy_O	37;27
M7Z,dummy	37;41		
M8Z,dummy	38;41		
M9Z,dummy	39;41		
AP,dummy	74;1		
BOTMIM,dummy	88;1		
MKTOPMIM,dummy	77;1		

Table of key devices with associated CAD Layers

Transistors										
CAD level Name	**NMOS**					**PMOS**				
	LVT[a]	**SVT**	**HVT**	**SVT18**	**SVT25**	**LVT[a]**	**SVT**	**HVT**	**SVT18**	**SVT25**
OD	x	x	x	x	x	x	x	x	x	x
PO	x	x	x	x	x	x	x	x	x	x
NW						x	x	x	x	x
VTH_N			x							
VTH_P								x		
VTL_N	x									
VTL_P						x				
NP	x	x	x	x	x					
PP						x	x	x	x	x
OD25					x					x
OD18				x					x	

a.only available in LP

Resistors									
CAD Level Name	**Unsilicided**					**Silicided**			
	N+ PO	**P+ PO**	**N+ OD**	**P+ OD**	**HIPO**	**N+ PO**	**P+ PO**	**N+ OD**	**P+ OD**
OD			x	x				x	x
PO	x	x				x	x		
NW	x	x		x	x	x	x		x
NP	x		x			x		x	
PP		x		x	x		x		x
RPO	x	x	x	x	x				
RH	x	x	x	x		x	x	x	x
HRI					x				

7.2.3 MASK TABLE

The masks are generated with logical operations done on CAD layers. These logical operations (CAD2MASK RADCS # R014280ADCS # 7767771) are performed during the data preparation for mask processing.

Mask Level Name	Mask Number [a]	Field	Derived from CAD Layer	Standard Process, (Option)
ACTIVE	2	Clear	OD	all
NISO	24	Dark	DNW	all
NWELL	1	Dark	NW, OD25	all
NWELLGO2	84	Dark	NW, OD25	all OD25
ADSHVTP	98	Dark	VTL_P, NW, OD25, OD18	all OD18, (~~LP~~Low Vt)
ADHVTP	83	Dark	VTH_P	all
PWELL	8	Clear	NW, OD25, NT_N, PW;blk	all
PWELLGO2	85	Dark	NW, OD25, NT_N, PW;blk	all OD25
ADSHVTN	86	Clear	VTL_N, NW, OD25, OD18	all OD18, (~~LP~~Low Vt)
ADHVTN	82	Dark	VTH_N	all
VTNCELL	94	Dark	SRM, NW	all
VTPCELL [b]	102	Dark	SRM, NW	all
GO2	6	Clear	OD25, OD18	all
GOX_LP	105	Dark	DCO, OD25, OD18	LPGP
POLY	13	Clear	PO, OD, OD25, OD18, DCO, RH, HRI, POFUSE	all
PPPREDOP	70 [b]	Dark	NW, RH, VAR	all
NLDD_LP	45	Dark	NP, NW, OD25, OD18, RH, HRI, POFUSE, DCO, BJTDMY, VAR, MKR,NOLDD	all
PLDD_LP	46	Dark	PP, NW, OD25, OD18, RH, HRI, POFUSE, DCO, BJTDMY, VAR, MKR,NOLDD	all
NLDD_GP	47	Dark	see NLDD_LP	LPGP
PLDD_GP	48	Dark	see PLLD_LP	LPGP
NLDDGO2	76	Dark	see NLDD_LP	all
PLDDGO2	77	Dark	see PLLD_LP	all
NPLUS	16	Dark	NP	all
PPLUS	17	Dark	PP	all
PRESIST	42	Dark	HRI	all, (HIPO)
SIPROT	18	Clear	RPO	all
CONTACT	19	Dark	CO, CO,LIL	all
METAL1	23	Dark	M1	all
VIAX1	148	Dark	VIA1X	all
METALX1	134	Dark	M2X	all
VIAX2	149	Dark	VIA2X	all
METALX2	135	Dark	M3X	all
VIAX3	150	Dark	VIA3X	all
METALX3	136	Dark	M4X	all
VIAX4	151	Dark	VIA4X	all
METALX4	137	Dark	M5X	all
VIAX5	152	Dark	VIA5X	all, 5 or more MiX metals
METALX5	138	Dark	M6X	all, 5 or more MiX metals
VIAX6	153	Dark	VIA6X	all, 6 or more MiX metals
METALX6	139	Dark	M7X	all, 6 or more MiX metals
VIAY1	156	Dark	VIA5Y, VIA6Y [c]	all, 1 or more MiY metals
METALY1	142	Dark	M6Y, M7Y [c]	all, 1 or more MiY metals
VIAY2	157	Dark	VIA6Y [c]	all, 2 or more MiY metals
METALY2	143	Dark	M7Y [c]	all, 2 or more MiY metals
VIAZ1	159	Dark	VIA5Z, VIA6Z, VIA7Z, VIA8Z [c]	all

	Process Feature	Opt	Devices	CAD Layers	Masks
Process Options	Low Vt ~~(LP flow only)~~	-L-	nlvtlp, plvtlp, dnlvtlp, dplvtlp	VTL_N, VTL_P	ADSHVTN, ADSHVTP
	GP High Density SRAM in GP oxide (LPGP flow only)		nsvtlppgsp, nsvtlppgdp, nsvtlppdsp, nsvtlppddp, nhvtlppgsp, nhvtlppgdp, nhvtlppdsp, nhvtlppddp, psvtlppusp, psvtlppudp, phvtlppusp, phvtlppudp	SRM .and. DCO	VTPCELL
	Other Metallization Options (with My or more than 7 metals)		rmy, cfrm1m5shx, cfrm1m5shy, cmxmy, cmymy, cmymz [a]	see §7.3.3	-
	Native-Vt	-N-	nnvtlp, dnnvtlp	NT_N	-
			nnvt18, dnnvt18	NT_N (OD18)	
			nnvt25, dnnvt25	NT_N (OD25)	
	HIPO	-A-	rhiporpo	HRI	PRESIST
	Copper Laser Fuse	-F-	rmz	FW	LASEROPEN
	EDRAM	-D-	nsvt25dram, nlvt25dram, dnsvt25dram, ce1e2	MKR,EDRAM, CELLIMP, CO,LIL, ELEC1, ELEC2, CO,C2	PWDRAM, CELLIMP, ELEC1, ELEC2, CTDRAM
	MIM	-R-	cmimmk	BOTMIM, MKTOPMIM	BOTMIM, MKTOPMIM
	Flip-Chip	-B-		MKR,fc	

a.resistors and capacitance models rely upon the chosen option metallization.