Assignment 5: 6-bit Segmented Current-Mode DAC Simulation and Design

Objectives

- To simulate the operation and the static and dynamic non-idealities of a CMOS Current-Mode DAC using a state-of-the art design kit and 65-nm CMOS technology.
- To design an 6-bit segmented Current-Mode DAC at transistor level using Cadence Analog Artist.

1. Preparation:

Study Chapters 16 in the textbook, the associated course slides, and read reference [1].

You will use Cadence Analog Artist with the cmos65nm design kit, the *s v t* GP MOSFETs with 60nm gate length and finger width, W_f, of 1um for the switch, the 2.5V MOSFETs with 0.25um gate length and 4um finger width for the p-MOSFET current sources, and the unsalicided p-poly resistors from the *cmos065* library in all simulations. Use a unit resistor width W between 1 and 2 um. The supply voltage is V_{DD}= 2.5 V. V_{bias} = 0.5 V. The maximum voltage on any of the GP MOSFETs should not exceed 1.2 V. V_{REF}= 256 mV.

2. 6-bit binary-weighted current-mode DAC (10 points)

Consider the positive supply, single-ended CMOS current-mode DAC in *Fig*.1. The op-amp is ideal, from the *ahdlLib,* with a gain of 100, infinite bandwidth, and infinite linearity. Add individual *vpulse* sources to drive each switch. The *vpulse* sources have V_{low} = 0.1 V, V_{high} = 0.9 V, 50% duty cycle, a DC level of 0.5 V, and 5ps rise and fall times. The full scale value of V_{out} is 256 mV.

a) Find the value, width and length of the resistor R_{ref}, the number of fingers of the 2.5V MOSFET current sources and of the GP MOSFET so that the GP p-MOSFET switches are biased at a current density of at most 0.05 mA/um when the gate voltage at $d_i = V_{bias} =$ 0.5 V. The DC voltage at the drains of the current sources should be between 1.1 and 1.3V. Design the 50Ohm load resistor out of the same unit used for R_{ref}. Provide hand-design equations and the component dimensions L, W_f, N_f for all MOSFETs and W, L and number of units for all resistors. **(5 points).**

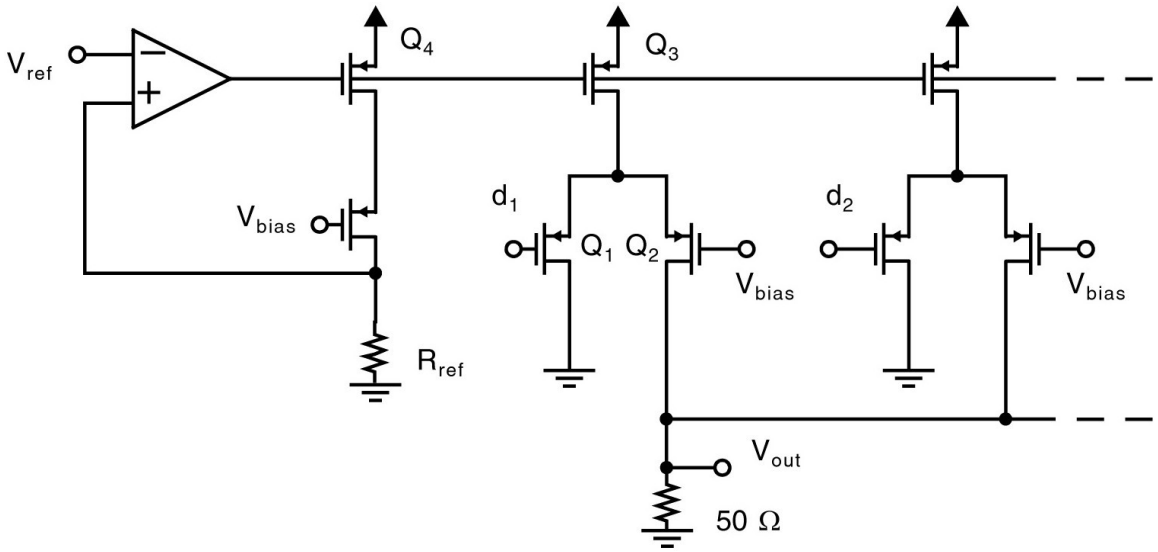

Fig.1 CMOS Current-Mode DAC schematic.

b) Simulate the INL and DNL at 65 C in the nominal process corner using 50 statistical simulations for resistors and transistors. The setup for Monte-Carlo statistical simulation including both process variation and local device mismatch is shown in Fig. 2. **(2 points**).

c) Simulate and plot the ***SDR*** and ***ENOB*** as a function of frequency when generating a full scale output sinusoid at 100 MHz, 1.1 GHz, 2.1 GHz, and 4.9 GHz at a sampling rate of 10 GS/s and 15 GS/s. What is the effective resolution bandwidth at each sampling frequency? You will need the ideal 8-bit ADC from the *ahdlLib* to generate the binary codes for the sinusoidal signals and activate only the first 6 MSBs (**3 points**).

$$N_{eff} = \frac{SNDR - 1.76\ dB}{6.02}$$

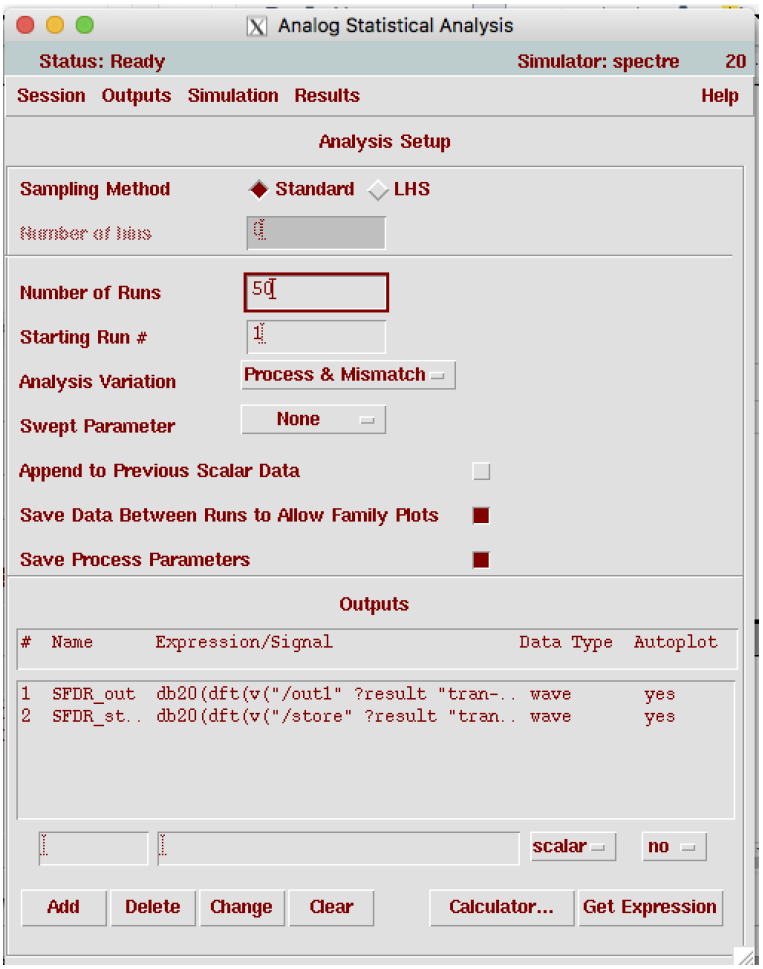

Fig.2 Setup for Monte-Carlo mismatch and process variation simulations.

3. 6-bit Segmented Current-Mode DAC (10 points)

a) Design a fully differential, segmented version of the DAC in **2)** above using the target specification in **Table 1**. Provide the full schematic, the hand design equations, the DC operating points, and the dimensions of all transistors and resistors, as above. You may use reference [1], which was implemented in the same 65nm CMOS process, as inspiration **(5 points).**

b) Simulate the static INL and DNL at 65 C in the nominal process corner using 50 statistical simulations for resistors and transistors. Explain why and how has it changed compared to that of the binary-weighted DAC in **2)** above? **(2 points**).

c) Simulate and plot the ***SDR*** and ***ENOB*** as a function of frequency when generating a full scale output sinusoid at 100 MHz, 1.1 GHz, 2.1 GHz, 3.1 GHz, $f_S/3$ +100 MHz, and $f_S/2$ -100 MHz. What is the effective resolution bandwidth? (**3 points**).

Table 1

Surname starts with	Segmented MSBs	V_{out} full scale	Sampling rate, f_S
A, B, C, D	2	400	12 GS/s
E, F, G, H,	4	350	15 GS/s
I, J, K, L	3	200	18 GS/s
M, N, O, P	2	250	18 GS/s
Q, R, S, T	3	200	15 GS/s
U,V,X,Y,Z	4	250	15 GS/s

[1] Y. Greshishchev et al., IEEE ISSCC, Feb. 2011.