HVT_GP MODELS (NHVTGP, PHVTGP)

1. CONDITIONS OF EXTRACTION

- Maturity: Preliminary
- Model parameters extraction based on lot : -
- Geometrical extraction domain:
  - Drawn gate length : 0.18 ≥ L ≥ 0.06 µm
  - Drawn transistor width : 10 ≥ W ≥ 0.12 µm
- Temperature extraction domain: -40 ˚C to 150 ˚C
- Bias extraction domain:
  - Gate bias: 0 ≤ |VGS| ≤ 1.1 V (VDD + 10%)
  - Drain bias: 0 ≤ |VDS| ≤ 1.1 V (VDD + 10%)
  - Bulk bias: 0 ≤ |VBS| ≤ 1.1 V (VDD + 10%)

2. CONDITIONS OF SIMULATION

- Temperature: 25 ˚C
- Currents:

  IDLIN = Ids at Vgs = 1.0 V, Vds = 50 mV and Vbs = 0 V

  ION = Ids at Vgs = 1.0 V, Vds = 1.0 V and Vbs = 0 V

  IOFF = Ids at Vgs = 0 V, Vds = 1.0 V and Vbs = 0 V

  IG_ON = Igs at Vgs = 1.0 V and Vd= Vs = Vb = 0 V

  IG_OFF = Igs at Vgs =Vbs = 0 V and Vds = 1.0 V
- Threshold voltage in linear and saturation regime

  VTLIN is Vgs value at Vds = 50 mV, Vbs = 0 V and Ids= 40*W/L nA.

  VTSAT is Vgs value at Vds = 1.0 V, Vbs = 0 V and Ids= 40*W/L nA.
- Current derivatives:

$$Gm = \frac{\partial}{\partial V_{gs}} Ids$$ at Vgs = VTLIN + 0.2 V, Vds = 0.5 V and Vbs = 0 V

$$Gd = \frac{\partial}{\partial V_{ds}} Ids$$ at Vgs = VTLIN + 0.2 V, Vds = 0.5 V and Vbs = 0 V

Analog gain = Gm/Gd

- Gate Capacitances:

  CGGINV = CGG at Vgs = 1.0 V, Vds = 0 V and Vbs = 0 V

  CGD_0V = CGD at Vgs = 0 V, Vds = 0 V and Vbs = 0 V

  $$CGGMEAN = \frac{1}{VDD} \cdot \int_{0}^{VDD} CGG \times dVgs$$ with VDD = 1.0 V and Vbs = 0 V

  TAU = CGGMEAN*VDD/ION

- Diode Capacitances:

  CBD OFF = CBD at Vgs = 0 V, Vds = 1.0 V and Vbs = 0 V

  Note: the area and perimiters of source/drain junction diodes used for simulation are defined with the the minimum poly-to-active distance specified in the DRM.

- Transition frequency:

  FT = frequency for which the small signal current gain H_{21} is 0 dB (i.e. $\left|\frac{I_d}{I_g}\right|$ = 0 dB).

3. MAIN ELECTRICAL CHARACTERISTICS OF NMOS HVT_GP TRANSISTORS

PARAMETERS	HVTGP_TT	HVTGP_SS	HVTGP_FF	units
N-channel transistors (nhvtgp)				
VTLIN W=1/L=0.18	386	412	360	mV
IDLIN W=1/L=0.18	3.75e-05	3.34e-05	4.19e-05	A
VTSAT W=1/L=0.18	364	390	338	mV
ION W=1/L=0.18	1.78e-04	1.51e-04	2.08e-04	A
VTLIN W=1/L=0.06	350	400	295	mV
IDLIN W=1/L=0.06	1.01e-04	8.60e-05	1.18e-04	A
VTSAT W=1/L=0.06	211	276	137	mV
ION W=1/L=0.06	6.33e-04	5.05e-04	7.88e-04	A
IOFF W=1/L=0.06	5.10e-09	1.23e-09	2.89e-08	A
IG_ON W=1/L=0.06	5.46e-09	2.73e-09	1.11e-08	A
IG_OFF W=1/L=0.06	1.06e-09	5.34e-10	2.12e-09	A
FT W=1/L=0.06	2.94e+11	2.65e+11	3.27e+11	Hz
CGGinv W=1/L=0.06	8.03e-16	8.42e-16	7.61e-16	F
CGGmean W=1/L=0.06	7.60e-16	7.78e-16	7.38e-16	F
CGD 0V W=1/L=0.06	3.37e-16	3.34e-16	3.40e-16	F
CBD OFF[a] W=1/L=0.06	5.14e-16	5.84e-16	4.42e-16	F
Tau W=1/L=0.06	1.2	1.5	0.9	ps
Gm W=1/L=0.06	4.47e-04	3.98e-04	5.07e-04	S
Gd W=1/L=0.06	7.20e-05	5.69e-05	9.30e-05	S
Gain W=1/L=0.06	6.20e+00	6.98e+00	5.46e+00	
VTLIN W=0.12/L=0.06	307	356	253	mV
IDLIN W=0.12/L=0.06	1.39e-05	1.16e-05	1.65e-05	A
VTSAT W=0.12/L=0.06	198	259	131	mV
ION W=0.12/L=0.06	8.89e-05	7.02e-05	1.12e-04	A
IOFF W=0.12/L=0.06	5.65e-10	1.41e-10	3.10e-09	A
FT W=0.12/L=0.06	2.30e+11	2.05e+11	2.61e+11	Hz

Table 1: Main electrical characteristics for NMOS

a. Value coresponding to the minimum poly-to-acvtive distance specified in the DRM

4. MAIN ELECTRICAL CHARACTERISTICS OF PMOS HVT_GP TRANSISTORS

PARAMETERS	HVTGP_TT	HVTGP_SS	HVTGP_FF	units
P-channel transistors (phvtgp)				
VTLIN W=1/L=0.18	315	343	287	mV
IDLIN W=1/L=0.18	1.67e-05	1.49e-05	1.87e-05	A
VTSAT W=1/L=0.18	285	314	257	mV
ION W=1/L=0.18	1.03e-04	8.78e-05	1.21e-04	A
VTLIN W=1/L=0.06	344	390	287	mV
IDLIN W=1/L=0.06	4.03e-05	3.42e-05	4.78e-05	A
VTSAT W=1/L=0.06	229	290	155	mV
ION W=1/L=0.06	3.00e-04	2.35e-04	3.90e-04	A
IOFF W=1/L=0.06	3.07e-09	8.74e-10	1.78e-08	A
IG_ON W=1/L=0.06	3.95e-09	1.88e-09	8.54e-09	A
IG_OFF W=1/L=0.06	1.04e-09	5.17e-10	2.10e-09	A
FT W=1/L=0.06	1.33e+11	1.09e+11	1.62e+11	Hz
CGGinv W=1/L=0.06	8.31e-16	9.03e-16	7.68e-16	F
CGGmean W=1/L=0.06	7.82e-16	8.22e-16	7.48e-16	F
CGD 0V W=1/L=0.06	3.26e-16	3.23e-16	3.28e-16	F
CBD OFF[a] W=1/L=0.06	5.19e-16	5.90e-16	4.45e-16	F
Tau W=1/L=0.06	2.6	3.5	1.9	ps
Gm W=1/L=0.06	2.54e-04	2.26e-04	2.87e-04	S
Gd W=1/L=0.06	3.22e-05	2.44e-05	4.40e-05	S
Gain W=1/L=0.06	7.90e+00	9.24e+00	6.52e+00	
VTLIN W=0.12/L=0.06	264	314	206	mV
IDLIN W=0.12/L=0.06	6.31e-06	5.26e-06	7.62e-06	A
VTSAT W=0.12/L=0.06	179	237	109	mV
ION W=0.12/L=0.06	5.00e-05	3.86e-05	6.57e-05	A
IOFF W=0.12/L=0.06	6.08e-10	1.62e-10	3.68e-09	A
FT W=0.12/L=0.06	9.89e+10	8.18e+10	1.13e+11	Hz

Table 2: Main electrical characteristics for PMOS

a. Value coresponding to the minimum poly-to-acvtive distance specified in the DRM

5. ION, IOFF, VT BEHAVIOR VERSUS GATE LENGTH AND CHANNEL WIDTH FOR NMOS HVT_GP TRANSISTORS

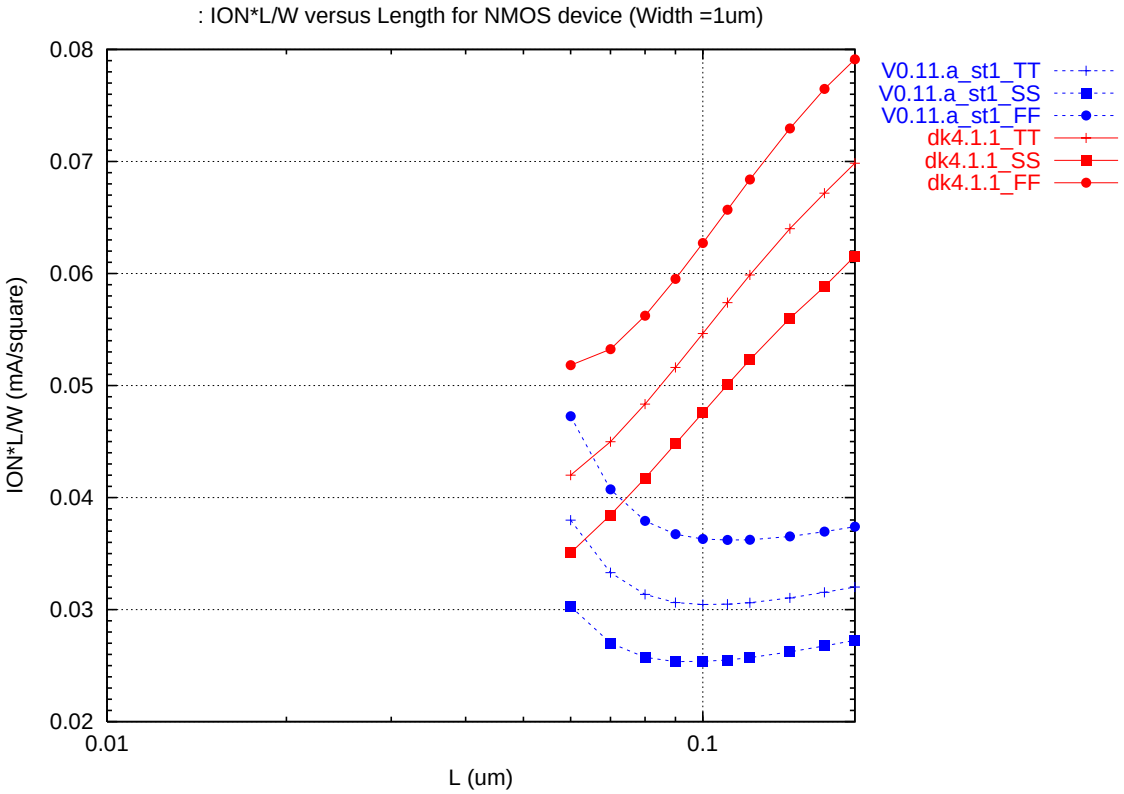

Figure 1 : ION/❑=ION*L/W versus drawn gate length for NMOS HVT_GP transistors (W = 1 µm)

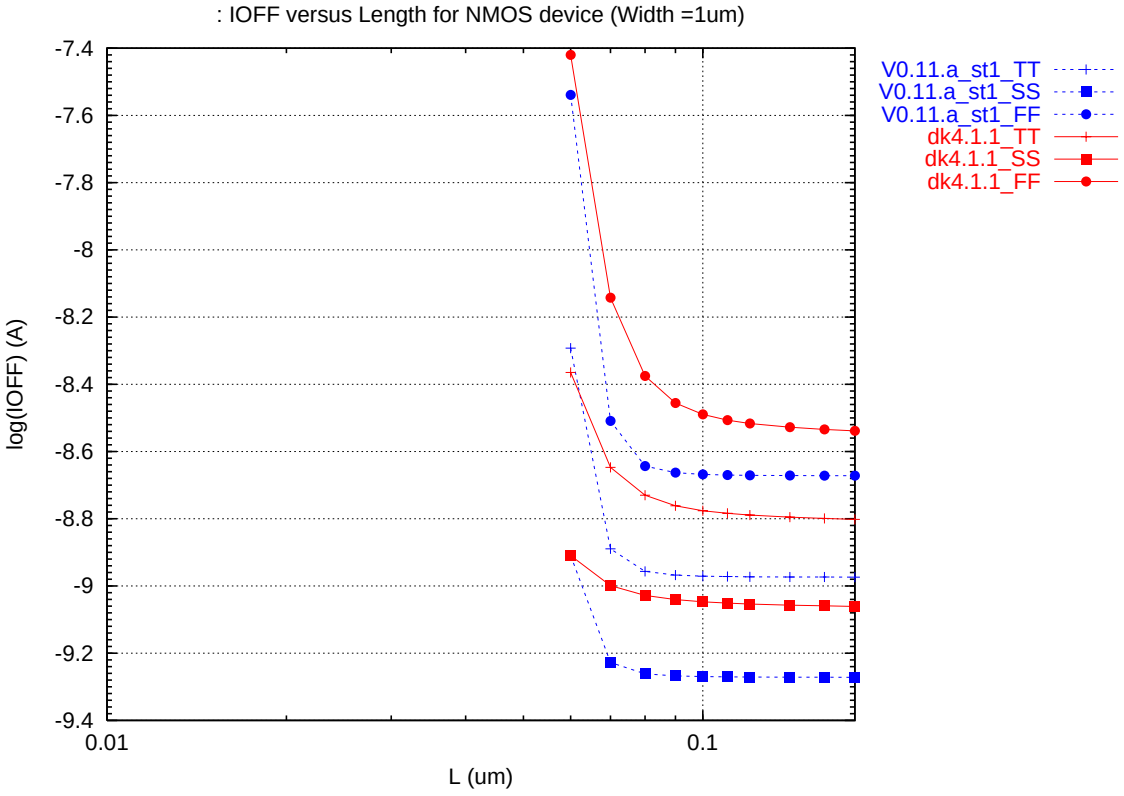

Figure 2 : IOFF versus drawn gate length for NMOS HVT_GP transistors (W = 1 µm)

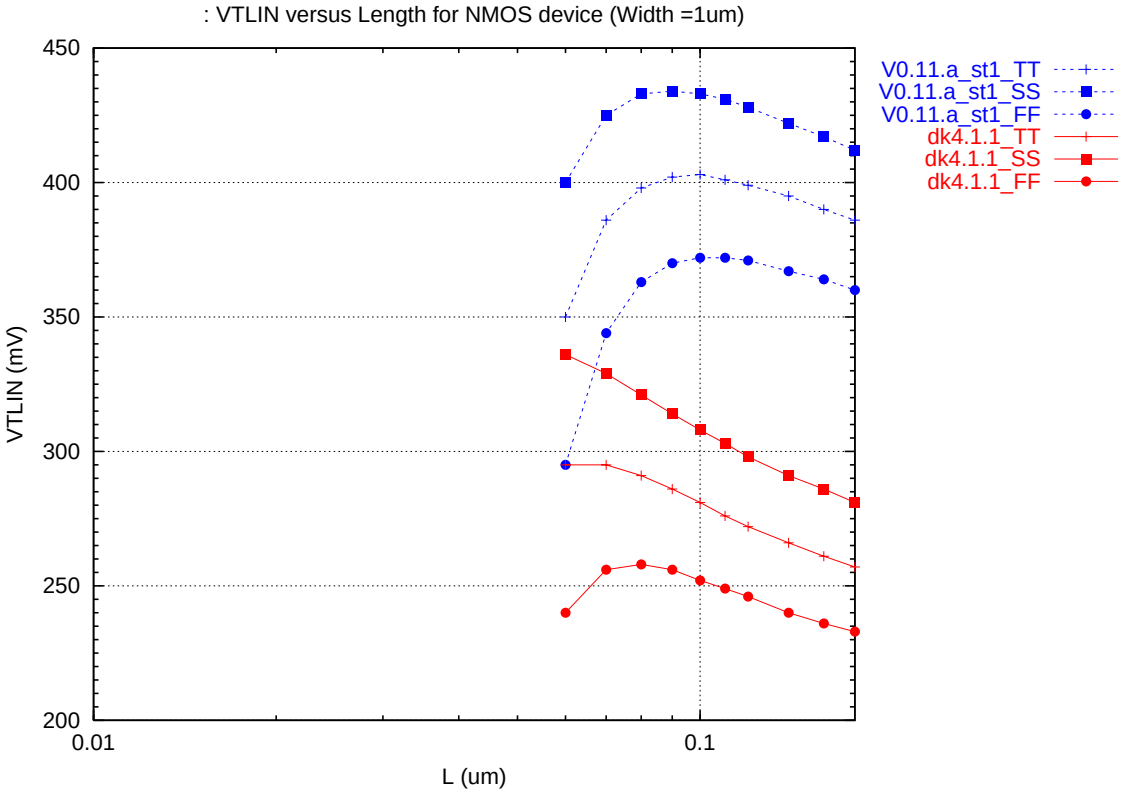

Figure 3 : Threshold voltage VTLIN versus drawn gate length for NMOS HVT_GP transistors (W = 1 µm)

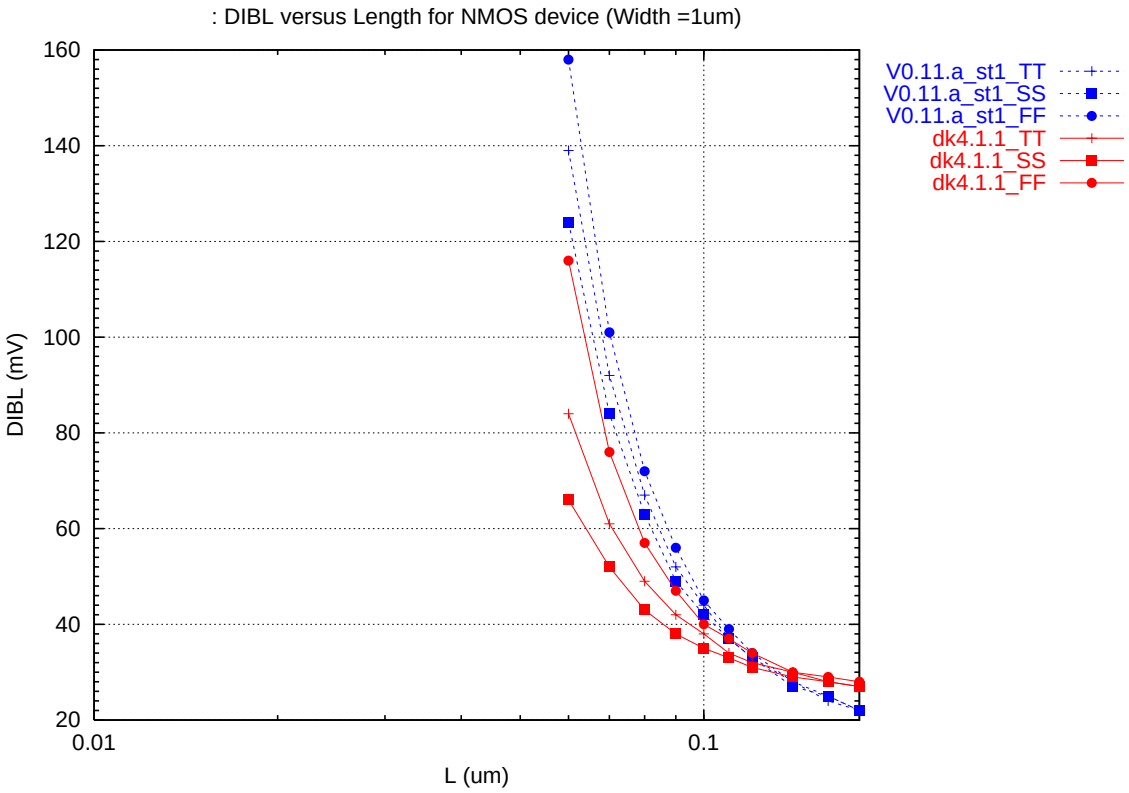

Figure 4 : DIBL= VTLIN-VTSAT versus drawn gate length for NMOS HVT_GP transistors (W = 1 µm)

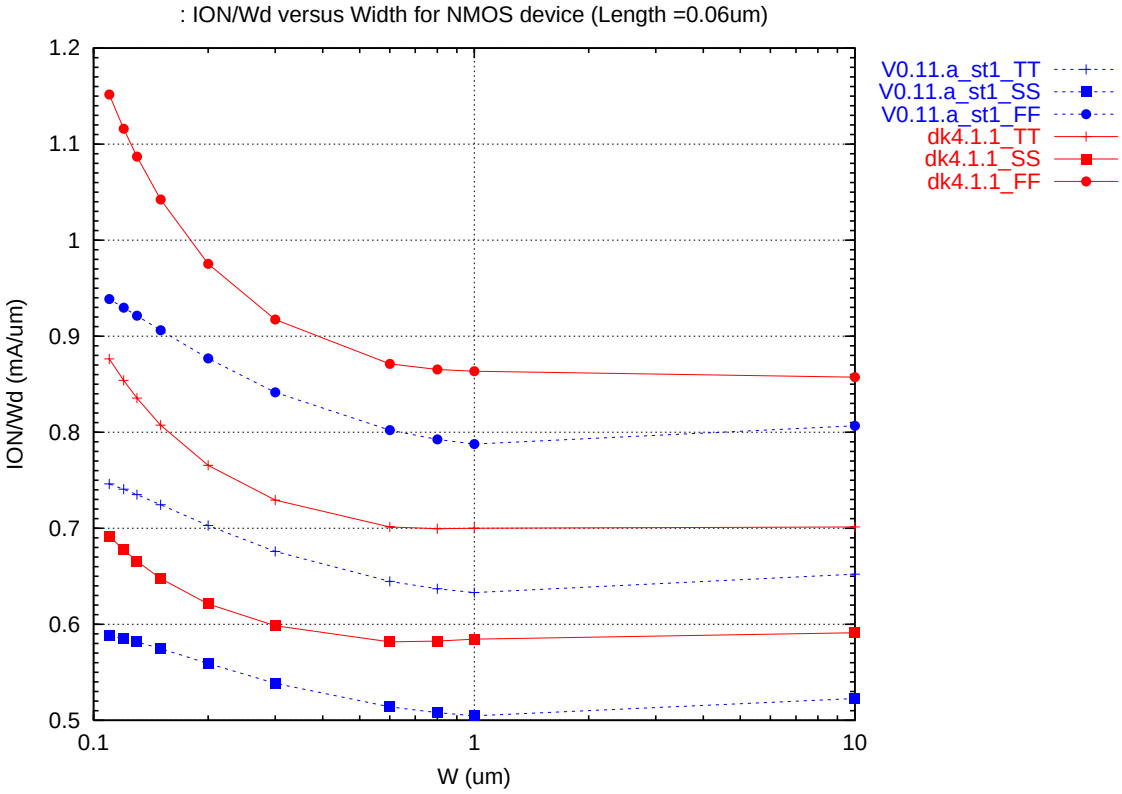

Figure 5 : ION versus drawn channel width for NMOS HVT_GP transistors (L = 0.06 µm)

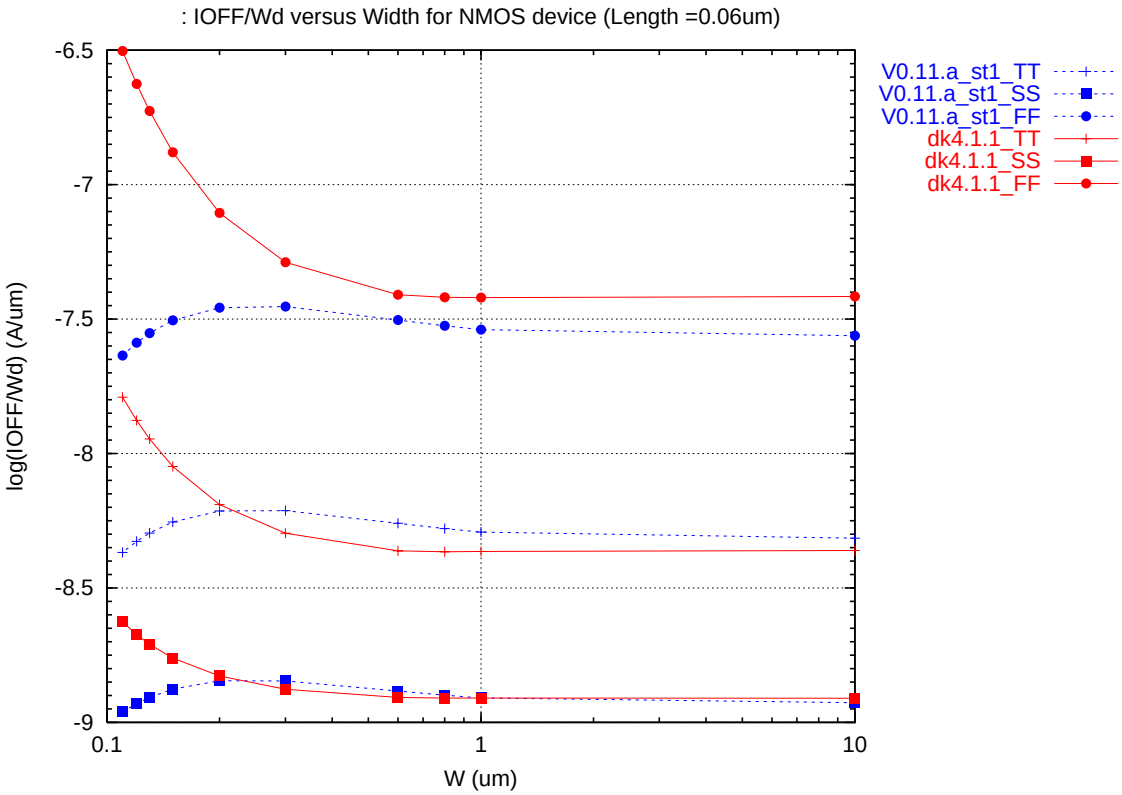

Figure 6 : IOFF versus drawn channel width for NMOS HVT_GP transistors (L = 0.06 µm)

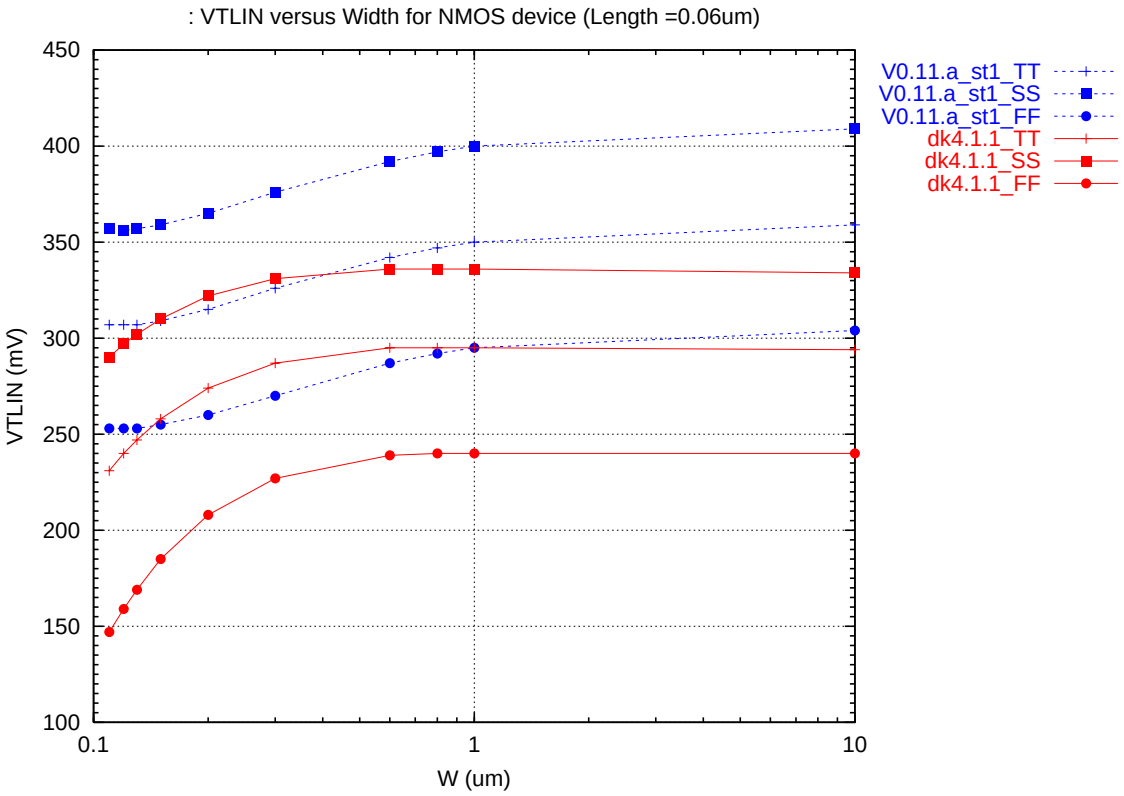

Figure 7 : Threshold voltage VTLIN versus drawn channel width for NMOS HVT_GP transistors (L = 0.06 µm)

6. ION, IOFF, VT BEHAVIOR VERSUS GATE LENGTH AND CHANNEL WIDTH FOR PMOS HVT_GP TRANSISTORS

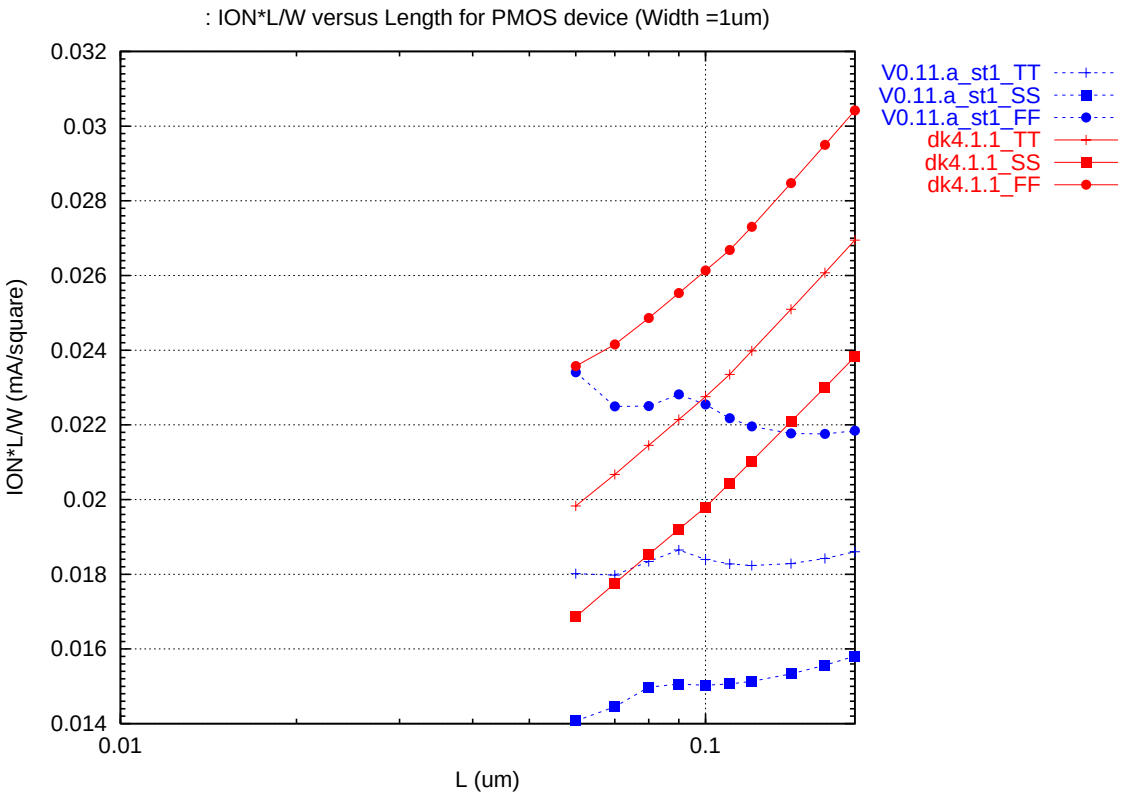

Figure 8 : ION versus drawn gate length for PMOS HVT_GP transistors (W = 1 µm)

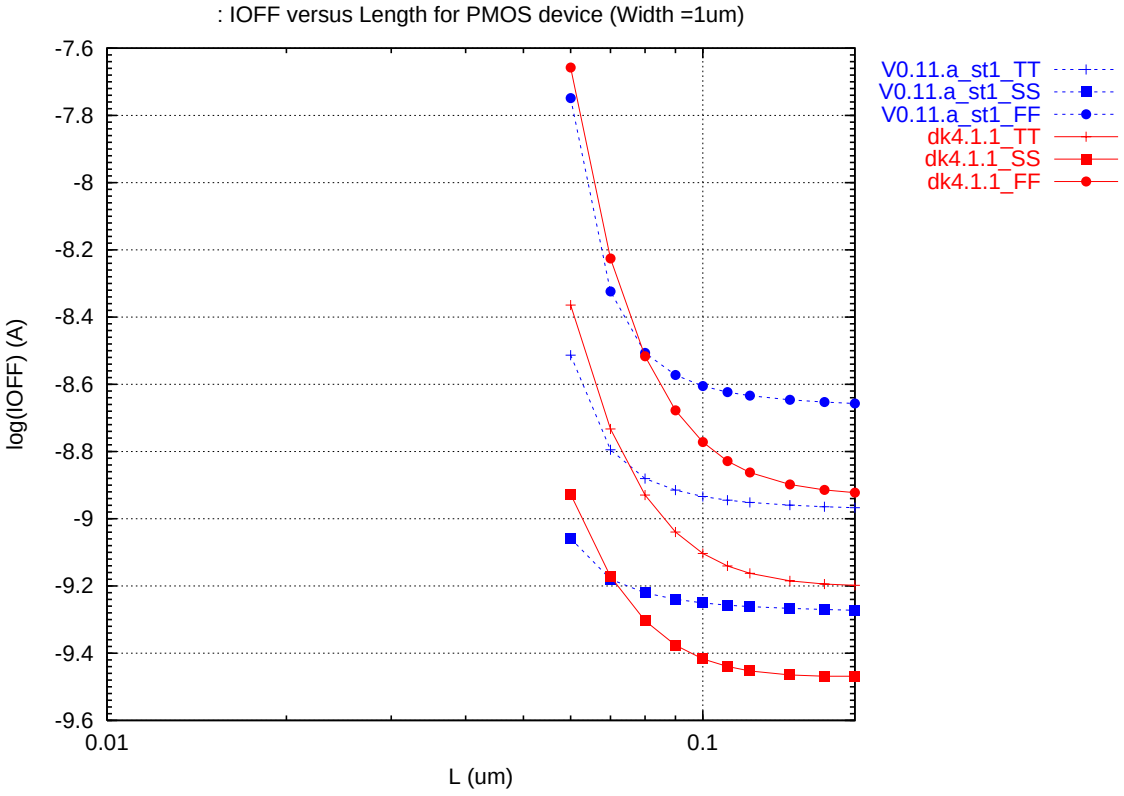

Figure 9 : IOFF versus drawn gate length for PMOS HVT_GP transistors (W = 1 µm)

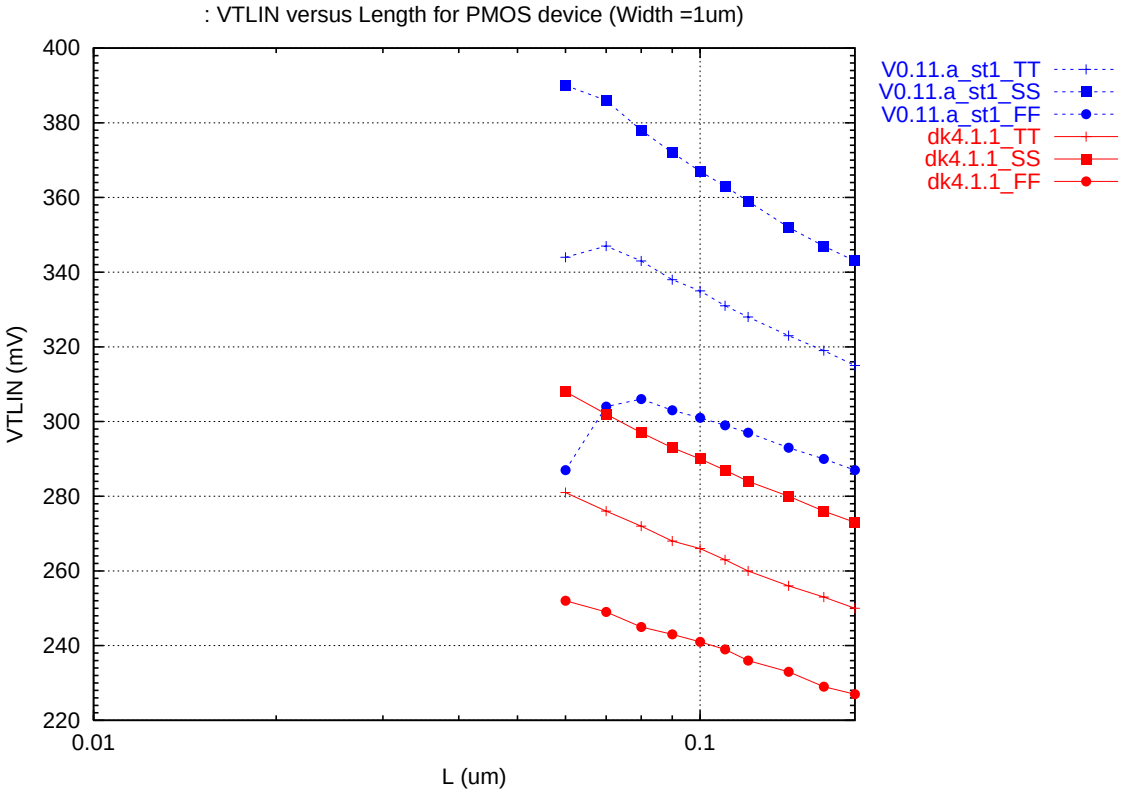

Figure 10 : Threshold voltage VTLIN versus drawn gate length for PMOS HVT_GP transistors (W = 1 µm)

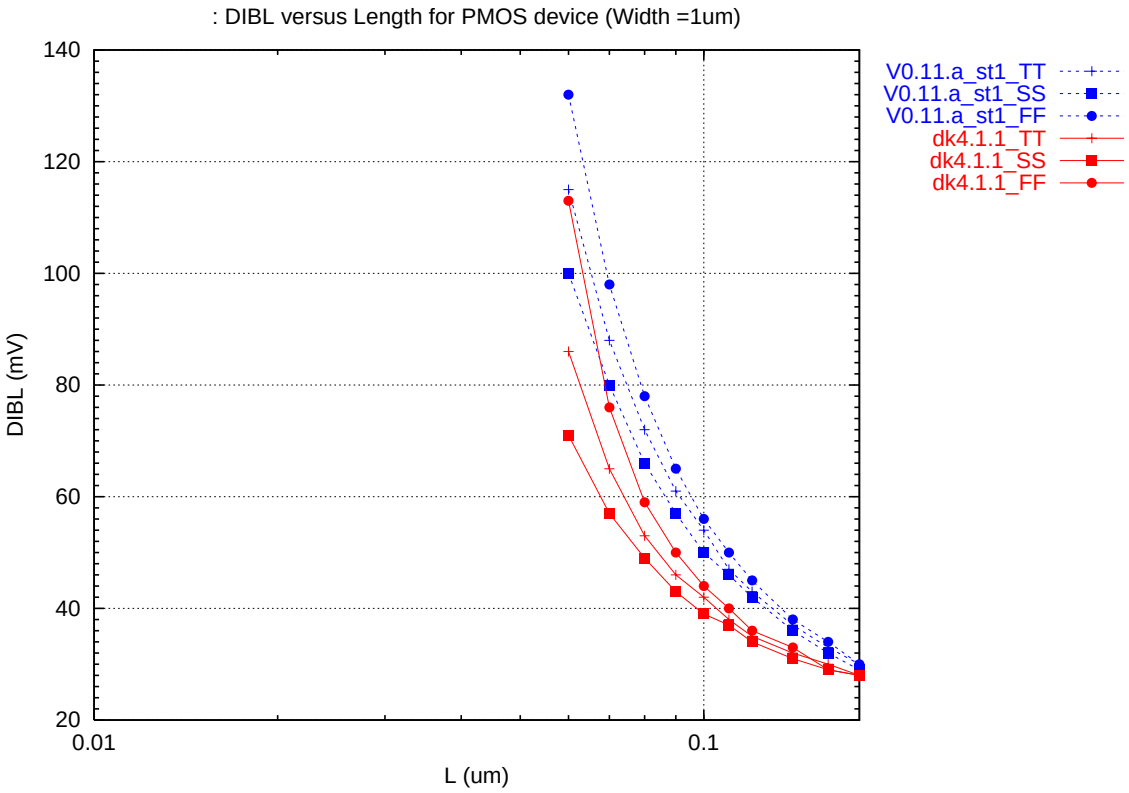

Figure 11 : DIBL= VTLIN-VTSAT versus drawn gate length for PMOS HVT_GP transistors (W = 1 µm)

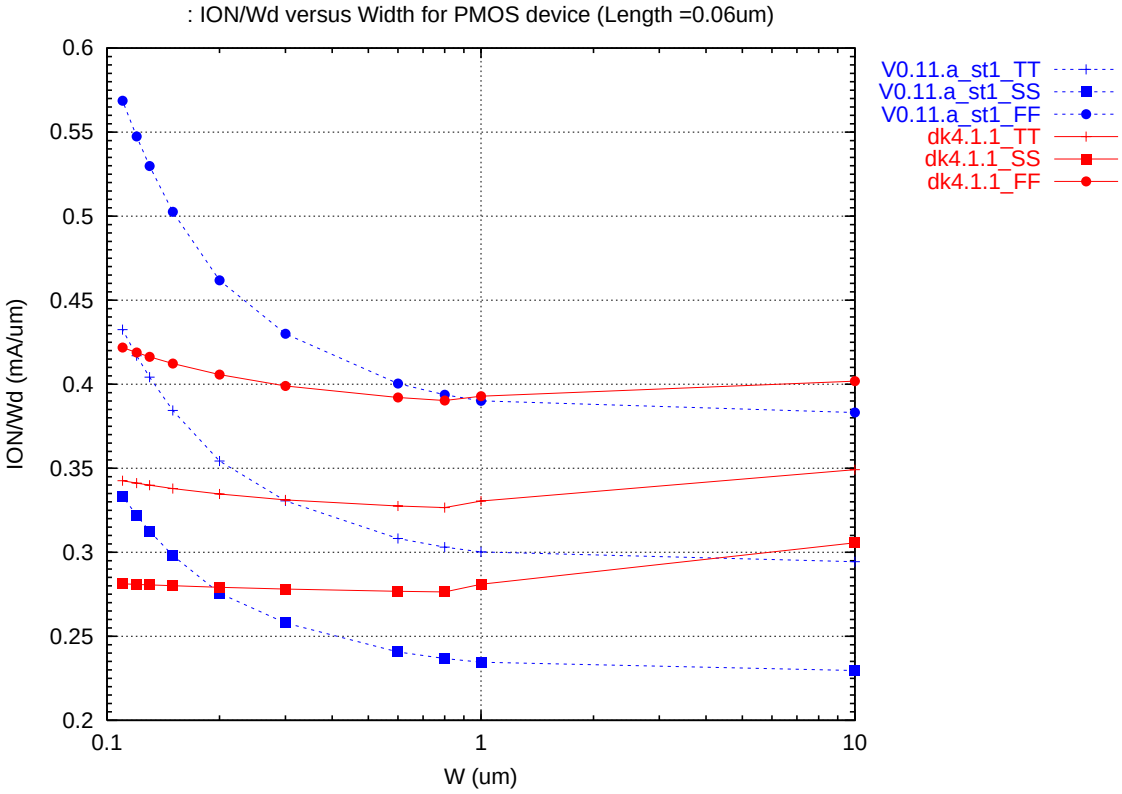

Figure 12 : ION versus drawn channel width for PMOS HVT_GP transistors (L = 0.06 µm)

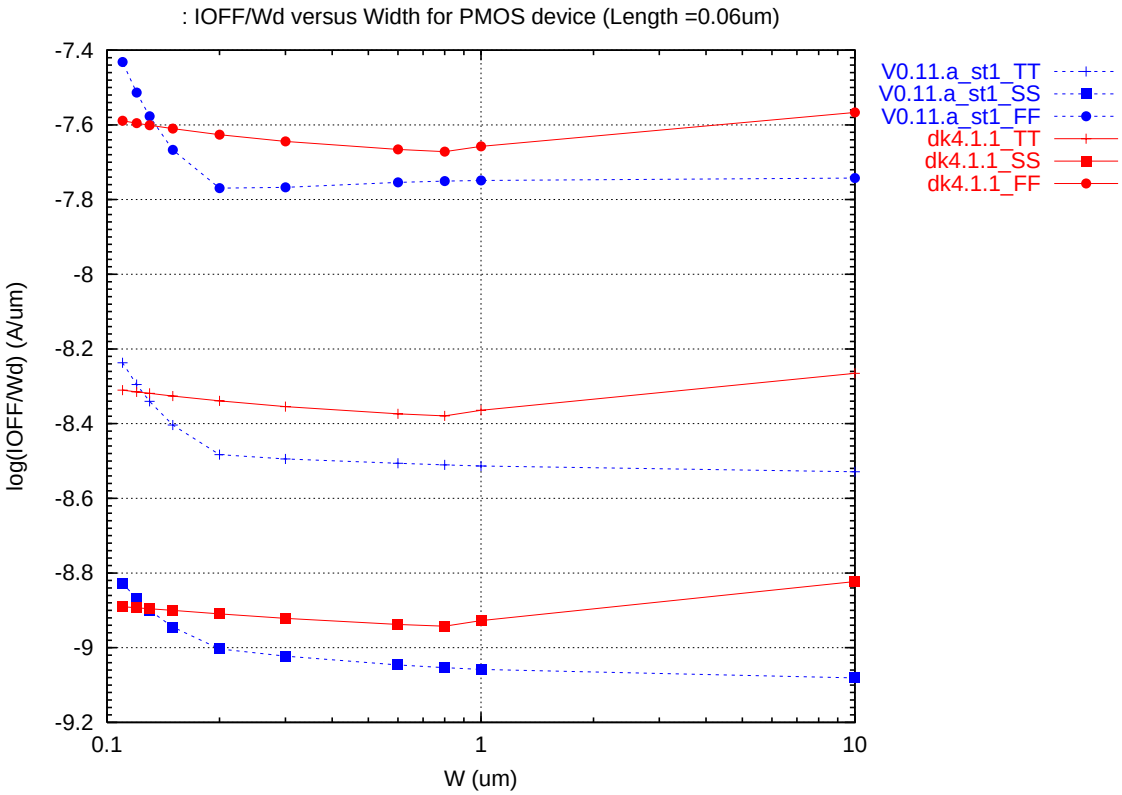

Figure 13 : IOFF versus drawn channel width for PMOS HVT_GP transistors (L = 0.06 µm)

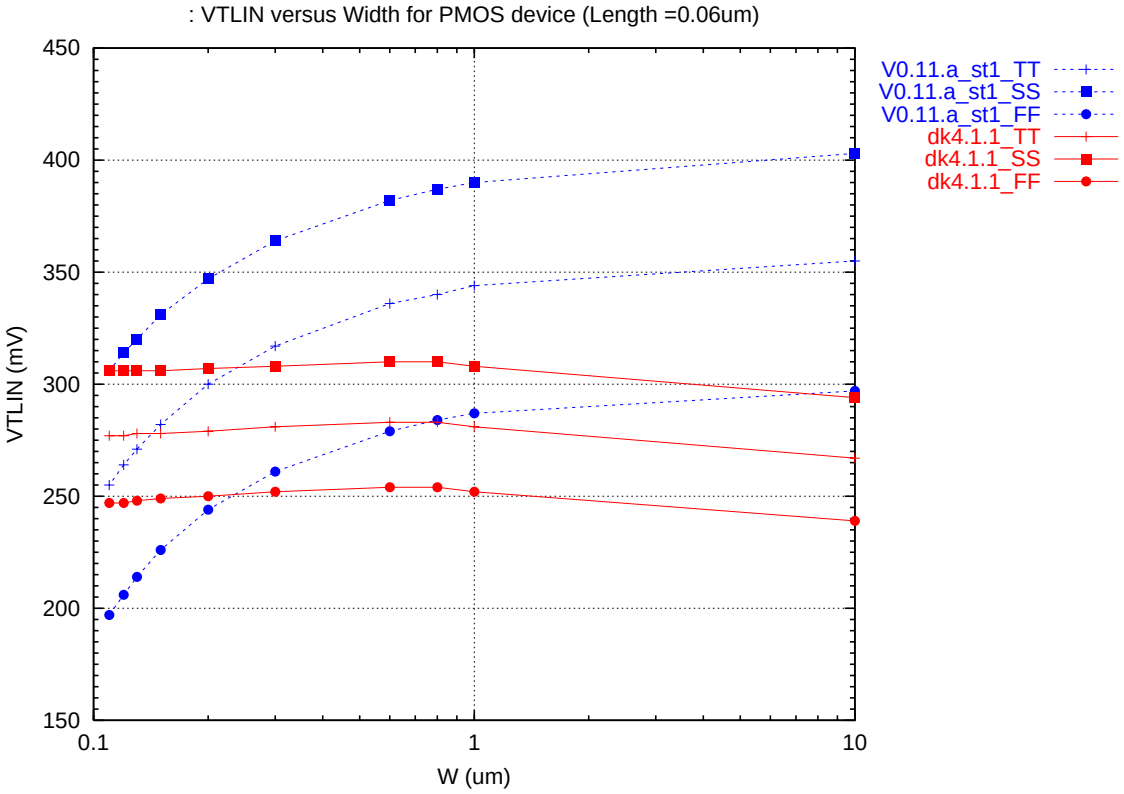

Figure 14 : Threshold voltage VTLIN versus drawn channel width for PMOS HVT_GP transistors (L = 0.06 µm)