# SVT_1V8 MODELS (NSVT18, PSVT18)

## 1. CONDITIONS OF EXTRACTION

- Maturity: Tentative
- Model parameters extraction based on lot : -
- Geometrical extraction domain:
  - Drawn gate length : 10.0 ≥ L ≥ 0.2 µm
  - Drawn transistor width : 10 ≥ W ≥ 0.4 µm
- Temperature extraction domain: -40 ˚C to 150 ˚C
- Bias extraction domain:
  - Gate bias: 0 ≤ |VGS| ≤ 1.98 V (VDD + 10%)
  - Drain bias: 0 ≤ |VDS| ≤ 1.98 V (VDD + 10%)
  - Bulk bias: 0 ≤ |VBS| ≤ 1.98 V (VDD + 10%)

## 2. CONDITIONS OF SIMULATION

- Temperature: 25 ˚C
- Currents:

  IDLIN = Ids at Vgs = 1.8 V, Vds = 100 mV and Vbs = 0 V

  ION = Ids at Vgs = 1.8 V, Vds = 1.8 V and Vbs = 0 V

  IOFF = Ids at Vgs = 0 V, Vds = 1.8 V and Vbs = 0 V

  IG_ON = Igs at Vgs = 1.8 V and Vd= Vs = Vb = 0 V

  IG_OFF = Igs at Vgs =Vbs = 0 V and Vds = 1.8 V
- Threshold voltage in linear and saturation regime

  VTLIN is Vgs value at Vds = 100 mV, Vbs = 0 V and Ids=100*W/L nA.

  VTSAT is Vgs value at Vds = 1.8 V, Vbs = 0 V and Ids=100*W/L nA.
- Current derivatives:

$$Gm = \frac{\partial}{\partial V_{gs}} Ids$$ at Vgs = VTLIN + 0.2 V, Vds = 0.9 V and Vbs = 0 V

$$Gd = \frac{\partial}{\partial V_{ds}} Ids$$ at Vgs = VTLIN + 0.2 V, Vds = 0.9 V and Vbs = 0 V

Analog gain = Gm/Gd

- Gate Capacitances:

  CGGINV = CGG at Vgs = 1.8 V, Vds = 0 V and Vbs = 0 V

  CGD_0V = CGD at Vgs = 0 V, Vds = 0 V and Vbs = 0 V

  $$CGGMEAN = \frac{1}{VDD} \cdot \int_{0}^{VDD} CGG \times dVgs$$ with VDD = 1.8 V and Vbs = 0 V

  TAU = CGGMEAN*VDD/ION

- Diode Capacitances:

  CBD OFF = CBD at Vgs = 0 V, Vds = 1.8 V and Vbs = 0 V

  **Note**: the area and perimiters of source/drain junction diodes used for simulation are defined with the the minimum poly-to-active distance specified in the DRM.

- Transition frequency:

  FT = frequency for which the small signal current gain $H_{21}$ is 0 dB (i.e. $\left|\frac{I_d}{I_g}\right|$ = 0 dB).

## 3. MAIN ELECTRICAL CHARACTERISTICS OF NMOS SVT_1V8 TRANSISTORS

| PARAMETERS | SVT18_TT | SVT18_SSA | SVT18_FFA | units |
|---|---|---|---|---|
| N-channel transistors (nsvt18) | | | | |
| VTLIN W=10/L=10.0 | 295 | 359 | 231 | mV |
| IDLIN W=10/L=10.0 | 3.43e-05 | 3.04e-05 | 3.85e-05 | A |
| VTSAT W=10/L=10.0 | 288 | 352 | 225 | mV |
| ION W=10/L=10.0 | 2.44e-04 | 2.06e-04 | 2.87e-04 | A |
| VTLIN W=10/L=0.2 | 424 | 499 | 349 | mV |
| IDLIN W=10/L=0.2 | 1.60e-03 | 1.31e-03 | 1.96e-03 | A |
| VTSAT W=10/L=0.2 | 388 | 462 | 312 | mV |
| ION W=10/L=0.2 | 6.79e-03 | 5.45e-03 | 8.43e-03 | A |
| IOFF W=10/L=0.2 | 2.80e-10 | 1.99e-11 | 3.40e-09 | A |
| IG_ON W=10/L=0.2 | 0.00e+00 | 0.00e+00 | 0.00e+00 | A |
| IG_OFF W=10/L=0.2 | 0.00e+00 | 0.00e+00 | 0.00e+00 | A |
| FT W=10/L=0.2 | 8.39e+10 | 7.31e+10 | 9.66e+10 | Hz |
| CGGinv W=10/L=0.2 | 1.51e-14 | 1.53e-14 | 1.50e-14 | F |
| CGGmean W=10/L=0.2 | 1.38e-14 | 1.36e-14 | 1.39e-14 | F |
| CGD 0V W=10/L=0.2 | 3.75e-15 | 3.57e-15 | 4.05e-15 | F |
| CBD OFF[a] W=10/L=0.2 | 6.15e-15 | 6.93e-15 | 5.35e-15 | F |
| Tau W=10/L=0.2 | 3.7 | 4.5 | 3.0 | ps |
| Gm W=10/L=0.2 | 1.80e-03 | 1.49e-03 | 2.24e-03 | S |
| Gd W=10/L=0.2 | 5.39e-05 | 4.60e-05 | 5.90e-05 | S |
| Gain W=10/L=0.2 | 3.34e+01 | 3.25e+01 | 3.80e+01 | |
| VTLIN W=0.4/L=0.2 | 482 | 554 | 410 | mV |
| IDLIN W=0.4/L=0.2 | 5.81e-05 | 4.66e-05 | 7.21e-05 | A |
| VTSAT W=0.4/L=0.2 | 445 | 516 | 373 | mV |
| ION W=0.4/L=0.2 | 2.45e-04 | 1.90e-04 | 3.13e-04 | A |
| IOFF W=0.4/L=0.2 | 2.54e-12 | 1.82e-13 | 3.20e-11 | A |
| FT W=0.4/L=0.2 | 6.24e+10 | 5.40e+10 | 7.23e+10 | Hz |

Table 1: Main electrical characteristics for NMOS

a. Value coresponding to the minimum poly-to-acvtive distance specified in the DRM

## 4. MAIN ELECTRICAL CHARACTERISTICS OF PMOS SVT_1V8 TRANSISTORS

| PARAMETERS | SVT18_TT | SVT18_SSA | SVT18_FFA | units |
|---|---|---|---|---|
| P-channel transistors (psvt18) | | | | |
| VTLIN W=10/L=10.0 | 366 | 430 | 304 | mV |
| IDLIN W=10/L=10.0 | 7.39e-06 | 6.61e-06 | 8.22e-06 | A |
| VTSAT W=10/L=10.0 | 348 | 411 | 286 | mV |
| ION W=10/L=10.0 | 5.58e-05 | 4.82e-05 | 6.40e-05 | A |
| VTLIN W=10/L=0.2 | 421 | 499 | 344 | mV |
| IDLIN W=10/L=0.2 | 4.72e-04 | 3.92e-04 | 5.70e-04 | A |
| VTSAT W=10/L=0.2 | 348 | 431 | 261 | mV |
| ION W=10/L=0.2 | 3.00e-03 | 2.40e-03 | 3.78e-03 | A |
| IOFF W=10/L=0.2 | 2.78e-10 | 2.05e-11 | 4.12e-09 | A |
| IG_ON W=10/L=0.2 | 0.00e+00 | 0.00e+00 | 0.00e+00 | A |
| IG_OFF W=10/L=0.2 | 0.00e+00 | 0.00e+00 | 0.00e+00 | A |
| FT W=10/L=0.2 | 3.19e+10 | 2.79e+10 | 3.70e+10 | Hz |
| CGGinv W=10/L=0.2 | 1.65e-14 | 1.66e-14 | 1.65e-14 | F |
| CGGmean W=10/L=0.2 | 1.47e-14 | 1.44e-14 | 1.49e-14 | F |
| CGD 0V W=10/L=0.2 | 4.09e-15 | 3.91e-15 | 4.32e-15 | F |
| CBD OFF[a] W=10/L=0.2 | 6.13e-15 | 6.99e-15 | 5.25e-15 | F |
| Tau W=10/L=0.2 | 8.8 | 10.8 | 7.1 | ps |
| Gm W=10/L=0.2 | 9.47e-04 | 8.11e-04 | 1.14e-03 | S |
| Gd W=10/L=0.2 | 3.41e-05 | 2.68e-05 | 4.69e-05 | S |
| Gain W=10/L=0.2 | 2.78e+01 | 3.02e+01 | 2.43e+01 | |
| VTLIN W=0.4/L=0.2 | 415 | 501 | 325 | mV |
| IDLIN W=0.4/L=0.2 | 2.02e-05 | 1.60e-05 | 2.57e-05 | A |
| VTSAT W=0.4/L=0.2 | 342 | 434 | 243 | mV |
| ION W=0.4/L=0.2 | 1.28e-04 | 9.70e-05 | 1.69e-04 | A |
| IOFF W=0.4/L=0.2 | 1.31e-11 | 7.59e-13 | 2.69e-10 | A |
| FT W=0.4/L=0.2 | 2.78e+10 | 2.41e+10 | 3.26e+10 | Hz |

Table 2: Main electrical characteristics for PMOS

a. Value coresponding to the minimum poly-to-acvtive distance specified in the DRM

# 5. ELECTRICAL BEHAVIOR VERSUS GATE LENGTH AND CHANNEL WIDTH FOR NMOS SVT_1V8 TRANSISTORS

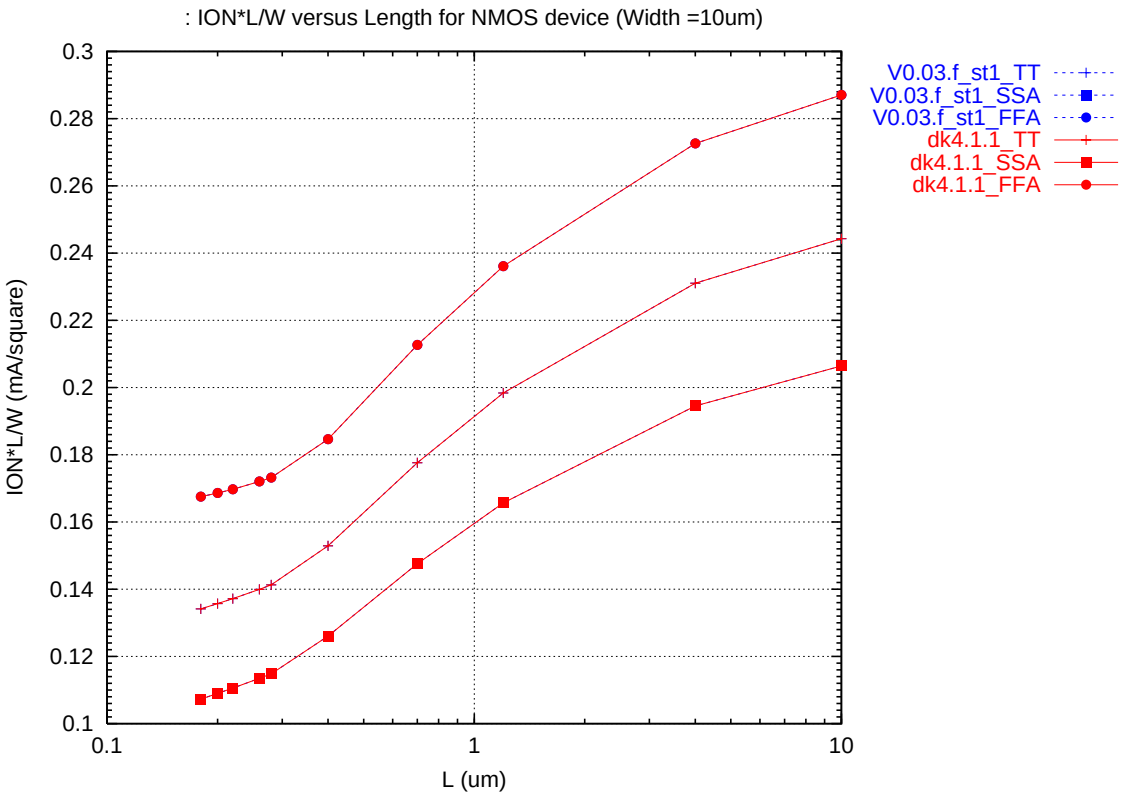


**Figure 1 : ION/❑=ION*L/W versus drawn gate length for NMOS SVT_1V8 transistors (W = 10 µm)**

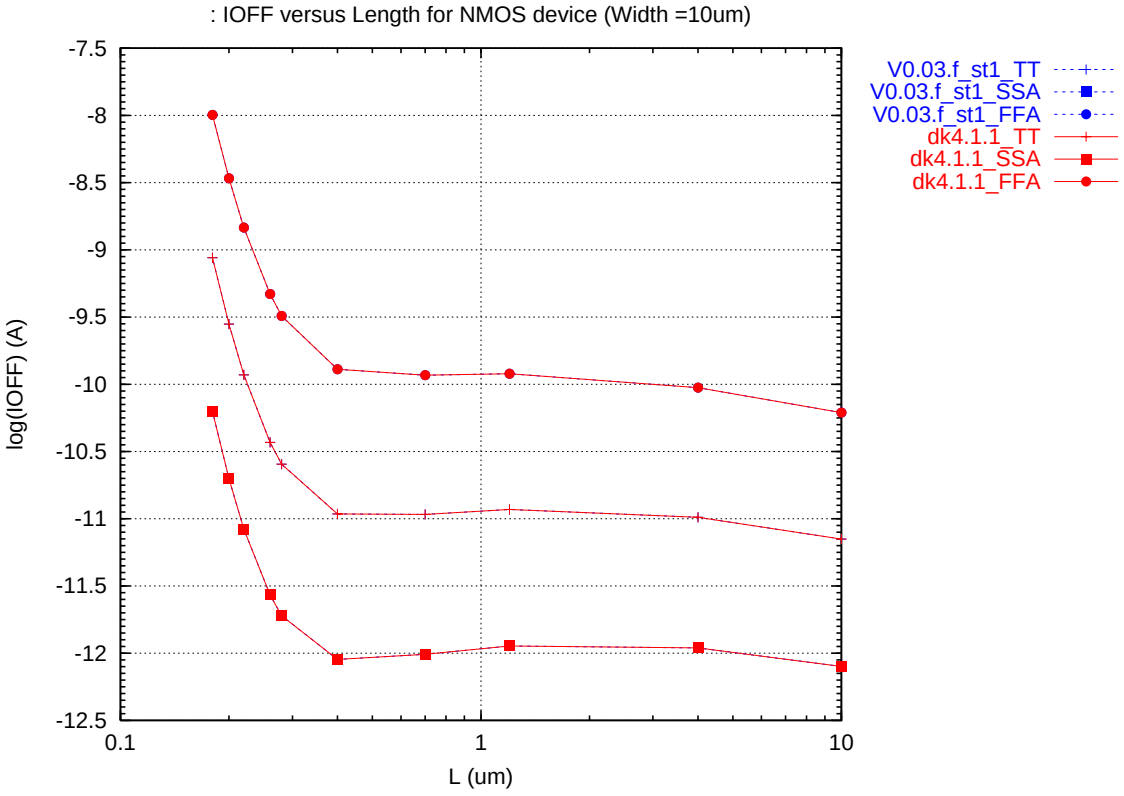


**Figure 2 : IOFF versus drawn gate length for NMOS SVT_1V8 transistors (W = 10 µm)**

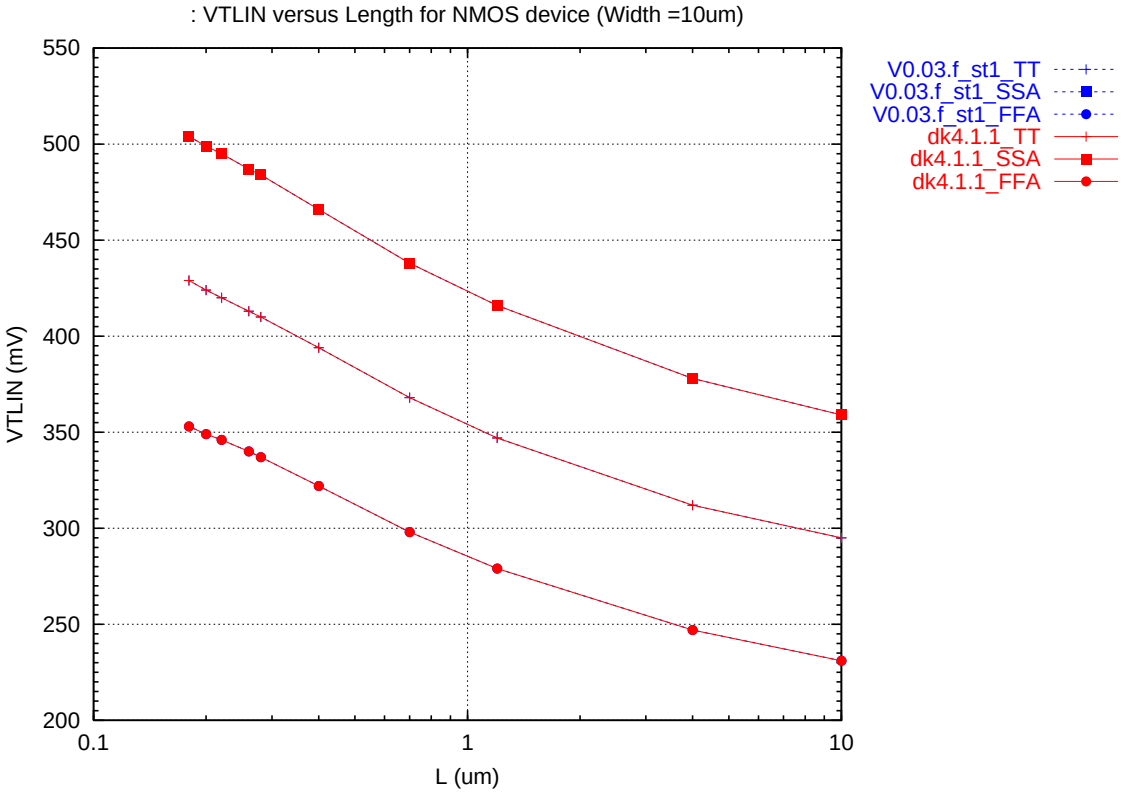


**Figure 3 : Threshold voltage VTLIN versus drawn gate length for NMOS SVT_1V8 transistors (W = 10 µm)**

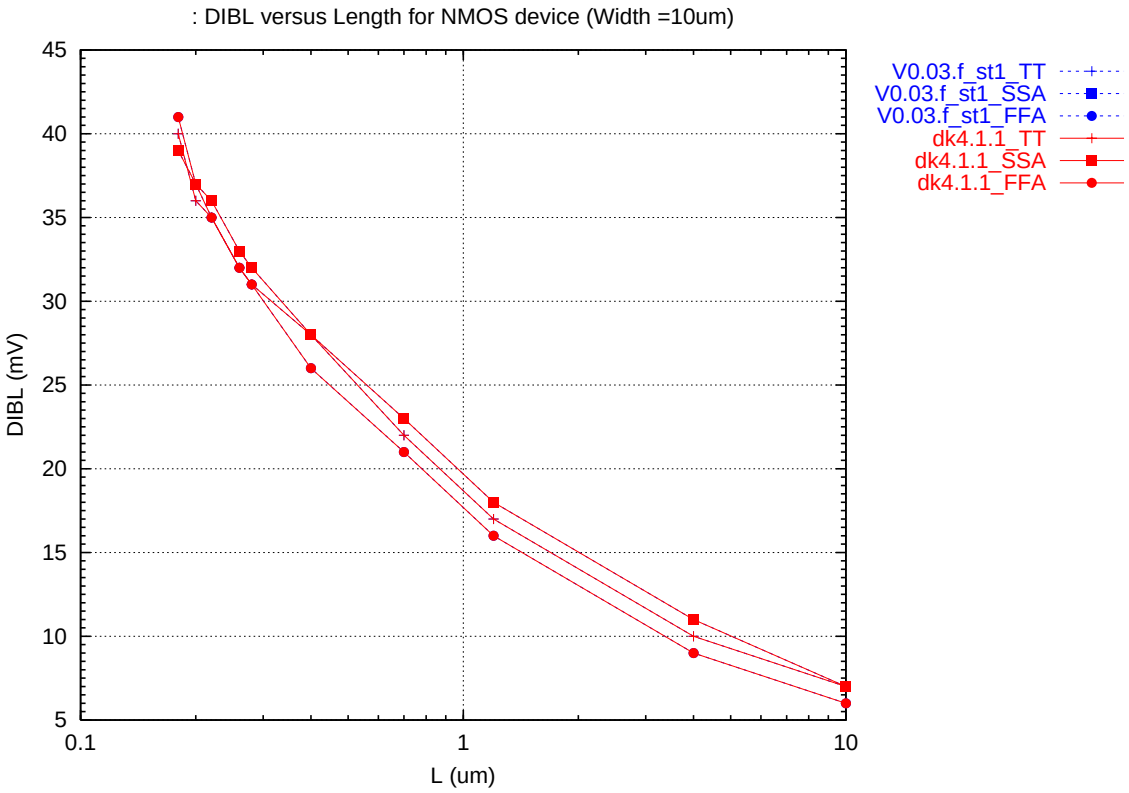


**Figure 4 : DIBL= VTLIN-VTSAT versus drawn gate length for NMOS SVT_1V8 transistors (W = 10 µm)**

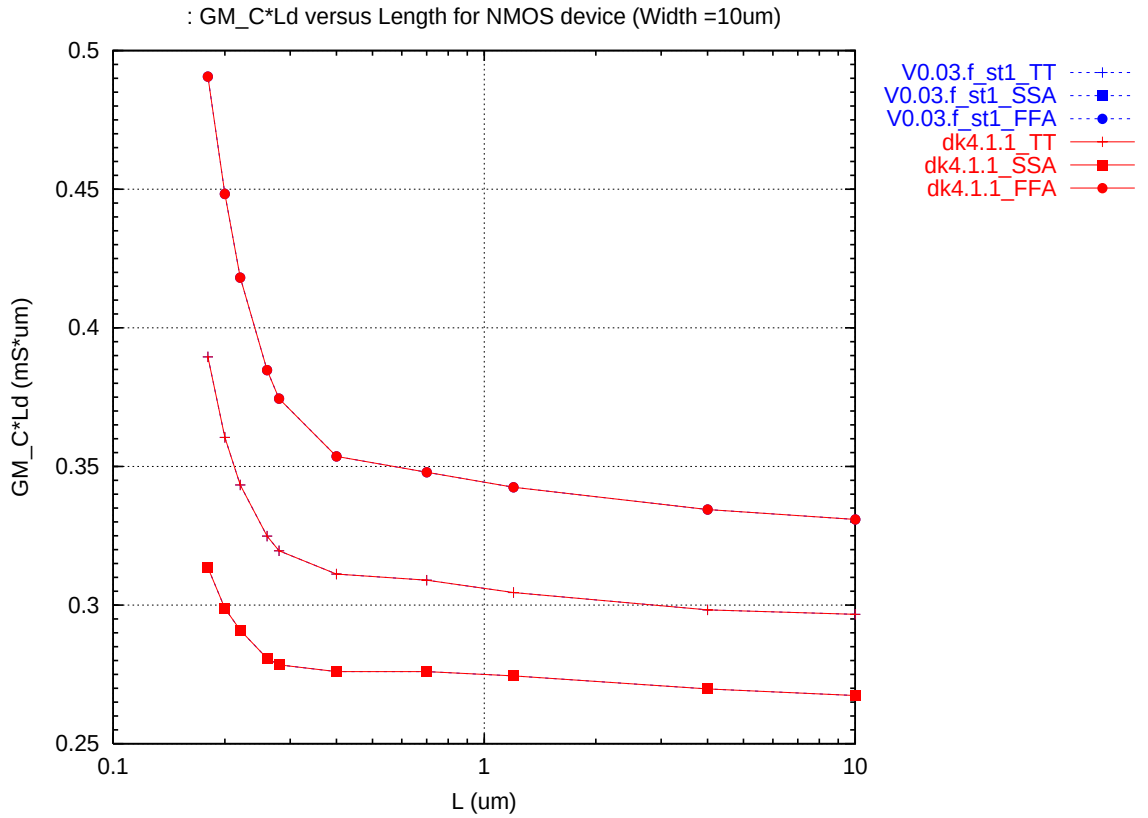


**Figure 5 : GM*Ld versus drawn gate length for NMOS SVT_1V8 transistors (W = 10 µm)**

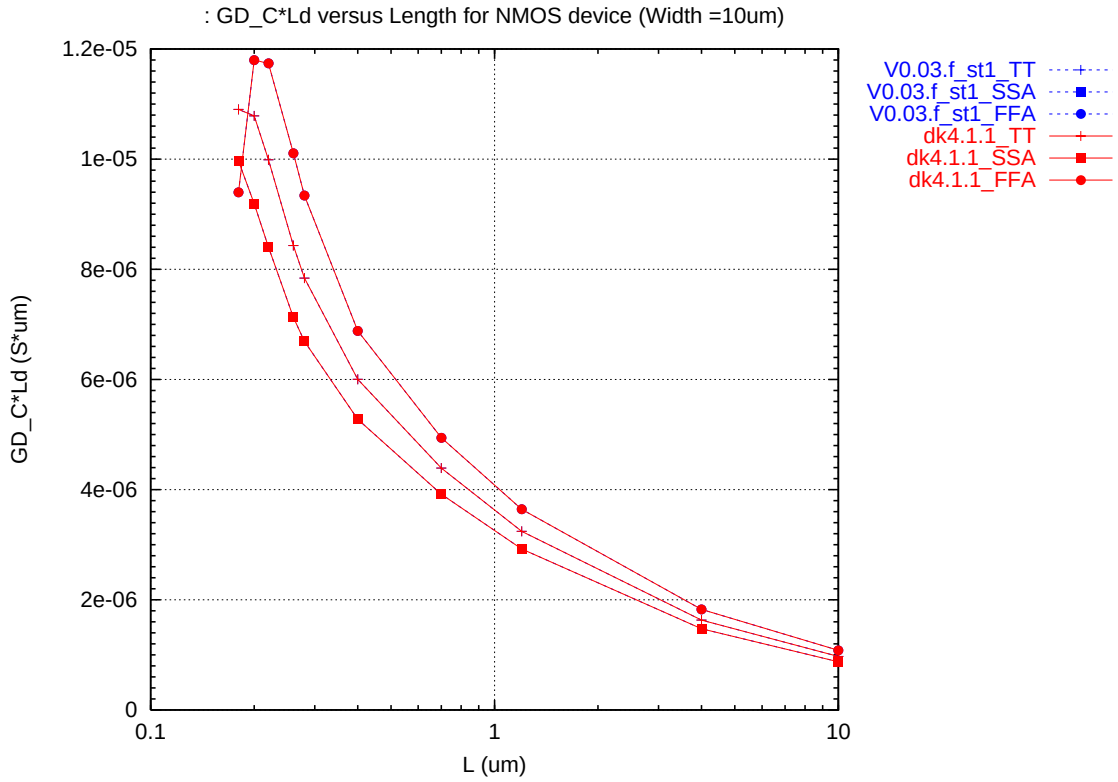


**Figure 6 : GD*Ld versus drawn gate length for NMOS SVT_1V8 transistors (W = 10 µm)**

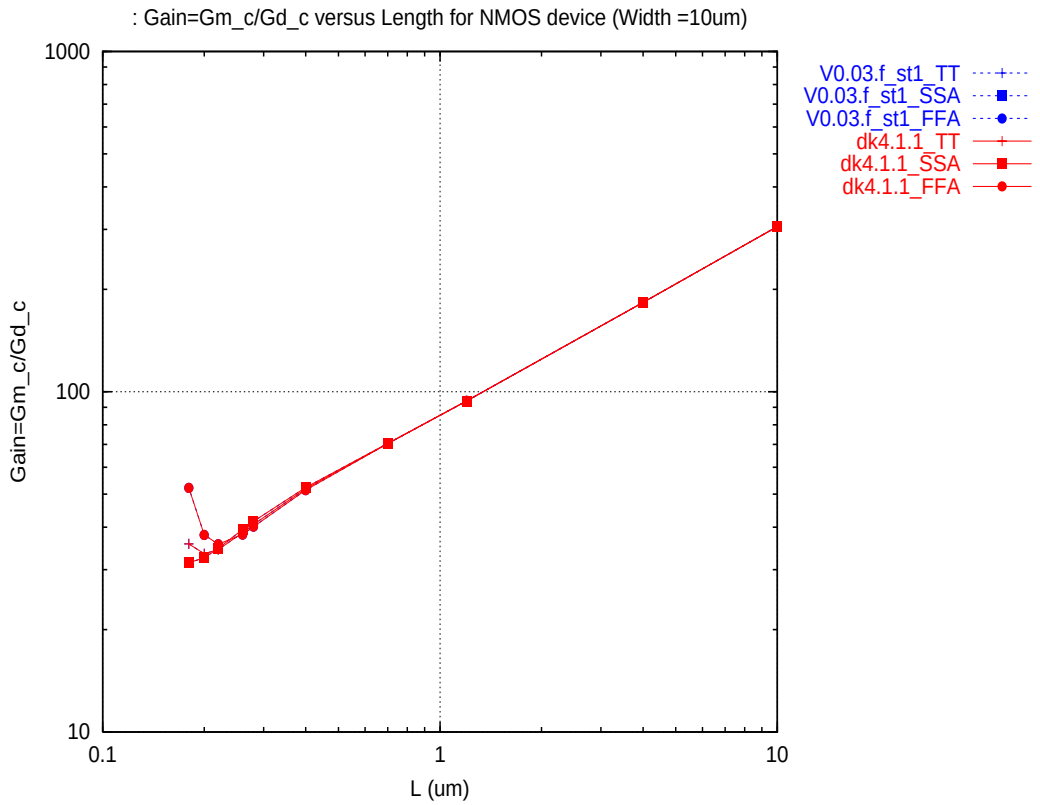


**Figure 7 : GAIN versus drawn gate length for NMOS SVT_1V8 transistors (W = 10 µm)**

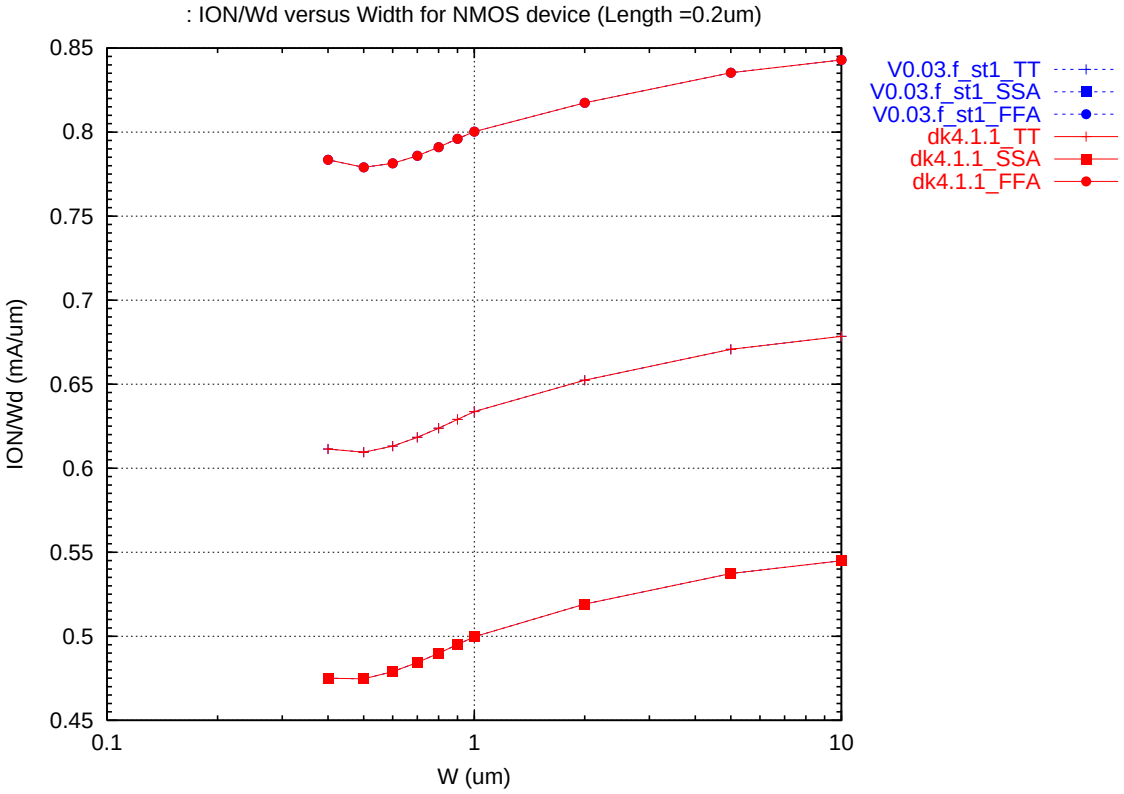


**Figure 8 : ION versus drawn channel width for NMOS SVT_1V8 transistors (L = 0.2 µm)**

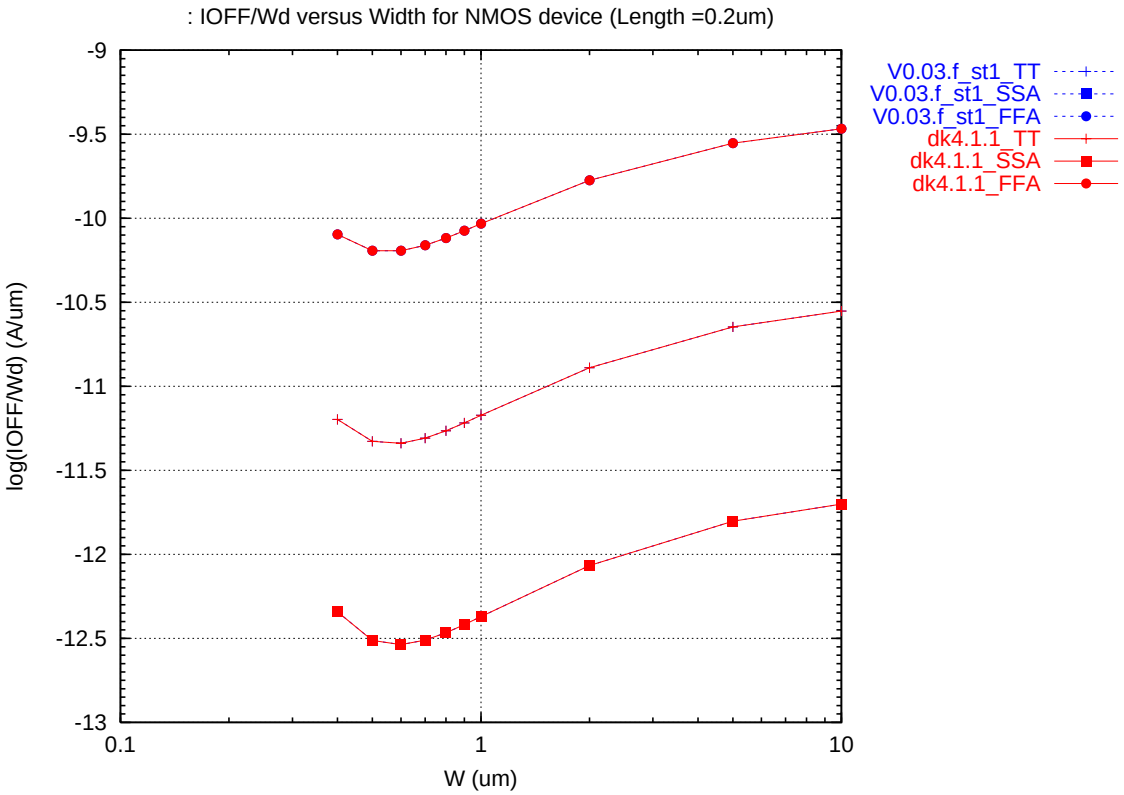


**Figure 9 : IOFF versus drawn channel width for NMOS SVT_1V8 transistors (L = 0.2 µm)**

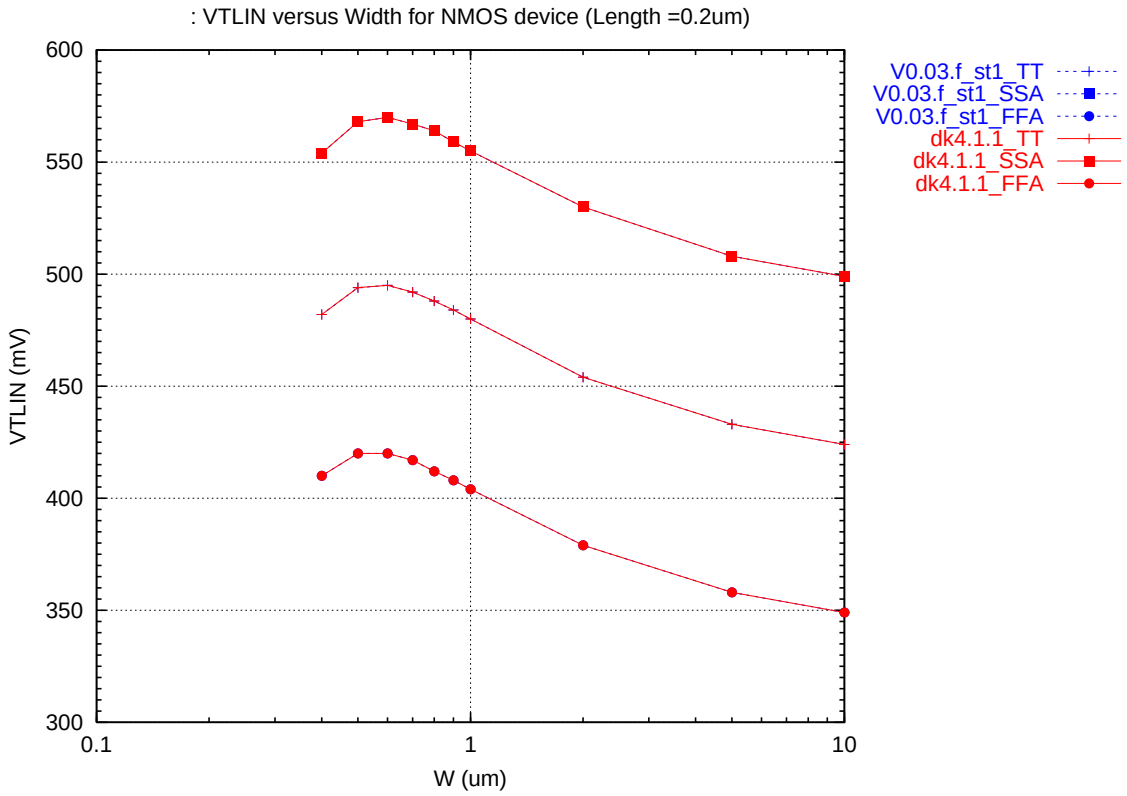


**Figure 10 : Threshold voltage VTLIN versus drawn channel width for NMOS SVT_1V8 transistors (L = 0.2 µm)**

# 6. ELECTRICAL BEHAVIOR VERSUS GATE LENGTH AND CHANNEL WIDTH FOR PMOS SVT_1V8 TRANSISTORS

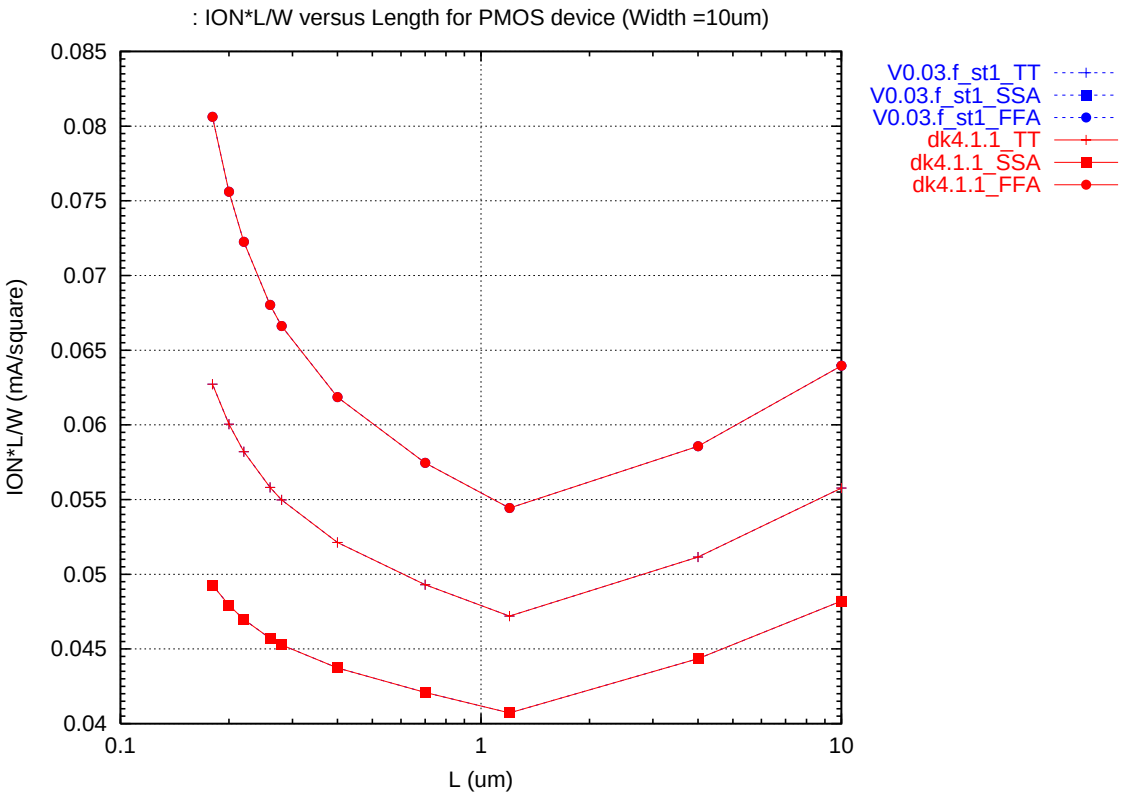


**Figure 11 : ION versus drawn gate length for PMOS SVT_1V8 transistors (W = 10 µm)**

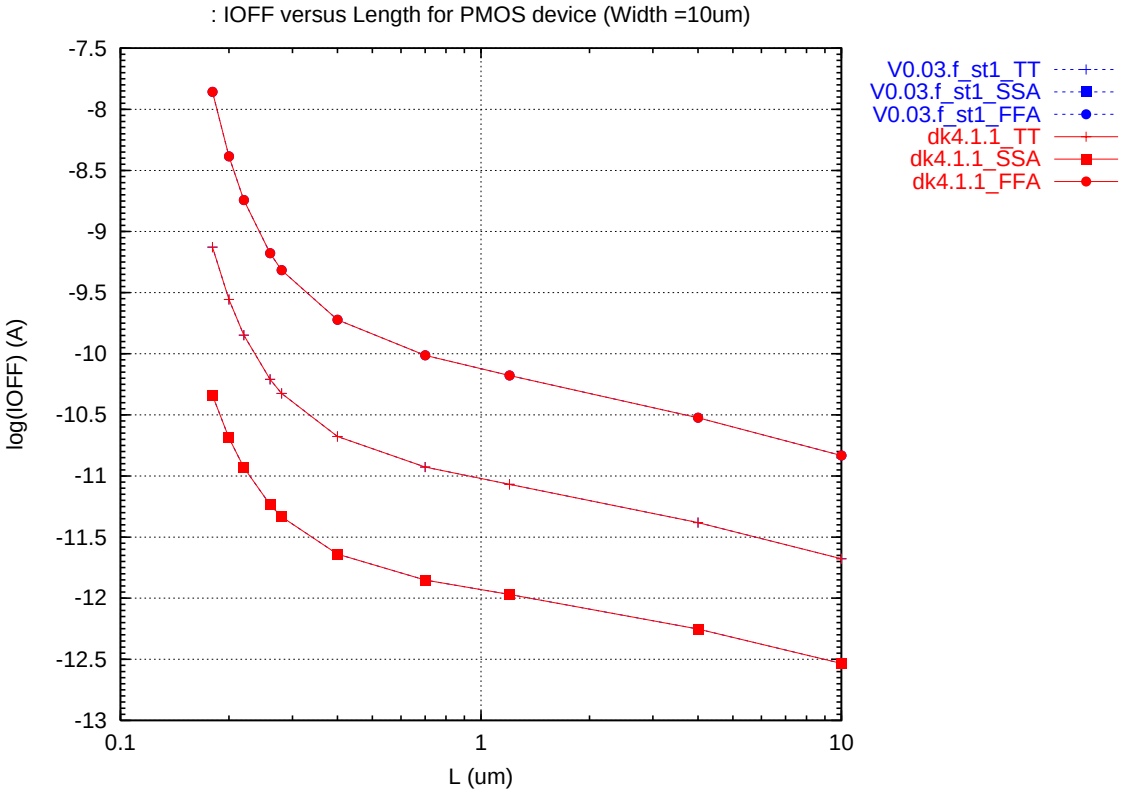


**Figure 12 : IOFF versus drawn gate length for PMOS SVT_1V8 transistors (W = 10 µm)**

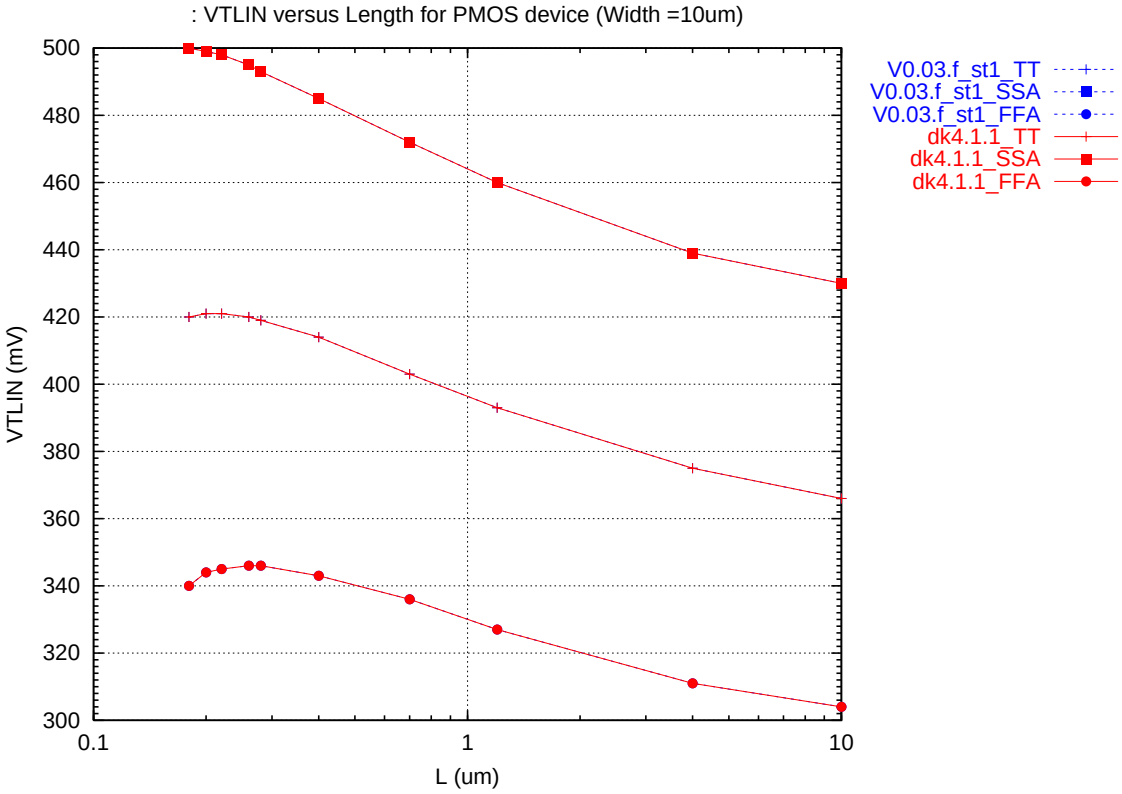


**Figure 13 : Threshold voltage VTLIN versus drawn gate length for PMOS SVT_1V8 transistors (W = 10 µm)**

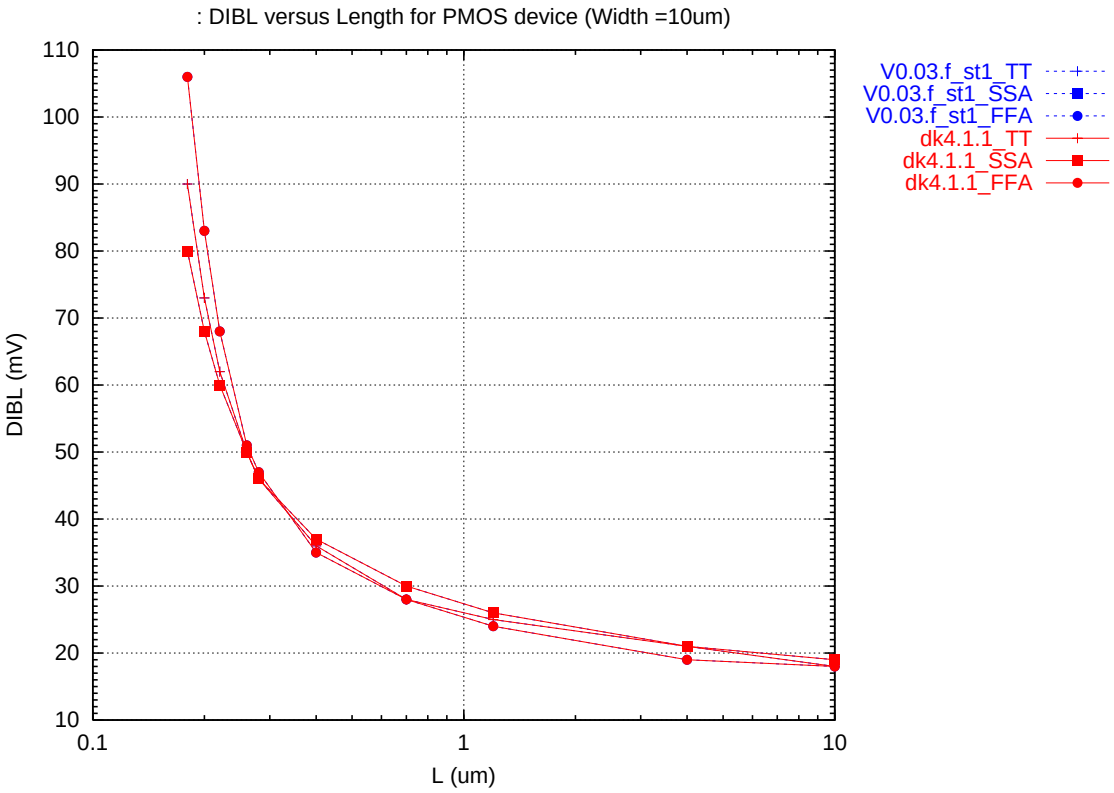


**Figure 14 : DIBL= VTLIN-VTSAT versus drawn gate length for PMOS SVT_1V8 transistors (W = 10 µm)**

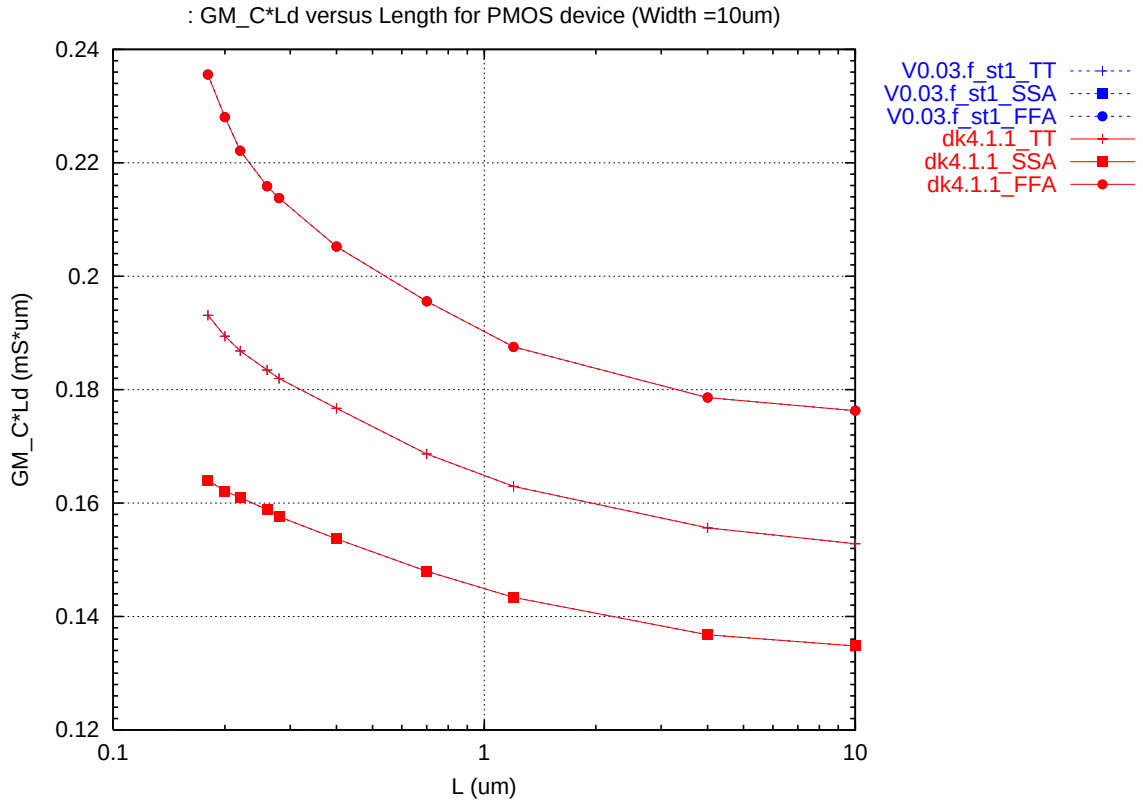


**Figure 15 : GM*Ld versus drawn gate length for PMOS SVT_1V8 transistors (W = 10 µm)**

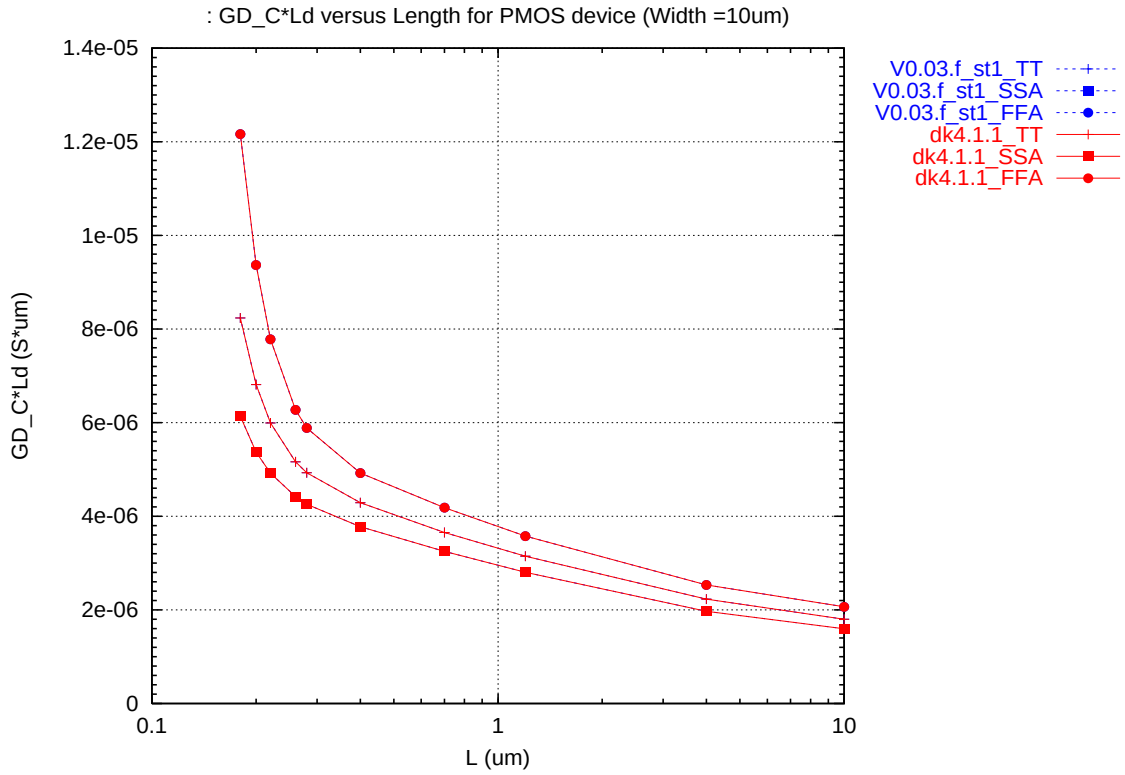


**Figure 16 : GD*Ld versus drawn gate length for PMOS SVT_1V8 transistors (W = 10 µm)**

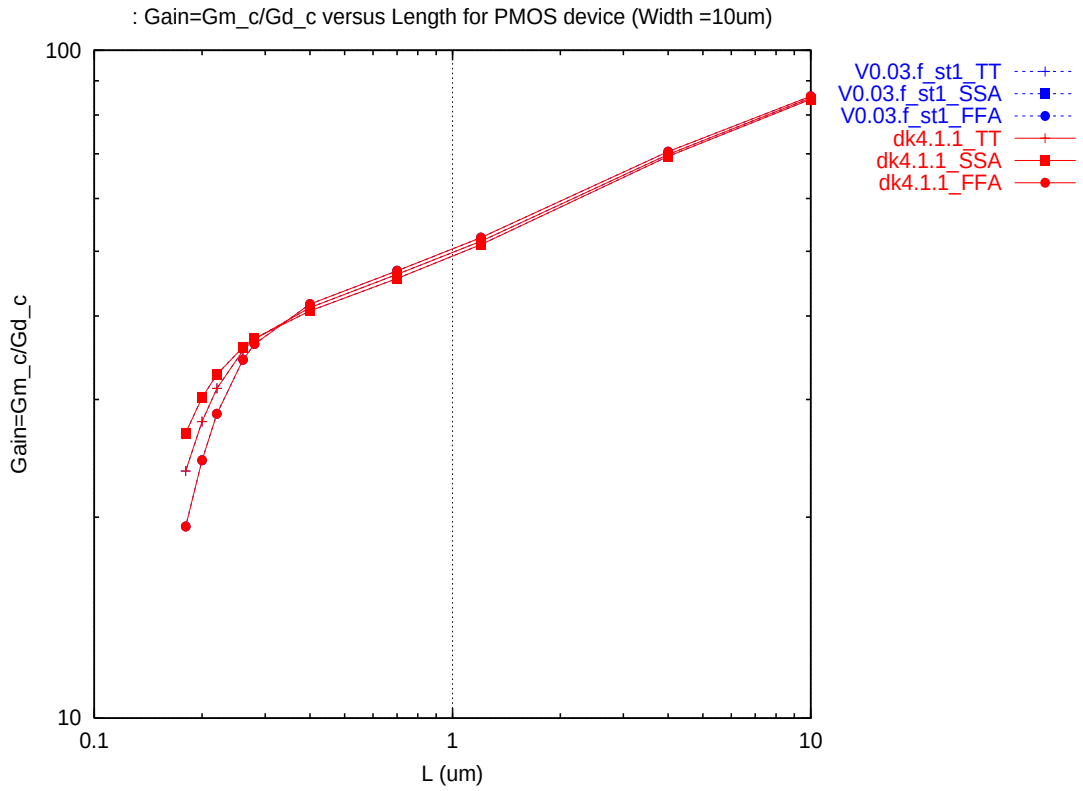


**Figure 17 : GAIN versus drawn gate length for PMOS SVT_1V8 transistors (W = 10 µm)**

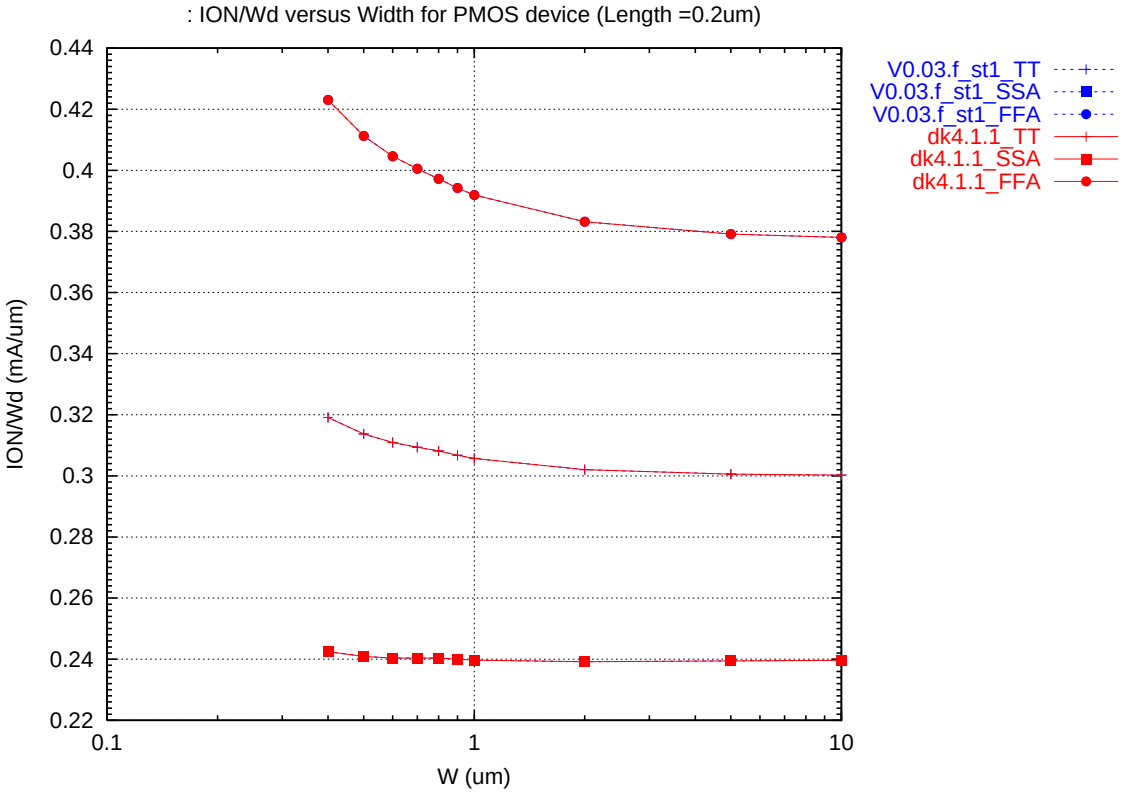


**Figure 18 : ION versus drawn channel width for PMOS SVT_1V8 transistors (L = 0.2 µm)**

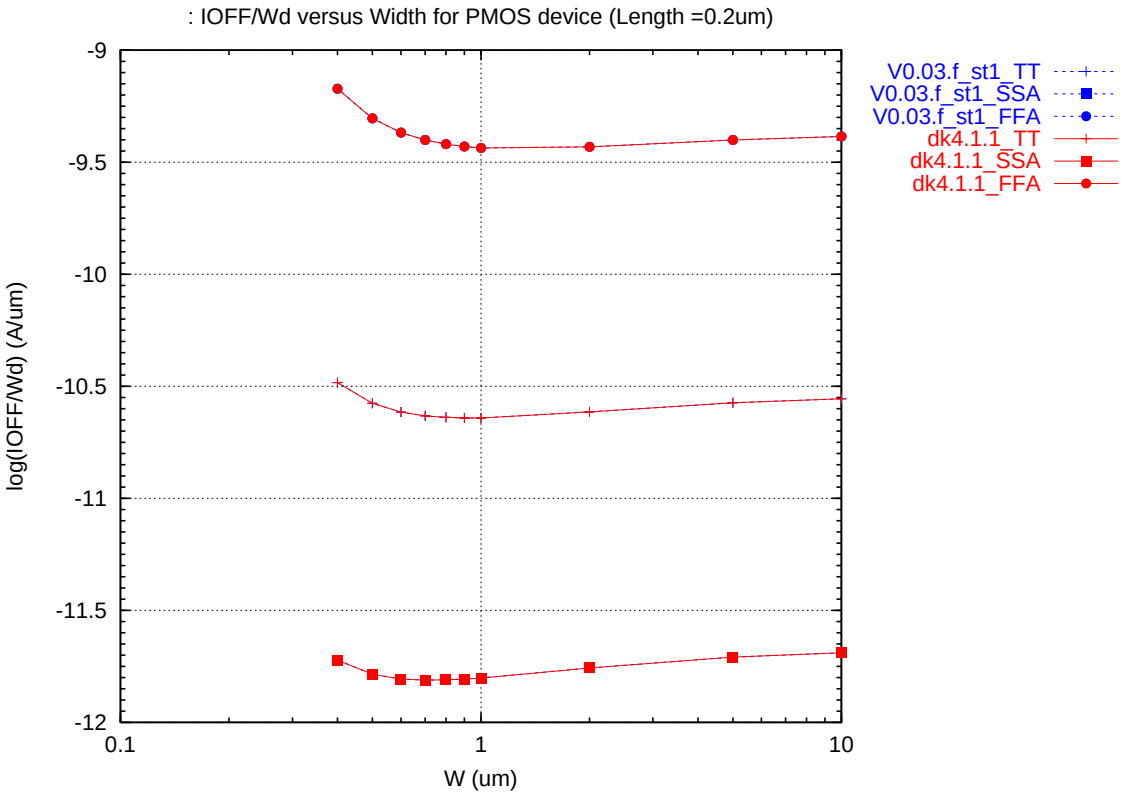


**Figure 19 : IOFF versus drawn channel width for PMOS SVT_1V8 transistors (L = 0.2 µm)**

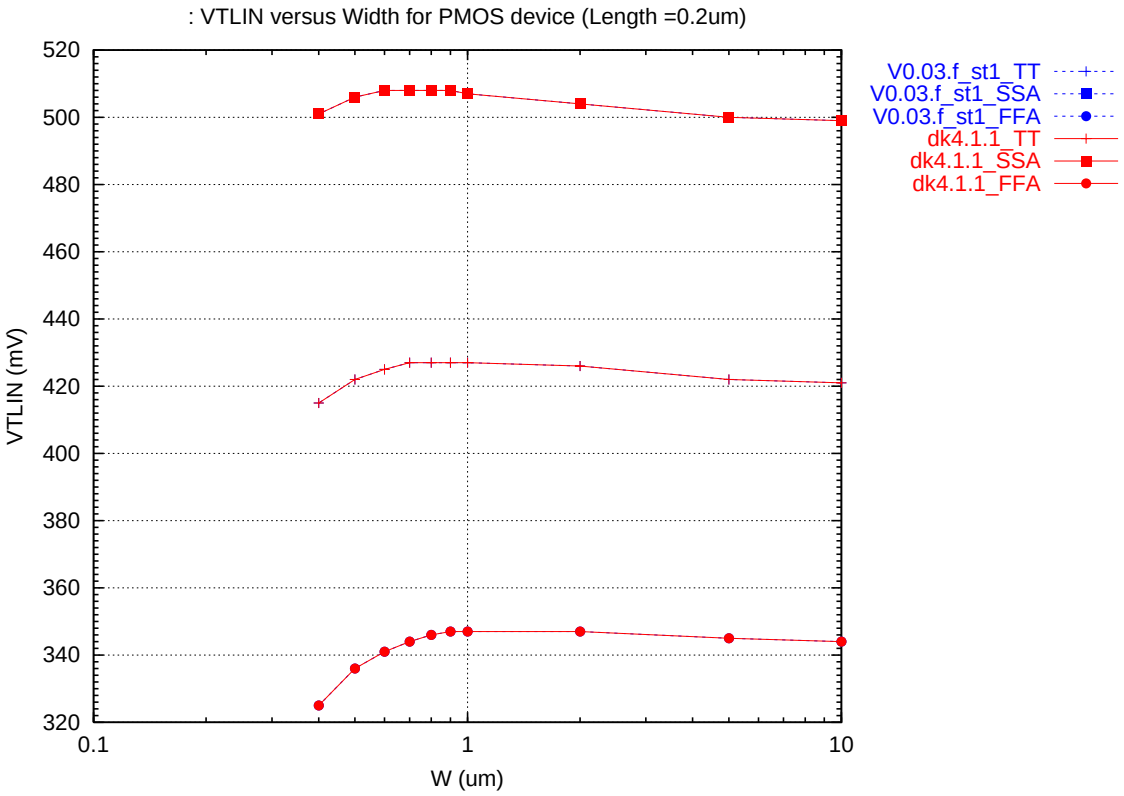


**Figure 20 : Threshold voltage VTLIN versus drawn channel width for PMOS SVT_1V8 transistors (L = 0.2 µm)**