ECE1396H Assignment 6

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A. 8-bit ADC Simulation and Characterization

We will still use a ramp input voltage to test DNL of the 8-bit ADC. The ramp input voltage will be from 0-1.1 V. To determined the slope of ramp, the following calculations will be carrier. Assume one wants to achieved a resolution of LSB $Res = 0.1LSB$ that equivalently means 10 samples/code, given the sampling frequency $f_s = 7GHz$ and $V_{LSB} = 1.1/2^8 = 4.3mV$, the ramp duration per code can be calculated as

$$\text{ramp duration/code} = \frac{1}{Res}\frac{1}{f_s} = 1.43ns \tag{1}$$

Therefore, the slope of the ramp voltage is

$$\text{ramp slope} = \frac{V_{LSB}}{\text{ramp duration/code}} = 3mV/ns \tag{2}$$

Finally, the ramp voltage duration is

$$T_{ramp} = \frac{1.1}{\text{ramp slope}} = 365.7ns \tag{3}$$

Fig. 1 and 2 shows the DNL of a 8-bit ADC with a 0 % and 1 % mismatch factor, respectively. Exclude the redundant numerical error generated during the simulation, the DNL across all code words are very close to zero that matches to the performance of an ideal ADC. When a 1 % mismatch factor is introduced to the ADC, one can observe a minimum resolution DNL error has been found across various code words.

Fig. 3 and 4 shows the SDR and ENOB with respect to various sinusoidal input amplitude given the input frequency 100 MHz. It can be seen that the SDR and ENOB increase with respect to the increase of input amplitude. When the signal utilizes the full-scale input voltage range, the highest SDR and ENOB have been achieved.

Fig. 5 and 6 shows the SDR and ENOB with respect to various sinusoidal input frequency given the input amplitude 550 mV. The sampling frequency is 7 GHz so the first Nyquist band is from 0 up to 3.5 GHz. It can be seen that from 100 MHz to 1.1 GHz the SDR drops 3 dB. So strictly speaking by definition the effective bandwidth is 1.1 GHz. The ADC reaches the minimum SDR and ENOB when the frequency is at 3.1 GHz, where still an ENOB = 8.8 is achieved, meets the 8-bit specification.

B. 2× time-interleaved 8-bit ADC Simulation and Characterization

Fig. 7 shows the DNL of 2× time-interleaved 8-bit ADC with a mismatch factor 1 % giveh the same ramp voltage duration as calculated before. Compared to Fig. 2, it can be seen that the DNL is about halved as single ADC configuration.

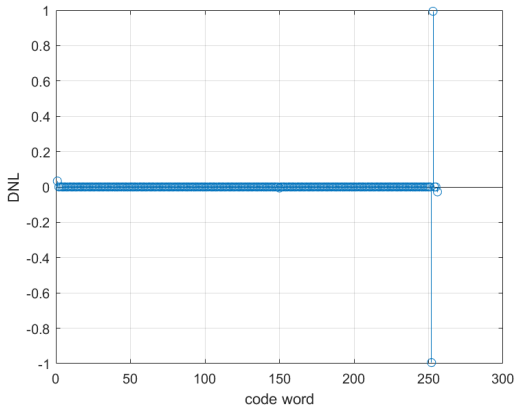

Fig. 1: DNL of 8-bit ADC with mismatch factor = 0%.

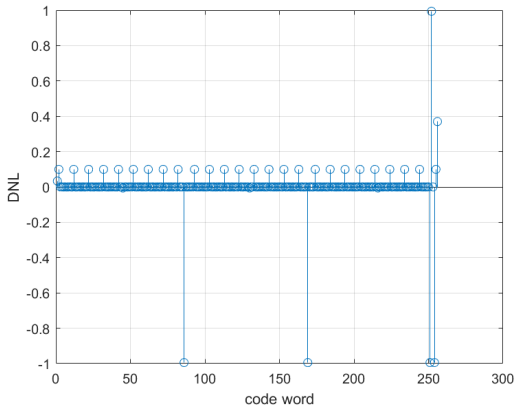

Fig. 2: DNL of 8-bit ADC with mismatch factor = 1%.

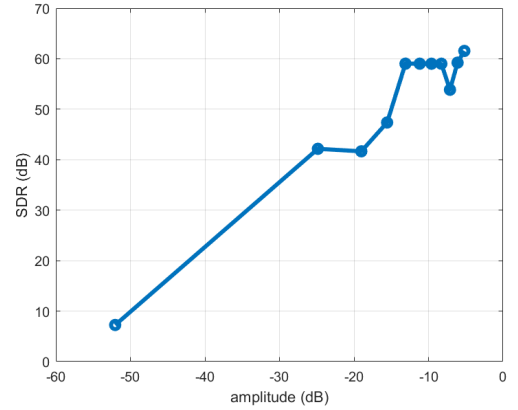

Fig. 3: SDR with respect to input sinusoidal signal amplitude. The input frequency is 100 MHz and the mismatch factor = 1 %.

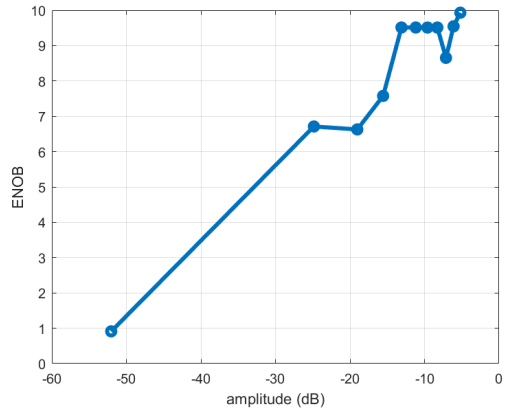

Fig. 4: ENOB with respect to input sinusoidal signal amplitude. The input frequency is 100 MHz and the mismatch factor = 1 %.

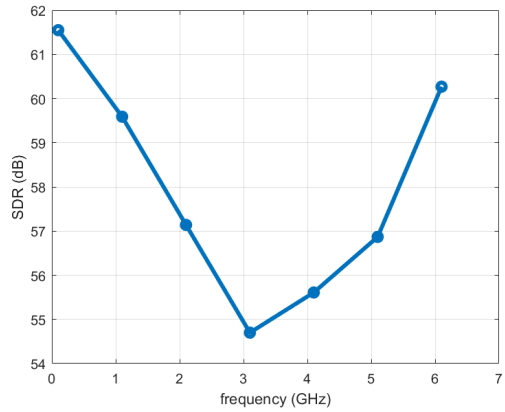

Fig. 5: SDR with respect to sinusoidal input signal frequency. The input amplitude is 550 mV and the mismatch factor = 1 %.

Fig. 8 shows the SDR of an input sinusoidal signal with respect to various frequency of a 2× time-interleaved 8-bit ADC. It can also be seen that SDR drops 3 dB around 1.5 - 2.1 GHz, so it almost double the effective bandwidth of single ADC configuration. The same improvement can be found in ENOB plot in Fig. 9. Especially at 3.1 GHz, one can see that both SDR and ENOB receive a big improvement compared to single ADC design due to the cancellation of out-of-phase harmonic distortions. The effective sampling rate here is also

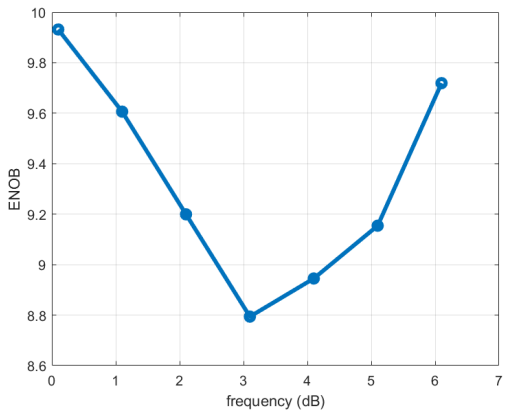

Fig. 6: SDR with respect to sinusoidal input signal frequency. The input amplitude is 550 mV and the mismatch factor = 1 %.

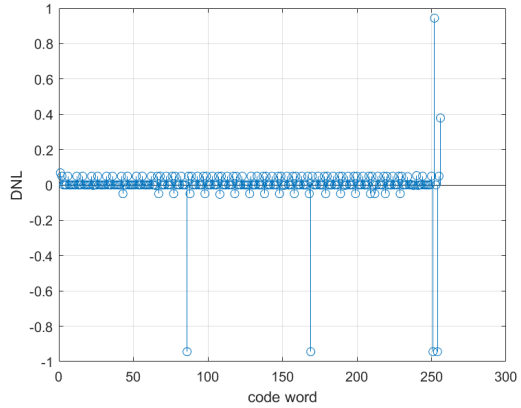

Fig. 7: DNL of 2× time-interleaved 8-bit ADC with mismatch factor = 1%.

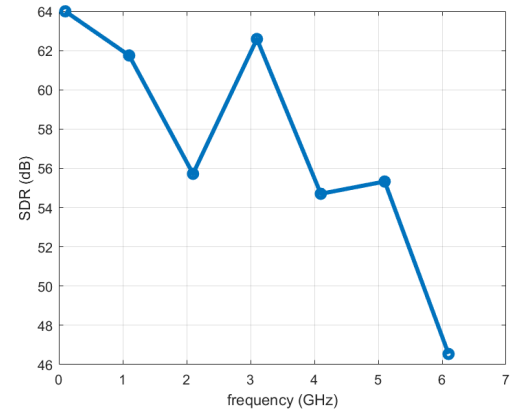

Fig. 8: SDR with respect to input sinusoidal signal frequency of 2× time-interleaved 8-bit ADC. The input amplitude is 550 mV and the mismatch factor = 1 %.

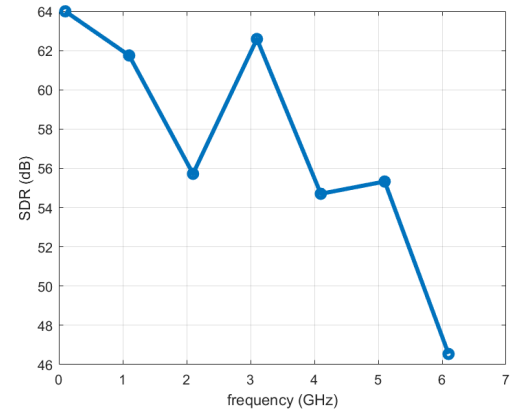

Fig. 9: ENOB with respect to input sinusoidal signal frequency of 2× time-interleaved 8-bit ADC. The input amplitude is 550 mV and the mismatch factor = 1 %.

doubled, giving a 14 GS/s if individual ADC is sampling at 7 GS/s.