LVT_LP MODELS (NLVTLP, PLVTLP)

1. CONDITIONS OF EXTRACTION

- Maturity: Preliminary
- Model parameters extraction based on lot : Q539TVB
- Geometrical extraction domain:
  - Drawn gate length : 10.0 ≥ L ≥ 0.06 µm
  - Drawn transistor width : 10 ≥ W ≥ 0.12 µm
- Temperature extraction domain: -40 ˚C to 150 ˚C
- Bias extraction domain:
  - Gate bias: 0 ≤ |VGS| ≤ 1.32 V (VDD + 10%)
  - Drain bias: 0 ≤ |VDS| ≤ 1.32 V (VDD + 10%)
  - Bulk bias: 0 ≤ |VBS| ≤ 1.32 V (VDD + 10%)

2. CONDITIONS OF SIMULATION

- Temperature: 25 ˚C
- Currents:

  IDLIN = Ids at Vgs = 1.2 V, Vds = 50 mV and Vbs = 0 V

  ION = Ids at Vgs = 1.2 V, Vds = 1.2 V and Vbs = 0 V

  IOFF = Ids at Vgs = 0 V, Vds = 1.2 V and Vbs = 0 V

  IG_ON = Igs at Vgs = 1.2 V and Vd= Vs = Vb = 0 V

  IG_OFF = Igs at Vgs =Vbs = 0 V and Vds = 1.2 V
- Threshold voltage in linear and saturation regime

  VTLIN is Vgs value at Vds = 50 mV, Vbs = 0 V and Ids= 40*W/L nA.

  VTSAT is Vgs value at Vds = 1.2 V, Vbs = 0 V and Ids= 40*W/L nA.
- Current derivatives:

$$Gm = \frac{\partial}{\partial V_{gs}} Ids$$ at Vgs = VTLIN + 0.2 V, Vds = 0.6 V and Vbs = 0 V

$$Gd = \frac{\partial}{\partial V_{ds}} Ids$$ at Vgs = VTLIN + 0.2 V, Vds = 0.6 V and Vbs = 0 V

Analog gain = Gm/Gd

- Gate Capacitances:

  CGGINV = CGG at Vgs = 1.2 V, Vds = 0 V and Vbs = 0 V

  CGD_0V = CGD at Vgs = 0 V, Vds = 0 V and Vbs = 0 V

  $$CGGMEAN = \frac{1}{VDD} \cdot \int_{0}^{VDD} CGG \times dVgs$$ with VDD = 1.2 V and Vbs = 0 V

  TAU = CGGMEAN*VDD/ION

- Diode Capacitances:

  CBD OFF = CBD at Vgs = 0 V, Vds = 1.2 V and Vbs = 0 V

  Note: the area and perimiters of source/drain junction diodes used for simulation are defined with the the minimum poly-to-active distance specified in the DRM.

- Transition frequency:

  FT = frequency for which the small signal current gain H_{21} is 0 dB (i.e. $\left|\frac{I_d}{I_g}\right|$ = 0 dB).

3. MAIN ELECTRICAL CHARACTERISTICS OF NMOS LVT_LP TRANSISTORS

PARAMETERS	LVTLP_TT	LVTLP_SS	LVTLP_FF	units
N-channel transistors (nlvtlp)				
VTLIN W=1/L=10.0	120	142	100	mV
IDLIN W=1/L=10.0	1.60e-06	1.50e-06	1.71e-06	A
VTSAT W=1/L=10.0	98	120	77	mV
ION W=1/L=10.0	1.71e-05	1.57e-05	1.86e-05	A
VTLIN W=1/L=0.06	363	414	300	mV
IDLIN W=1/L=0.06	1.08e-04	9.25e-05	1.28e-04	A
VTSAT W=1/L=0.06	194	266	103	mV
ION W=1/L=0.06	7.40e-04	6.24e-04	8.84e-04	A
IOFF W=1/L=0.06	5.06e-09	7.04e-10	5.48e-08	A
IG_ON W=1/L=0.06	8.15e-12	3.99e-12	1.70e-11	A
IG_OFF W=1/L=0.06	1.46e-12	7.08e-13	3.01e-12	A
FT W=1/L=0.06	1.60e+11	1.43e+11	1.79e+11	Hz
CGGinv W=1/L=0.06	1.17e-15	1.23e-15	1.10e-15	F
CGGmean W=1/L=0.06	1.04e-15	1.07e-15	1.01e-15	F
CGD 0V W=1/L=0.06	3.82e-16	3.73e-16	3.99e-16	F
CBD OFF[a] W=1/L=0.06	3.94e-16	4.42e-16	3.44e-16	F
Tau W=1/L=0.06	1.7	2.1	1.4	ps
Gm W=1/L=0.06	4.99e-04	4.43e-04	5.67e-04	S
Gd W=1/L=0.06	7.67e-05	5.99e-05	1.01e-04	S
Gain W=1/L=0.06	6.51e+00	7.40e+00	5.60e+00	
VTLIN W=0.12/L=0.06	318	376	247	mV
IDLIN W=0.12/L=0.06	1.47e-05	1.23e-05	1.77e-05	A
VTSAT W=0.12/L=0.06	200	271	112	mV
ION W=0.12/L=0.06	1.03e-04	8.43e-05	1.26e-04	A
IOFF W=0.12/L=0.06	5.06e-10	7.32e-11	5.23e-09	A
FT W=0.12/L=0.06	1.29e+11	1.15e+11	1.45e+11	Hz

Table 1: Main electrical characteristics for NMOS

a. Value coresponding to the minimum poly-to-acvtive distance specified in the DRM

4. MAIN ELECTRICAL CHARACTERISTICS OF PMOS LVT_LP TRANSISTORS

PARAMETERS	LVTLP_TT	LVTLP_SS	LVTLP_FF	units
P-channel transistors (plvtlp)				
VTLIN W=1/L=10.0	216	236	196	mV
IDLIN W=1/L=10.0	4.88e-07	4.55e-07	5.22e-07	A
VTSAT W=1/L=10.0	196	216	176	mV
ION W=1/L=10.0	4.71e-06	4.29e-06	5.17e-06	A
VTLIN W=1/L=0.06	421	459	377	mV
IDLIN W=1/L=0.06	4.46e-05	3.87e-05	5.16e-05	A
VTSAT W=1/L=0.06	253	312	178	mV
ION W=1/L=0.06	3.94e-04	3.33e-04	4.70e-04	A
IOFF W=1/L=0.06	2.43e-09	4.20e-10	1.74e-08	A
IG_ON W=1/L=0.06	2.15e-12	1.10e-12	4.16e-12	A
IG_OFF W=1/L=0.06	7.18e-13	3.65e-13	1.40e-12	A
FT W=1/L=0.06	9.62e+10	8.71e+10	1.06e+11	Hz
CGGinv W=1/L=0.06	1.18e-15	1.25e-15	1.12e-15	F
CGGmean W=1/L=0.06	1.01e-15	1.04e-15	9.82e-16	F
CGD 0V W=1/L=0.06	3.56e-16	3.52e-16	3.64e-16	F
CBD OFF[a] W=1/L=0.06	3.97e-16	4.45e-16	3.47e-16	F
Tau W=1/L=0.06	3.1	3.8	2.5	ps
Gm W=1/L=0.06	2.86e-04	2.50e-04	3.32e-04	S
Gd W=1/L=0.06	4.76e-05	3.65e-05	6.42e-05	S
Gain W=1/L=0.06	6.01e+00	6.85e+00	5.17e+00	
VTLIN W=0.12/L=0.06	373	426	308	mV
IDLIN W=0.12/L=0.06	6.53e-06	5.55e-06	7.71e-06	A
VTSAT W=0.12/L=0.06	242	310	157	mV
ION W=0.12/L=0.06	5.86e-05	4.80e-05	7.21e-05	A
IOFF W=0.12/L=0.06	1.94e-10	2.25e-11	2.19e-09	A
FT W=0.12/L=0.06	7.78e+10	7.05e+10	8.54e+10	Hz

Table 2: Main electrical characteristics for PMOS

a. Value coresponding to the minimum poly-to-acvtive distance specified in the DRM

5. ELECTRICAL BEHAVIOR VERSUS GATE LENGTH AND CHANNEL WIDTH FOR NMOS LVT_LP TRANSISTORS

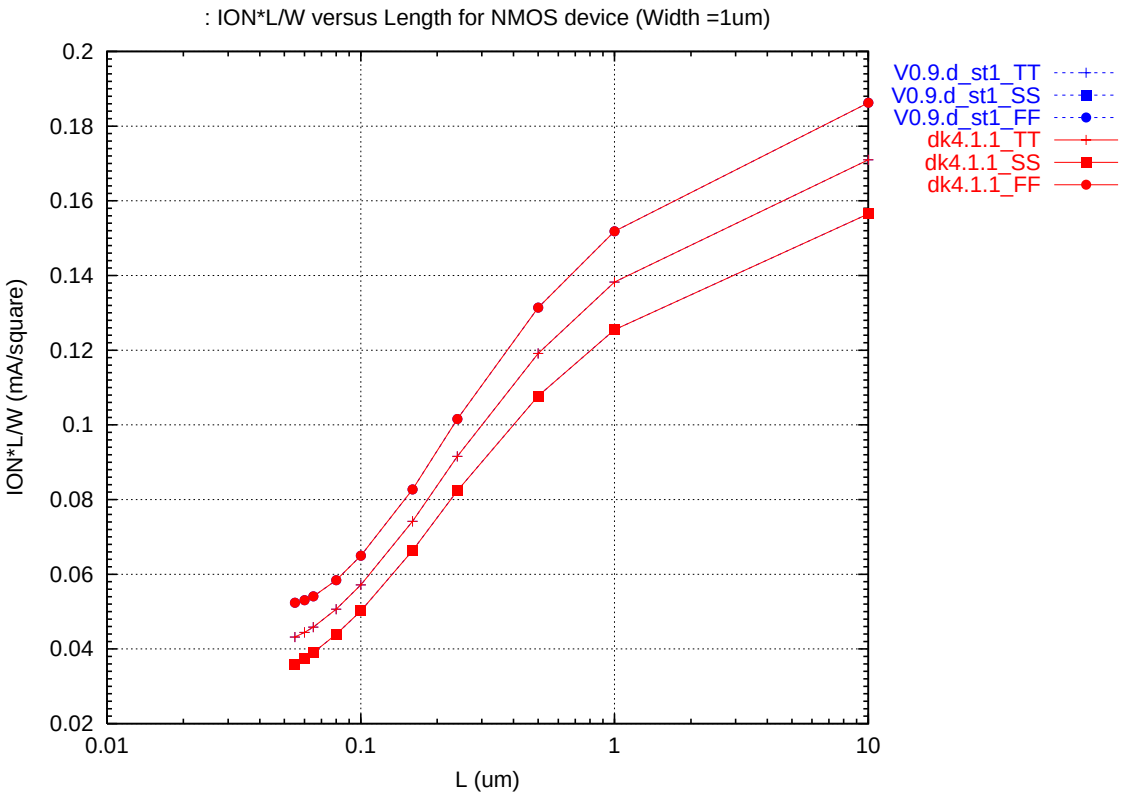

Figure 1 : ION/❑=ION*L/W versus drawn gate length for NMOS LVT_LP transistors (W = 1 µm)

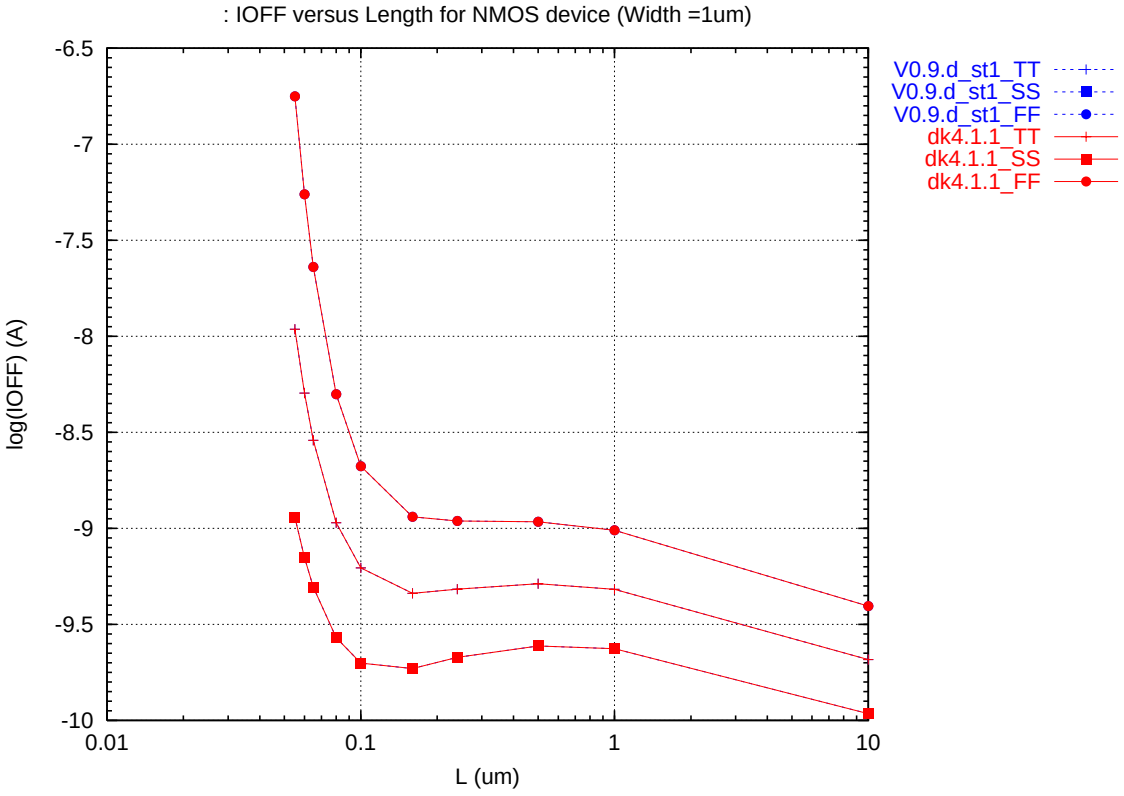

Figure 2 : IOFF versus drawn gate length for NMOS LVT_LP transistors (W = 1 µm)

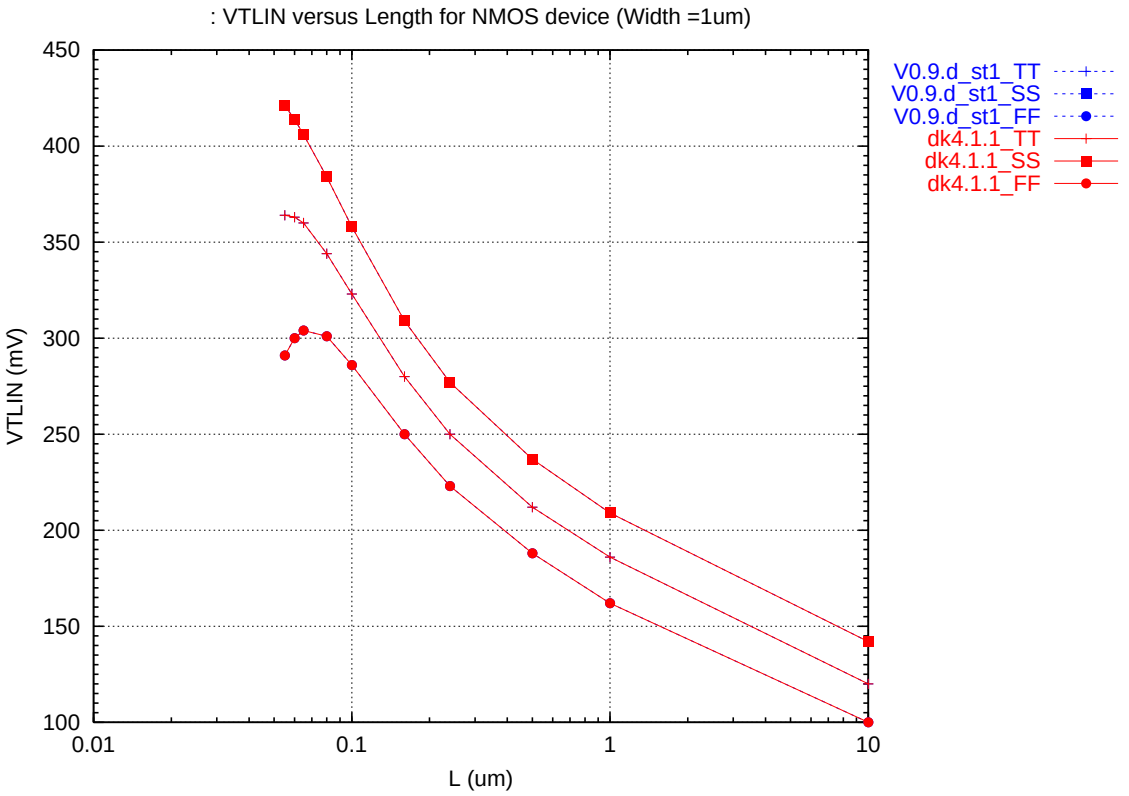

Figure 3 : Threshold voltage VTLIN versus drawn gate length for NMOS LVT_LP transistors (W = 1 µm)

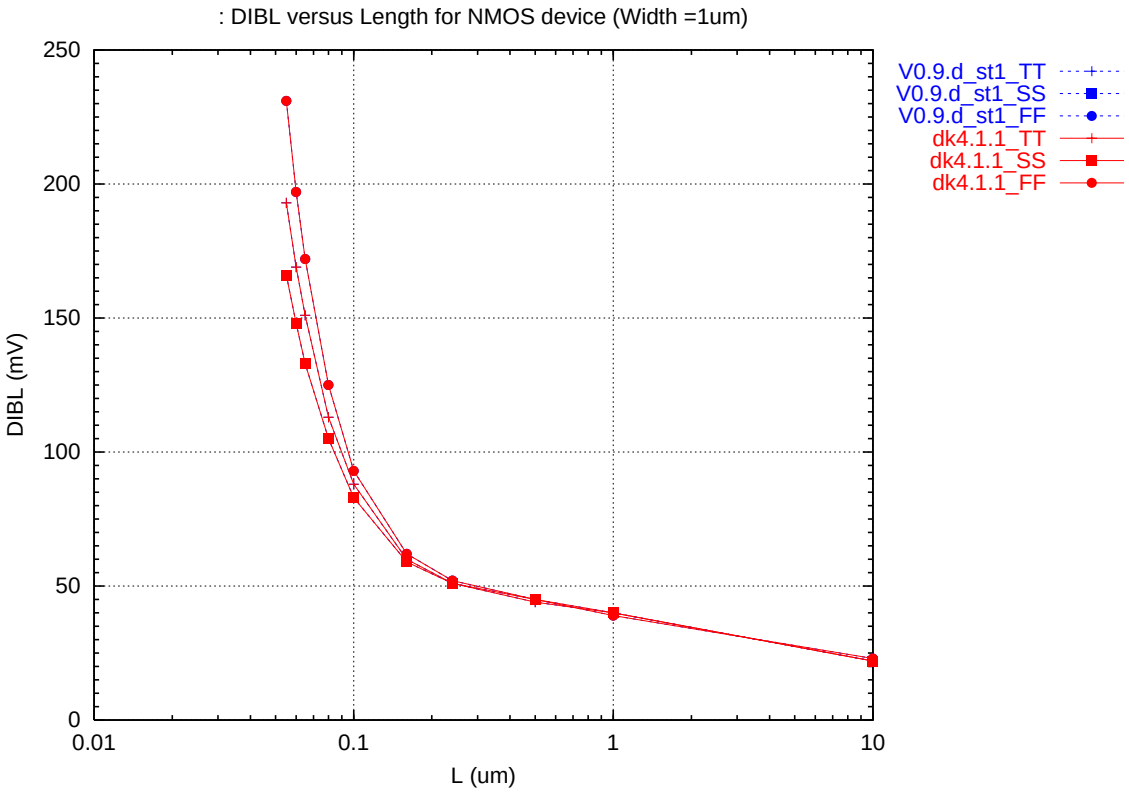

Figure 4 : DIBL= VTLIN-VTSAT versus drawn gate length for NMOS LVT_LP transistors (W = 1 µm)

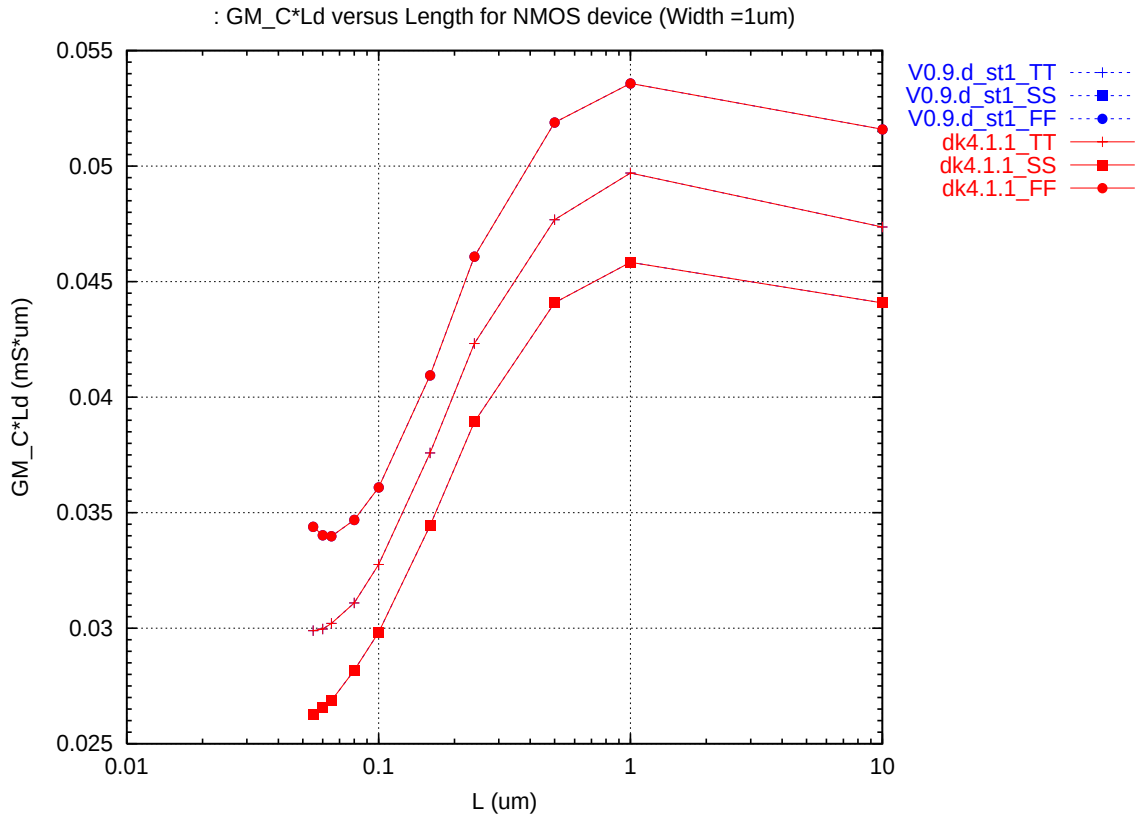

Figure 5 : GM*Ld versus drawn gate length for NMOS LVT_LP transistors (W = 1 µm)

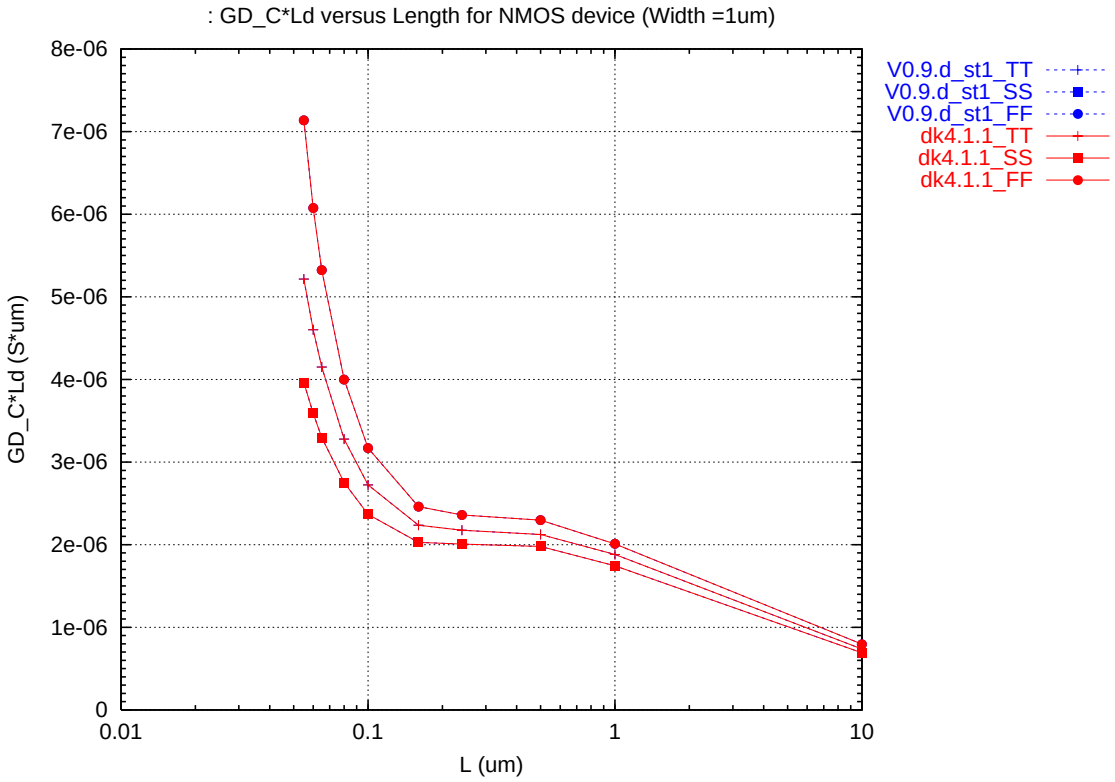

Figure 6 : GD*Ld versus drawn gate length for NMOS LVT_LP transistors (W = 1 µm)

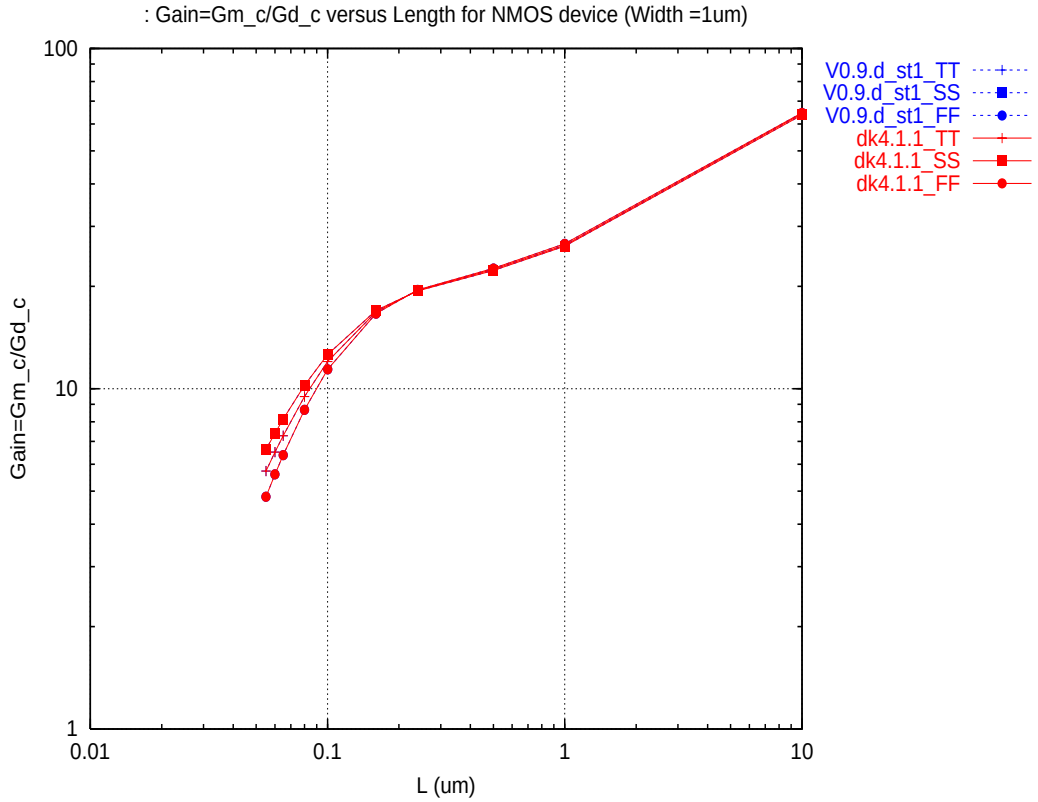

Figure 7 : GAIN versus drawn gate length for NMOS LVT_LP transistors (W = 1 µm)

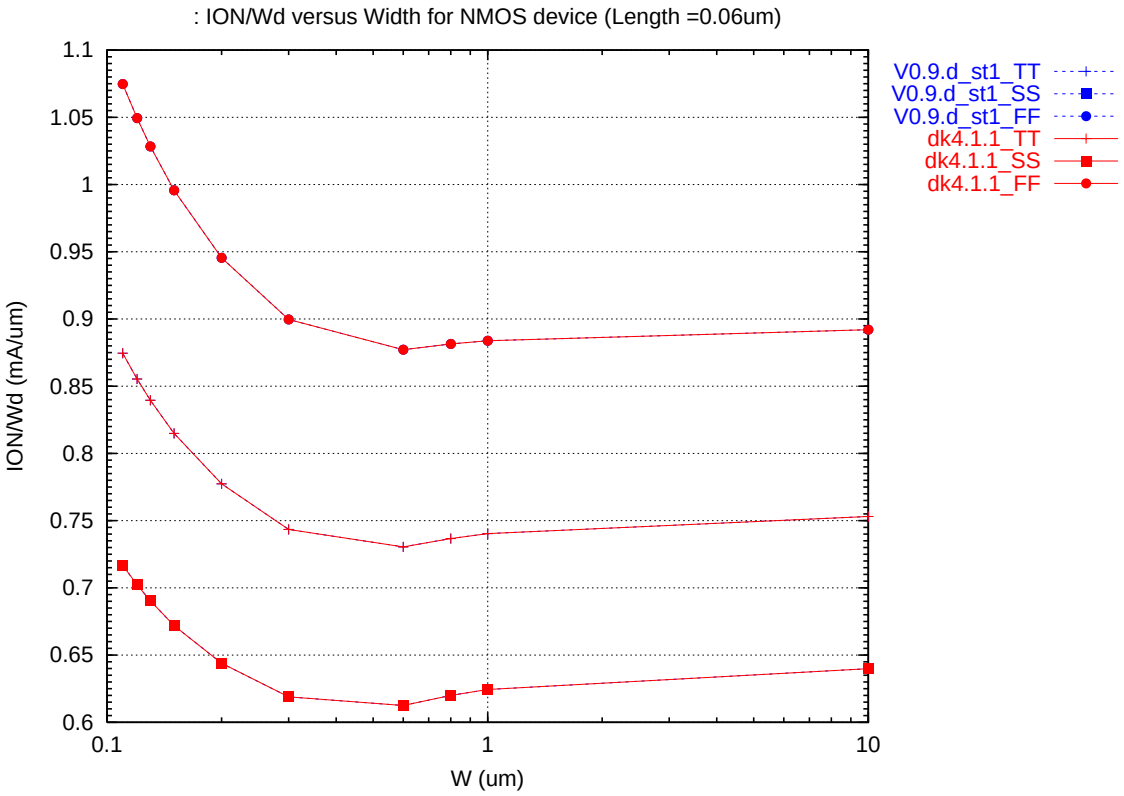

Figure 8 : ION versus drawn channel width for NMOS LVT_LP transistors (L = 0.06 µm)

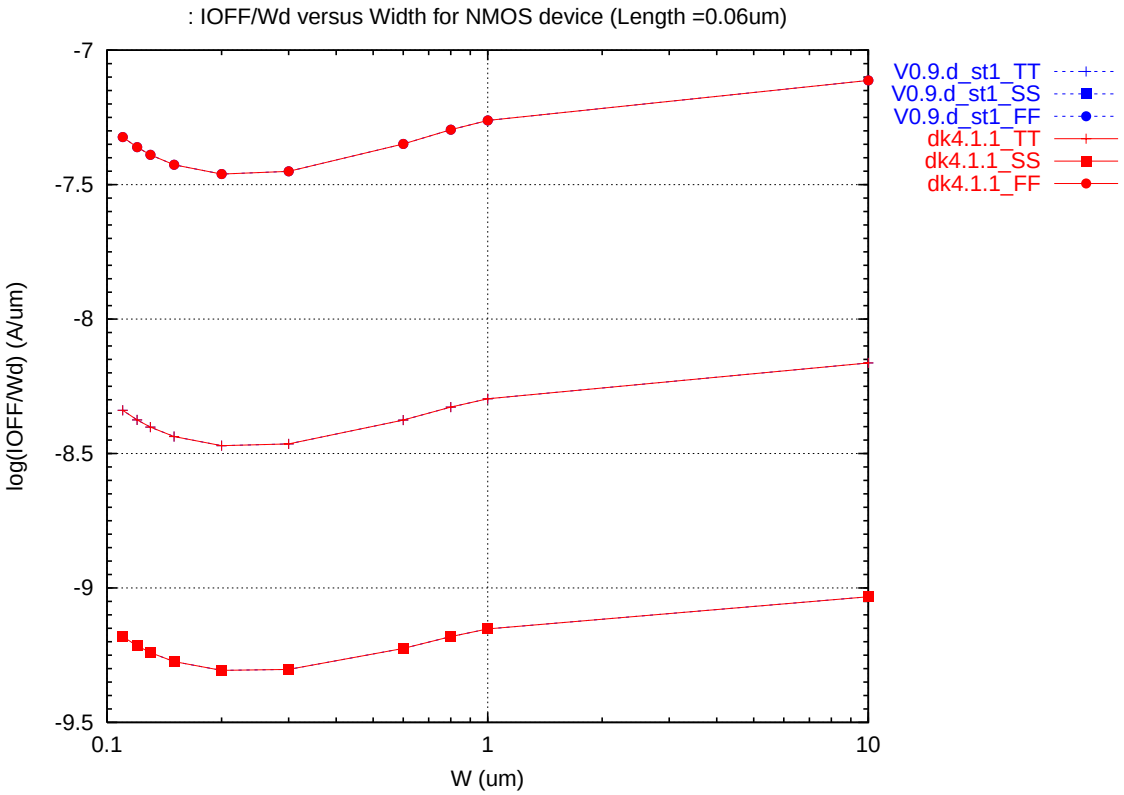

Figure 9 : IOFF versus drawn channel width for NMOS LVT_LP transistors (L = 0.06 µm)

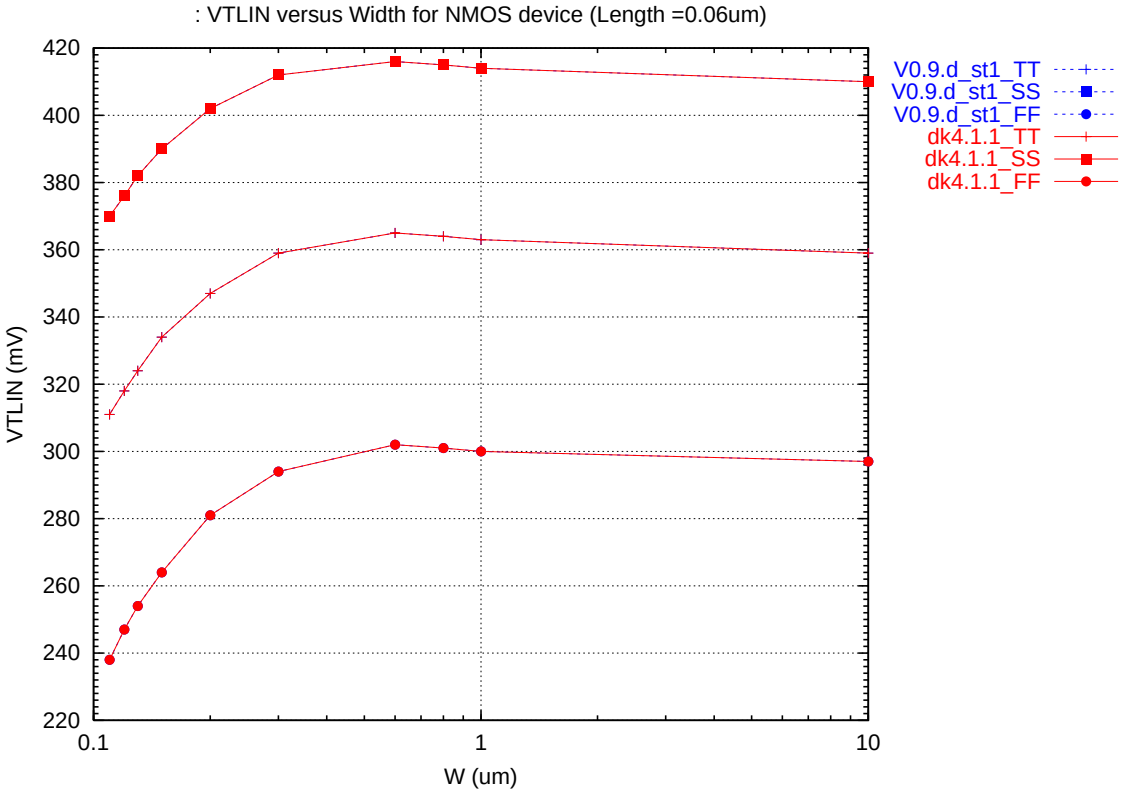

Figure 10 : Threshold voltage VTLIN versus drawn channel width for NMOS LVT_LP transistors (L = 0.06 µm)

6. ELECTRICAL BEHAVIOR VERSUS GATE LENGTH AND CHANNEL WIDTH FOR PMOS LVT_LP TRANSISTORS

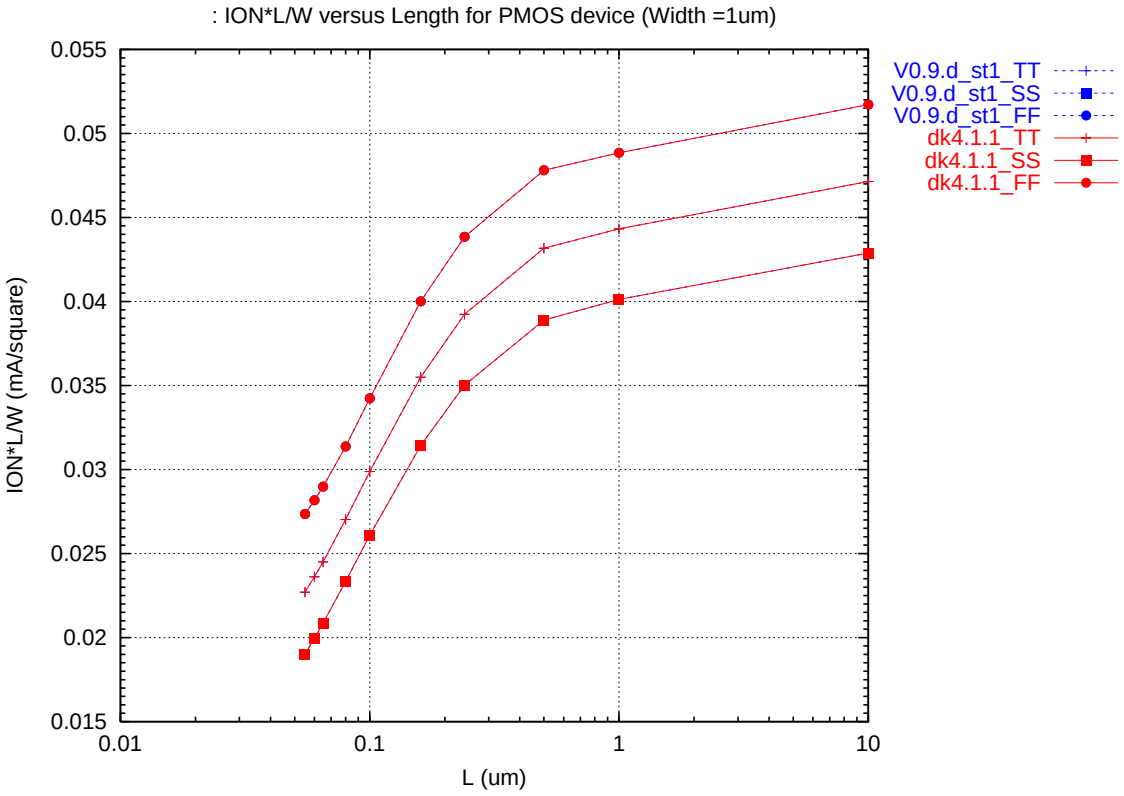

Figure 11 : ION versus drawn gate length for PMOS LVT_LP transistors (W = 1 µm)

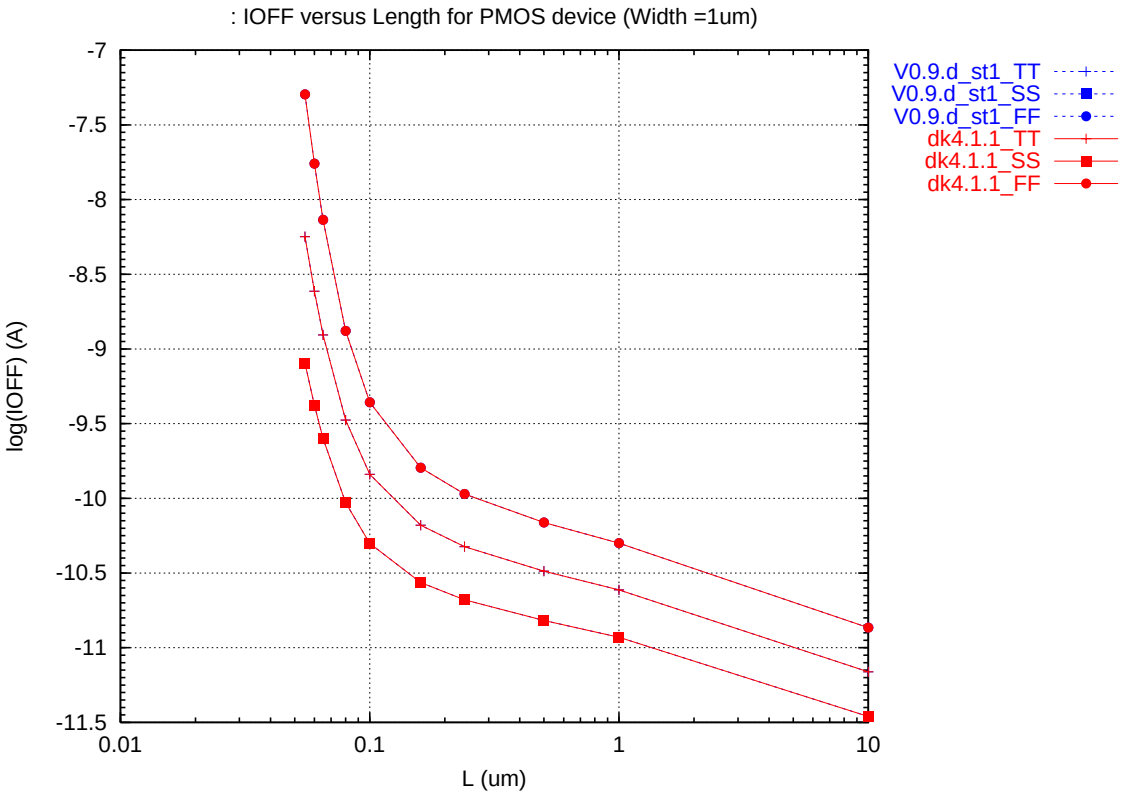

Figure 12 : IOFF versus drawn gate length for PMOS LVT_LP transistors (W = 1 µm)

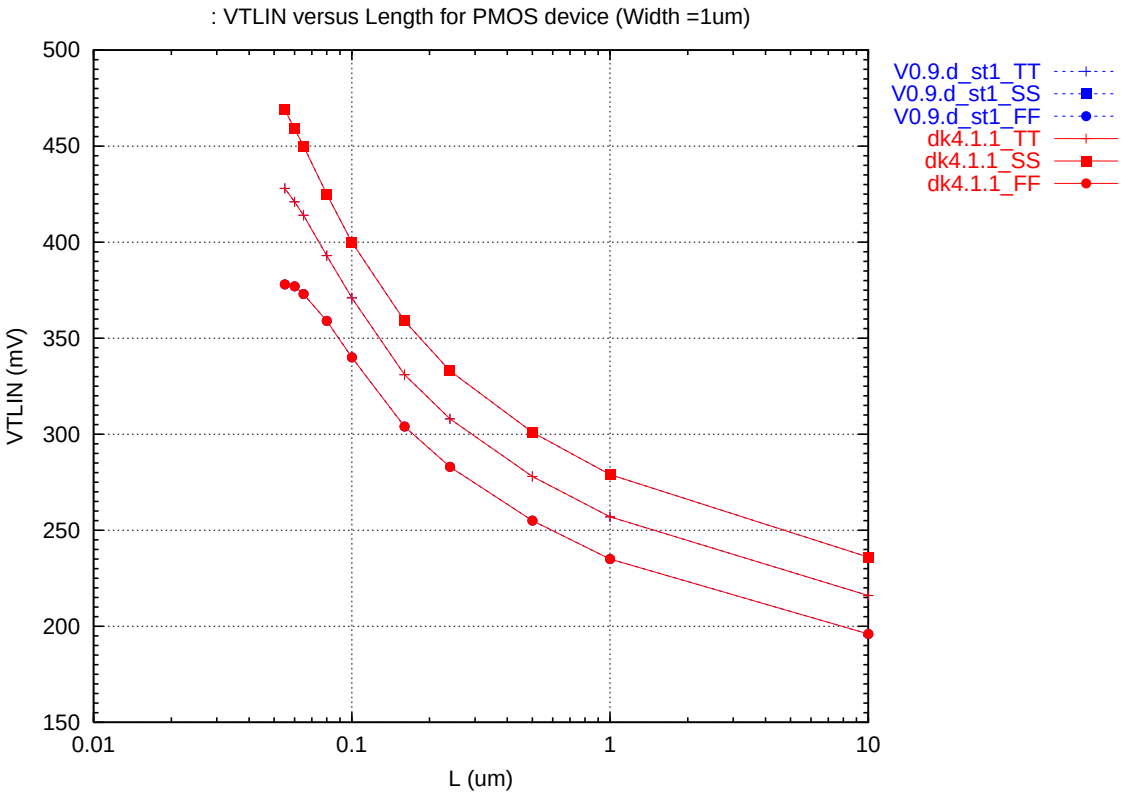

Figure 13 : Threshold voltage VTLIN versus drawn gate length for PMOS LVT_LP transistors (W = 1 µm)

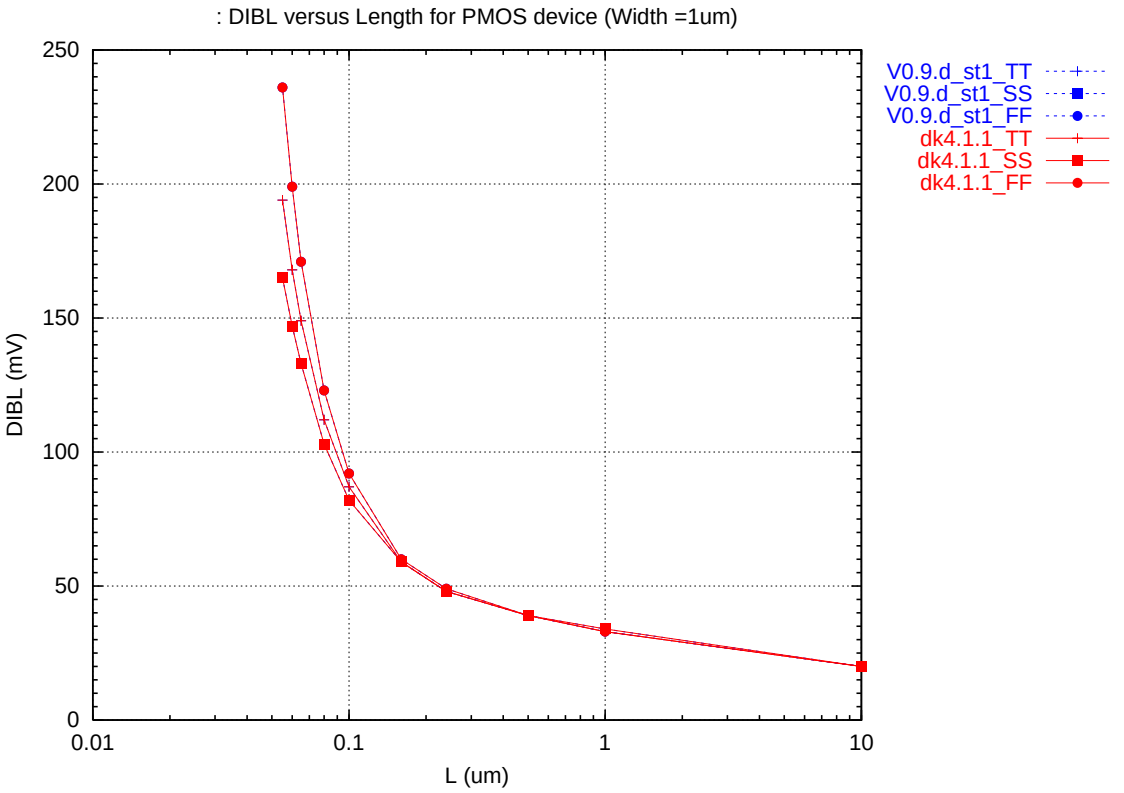

Figure 14 : DIBL= VTLIN-VTSAT versus drawn gate length for PMOS LVT_LP transistors (W = 1 µm)

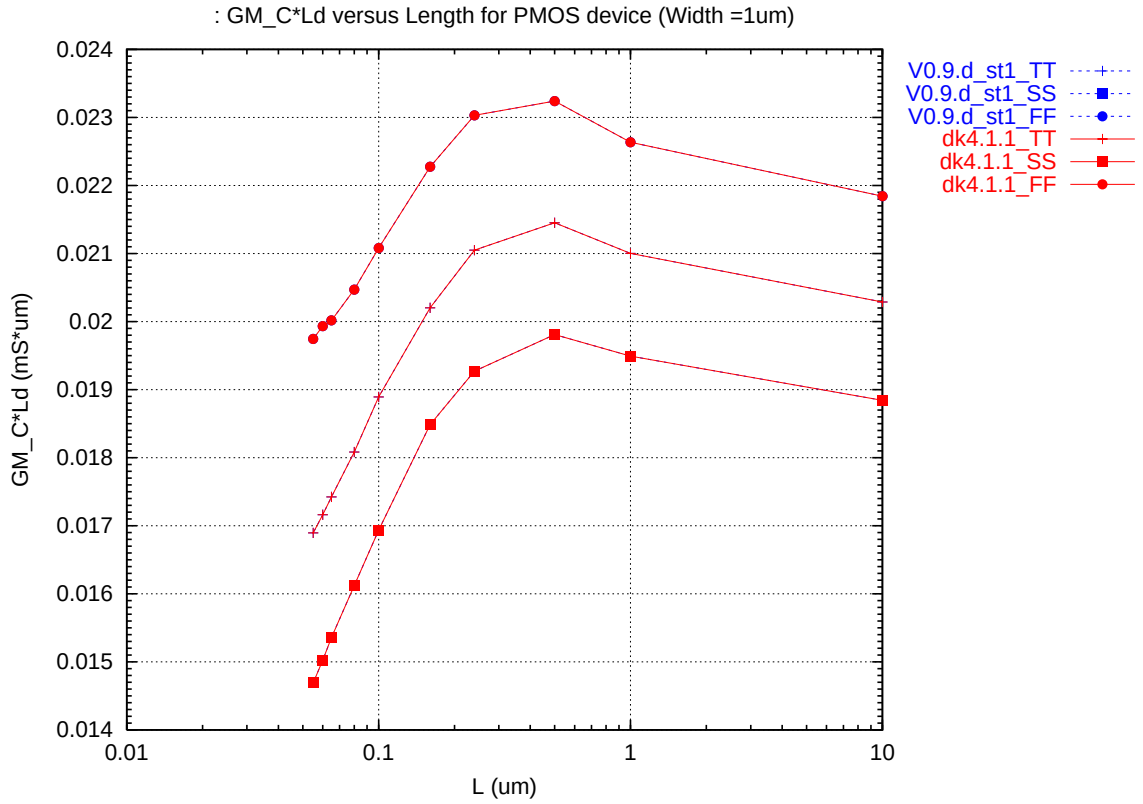

Figure 15 : GM*Ld versus drawn gate length for PMOS LVT_LP transistors (W = 1 µm)

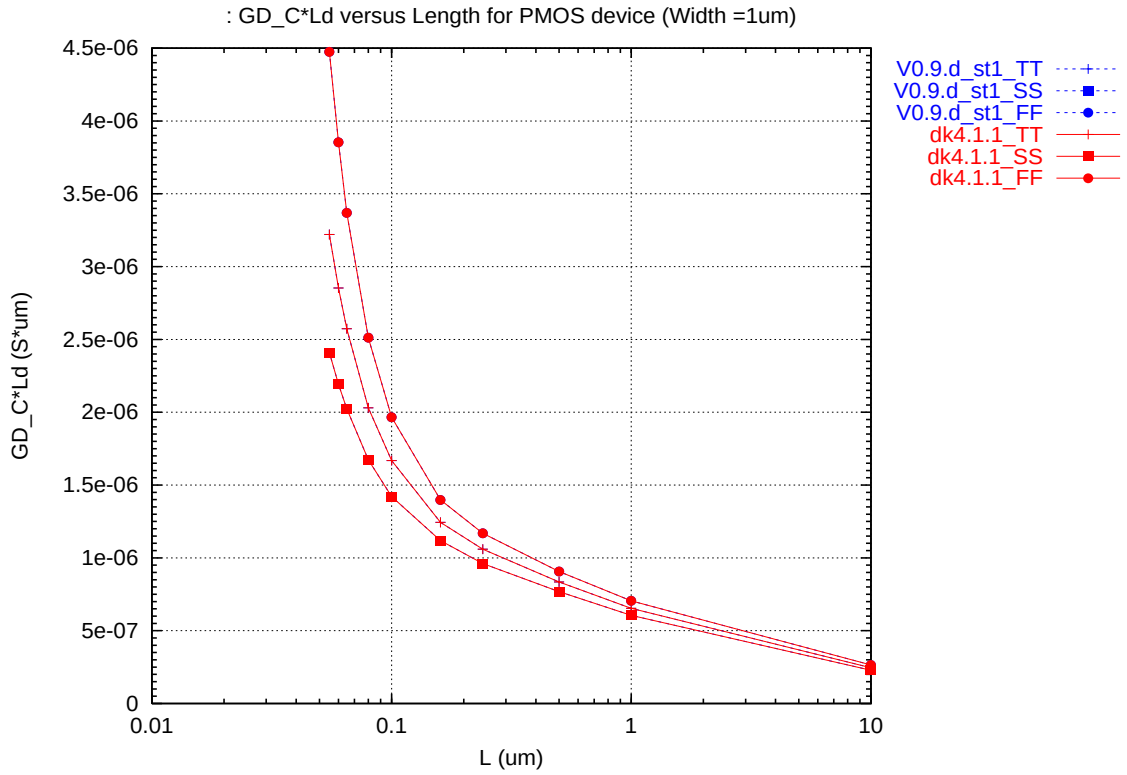

Figure 16 : GD*Ld versus drawn gate length for PMOS LVT_LP transistors (W = 1 µm)

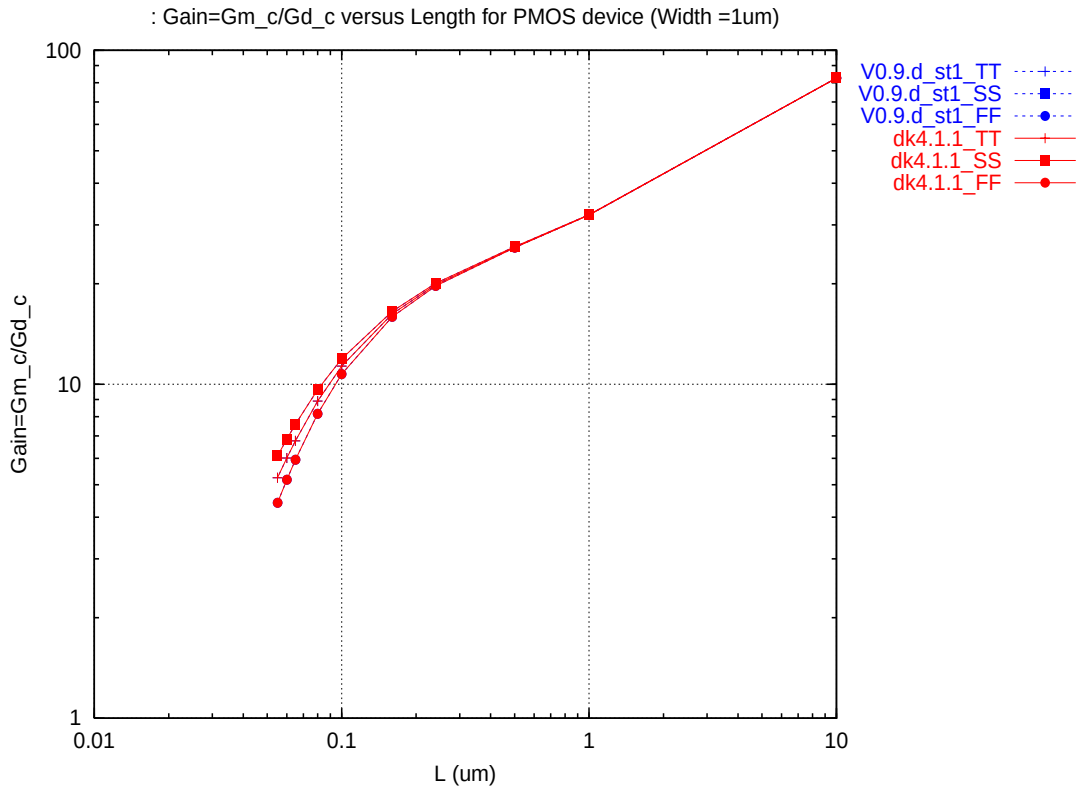

Figure 17 : GAIN versus drawn gate length for PMOS LVT_LP transistors (W = 1 µm)

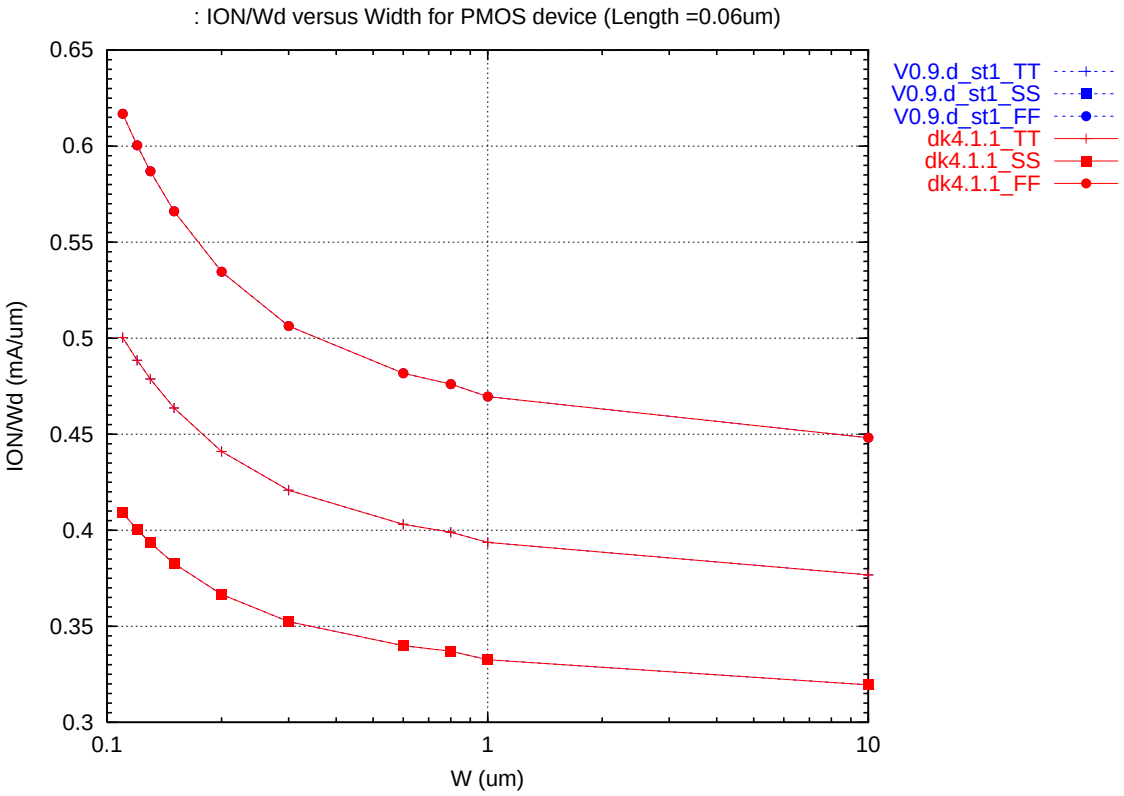

Figure 18 : ION versus drawn channel width for PMOS LVT_LP transistors (L = 0.06 µm)

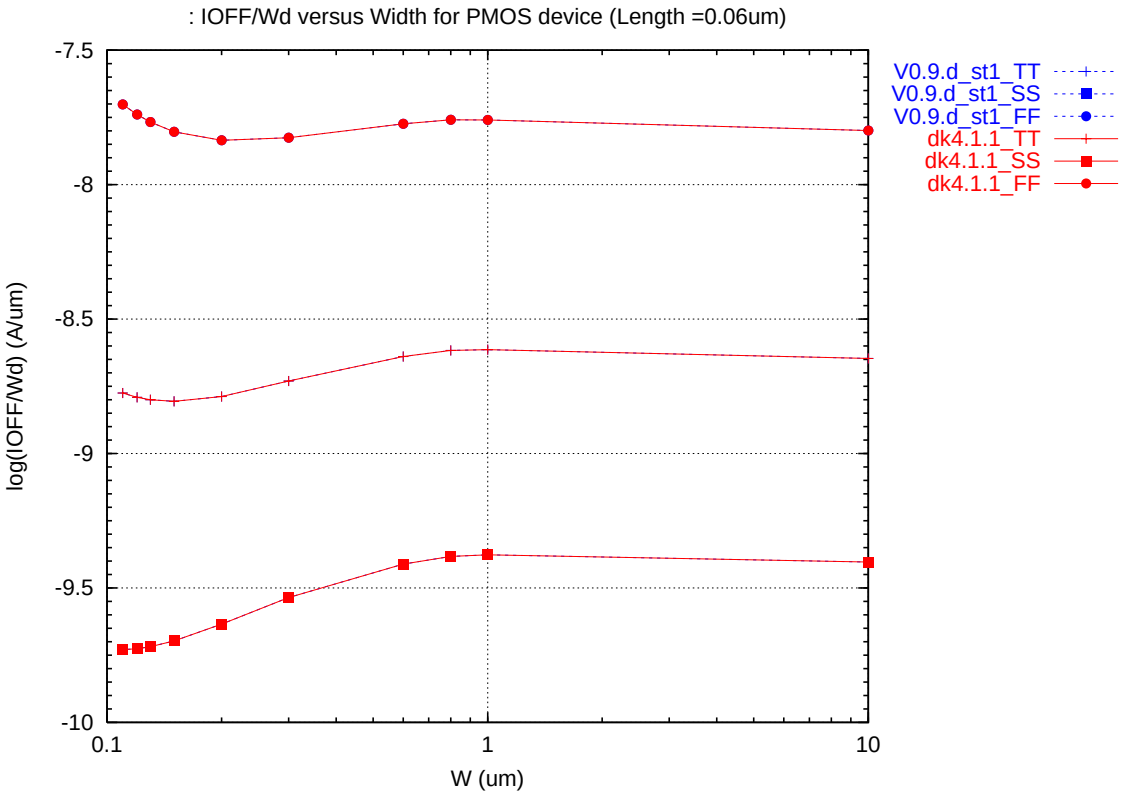

Figure 19 : IOFF versus drawn channel width for PMOS LVT_LP transistors (L = 0.06 µm)

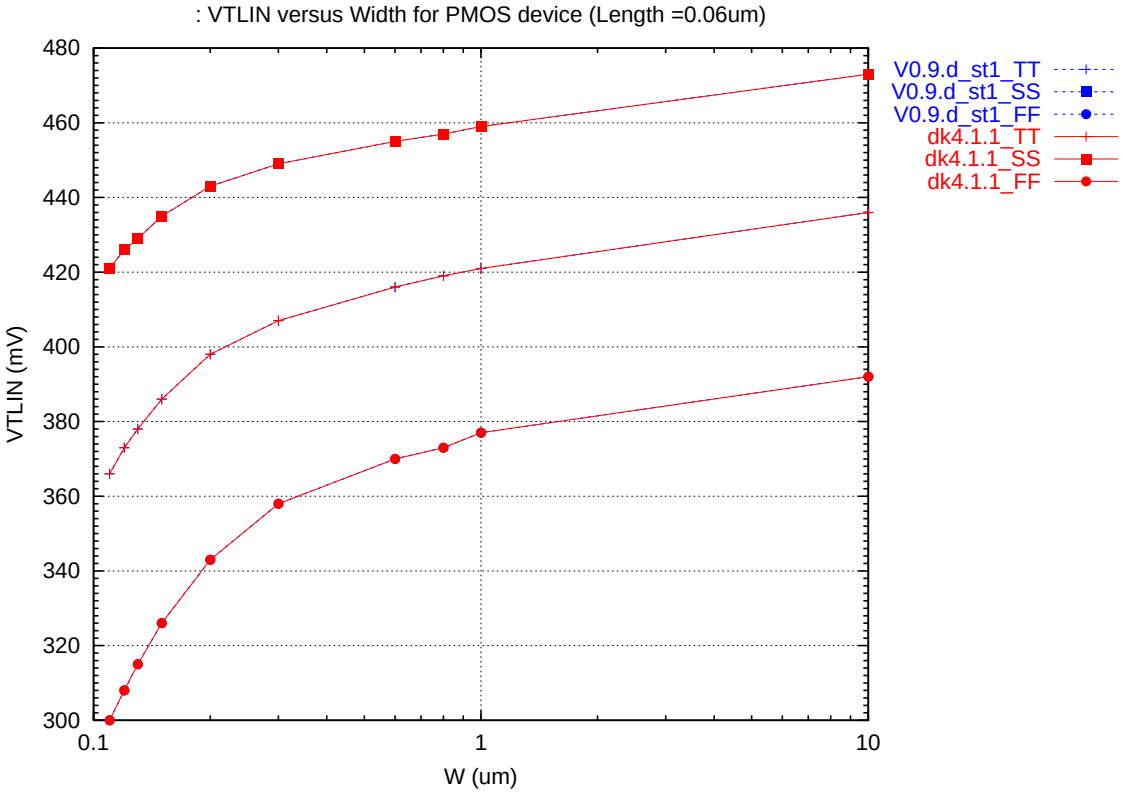

Figure 20 : Threshold voltage VTLIN versus drawn channel width for PMOS LVT_LP transistors (L = 0.06 µm)