Assignment 3: Switched Capacitor Integrators and Filters

Objectives

- Understand the operation and non-idealities of the switched capacitor using a state-of-the art design kit and 65nm CMOS technology.
- To design a discrete-time bandpass filter using switched capacitor integrators and Cadence Analog Artist.

1. Preparation:

Study Chapter 14 in the textbook and the associated course slides.

You will use Cadence Analog Artist with the cmos65nm design kit and the svt MOSFETs from the *cmos065* library in all simulations, as in Assignment 1. You may use the same verilogA model for the opamp as in Assignment 1 or the single-input single-output *amp* cell from the Cadence ahdl library.

2. MOSFET switch simulation and modelling (5 points)

Condider the MOSFET switch test bench in Fig.1.

a) Using the *port* cell from *analogLib* simulate the S-parameters of an SVT n-MOSFET with L=60nm, W_f=1um and N_f=10 from 100 MHz to 10 GHz and extract $C'_{gs}+C'_{sb}$ from *imag*($Y_{11}+Y_{12}$) and $C'_{gd}+C'_{db}$ from *imag*($Y_{22}+Y_{12}$) when the gate and substrate resistances are set to 0.1 Ω and V_C= 0 V, and calculate C_{OFF} per unit gate width as $C'_{OFF} = C'_{gs}+C'_{gd}+C'_{db}+C'_{sb}$. Extract the on-resistance per unit gate width, R'_{ON}, from 1/real(-Y12) when V_C=1.1V.

What is the figure of merit of the switch FoM = $R_{ON}C_{OFF}$? **(3 points)**

b) Repeat a) when the gate and substrate resistances are 10 kΩ. Explain the results and the implications. **(2 points)**

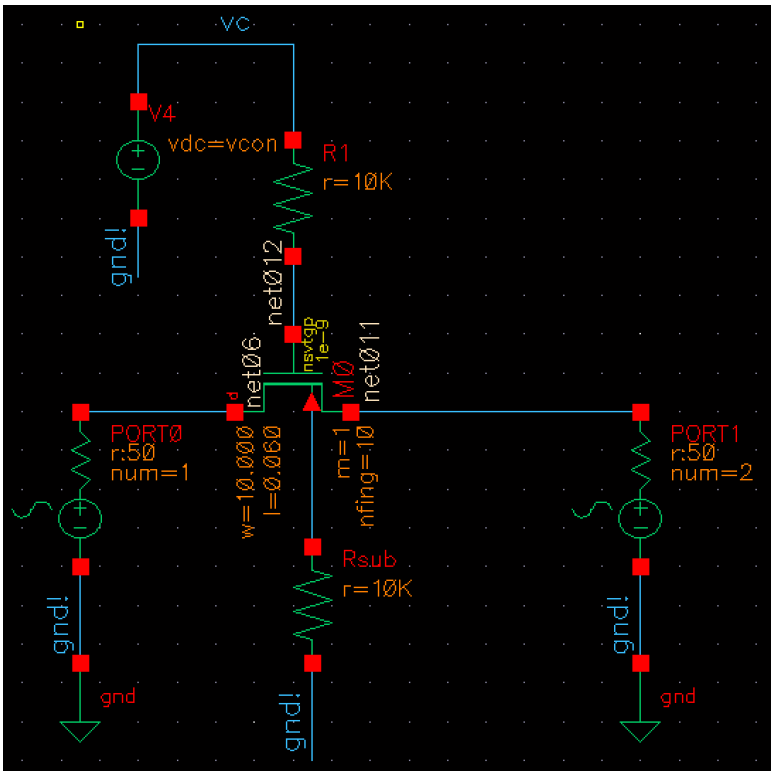

Fig.1 n-MOS switch testbench.

3. Switched capacitor simulation and charge injection (5 points)

Consider the CMOS switched capacitor testbench in Fig.2 with identical-size SVT n-MOSFET and SVT p-MOSFET, each with L=60nm, W_f=1um and N_f=5 and a 200fF

capacitor. The sampling clock signals are 25% duty cycle and are non-overlapping. The clock signal can be as high as 2 GHz.

Simulate the signal waveforms at the input, output, and *store* nodes with an 500mV amplitude sinusoidal input signal at 50 MHz, clocked by a 2 GHz clock. **(1 point)**

What is the maximum error due to charge injection on the held output signal at the store node? **(1 point)**

What is the SDR (signal to distortion) at the output of the circuit? **(1 point)**

How does the maximum error due to charge injection change if the transistor size is increased by a factor of 10 i.e. 50 fingers, each 1um wide? Explain why. **(1 point)**

How do the maximum error due to charge injection and SDR change if the switches are replaced by n-MOSFET switches? Explain. **(1 point)**

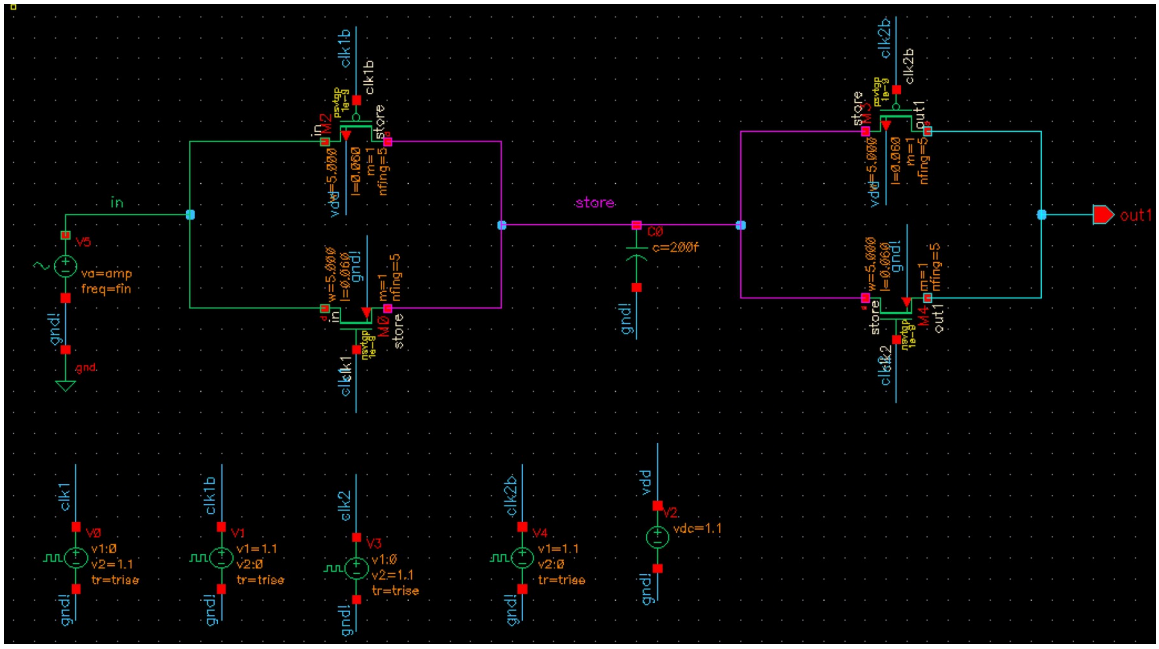

Fig. 2 CMOS switched capacitor test bench.

4. Discrete-Time Bandpass Filter Design (10 points)

Design a bandpass filter with the specification in Table 1 using the Biquad schematic in Fig. 14.28 in the textbook.

a) Provide the *z*-transfer function, schematic with all the component values, and the hand design equations. **(5 points)**

b) Plot the simulated signal waveforms at the input and at the output for an input signal amplitude of 500mV amplitude at the centre frequency. **(2 points)**

c) Plot the output spectrum for a two-tone test at V_{in} = 10mV and V_{in} = 100mV amplitude and calculate the IIP3. **(3 points)**

Table 1

Surname starts with	f_{osc} (GHz)	Q	Gain
A, B, C, D	200 MHz	4	1
E, F, G, H,	220 MHz	6	1
I, J, K, L	180 MHz	8	0.8
M, N, O, P	160 MHz	10	0.9
Q, R, S, T	160 MHz	6	0.9
U,V,X,Y,Z	200 MHz	8	0.8

Supply voltage and control voltage is 1.1V or lower.