22.3 A 20GHz-BW 6b 10GS/s 32mW Time-Interleaved SAR ADC with Master T&H in 28nm UTBB FDSOI Technology

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To sustain ever-growing data traffic, modern wireline communication devices (over copper or fiber optic media) require a high-speed ADC in their receive path to do the digital equalization, or to recover the complex-modulated information. A 6b 10GS/s ADC able to acquire up to 20GHz input signal frequency and showing 5.3 ENOB in Nyquist condition is presented. It is based on a Master Track & Hold (T&H) followed by a time-interleaved synchronous SAR ADC, thus avoiding the need for any kind of skew or bandwidth calibration. Ultra Thin Body and BOX Fully Depleted SOI (UTBB FDSOI) 28nm CMOS technology is used for its fast switching and regenerating capability. The core ADC consumes 32mW from 1V power supply and occupies 0.009mm^2 area. The FoM is 81fJ/conversion step.

An input driver made of a PMOS GmR stage (Fig. 22.3.1) buffers the on-chip 50Ω matched differential input signal. Gm is 25mS and R is 40Ω to keep low impedance driving of the Master T&H. The current consumed in this stage is about 10mA. The high-frequency continuous-time signal is then sampled and held by a 20µm×30nm Low-V_{TH} (LVT) NMOS transistor using 1V Forward Body Bias (FBB) to further reduce its V_{TH} and thus lower its ON resistance (Fig. 22.3.3). A simple "top-plate sampling" scheme is used without the need for any switch bootstrapping or charge-injection cancellation. The sampling capacitor is made of 100fF routing and metal capacitor. During each hold phase, the sampled charges are successively shared with one of the 25fF sampling capacitors of the time-interleaved SARs (Fig. 22.3.2). This eliminates the need for intermediate buffering that would have been difficult to realize under 1V power supply with 50ps half-period for settling time. Signal attenuation penalty is 100fF/125fF, which is acceptable for 6b-resolution ADCs. The 10GHz 0° and 90° external clocks are used to create the 25ps Track pulses. When integrated onto an SoC, they may be derived from a 10GHz quadrature VCO.

A total of 8 clock cycles are needed to do the sampling, the 6b successive approximation, and the reset, leading to a SAR interleaving ratio of 8. Each SAR is made of a compact comb capacitor array, a comparator, and 6b registers. The capacitor array is made of binary-weighted fingers using the minimum pitch of the technology to limit propagation effects in the finger connections [1]. The resulting capacitor array width is less than 7µm. The comparator is made of a preamplifier followed by a clocked inverter [2] that drives a latch (Fig. 22.3.4). The speed performance of the comparator is mainly NMOS-based, and leverages the 1V FBB capability. The latch is not clocked and thus burns some current during its reset phase. As a result, it presents a fast regeneration time of <40ps for input smaller than 0.5mV, ensuring low BER at 10GS/s operation. The 6b registers are made of synchronous logic with a maximum of 4 gates delay in their critical path.

Two reference voltages Vtop and Vbot, together with an intermediate voltage Vc, are embedded on chip. Vc is applied during SAR charge-transfer and reset phases. As described in [3], depending on latch decision, the top plate of each capacitor is switched from Vc to either Vtop or Vbot on the positive side of the capacitor array, and from Vc to either Vbot or Vtop on the negative side of the array. By contrast to the classical 2-reference-voltage "set and correct" successive approximation algorithm, this 2-reference-voltage plus 1-intermediate-voltage "decide right" scheme makes the switching operation symmetrical, drawing the same current from the references whatever the decision is. It results in a very low dependency of the charge drawn from the references as a function of the input voltage, enabling a low-power design for the references (less than 2mA here). Additionally, only 5 capacitors instead of 6 in the classical way are needed to do the 6b quantization.

After quantization, each SAR stores its 6b word in 2 ping-pong 512-word RAMs running at 10GHz/8/2=625MHz. The total 8K words are finally read at low speed through a JTAG controller.

The chip is fabricated in 28nm CMOS UTBB FDSOI technology, using 10 metal layers and MIM capacitors for decoupling. Each SAR occupies 50×13µm^2 (0.0007mm^2) and the complete ADC core is 80×115µm^2 (0.009mm^2). It is mounted in a soft polymeric substrate (PTFE) with a cavity for the die gluing, such that bonding wires are kept as small as possible (Fig. 22.3.7).

Measurement results at 10GS/s are presented in Fig. 22.3.5. Offset mismatch between the 8 SARs is not calibrated on-chip and leads to 1.5dB penalty in dynamic range. In the following results, signal amplitude is thus set at -3dBFS and offset spurs are calibrated off-chip. At 4.8GHz input, ENOB is 5.3 and is thermal-noise limited. ENOB is still 4.6 at 20GHz input, limited by single-ended clock jitter (that can be calculated to 260fs$_{rms}$). THD and SFDR are maintained below 40dB over the whole bandwidth, and they are mainly due to input driver distortion. No gain or skew spurs are visible, demonstrating the efficiency of the Master T&H and the timing accuracy between the Master T&H and the 8 SAR sampling capacitors.

This work compares favorably with [4-7], as depicted in Fig. 22.3.6. It shows 81fJ/conversion step in Nyquist conditions with a very small 0.009mm^2 area and it has up to 20GHz sampling capability without any need for gain & skew calibration, which makes it ideal for further higher-speed interleaving (100Gb/s optical links for instance).

In conclusion, we demonstrate in this work the efficiency of the pure passive "sampling and redistribute" concept for signals up to 20GHz. Together with the low-power capability of the 28nm CMOS UTBB FDSOI technology, we can reach 10GS/s operation while keeping the power consumption at 32mW under 1V supply.

Acknowlegments:
The authors thank Alex Zabroda for initial concept discussions, Philipp Ritter and Martin Müller from Saarland University for module fabrication & chip assembly, and Dimitri Goguet for bench set-up and measurements.

References:
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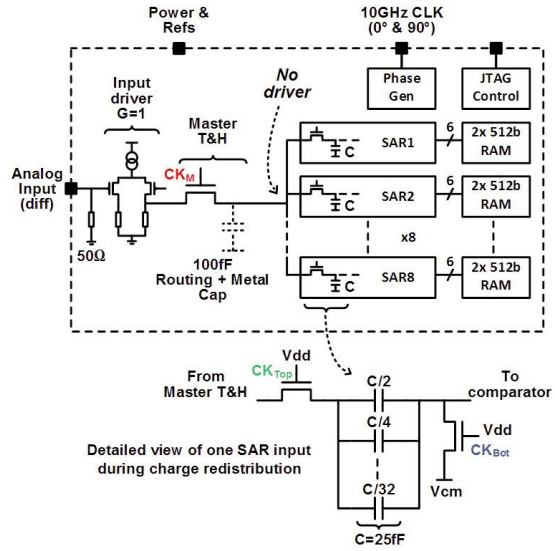

Figure 22.3.1: ADC block diagram.

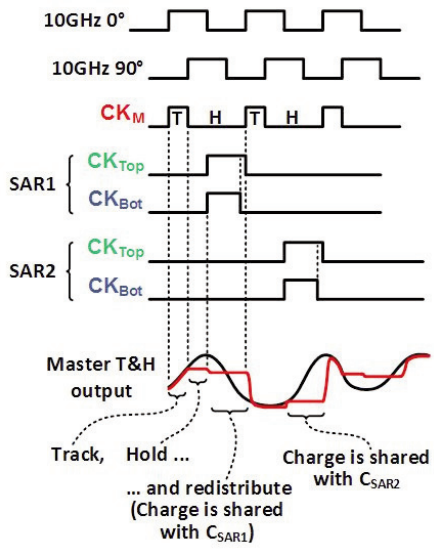

Figure 22.3.2: Master T&H and charge-redistribution timing diagram.

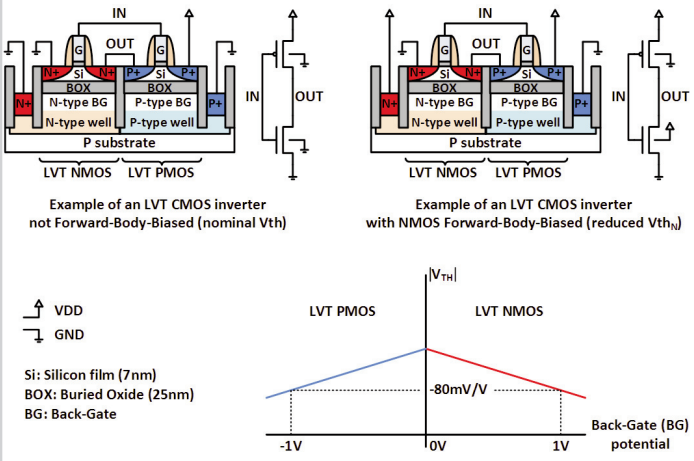

Figure 22.3.3: Fully Depleted Silicon-on-Insulator LVT transistors (flipped-well).

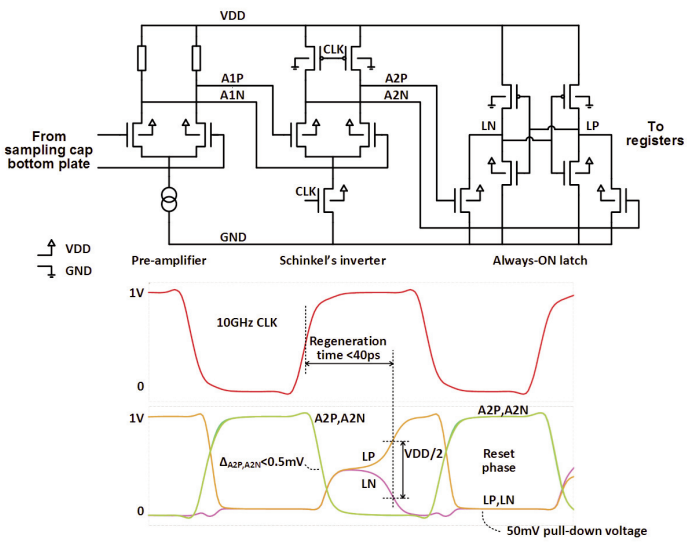

Figure 22.3.4: Comparator schematic.

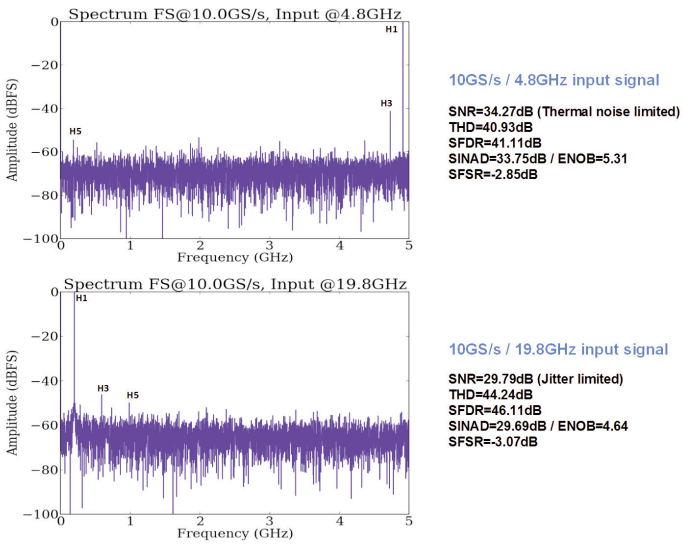

Figure 22.3.5: Output spectrum at 10GS/s.

	JSSC 2011 [4]	ISSCC 2013 [5]	VLSI 2013 [6]	VLSI 2013 [7]	This Work
Technology	65nm CMOS	40nm CMOS	65nm CMOS	32nm SOI	28nm UTBB FDSOI
Architecture	TI-FLASH	TI-FLASH	TI-SAR	TI-SAR	TI-SAR
Power Supply (V)	1.1	0.9	1.1 / 0.9	1	1
Sampling Rate (GS/s)	12	10.3	10	8.8	10
Resolution (bits)	5	6	6	8	6
Power Consumption (mW)	81	240	79.1	35	32
SNDR @ Nyquist (dB)	25.1	33	26	38.5	33.8
Active Area (mm²)	0.44	0.27	0.33	0.025	0.009
FOM @ Nyquist (fJ/conv step)	460	700	480	58	81
Max Input Frequency (GHz)	8	6	4.5	4.2	20
Gain/Skew Calibration	Yes	Yes	Yes	Yes	No

Figure 22.3.6: Performance summary and state-of-the-art comparison.

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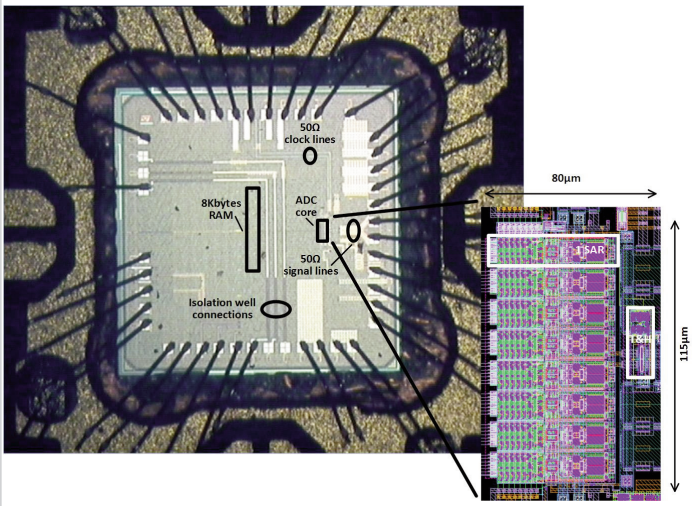

Figure 22.3.7: Die photo in its chip-on-board cavity

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