# 1. POST LAYOUT EXTRACTION: RC MODELS

## 1.1 Purpose

The Post layout extraction flow is aimed to provide spice transistor flat netlist back annotated with parasitic C's and R's extracted on interconnections. This flow is based on Calibre-StarRCXT tools.

RCmodels represent the analytical models used on the fly by starRCXT to compute the Resistances and capacitances. RCmodels computation is based on the interconnect stack parameters described in the DRM.

## 1.2 Extraction corners

To cover the potential process deviation, 7 process corners are proposed:

- RCTYP: typical resistors and capacitors
- RCMIN: best resistors and capacitors
- RCMAX: worst resistors and capacitors
- CMIN: best capitulates
- CMAX: worst capacitors
- XTLK: worst crosstalk configuration
- DLY: worst delay configuration

Process corners are defined by the combination of the lines thickness, lines width, dielectric thickness and permittivity, metal sheet resistance, temperature coefficient and via resistance as summarized in Table 1. For each parameter the typical value and the deviation is mentioned in the DRM.

| Corner | Metal thick | Metal width | Via thick. | Via res. | Metal res. | K_intra | K_inter | Temperature (2) | |
|---|---|---|---|---|---|---|---|---|---|
| RCTYP | typ | typ | typ | typ | typ | typ | typ | typ | 25 |
| RCMIN | min | min | max | min | min | min | min | typ | 25 |
| RCMAX | max | max | min | max | max | max | max | typ | 25 |
| CMIN | min | min | max | min | max (1) | min | min | min | -40 |
| CMAX | max | max | min | max | min (1) | max | max | max | 125 |
| XTLK | max | max | max | min | min (1) | max | min | min | -40 |
| DLY | min | min | min | max | max (1) | min | max | max | 125 |

**Table 1 : Process corners parameters**

(1) The sheet resistance value is correlated to the line thickness.

(2) The temperature effect on the sheet resistance is: Rsh' = Rsh . (1+ Tcoeff . ΔT)

Tcoeff is specified in the DRM.

To select one of proposed corners the user had to set the corresponding starRCXT library in the command file such as:

TCAD_GRD_FILE: RCTYP.nxtgrd
TCAD_GRD_FILE: RCMIN.nxtgrd
TCAD_GRD_FILE: RCMAX.nxtgrd
TCAD_GRD_FILE: CMIN.nxtgrd
TCAD_GRD_FILE: CMAX.nxtgrd
TCAD_GRD_FILE: XTLK.nxtgrd
TCAD_GRD_FILE: DLY.nxtgrd

## 2. POLY AND SUBSTRATE LAYERS

As far as POLY and substrate layers are concerned, we have to deal with the non planarity of the substrate. Figure 1: and Figure 2: respectively illustrate the real cross-section of the susbtrate and the cross-section supported by starRCXT (*).

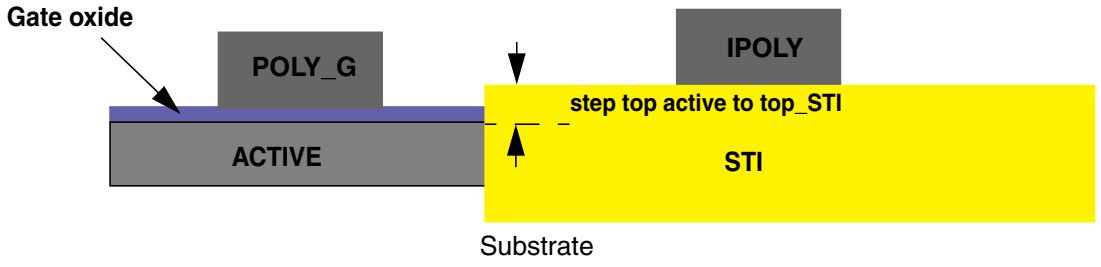


Figure 1: Substrate cross-section (POLY_G : gate ; IPOLY: interconnect POLY)

Figure 2: RCmodels substrate cross-section

The key points of the starRCXT representation are:

- the step beween top of ACTIVE and top of STI is not described. Indeed, description of this step assumes to make the distinction between POLY_gate and Interconnect POLY both at LVS and at ITF level which is very painful compared to the impact on the capacitances. On top of that, the capacitances related to the gate will not be computed by starRCXT but supported by the device Model.

- The ACTIVE thickness is assumed to be half of the STI thickness. This estimation is done to be consistent with MOS models as this dimension is theoretically dependent of the current in the device

*(*) The substrate description supported is a technical decision and not a limitation of the tool Star-RCXT.*

## 3. SPECIAL CONNECTIVITY LAYERS

As a general rule, it is mandatory for the calibre-starRCXT flow to have 1-to-1 mapping between layers involved into calibre data base and physical nxtgrd layers.

So, we need to add specific layers into nxtgrd file to have correct extraction and netlisting of devices embedded in the interconnect stack such as the MIM capacitor, the DRAM mos or the SRAM devices.

Implementation of these devices into RCmodels is detailed below.

### 3.1 MIM capacitor

The MIM capacitor was stacked between te last thick metal level and the alucap until the DRM revision C. Since DRM revision D, the MIM take place under the first thick metal level.

- the high K dielectrics related to the MIM are replaced by the surrounding oxide. The impact of this approximation is very limited as the parasitic between MKTOPMIM and BOTMIM are not computed by the Post-layout tool but come from the device model.

### 3.2 DRAM layers

In order to support DRAM devices in Post-layout extraction specific layers and vias have been added into RCmodels to maintain consistency between LVS and starRCXT. Figure 3: illustrates the stack used for DRAM layers.

Because no parasitics need to be extracted on DRAM layers (device model used) and because DRAM process assumes larger POLY to METAL1 distance, none physical dimensions are used for ELEC1,ELEC2 conductors and CTELEC2_FINAL, LILTACT_FINAL and LILINTPOL_FINAL vias i.e:

- closed to zero sheet resistances and resistances;

- 0.01 um thickness for ELEC1, ELEC2 and CTELEC2_FINAL layers.

### 3.3 SRAM layers

The same approach as for DRAM is used for SRAM (cf. Figure 3:). The layers added are:

- SRAM_INTER with null sheet resistance and 0.01um of thickness. Please note that this conductor is co-vertical with the POLY.

- CT_SRAM_INTER and CT_SRAM_OD vias with null resistance.

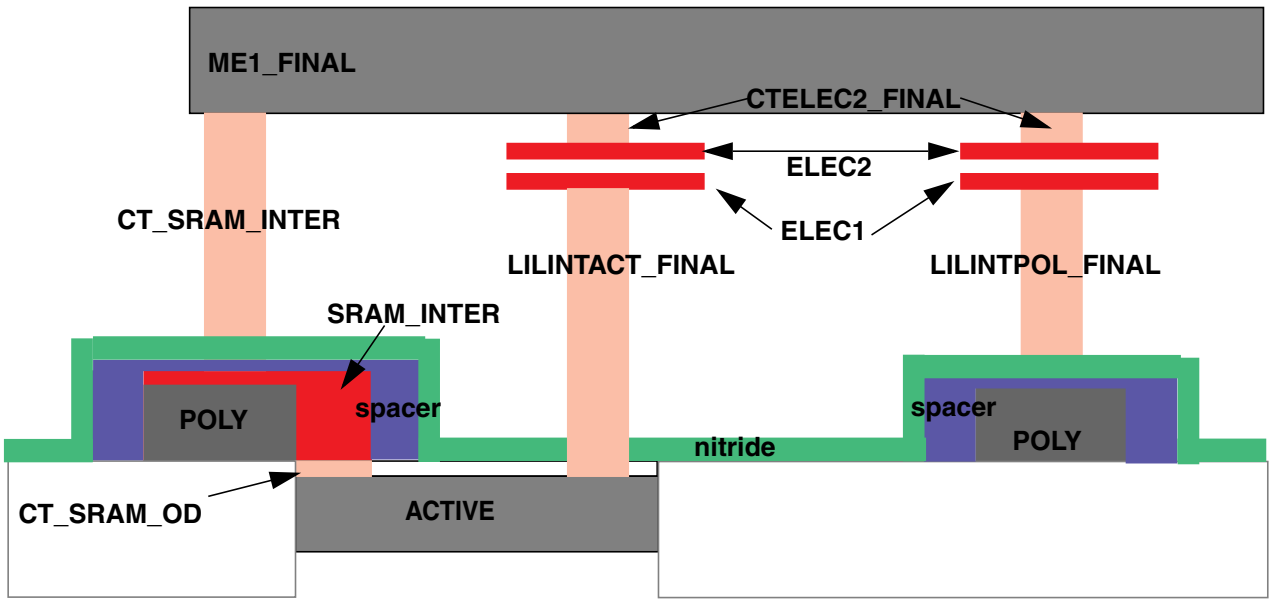


Figure 3: DRAM and SRAM layers

## 4. ISOLATED LINES UPSIZING

The purpose is to reproduce the oversizing of the isolated lines done at mask level to enable lithography operations. It impacts both resistances and capacitances computation for Metal1 and thin metal levels. Upsizing is modelled with ETCH_VS_WIDTH_AND_SPACING function. To be consistent with CD biasing involved in Capacitance computation , model used for C is such as:

- Upsizing for Capacitance computation: ETCH_VS_WIDTH_AND_SPACING

The associated values correspond to ΔCD(biasing)+ΔCD(upsizing)

The point is that ETCH_VS_WIDTH_AND_SPACING values should be properly defined to fit with the step by step behavior of the upsizing. So, the implementation is done as follow :

1- upsizing is applied from min width to 0.15um width in 3 steps: below 0.115um width, between 0.115um and 0.13um width and between 0.13um and 0.15um width.

2- upsizing correction is applied by step of space such as for metal x levels:

2nm correction on width per side for a space smaller than 0.13um

4nm correction on width per side for a space greater or equal than 0.13um and smaller than 0.15um

7nm correction on width per side for a space greater or equal than 0.15um and smaller than 0.17um

....

Translation in StarRCXT language gives:

```
ETCH_VS_WIDTH_AND_SPACING {
    SPACINGS    { 0.100 0.129 0.130 0.149 0.150 ....}
    WIDTHS      { 0.100 0.114 0.115 0.129 0.130 0.149 0.150 0.200}
    VALUES      {-0.002 -0.002 -0.004 -0.004 -0.007 ...
                 -0.002 -0.002 -0.004 -0.004 -0.007  ...}
```

Note:

VALUES is a function of W and S (W as rows, and S as columns)

## 5. SHEET RESISTANCE FUNCTION OF THE WIDTH

Due to dimensions decreasing of copper lines, the sheet resistance is now a function of the width. The sheet resistance decrease when the width of the lines increase.

The corresponding starRCXT function is: RPSQ_VS_SI_WIDTH. This function can be used with the ETCH_VS_WIDTH_AND_SPACING function because the RPSQ evaluation take effect after the

etching operation. So the extractor know the width of a line on silicon and replace the sheet resistance by the right value.

Metal1 typical corner is illustrated below:

DRM value for W<0.16um Rspq= 195 mOhm/sq

DRM value for W>= 0.16um Rspq = 145 mOhm/sq

This fonction in StarRCXT language is taking into account as follow :

RPSQ_VS_SI_WIDTH {(0.100,0.155) (0.159,0.155) (0.160,0.115) (12.0,0.115)}

## 6. TEMPERATURE DERATING

As the sheet resistance of the lines depends on the temperature, temperature derating coefficients (CRT) are implemented fo rmetal1 and thin metal levels of interconnects.

It allows the PLS user to specify an operating temperature and obtain corrected parasitic resistances such as:

$$R(T_{operating}) = R(T_{25}) . [ 1 + ( T_{operating} - 25).CRT ]$$

with $T_{25}$ = ambient temperature i.e. 25 degrees

Please note, that only one operating temperature can by specified and will applied on all interconnect levels where CRT is defined (i.e. for metal1 and thin metal levels only).

The CRT values came from reliability measurement.

## 7. IDEAL VIA CONNECTIONS

The constraint of 1-to-1 mapping between LVS connectivity data base and RCmodels, associated to the respect of LPE flag in devices leads to have ideal vias connections between lower conductors and substrate layers.

These ideal vias should have a resistance close to zero but should not be small to avoid simulator crashes. Indeed, spectre simulator can not support very small resistor values.

The work-around is to use a small values for the parameters AREA and RPV to obtain a resistance for these vias equal to 0.001Ohm.

For cmos065 technology only the STRAP Via between ACTIVE conductor and the reference layer (SUBSTRATE) is impacted.