SVT_LP MODELS (NSVTLP, PSVTLP)

1. CONDITIONS OF EXTRACTION

- Maturity: Pre-Production
- Model parameters extraction based on lot : Q539TVB
- Geometrical extraction domain:
  - Drawn gate length : 10.0 ≥ L ≥ 0.06 µm
  - Drawn transistor width : 10 ≥ W ≥ 0.12 µm
- Temperature extraction domain: -40 ˚C to 150 ˚C
- Bias extraction domain:
  - Gate bias: 0 ≤ |VGS| ≤ 1.32 V (VDD + 10%)
  - Drain bias: 0 ≤ |VDS| ≤ 1.32 V (VDD + 10%)
  - Bulk bias: 0 ≤ |VBS| ≤ 1.32 V (VDD + 10%)

2. CONDITIONS OF SIMULATION

- Temperature: 25 ˚C
- Currents:

  IDLIN = Ids at Vgs = 1.2 V, Vds = 50 mV and Vbs = 0 V

  ION = Ids at Vgs = 1.2 V, Vds = 1.2 V and Vbs = 0 V

  IOFF = Ids at Vgs = 0 V, Vds = 1.2 V and Vbs = 0 V

  IG_ON = Igs at Vgs = 1.2 V and Vd= Vs = Vb = 0 V

  IG_OFF = Igs at Vgs =Vbs = 0 V and Vds = 1.2 V
- Threshold voltage in linear and saturation regime

  VTLIN is Vgs value at Vds = 50 mV, Vbs = 0 V and Ids= 40*W/L nA.

  VTSAT is Vgs value at Vds = 1.2 V, Vbs = 0 V and Ids= 40*W/L nA.
- Current derivatives:

$$Gm = \frac{\partial}{\partial V_{gs}} Ids$$ at Vgs = VTLIN + 0.2 V, Vds = 0.6 V and Vbs = 0 V

$$Gd = \frac{\partial}{\partial V_{ds}} Ids$$ at Vgs = VTLIN + 0.2 V, Vds = 0.6 V and Vbs = 0 V

Analog gain = Gm/Gd

- Gate Capacitances:

  CGGINV = CGG at Vgs = 1.2 V, Vds = 0 V and Vbs = 0 V

  CGD_0V = CGD at Vgs = 0 V, Vds = 0 V and Vbs = 0 V

  $$CGGMEAN = \frac{1}{VDD} \cdot \int_{0}^{VDD} CGG \times dVgs$$ with VDD = 1.2 V and Vbs = 0 V

  TAU = CGGMEAN*VDD/ION

- Diode Capacitances:

  CBD OFF = CBD at Vgs = 0 V, Vds = 1.2 V and Vbs = 0 V

  Note: the area and perimiters of source/drain junction diodes used for simulation are defined with the the minimum poly-to-active distance specified in the DRM.

- Transition frequency:

  FT = frequency for which the small signal current gain H_{21} is 0 dB (i.e. $\left|\frac{I_d}{I_g}\right|$ = 0 dB).

3. MAIN ELECTRICAL CHARACTERISTICS OF NMOS SVT_LP TRANSISTORS

PARAMETERS	SVTLP_TT	SVTLP_SS	SVTLP_FF	units
N-channel transistors (nsvtlp)				
VTLIN W=1/L=10.0	263	283	242	mV
IDLIN W=1/L=10.0	1.22e-06	1.14e-06	1.31e-06	A
VTSAT W=1/L=10.0	252	273	231	mV
ION W=1/L=10.0	9.87e-06	8.91e-06	1.09e-05	A
VTLIN W=1/L=0.06	433	485	368	mV
IDLIN W=1/L=0.06	9.54e-05	8.06e-05	1.14e-04	A
VTSAT W=1/L=0.06	302	369	217	mV
ION W=1/L=0.06	6.13e-04	5.04e-04	7.59e-04	A
IOFF W=1/L=0.06	3.61e-10	5.07e-11	3.84e-09	A
IG_ON W=1/L=0.06	5.58e-12	2.80e-12	1.13e-11	A
IG_OFF W=1/L=0.06	1.00e-12	4.97e-13	2.03e-12	A
FT W=1/L=0.06	1.62e+11	1.42e+11	1.87e+11	Hz
CGGinv W=1/L=0.06	1.17e-15	1.23e-15	1.10e-15	F
CGGmean W=1/L=0.06	1.01e-15	1.03e-15	9.82e-16	F
CGD 0V W=1/L=0.06	3.88e-16	3.83e-16	3.97e-16	F
CBD OFF[a] W=1/L=0.06	4.57e-16	5.17e-16	3.95e-16	F
Tau W=1/L=0.06	2.0	2.5	1.6	ps
Gm W=1/L=0.06	3.87e-04	3.49e-04	4.30e-04	S
Gd W=1/L=0.06	5.06e-05	3.98e-05	6.63e-05	S
Gain W=1/L=0.06	7.64e+00	8.78e+00	6.49e+00	
VTLIN W=0.12/L=0.06	379	429	317	mV
IDLIN W=0.12/L=0.06	1.27e-05	1.06e-05	1.53e-05	A
VTSAT W=0.12/L=0.06	288	347	215	mV
ION W=0.12/L=0.06	8.43e-05	6.92e-05	1.04e-04	A
IOFF W=0.12/L=0.06	6.18e-11	1.09e-11	4.85e-10	A
FT W=0.12/L=0.06	1.27e+11	1.12e+11	1.45e+11	Hz

Table 1: Main electrical characteristics for NMOS

a. Value coresponding to the minimum poly-to-acvtive distance specified in the DRM

4. MAIN ELECTRICAL CHARACTERISTICS OF PMOS SVT_LP TRANSISTORS

PARAMETERS	SVTLP_TT	SVTLP_SS	SVTLP_FF	units
P-channel transistors (psvtlp)				
VTLIN W=1/L=10.0	345	366	325	mV
IDLIN W=1/L=10.0	4.01e-07	3.72e-07	4.31e-07	A
VTSAT W=1/L=10.0	336	357	316	mV
ION W=1/L=10.0	3.22e-06	2.90e-06	3.57e-06	A
VTLIN W=1/L=0.06	479	509	448	mV
IDLIN W=1/L=0.06	3.76e-05	3.27e-05	4.32e-05	A
VTSAT W=1/L=0.06	347	391	298	mV
ION W=1/L=0.06	3.11e-04	2.66e-04	3.61e-04	A
IOFF W=1/L=0.06	9.96e-11	2.30e-11	4.98e-10	A
IG_ON W=1/L=0.06	1.46e-12	7.30e-13	2.93e-12	A
IG_OFF W=1/L=0.06	4.89e-13	2.36e-13	1.02e-12	A
FT W=1/L=0.06	8.19e+10	7.31e+10	9.16e+10	Hz
CGGinv W=1/L=0.06	1.19e-15	1.25e-15	1.12e-15	F
CGGmean W=1/L=0.06	1.01e-15	1.04e-15	9.76e-16	F
CGD 0V W=1/L=0.06	3.57e-16	3.54e-16	3.62e-16	F
CBD OFF[a] W=1/L=0.06	4.34e-16	4.89e-16	3.77e-16	F
Tau W=1/L=0.06	3.9	4.7	3.2	ps
Gm W=1/L=0.06	2.70e-04	2.40e-04	3.06e-04	S
Gd W=1/L=0.06	3.76e-05	3.03e-05	4.78e-05	S
Gain W=1/L=0.06	7.18e+00	7.92e+00	6.39e+00	
VTLIN W=0.12/L=0.06	404	441	364	mV
IDLIN W=0.12/L=0.06	5.84e-06	5.02e-06	6.80e-06	A
VTSAT W=0.12/L=0.06	315	359	267	mV
ION W=0.12/L=0.06	4.83e-05	4.09e-05	5.69e-05	A
IOFF W=0.12/L=0.06	1.23e-11	2.88e-12	6.14e-11	A
FT W=0.12/L=0.06	6.72e+10	6.01e+10	7.48e+10	Hz

Table 2: Main electrical characteristics for PMOS

a. Value coresponding to the minimum poly-to-acvtive distance specified in the DRM

5. ELECTRICAL BEHAVIOR VERSUS GATE LENGTH AND CHANNEL WIDTH FOR NMOS SVT_LP TRANSISTORS

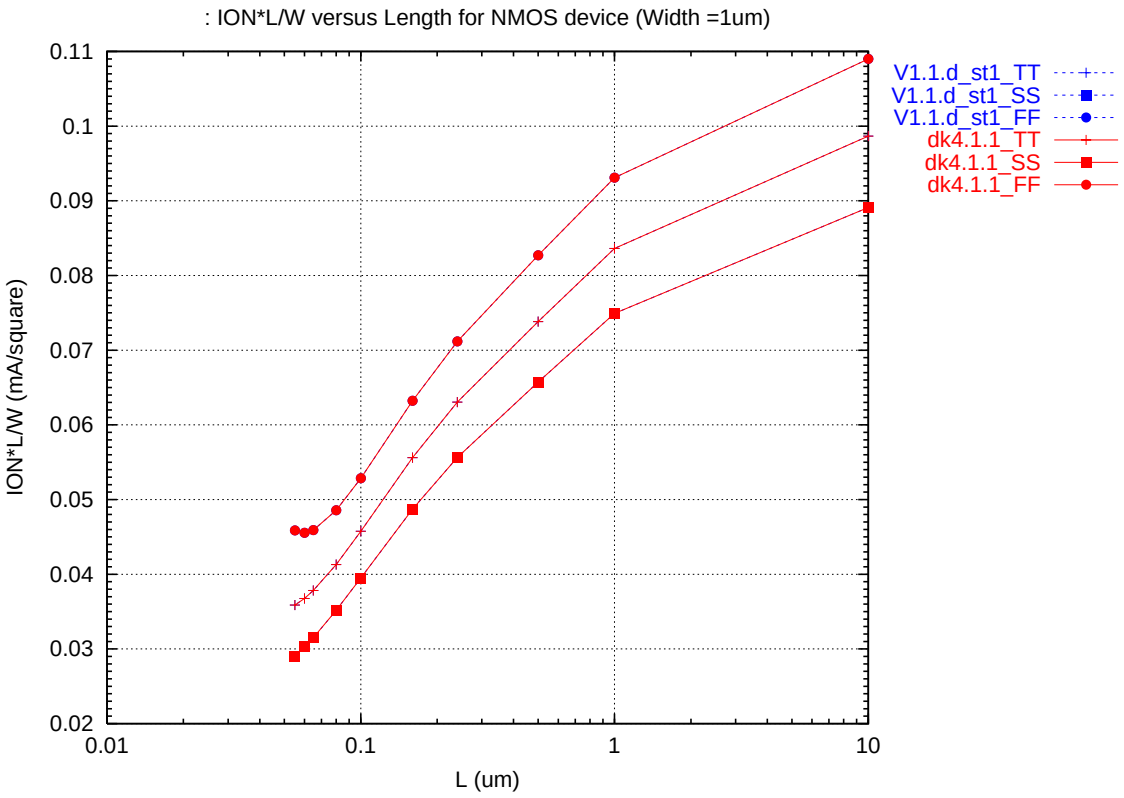

Figure 1 : ION/❑=ION*L/W versus drawn gate length for NMOS SVT_LP transistors (W = 1 µm)

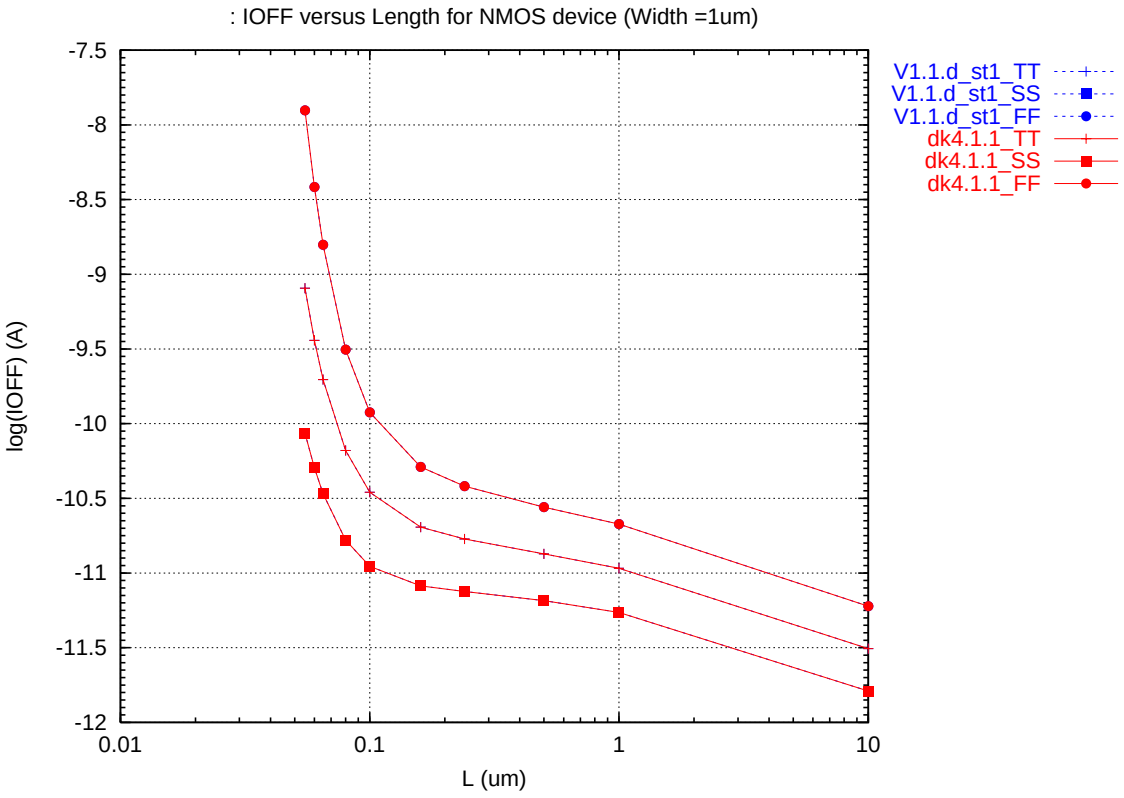

Figure 2 : IOFF versus drawn gate length for NMOS SVT_LP transistors (W = 1 µm)

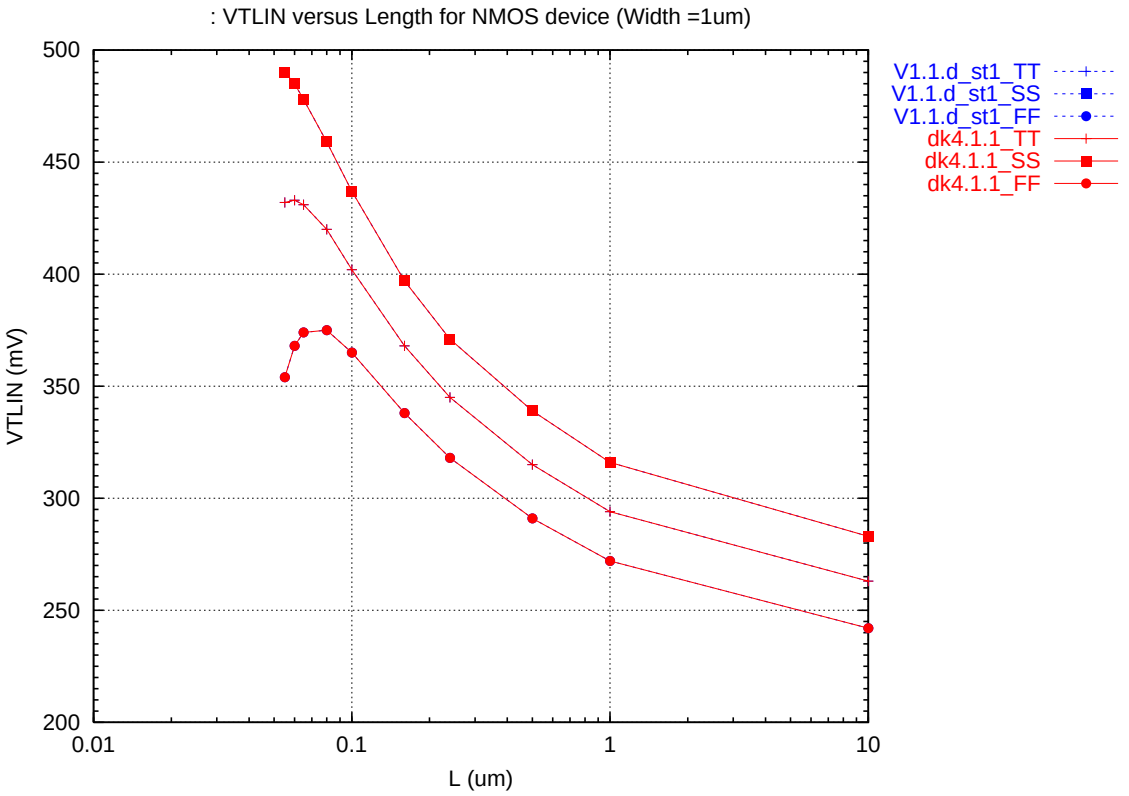

Figure 3 : Threshold voltage VTLIN versus drawn gate length for NMOS SVT_LP transistors (W = 1 µm)

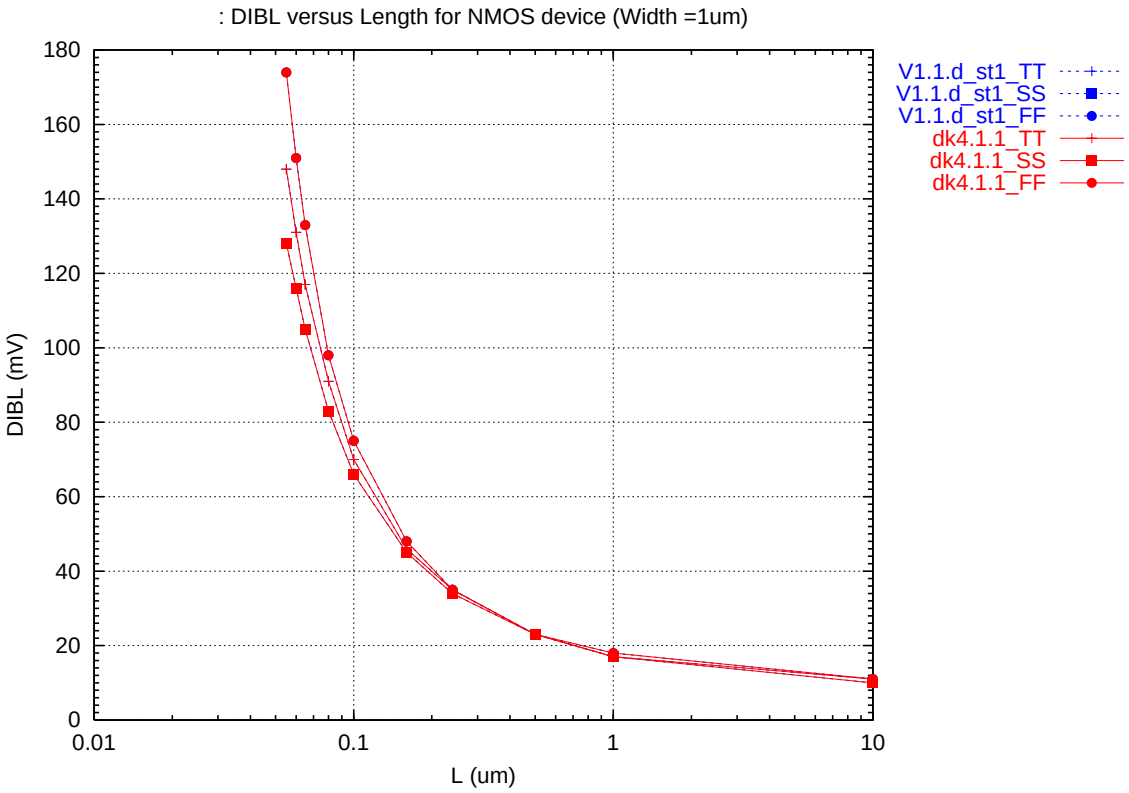

Figure 4 : DIBL= VTLIN-VTSAT versus drawn gate length for NMOS SVT_LP transistors (W = 1 µm)

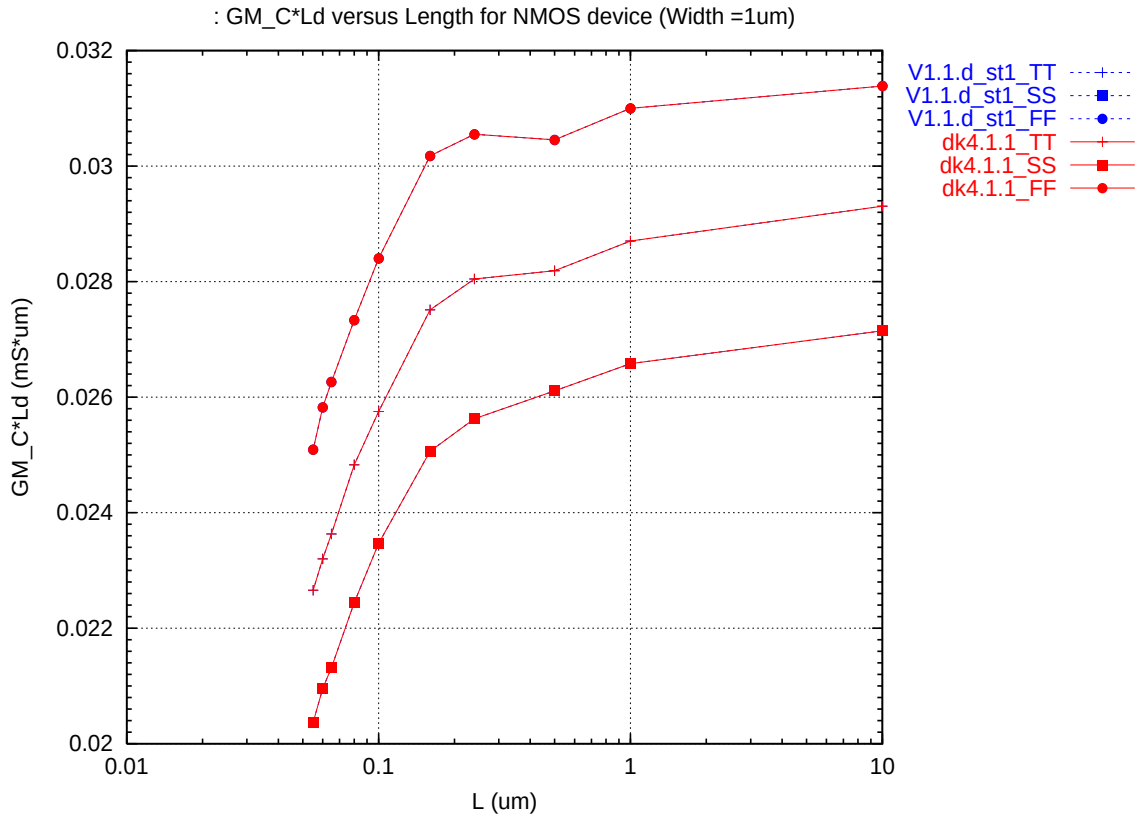

Figure 5 : GM*Ld versus drawn gate length for NMOS SVT_LP transistors (W = 1 µm)

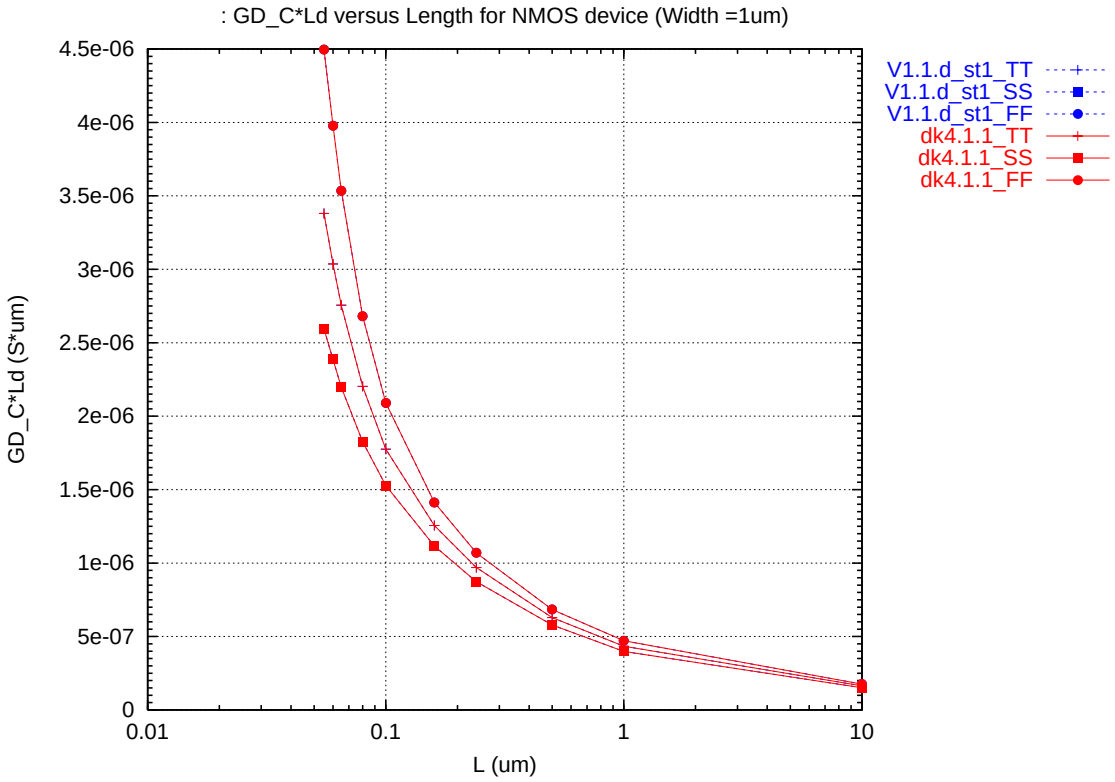

Figure 6 : GD*Ld versus drawn gate length for NMOS SVT_LP transistors (W = 1 µm)

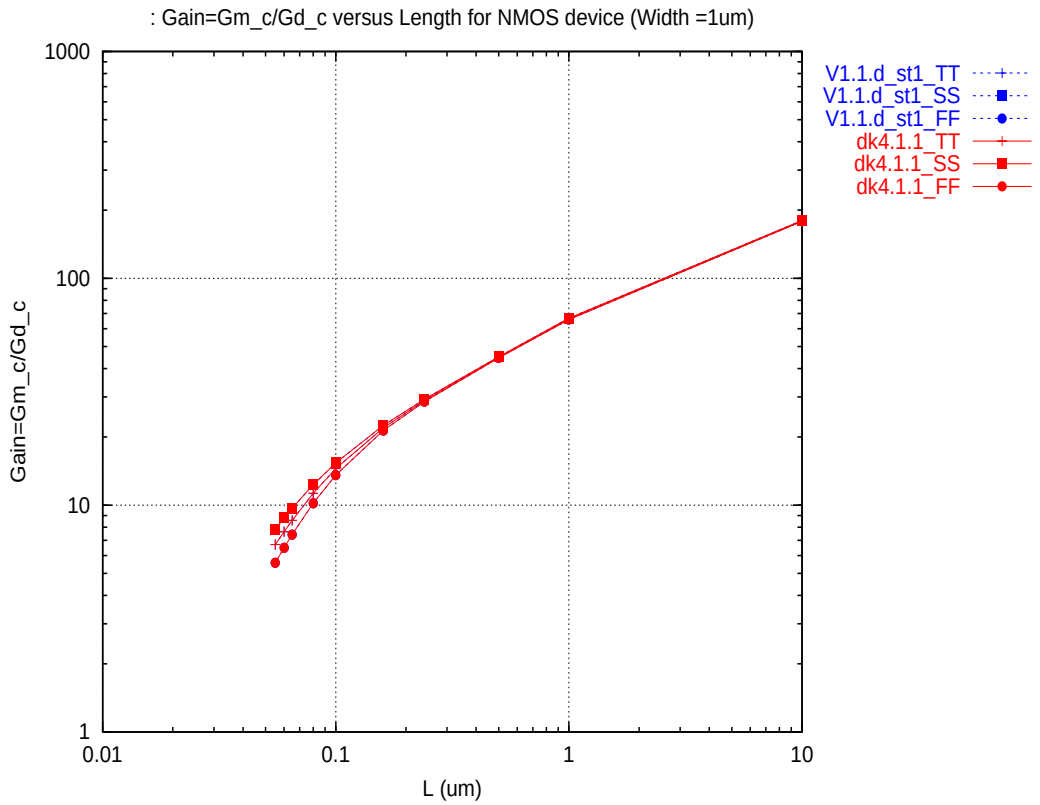

Figure 7 : GAIN versus drawn gate length for NMOS SVT_LP transistors (W = 1 µm)

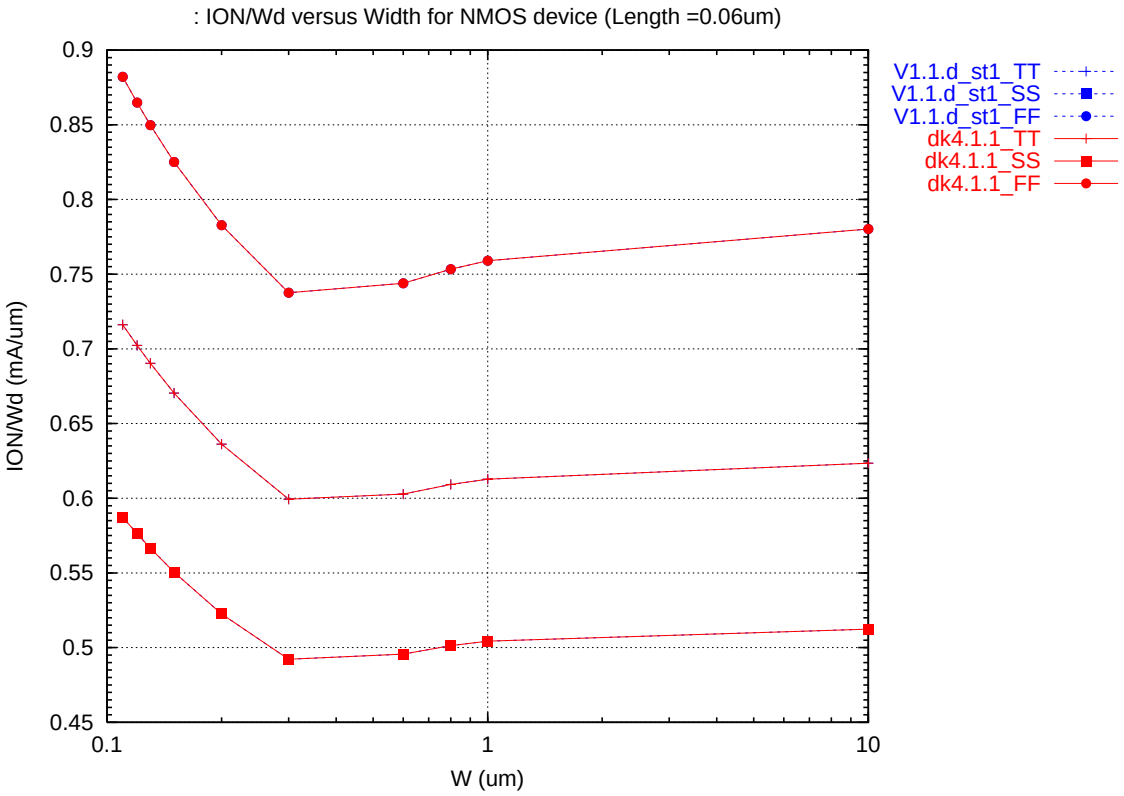

Figure 8 : ION versus drawn channel width for NMOS SVT_LP transistors (L = 0.06 µm)

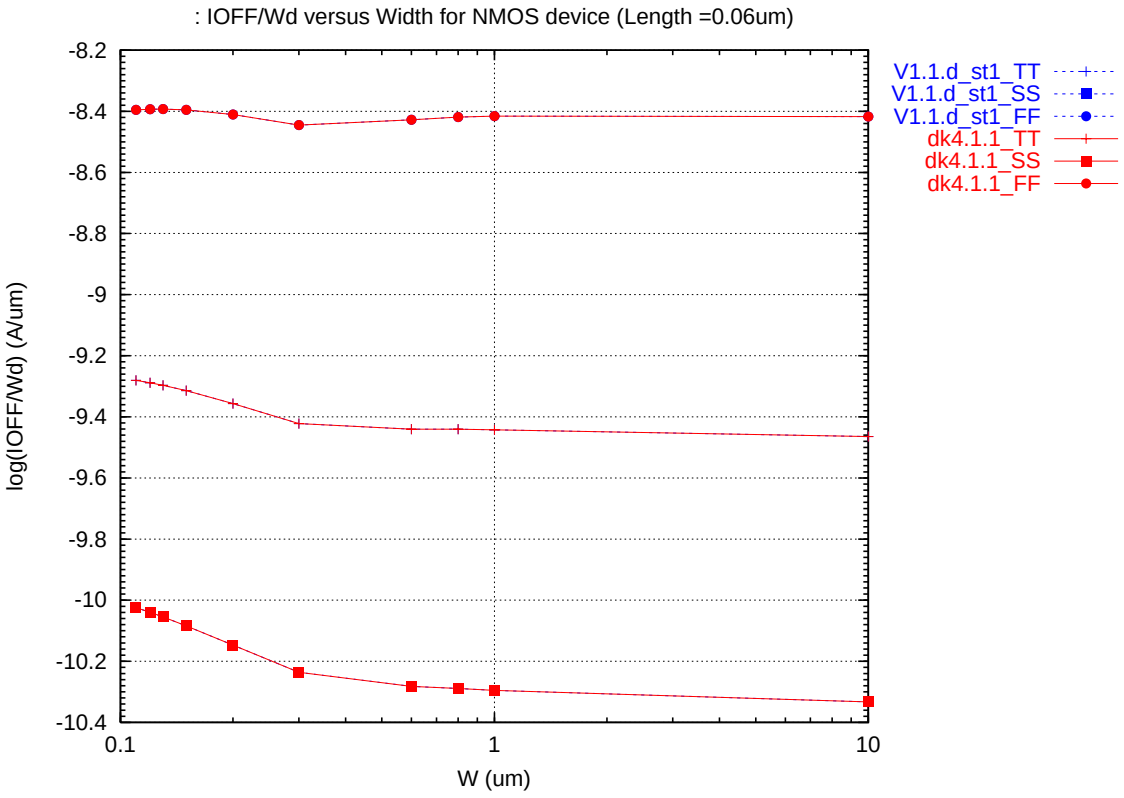

Figure 9 : IOFF versus drawn channel width for NMOS SVT_LP transistors (L = 0.06 µm)

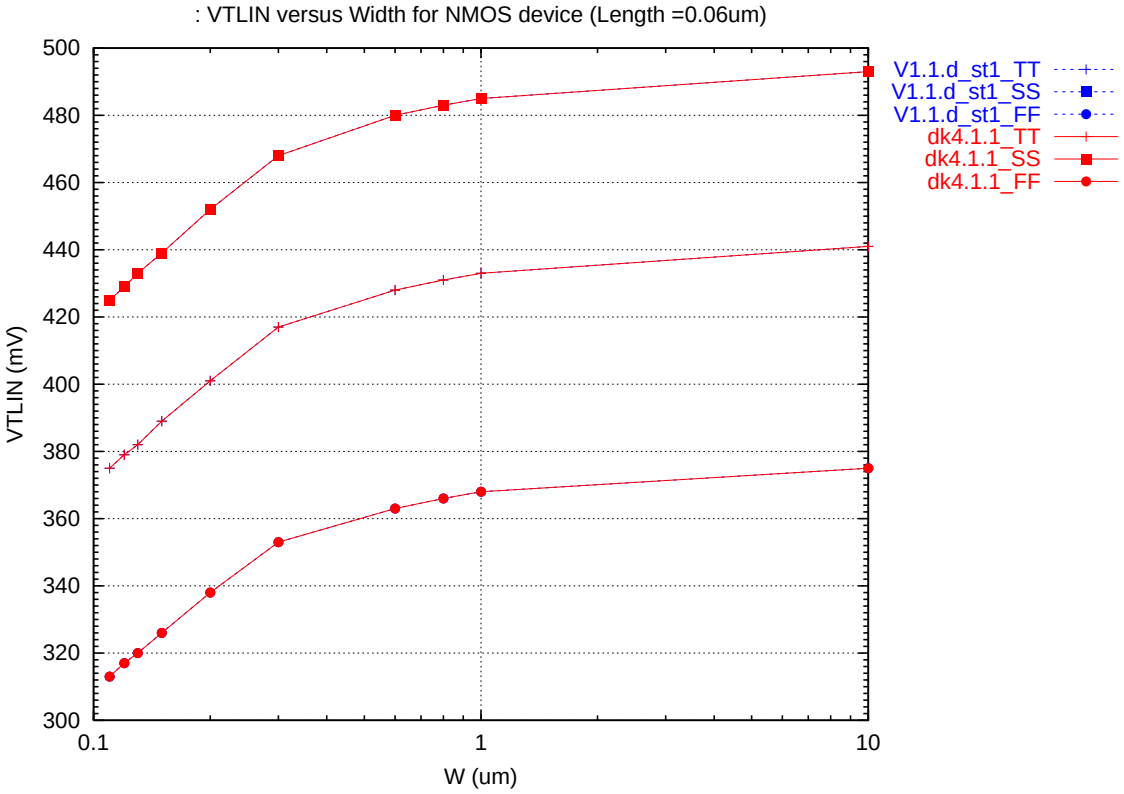

Figure 10 : Threshold voltage VTLIN versus drawn channel width for NMOS SVT_LP transistors (L = 0.06 µm)

6. ELECTRICAL BEHAVIOR VERSUS GATE LENGTH AND CHANNEL WIDTH FOR PMOS SVT_LP TRANSISTORS

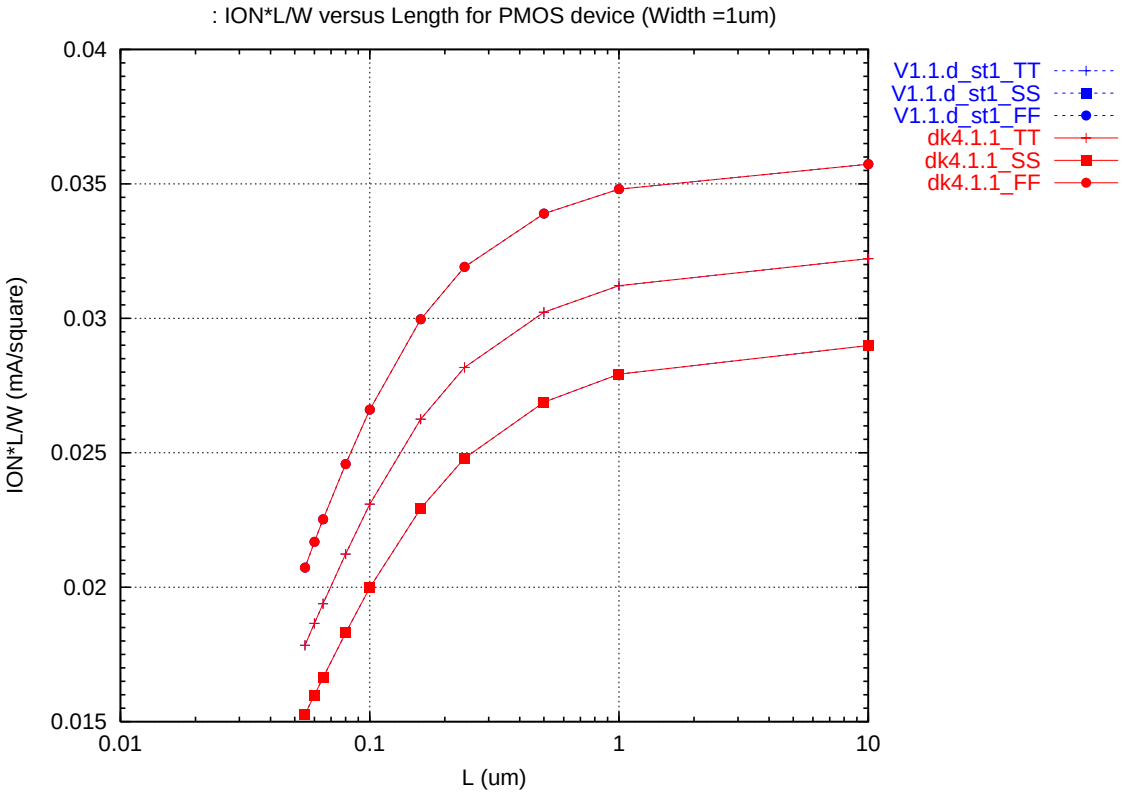

Figure 11 : ION versus drawn gate length for PMOS SVT_LP transistors (W = 1 µm)

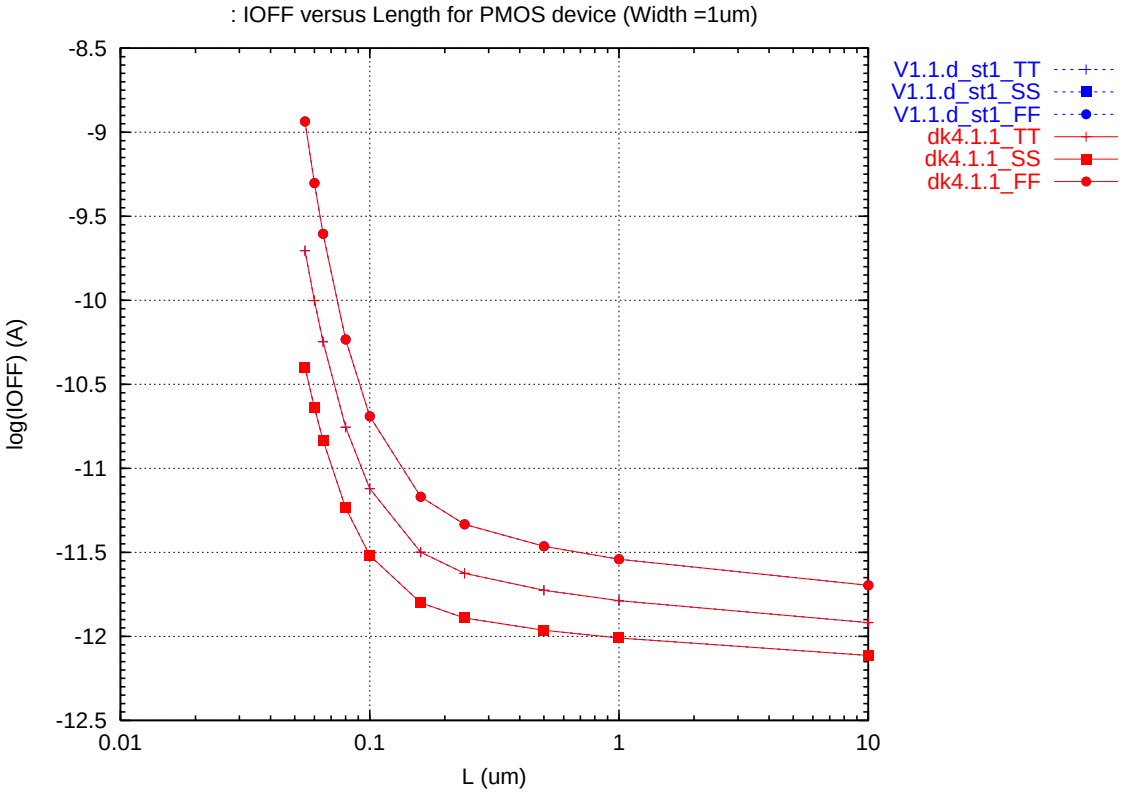

Figure 12 : IOFF versus drawn gate length for PMOS SVT_LP transistors (W = 1 µm)

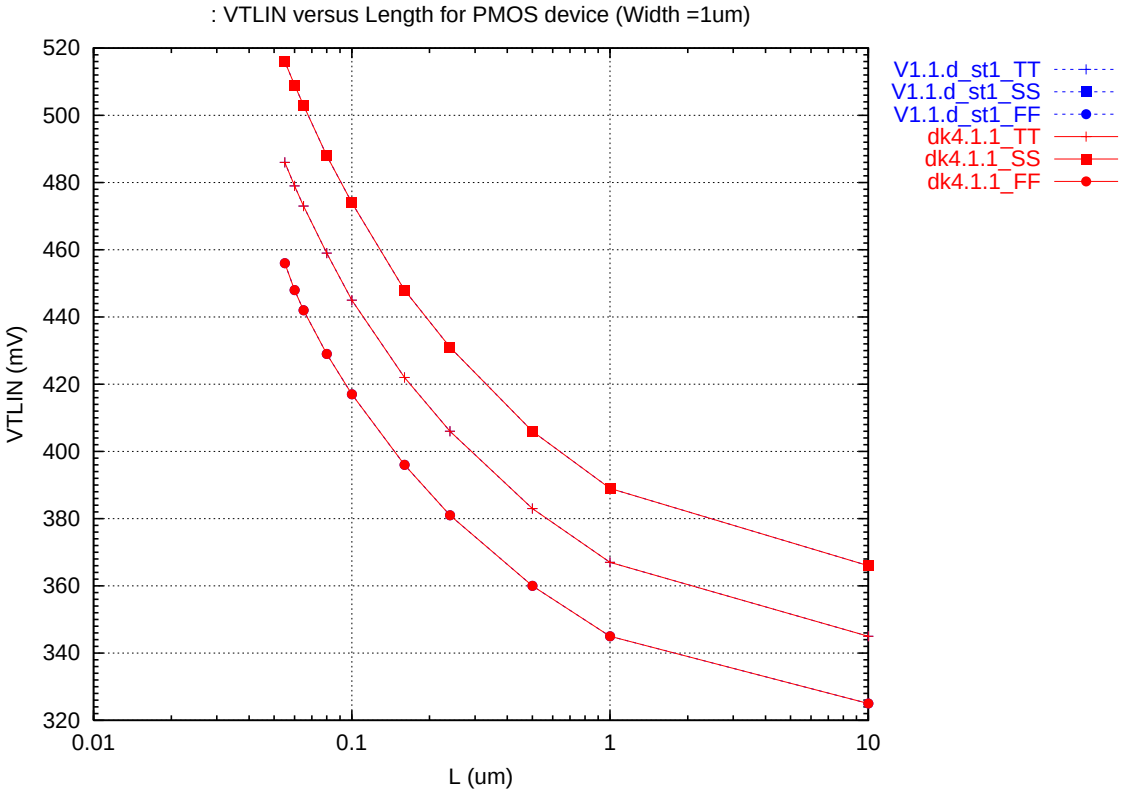

Figure 13 : Threshold voltage VTLIN versus drawn gate length for PMOS SVT_LP transistors (W = 1 µm)

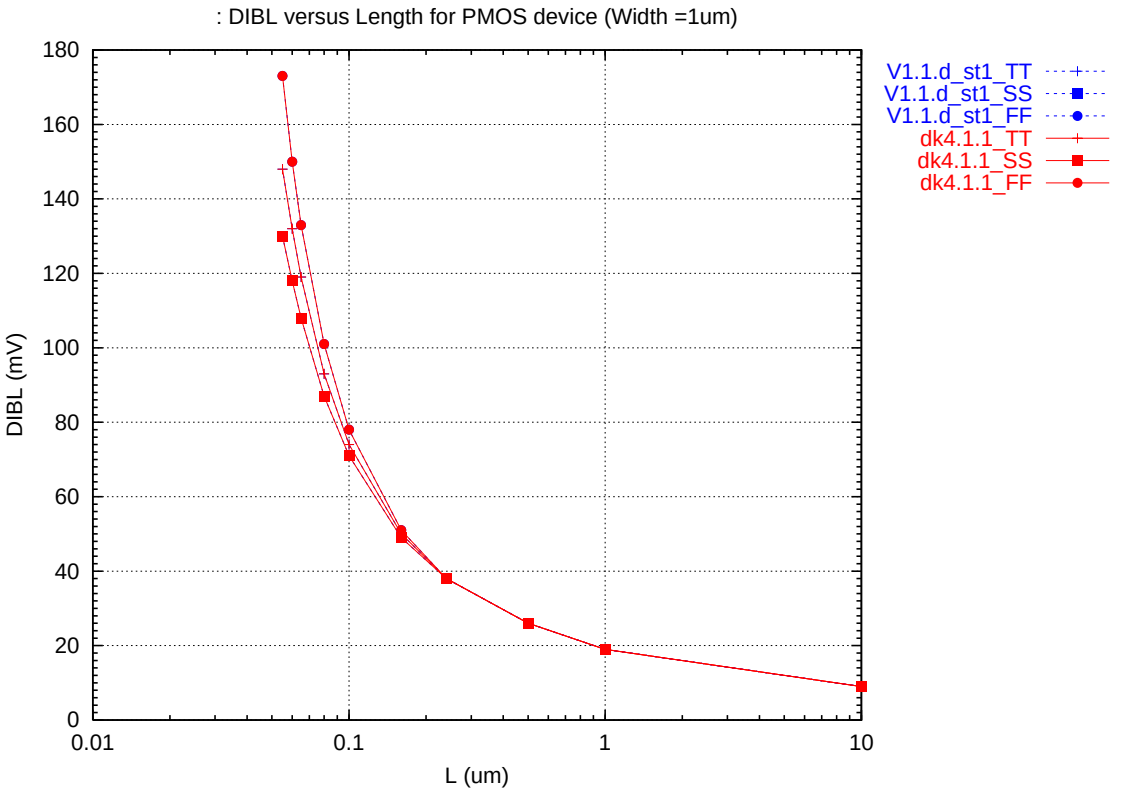

Figure 14 : DIBL= VTLIN-VTSAT versus drawn gate length for PMOS SVT_LP transistors (W = 1 µm)

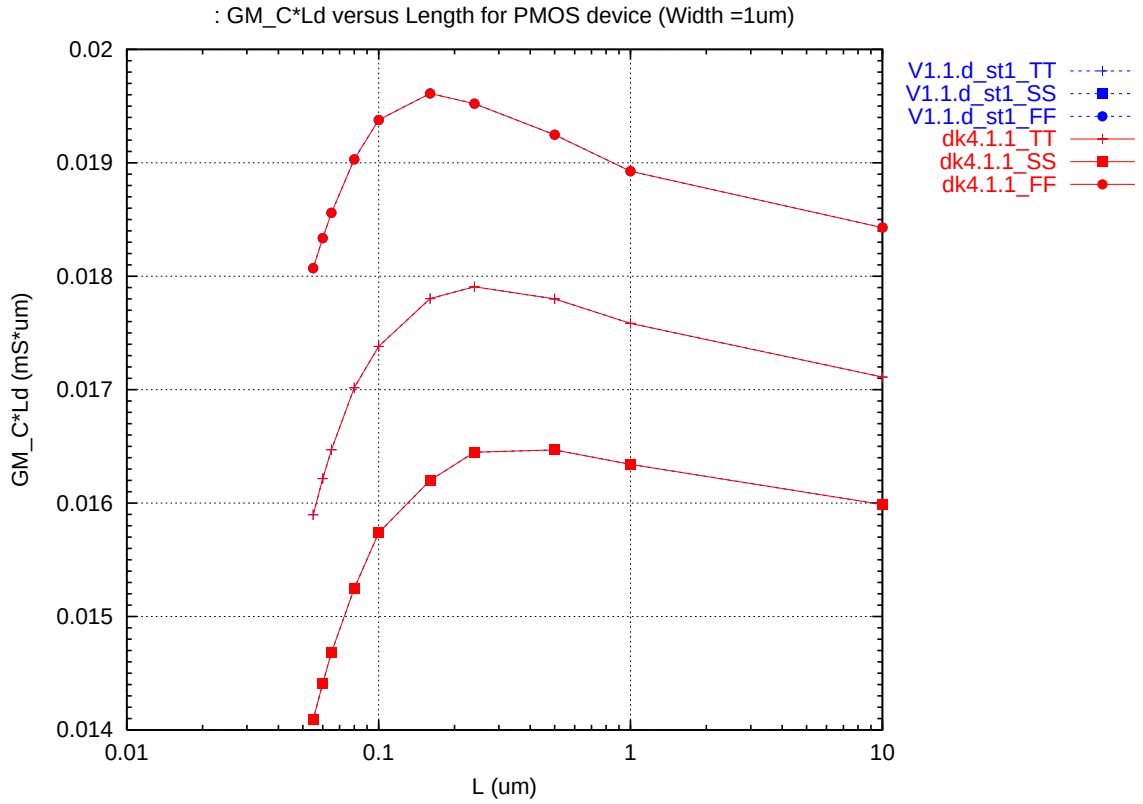

Figure 15 : GM*Ld versus drawn gate length for PMOS SVT_LP transistors (W = 1 µm)

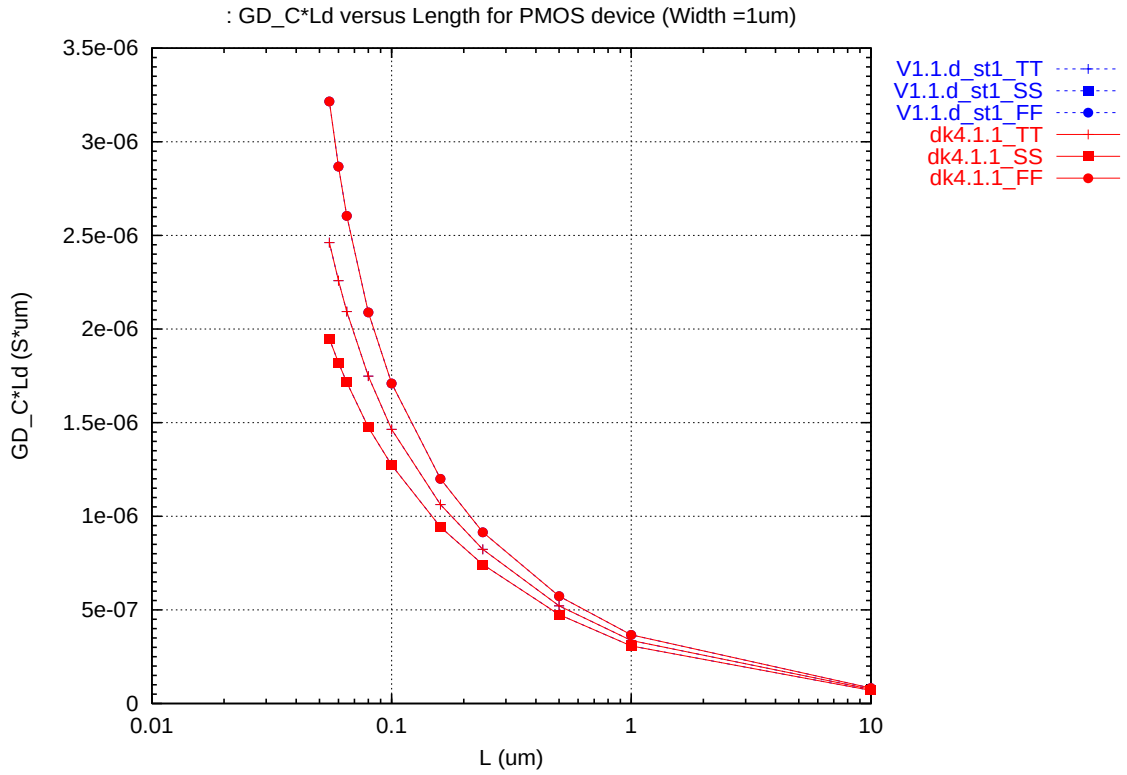

Figure 16 : GD*Ld versus drawn gate length for PMOS SVT_LP transistors (W = 1 µm)

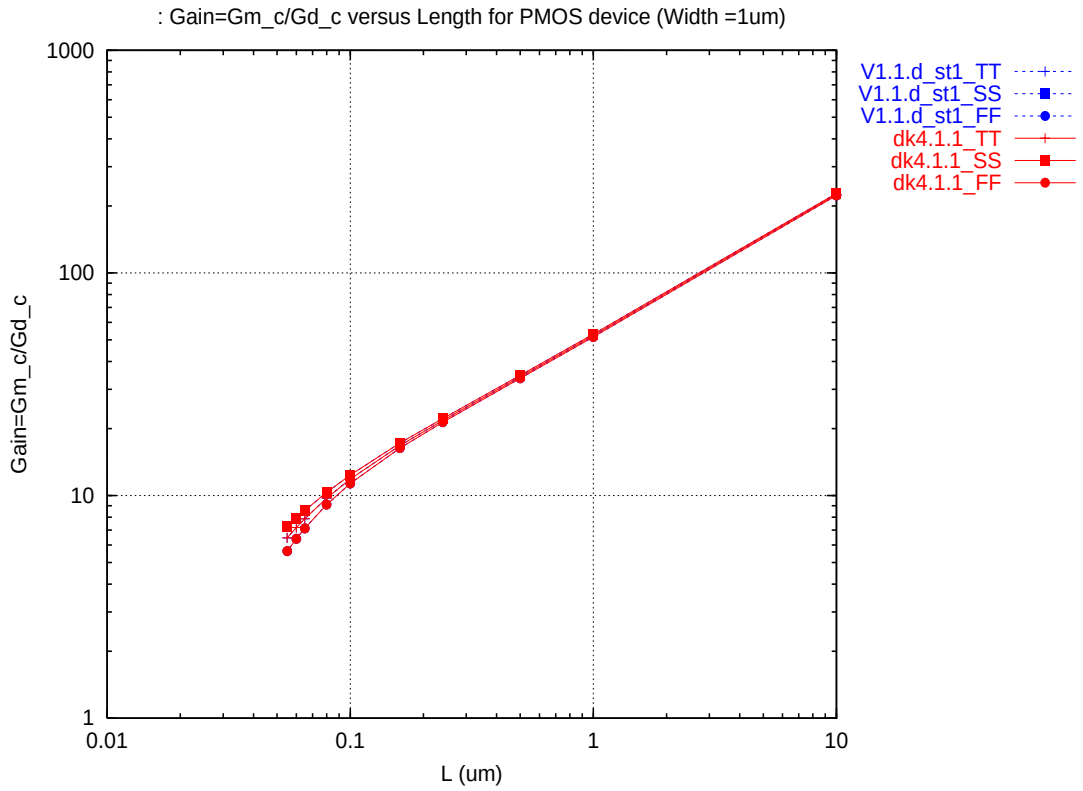

Figure 17 : GAIN versus drawn gate length for PMOS SVT_LP transistors (W = 1 µm)

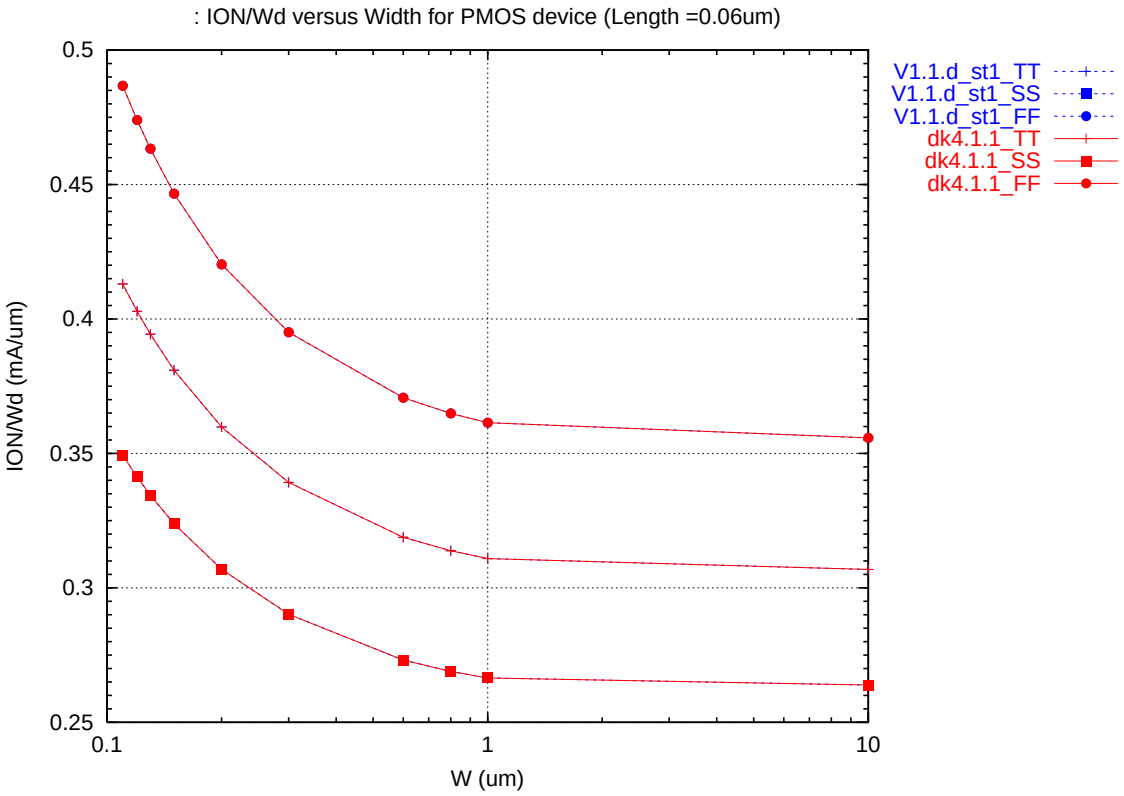

Figure 18 : ION versus drawn channel width for PMOS SVT_LP transistors (L = 0.06 µm)

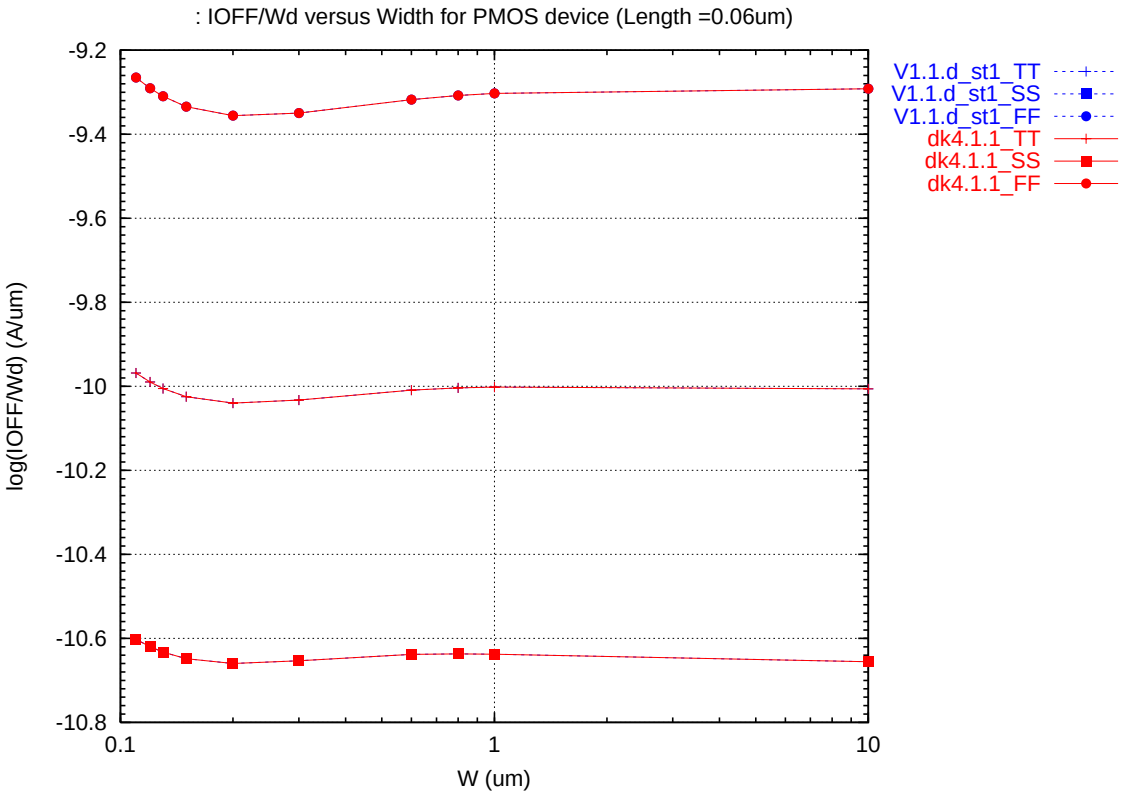

Figure 19 : IOFF versus drawn channel width for PMOS SVT_LP transistors (L = 0.06 µm)

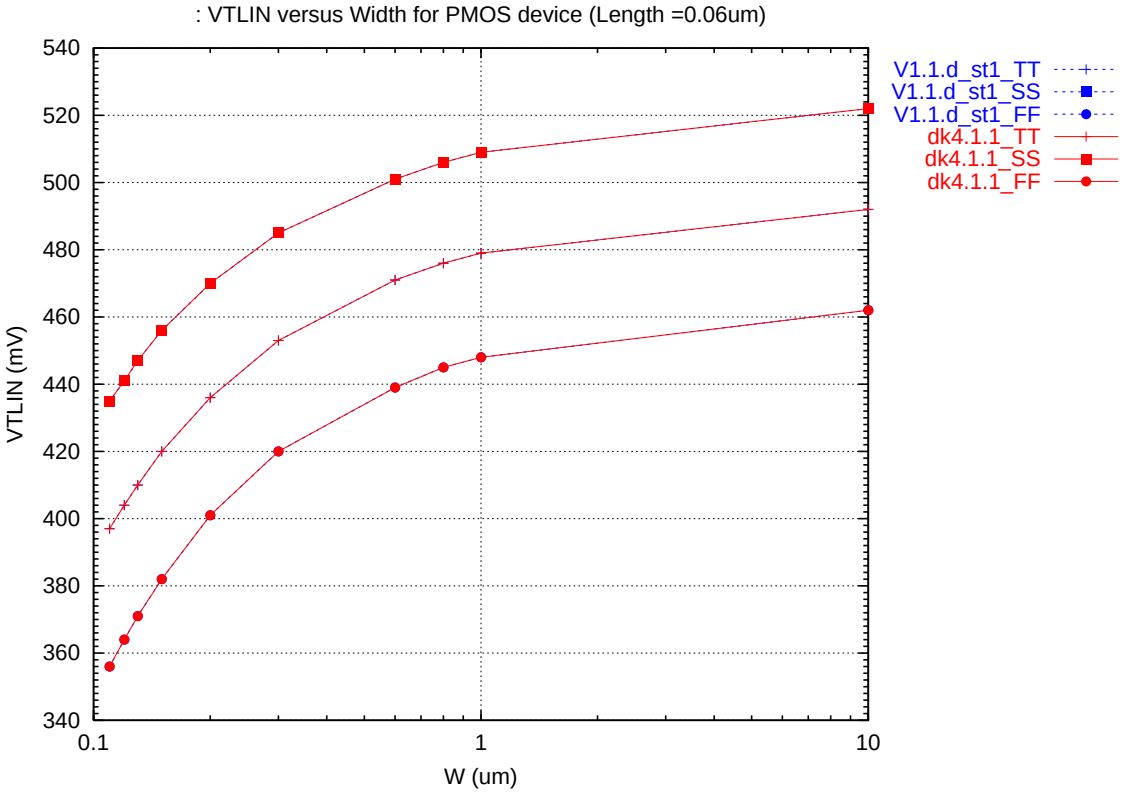

Figure 20 : Threshold voltage VTLIN versus drawn channel width for PMOS SVT_LP transistors (L = 0.06 µm)