ECE1396H Assignment 4

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A. CMOS T/H and S/H simulation

1) a: The transfer funcion plot from input to T/H and S/H node are given in Fig.1. The 3dB bandwidth at the first hold capacitor is around 1.073 GHz, and at the second hold capacitor is about 638.8 MHz.

2) b: Waveforms at input, T/H node and S/H node are in Fig. 2, centered at $Vdd/2$. The pedestal value is found to be about 22 mV (Fig. 3) when the input signal is sampled at the minimum value. This value here is dependent to the signal. Fig. 4 shows the FFT of the input and output signal, and SDR is about 43.478 dB at the output. Majorly, charge injection and clock feed-through cause the degrade of SDR.

3) c: With 5mV input amplitude, waveforms at input, T/H node and S/H node are in Fig. 5, centered at $V_{dd}/2$. The pedestal value is found to be about 6 mV (Fig. 6) when the input signal is sampled at the minimum value. This value here is dependent to the signal. Fig. 4 shows the FFT of the input and output signal, and SDR is also about 43.478 dB at the output. Majorly, charge injection and clock feed-through cause the degrade of SDR. One can see the spikes (about 30 mV in magnitude) at the T/H and S/H waveform when it goes from sample mode to the hold mode. This is because for the transmission gate, PMOS and NMOS transistors do not open (or close) at the same time if they are just geometrically (gate length and width) matched to each other. This causes the glitch (overshoot) at the transition between sample and hold states at T/H and S/H nodes.

4) d: For IIP3 simulation, two signals that are at 50 and 51 MHz are used, and their input power are swept from 0 to 10 dBm. Fig. 8 shows the IIP3 plot of the circuit, which is found to be about 18.91 dBm. Therefore, the circuit demonstrates very high linearity over a wide range of input power.

5) e: The output signal spectrum with different input frequency (50 MHz per increment instead, input signal amplitude is 500 mV) are plotted in Fig. 9. It can be seen that when input frequency is 50 MHz, SDR is about 43.788 dB. When it increases up to 100 MHz, SDR drops to 41 dB, about 3 dB lower than its lower frequency. From this perspective, the large signal bandwidth is about 100 MHz.

B. 4 time-interleaved S/H ADC front-end

From Fig. 10, the small signal bandwidth from input to $C_{s,ADC}$ is about 751.1 MHz. In this design, both sampling and subsampling transistors are using a gate length of 60 nm and gate width of 1 μm, and the input signal's frequency is set to 50 MHz. The signals at the input and the first 4 capacitor output (just to show the idea to prevent the crowdedness) are in Fig. 11. Fig. 12 shows the output signal spectrum at $C_{s,ADC}$ with respect to different input signal frequency, which is from 50 MHz to 300 MHz with an increment of 50 MHz, and Fig. 13 shows the output SDR at $C_{s,ADC}$ as a function of input frequency. Fig. 14 shows the clock signal. Fig. 15 shows the sum of all 16 outputs. The DC offset is caused by the pedestal of each output, which can be removed by DC calibration. The single output spectrum and the 16-summed signal output spectrum are plotted in Fig. 16. For one output from $C_{s,ADC}$, the SDR is about 40.488 dB. For 16-summed signal output, the SDR is about 40.49 dB. Interleaved S/H allows one to use slower sampling clocks to sample a signal faster with multiple interleaved clock signals. This can reduce the sampled signal distortion and improves SDR.

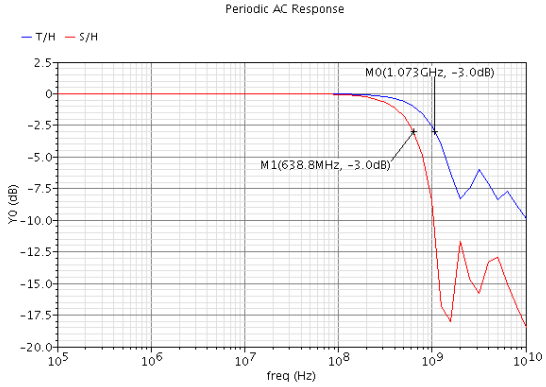

Fig. 1: Small signal transfer function from input to T/H and S/H nodes.

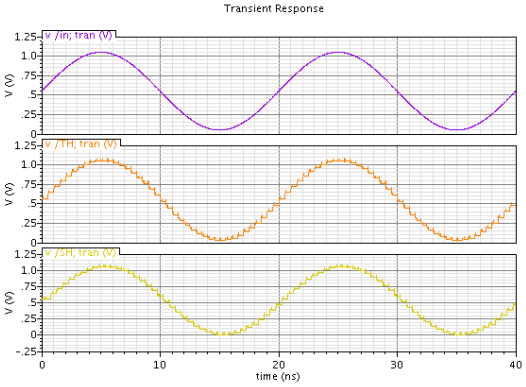

Fig. 2: Waveform at input, T/H and S/H nodes.

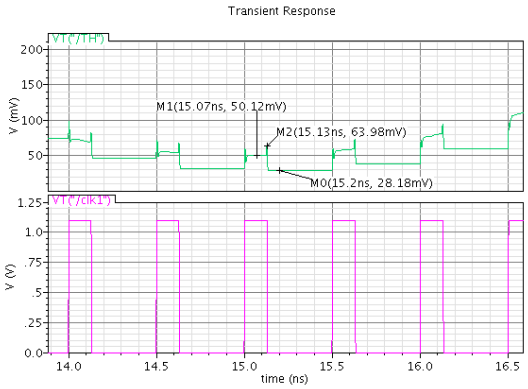

Fig. 3: Signal pedestal from sample mode to hold mode at T/H node.

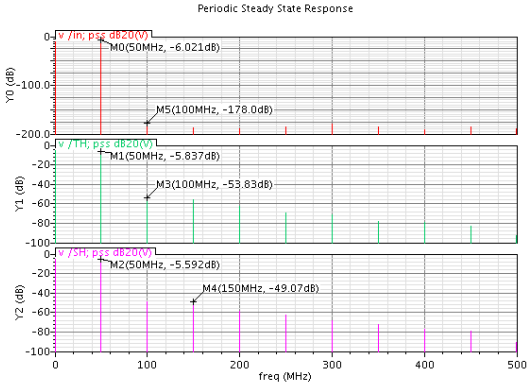

Fig. 4: Spectrum at input, T/H and S/H node.

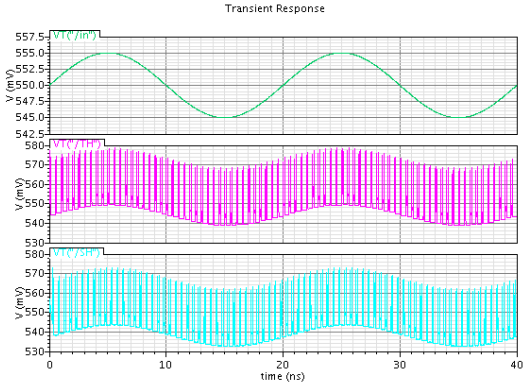

Fig. 5: 5mV amplitude input's waveform at input, T/H and S/H nodes.

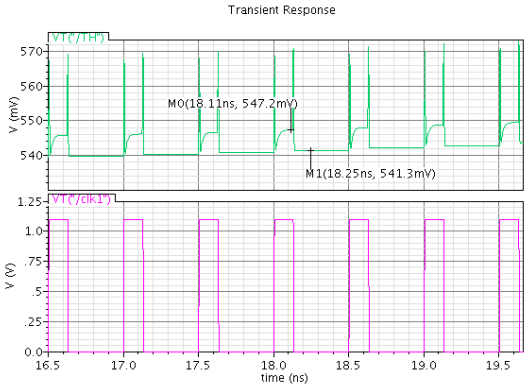

Fig. 6: 5 mV amplitude input signal pedestal from sample mode to hold mode at T/H node.

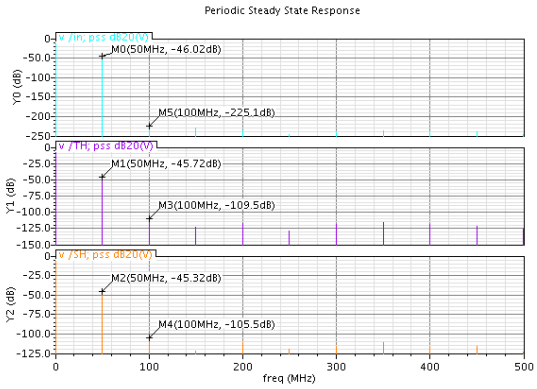

Fig. 7: 5 mV amplitude input signal Spectrum at input, T/H and S/H node.

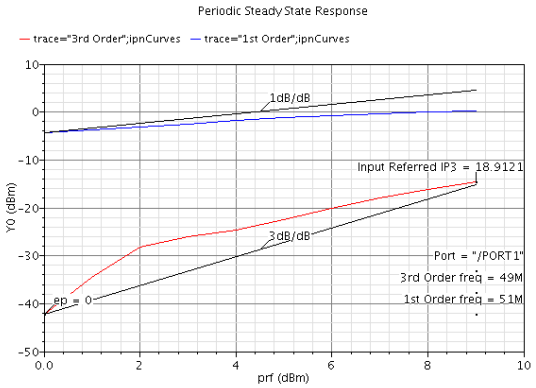

Fig. 8: IIP3 of the circuit.

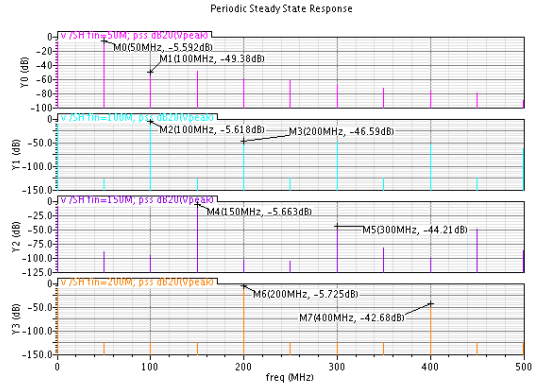

Fig. 9: Output spectrum with different input signal frequency.

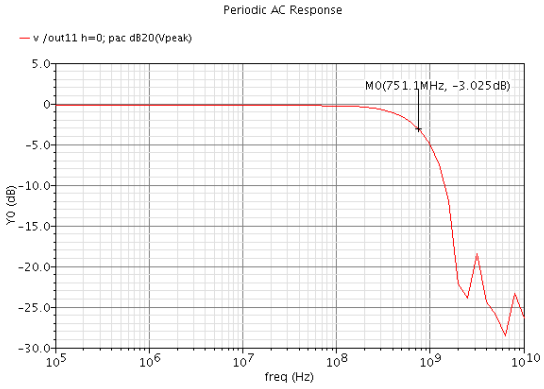

Fig. 10: Small-signal transfer function from input to $C_{s,ADC}$.

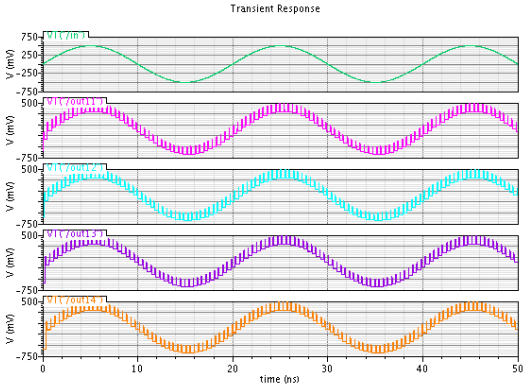

Fig. 11: Input and first 4 $C_{s,ADC}$ output waveform.

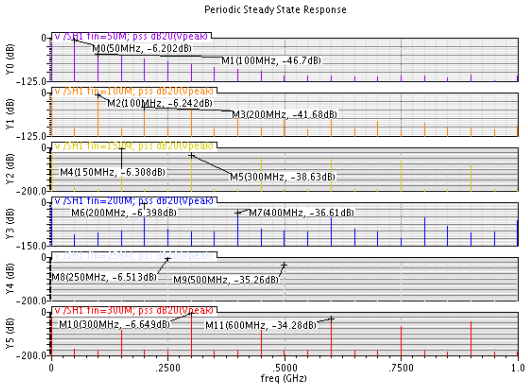

Fig. 12: Output signal spectrum at $C_{s,ADC}$ with respect to different input signal frequency, from 50 MHz to 300 MHz with an increment of 50 MHz per simulation.

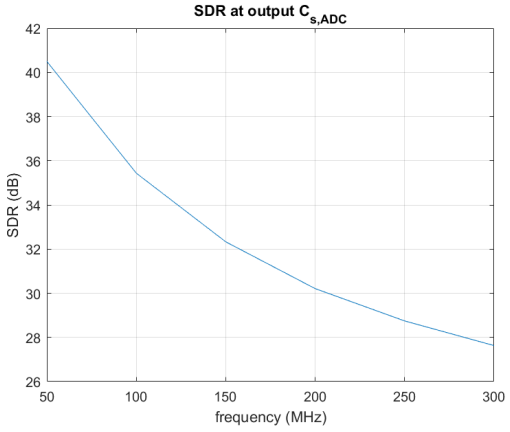

Fig. 13: Output signal SDR at $C_{s,ADC}$ as a function of input frequency.

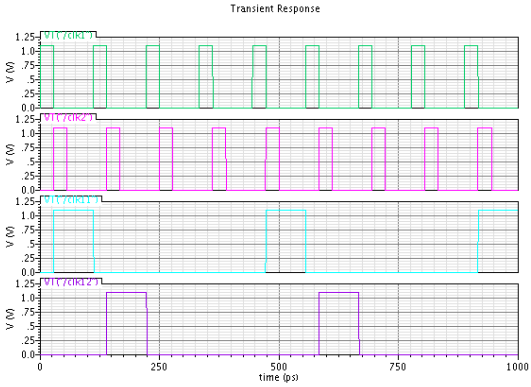

Fig. 14: Clock signal at sampling and sub-sampling side.

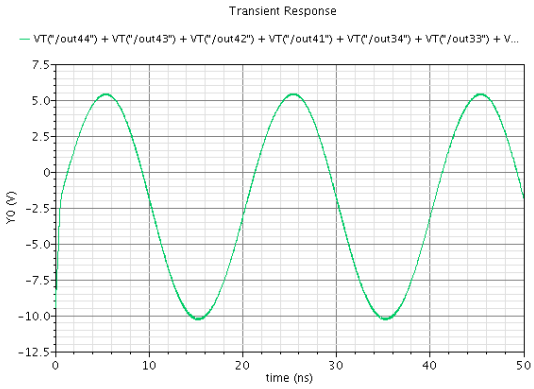

Fig. 15: Summation of all 16 outputs.

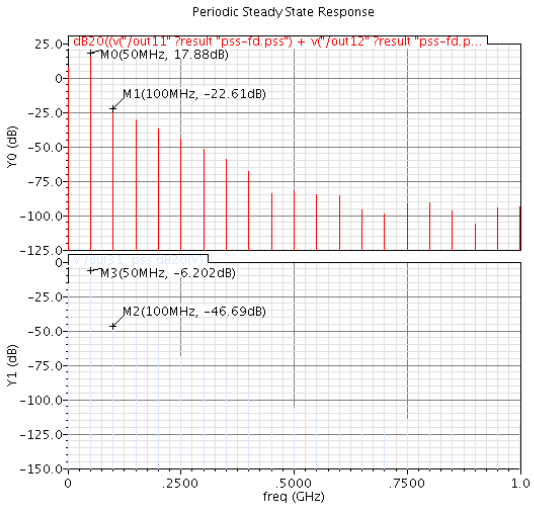

Fig. 16: Spectrum of single signal output (down) and 16-summed signal output (up).