SVT_2V5 MODELS (NSVT25, PSVT25)

1. CONDITIONS OF EXTRACTION

- Maturity: Preliminary
- Model parameters extraction based on lot : Q527AJA
- Geometrical extraction domain:
  - Drawn gate length : 10.0 ≥ L ≥ 0.28 µm
  - Drawn transistor width : 10 ≥ W ≥ 0.4 µm
- Temperature extraction domain: -40 ˚C to 150 ˚C
- Bias extraction domain:
  - Gate bias: 0 ≤ |VGS| ≤ 2.75 V (VDD + 10%)
  - Drain bias: 0 ≤ |VDS| ≤ 2.75 V (VDD + 10%)
  - Bulk bias: 0 ≤ |VBS| ≤ 2.75 V (VDD + 10%)

2. CONDITIONS OF SIMULATION

- Temperature: 25 ˚C
- Currents:

  IDLIN = Ids at Vgs = 2.5 V, Vds = 100 mV and Vbs = 0 V

  ION = Ids at Vgs = 2.5 V, Vds = 2.5 V and Vbs = 0 V

  IOFF = Ids at Vgs = 0 V, Vds = 2.5 V and Vbs = 0 V

  IG_ON = Igs at Vgs = 2.5 V and Vd= Vs = Vb = 0 V

  IG_OFF = Igs at Vgs =Vbs = 0 V and Vds = 2.5 V
- Threshold voltage in linear and saturation regime

  VTLIN is Vgs value at Vds = 100 mV, Vbs = 0 V and Ids=100*W/L nA.

  VTSAT is Vgs value at Vds = 2.5 V, Vbs = 0 V and Ids=100*W/L nA.
- Current derivatives:

$$Gm = \frac{\partial}{\partial V_{gs}} Ids$$ at Vgs = VTLIN + 0.2 V, Vds = 1.25 V and Vbs = 0 V

$$Gd = \frac{\partial}{\partial V_{ds}} Ids$$ at Vgs = VTLIN + 0.2 V, Vds = 1.25 V and Vbs = 0 V

Analog gain = Gm/Gd

- Gate Capacitances:

  CGGINV = CGG at Vgs = 2.5 V, Vds = 0 V and Vbs = 0 V

  CGD_0V = CGD at Vgs = 0 V, Vds = 0 V and Vbs = 0 V

  $$CGGMEAN = \frac{1}{VDD} \cdot \int_{0}^{VDD} CGG \times dVgs$$ with VDD = 2.5 V and Vbs = 0 V

  TAU = CGGMEAN*VDD/ION

- Diode Capacitances:

  CBD OFF = CBD at Vgs = 0 V, Vds = 2.5 V and Vbs = 0 V

  Note: the area and perimiters of source/drain junction diodes used for simulation are defined with the the minimum poly-to-active distance specified in the DRM.

- Transition frequency:

  FT = frequency for which the small signal current gain H_{21} is 0 dB (i.e. $\left|\frac{I_d}{I_g}\right|$ = 0 dB).

3. MAIN ELECTRICAL CHARACTERISTICS OF NMOS SVT_2V5 TRANSISTORS

PARAMETERS	SVT25_TT	SVT25_SSA	SVT25_FFA	units
N-channel transistors (nsvt25)				
VTLIN W=10/L=10.0	420	451	389	mV
IDLIN W=10/L=10.0	3.28e-05	3.10e-05	3.48e-05	A
VTSAT W=10/L=10.0	417	448	386	mV
ION W=10/L=10.0	2.98e-04	2.75e-04	3.22e-04	A
VTLIN W=10/L=0.28	432	469	394	mV
IDLIN W=10/L=0.28	9.32e-04	8.62e-04	1.01e-03	A
VTSAT W=10/L=0.28	395	435	355	mV
ION W=10/L=0.28	5.68e-03	5.28e-03	6.11e-03	A
IOFF W=10/L=0.28	9.88e-11	3.38e-11	2.95e-10	A
IG_ON W=10/L=0.28	0.00e+00	0.00e+00	0.00e+00	A
IG_OFF W=10/L=0.28	0.00e+00	0.00e+00	0.00e+00	A
FT W=10/L=0.28	3.60e+10	3.43e+10	3.78e+10	Hz
CGGinv W=10/L=0.28	1.93e-14	1.92e-14	1.94e-14	F
CGGmean W=10/L=0.28	1.75e-14	1.73e-14	1.77e-14	F
CGD 0V W=10/L=0.28	3.90e-15	3.79e-15	4.07e-15	F
CBD OFF[a] W=10/L=0.28	4.64e-15	5.23e-15	4.05e-15	F
Tau W=10/L=0.28	7.7	8.2	7.2	ps
Gm W=10/L=0.28	1.02e-03	9.40e-04	1.11e-03	S
Gd W=10/L=0.28	1.55e-05	1.33e-05	1.81e-05	S
Gain W=10/L=0.28	6.60e+01	7.08e+01	6.11e+01	
VTLIN W=0.4/L=0.28	349	386	312	mV
IDLIN W=0.4/L=0.28	3.87e-05	3.45e-05	4.32e-05	A
VTSAT W=0.4/L=0.28	312	352	272	mV
ION W=0.4/L=0.28	2.41e-04	2.16e-04	2.68e-04	A
IOFF W=0.4/L=0.28	3.96e-11	1.38e-11	1.16e-10	A
FT W=0.4/L=0.28	3.14e+10	2.97e+10	3.32e+10	Hz

Table 1: Main electrical characteristics for NMOS

a. Value coresponding to the minimum poly-to-acvtive distance specified in the DRM

4. MAIN ELECTRICAL CHARACTERISTICS OF PMOS SVT_2V5 TRANSISTORS

PARAMETERS	SVT25_TT	SVT25_SSA	SVT25_FFA	units
P-channel transistors (psvt25)				
VTLIN W=10/L=10.0	475	534	416	mV
IDLIN W=10/L=10.0	9.29e-06	8.51e-06	1.01e-05	A
VTSAT W=10/L=10.0	474	534	415	mV
ION W=10/L=10.0	8.88e-05	7.82e-05	1.00e-04	A
VTLIN W=10/L=0.28	401	463	341	mV
IDLIN W=10/L=0.28	3.52e-04	3.18e-04	3.91e-04	A
VTSAT W=10/L=0.28	358	421	295	mV
ION W=10/L=0.28	3.35e-03	2.97e-03	3.77e-03	A
IOFF W=10/L=0.28	1.00e-10	1.60e-11	6.54e-10	A
IG_ON W=10/L=0.28	0.00e+00	0.00e+00	0.00e+00	A
IG_OFF W=10/L=0.28	0.00e+00	0.00e+00	0.00e+00	A
FT W=10/L=0.28	2.08e+10	1.94e+10	2.23e+10	Hz
CGGinv W=10/L=0.28	1.90e-14	1.89e-14	1.91e-14	F
CGGmean W=10/L=0.28	1.73e-14	1.70e-14	1.75e-14	F
CGD 0V W=10/L=0.28	3.55e-15	3.44e-15	3.74e-15	F
CBD OFF[a] W=10/L=0.28	4.84e-15	5.45e-15	4.23e-15	F
Tau W=10/L=0.28	12.9	14.3	11.6	ps
Gm W=10/L=0.28	6.18e-04	5.49e-04	7.06e-04	S
Gd W=10/L=0.28	1.29e-05	1.06e-05	1.61e-05	S
Gain W=10/L=0.28	4.79e+01	5.19e+01	4.37e+01	
VTLIN W=0.4/L=0.28	391	454	328	mV
IDLIN W=0.4/L=0.28	1.71e-05	1.49e-05	1.95e-05	A
VTSAT W=0.4/L=0.28	348	414	283	mV
ION W=0.4/L=0.28	1.53e-04	1.29e-04	1.80e-04	A
IOFF W=0.4/L=0.28	5.37e-12	8.14e-13	3.66e-11	A
FT W=0.4/L=0.28	2.18e+10	2.01e+10	2.36e+10	Hz

Table 2: Main electrical characteristics for PMOS

a. Value coresponding to the minimum poly-to-acvtive distance specified in the DRM

5. ELECTRICAL BEHAVIOR VERSUS GATE LENGTH AND CHANNEL WIDTH FOR NMOS SVT_2V5 TRANSISTORS

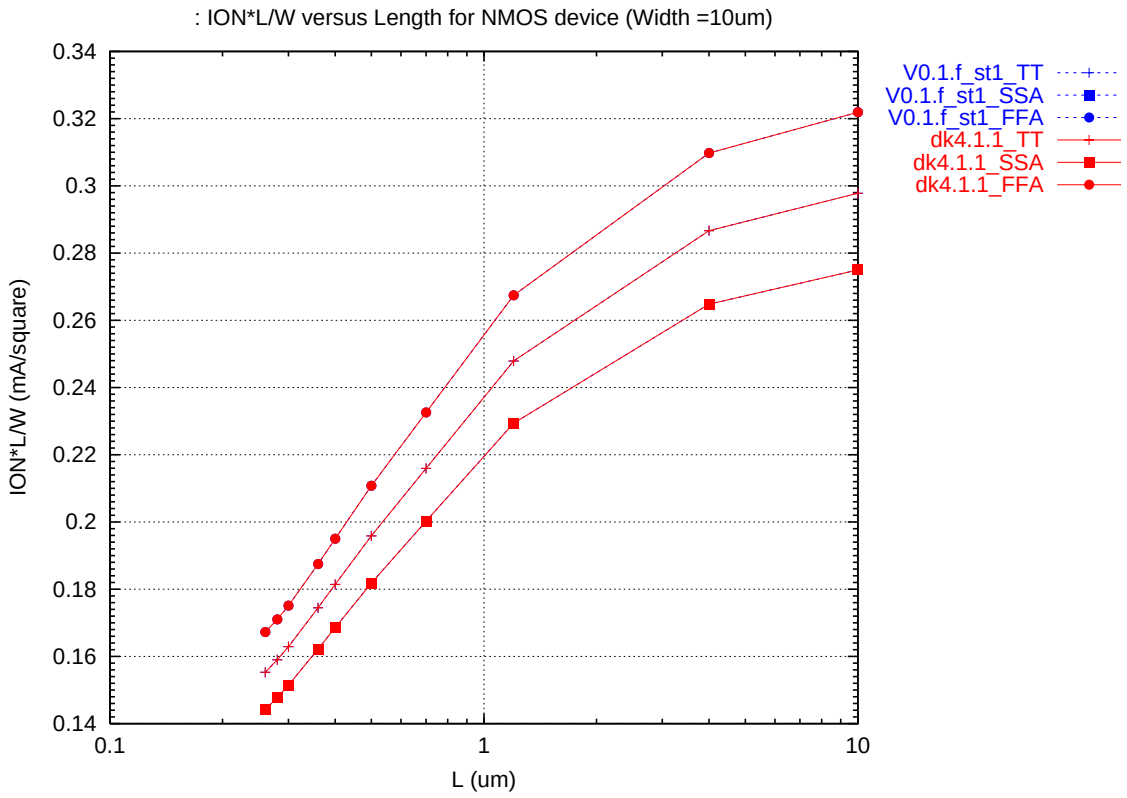

Figure 1 : ION/❑=ION*L/W versus drawn gate length for NMOS SVT_2V5 transistors (W = 10 µm)

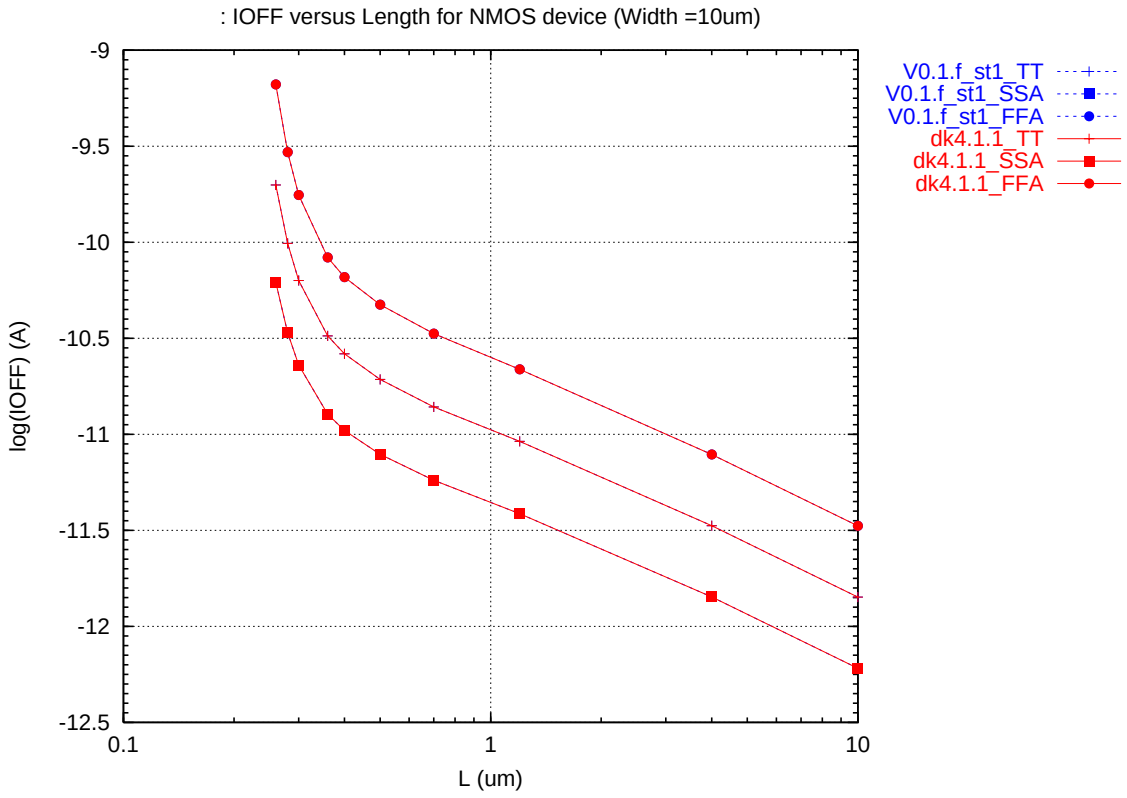

Figure 2 : IOFF versus drawn gate length for NMOS SVT_2V5 transistors (W = 10 µm)

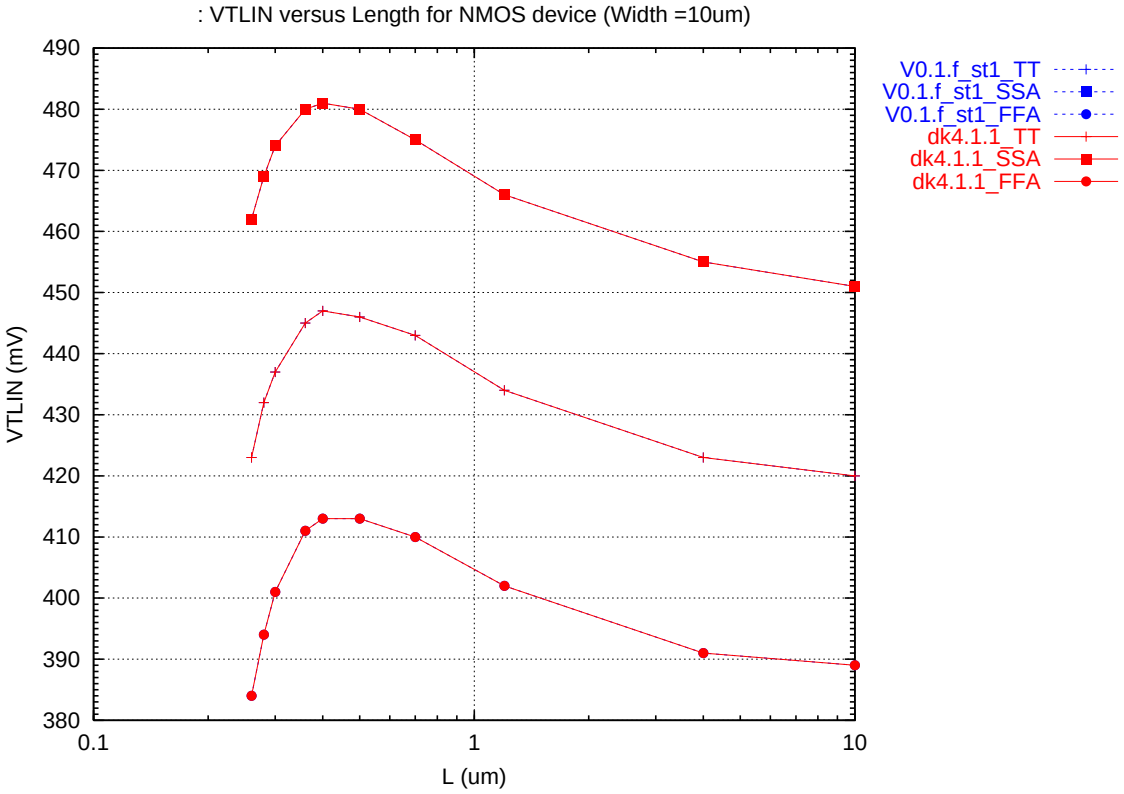

Figure 3 : Threshold voltage VTLIN versus drawn gate length for NMOS SVT_2V5 transistors (W = 10 µm)

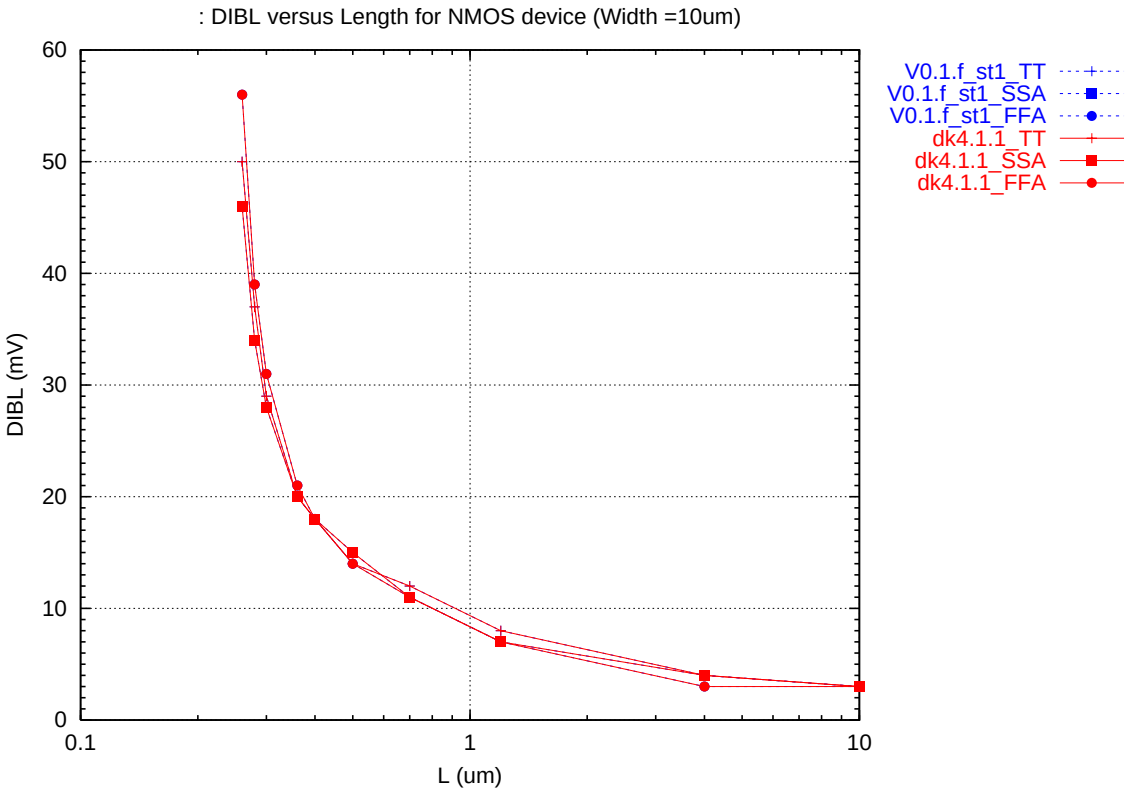

Figure 4 : DIBL= VTLIN-VTSAT versus drawn gate length for NMOS SVT_2V5 transistors (W = 10 µm)

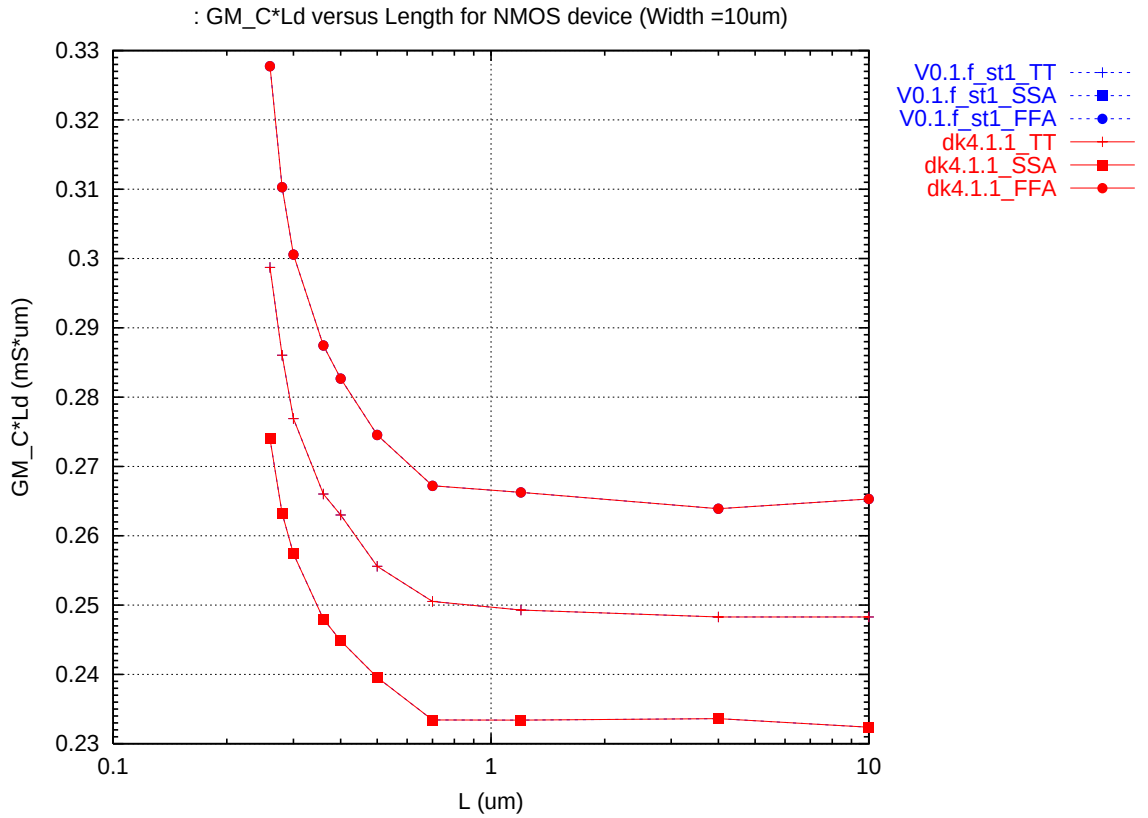

Figure 5 : GM*Ld versus drawn gate length for NMOS SVT_2V5 transistors (W = 10 µm)

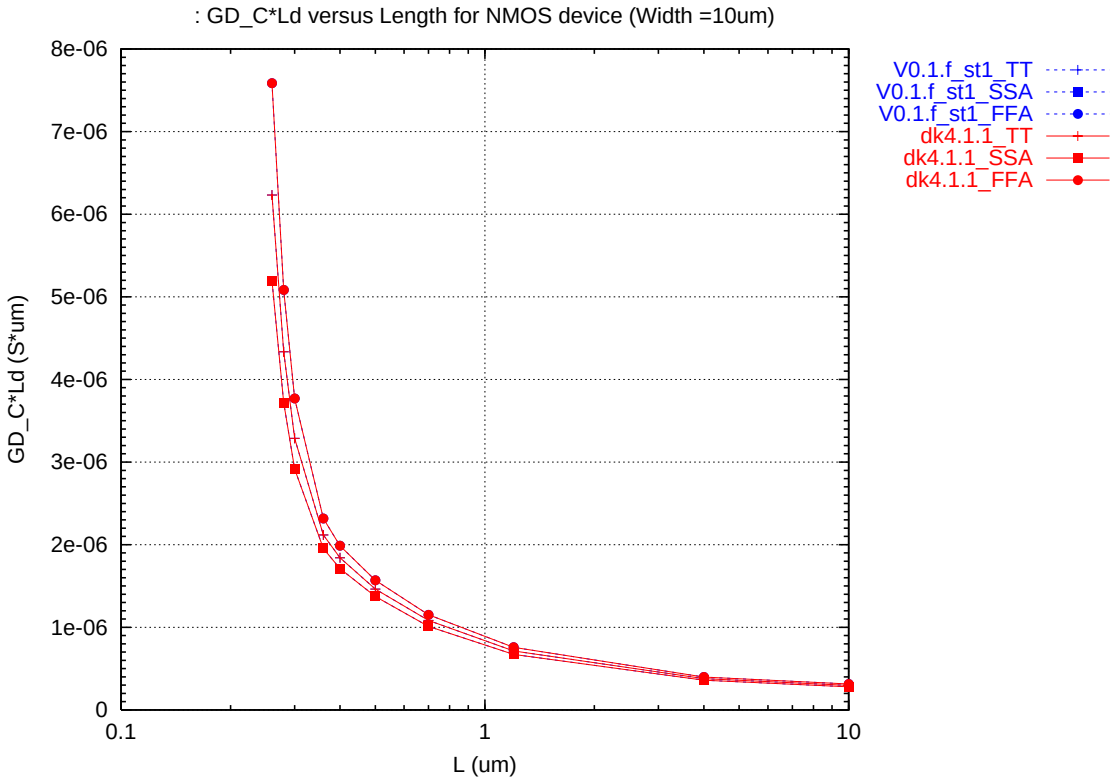

Figure 6 : GD*Ld versus drawn gate length for NMOS SVT_2V5 transistors (W = 10 µm)

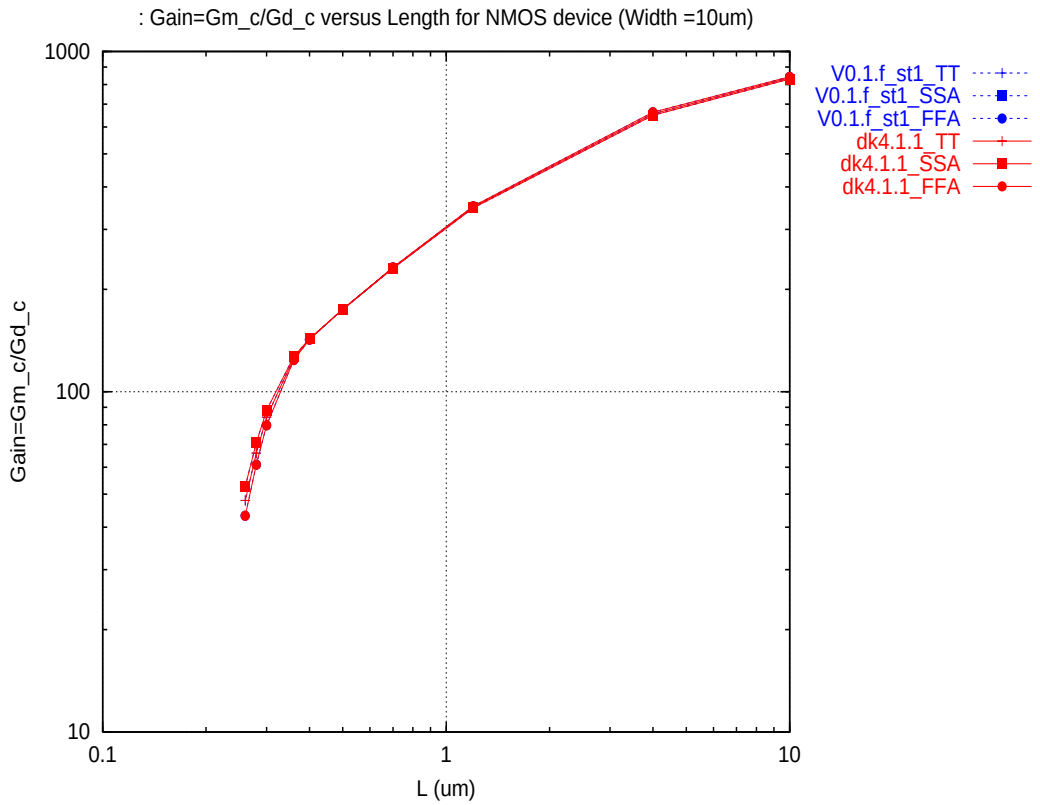

Figure 7 : GAIN versus drawn gate length for NMOS SVT_2V5 transistors (W = 10 µm)

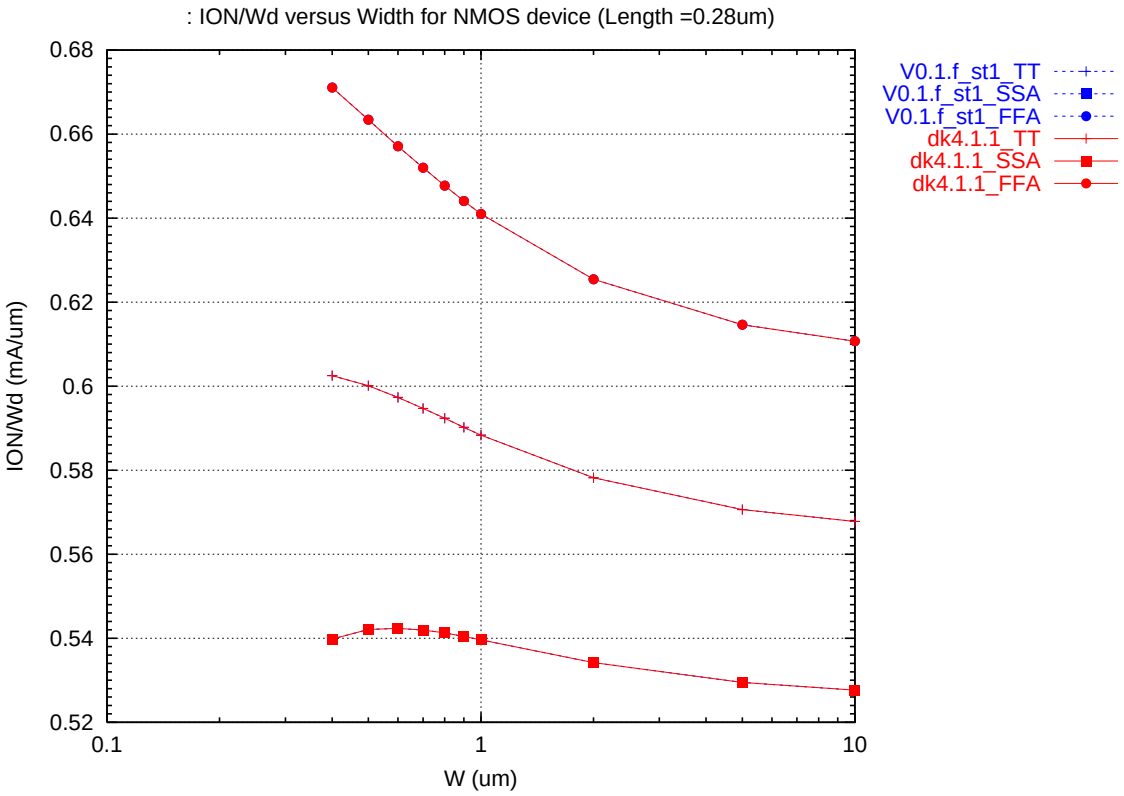

Figure 8 : ION versus drawn channel width for NMOS SVT_2V5 transistors (L = 0.28 µm)

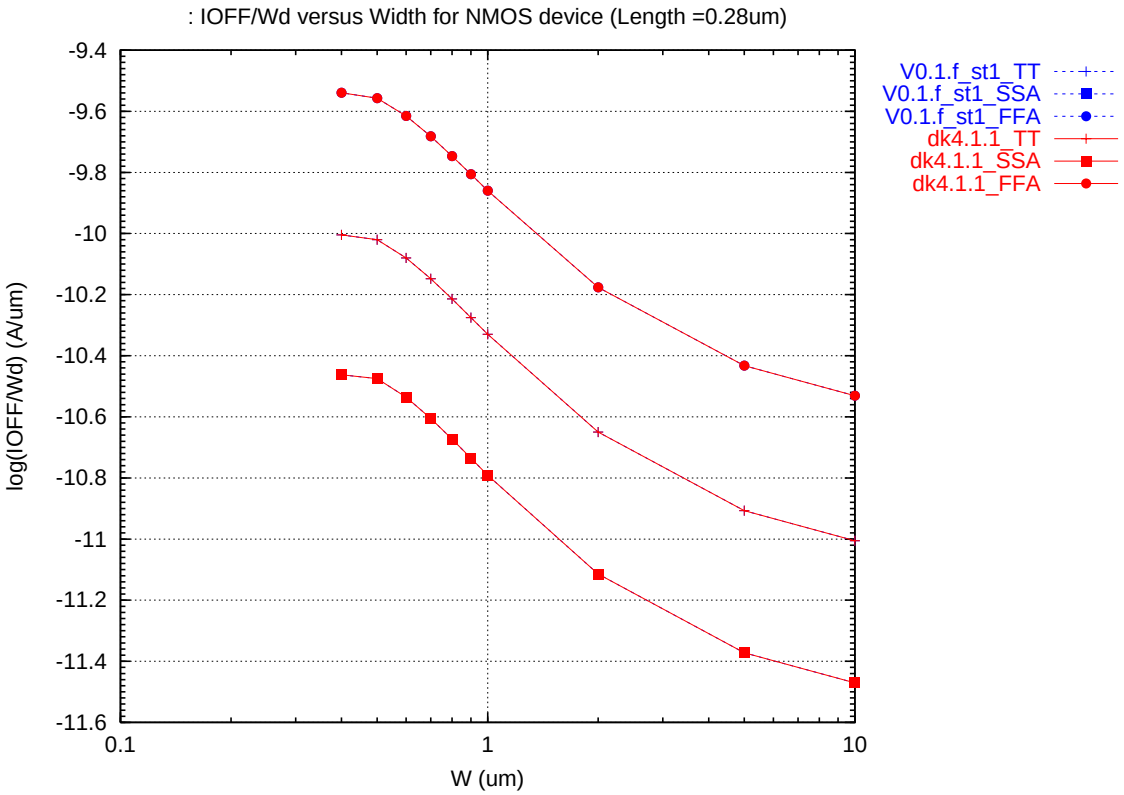

Figure 9 : IOFF versus drawn channel width for NMOS SVT_2V5 transistors (L = 0.28 µm)

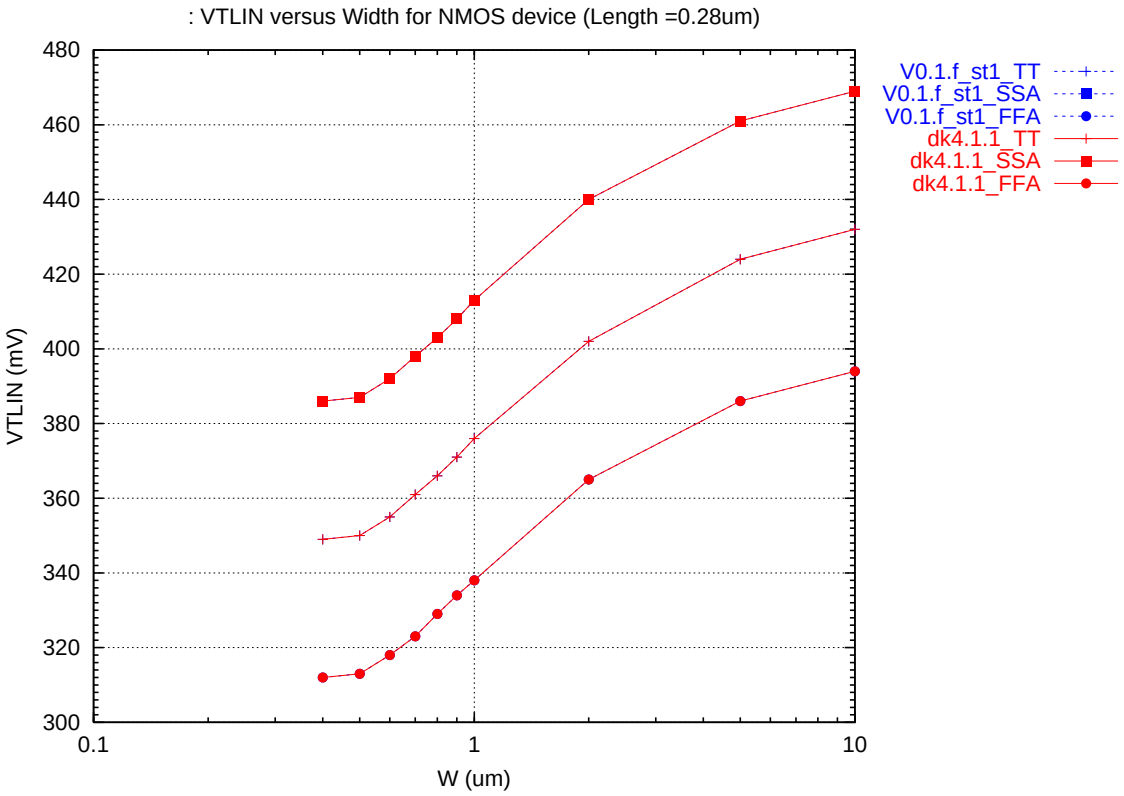

Figure 10 : Threshold voltage VTLIN versus drawn channel width for NMOS SVT_2V5 transistors (L = 0.28

6. ELECTRICAL BEHAVIOR VERSUS GATE LENGTH AND CHANNEL WIDTH FOR PMOS SVT_2V5 TRANSISTORS

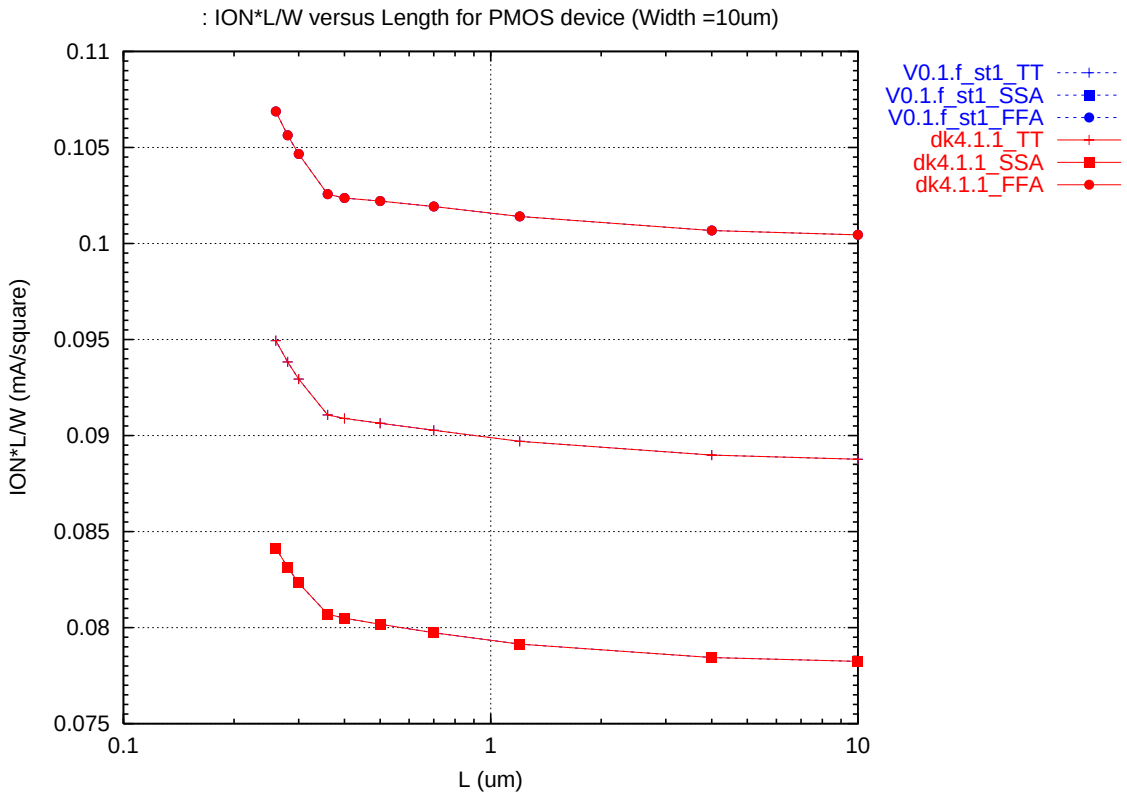

Figure 11 : ION versus drawn gate length for PMOS SVT_2V5 transistors (W = 10 µm)

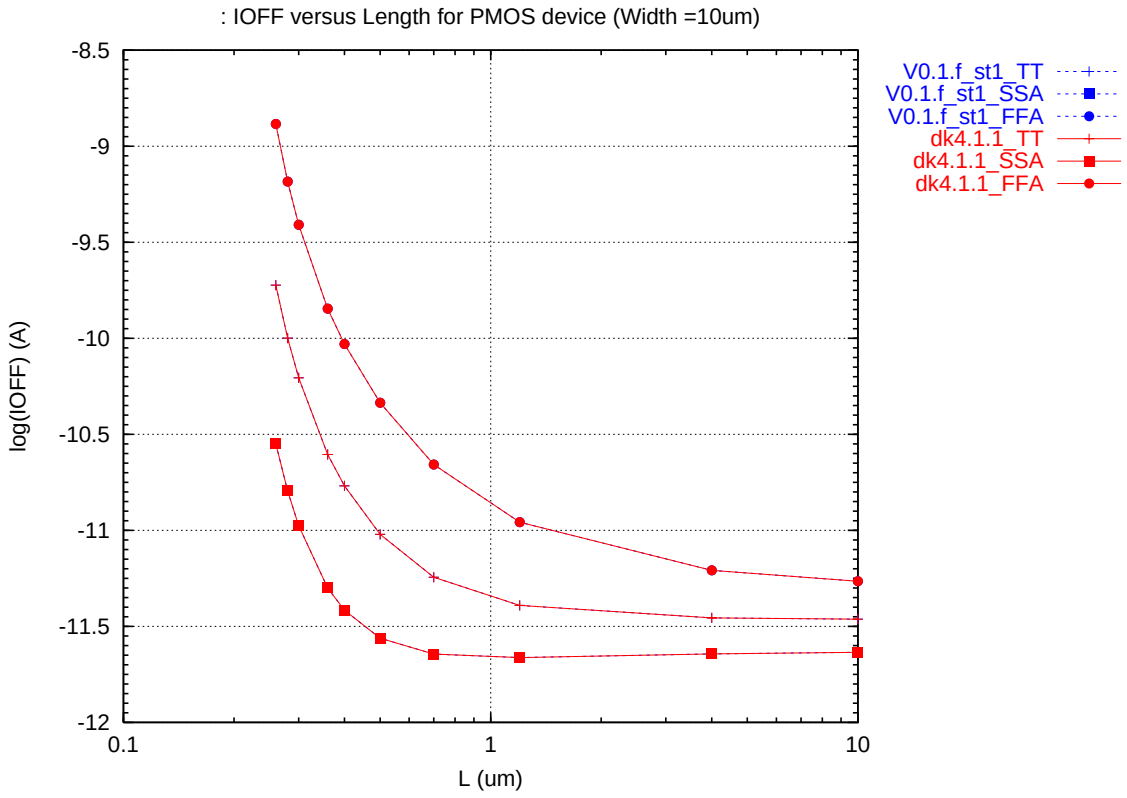

Figure 12 : IOFF versus drawn gate length for PMOS SVT_2V5 transistors (W = 10 µm)

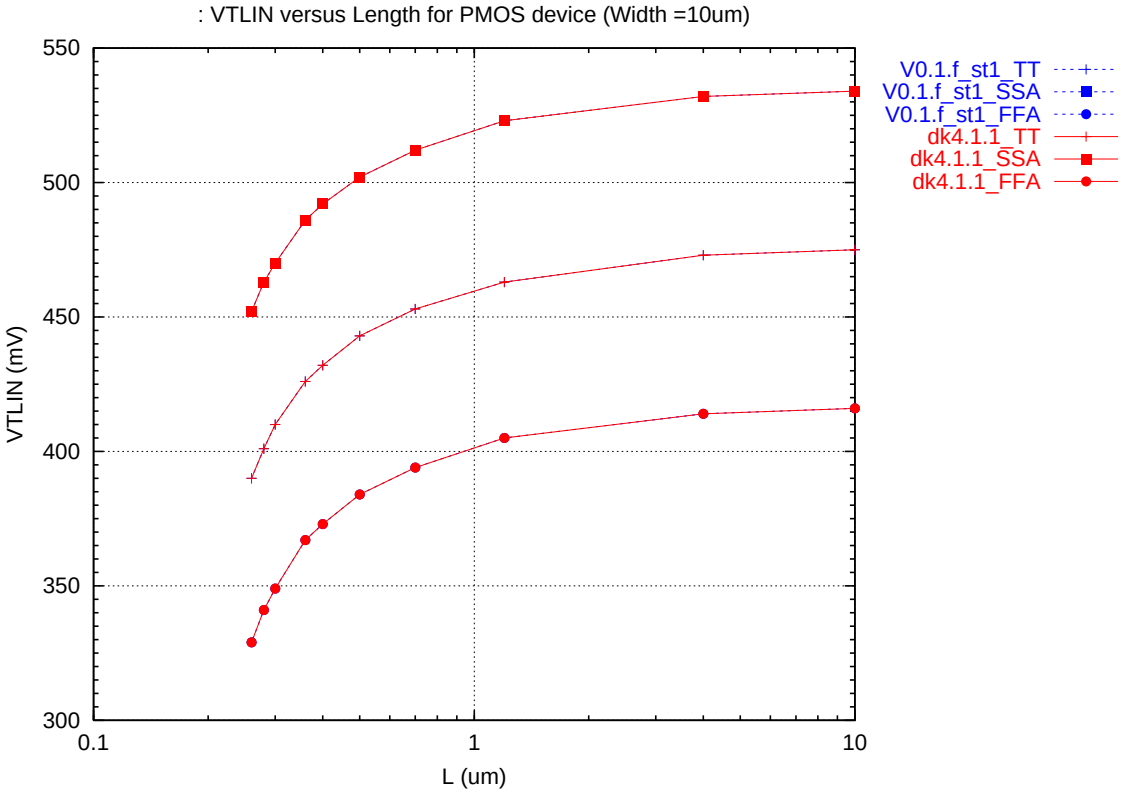

Figure 13 : Threshold voltage VTLIN versus drawn gate length for PMOS SVT_2V5 transistors (W = 10 µm)

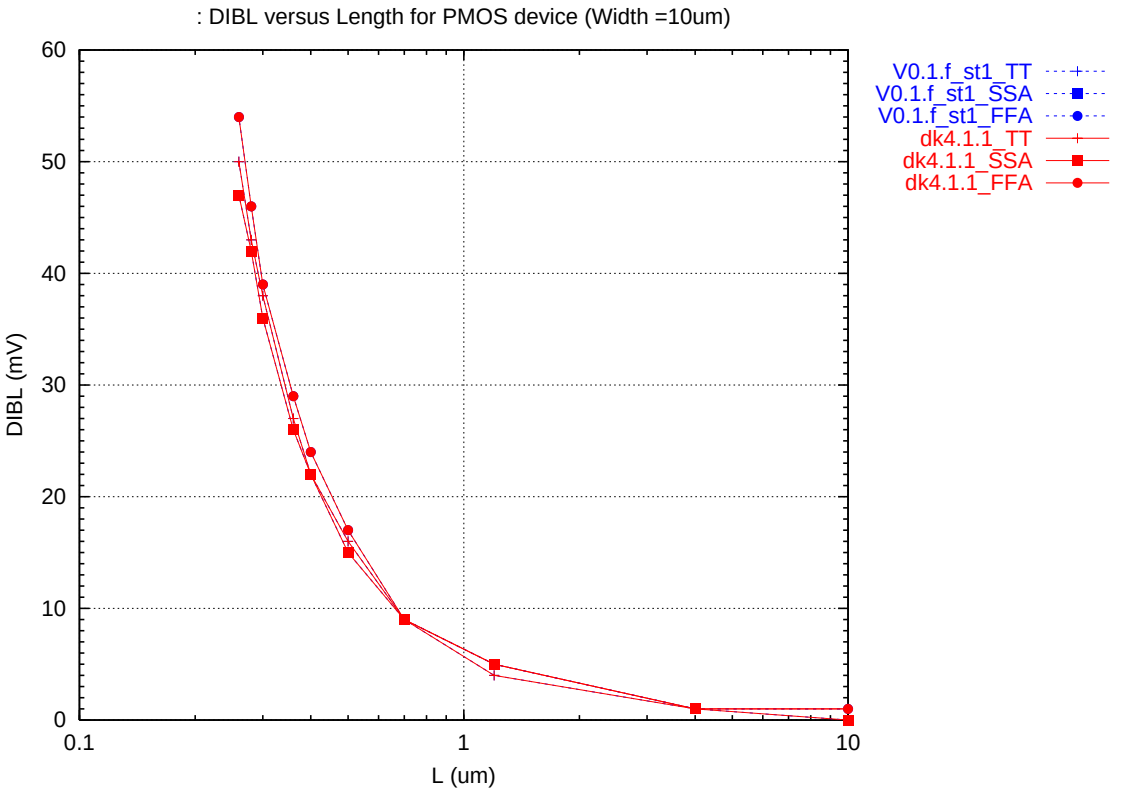

Figure 14 : DIBL= VTLIN-VTSAT versus drawn gate length for PMOS SVT_2V5 transistors (W = 10 µm)

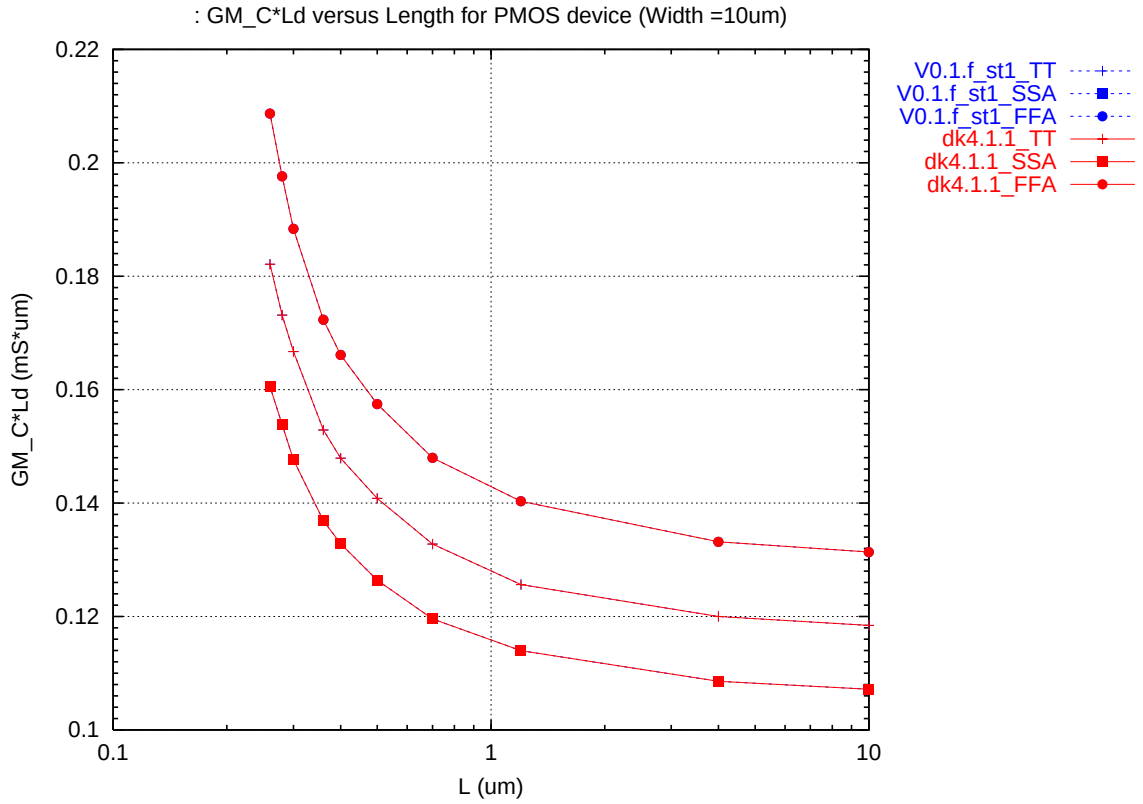

Figure 15 : GM*Ld versus drawn gate length for PMOS SVT_2V5 transistors (W = 10 µm)

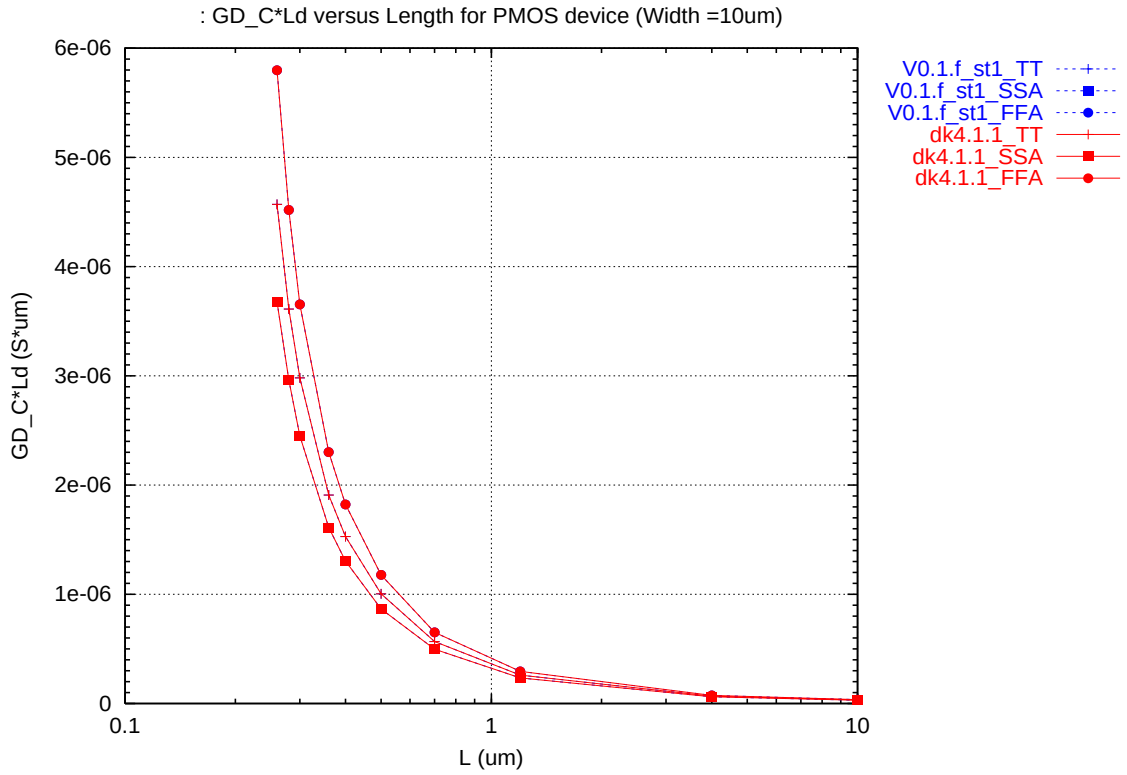

Figure 16 : GD*Ld versus drawn gate length for PMOS SVT_2V5 transistors (W = 10 µm)

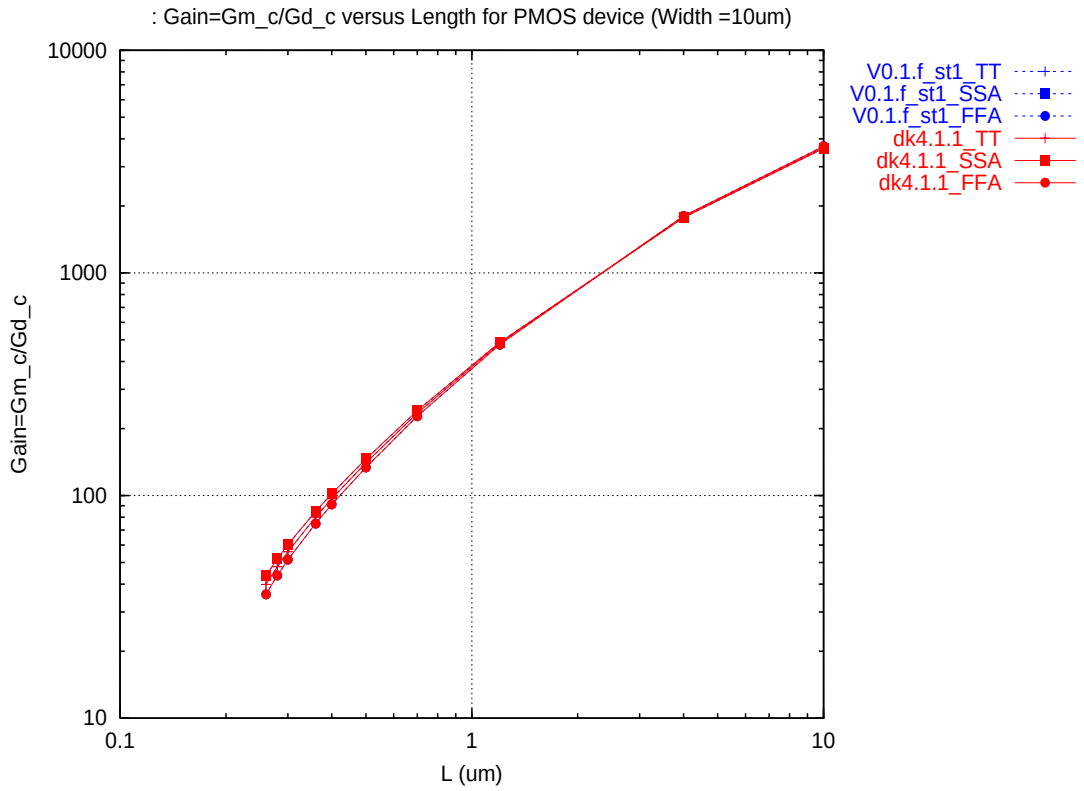

Figure 17 : GAIN versus drawn gate length for PMOS SVT_2V5 transistors (W = 10 µm)

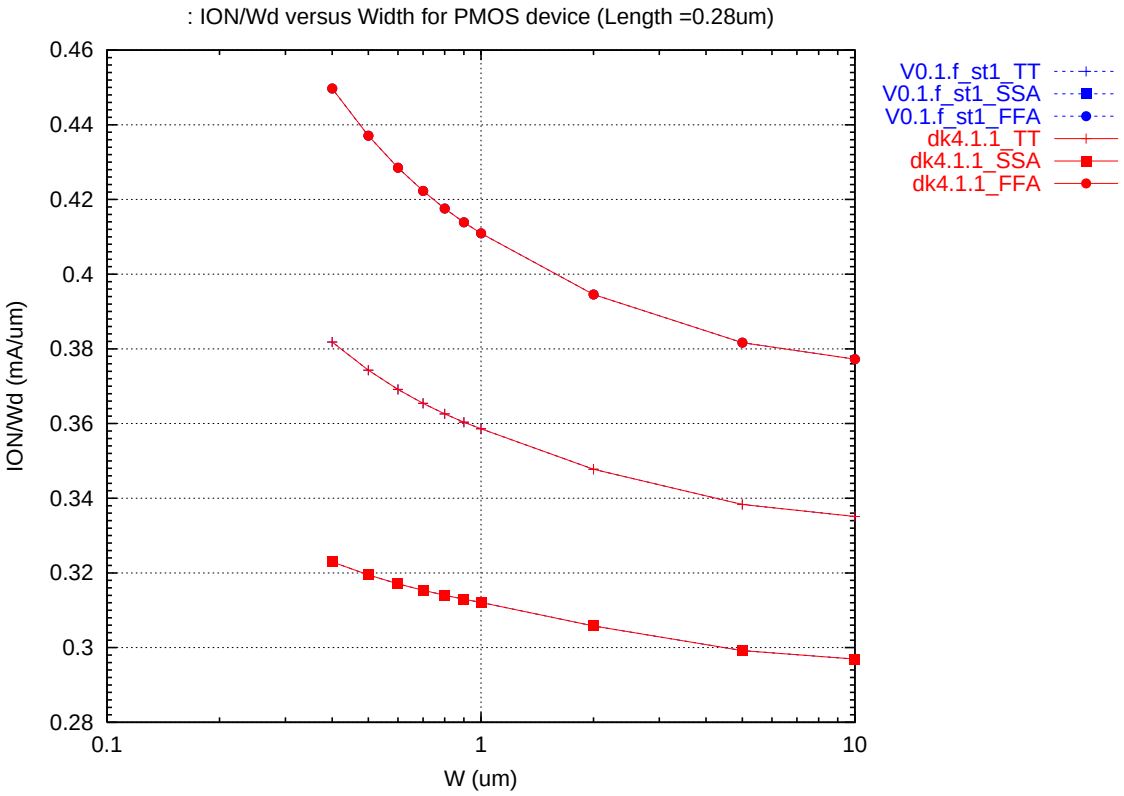

Figure 18 : ION versus drawn channel width for PMOS SVT_2V5 transistors (L = 0.28 µm)

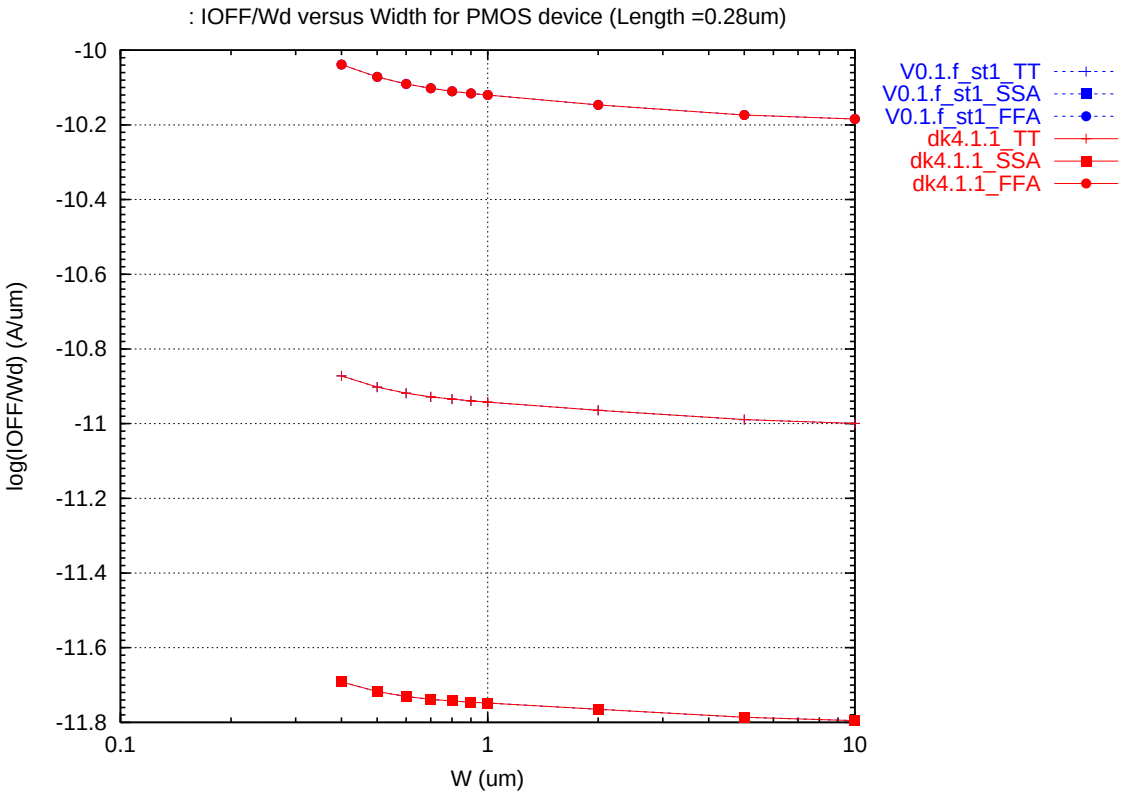

Figure 19 : IOFF versus drawn channel width for PMOS SVT_2V5 transistors (L = 0.28 µm)

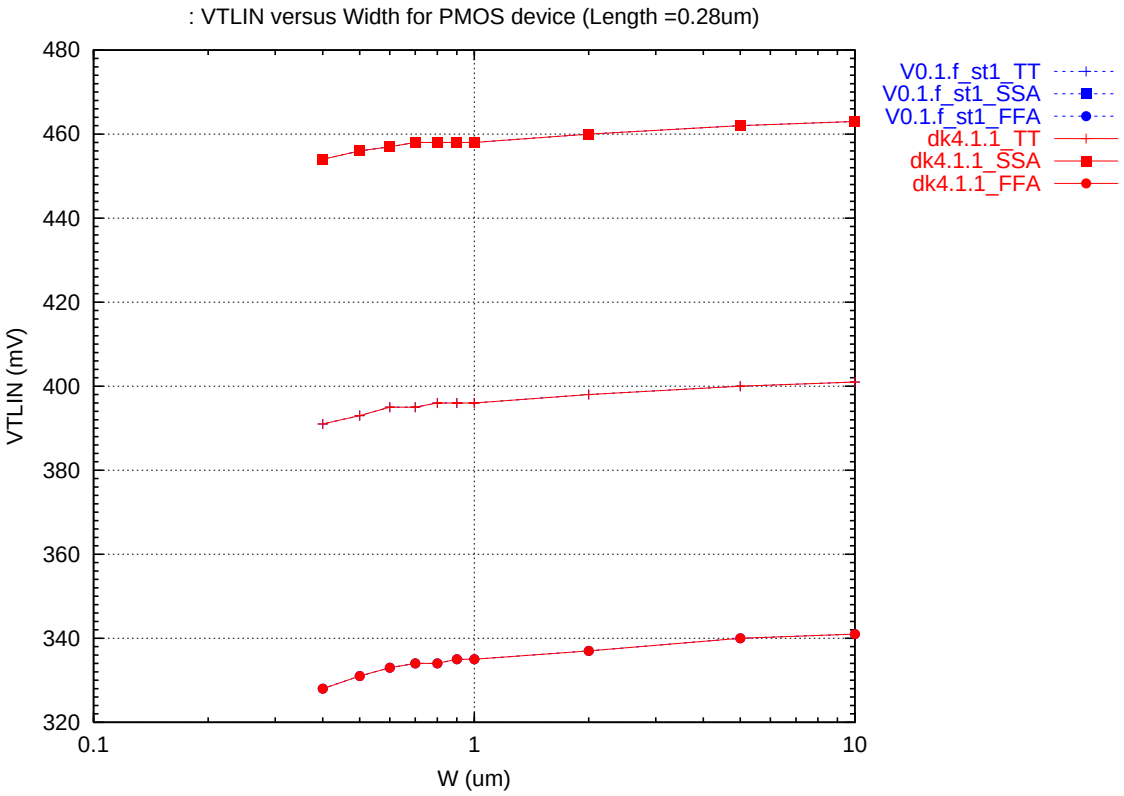

Figure 20 : Threshold voltage VTLIN versus drawn channel width for PMOS SVT_2V5 transistors (L = 0.28 µm)