Implementation of Low-Power 6–8 b 30–90 GS/s Time-Interleaved ADCs With Optimized Input Bandwidth in 32 nm CMOS

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***Abstract*—A model for voltage-based time-interleaved sampling is introduced with two implementations of highly interleaved analog-to-digital converters (ADCs) for 100 Gb/s communication systems. The model is suitable for ADCs where the analog input bandwidth is of concern and enables a tradeoff between different architectures with respect to the analog input bandwidth, the hold time of the sampled signal, and constraints on the clock path. The two ADCs at 6 and 8 b resolution implement inline demux sampling with $32\times$ and $64\times$ interleaving to achieve 36 GS/s at 110 mW and 90 GS/s at 667 mW, respectively. The analog input bandwidth of both ADCs exceeds 20 GHz. The SNDR of the $64\times$ interleaved ADC is above 36 dB up to 6.1 GHz and above 33 dB up to 19.9 GHz at 90 GS/s, and the SNDR of the $32\times$ interleaved ADC exceeds 31.6 dB up to Nyquist at 36 GS/s. The $32\times$ and $64\times$ interleaved ADCs are optimized for area and occupy 0.048 and 0.45 mm^2, respectively, in 32 nm CMOS SOI technology.**

***Index Terms*—Analog-to-digital converter (ADC), successive approximation (SAR), 100 GBE, interleaver, time-interleaved, sampling, bandwidth model, inline demux, asynchronous, alternate comparators.**

I. Introduction

TIME-INTERLEAVED analog-to-digital converters (ADCs) have been gaining popularity in the past few years, not only because communication systems require faster converters, but also because newer CMOS technologies no longer provide significant speed advantages. Furthermore, successive approximation (SAR) ADCs, known for their flexible architecture, power efficiency, and suitability for digital CMOS processes, became much more popular over Flash and pipelined ADCs, although they generally run at a slower clock rate. The combination of highly optimized SAR ADCs with a time-interleaved front-end sampler becomes a powerful architecture to tackle high-speed converter that challenges at 10 GS/s and beyond [1]–[5]. Recent and emerging wired communication standards are increasingly building on ADCs. The 100 Gb/s Ethernet standard IEEE 802.3bj uses four lanes with NRZ or PAM-4 coding and suggests sampling rates close to 30 GS/s at 5–6 b effective resolution [6]. The long-haul optical communication standard ITU-OTU4 transmits 100 Gb/s over a single wavelength of a fiber by using two polarization phases with I and Q. To overcome aliasing issues, the sampling rate is assumed to be twice the bit rate, which is 56–65 GS/s, including forward error correction. Future standards will use higher-order modulation such as PAM-16 or more to increase the data rate in the same band in addition to increasing the symbol rate. Thus, the need for ADCs with at least 8 b resolution at high sampling rates will continue to grow.

Up to a resolution of 6 b efficient Flash ADCs can be found [7]. For resolutions $>$ 6 b, however, SAR ADCs become attractive because of their low total number of comparisons to determine the digital output and the absence of amplification during conversion as found in pipelined ADCs. The latter in particular simplifies a converter which runs at low supply voltage. The fastest SAR ADCs are just above 1 GS/s [1], [8], [9]. As a result, a high interleaving factor of a few tens [1], [4], [5] to a few hundreds [2], [3] will be necessary. Time-interleaved ADCs represent a divide-and-conquer approach as power and area are generally determined by the sub-ADC, whereas speed, bandwidth, and interleaving accuracy are determined by the front-end interleaver. The term interleaver defines an analog input-signal demultiplexing structure that may include a sampling stage and/or buffers.

Two different approaches for sampling the input signal onto the sub-ADCs are used. Charge-based sampling is implemented in [3], and voltage-based sampling is found in [1], [2], [4], and [5]. This paper focuses on voltage-based sampling at high sampling rates, where the analog input bandwidth becomes a limiting factor, and the hold time of the sampled signal is an issue. Interleaving error calibration and correction are not part of this paper.

Section II presents fundamental ADC limits and design tradeoffs for efficient high-speed, low-power ADCs.

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Section III provides a detailed analysis of voltage-based time-interleaving architectures suitable for high-speed ADCs with, but not limited to, low-to-medium resolution. Key aspects, in particular the relation between the analog input bandwidth of an interleaved sampler and the hold time available to process the sample, are analyzed in detail.

Section IV highlights the implementation and measurement results of a high-speed CMOS ADC at 90 GS/s and 8 bit resolution, and a low-power implementation at 36 GS/s and 6 bit resolution based on the models derived in the first part. While the 90 GS/s ADC is tuned for maximum performance and consumes 667 mW, the 36 GS/s ADC is optimized for minimum power and area and runs on 110 mW with an area of 0.048 mm^2. Both designs are implemented in a digital 32 nm CMOS SOI process.

II. High-Speed ADC Design Considerations

First, key properties of interleaved ADC designs are highlighted, which help identify the requirements for the interleaver and sub-ADCs. The second part provides a noise and distortion analysis for an ADC to help assign design specifications to the blocks.

A. Requirements for Interleaved ADCs

The limitations for high-speed ADCs largely differ from those of lower-speed designs. Generally, interleaved designs enable the separation of ADC requirements into those for the interleaver and those for the sub-ADCs. In most high-speed designs, the interleaver consumes significantly less power and area than the total of the sub-ADCs [1], [2], [4], [5]. Therefore, it is crucial to optimize the sub-ADCs for minimum total area and total power. This means that a single sub-ADC should have the best speed-per-power and speed-per-area ratios possible. A small area of the sub-ADC array is also beneficial for the signal routing from the interleaver to the sub-ADCs. The interleaver has to fulfill requirements on the analog input bandwidth and nonlinearity. Both the sub-ADCs and the interleaver contribute to the total noise budget. Generally, the higher the speed and precision requirements of an ADC are, the larger the portion of the noise budget that should be allocated to the interleaver, as the interleaver is more strongly bound by technology constraints than the sub-ADC.

In an interleaved ADC, mismatch of components results in mismatch between the ADC channels. Skew and bandwidth mismatches only affect the first sampling stage, but gain mismatch and offset can also be introduced by the sub-ADCs.

B. Noise and Distortion Budget of an ADC

The signal-to-noise and distortion ratio (SNDR) is given by

$$\mathrm{SNDR_{tot}} = 10\log\frac{\frac{1}{2}A^2}{\frac{V_{\mathrm{i,pp\text{-}diff}}^2}{2^{2N}}\left(\frac{1}{12}+\frac{1}{4}\sigma_{\mathrm{DNL}}^2+\sigma_{\mathrm{INL}}^2\right)+(\sqrt{2}\pi f_{\mathrm{in}}A\sigma_{\mathrm{j}})^2+\sigma_{\mathrm{n}}^2} \quad (1)$$

where A is the amplitude of the input signal, $V_{\mathrm{i,pp\text{-}diff}}$ the maximum peak-peak differential input voltage, and N the resolution of the ADC; σ_{DNL} and σ_{INL} are the standard deviation of the DNL and INL in LSBs, respectively; f_{in} is the input frequency, σ_{j} the standard deviation of the timing jitter in seconds, and σ_{n} the thermal noise of the ADC [10], [11]. Effects from time interleaving are not reflected in (1).

The first term in the denominator is quantization noise ($V_{\mathrm{i,pp\text{-}diff}}^2/(12\cdot 2^{2N})$) and is only influenced by the sub-ADC. INL, DNL, and thermal noise have contributions from both the interleaver and the sub-ADC. Important contributors are the nonlinearity of the interleaver and the kT/C noise of the sampling capacitor. The noise of the $2\times 50\ \Omega$ differential input termination resistors limits an ADC design with 50 GHz input bandwidth to 56 dB SNDR at 100 °C with 500 mV$_{\mathrm{pp,diff}}$ [12] and is thus neglected.

Timing jitter solely impacts the interleaver up to the first sampling stage. The clock signal, which is used to sample the ADC input signal, exhibits timing jitter, which is mainly caused by thermal noise and noise on the power supply. The latter can be minimized by careful layout, decoupling, and wiring of separate power domains. The available power budget on the clock path determines the minimum achievable clock jitter due to thermal noise. As four times the power is required to reduce clock jitter by a factor of 2, it is expensive in terms of power to reduce clock jitter beyond a certain threshold. The most advanced designs exhibit around 50–60 fs clock jitter [3], [4]. The SNDR limit from jitter in (1) [11] can be written as

$$\mathrm{SNDR_{jitter}} = -20\log(2\pi f_{\mathrm{in}}\sigma_{\mathrm{j}}). \quad (2)$$

As can be seen from (2), even 50 fs jitter is of importance at high input frequency. In most applications, the input signal amplitude fortunately is attenuated at higher input frequencies, and the assumption of a full-scale input signal at the upper end of the band of interest is pessimistic. Moreover, assuming that a sinusoidal input imposes too higher than a jitter requirement is realistic [13].

III. High-Speed Interleaver Analysis

The aim of this section is to create a foundation for deciding which interleaving architecture suits given specifications best. The models derived here relate the analog input bandwidth to the hold time on the sampling capacitor and highlight requirements on the sampling clock. The analysis applies for different switch types, e.g., for NMOS or PMOS switches and boot-strapped switches, with or without signal feed through compensation.

A. Voltage-Based Interleaver Architectures

Different types of voltage-based interleavers can be used. They will be categorized as direct sampling [2] and inline demux sampling [4], [5] in our work. Both designs implement subsampling to achieve a larger interleaving ratio.

Direct sampling, shown in Fig. 1, provides the shortest path from the input to the sampling capacitor with minimum resistance. One or more of the sampling switches are closed at the

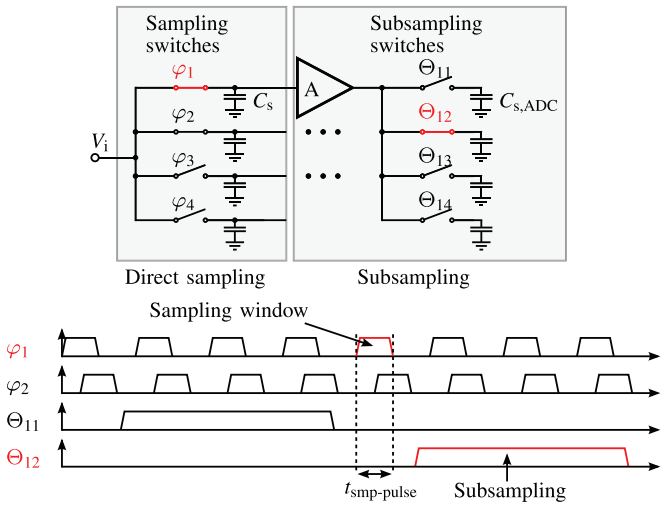

Fig. 1. Direct sampling with buffered subsampling [2]. Waveforms are shown for 50% duty cycle clocking.

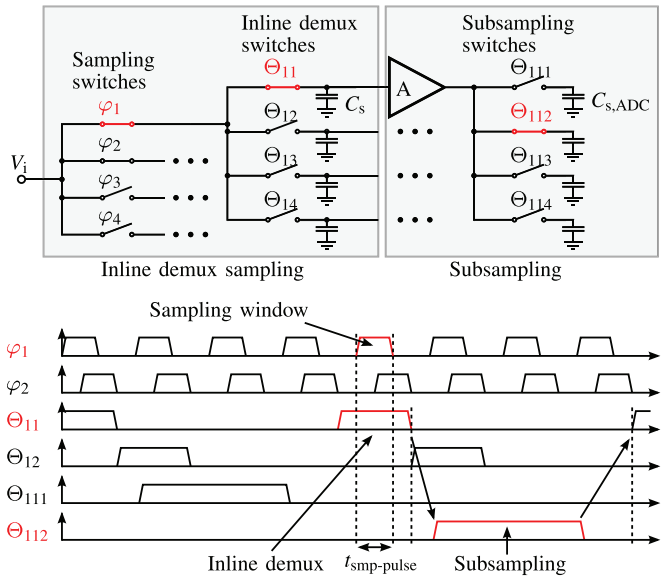

Fig. 2. Inline demux sampling with buffered subsampling [4].

same time. If only one switch is closed at a time, the highest bandwidth results but the shortest sampling pulses are required. Direct sampling is very efficient for a small number of parallel switches (usually ≤ 8; see [2]), as too many switches will increase the input capacitance at the node V_i. The sampled voltage is stored on the sampling capacitor C_s and forwarded through a buffer and demux structure to the sampling capacitor of the sub-ADC $C_{s,ADC}$.

Inline demux sampling, see Fig. 2, stacks two switches to reduce the number of parallel switches at the input. The inline demux switch closes before the sampling switch closes and opens after the sampling switch opens. Thus, the sampling time depends only on the falling edge of the sampling switch clock. The use of inline demux switches significantly reduces the number of timing critical clock signals. The interleaver in [4] only requires four clock signals with a 50% duty cycle, thus greatly relaxes the clock signal constraints. The increased

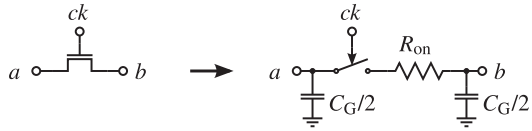

Fig. 3. Simplified switch model.

resistance of two series-connected switches is accompanied by a smaller input capacitance because of the smaller number of parallel sampling switches.

B. Interleaver Model

The analog input bandwidth of an interleaver depends on the size of the sampling capacitor, which is usually sized not much larger than required by the kT/C noise for the target SNDR. Furthermore, the analog input bandwidth depends on the input network. For high-speed ADCs, the input is often terminated with a 50 Ω resistor to reduce signal reflections. The ADC sees a 25 Ω resistance from the termination resistor and the input source resistance. A lower resistance is beneficial to obtain a higher bandwidth, and could be achieved, e.g., by introducing a buffer with a low output impedance or using a resistive divider as termination resistor. The former has an inherent bandwidth limit due to the buffer transistors, and the latter reduces the signal swing at the ADC.

For a given input resistance and capacitor size, the remaining degree of freedom is the architecture of the interleaver, specifically, the number of switches in each stage and their sizing.

To obtain more insight into direct and inline demux sampling interleavers, a simplified switch model is applied, as shown in Fig. 3. The gate capacitance C_G is equal to the total gate capacitance to source, drain and bulk, i.e., $C_G = C_{GS} + C_{GD} + C_{GB}$. The resistor R_{on} represents the on-resistance of the switch. The model assumes constant C_{GD} and C_{GS}, independent of the gate voltage. Because the capacitance associated with drain and source consists not only of the transistor parasitics C_{GD} and C_{GS}, but also of the wire parasitic capacitance associated with the switch, the error introduced by this assumption is tolerable. Note that the model does not take into account leakage from the sampling capacitor through a switch in off-state; this must be handled by choosing the switch operating point correctly.

To further simplify the model, C_G and R_{on} are linked with the technology transition frequency f_T

$$f_T = \frac{g_m}{2\pi C_G} \tag{3}$$

by setting $R_{on} = 1/g_m$ [14]. For a given f_T and R_{on} of a switch, its C_G is then

$$C_G = \frac{1}{2\pi R_{on} f_T}. \tag{4}$$

According to the model assumptions, the effective transition frequency (which includes parasitics from the full layout) $f_{T,eff}$ of an NMOS (or PMOS) switch is equivalent to the technology-dependent f_T. Wiring on both ends of the switch increases C_G

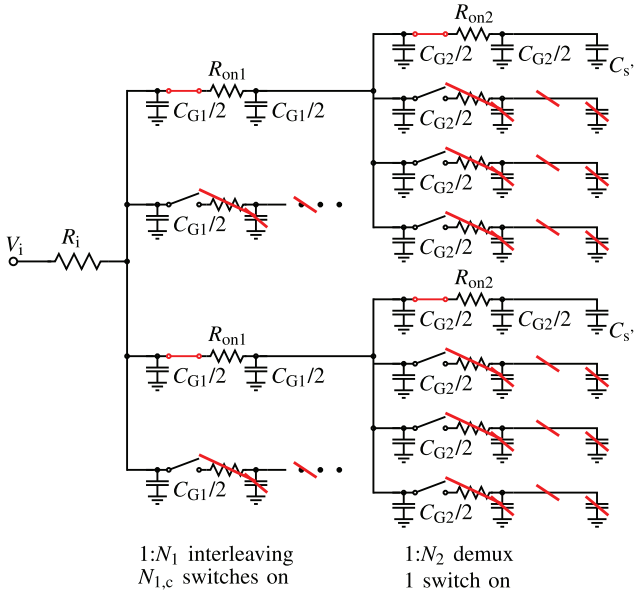

Fig. 4. Inline demux interleaver (Fig. 2) with simplified switch model of Fig. 3. Elements that are disconnected from open switches are crossed out in red.

and R_{on} and is taken into account by

$$f_{T,eff} = pf_T \tag{5}$$

where p is a correction factor taking the parasitic capacitors and resistors into account. Differential NMOS (or PMOS) switches with cross-coupled transistors with gates connected to ground for feed-through compensation result in half the f_T of NMOS (or PMOS) switches without feed-through compensation when the model of Fig. 3 is applied. Boot-strapped switches will have a lower R_{on} but a higher capacitance attached to one side of the switch because of the circuitry connected for a constant V_{GS}.

The f_T correction factor p can be found by calculating the ratio of the extracted layout parasitic capacitance and resistance due to the wiring of a sampling switch to those of a sampling switch without wiring, or by simulating the transfer function of an extracted interleaver and fitting p. Different interleavers in the same technology are assumed to have a very similar p.

C. Inline Demux Sampling Model

Applying the model of Fig. 3 to our interleaver in Fig. 2 results in the equivalent circuit shown in Fig. 4. The sampling capacitor $C_{s'}$ is defined as $C_s = C_s' - C_{G2}/2$. Thus, the total sampling capacitance, which defines the kT/C noise limit of the converter, is C_s. The input resistance to the interleaver is R_i.

The sampling switch in [4] is implemented as a single NMOS switch, and the inline demux switch uses feed-through compensation to improve the differential isolation between the sampling capacitor and the nodes between sampling switch and inline demux switch during hold time. The $f_{T,eff}$ of the sampling switch $f_{T,eff1}$ links R_{on1} with C_{G1}, and $f_{T,eff2}$ links R_{on2} with C_{G2} of the inline demux switches by (4). The architecture is parametrized by the number of sampling switches N_1, the number of sampling switches concurrently turned on $N_{1,c}$, and the number of inline demux switches N_2. The inline demux

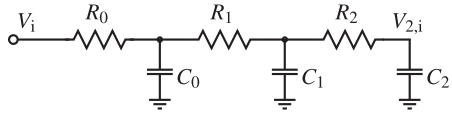

Fig. 5. RC equivalent of the inline demux interleaver from Fig. 4.

sampling architecture shown in Fig. 2 uses $N_1 = 4$ sampling switches, of which $N_{1,c} = 2$ are turned on concurrently, and $N_2 = 4$ inline demux switches.

The circuit of Fig. 4 can be simplified into an RC filter, as shown in Fig. 5. The elements of the RC circuit can be expressed by the architecture parameters N_1, $N_{1,c}$, N_2, the switch parameters R_{on1}, $f_{T,eff1}$, R_{on2}, $f_{T,eff2}$, the size of the total sampling capacitor C_s, and the input resistance R_i

$$\begin{aligned} R_0 &= R_i, & C_0 &= N_1\frac{C_{G1}}{2} \\ R_1 &= \frac{R_{on1}}{N_{1,c}}, & C_1 &= N_{1,c}\frac{C_{G1}}{2} + N_{1,c}N_2\frac{C_{G2}}{2} \\ R_2 &= \frac{R_{on2}}{N_{1,c}}, & C_2 &= \max\left(N_{1,c}\frac{C_{G2}}{2}, N_{1,c}C_s\right). \end{aligned} \tag{6}$$

The transfer function from V_i to $V_{2,i}$ can be used to calculate the 3 dB analog input bandwidth and is given by

$$\begin{aligned} \frac{V_{2,i}}{V_0} = &[((1+sR_2C_2)(1+sR_1C_1)+sR_1C_2)(1+sR_0C_0) \\ &+ (1+sR_2C_2)sR_0C_1 + sR_0C_2]^{-1} \end{aligned} \tag{7}$$

where $s = j\omega = j2\pi f_i$ and f_i is the input frequency. The 3 dB bandwidth $f_{i,3dB}$ is defined by

$$\left.\frac{V_{2,i}}{V_i}(f_i)\right|_{f_i=f_{i,3dB}} = \frac{1}{\sqrt{2}}. \tag{8}$$

It can be calculated from (6)–(8) and written as

$$f_{i,3dB} = f_{i,3dB}(R_1, R_2, N_1, N_{1,c}, N_2, R_i, C_s, f_{T,eff1}, f_{T,eff2}). \tag{9}$$

Fig. 2 shows that the signal is sampled every $N_1N_2 = 16$ periods to the same capacitor and that it is constant during this time except for the duration of the inline demux switch pulse, which is assumed to be twice the width of the sampling pulse width $t_{smp\text{-}pulse}$. The sampling pulse width $t_{smp\text{-}pulse}$ is assumed to be

$$t_{smp\text{-}pulse} = \begin{cases} N_{1,c}t_s & \text{for } N_1 \geq 2 \\ \frac{1}{2}t_s & \text{for } N_1 = 1 \end{cases} \tag{10}$$

where the sampling period of the ADC is $t_s = 1/f_s$ and the ADC sampling frequency is f_s. The master sampling interleaver with $N_1 = 1$ is a special case in which the width of the sampling window cannot be equal to $N_{1,c}t_s$, as otherwise the sampling switch would always be closed. Hence, the sampling pulse length is assumed to be half the sampling period t_s.

The hold time $t_{h,i}$ on the sampling capacitor C_s in Fig. 2 can be calculated as

$$t_{h,i} = N_1N_2t_s - 2t_{smp\text{-}pulse} \tag{11}$$

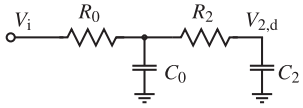

Fig. 6. RC equivalent of a direct interleaver, as shown in Fig. 1.

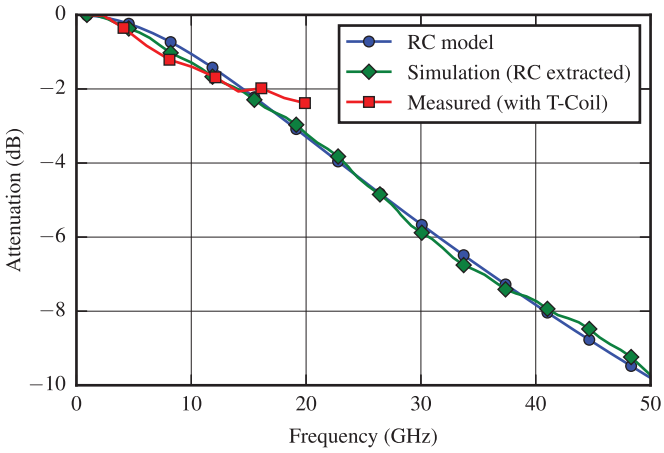

Fig. 7. Attenuation versus input frequency. The model parameters are $N_1 = 4$, $N_{1,c} = 2$, $N_2 = 4$, $R_i = 25\ \Omega$, $C_s = 32$ fF, $f_T = 300$ GHz [15], and $p = 0.7$.

which is

$$t_{h,i} = \begin{cases} (N_1 N_2 - 2N_{1,c})t_s & \text{for } N_1 \geq 2 \\ (N_1 N_2 - 1)t_s & \text{for } N_1 = 1. \end{cases} \quad (12)$$

D. Direct Sampling Model

The same analysis for direct sampling leads to a simplified RC circuit, as shown in Fig. 6, by eliminating R_1 and C_1.

The definitions of R_0, C_0, R_2, and C_2 are the same as in (6), but R_2 and C_2 characterize the sampling switches, of which N_1 are in parallel and $N_{1,c}$ are concurrently turned on. The transfer function for direct interleaving is given by

$$\frac{V_{2,d}}{V_i} = \frac{1}{(1 + sR_2C_2)(1 + sR_0C_0) + sR_0C_2}. \quad (13)$$

For direct sampling, the hold time can be calculated as

$$t_{h,d} = N_1 t_s - t_{smp\text{-}pulse} \quad (14)$$

which equals

$$t_{h,d} = \begin{cases} (N_1 - N_{1,c})t_s & \text{for } N_1 \geq 2 \\ \frac{1}{2}t_s & \text{for } N_1 = 1. \end{cases} \quad (15)$$

The transient simulation of the clocked interleaver with extracted R and C values and the measurement results match the inline demux model well (see Fig. 7).

The measured ADC attenuation versus frequency includes a T-coil at the input to eliminate part of the ESD capacitance and results in some peaking, as can also be seen in Fig. 7. Inductance of wires is neither modeled nor simulated. As the wire lengths on chip are usually much shorter than the wavelength of the sampled signal, the effect of wire inductance is not significant, In general, omitting the wire inductance results in a slightly lower bandwidth in the model.

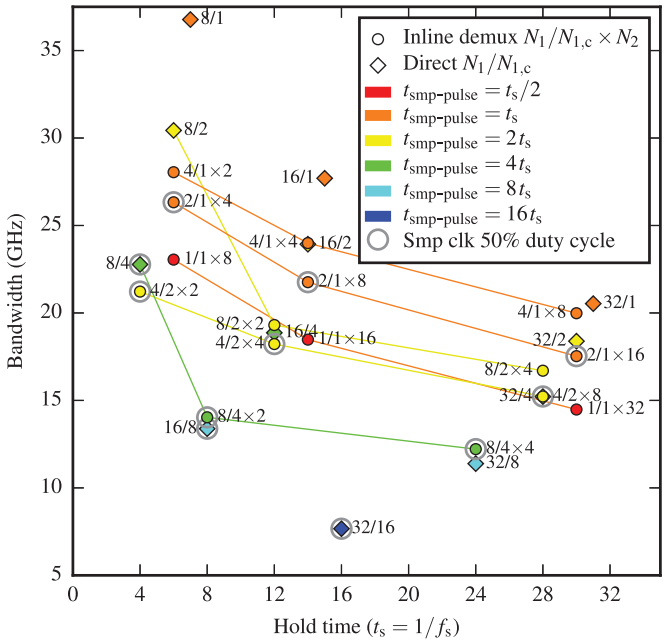

Fig. 8. Maximum achievable 3 dB bandwidth versus hold time for different inline demux sampling and direct sampling configurations. Parameter assumptions are $R_i = 25\ \Omega$, $C_s = 32$ fF, $f_T = 300$ GHz, and $p = 0.7$. Feed-through compensation for the switches connected to the sampling capacitors is assumed.

E. Comparison and Discussion

It is computationally easy to maximize the 3 dB bandwidth of, e.g., the architecture in Fig. 2 for given N_1, $N_{1,c}$, N_2, f_T, and p by finding the optimum resistance R_{on1} (and R_{on2}) for the sampling switch and inline demux switch. The power of the interleaver bandwidth analysis is revealed when this optimization is carried out for different architecture parameters, i.e., N_1, $N_{1,c}$, and N_2 for inline demux sampling or N_1 and $N_{1,c}$ for direct sampling, respectively, as seen in Fig. 8.

The hold time of the sampled voltage on the sampling capacitor is used to process the sample, which often means buffering the sample and connecting it by subsampling to a sub-ADC. To eliminate ISI, a reset of the capacitor is required, which increases the hold time. The hold time is therefore given by the time to transfer the sample to the sub-ADC and the time for reset. Fig. 8 shows that a lower hold time enables a higher analog input bandwidth. The analysis for a three-stage inline demux interleaver was also carried out but did not show any benefits over inline demux sampling for hold times up to 32 t_s. For a given hold time of the sample in seconds, a higher sampling speed can be achieved with architectures that provide higher interleaving (thus, a longer hold time in number of sampling periods t_s); they are found toward the right in Fig. 8. It can be seen that lower analog input bandwidths can be achieved with interleaving architectures that provide long hold times. Thus, the optimum architecture would have to be in the upper right corner of Fig. 8.

The pulse width for the sampling clock $t_{smp\text{-}pulse}$ puts constraints on the clock logic. The shorter the pulse is, the faster the rise and fall time of the clock signal must be to enable the sampling switch fully. Sampling clock signals without a 50% duty cycle can be achieved by either clock gating [16] or

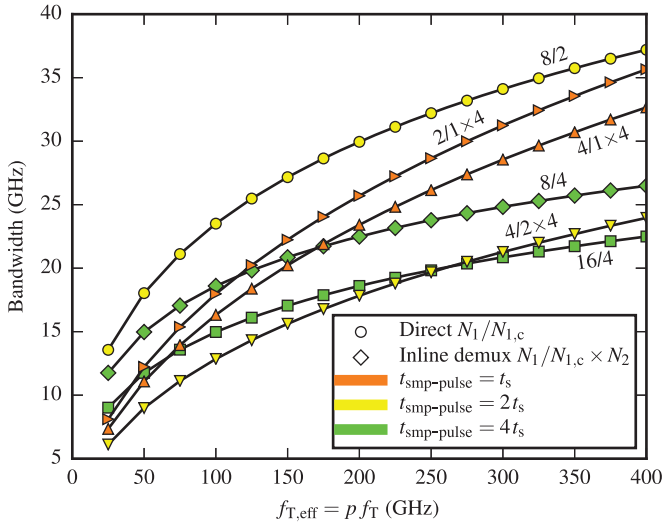

Fig. 9. Maximum achievable 3 dB bandwidth versus $f_{T,eff}$ for different interleaver architectures. Parameters are $R_i = 25\ \Omega$ and $C_s = 32$ fF.

combinatorial logic blocks, such as a NAND or NOR. With the former, the maximum clock frequency required for the ADC is $1/(2\,t_{smp\text{-}pulse})$, which has become critical for high-speed ADCs in recent CMOS processes because electromigration and reliability constraints require wider metal connections at inverters. The additional metal increases the parasitic capacitance and thus limits the maximum achievable clock frequency. The use of combinatorial blocks could relax the maximum clock frequency required to generate the sampling clock signals but adds complexity for mismatch calibration and potentially has a stronger impact on jitter than clock gating. Architecture options with a 50% duty cycle sampling clock are easier to implement and require the least elements in the clock path, which are beneficial for mismatch and jitter.

Also, the lower the number of clock signals, the easier it is to achieve sufficient phase accuracy. The simplest form is a single clock, as it is used in a master sampling interleaver [17]. It cannot achieve the same bandwidth efficiency as an interleaver with two critical phases, because the input signal is only loaded 50% of the time. The highest achievable bandwidth is always obtained with only one active clock at a time and two sampling channels ($N_1/N_{1,c} = 2/1$), but this is not practical for high-speed interleavers.

It is interesting to compare that the effect different values of $f_{T,eff}$ have on the achievable bandwidth of different interleaver configurations. The variation in nominal f_T for different high-performance ≤ 65 nm CMOS processes is very little and usually between 250 and 300 GHz, but the layout parasitics also contribute to $f_{T,eff}$, so that newer technologies could benefit slightly. The effect of $f_{T,eff}$ on the maximum achievable interleaver bandwidth is shown in Fig. 9. It can be seen that the optimal choice of interleaver architecture is not necessarily the same for all $f_{T,eff}$. The achievable 3 dB bandwidth increases far less than linearly with $f_{T,eff}$; thus, comparable technologies yield about the same potential for the analog input bandwidth.

The maximum achievable 3 dB bandwidth with $f_{T,eff} \to \infty$ can be found by setting all C_G and R_{on} in (6) to zero. The remaining equivalent circuit is an RC filter consisting of $R_0 = R_i$ and $C_2 = N_{1,c}C_s$. The maximum bandwidth is then given by

$$f_{i,3dB,max} = \frac{1}{2\pi N_{1,c} R_i C_s} \tag{16}$$

which is $199\ \text{GHz}/N_{1,c}$ for $R_i = 25\ \Omega$ and $C_s = 32$ fF. Although increasing $f_{T,eff}$ does not result in a linearly increased 3 dB bandwidth, there is still room for higher analog input bandwidths at faster technology nodes. Equation (16) also explains why the bandwidth increase for high $f_{T,eff}$ on the right-hand side of Fig. 9 is steeper for smaller $N_{1,c}$.

F. Additional Bandwidth Enhancement Techniques

There are several ways to achieve a higher bandwidth than the one shown above, and they can be grouped into different categories, such as reduced input resistance, smaller sampling capacitance, and inductive peaking.

A reduced input resistance is very effective for achieving higher analog input bandwidth [2], [18]. The disadvantage is a loss in signal amplitude. A high-speed input buffer could be used to present a lower impedance to the sampling switches. A source follower is an attractive solution, as highlighted in [19], because it results in a reduced impedance and some peaking. The implementation of such a source follower requires significant power and is not trivial in deep submicron processes because of electromigration issues.

Because of the kT/C limit, a smaller sampling capacitance can usually only be achieved when a higher input amplitude is fed to the interleaver. The resulting third-order distortion has to be addressed by either highly linear switches or digital compensation.

Inductive peaking can be used at various locations in the interleaver to tune out some capacitance and thus reduce the load to the switches and to the input. However, inductors generally occupy a large area and have to be sized carefully.

IV. High-Speed ADC Implementation

This section covers two high-speed CMOS ADCs: a $64\times$ interleaved 8 b ADC at 90 GS/s [4] and a $32\times$ interleaved 6 b ADC at 36 GS/s ADC [5]. Both implement an inline demux interleaver with similar configuration [12].

A. Architecture

Fig. 10 shows a top-level overview of the ADCs. The differential input is terminated by $2 \times 50\ \Omega$, protected with reduced ESD diodes, and directly connected to the sampling and interleaving slices that feed buffered samples to the sub-ADCs. Because of the T-Coil, which is in the input signal path and connects the ESD diodes, a part of the ESD capacitance is not seen at high frequencies. The aggregated digital output is captured by a large high-speed memory block storing 128 samples per sub-ADC. The $64\times$ interleaved ADC requires four clock signals, which are derived from a half-rate differential CML clock with a CML divider. The CML divider consists of two

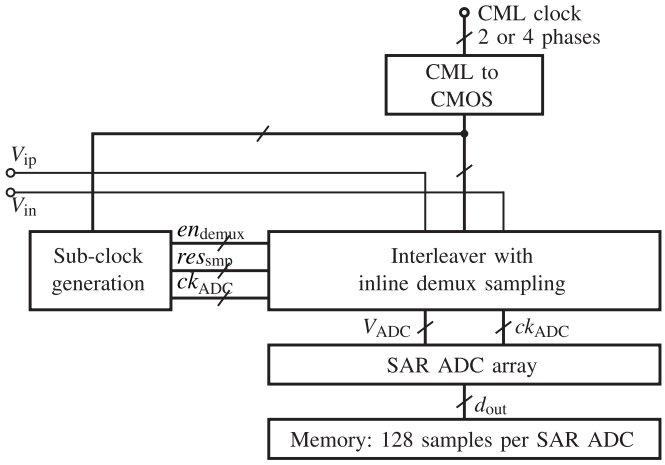

Fig. 10. Architecture of the highly interleaved SAR ADCs.

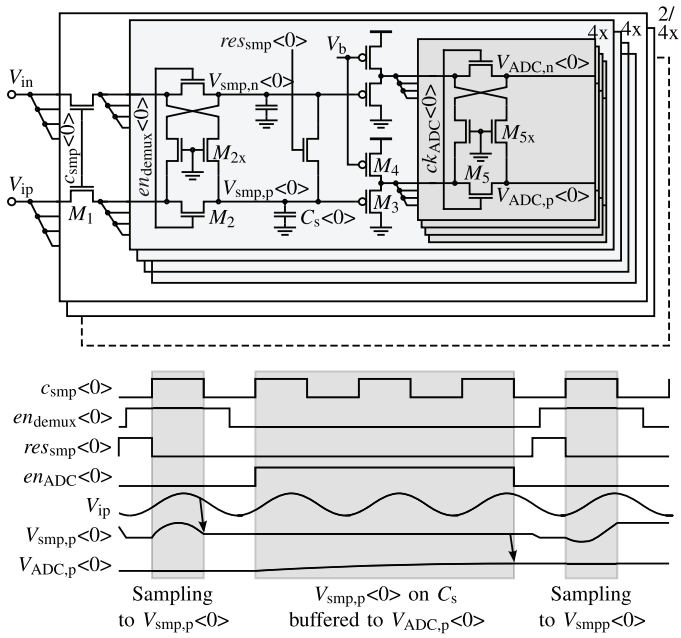

Fig. 11. Schematic details of the differentially implemented 1:64 interleaver with four sampling slices and the 1:32 interleaver with two sampling slices.

CML latches, as found in [20]. These CML signals are converted to CMOS with an inverter-based structure, similar to [20]. The $64\times$ interleaved ADC has 64 sub-ADCs and the $32\times$ interleaved ADC 32 sub-ADCs. A separate subclock generation block receives the sampling clock phases and generates all nontiming critical subclocks for the interleaver and sub-ADCs.

B. Interleaver With Inline Demux Sampling

The interleaver for the $64\times$ interleaved ADC should have an analog bandwidth of at least 1/4 of the nominal sampling frequency f_s for ITU-OTU4 at 56–65 GHz because oversampling by the ADC by a factor of 2 prevents aliasing issues. The hold time to buffer, subsample, and reset the sampled voltages was estimated to be at least 120 ps, equivalent to approx. 11 t_s. The 32 nm CMOS SOI technology is capable of CMOS clock signals of at least 16 GHz. To minimize jitter, 50% duty cycle clocks are chosen. As can be seen from Fig. 8, the inline demux sampling interleaver with $N_1/N_{1,c} \times N_2 = 4/2 \times 4$ provides the highest analog input bandwidth under these constraints and has therefore been implemented. The $2/1 \times 8$ configuration provides slightly more bandwidth and slightly more hold time with a 50% duty cycle clock but requires a CMOS clock frequency of 32 GHz, which is considered to be difficult to achieve in terms of electromigration at high operating temperature. The $4/2 \times 2$ configuration also provides more bandwidth with a 50% duty cycle clock but does not provide enough hold time. The $16/2$ configuration with direct sampling provides the highest bandwidth for a pulse width of $\geq 4t_s$, but its duty cycle is only 1/8; thus, it was not considered. Also the high number of 16 active clock phases, which have to be accurately controlled, complicates the implementation of the $16/2$ configuration.

For the $32\times$ interleaver, the same hold time of 120 ps of the $64\times$ interleaved ADC requires only approx. 5 t_s, which leads to the conclusion that a $2/1 \times 4$ interleaver provides the highest analog input bandwidth, which is beyond the Nyquist frequency, but enables higher SNDR at Nyquist. A $4/2 \times 4$ interleaver provides more time for the buffer to sample the signal onto the sub-ADCs. This results in less time available for SAR conversion and an overall slower sampling rate. The power saved in the buffer because of the lower bandwidth requirement would mostly be compensated by the larger number of buffers. The interleaver schematics for both ADCs are shown in Fig. 11.

In both the $32\times$ and the $64\times$ interleaver, each sampling switch, M_1 is connected in series with a one-by-four demux stage, formed by transistors M_2, and terminated by the sampling capacitors C_s [4]. The cross-coupled transistors M_{2x} prevent signal feed-through, which is important because the node between M_1 and M_2 is not constant during the hold time of C_s. Single NMOS sampling switches are fast and provide sufficient linearity for an 8 b ADC [5]. Size, common mode, and input signal swing of the sampling transistors are optimized for high bandwidth and high linearity across corners, with operating temperatures up to 100 °C, where leakage through M_2 is of concern. One of the four demux switches is enabled by en_{demux} before the rising edge of c_{smp} and disabled after the falling edge of c_{smp} to eliminate the influences of en_{demux} on the sampling window. The sampling capacitor C_s is reset shortly before the sampling window by res_{smp}. The signal en_{demux} is enabled before res_{smp} is disabled to eliminate ISI by canceling any remaining charges on transistor M_1 and the parasitic capacitance between M_1 and M_2 from the preceding sampling phase. A source follower (M_3 and M_4) was chosen to buffer the sampled voltage because of its superior speed, noise figure, and linearity. For high linearity, the source follower is operated with an output common mode close to half the supply voltage. Its output common mode also defines the common mode of the sub-ADC and therefore the comparator. Control of the comparator common mode enables a good trade-off between conversion speed and comparator input-referred noise [9]. The buffered voltage is connected through a second demux stage (M_5) controlled by en_{ADC} to the capacitive DAC

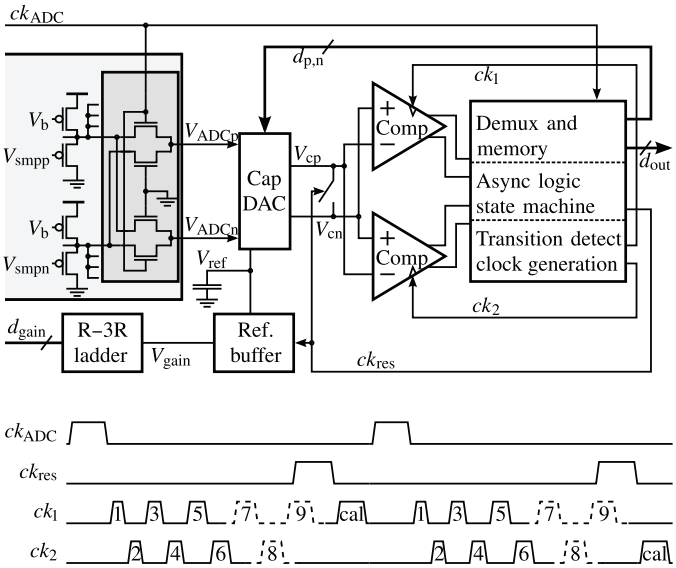

Fig. 12. SAR ADC architecture with last demux stage of the interleaver and corresponding timing diagram.

TABLE I
SAR ADC FEATURE COMPARISON

Feature	↑ speed	↑ precision	↓ power	↓ area	↓ complexity
Asynchronous timing	+	o	+	o	o/+
Alternate comparators	+	o	o/+	o	o
Set-and-up/down DAC	+	+	+	o	+
Redundant DAC (only 8 b)	+	o	o	o	o
Fractional reference voltages	o	o	o	+	o
Clocked reference buffer	o	o	+	o	o
Dynamic logic	+	o	o	o	o/+
Memory with state detection	+	o	+	+	+

of a SAR ADC. Signal en_{ADC} is also used to trigger the conversion of the asynchronous SAR ADC. The second demux stage implements feed-through compensation with transistors M_{5x}, because the buffered node between the source follower and the second demux stage and the SAR DAC voltages are not constant during the SAR conversion [12].

C. Sub-ADC

The asynchronous SAR ADC is implemented with 8 b resolution for the $64\times$ interleaved ADC [9] and with 6 b resolution for the $32\times$ interleaved ADC. The architecture of the SAR ADCs is shown in Fig. 12. It features a number of techniques that increase the speed per area or the speed per power ratios [12], highlighted in Table I.

Asynchronous internal timing [21] in combination with the alternate comparators [22] is the key architectural choices to boost the speed of the SAR ADC beyond 1 GS/s. Asynchronous timing eliminates any waiting time after a successful decision by implementing a decision-detect block that clocks the internal

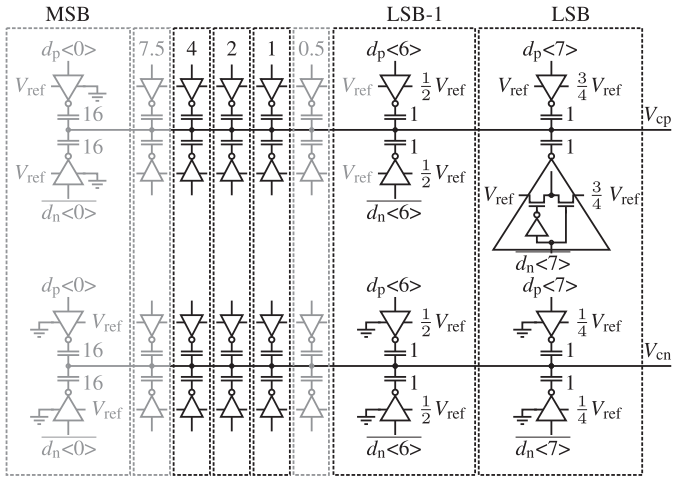

Fig. 13. Capacitive DAC with set-and-up/down for a constant common mode and fractional reference voltages to decrease the area of the DAC. The differences between the 8 b DAC and 6 b DAC are shown in gray.

logic. An important additional benefit is the relaxed metastability requirement: With a nonredundant DAC, metastability can only occur once and the additional time to resolve metastability by gain in the comparator has to be added only once at the end of the conversion. As can be seen from Fig. 12, this time is used to run the comparator offset calibration [22]. The time which is required for the offset calibration is larger than the time that is needed to cover metastability down to a failure rate of 10^{-12}. In rare cases of metastability, an offset calibration cycle can be skipped at no precision penalty.

With alternate comparators, comparator 1 takes the first decision; see Fig. 12. Then comparator 2 takes the second decision, while comparator 1 resides in reset. This eliminates the reset of the comparator from the critical path and thus results in about 30% more speed. Furthermore, it reduces the demux size at the output of each comparator by about a factor of 2, relaxes the timing of the asynchronous state logic, and reduces electromigration issues due to the lower switching activity of a single comparator.

Set-and-up/down switching of the capacitive DAC as shown in Fig. 13 eliminates any DAC switching after sampling prior to the first decision [22]. It also keeps the common mode of the comparator input constant, which is important if there is no buffer in front of the comparator to control noise, offset, and speed of the comparator.

The 8 b sub-ADC implements DAC redundancy with one additional cycle to reduce the DAC settling time by almost a factor of 2 for the MSBs [22]. As the benefit of redundancy decreases toward the LSBs, redundancy is not implemented for the 6 b sub-ADC of the $32\times$ interleaved ADC. The total time for redundancy with one additional cycle for the 6 b sub-ADC and without redundancy are about the same, but without redundancy power can be saved [4].

The reference buffer for V_{ref} is based on a clocked buffer with a large capacitor, which compares the internal reference capacitor voltage against a programmable voltage from an R–3R ladder [4], [22]. It is very low power and does not need extra area as its large capacitor is stacked with the capacitive DAC.

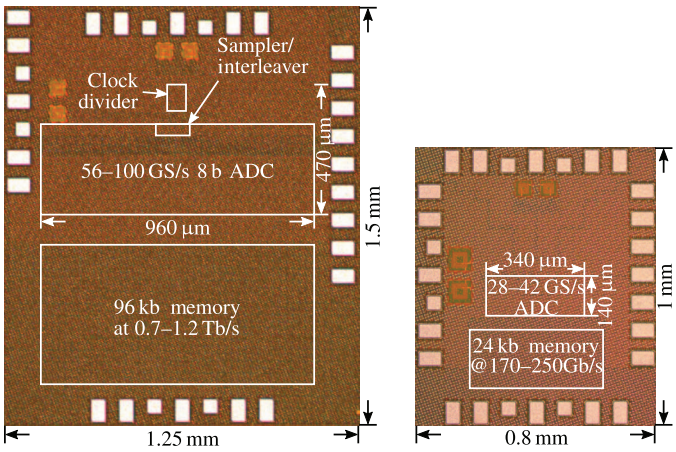

Fig. 14. Chip micrograph of the 90 and 36 GS/s ADC. The 64× interleaved ADC requires a CML clock divider to get four phases for the interleaver.

Dynamic logic and memory stage detection help increase the speed and reduce power further [22].

V. Measurement Results

Both ADCs are manufactured in 32 nm CMOS SOI, the 64× interleaved ADC on an area of $470 \times 960\ \mu m^2$, and the 32× interleaved ADC on $140 \times 340\ \mu m^2$, as shown in Fig. 14. The 64× interleaved ADC requires a CML clock divider to get four phases for the interleaver. As can be seen, the 32× interleaved ADC is much less than half the size of the 64× interleaved ADC because the routing between interleaver and sub-ADCs is much denser and less optimized for low signal distortion and parasitic capacitance, as the latter are not needed for 6 b resolution. At 90 GS/s on the 64× interleaved ADC, the supply on the interleaver and clock logic (V_{DI}) and the sub-ADCs (V_{DA}) is set to 1.2 V. A high supply voltage on the interleaver compensates the shorter tracking time by a higher overdrive for higher sampling frequencies. A supply of 1.2 V on the sub-ADCs is required as they limit the conversion speed at 90 GS/s. For lower conversion rates, lowering the supply of the sub-ADCs is a very effective way to save power. In addition to a full redesign of the ADC with many power-saving features, a lower supply on the sub-ADCs is key to reach a very power-efficient design on the 32× interleaved ADC. The 64× interleaved ADC running at 90 GS/s consumes 667 mW: 8% of this is consumed by the input clock path, 17% by the interleaver, and 75% by the sub-ADCs. The 32× interleaved ADC consumes 110 mW at 36 GS/s, with 30% consumed by the interleaver and 70% by the sub-ADCs. The higher percentage on the interleaver, which is still lower per GS/s than for the 64× interleaved ADC, shows the effectiveness of the power-saving features of the sub-ADC in the 32× interleaved ADC. Fig. 15 illustrates the SNDR and the amplitude versus input frequency for both ADCs. The amplitude versus input frequency follows the RC model derived in Section III, as shown in Fig. 7. The difference is explained by the input T-coil.

The SNDR versus sampling frequency is shown in Fig. 16. The SNDR degrades gradually with higher sampling frequencies, when the offset calibration of some ADCs is no longer completed. Power efficiency degrades significantly for both

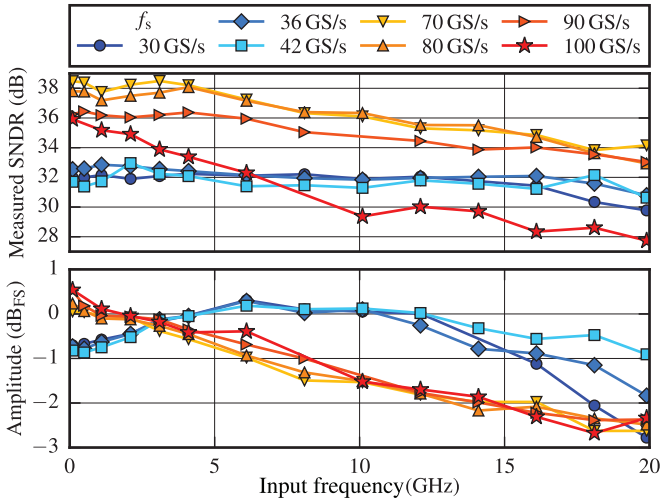

Fig. 15. SNDR and amplitude versus input frequency for the 32× interleaved ADC (30–42 GS/s) and the 64× interleaved ADC (70–100 GS/s). Corresponding supply voltages are shown in Fig. 16. The measurement at 100 GS/s is taken without skew calibration.

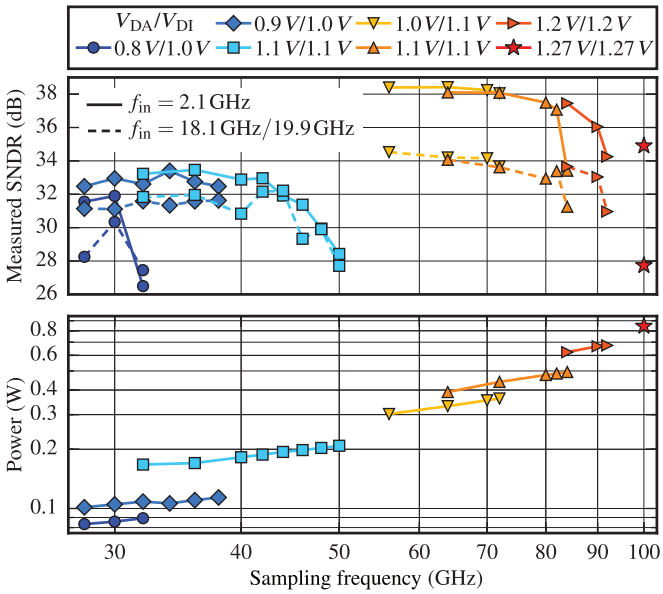

Fig. 16. SNDR and power versus sampling frequency for the 32× interleaved ADC (28–50 GS/s) and the 64× interleaved ADC (56–100 GS/s). V_{DA} and V_{DI} are the supply voltages of the sub-ADCs and the interleaver, respectively.

ADCs at higher supply voltages, but both designs are functional across a large voltage range. The interleaver supply voltage V_{DI} determines the overdrive of the sampling switches. A low overdrive results in more attenuation at frequencies close to Nyquist (see Fig. 15). The SAR supply voltage V_{DA} determines the average conversion time used by the SAR ADC and thus the maximum achievable sampling frequency without SNDR degradation due to early termination of the SAR ADCs. The SAR supply voltage is the main parameter for the overall power consumption of the ADCs. 100 GS/s sampling frequency can be achieved with the 64× interleaved ADC at 1.27 V supply. A FoM of 203 fJ/conv.-step and 121 fJ/conv.-step is achieved at 90 and 70 GS/s, respectively. Low FoM is more difficult to achieve at lower SNDR, but thanks to design optimizations, the 32× interleaved ADC achieves 98 fJ/conv.-step at 36 GS/s.

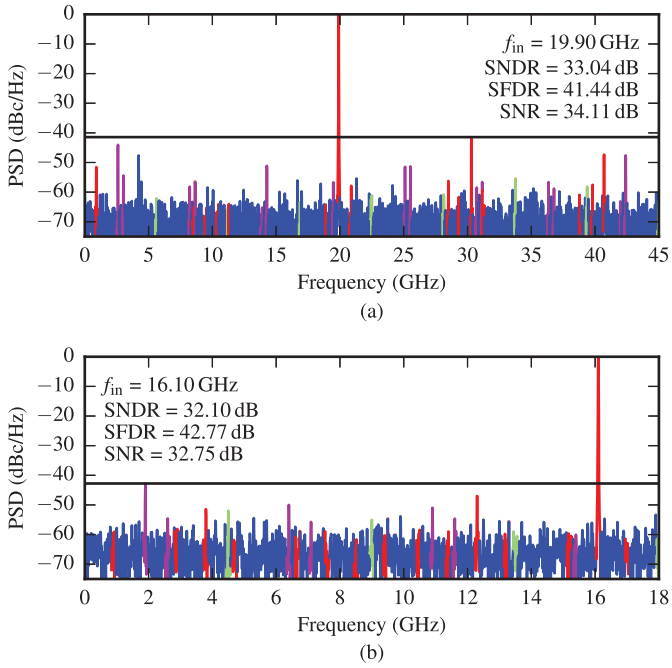

Fig. 17. Power spectral density of the high-speed interleaved ADCs. The SFDR is not limiting the SNDR. Harmonic spurs: red. Spurs from offset: green. Spurs from amplitude mismatch, skew, and bandwidth mismatch: purple. The main source for interleaving spurs is the inline demux sampling. (a) Spectrum of the 64× interleaved ADC with spurs from the 1:16 inline sampling stage. (b) Spectrum of the 32× interleaved ADC with spurs from the 1:8 inline sampling stage.

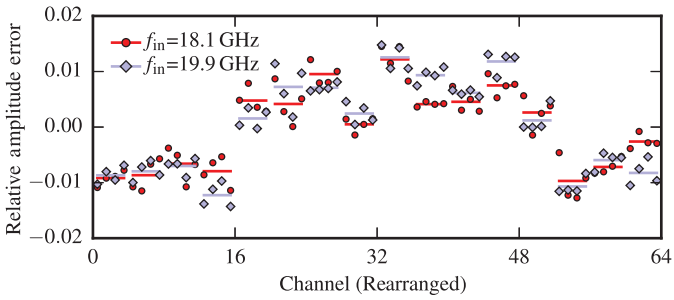

Fig. 18. Bandwidth mismatch per channel for the 64× interleaved ADC. Channels are grouped by sampling switch and sampling capacitor. The measurement series are labeled as in Fig. 16, where the supply voltages can be found. Gain is calibrated at 2.1 GHz.

The spectra of both ADCs in Fig. 17 are very similar. Both designs show spurs from the third-order harmonic and from skew, which are limiting the SFDR at approx. 41–43 dB. The main source for interleaving mismatch spurs is the inline demux sampling. For all measurements, the ADC is calibrated once at startup for each supply voltage and sampling frequency. Gain is adjusted on chip based on a single tone at 2.1 GHz, and skew is calibrated at 19.9 GHz input frequency for higher sensitivity. Interchannel offset is subtracted off chip based on the single-tone measurement at 2.1 GHz, whereas the offset between the comparators inside the sub-ADC is background calibrated on chip.

Fig. 18 provides details on the relative amplitude error and indicates that the on-resistance and capacitance of the sampling

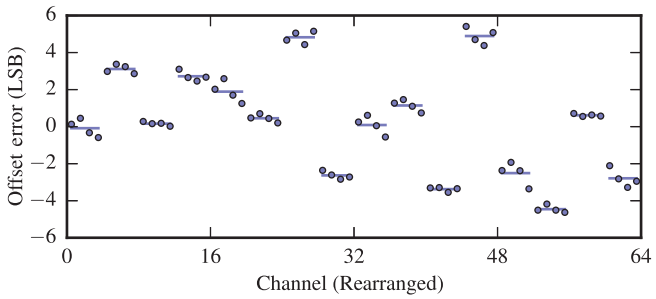

Fig. 19. Offset mismatch per channel for the 64× interleaved ADC, grouped as in Fig. 18. Channels are grouped by sampling switch and sampling capacitor. The offset is estimated at 2.1 GHz input frequency.

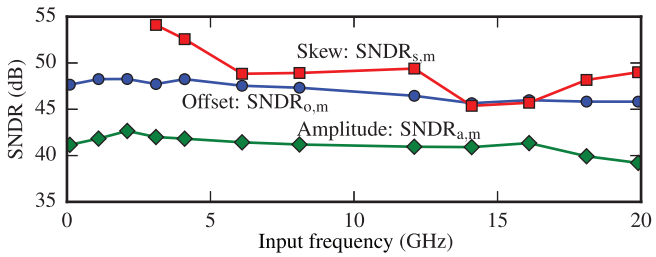

Fig. 20. Limitation from channel mismatch of the 64× interleaved ADC based on sine-fitted data. Bandwidth mismatch is a combination of amplitude mismatch and skew. The best performance is expected for offset and gain calibration at low input frequency and skew calibration at high input frequency.

switches cause most of the spread, shown by four distinctive groups. The estimated standard deviation of the bandwidth based on Fig. 18 for the different sampling channels is 1.5%–1.7% [12].

The offset mismatch in Fig. 19 is mainly caused by the mismatch of the charge kickback of the inline demux switches, the source followers, and the mismatch of the sampling capacitors and wiring.

The total amplitude SNDR (SNDR$_{a,m}$) measured consists of gain/amplitude mismatch, which remains after calibration SNDR$_a$ and bandwidth mismatch SNDR$_{bw}$ and is given by

$$\frac{1}{\mathrm{SNDR}_{a,m}(f_{in})} = \frac{1}{\mathrm{SNDR}_{a}} + \frac{1}{\mathrm{SNDR}_{bw,amp}(f_{in})}. \qquad (17)$$

The remaining amplitude mismatch after calibration is estimated at low input frequencies. Additional amplitude errors at higher input frequencies are caused by bandwidth mismatch. The channel mismatch limitation on the SNDR of the 64× interleaved ADC is estimated by sine-fitting each channel, which gives the amplitude, offset, and phase of each of the 64 channels. The best performance is expected at a calibration frequency of 2.1 GHz for offset and amplitude, which is reflected in Fig. 20. The impact of skew is highest for higher input frequencies but also shows a minimum at the calibration frequency of 19.9 GHz. The main limitation in ADC interleaving is the remaining amplitude mismatch, but it is not yet critical because the SNDR$_{a,m}$ still is about 6 dB above the total SNDR of the ADC.

Jitter is a major concern in ADCs, as a standard deviation of 100 fs at the sampling clock edge already limits the ENOB to 6 at 20 GHz input frequency [11]. Simulation of the clock path

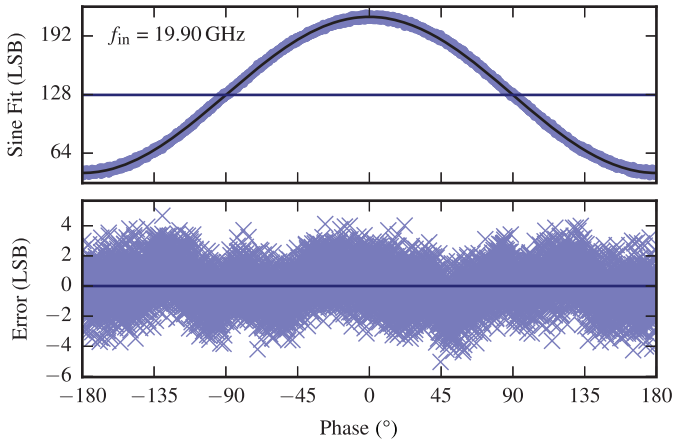

Fig. 21. Modulo-time plot of the 64× interleaved ADC with jitter estimated at 60 fs including measurement equipment.

TABLE II
PERFORMANCE COMPARISON

					This work	
Specification	[2]	[3]	[1]	[7]	[5]	[4]
Architecture (all TI)	Flash	SAR	SAR	Flash	SAR	SAR
Tech. CMOS (nm)	65	40	28	32	32	32
Resolution (b)	8	6	6	6	6	8
f_s (GS/s)	40	65	10	20	36	90
V_{DI} interleaver (V)	1.2	±1.8	1.0	0.9	1.0	1.2
V_{DA} sub-ADCs (V)		1.0	±0.9	0.9	0.9	1.2
$V_{in,pp\text{-}diff}$ (V)	1.2	0.7			0.6	0.8
SNDR@$f_{in,low}$ (dB)	34.9	36.1	33.8	35.0	32.6	36.0
SNDR@$f_{in,high}$ (dB)	25.2		33.8	30.7	31.6	33.0
$f_{in,high}$ (GHz)	18		4.8	10.0	18.1	19.9
Power (mW)	1500	1200	32	69.5	110	667
FoM@$f_{in,low}$ (fJ/c-s)	829	355	80	76	88	144
FoM@$f_{in,high}$ (fJ/c-s)	2512		80	124	98	203
Area (mm^2)	16	3	0.009	0.25	0.048	0.45

TABLE III
PERFORMANCE SUMMARY OF THE 32× AND 64× TIME-INTERLEAVED SAR ADC

Technology (nm)	32 nm CMOS SOI						
Resolution (b)	6			8			
f_s (GS/s)	30	36	42	70	80	90	100
V_{DI} interleaver (V)	1.0	1.0	1.1	1.1	1.1	1.2	1.27
V_{DA} sub-ADC (V)	0.8	0.9	1.1	1.0	1.1	1.2	1.27
Input range ($V_{pp\text{-}diff}$)	0.55	0.6	0.65	0.7	0.7	0.8	0.85
SNDR up to $f_{in,low}$ (dB)	32.0	32.6	31.4	37.7	37.2	36.0	34.9
SNDR up to $f_{in,high}$ (dB)	30.5	31.6	30.6	34.2	32.9	33.0	27.7
$f_{in,high}$ (GHz)	14.1	18.1	19.9	19.9	19.9	19.9	19.9
3 dB bandwidth (GHz)	20	>20	>20	>20	22	>20	>20
Power (mW)	86	110	187	355	477	667	845
FOM at $f_{in,low}$ (fJ/c.-s.)	88	88	147	81	101	144	186
FOM at $f_{in,high}$ (fJ/c.-s.)	105	98	161	121	165	203	426
Area (mm^2)	0.048			0.45			

predicted 30–50 fs jitter. Two different methods were used to analyze jitter. A modulo-time plot, see Fig. 21, visualizes the impact of jitter. The upper panel of the plot shows the measured data versus phase and the sine-fit for the data. The lower panel shows the measured data after subtracting the sine-fitted wave. The remaining error reflects INL, thermal noise, and jitter. INL modulates the mean of the data errors at a certain phase. At 0° and 180° phases, there is no jitter as the derivative of the input signal is zero. At ±90°, the impact of jitter on the total error is maximum but not visible in the modulo time plot. Analyzing the modulo time plot errors in segments of 1° width results in the best accuracy to eliminate the impact of INL on the jitter estimation. Plotting the standard deviation of each of these segments versus the input-signal phase results in a double cosine wave, which can be used to estimate jitter. The second method to estimate jitter compares the SNR (excluding distortion) for the individual channels at low and high input frequencies. Both methods result in 60 fs jitter, including measurement equipment jitter. Clock and data input are generated from a high-quality external signal generator connected to the differential clock and data inputs of the chip. Jitter from the clock path showed 30–50 fs jitter in simulation.

Table II compares the ADCs presented in this paper with previously published work. The 64× interleaved ADC achieves the highest CMOS ADC sampling speed to date. Its FoM is more than 50% lower and the technology adjusted area 4× smaller than those of previously reported 6 b+, > 20 GS/s ADCs [23]. The 32× interleaved ADC is optimized for best power and area efficiency. Its FoM is similar to designs at 10–20 GS/s but achieves twice their sampling speeds. The area is 9× smaller than those of previously reported 4 b+, > 20 GS/s ADCs [23]. The 6 b sub-ADC of the 32× interleaved ADC occupies 0.0008 mm^2, including the R–3R ladder, and is on par with the smallest 6 b+ ADCs published [1], [23].

Table III summarizes the performance of the 32× and the 64× interleaved ADC at different supply voltages and sampling frequencies.

VI. CONCLUSION

This paper introduces a model for high-speed interleavers and describes the implementation of two high-speed ADCs at 6 b and 8 b resolution with interleavers based on this model. The interleaver model can be used to evaluate different voltage-based interleavers in terms of their analog input bandwidth and sample hold time. It also reveals implications regarding the clock generation circuit requirement, which is key to a successful design of high-performance ADCs. The two ADCs achieved 90 GS/s at 667 mW and 36 GS/s at 110 mW in a 32 nm CMOS SOI process, both with at least 20 GHz analog input bandwidth.

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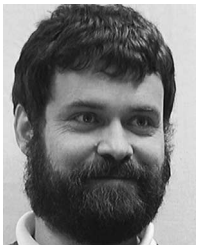

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