

RESISTOR MODEL

CROLLES2 ALLIANCE
CMOS65nm TECHNOLOGY

DEVICE MODELLING TEAM (SALIM EL GHOULI)

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OVERVIEW

The RESISTOR device model is a physical model. The resistance value is calculated using the expression:

$$R = \frac{\rho \times L}{W \times t} = \left(\frac{\rho}{t}\right) \times \left(\frac{L}{W}\right) = R_S \times \frac{L}{W}$$
 (1)

where:

R : Resistance (Ω)

 ρ : resistivity of the material (Ω -m)

L¹: length of the strip (m)

W: width of the strip (m)

t: thickness of the strip (m)

Rs: sheet resistance (Ω /square)

□ Pins

Resistor is a symmetrical and 3 pins device:

- Plus pin
- Minus pin
- One pin for substrate: Sub

Resistors can be built in the following flavors:

- either Poly or OD (active), according to the layer in which they are fabricated
- 1. The drawn length is defined as the distance between the contacts for silisided resistors and the length of the resulting shape of intersection of the RPO layer and the PO/OD for unsilisided resistors (see DRM RevC 7.3.9.1)

- either N+ or P+, as to the doping type
- either unsilicided or silicided, relying on the presence or not of the silicidation protection

☐ Model nomenclature

Table below contains all available models and their names.

P+ Unsilicided Active RESISTOR	RPODRPO and RPODRPO_ACC
N+ Silicided Poly RESISTOR	RNPO and RNPO_ACC
N+ Unsilicided Poly RESISTOR	RNPORPO and RNPORPO_ACC
P+ Unsilicided Poly RESISTOR	RPPORPO and RPPORPO_ACC
High Resistive Poly RESISTOR	RHIPORPO and RHIPORPO_ACC

DEVICE INSTANTIATION PARAMETERS

☐ Model CALL:

Xname Plus_Pin Minus_Pin Substrate_Pin ModelName w=resistor_width l=resistor_length r=resistance_value¹ mult=MULT_value mismatch=mismatch_flag lpe=LPE_Value tometer=microns_to_meter nhead=head_number

Plus_Pin	is the first resistor terminal		
Minus_Pin	is the second resistor terminal		
Substrate_Pin	e_Pin the node connected to the substrate		
ModelName	rnpo_acc, rpporpo_acc, rpodrpo_acc, rhiporpo_acc or rnporpo_acc (string)		
w	is the desired width of the resistor (float)		
1	is the desired length of the resistor (float)		
r	is the resistance value (not used in the model)		
mult	is the multiplication factor (parallel resistors configuration)		
mismatch	to activate the mismatch effect for the device (0=disable, 1=enable)		
lpe	flag is a user option to take into account the post-layout extraction mode (0,1, 2 or 3)		
tometer	parameter used to transform distances in microns to meters unit		
nhead	number of heads available in the instantiated device		

^{1.} The value specified here is not used in the model.

PCELL & LAYOUT

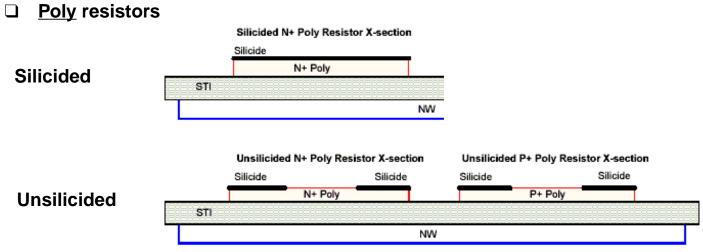


Figure 1 - Side view of poly resistors Pcell

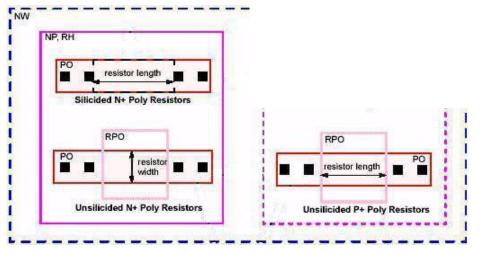


Figure 2 - Top view of poly resistors Pcell (Layout)

2005 May 17th DM_AL_05_039 Resistor Model

Unsilicided P+ Active Resistor

Unsilicided P+ OD Resistor X-section

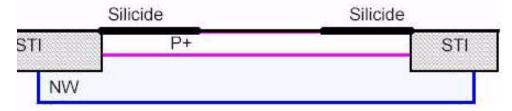


Figure 3 - Side view of unsilicided P+ active resistors Pcell

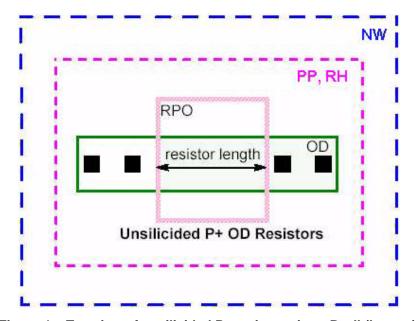


Figure 4 - Top view of unsilicided P+ active resistor Pcell (Layout)

EQUIVALENT CIRCUIT SCHEMATICS

□ Poly equivalent circuit schematics

Resistor model calculates Rbody and Rhead resistances (Figure 5):

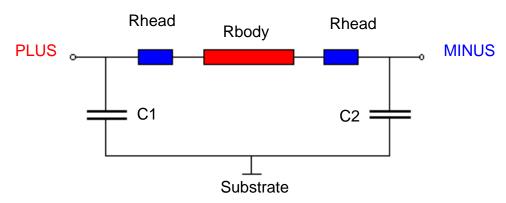


Figure 5 - Circuit diagram of poly resistor device

Where:

- Rbody: the intrinsic (main) resistance between the Plus/Minus terminals without head parts.
- Rhead: resistance of one head. Its value depends on contact and silicidation.
- C1: the parasitic capacitor between the PLUS terminal and the substrate.
- C2: the parasitic capacitor between the MINUS terminal and the substrate.

NOTE: for unsilicided poly resistors a detailed circuit schematics¹ is shown in paragraph bellow (figure 7)

^{1.} replace P+/NWell diodes by parasitics capacitors.

Active equivalent circuit schematics

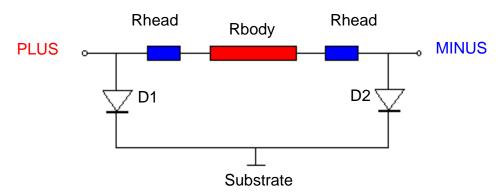


Figure 6 - Circuit diagram of active resistor device

Where:

- Rbody: the intrinsic (main) resistance between the Plus/Minus terminals without head parts.
- Rhead: resistance of one head. Its value depends on contact and silicidation.
- D1: the parasitic diode (P+/NWell) between the PLUS terminal and the substrate.
- D2: the parasitic diode (P+/NWell) between the MINUS terminal and the substrate.

NOTE: detailed unsilisided resistor equivalent circuit schematics is shown in figure below:

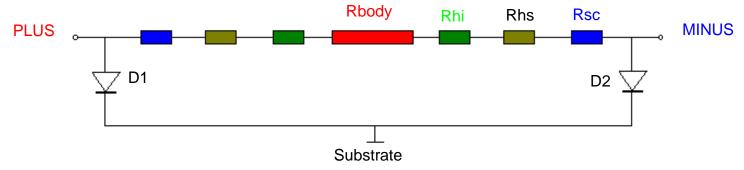


Figure 7 - Circuit diagram of unsilicided active resistor device

Where:

- Rbody: the intrinsic (main) resistance between the Plus/Minus terminals without head parts.
- Rhi: resistance of interface between head and body
- Rhs: resistance of silisided head part
- Rsc: contact resistance

This configuration can be seen also in poly unsilicided resistors.

NOTE: for high resistive poly resistor another resistive contribution is due to the P+ unsilicided head part. This effect is due to the resulting shape of intersection of the RPO layer and OD for unsilicided resistors.

Modeled effects

GEOMETRY SCALING

Silicided resistor model

The resistance value is calculated using the expression:

$$R = \text{Rho} \times \frac{L}{W - \Delta W} + 2 \times \frac{\text{Rsc}}{2 \times N_C} = \text{Rbody} + 2 \times \text{Rhead}$$
 (2)

where:

Rho: body sheet resistance (Ω /square)

 ΔW : width offset (μm) = Drawn width - Effective width

L: body length (μm)

W: body width (µm)

Rsc : contact resistance (Ω)

Nc: number of contacts in a row for one head (resistors have to be designed with two rows of contacts)

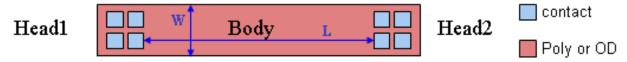


Figure 8 - Layout of one two head salicided resistor

Hypothesis: distance between contacts is constant (no offset)

Unsilicided resistor model

The resistance value is calculated using the expression:

$$R = \text{Rho} \times \frac{L - \Delta L}{W - \Delta W} + 2 \times \frac{\text{Rsc}}{2 \times N_C} + 2 \times \frac{\text{Rhs} \times \left(\text{Lhs} + \frac{\Delta L}{2}\right) + \text{Rhi}}{W - \Delta W} = \text{Rbody} + 2 \times \text{Rhead}$$
 (3)

where:

Rho : body sheet resistance (Ω /square)

 Δ L: length offset (μ m) = Drawn length - Effective length

 ΔW : width offset (μm) = Drawn width - Effective width

L: body length (μm)

W: body width (μm)

Rhs: silicided head sheet resistance (Ω /square)

Lhs: silicided head length (µm)

Rsc : contact resistance (Ω)

Rhi : access resistance between head and body ($\Omega \mu m$) (Rhi=0 in the model: its impact is included in the ΔL value)

Nc: number of contacts in a row for one head (resistors have to be designed with two rows of contacts)

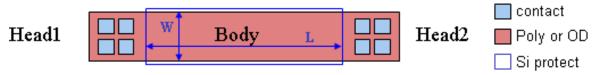


Figure 9 - Layout of one two head unsilicided resistor

HIPO resistor model

The resistance value is calculated using the expression:

$$R = \text{Rho} \times \frac{L - \Delta L_2}{W - \Delta W} + 2 \times \frac{\text{Rsc}}{2 \times N_C} + 2 \times \frac{\text{Rhs} \times \left(\text{Lhs} + \frac{\Delta L_1}{2}\right) + \text{Rhu} \times \left(\text{Lhu} - \frac{\Delta L_1}{2} + \frac{\Delta L_2}{2}\right) + \text{Rhi}}{W - \Delta W} = \text{Rbody} + 2 \times \text{Rhead}$$
(4)

where (see figure bellow):

Rho: body sheet resistance (Ω /square)

 Δ L₁: Si-protect length offset (μ m), extracted on P+ poly resistors

 Δ L2: P+ diffusion length offset (μ m)

 ΔW : width offset (μm) = Drawn width - Effective width

 $L: body \ length \ (\mu m)$

W: body width (µm)

Rhs: silicided head sheet resistance (Ω /square)

Lhs: silicided head length (µm)

Rhu: unsilicided head sheet resistance (Ω /square)

Lhu: unsilicided head length (µm)

Rsc : contact resistance (Ω)

Rhi : access resistance between head and body ($\Omega \mu m$) (Rhi=0 in the model: its impact is included in the ΔL value)

Nc: number of contacts in a row for one head (resistors have to be designed with two rows of contacts)

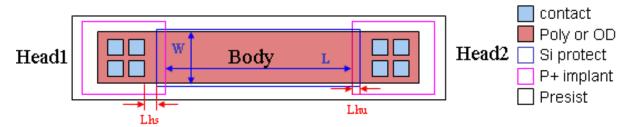


Figure 10 - Layout of one two head hipo resistor

☐ Equivalent sheet resistance

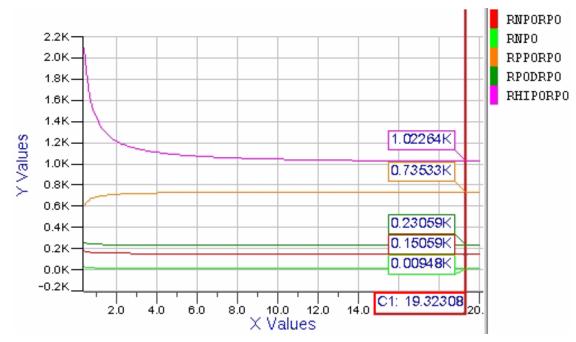


Figure 11 - Sheet resistance versus length (0.4 μ m<L<20 μ m ; W = 1 μ m)

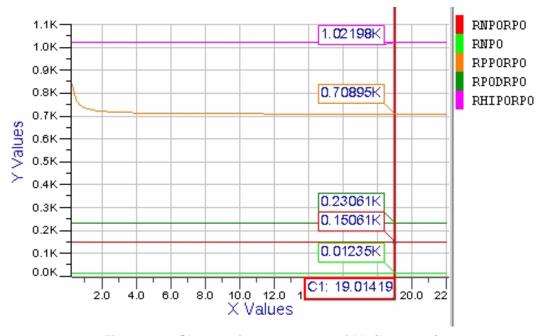


Figure 12 - Sheet resistance versus width (L = $20\mu m$)

NOTE: for great resistor length the sheet resistance is a fixed value.

MISMATCH MODEL

A normal distribution is used to estimate the expected main resistance value:

$$R = R_0 \times (1 + \varepsilon)$$

where

- Ro: is the mean resistance value given by the physical equation (2, 3 or 4)
- ε : is a normal distribution with a standard deviation given by:

$$\sigma = \frac{\sqrt{\sigma_B^2 + N_C^2 \times \sigma_H^2}}{R_0}$$

where

$$\sigma_B = Rbody \times \frac{r_A}{\sqrt{2 \times W \times L}}$$
 and $\sigma_H = Rhead \times \frac{r_K}{\sqrt{2 \times W}}$

where

r_A: is the mismatch coefficient for body resistor given by measurement values.

r_K: is the mismatch coefficient for head resistor given by measurement values.

When r_A and r_K parameters are not specified no distribution is used and resistance value is equal to R₀.

The normal distribution is provided using the Eldo function: gauss

$$\varepsilon = 0$$
 $dev/gauss = '\sigma \times mismatch \times fudge'$

where

mismatch is a flag used to enable or disable mismatch effect. Fudge parameter is used to be sure that the resistance range covers measurements.

Bellow is a result of a mismatch effect simulation:

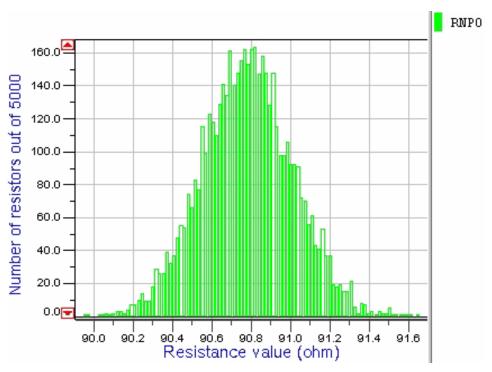


Figure 13 - Number of resistors out of 5000 versus resistance value for an RNPO resistor (W = $10\mu m$; L = $100\mu m$)

Example above is done for one RNPO resistor (W = $10\mu m$; L = $100\mu m$) simulation gives roughly: 90.8Ω as resistance value.

Standard deviation specified: 0.23166

Standard deviation simulated (5000 random selection using a Monte Carlo Analysis): 0.23172

TEMPERATURE DEPENDENCE

The model used to determinate the resistance variation versus temperature is: $R = R_{T0} \times (1 + \text{tc1} \cdot (T - \text{Tref}) + \text{tc2} \cdot (T - \text{Tref})^2)$

where:

RT0: is resistance (Ω) at temperature Tref=300K

Tc1 and Tc2 are first and second order temperature parameters

T: is the current resistor temperature

NOTE: Tc1 and Tc2 are given for one typical dimension

Figure bellow shows the variation of sheet resistance versus temperature:

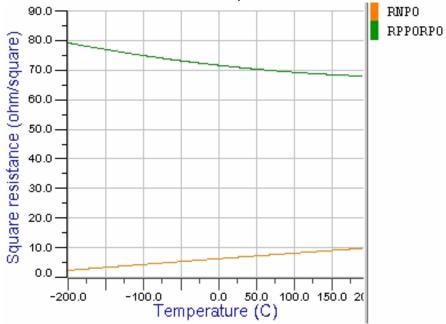


Figure 14 - Sheet resistance versus temperature for RNPO and RPPORPO resistors

Noise Model

The model used to determinate the resistance noise versus frequency is:

$$S_i(f) = \frac{4k_BT}{R} + \frac{K_f}{f} \times I^{A_f}$$
 = Thermal_noise + Flicker or low frequency_noise

where: Si: is the noise spectral density of a resistor

R : resistance value f : current frequency

I : current

kB: Boltzmann coefficient

Af and Kf: are flicker noise model coefficients, they are extracted for each supported resistor

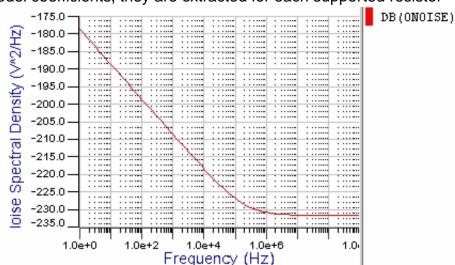


Figure 15 - Noise spectral density versus frequency for RNPORPO ressistor

PARASITIC COMPONENTS

□ P+/NWell diodes (for active resistor):

The parasitic diode P+/NWell must be in reverse-bias mode. The diode model dpsvtlp (P+/NWell) is instantiated using:

- Area = area of one head + 1/2 body area
- Perimeter = perimeter of one head + 1/2 body perimeter

The diode is connected to both PLUS or MINUS and substrate as in figure 6.

□ Parasitic capacitances (for poly resistors):

Capacitance value is calculated using the expression:

$$C = Ch + 0.5 \times Cb$$

where:

Cb =
$$cap \times Areab + cfp \times Perimeterb$$

$$Ch = cap \times Areah + cfp \times Perimeterh$$

cap : specific capacitance (F/m2)

cfp: perimeter capacitance coefficient (F/m)

POST LAYOUT SIMULATION

Each device is composed of two description levels (name, name_acc) coupled with the two pin model definitions. Each one is managed by the LPE flag option, which permits to select the Resistor/Capacitor access modeling mode. See the following table depicting the proposed options:

LPE	Body	Access_R	Access_C	Extraction_mode
0	yes	yes	yes	
1	yes	yes	no	С
2	yes	no	yes	R
3	yes	no	no	RC

The Front-End Models (F-E):

name, a simple model which accounts for resistor components (LPE=0).

name_acc is a more suitable model which accounts flicker noise.

The Back-End models (B-E):

The **name** B-E model is identical to the **name** F-E model concerning the intrinsic resistance functionnality, but it excludes contributions related to head (LPE=1,2 or 3 according to the user choice).

The name_acc B-E model is identical to the name_acc F-E model but it excludes contributions related to head (LPE=1,2 or 3).

CORNERS CONSTRUCTION

<u>Parameter</u>	MIN	TYP	MAX	Source	<u>Definition</u>
rho	min	typ	max	DRM ^a	(ohm/sq) Sheet Res. (DRM)
rsc	min	typ	max	DRM	(ohm) Contact Res. (DRM)
rhi	min	typ	max	ECb	(ohm.m) Silicided/Unsilicided Acc. Res.
rhu	min	typ	max	DRM	(ohm/sq) Unsilicided Head sheet Res.
rhs	min	typ	max	DRM	(ohm/sq) Silicided Head sheet Res. (DRM)
dl	max	typ	min	EC	(m) Length Offset
dw	min	typ	max	EC	(m) Width Offset
tc1	min	typ	max	EC	(1/K) temperature coeff.
tc2	min	typ	max	EC	(1/K^2) temperature coeff.
cap	min	typ	max	EC	area cap (F/m2)
cf0p	min	typ	max	EC	fringe cap (F/m)

a. DRM: Design Rule Manual parameterb. EC: Electrical Characterization parameter

Model Parameter List

diode	parasitic diode model name for active resistors
wdef	(m) Min model Width given by test structures
ldef	(m) Min model Length given by test structures
wcon	(m) min Width contact (DRM ^a rule: CO.W.1)
scon	(m) space between contacts (DRM rule: CO.S.2)
wminabs	(m) min width given by the DRM rule: ROU.W.1
wmin	(m) min width given by test structures
Iminabs	(m) min length given by the DRM rule: RPO.W.1.
lmin	(m) min length given by test structures
wmax	(m) max width given by test structures
lmax	(m) max length given by test structures
cea	(m) Contact enclosure by OD (DRM rule: C0.EN.2)
сер	(m) Contact enclosure by poly (DRM rule: C0.EN.1)
lhs	(m) Length of Silicided head part (DRM rule: RPO.D.2)
lhu	(m) Length of Unsilicided Head part
ncdef	number of contact by default
af	() LFNoise coefficient
kf	(m2) LFNoise coefficient
r_Abody	(m) for body mismatch

r_Khead	(sqrt(m)) for head mismatch
rho ^b	(ohm/sq) Sheet Res. (DRM)
rsc	(ohm) Contact Res. (DRM)
rhi	(ohm.m) Silicided/Unsilicided Acc. Res.
rhu	(ohm/sq) Unsilicided Head sheet Res.
rhs	(ohm/sq) Silicided Head sheet Res. (DRM)
dl	(m) Length Offset
dw	(m) Width Offset
tc1	(1/K) temperature coeff.
tc2	(1/K^2) temperature coeff.
cap	area cap (F/m2)
cf0p	fringe cap (F/m)

a. Design Rule Manual (CMOS65nm RevC)

b. In blue: parameters with provided MIN and MAX corners (see paragraph before)