CFRINGE CAPACITOR MODEL (5 AND 4 PIN DEVICES)

V 0.2

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OVERVIEW

The Cfringe device model is a fit capacitance-value model. The results of Quickcap[1] simulation (or measurements) are used to calculate a and b coefficients for contributions of the main and parasitic capacitors. The capacitance value contribution of one elementary capacitor is calculated using the expression:

$$\text{capacitance} = acoeff \times area + bcoeff \qquad (1)$$ (Extraction: see example in appendix - 1)

❑ Pins

Cfringe capacitor is a 5 or 4 pin device:

❍ 5 pin cfringe capacitor:

- two pins for the main capacitor (**a_po** = Plus, **b_od** = Minus). a_po pin is placed over poly fingers and b_od is placed over the active fingers.
- two pins for the poly and OD shield: **shpo** and **shod**
- one pin for substrate: **Sub**

❍ 4 pin cfringe capacitor:

- two pins for the main capacitor (**a_po** = Plus, **b_od** = Minus). a_po pin is placed over poly fingers and b_od is placed over the active fingers.
- two pins for the poly and OD shield: **shpo** and **shod**

1. QuickCap is a parasitic capacitance extraction tool. It is used in applications that demand high 3D-extraction accuracy, such as process analysis, library cell characterization, parameter extraction and modeling, correlation studies, critical block design, and critical net analysis. QuickCap provides the high accuracy parasitic data required for accurate delay and signal integrity analysis, verification, and post-layout simulation.

NOTE: in the cfringe with 4 pins the pin linked to substrate doesn't exist. The isolation diode is not implemented in the model.

❑ Model nomenclature

Cfringe models are available only from metal1 to metal5 levels : M1-> M5

❍ 5 pin cfringe capacitor:

Cfringe 5 pin capacitor model names : **cfrm1m5shx**, **cfrm1m5shx_acc, cfrm1m5shy, cfrm1m5shy_acc, cfrm1m5shz, cfrm1m5shz_acc**.

The name includes the right configuration of metals used to perform the capacitor: metal 1 to metal 5 for the core and metal x,y or z for level 6 (shielding pattern). It is important that the name contains information on the metal 6 shielding metal type.

❍ 4 pin cfringe capacitor:

Cfringe 4 pin capacitor model names : **cfrm1m5shxnosub**, **cfrm1m5shxnosub_acc, cfrm1m5shynosub, cfrm1m5shynosub_acc, cfrm1m5shznosub, cfrm1m5shznosub_acc**.

The name includes the right configuration of metals used to perform the capacitor: metal 1 to metal 5 for the core and metal x,y or z for level 6 (shielding pattern). It is important that the name contains information on the metal 6 shielding metal type.

DEVICE INSTANTIATION PARAMETERS

❑ Model CALL for the 5 pin fringe capacitor:

Xname **Plus_Pin** **Minus_Pin** **Shiel_od_Pin** **Shield_poly_Pin** **Substrate_Pin** **ModelName** l=**finger_length** nf=**finger_number** lpe=**LPE_Value** mult=**MULT_value** mismatch=**mismatch_flag** c=**capacitance_value**[1]

Plus_Pin	(a_po) is the node whose metal fingers are placed over the poly fingers
Minus_Pin	(b_od) the node whose metal fingers are placed over the OD fingers
Shiel_od_Pin	the node connected to active shield
Shield_poly_Pin	the node connected to poly and+metal6 shield
Substrate_Pin	the node connected to the substrate
ModelName	cfrm1m5shx_acc, cfrm1m5shy_acc or cfrm1m5shz_acc (string)
l	is the desired length of the face to face part of the capacitor fiingers (float)
nf	is the desired number of all plus and minus sides fingers (integer)
lpe	flag: is a user option to take into account the post-layout extraction mode (0,1, 2 or 3)
mult	is the multiplication factor (parallel devices)
mismatch	flag: to activate the mismatch effect for the device (0=disable, 1=enable)
c	capacitance value (not used in the model)

1. The value specified here is not used in the model.

DEVICE INSTANTIATION PARAMETERS

❑ Model CALL for the 4 pin fringe capacitor:

Xname **Plus_Pin** **Minus_Pin** **Shiel_od_Pin** **Shield_poly_Pin** **ModelName** l=**finger_length** nf=**finger_number** lpe=**LPE_Value** mult=**MULT_value** mismatch=**mismatch_flag** c=**capacitance_value**[1]

Plus_Pin	(a_po) is the node whose metal fingers are placed over the poly fingers
Minus_Pin	(b_od) the node whose metal fingers are placed over the OD fingers
Shiel_od_Pin	the node connected to active shield
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c	capacitance value (not used in the model)

1. The value specified here is not used in the model.

PCELL & LAYOUT

Five metal levels are used to build the core of cfringe capacitor. The sixth level (linked up with the poly) is used to make the shielding pattern (protection against interference). The level 6 metal is x, y or z type, that's why the Cfringe family is composed of three different models depending on technology option. The models are named: cfrm1m5shx (metal 6 is x), cfrm1m5shy (metal 6 is y) and cfrm1m5shz (metal 6 is z).

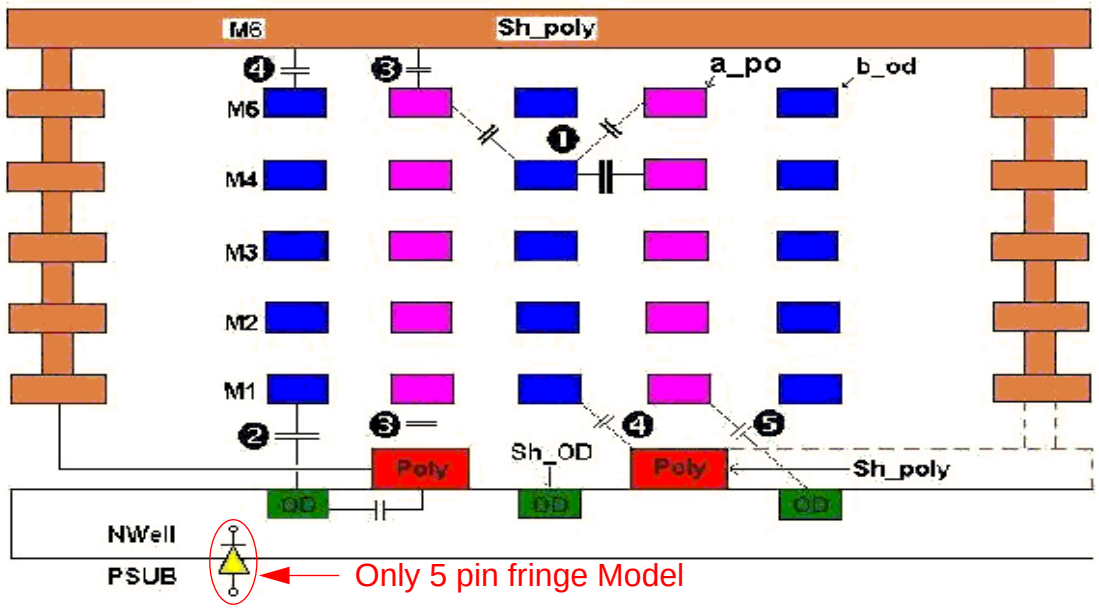

Figure 1 - Side view of cfringe Pcell (A-A': next figure)

The main capacitance (1) is between the two terminals (Plus = a_po and Minus = b_od).

For the 4 pin fringe capacitor the isolation diode and the link to bulk are removed.

NOTE1 (Important): poly/OD shield must be tied to a fixed voltage to fit electrical model.

NOTE2: the shielding patterns can be biased independently one to the other.

NOTE3: the number of fingers for one level must have odd-numbered value (>= 11)

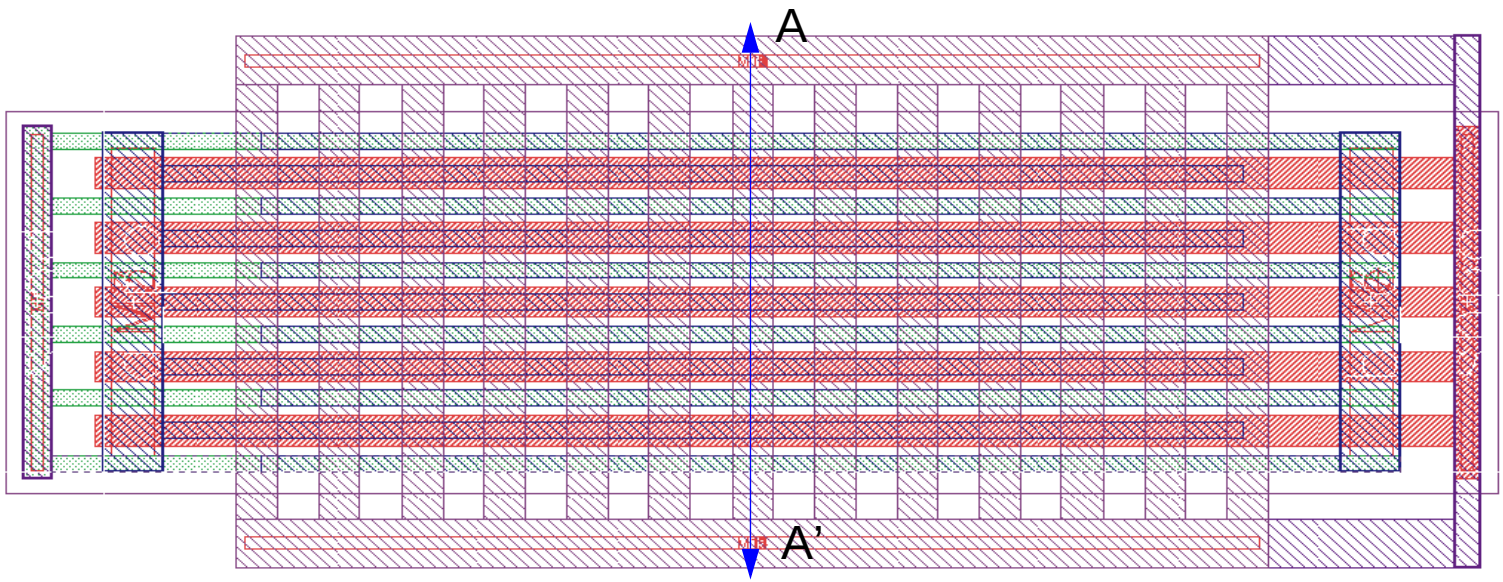

Figure 2 - Top view of the cfringe Pcell (Layout)

EQUIVALENT CIRCUIT SCHEMATICS

Both capacitor models calculate the main and parasitic capacitances which are accounted respectively between the Plus/Minus terminals, Plus/Shield_Poly, Plus/Shield_OD, Minus/Shield_Poly, Minus/Shield_OD and Shield_Poly/Shield_OD (Figure 1 and 3):

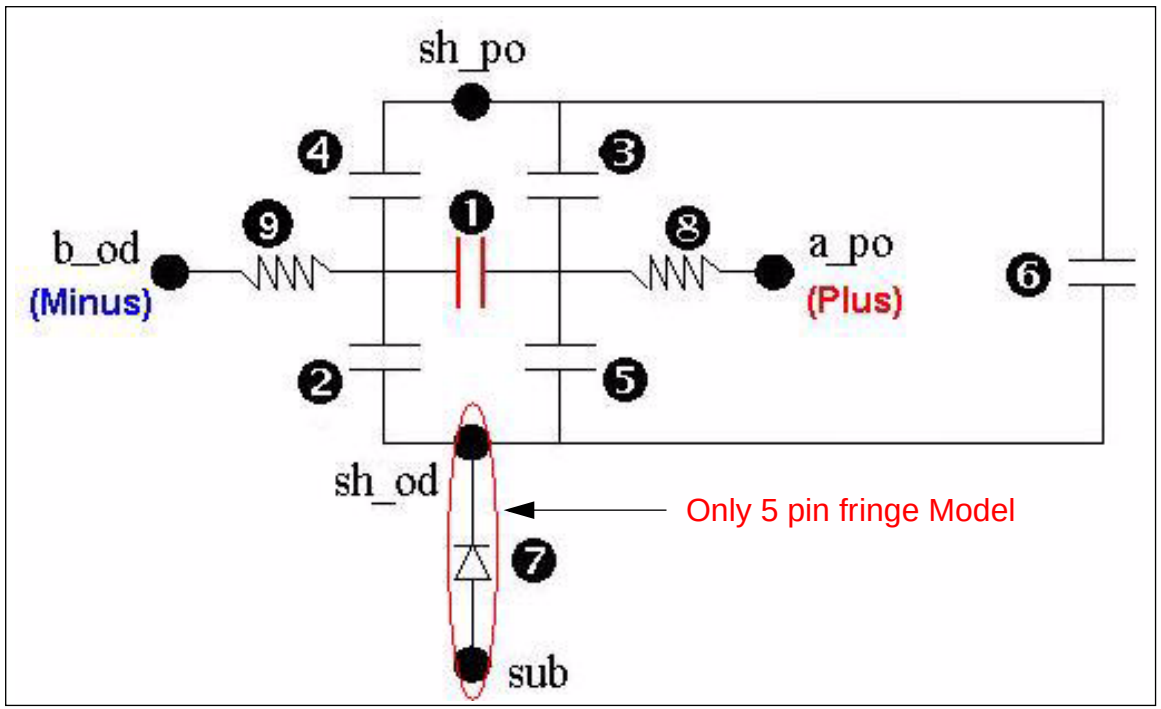

Figure 3 - Circuit diagram of cfringe device

- cc (1): intrinsic (main) capacitor between the Plus/Minus terminals.
- cc_minus_od (2): parasitic capacitor between the minus terminal and the active shield.
- cc_plus_po (3): parasitic capacitor between the plus terminal and the poly shield.
- cc_minus_po (4): parasitic capacitor between the minus terminal and the poly shield.

- cc_plus_od (5): parasitic capacitor between the plus terminal and the active shield (N+).
- cc_od_po (6): parasitic capacitor between the poly and acitve shields.

The isolation diode (7) is an NWell/Psub diode (for 5 pin fringe model). It must be in reverse-bias mode (Vnwell > Vsub).

name_acc models include two series resistances: rvalp (8): for the plus terminal. It takes into account the vias (VIA1X, VIA2X, VIA3X, VIA4X and VIA5X) and the 5 metal levels resistance belonging to the plus side.

rvalm (9): for the minus terminal. It takes into account the vias (VIA1X, VIA2X, VIA3X, VIA4X and VIA5X) and the 5 metal levels resistance belonging to the minus side.

MODELED EFFECTS

GEOMETRY SCALING

The capacitance value contribution of one elementary capacitor is calculated using the expression:

$$capacitance = acoeff \times area + bcoeff$$

Capacitance variations for length = 10um see curves shown here (CC main capacitance is roughly 96% of total capacitance):

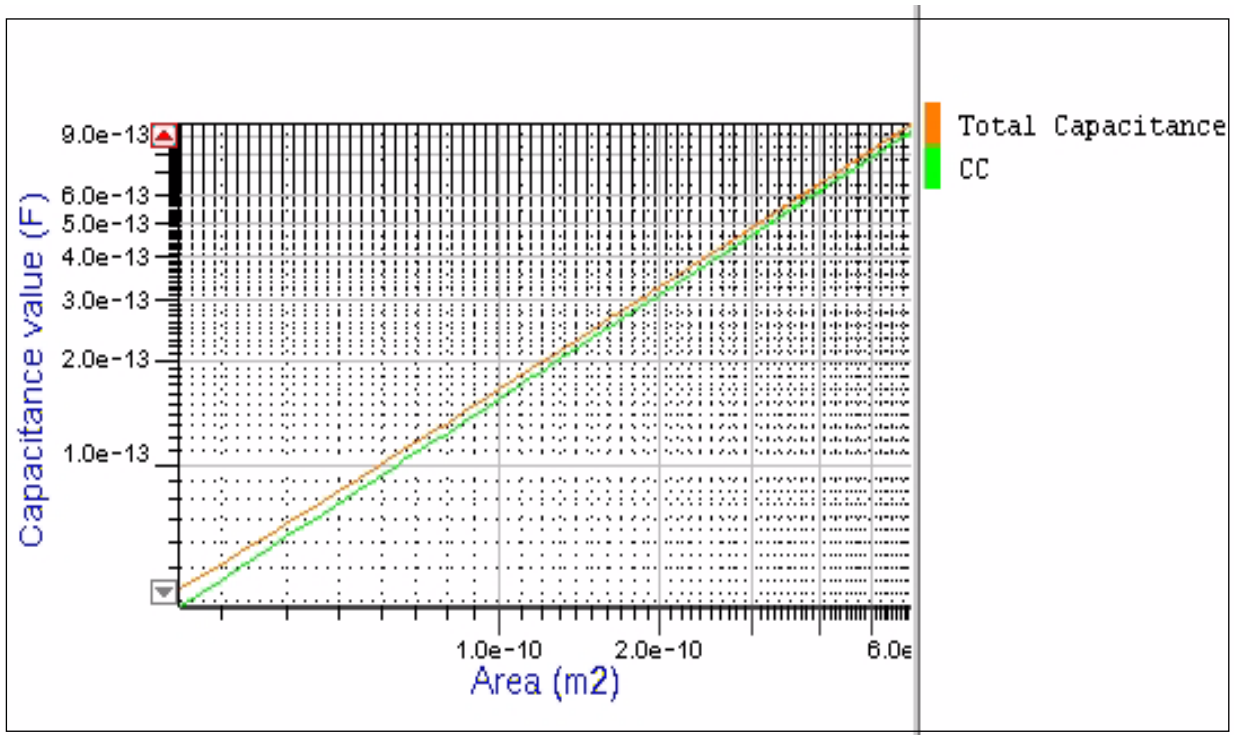

Figure 4 - Total and main capacitance values versus Area (for l = 10um)

Area is calculated as follows:

$$Area = l \times (\text{nf\_eff} \times pitch - space)$$

where

l : is capacitor lengthis specified fingers number.

nf_eff : is number of fingers recalculated inside the model to have odd number = plus pin fingers + minus pin fingers.

pitch : is space + finger width

space: is distance between two successive fingers

Variation of specific capacitance is shown in figure below for length = 50um:

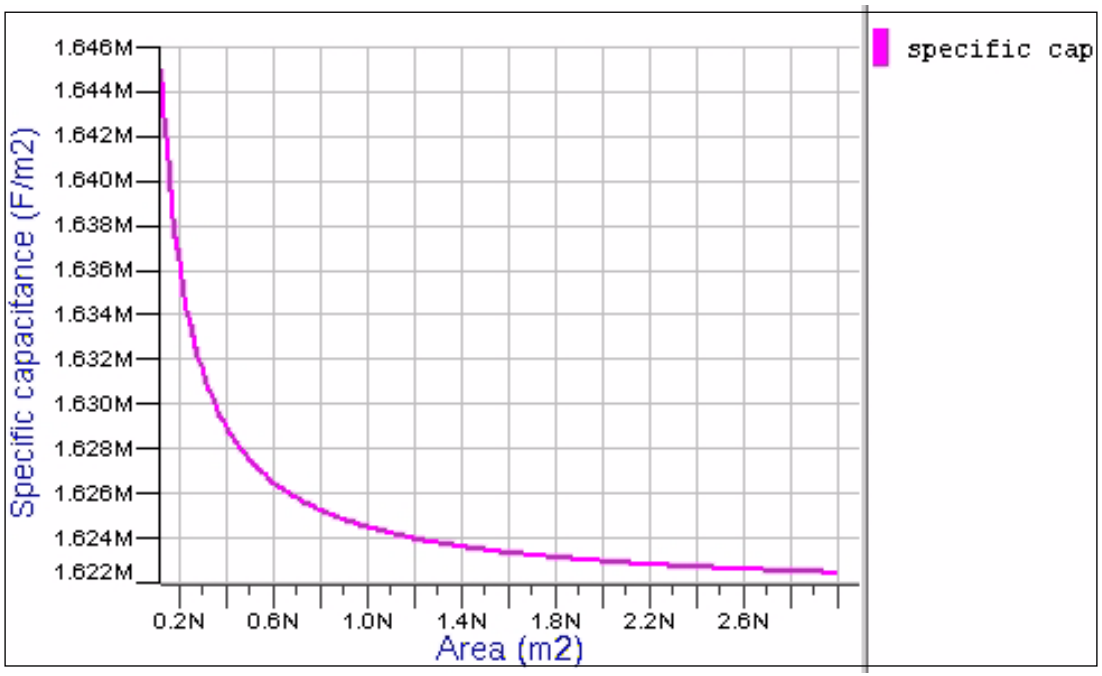

Figure 5 - Specific capacitance versus Area (for l = 50um)

MISMATCH MODEL

A normal distribution is used to estimate the expected main capacitance value:

$$capacitance = c0 \times (1 + \varepsilon)$$

where

- c0 : is the mean capacitance value given by the linear equation (1)
- ε : is a normal distribution with a standard deviation given by:

$$\sigma = \frac{c\_A}{\sqrt{2 \times c0}}$$

where

c_A : is the mismatch coefficient given by measurement values.

When c_A parameter is not specified no distribution is used and capacitance value is equal to c0+parasitic_capacitances.

The normal distribution is provided using the Eldo function: gauss

$$\varepsilon = 0 \qquad dev/gauss = 'fudge \times c\_A/(\sqrt{2 \times c0})'$$

where

fudge is a security parameter. It is used to be sure that the capacitance range covers measurements.

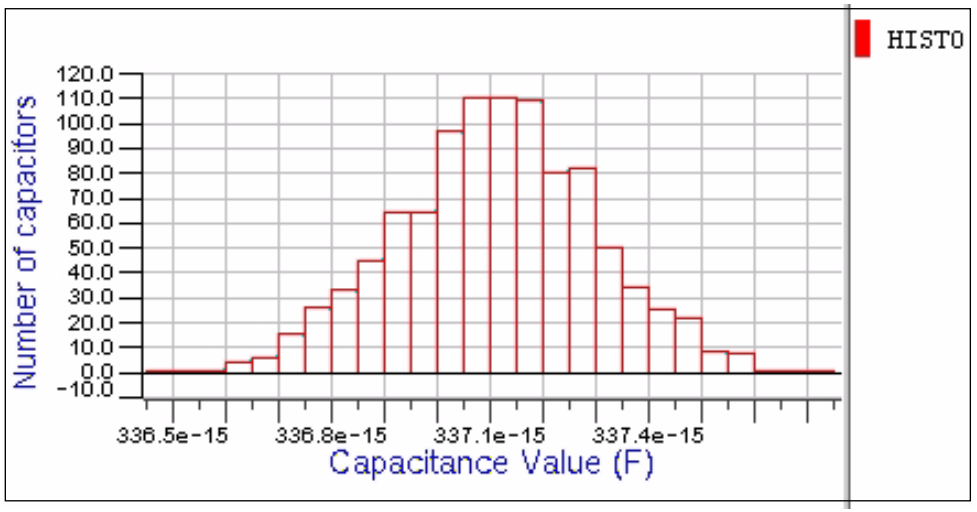

Figure 6 - Number of capacitors out of 1000 versus capacitance value

Example above is done for one cfrm1m5shx capacitor (number of fingers = 19 ; L = 50µm) simulation gives roughly: 337fF as capacitance value.

Relative[1] Standard Deviation specified: 0.59e-3

Relative Standard Deviation simulated (1000 random selection using a Monte Carlo Analysis): 0.56e-3

1. Standard deviation = Relative Standard deviation * Capacitance value.

PARASITIC COMPONENTS

❑ N+/Psubstrate diode (only the 5 pin fringe capacitor):

The isolation diode NWell/Psub must be in reverse-bias mode (Vod_shield ≈ Vnwell > Vsub). The diode model dnwps (nwell/psub) is instantiated using:

- Area = area of NWell rectangle Layout
- Perimeter = perimeter of NWell rectangle Layout.

The diode is connected to both OD shield and substrate as in figure 3.

❑ Series Resistors:

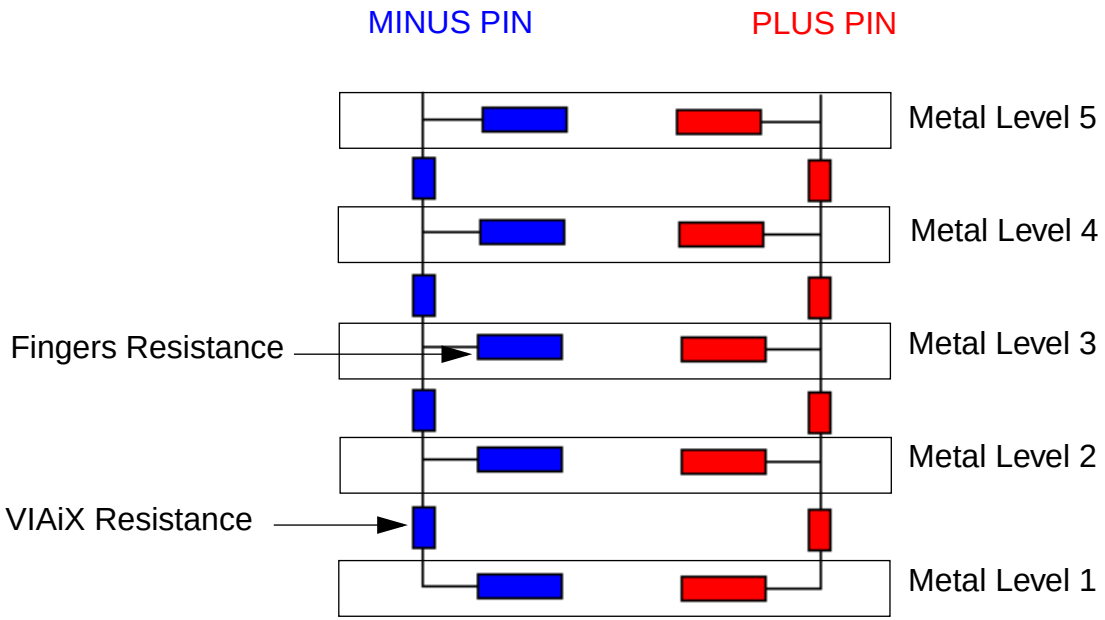

Figure 7 - Parasitic Resistors configuration for Pins PLUS and MINUS

POST LAYOUT SIMULATION

Each device is composed of two description levels (**name**, **name_acc**) coupled with the five pin model definitions. Each one is managed by the LPE flag option, which permits to select the Resistor/Capacitor access modeling mode. See the following table depicting the proposed options :

LPE	Body	Access_R	Access_C	Extraction_mode
0	yes	yes	yes	--
1	yes	yes	no	C
2	yes	no	yes	R
3	yes	no	no	RC

The Front-End Models (F-E) :

name, a simple model which contains intrinsic and parasitic capacitances (between the Plus/Shield_Poly, Plus/Shield_OD, Minus/Shield_Poly, Minus/Shield_OD and Shield_Poly/Shield_OD) and isolation diode (NWell/Substrate) but it excludes parasitic series resistances (LPE=0).

name_acc, a complete model which contains intrinsic, parasitic capacitances, and series resistances (LPE=0).

The Back-End Models (B-E) :

The **name** B-E model is identical to the **name** F-E model concerning the elementary capacitances contribution, but it excludes the NWell/substrate diode (LPE=1,2 or 3 according to the user choice).

The **name_acc** B-E model is identical to the **name_acc** F-E model concerning the elementary capacitances contribution and parasitic resistance, but it excludes the NWell/substrate diode (LPE=1,2 or 3).

CORNERS CONSTRUCTION

❑ Design Rule Manual parameters

rsq_M1, rsq_M2_4 and rviax parameter corners are given by DRM

❑ Simulation parameters

Linear coefficients coeffa, coeffb, acoeffapo_shpo, bcoeffapo_shpo, acoeffapo_shod, bcoeffapo_shod, acoeffbod_shpo, bcoeffbod_shpo, acoeffbod_shod, bcoeffbod_shod, acoeffshod_shpo and bcoeffshod_shpo are extracted using Quickcap simulations and the expressions below:

capacitance_MIN_Corner = acoeff_MIN*$area$ + bcoeff_MIN

capacitance_MAX_Corner = acoeff_MAX*$area$ + bcoeff_MAX

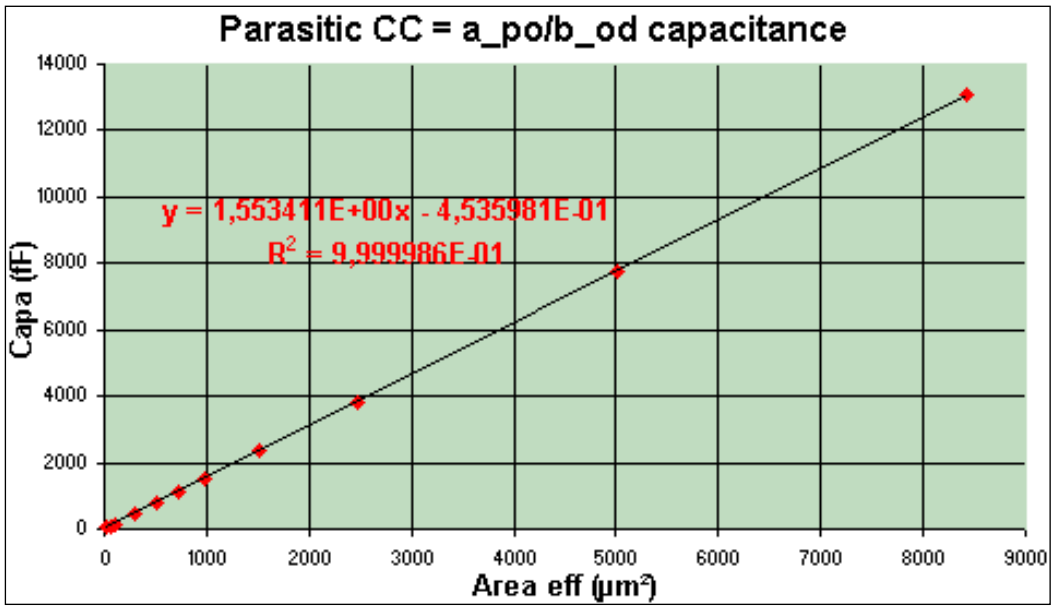

Figure 8 - Example of main capacitance a and b coefficients extraction

Figure below shows capacitance corners versus area. This result depends on the construction of MAX and MIN corners shown in paragraph above.

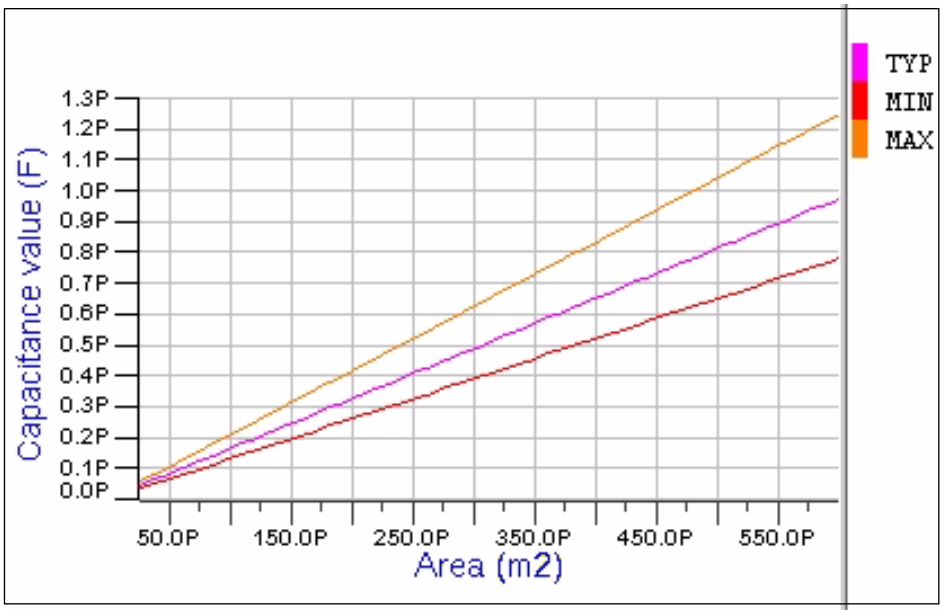

Figure 9 - Example of capacitance corners simulation (MAX and MIN)

MODEL PARAMETER LIST

diode	parasitic diode model name
cdef	(F) minimum device capacitance
cmin	(F) cmin=cdef by default
cmax	(F) maximum device capacitance
nfdef	() default number of fingers
nfmin	() minimum number of fingers
nfmax	() maximum number of fingers given
wvia	(m) via width
spacevia	(m) space via
cem	(m) enclosure via by metal1
ldef	(m) Lfinger_effective_min
lmin	(m) Lfinger_effective_min
lmax	(m) Lfinger_effective_max
lbusdef	(m) lbus min given by definition (fingermin=nfdef*pitch-space)
lbusmin	(m) lbus min given by definition (fingermin=nfmin*pitch-space)
lbusmax	(m) lbus max given by (fingermax=nb_finger_max*pitch-space)
space	(m) Space between metaln-metaln
wf	(m) Width metaln for fingers
lfbus	(m) Length between end of finger and bus

wbus	(m) width of bus
mtlbot	() (PCELL) Metal bottom level for capacitor
mtltop	() (PCELL) Metal top level for capacitor
shieldext	(m) Distance from bus cap to metal1 shield
shieldcont	(m) Width of metal1 shields
shieldnw	(m) Distance nwell to metal1 of shield
shieldencp	(m) Shield enclosure plus finger
shieldencm	(m) Shield enclosure minus finger
c_A	(sqrt(F)) for capacitance mismatch
fudge	() security margin
rsq_M1[a]	(ohm/square) sheet Resistance of M1
rsq_M2_4	(ohm/square) sheet Resistance of metals M2 to M5
rviax	(ohm) Resistance of one Viaix
coeffa	(F/m2) A_MAIN_CAP: fit coef. for main cap. on Quickcap extraction
coeffb	(F) B_MAIN_CAP: fit coef for par cap. on Quickcap extraction
acoeffapo_shpo	(F/m2) A_PLUS_SH.POLY: fit coef for par cap.F/m2 on Quickcap extraction
bcoeffapo_shpo	(F) B_PLUS_SH.POLY: fit coef for par cap.F on Quickcap extraction
acoeffapo_shod	(F/m2) A_PLUS_SH.OD: fit coef for par cap.F/m2 on Quickcap extraction
bcoeffapo_shod	(F) B_PLUS_SH.OD: fit coef for par cap.F on Quickcap extraction
acoeffbod_shpo	(F/m2) A_MINUS_SH.POLY: fit coef for par cap.F/m2 on Quickcap extraction
bcoeffbod_shpo	(F) B_MINUS_SH.POLY: fit coef for par cap.F on Quickcap extraction

acoeffbod_shod	(F/m2) A_MINUS_SH.OD: fit coef for par cap.F/m2 on Quickcap extraction
bcoeffbod_shod	(F) B_MINUS_SH.OD: fit coef for par cap.F on Quickcap extraction
acoeffshod_shpo	(F/m2) A_SH.OD_SH.POLY: fit coef for par cap.F/m2 on Quickcap extraction
bcoeffshod_shpo	(F) B_SH.OD_SH.POLY: fit coef for par cap.F on Quickcap extraction

a. In blue: parameters with MIN and MAX corners (see paragraph before)