SVT_GP MODELS (NSVTGP, PSVTGP)

1. CONDITIONS OF EXTRACTION

- Maturity: Preliminary
- Model parameters extraction based on lot : -
- Geometrical extraction domain:
  - Drawn gate length : 0.18 ≥ L ≥ 0.06 µm
  - Drawn transistor width : 10 ≥ W ≥ 0.12 µm
- Temperature extraction domain: -40 ˚C to 150 ˚C
- Bias extraction domain:
  - Gate bias: 0 ≤ |VGS| ≤ 1.1 V (VDD + 10%)
  - Drain bias: 0 ≤ |VDS| ≤ 1.1 V (VDD + 10%)
  - Bulk bias: 0 ≤ |VBS| ≤ 1.1 V (VDD + 10%)

2. CONDITIONS OF SIMULATION

- Temperature: 25 ˚C
- Currents:

  IDLIN = Ids at Vgs = 1.0 V, Vds = 50 mV and Vbs = 0 V

  ION = Ids at Vgs = 1.0 V, Vds = 1.0 V and Vbs = 0 V

  IOFF = Ids at Vgs = 0 V, Vds = 1.0 V and Vbs = 0 V

  IG_ON = Igs at Vgs = 1.0 V and Vd= Vs = Vb = 0 V

  IG_OFF = Igs at Vgs =Vbs = 0 V and Vds = 1.0 V
- Threshold voltage in linear and saturation regime

  VTLIN is Vgs value at Vds = 50 mV, Vbs = 0 V and Ids= 40*W/L nA.

  VTSAT is Vgs value at Vds = 1.0 V, Vbs = 0 V and Ids= 40*W/L nA.
- Current derivatives:

$$Gm = \frac{\partial}{\partial V_{gs}} Ids$$ at Vgs = VTLIN + 0.2 V, Vds = 0.5 V and Vbs = 0 V

$$Gd = \frac{\partial}{\partial V_{ds}} Ids$$ at Vgs = VTLIN + 0.2 V, Vds = 0.5 V and Vbs = 0 V

Analog gain = Gm/Gd

- Gate Capacitances:

  CGGINV = CGG at Vgs = 1.0 V, Vds = 0 V and Vbs = 0 V

  CGD_0V = CGD at Vgs = 0 V, Vds = 0 V and Vbs = 0 V

  $$CGGMEAN = \frac{1}{VDD} \cdot \int_{0}^{VDD} CGG \times dVgs$$ with VDD = 1.0 V and Vbs = 0 V

  TAU = CGGMEAN*VDD/ION

- Diode Capacitances:

  CBD OFF = CBD at Vgs = 0 V, Vds = 1.0 V and Vbs = 0 V

  Note: the area and perimiters of source/drain junction diodes used for simulation are defined with the the minimum poly-to-active distance specified in the DRM.

- Transition frequency:

  FT = frequency for which the small signal current gain H_{21} is 0 dB (i.e. $\left|\frac{I_d}{I_g}\right|$ = 0 dB).

3. MAIN ELECTRICAL CHARACTERISTICS OF NMOS SVT_GP TRANSISTORS

PARAMETERS	SVTGP_TT	SVTGP_SS	SVTGP_FF	units
N-channel transistors (nsvtgp)				
VTLIN W=1/L=0.18	274	300	249	mV
IDLIN W=1/L=0.18	4.56e-05	4.12e-05	5.04e-05	A
VTSAT W=1/L=0.18	244	269	218	mV
ION W=1/L=0.18	2.53e-04	2.20e-04	2.89e-04	A
VTLIN W=1/L=0.06	245	296	187	mV
IDLIN W=1/L=0.06	1.27e-04	1.11e-04	1.46e-04	A
VTSAT W=1/L=0.06	115	178	44	mV
ION W=1/L=0.06	8.10e-04	6.76e-04	9.70e-04	A
IOFF W=1/L=0.06	5.09e-08	1.12e-08	2.58e-07	A
IG_ON W=1/L=0.06	6.77e-09	3.38e-09	1.37e-08	A
IG_OFF W=1/L=0.06	1.10e-09	5.57e-10	2.20e-09	A
FT W=1/L=0.06	2.97e+11	2.65e+11	3.35e+11	Hz
CGGinv W=1/L=0.06	8.04e-16	8.51e-16	7.52e-16	F
CGGmean W=1/L=0.06	7.72e-16	7.97e-16	7.39e-16	F
CGD 0V W=1/L=0.06	3.44e-16	3.40e-16	3.48e-16	F
CBD OFF[a] W=1/L=0.06	4.85e-16	5.50e-16	4.17e-16	F
Tau W=1/L=0.06	1.0	1.2	0.8	ps
Gm W=1/L=0.06	5.20e-04	4.75e-04	5.69e-04	S
Gd W=1/L=0.06	8.02e-05	6.74e-05	9.56e-05	S
Gain W=1/L=0.06	6.49e+00	7.05e+00	5.94e+00	
VTLIN W=0.12/L=0.06	208	259	152	mV
IDLIN W=0.12/L=0.06	1.75e-05	1.50e-05	2.03e-05	A
VTSAT W=0.12/L=0.06	107	165	41	mV
ION W=0.12/L=0.06	1.08e-04	8.74e-05	1.32e-04	A
IOFF W=0.12/L=0.06	7.43e-09	1.80e-09	3.33e-08	A
FT W=0.12/L=0.06	2.28e+11	1.97e+11	2.67e+11	Hz

Table 1: Main electrical characteristics for NMOS

a. Value coresponding to the minimum poly-to-acvtive distance specified in the DRM

4. MAIN ELECTRICAL CHARACTERISTICS OF PMOS SVT_GP TRANSISTORS

PARAMETERS	SVTGP_TT	SVTGP_SS	SVTGP_FF	units
P-channel transistors (psvtgp)				
VTLIN W=1/L=0.18	191	218	165	mV
IDLIN W=1/L=0.18	2.09e-05	1.88e-05	2.33e-05	A
VTSAT W=1/L=0.18	155	182	127	mV
ION W=1/L=0.18	1.70e-04	1.47e-04	1.96e-04	A
VTLIN W=1/L=0.06	249	300	186	mV
IDLIN W=1/L=0.06	4.55e-05	3.89e-05	5.35e-05	A
VTSAT W=1/L=0.06	140	202	60	mV
ION W=1/L=0.06	3.82e-04	3.07e-04	4.84e-04	A
IOFF W=1/L=0.06	2.46e-08	4.84e-09	1.75e-07	A
IG_ON W=1/L=0.06	5.06e-09	2.31e-09	1.19e-08	A
IG_OFF W=1/L=0.06	1.02e-09	5.09e-10	2.06e-09	A
FT W=1/L=0.06	1.32e+11	1.11e+11	1.58e+11	Hz
CGGinv W=1/L=0.06	8.66e-16	9.32e-16	8.03e-16	F
CGGmean W=1/L=0.06	8.11e-16	8.47e-16	7.74e-16	F
CGD 0V W=1/L=0.06	3.33e-16	3.20e-16	3.43e-16	F
CBD OFF[a] W=1/L=0.06	5.00e-16	5.66e-16	4.30e-16	F
Tau W=1/L=0.06	2.1	2.8	1.6	ps
Gm W=1/L=0.06	2.89e-04	2.54e-04	3.35e-04	S
Gd W=1/L=0.06	4.13e-05	3.12e-05	5.81e-05	S
Gain W=1/L=0.06	6.99e+00	8.15e+00	5.76e+00	
VTLIN W=0.12/L=0.06	166	223	91	mV
IDLIN W=0.12/L=0.06	6.90e-06	5.92e-06	8.02e-06	A
VTSAT W=0.12/L=0.06	69	136	-16	mV
ION W=0.12/L=0.06	6.05e-05	4.83e-05	7.66e-05	A
IOFF W=0.12/L=0.06	1.31e-08	2.24e-09	1.18e-07	A
FT W=0.12/L=0.06	9.22e+10	7.80e+10	1.06e+11	Hz

Table 2: Main electrical characteristics for PMOS

a. Value coresponding to the minimum poly-to-acvtive distance specified in the DRM

5. ION, IOFF, VT BEHAVIOR VERSUS GATE LENGTH AND CHANNEL WIDTH FOR NMOS SVT_GP TRANSISTORS

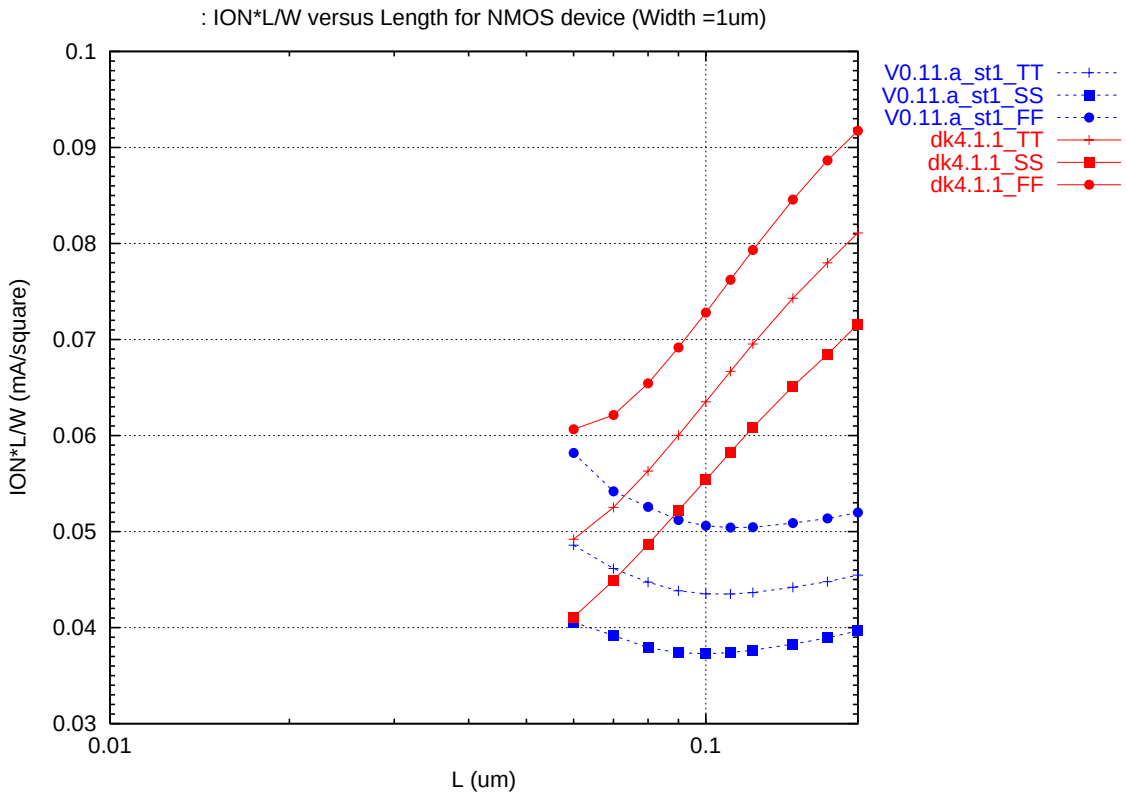

Figure 1 : ION/❑=ION*L/W versus drawn gate length for NMOS SVT_GP transistors (W = 1 µm)

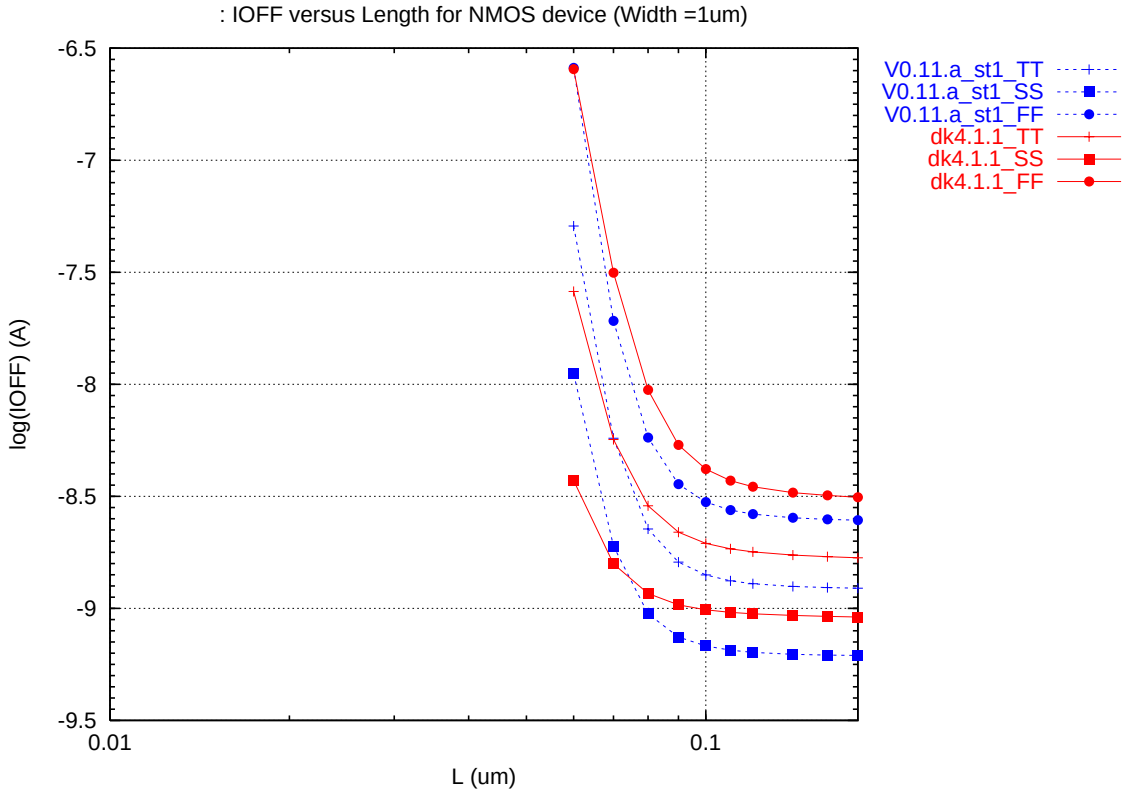

Figure 2 : IOFF versus drawn gate length for NMOS SVT_GP transistors (W = 1 µm)

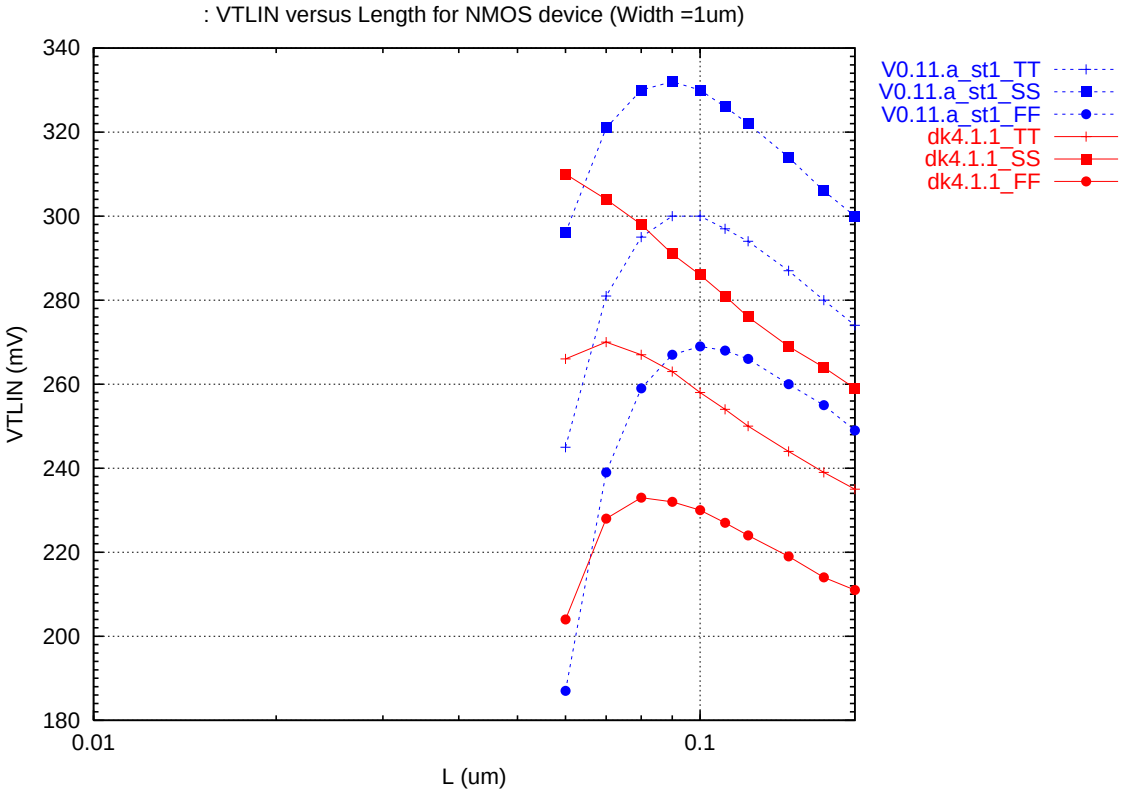

Figure 3 : Threshold voltage VTLIN versus drawn gate length for NMOS SVT_GP transistors (W = 1 µm)

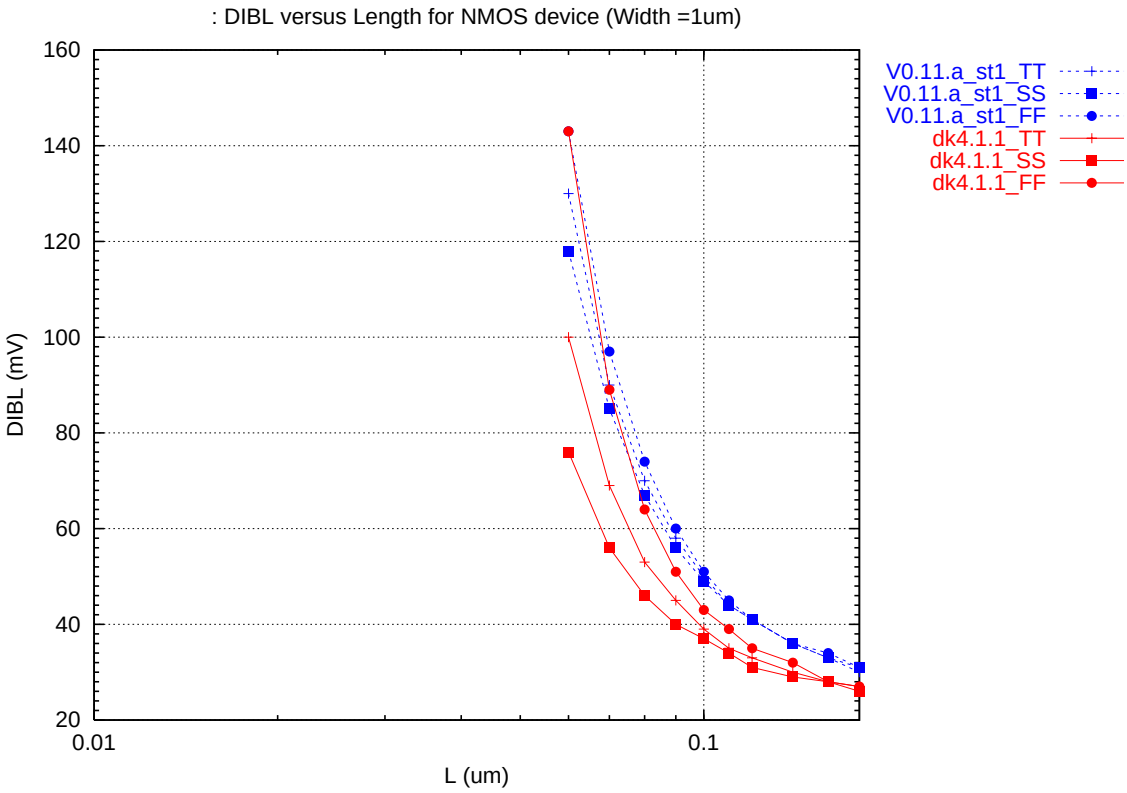

Figure 4 : DIBL= VTLIN-VTSAT versus drawn gate length for NMOS SVT_GP transistors (W = 1 µm)

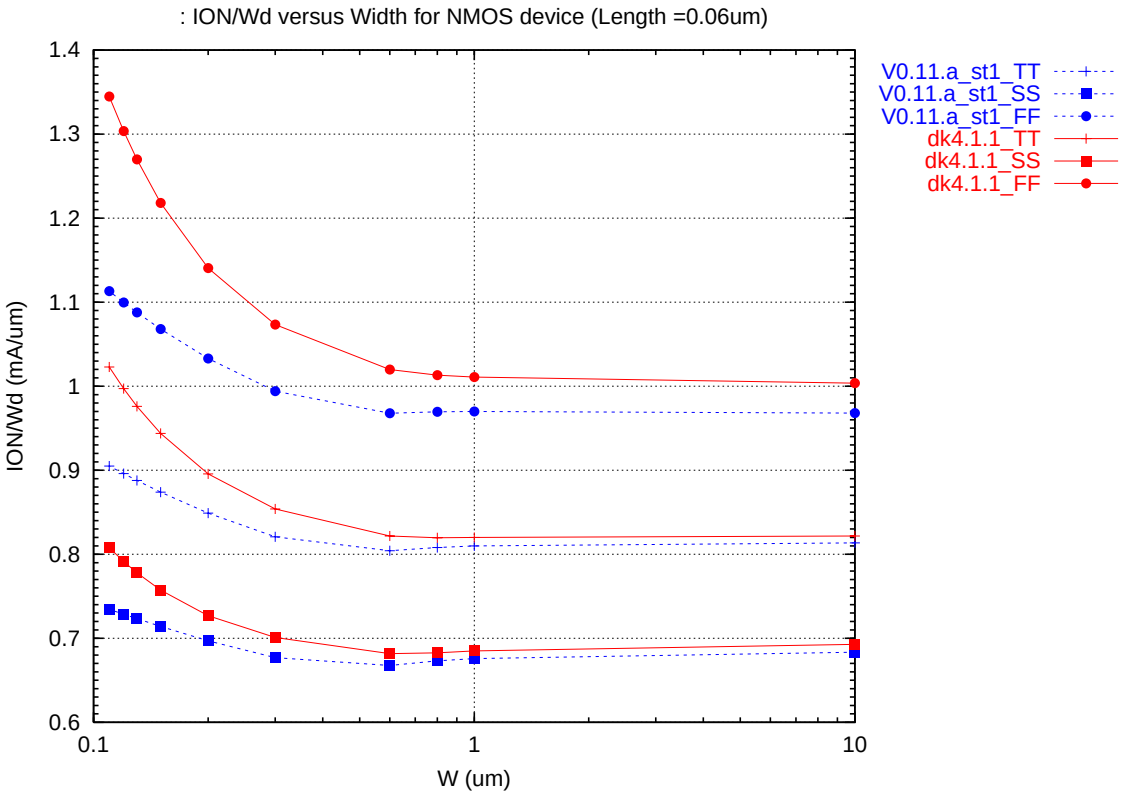

Figure 5 : ION versus drawn channel width for NMOS SVT_GP transistors (L = 0.06 µm)

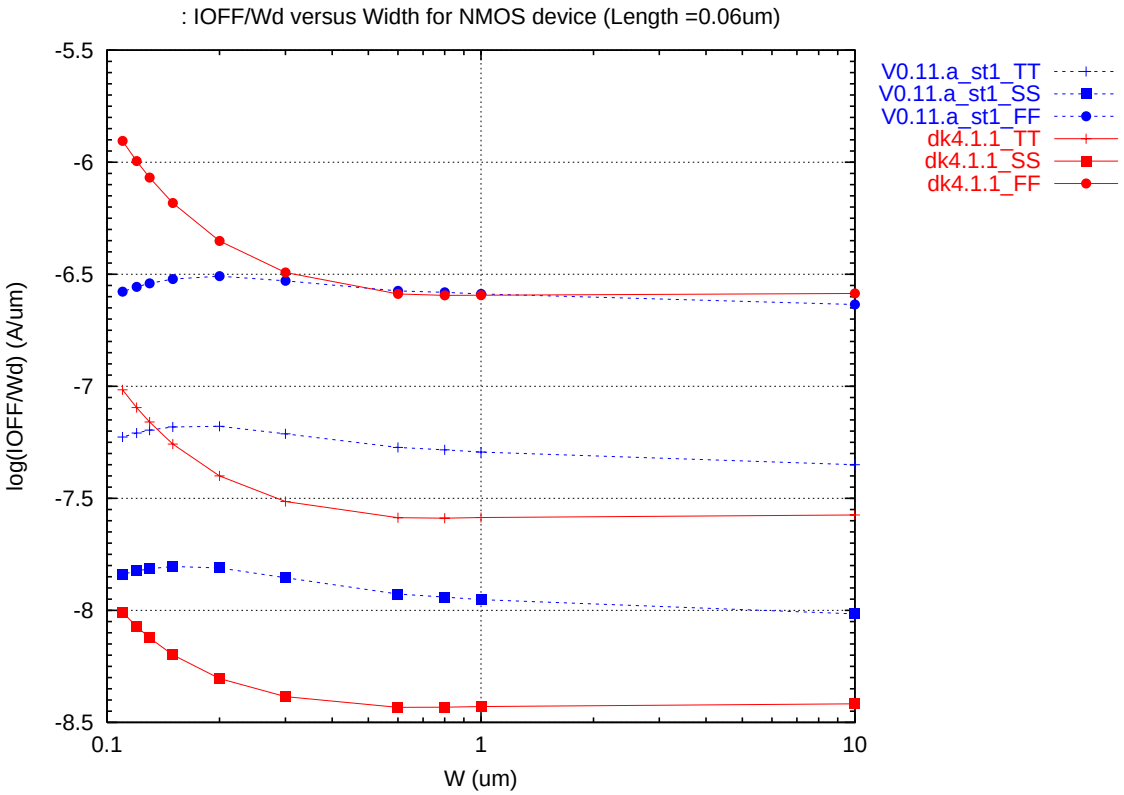

Figure 6 : IOFF versus drawn channel width for NMOS SVT_GP transistors (L = 0.06 µm)

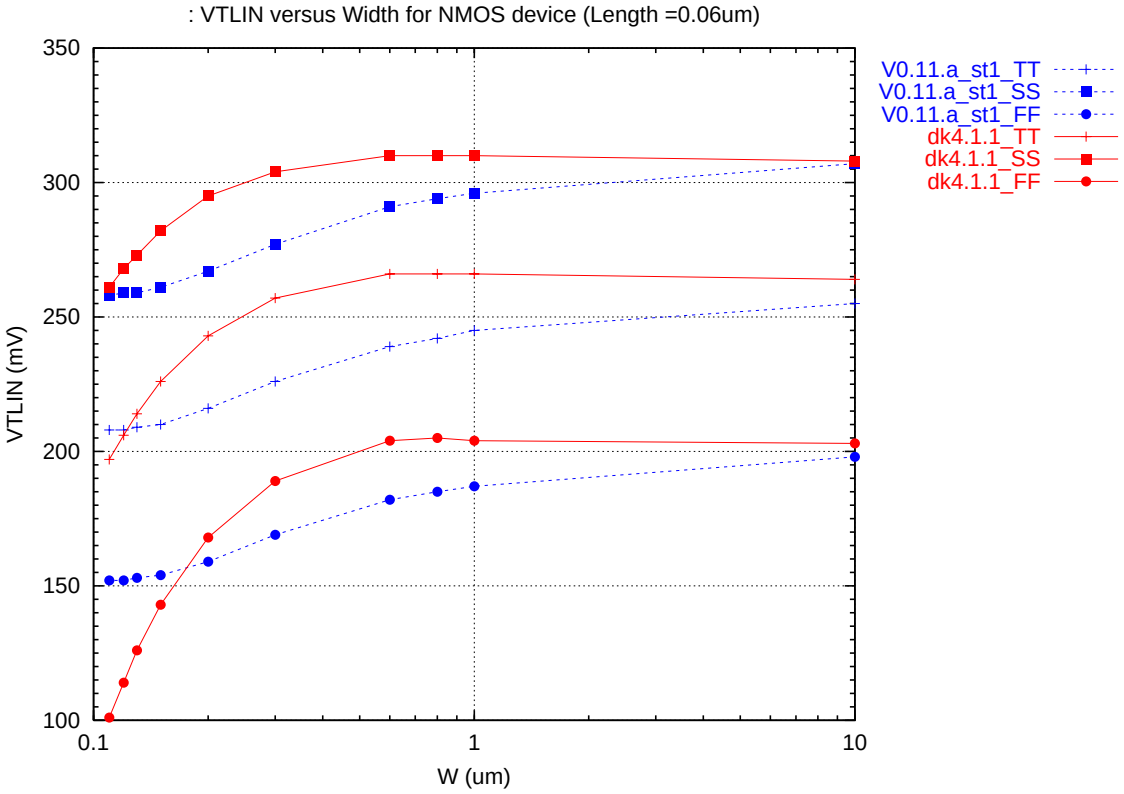

Figure 7 : Threshold voltage VTLIN versus drawn channel width for NMOS SVT_GP transistors (L = 0.06 µm)

6. ION, IOFF, VT BEHAVIOR VERSUS GATE LENGTH AND CHANNEL WIDTH FOR PMOS SVT_GP TRANSISTORS

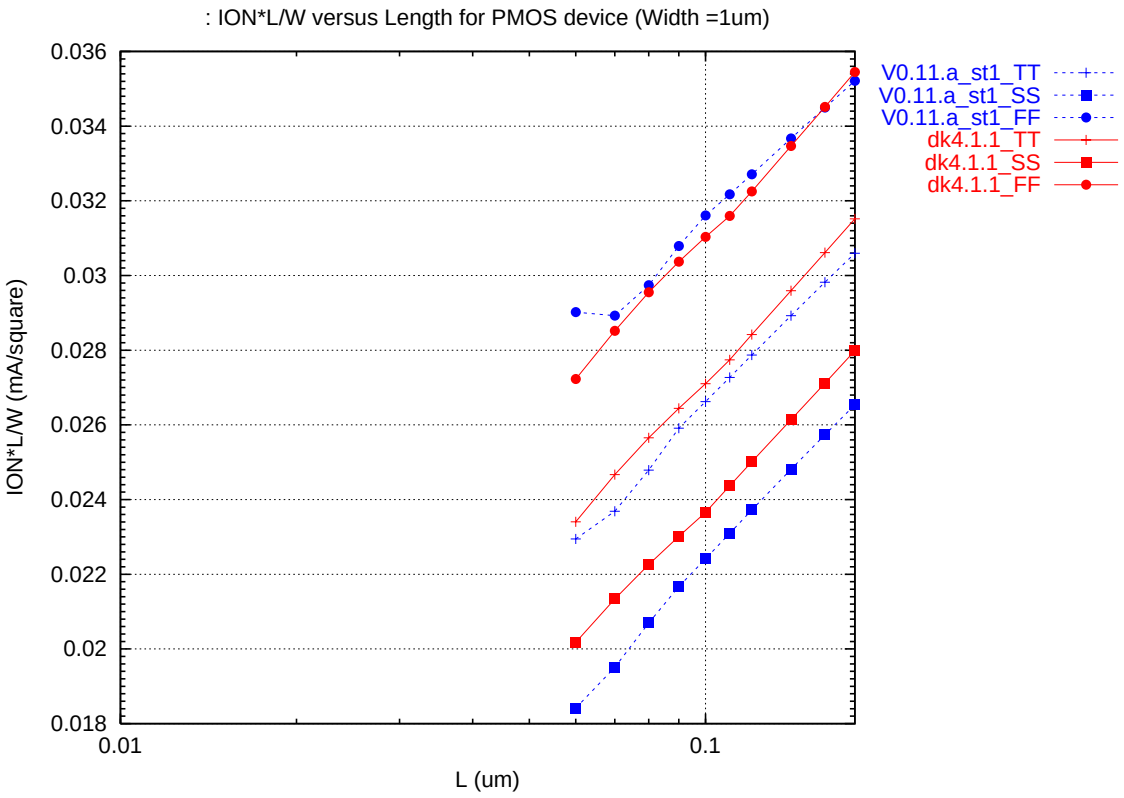

Figure 8 : ION versus drawn gate length for PMOS SVT_GP transistors (W = 1 µm)

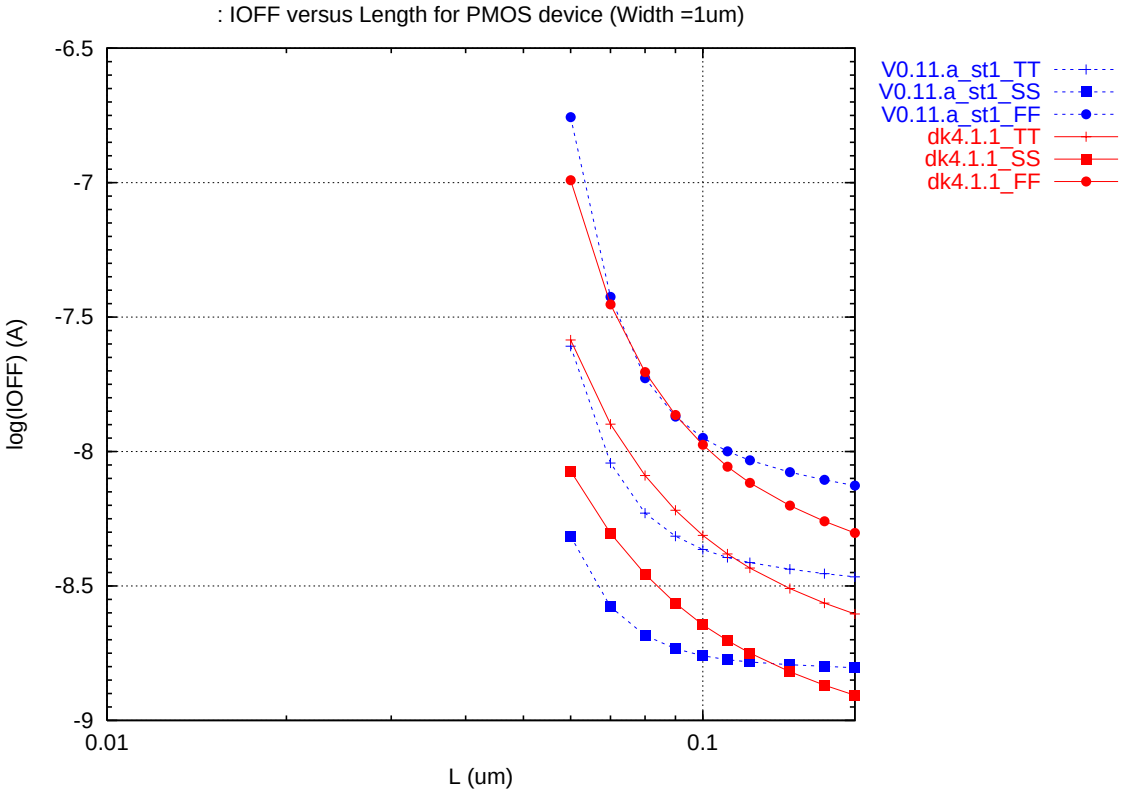

Figure 9 : IOFF versus drawn gate length for PMOS SVT_GP transistors (W = 1 µm)

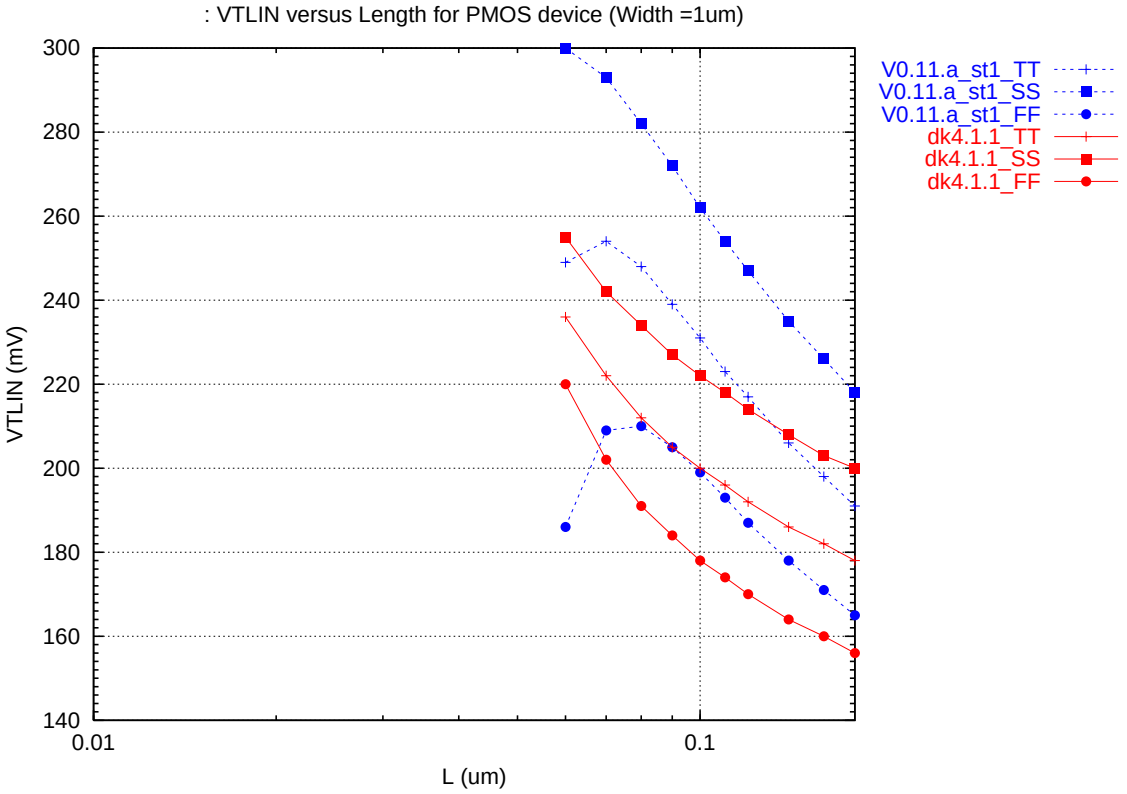

Figure 10 : Threshold voltage VTLIN versus drawn gate length for PMOS SVT_GP transistors (W = 1 µm)

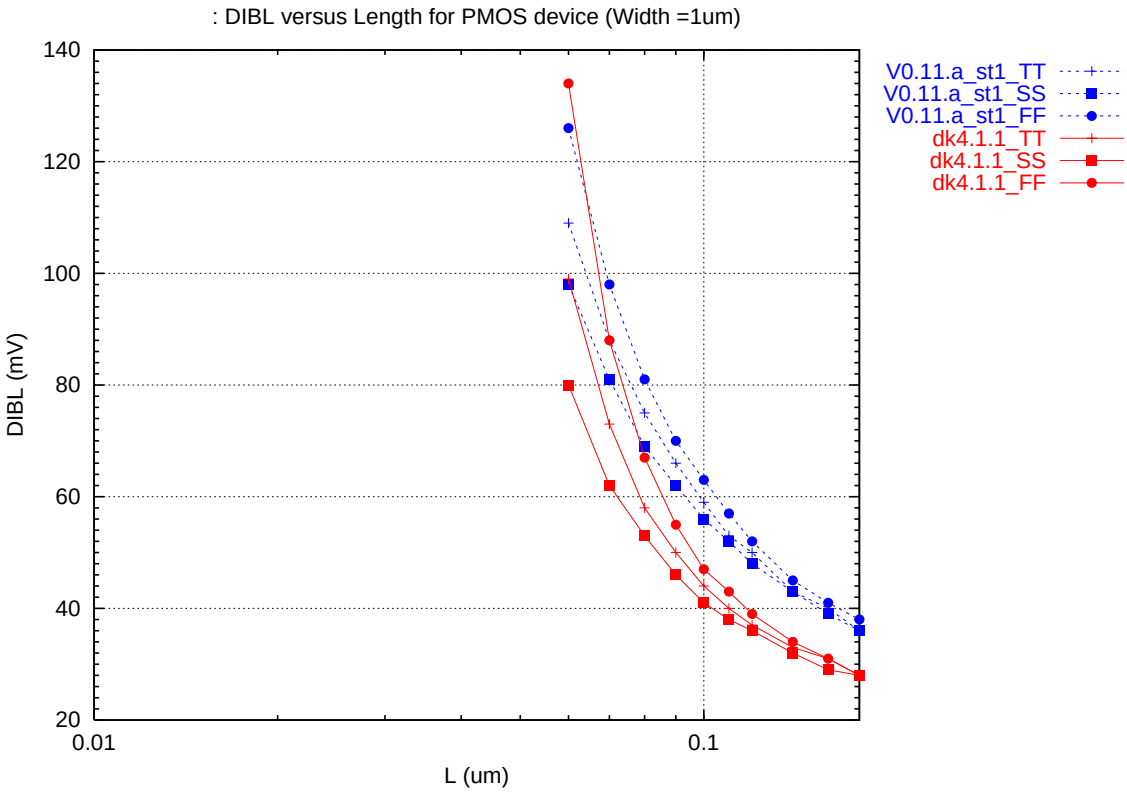

Figure 11 : DIBL= VTLIN-VTSAT versus drawn gate length for PMOS SVT_GP transistors (W = 1 µm)

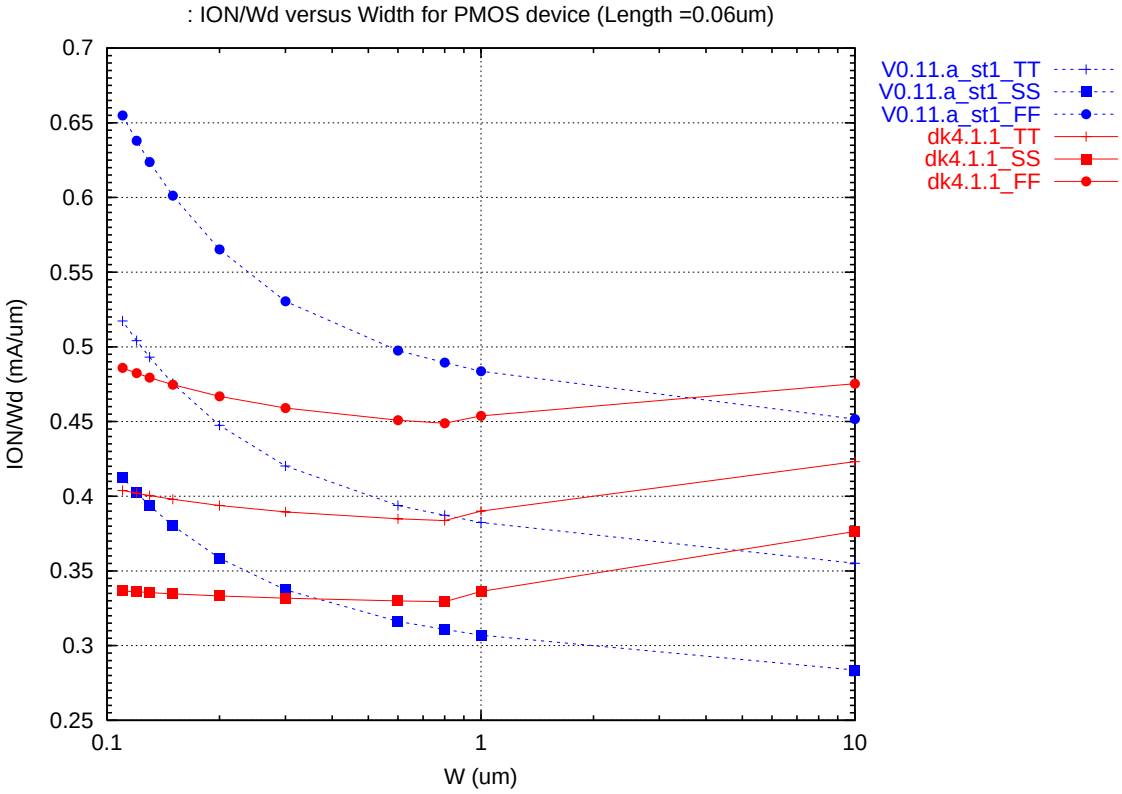

Figure 12 : ION versus drawn channel width for PMOS SVT_GP transistors (L = 0.06 µm)

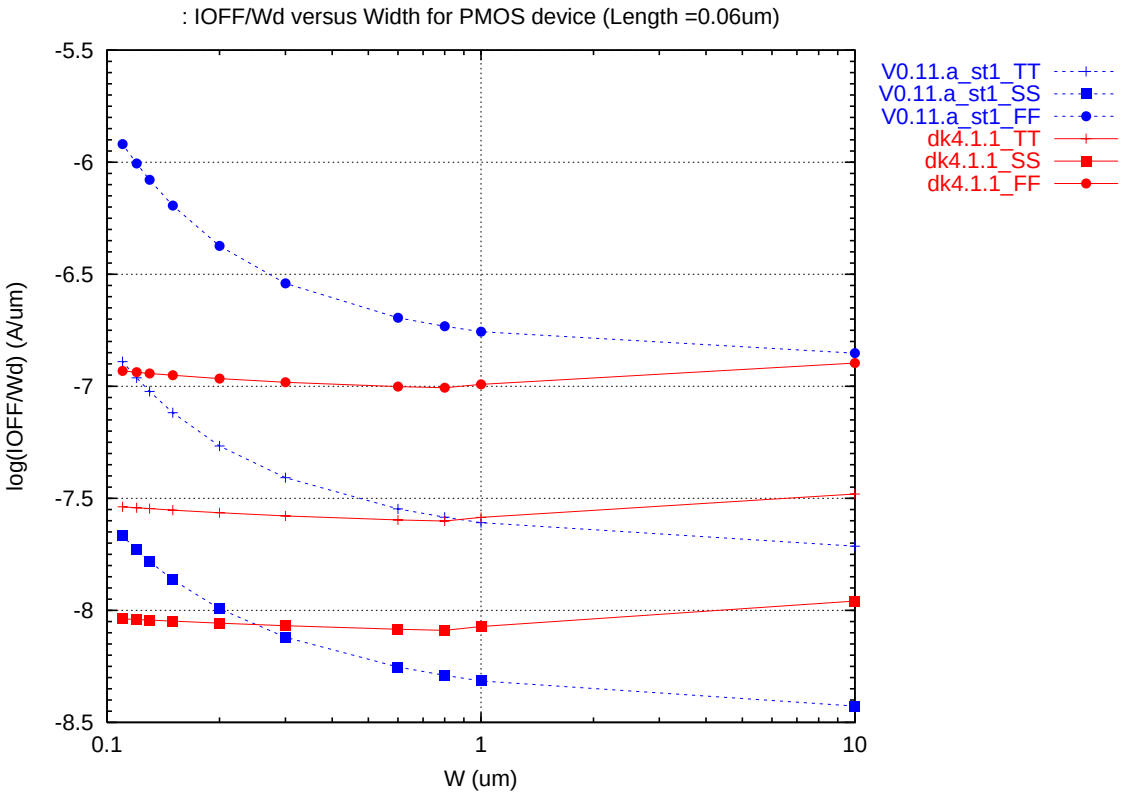

Figure 13 : IOFF versus drawn channel width for PMOS SVT_GP transistors (L = 0.06 µm)

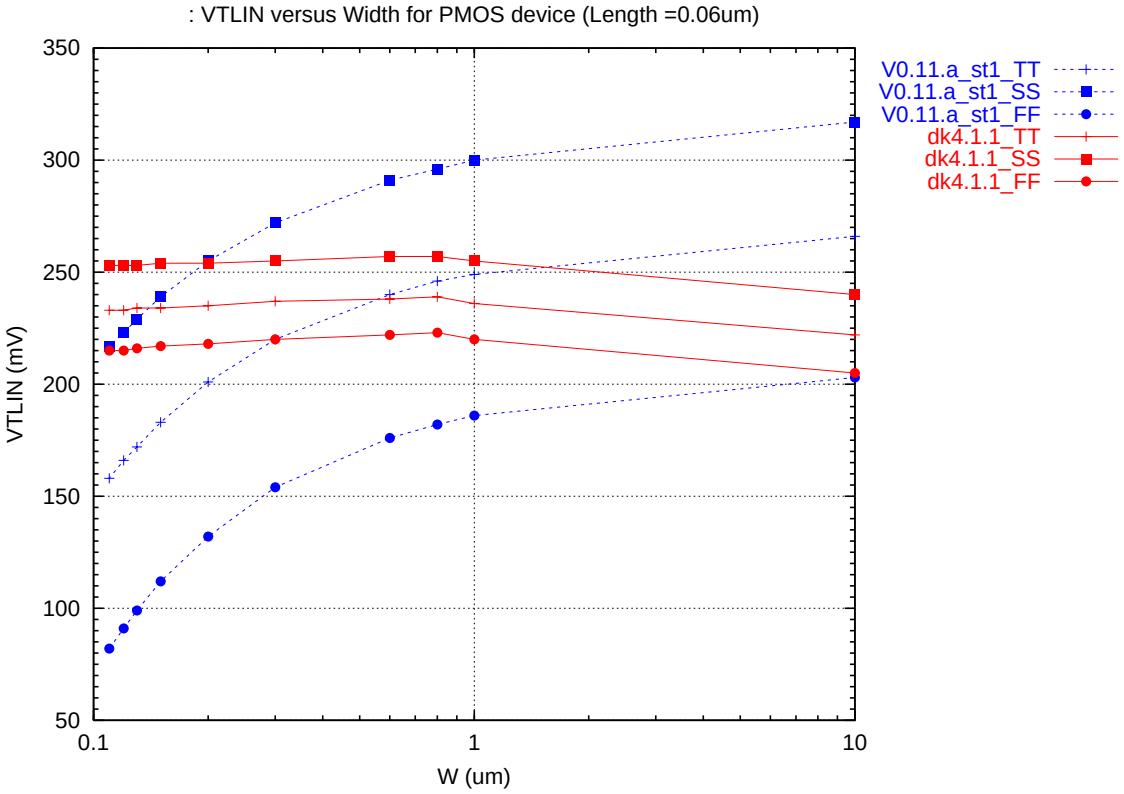

Figure 14 : Threshold voltage VTLIN versus drawn channel width for PMOS SVT_GP transistors (L = 0.06 µm)