CMOS065 DESIGN KIT

VERSION 4.x

UNICAD 24 / May 2006

Central CAD & Design Solutions
Front-End Technology & Manufacturing

UNICAD™ © 1989 All rights reserved

UNICAD™ is a trademark of STMicroelectronics

The following names are trademarks, registered trademarks, and service marks of other companies that appear in Unicad publications:

Adobe, the Adobe logo,FrameMaker, the FrameMaker logo, Acrobat, the Acrobat logo, Exchange, and PostScript are registered trademarks of Adobe Systems Incorporated.

ADS, AHB, AMBA, PrimeXsys, STD are trademarks of ARM, ltd.

Alanza, Allegro, Ambit, Analog Artist, Assura, BuildGates, Cadence, Cadence Logo, CoBALT, Composer, Concept, Connection, Diva, Dracula, Envisia, Formal Check, Gate Ensemble, GDSII, HDL_ICE, MegaSim, Mercury, NC Verilog, Orcad, Orcad Capture, Orcad Layout, Palladium, Pearl, PowerSuite, PSpice, Q/Bridge, QPlace, Quest, Quickturn, Radium, Transaction Explorer, Test Builder, Verification Cockpit Vampire, Verilog, Verilog XL, Verifault, Verifault XL, NC-Verilog, Cell3 Ensemble, Silicon Ensemble, Virtuoso, Spectre, and Leapfrog are trademarks and registered trademarks of Cadence Design Systems, Inc.

MemMaker, PureView, PureData are trademarks of Denali, Software Inc.

ApolloII, ApolloGAII, Apollo-DPII, Aurora, ASIC Synthesizer, AvanTestchip, AvanWaves, ChipPlanner, Columbia, Columbia-CE, Cyclelink, Davinci, DFM Workbench, Driveline, Dynamic Model Switcher, Electrically Aware, Enterprise, Evaccess, Hercules, Hercules-Explorer, HotPlace, HSPICE, HSPICE-LINK, Jupiter, LTL, Libra-Passport, Lynx, Lynx-LB, Lynx-VHDL, Mars, Mars-Rail, Mars-Xtalk, MASTER Toolbox, Medici, Michelangelo, Milkyway, Optimum Silicon, Passport, Pathfinder, Planet, Planet-PL, Planet-RTL, Polaris, Polaris-CBS, Polaris-MT, Progen, Prospector, Raphael, Raphael-NES, Saturn, Sirius, Silicon Blueprint, Smart Extraction, Solar, Solar II, Star, Star-Sim, Star-Hspice, Star-HspiceLink, Star-DC, Star-RC, Star-RCXT, Star-Power, Star-Time, Star-MTB, Star-XP, Taurus, Taurus-Device, Taurus-Layout, Taurus-Lithography, Taurus-OPC, Taurus-Process, Taurus-Topography, Taurus-Visual, Taurus-Workbench, TimeSlice, and TSUPREM-4 are trademarks of Avant! Corporation. Avant!, Avant! logo, AvanLabs, and avanticorp are trademarks and service-marks of Avant! Corporation.

ASAP, Aspire, C-FAS, CMPI, Eldo-FAS, EldoHDL, Eldo-Opt, Eldo-UDM, EldoVHDL, Eldo-XL, Elga, Elib, Elib-Plus, ESim, Fidel, Fideldo, GENIE, GENLIB, HDL-A, MDT, MGS-MEMT, MixVHDL, Model Generator Series (MGS), Opsim, SimLink, SimPilot, SpecEditor, Success, SystemEldo, VHDeLDO and Xelga are registered trademarks of ANACAD

Eldo, Calibre, ModelSim, FastScan, DFTAdvisor, Seamless, CVE, XRAY are registered trademarks of Mentor Graphics Corporation.

Debussy is a trademark of Novas Software, Inc.

DesignSync, DesignSync DFII, ProjectSync, IPGear are registered trademarks of Synchronicity Software, Inc.

FLEXlm is a trademark of Globetrotter Software, Inc.

HSPICE is a registered trademark of Meta-Software, Inc.

IKOS and Voyager are registered trademarks of IKOS Systems, Inc.

Java and all Java-based trademarks and logos are trademarks or registered trademarks of Sun Microsystems, Inc.

NeoCell, NeoCircuit are registered trademarks of Neolinear, Inc.

Netscape is a trademark of Netscape Communications Corporation.

SPARC is a registered trademark, and SPARCstation is a trademark, of SPARC International, Inc. Sun Microsystems, Sun Workstation, and NeWS are registered trademarks of Sun Microsystems, Inc.

Sun, Sun-2, Sun-3, Sun-4, OpenWindows, SunOS, SunView, NFS, and NSE are trademarks of Sun Microsystems, Inc.

Synopsys, Design Compiler, Physical Compiler, DFT Compiler, Test Compiler, Power Compiler, Module Compiler, Library Compiler, PrimeTime, Formality, Arcadia, Liberty, TetraMAX, LEDA, PathMill, PowerMill, TimeMill, Chip Architect and VSS are trademarks or registered trademarks of Synopsys, Inc.

UNIX, Solaris and OPEN LOOK are registered trademarks of UNIX System Laboratories, Inc.

Verisity is a trademark of Verisity Ltd. or its subsidiaries (Verisity),registered in the United States and other jurisdictions. The Verisity logo, Specman, Specview, Specman Elite, Verification Advisor, eVC, Pure IP, InvisibleSpecman, SureLint, Lintrpt, SureCov, and SureSight are trademarks of Verisity.

Versatec is a trademark of Xerox Engineering Systems, Inc.

Fire & Ice is a registered trademark, and ClockStorm, ElectronStorm, VoltageStorm, SubstrateStorm, IceCaps, Rain, SI Report, QIC Engine, 3D Adaptive Analytical Extraction, Accura, PGS Exploration, PerturbingPath, NetConnect, and SoC Design Foundry are trademarks of Simplex Solutions, Inc.

TransEDA, VeriSure, VHDLCover, HDLCover, CoverPlus, StateSure, Verification Navigator, State Navigator, TransEDA Verification Navigator and TransEDA State Navigator are trademarks of TransEDA Limited.

Other brand or product names that appear in Unicad publications are trademarks or registered trademarks of their respective holders.

Revision History

Release	Date	Summary of Changes
4.0	Feb 2006	- ch 1.1 : Added informations on DK documentations - ch 2.2.2 , cmos065 devices part : . MOS : new SRAM MOS + new nnvt native MOS . CAPACITORS : Addition of the mim capacitors, added notes on metal capacitors, addition of the cpolppw . MISC : Addition of the layout finishing flow devices - ch 2.2.3: . Added notes on obsolete and new contacts . Added table on supported contacts . Updated the symbolics contacts table . Added multipart paths and symbolic pin parts - ch. 2.3 : moved Tiling part layout finishing devices paragraph to a new chapter 5 : Layout Finishing flow - New ch.3 : Migration procedures Added notes on update cdf, update pcells, WOD and Design migration procedures - New chap 4: blackbox user guide - New ch.5 : Calibre part removed, infos moved to Calibre and PLS doc. Layout Finishing Flow part instead - ch. 6 : added MIM in electrical/geometrical devices list

© STMicroelectronics - Reproduction and Communication of this document is strictly prohibited unless specifically authorized in writing by STMicroelectronics

4.1	Mar 2006	- ch 2.2.2 , cmos065 devices part : . CAPACITORS : Addition of the cmstrstk capacitor (striped stacked metal capacitor) . Models update : addition of new models (gated diodes, diodes 18, otp mos) and removal of GP SRAM MOS models (no more supported) - ch 2.2.4, cmos065_a devices part: . added HPA (High Performance Analog) MOS : nhpalp and phpalp - ch 2.2.3: . Updated the symbolics contacts table : put AP_Mi, Mi_MKTOPMIM and Mi_BOTMIM in obsolete category - ch. 6 : added cmstrstk in electrical/geometrical devices list - ch 9.1 (DK RF only) : cmos065_rf part . INDUCTORS : addition of the inddif_lonw inductors . MOS : addition of the MOS HPA RF nhpalp_rf and phpalp_rf . CAPACITORS : addition of the MOM RF without and with shield - ch 9.2 (DK RF only) : addition of inddif_lonw inductors and MOM rf in electrical/geometrical devices list.
4.2	May 2006	- ch 2.2.2 , cmos065 devices part : . MOS : Addition of ndr18otp . Models update : addition of new models (ndr18otp, nsvt25dram, cpolpnw, cpolppw, cpo18nw, cpoGP SRAM 0.62um2 Dual Port)

© STMicroelectronics - Reproduction and Communication of this document is strictly prohibited unless specifically authorized in writing by STMicroelectronics

TABLE OF CONTENTS

© STMicroelectronics - Reproduction and Communication of this document is strictly prohibited unless specifically authorized in writing by STMicroelectronics

© STMicroelectronics - Reproduction and Communication of this document is strictly prohibited unless specifically authorized in writing by STMicroelectronics

© STMicroelectronics - Reproduction and Communication of this document is strictly prohibited unless specifically authorized in writing by STMicroelectronics

© STMicroelectronics - Reproduction and Communication of this document is strictly prohibited unless specifically authorized in writing by STMicroelectronics

1 - INTRODUCTION

1.1 Product description

A Design Kit can be defined as a unified and packaged set of data / libraries. It allows to perform all the steps of the design flow (for the design of cells/macrocells at device level) in a given CAD platform for a specific process or process option. (standard cell libraries not included).

The present Design Kit supports the following main features :

- **Schematic capture : CADENCE, COMPOSER**
- **Layout capture : CADENCE, VIRTUOSO**
- **Pcells**
- **Electrical simulation : Eldo, Spectre, Hspice, ADS (RF DKs only)**

See Modelsdoc and ModelsStatus directories under $DKITROOT/doc/Manuals/ for further details.

- **Layout verification : CALIBRE (DRC and LVS)**

See Calibre doc under $DKITROOT/doc/Manuals/ for further details

- **Post Layout Simulation : STAR-RCXT**

See PLS doc (i.e PLSTraining) under $DKITROOT/doc/Manuals/ for further details.

- **Layout-Finishing Flow : mask pattern addition (Pcell)+ Dummies generation + Calibre DRC & LVS**

See chapter 5 of this document for further details

For all extra features or tools included in the DK (DKtools, DKShared, GDSXor, calibrerun...), please refer either to the chapter 4 of this document ("Design Kit Extra Features") or to specific Manuals available in $DKITROOT/doc/Manuals/.

© STMicroelectronics - Reproduction and Communication of this document is strictly prohibited unless specifically authorized in writing by STMicroelectronics

WARNING: This design kit has been developed for Cadence Design Framework II version 5.1 (SunOS5.8). Therefore it is strongly recommended to be used with this Cadence release.

1.2 Document description

This document defines the structure of the Design Kit and gives the use instructions. It will help the designer to know what is available, where the data could be found and how they can be used as efficiently as possible. It defines the general rules applied to our Design Kits.

This document covers the specificity of the Design Kit versus the Cadence Design Environment. Please refer to your Cadence documentation to get explanations about the standard Cadence environment.

WARNING: This user guide describes in a general manner the 65nm Design Kits and gives some examples taken from the DK_cmos065lpgp_7m4x0y2z_50A option.

© STMicroelectronics - Reproduction and Communication of this document is strictly prohibited unless specifically authorized in writing by STMicroelectronics

2 - DESIGN KIT MANAGEMENT

2.1 Naming convention for cmos065 Design Kit

Different options exist in the cmos065 process.
Some of them cannot be used simultaneously, and are provided in different Design Kit. The product name of these Design Kits leads to the knowledge of these options.
For exemple:DK_cmos065lpgp_7m4x0y2z_50A28A : It proposes metal 1 up to metal7 (->7m) , mos double oxyde have either 50A gate oxyde (->50A) or 28A gate oxide (->28A). lpgp means that the LP GP process capability is enabled..
Note 1: the OD2 options are exclusive. It is possible to have OD2_18 and OD2_25 devices available in a same Design Kit, but it is not allowed to use these 2 options on a single chip.

Note 2 : Starting with revB of the DRM, the LPGP (CMOS065_LP and CMOS065_GP dual core oxide) process capability is enabled. LP and LPGP process features are availabe in the Design Kit but it is not allowed to use low Vt LP and LPGP process features on the same chip.

Indeed, up to DRM revA, two different DRMs are available: one specific to GP, the other one specific to LP. Consequently, up to releases 1.0 included, GP and LP common design kit products were delivered as separate options.

Naming convention :

lp,gp,lpgp : gate oxyde for MOS simple oxyde

m : total number of metal levels

x : numbers of thin metal

y : numbers of intermediate metal

z: numbers of thick metal

xxA : gate oxyde for MOS double oxyde

© STMicroelectronics - Reproduction and Communication of this document is strictly prohibited unless specifically authorized in writing by STMicroelectronics

2.2 The cmos065 Design Kit libraries

This DK is intended to be used with **Unicad2.4** (on **Opus** 5.1) and Artist simulation environment.

2.2.1 Introduction

This chapter presents the device libraries provided in the cmos065 Design Kit. The cmos065, the analogLib, the basic and the STlib libraries must be used with the Design Kit environment.

- **The analogLib library**

This library is proposed within the Cadence Framework. It contains extra devices and symbols which are technology independent. For more information about analogLib please refer to the Cadence documentation.

To get it in your library manager path, please update your "cds.lib" file with:
DEFINE analogLib $CDS_INSDIR/tools/dfII/etc/cdslib/artist/analogLib

If Eldo is used , the analogLib from AMS is automatically loaded and appears in the library manager.

- **The STlib library**

This library along with its related files are managed by the Design Kit environment. The aim of STlib library is to provide the user with a front end technology independent library (no layout provided) suited for simulation purposes and which completes the Cadence analogLib library. For further details, please refer to $DKITROOT/doc/Manuals/DK_STlib_doc.pdf.

- **The basic library**

This library is proposed within the Cadence Framework. It contains extra devices and symbols which are technology independent, such as pins or supplies. For more information about basic library, please refer to the Cadence documentation.

By default (neither Eldo nor ADS are used), the basic Lib from Cadence is loaded in the library manager.
If Eldo (Mentor Graphics) is used, the basic Lib from AMS is loaded.
If ADS (Agilent) is used , the basic Lib from ADS is loaded.

© STMicroelectronics - Reproduction and Communication of this document is strictly prohibited unless specifically authorized in writing by STMicroelectronics

If Eldo and ADS are used together, the user has the responsibility to select the correct library path by modifying the "cds.lib" file.

❑ The cmos065 library

Two parts can be defined in this library.

- Process part (means that the techfile has been compiled in the cmos065 library)

- Devices part (devices are included in the cmos065 library)

☞ Process part

This library contains technological references, layers, and symbolics.

☞ Devices part

This library provided within the cmos065 Design Kit contains the devices available in the cmos065 core process. The symbols are compatible with the Cadence template libraries in terms of graphics, labels and pins position. The cells proposed in this library are compatible with the following features:

❑ Optional libraries : cmos065_a, cmos065_rf

These libraries are available in the Design Kit, depending on the supported option.

See sections 2.2.4, 2.2.5 for further details.

© STMicroelectronics - Reproduction and Communication of this document is strictly prohibited unless specifically authorized in writing by STMicroelectronics

2.2.2 cmos065 library: devices part

❑ **MOS transistors**

-Naming convention : <TYPE><VT><OX_ID>[variant]

The naming convention defines the type of the transistors in term of family (n or p), and performance (various VT) etc... with this following syntax:

<TYPE>= n : nmos transistor

<TYPE>= p : pmos transistor

<VT>= svt : standard Vt

<VT>= hvt : high Vt

<VT>= lvt : low Vt

<VT>= dr : drift mos

<OX_ID>= lp,gp, double oxyde MOS (50A/2V5 or 28A/1V8)

[VARIANT]= rpo : for IO mos. with rpo layer.

[VARIANT]= rponoldd : for IO mos: ESD clamp

[VARIANT]= pgsp, pgdp, pdsp, pddp, pusp, pudp...SRAM bitcell MOS

[VARIANT] = dram

Examples: nsvtgp, nsvtlp, nsvt25, ndr25

☞ **Thin Oxide GP MOSFET**

Device	Device name in cmos065 library	CDF type	Pcell	Pins	Comment
Simple oxide GP NMOS 1.3nm SVT	nsvtgp	nmos	yes	d g s b	
Simple oxide GP PMOS 1.3nm SVT	psvtgp	pmos	yes	d g s b	
Simple oxide GP NMOS 1.3nm HVT	nhvtgp	nmos	yes	d g s b	
Simple oxide GP PMOS 1.3nm HVT	phvtgp	pmos	yes	d g s b	

© STMicroelectronics - Reproduction and Communication of this document is strictly prohibited unless specifically authorized in writing by STMicroelectronics

Simple oxide GP NMOS 1.3nm SVT unsilicided	nsvtgprpo	nmosrpo	no	d g s b	
Simple oxide GP PMOS 1.3nm SVT unsilicided	psvtgprpo	pmosrpo	no	d g s b	
Simple oxide GP NMOS 1.3nm HVT unsilicided	nhvtgprpo	nmosrpo	no	d g s b	
Simple oxide GP PMOS 1.3nm HVT unsilicided	phvtgprpo	pmosrpo	no	d g s b	
SRAM MOSFET (cell sizes)					
GP SRAM NMOS HVT (0.525um2 cell)	nhvtgppgsp, nhvtgppdsp	nmos	no	d g s b	no more supprted : model removed
GP SRAM NMOS HVT (0.620um2 cell)	nhvtgppgdp, nhvtgppddp nhvtgppdsp620, nhvtgppgsp620	nmos	no	d g s b	model available
GP SRAM PMOS HVT (0.525um2 cell)	phvtgppusp	pmos	no	d g s b	no more supprted : model removed
GP SRAM PMOS HVT (0.620um2 cell)	phvgptpudp, phvtgppusp620	pmos	no	d g s b	model available
Single GP SRAM NMOS SVT (0.525um2 cell)	nsvtgppgsp, nsvtgppdsp, nsvtgppgdp, nsvtgppddp	nmos	no	d g s b	no more supprted : model removed
GP SRAM PMOS SVT (0.525um2 cell)	psvtgppusp, psvgptpudp	pmos	no	d g s b	no more supprted : model removed

© STMicroelectronics - Reproduction and Communication of this document is strictly prohibited unless specifically authorized in writing by STMicroelectronics

☞ **Thin Oxide LP MOSFETS**

Device	Device name in cmos065 library	CDF type	Pcell	Pins	Comment
Simple oxide LP NMOS 1.3nm SVT	nsvtlp	nmos	yes	d g s b	
Simple oxide LP PMOS 1.3nm SVT	psvtlp	pmos	yes	d g s b	
Simple oxide LP NMOS 1.3nm HVT	nhvtlp	nmos	yes	d g s b	
Simple oxide LP PMOS 1.3nm HVT	phvtlp	pmos	yes	d g s b	
Simple oxide LP NMOS 1.3nm LVT	nlvtlp	nmos	yes	d g s b	allowed in LPGP process by DRM revE
Simple oxide LP PMOS 1.3nm LVT	plvtlp	pmos	yes	d g s b	allowed in LPGP process by DRM revE
Simple oxide LP NMOS 1.3nm SVT unsilicided	nsvtlprpo	nmosrpo	no	d g s b	
Simple oxide LP PMOS 1.3nm SVT unsilicided	psvtlprpo	pmosrpo	no	d g s b	
Simple oxide LP NMOS 1.3nm HVT unsilicided	nhvtlprpo	nmosrpo	no	d g s b	
Simple oxide LP PMOS 1.3nm HVT unsilicided	phvtlprpo	pmosrpo	no	d g s b	
LP NMOS 1.8nm 1.2V, Native Vt	nnvtlp	nmos	yes	d g s b	no model
SRAM MOSFET (cell sizes)					

© STMicroelectronics - Reproduction and Communication of this document is strictly prohibited unless specifically authorized in writing by STMicroelectronics

LP SRAM NMOS HVT (0.525um2 cell)	nhvtlppgsp, nhvtlppdsp, nhvtlppgdp, nhvtlppddp	nmos	no	d g s b	
LP SRAM PMOS HVT (0.525um2 cell)	phvtlppusp, phvtlppudp	pmos	no	d g s b	
LP SRAM NMOS SVT (0.525um2 cell)	nsvtlppgsp, nsvtlppdsp, nsvtlppgdp, nsvtlppddp	nmos	no	d g s b	
LP SRAM PMOS SVT (0.525um2 cell)	psvtlppusp, psvtlppudp	pmos	no	d g s b	
LP SRAM NMOS HVT (0.560um2 cell)	nhvtlppgsp560, nhvtlppdsp560	nmos	no	d g s b	no model
LP SRAM PMOS HVT (0.560um2 cell)	phvtlppusp560	pmos	no	d g s b	no model
LP SRAM NMOS SVT (0.560um2 cell)	nsvtlppgsp560, nsvtlppdsp560	nmos	no	d g s b	no model
LP SRAM PMOS SVT (0.560um2 cell)	psvtlppusp560	pmos	no	d g s b	no model
LP SRAM NMOS HVT (0.620um2 cell)	nhvtlppgsp620, nhvtlppdsp620	nmos	no	d g s b	
LP SRAM PMOS HVT (0.620um2 cell)	phvtlppusp620	pmos	no	d g s b	
LP SRAM NMOS SVT (0.620um2 cell)	nsvtlppgsp620, nsvtlppdsp620	nmos	no	d g s b	
LP SRAM PMOS SVT (0.620um2 cell)	psvtlppusp620	pmos	no	d g s b	
LP SRAM NMOS HVT (0.670um2 cell)	nhvtlppgsp670, nhvtlppdsp670	nmos	no	d g s b	no model
LP SRAM PMOS HVT (0.670um2 cell)	phvtlppusp670	pmos	no	d g s b	no model
LP SRAM NMOS SVT (0.670um2 cell)	nsvtlppgsp670, nsvtlppdsp670	nmos	no	d g s b	no model

© STMicroelectronics - Reproduction and Communication of this document is strictly prohibited unless specifically authorized in writing by STMicroelectronics

LP SRAM PMOS SVT (0.670um2 cell)	psvtlppusp670	pmos	no	d g s b	no model

☞ **Thick Oxide MOSFET**

Device	Device name in cmos065 library	CDF type	Pcell	Pins	Comment
OD18 NMOS 2.8nm 1.8V SVT	nsvt18	nmos	yes	d g s b	
OD18 PMOS 2.8nm 1.8V SVT	psvt18	pmos	yes	d g s b	
OD18 NMOS 2.8nm 1.8V SVT	nsvt18rpo	nmosrpo	no	d g s b	
OD18 PMOS 2.8nm 1.8V SVT	psvt18rpo	pmosrpo	no	d g s b	
OD18 NMOS-no-LDD 2.8nm unsilicided	nsvt18rponoldd	nmos-ponoldd	no	d g s b	
OD18 NMOS 2.8nm 1.8V Native Vt	nnvt18	nmos	yes	d g s b	Not yet fully supported : no model
OD25 NMOS 5.0nm 2.5V SVT	nsvt25	nmos	yes	d g s b	
OD25 PMOS 5.0nm 2.5V SVT	psvt25	pmos	yes	d g s b	
OD25 NMOS 5.0nm 2.5V SVT unsilicided	nsvt25rpo	nmosrpo	no	d g s b	
OD25 PMOS 5.0nm 2.5V SVT unsilicided	psvt25rpo	pmosrpo	no	d g s b	
OD25 NMOS-no-LDD 5.0nm unsilicided	nsvt25rponoldd	nmosr-ponoldd	no	d g s b	
OD25 NMOS 5.0nm 2.5V Native Vt	nnvt25	nmos	yes	d g s b	Not yet fully supported: no model

© STMicroelectronics - Reproduction and Communication of this document is strictly prohibited unless specifically authorized in writing by STMicroelectronics

Drift MOSFET					
OD25 NMOS-drift 5.0nm for OTP	ndr25otp	nmos	no	d g s b	
OD25 NMOS-drift 5.0nm	ndr25	nmos	yes	d g s b	
OD25 PMOS-drift 5.0nm	pdr25	pmos	yes	d g s b sub	
OD18 NMOS-drift 2.8 nm	ndr18	nmos	yes	d g s b	Not yet fully supported : no model
OD18 PMOS-drift 2.8nm	pdr18	pdrift	yes	d g s sb sub	Not yet fully supported : no model
OD25 NMOS-drift 2.8nm for OTP	ndr18otp	nmos	no	d g s b	
DRAM MOSFET					
OD25 NMOS 2,5V SVT	nsvt25dram	nmos	no	d g s b	Application specific (DRAM)
OD25 NMOS 2,5V LVT	nlvt25dram	nmos	no	d g s b	Application specific (DRAM) : no model

- **Passive and other devices**

☞ resistors: R<LAYERS>[CONTEXT]

- poly resistors : rnpo, rnpoi, rnporpo, rppoi, rpporpo, rhiporpo
- active resistors : rpodrpo, rpporpo
- metal resistors : rm1, rmx (with parameter metal whose value can be 1, 2, 3, 4 ,5 are thin metal layer resistors), rmy (with parameter metal whose value can be 6, 7, 8 are intermediate metal layer resistors), rmz (with parameter metal whose value can be

© STMicroelectronics - Reproduction and Communication of this document is strictly prohibited unless specifically authorized in writing by STMicroelectronics

6,7,8,9,10 are thick metal layer resistors)

- alucap resistor: rap

Device	Device name in cmos065 library	CDF type	Pcell	Pins	Comment
N+ Poly silicided	rnpo	resistor3	yes	plus minus b	
N+ Poly silicided intrinsic	rnpoi	resWithoutContact	no	plus minus	
P+ OD non-siliN+ Poly silicided	rpodrpo	resistor3	yes	plus minus b	
P+ Poly non-silicided	rpporpo	resistor3	yes	plus minus b	
N+ Poly non-silicided	rnporpo	resistor3	yes	plus minus b	
N+ OD non-silicided	rnodrpo	resistor3	yes	plus minus b	Not supported, reserved
P+ Poly silicided	rppo	resistor3	yes	plus minus b	Not supported, reserved
P+ Poly silicided intrinsic	rppoi	resWithoutContact	no	plus minus	
High-resistance P+ Poly	rhiporpo	resistor	yes	plus minus b	
Poly Fuse	rnpofuse	resistor	no	plus minus	Application specific, no model
metal1 resistor	rm1	resistor	yes	plus minus	absolute min length value to be used to allow setting different names to the same wire
thin metal resistor	rmx	resistor	yes	plus minus	
intermediate metal resistor	rmy	resistor	yes	plus minus	
thick metal resistor	rmz	resistor	yes	plus minus	
Alucap resistor	rap	resistor	yes	plus minus	

© STMicroelectronics - Reproduction and Communication of this document is strictly prohibited unless specifically authorized in writing by STMicroelectronics

NOTE: the support of poly fuse may require an additional cell in cmos065 library.

- ☞ diodes : D<MOS> , or -for other diodes- D<PPLATE><NPLATE> <MOS> is naming convention, PPLATE is the P layer.
- dnsvtgp/lp (N+/Pwell), dpsvtgp/lp(P+/Pwell), dnhvtlp, dphvtlp, dnlvtlp, dplvtlp, follows the same naming convention than for MOS. (svt for standard Vt, hvt for high Vt lp/gp etc...)
- dnwps is Nwell psubstrat
- ddnwpw is Pwell/Niso
- ddnwps is Niso/Psubstrat
- dnwpw is Nwell/Pwell

Device	Device name in cmos065 library	CDF type	Pcell	Pins	Comment
N+/PWELL GP SVT	dnsvtgp	diode	yes	plus minus	
P+/NWELL GP SVT	dpsvtgp	diode	yes	plus minus	
N+/PWELL GP HVT	dnhvtgp	diode	yes	plus minus	
P+/NWELL GP HVT	dphvtgp	diode	yes	plus minus	
N+/PWELL LP SVT	dnsvtlp	diode	yes	plus minus	
P+/NWELL LP SVT	dpsvtlp	diode	yes	plus minus	
N+/PWELL LP HVT	dnhvtlp	diode	yes	plus minus	
P+/NWELL LP HVT	dphvtlp	diode	yes	plus minus	
N+/PWELL LP LVT	dnlvtlp	diode	yes	plus minus	not allowed in LPGP process
P+/NWELL LP LVT	dplvtlp	diode	yes	plus minus	not allowed in LPGP process
N+/PWELL 5.0nm SVT	dnsvt25	diode	yes	plus minus	

© STMicroelectronics - Reproduction and Communication of this document is strictly prohibited unless specifically authorized in writing by STMicroelectronics

P+/NWELL 5.0 nm SVT	dpsvt25	diode	yes	plus minus	
N+/PWELL 2.8nm SVT	dnsvt18	diode	yes	plus minus	
P+/NWELL 2.8nm SVT	dpsvt18	diode	yes	plus minus	
Gated diodes					
P+/NWWELL 5.0nm gated diode	dgpsvt25	gdiode	yes	plus minus	gated diode required for IO design
N+/PWWELL 5.0nm gated diode	dgnsvt25	gdiode	yes	plus minus	gated diode required for IO design
P+/NWWELL 2.8nm gated diode	dgpsvt18	gdiode	yes	plus minus	gated diode required for IO design
N+/PWWELL 2.8nm gated diode	dgnsvt18	gdiode	yes	plus minus	gated diode required for IO design
Buried diodes					
NWELL/Psubstrate	dnwps	diode	no	plus minus	For simulation only (pre and post layout): See table below
Deep NWELL/Psub-strate	ddnwps	diode	no	plus minus	For simulation only (pre and post layout): See table below
PWELL/Deep NWELL	ddnwpw	diode	no	plus minus	
DRAM diodes					
N+/PWELL 5.0nm SVT (CELLIMP)	dnsvt25dram	diode	no	plus minus	Application specific (DRAM), no model

The table below explains how buried diodes are extracted and/or compared depending on the LVS flow.

	Standard LVS	**LVS for PLS**

© STMicroelectronics - Reproduction and Communication of this document is strictly prohibited unless specifically authorized in writing by STMicroelectronics

Nwell to Psubstrat diode **DNWPS** (appears only in basic Nwell)	Not Extracted => Not compared	Extracted => Compared Symbol is not mandatory in schematic
Deep Nwell to Psubstrat diode **DDNWPS** (appears only in Deep Nwell)	Not Extracted => Not compared	Extracted => Compared Symbol is not mandatory in schematic
Deep Nwell to Pwell Iso diode **DDNWPW** (appears only in Deep Nwell)	Extracted => Compared Symbol is mandatory in schematic	Extracted => Compared Symbol is mandatory in schematic

☞ capacitor:

Poly capacitors: CPO<OX_ID><WELL>

Metal Capacitors : - plate capacitors: C<TOP><BOTTOM>

- fringe capacitors: CFR<TOP><BOTTOM>

Device	Device name in cmos065 library	CDF type	Pcell	Pins	Comment
N+ Poly /NWELL GP	cpogpnw	cpolynwell	no	plus minus b	natural device, kept for compatibility only (2)
N+ Poly /NWELL LP	cpolpnw	cpolynwell	yes	plus minus b	for general purpose or Antifuse (2) : Verliog-A model
N+ Poly /NWELL LP	cpolppw	cpolypwell	no	plus minus b	for general purpose (2) : Verilog-A model

© STMicroelectronics - Reproduction and Communication of this document is strictly prohibited unless specifically authorized in writing by STMicroelectronics

N+ Poly/5.0nm Gox/NWELL	cpo25nw	cpolynwell	yes	plus minus b	
P+ Poly/5.0nm Gox/PWELL	cpo25pw	cpolypwell	yes	plus minus b	
N+ Poly/2.8nm Gox/NWELL	cpo18nw	cpolynwell	yes	plus minus b	
P+ Poly/2.8nm Gox/PWELL	cpo18pw	cpolypwell	yes	plus minus b	Not yet fully supported: no model
Monolayer metal fringe capacitor	cfrm1	cElemFringe	yes	plus, minus	Metal1 elementary fringe capacitor (1)
	cfrmx	cElemFringe	yes	plus, minus	Thin Metal elementary fringe capacitor(1)
	cfrmy	cElemFringe	yes	plus, minus	intermediate Metal elementary fringe capacitor(1)
	cfrmz	cElemFringe	yes	plus, minus	Thick Metal elementary fringe capacitor(1)

© STMicroelectronics - Reproduction and Communication of this document is strictly prohibited unless specifically authorized in writing by STMicroelectronics

Stacked metal fringe capacitor	cfrm1m5shx	cfringe	yes	a_po b_od shod shop sub	Stacked metal fringe capacitor with thin metal shield (5 pins) (1)
	cfrm1m5shy	cfringe	yes	a_po b_od shod shop sub	Stacked metal fringe capacitor with intermediate metal shield (5 pins) (1)
	cfrm1m5shz	cfringe	yes	a_po b_od shod shop sub	Stacked metal fringe capacitor with thick metal shield (5 pins)
	cfrm1m5shx nosub	cfringe	yes	a_po b_od shod shop sub	Stacked metal fringe capacitor with thin metal shield (4 pins) (1)
	cfrm1m5shy nosub	cfringe	yes	a_po b_od shod shop sub	Stacked metal fringe capacitor with intermediate metal shield (4 pins) (1)
	cfrm1m5shz nosub	cfringe	yes	a_po b_od shod shop sub	Stacked metal fringe capacitor with thick metal shield (4 pins) (1)
Striped stacked metal capacitor	cmstrstk	cstripe	yes	plus, minus	
2 layer metal plate capacitor	cmimj (i =1,x,y,z and j = x,y,z)	cNoBulkVar	yes	plus, minus	(1)

© STMicroelectronics - Reproduction and Communication of this document is strictly prohibited unless specifically authorized in writing by STMicroelectronics

High linearity MIM capacitor for 4 thin , 0 inter-mediate metal process option	cmimmk4x0y	cmim	yes	plus minus b	no model
High linearity MIM capacitor for 4 thin , 1 inter-mediate metal process option	cmimmk4x1y	cmim	yes	plus minus b	no model
High linearity MIM capacitor (without substrate pin) for 4 thin , 0 intermediate metal process option	cmimmk4x0y	cmimnosub	yes	plus minus	no model
High linearity MIM capacitor (without substrate pin) for 4 thin , 1 intermediate metal process option	cmimmk4x0y	cmimnosub	yes	plus minus	no model
DRAM capacitor	ce1e2	cNoBulk	no	plus minus	Application spe-cific (DRAM) : no model

(1) Metal capacitors

They are realized with metal layers are of two types: fringes (lateral coupling effect) and plates or stripes (vertical effect). These capacitors can be:

© STMicroelectronics - Reproduction and Communication of this document is strictly prohibited unless specifically authorized in writing by STMicroelectronics

- elementary (two neighboring fingers in the same metal layer for fringe, plates (or stripes) in two consecutive metal layers for plate) (Cells for elementary metal plate (or stripe) capacitors have two pins). In this case, the corresponding model (used for simulation from schematic database) is basic; PLS flow computes all capacitors inside the device (lpe flag removes all capacitors from simulation model, when simulation from layout database)
- or stacked; in this case, the device is considered as a black box: the simulation model (both from schematic and layout database) is accurate, and PLS flow does not compute capacitors inside the device (stops at device boundary)

(2) Poly/Well capacitors

Poly over well capacitors can exist in both simple and double oxide flavours. Starting with DK C065 4.0, simple oxide poly over well capacitors are supported in LP only .
Simple oxide poly/well capacitors in GP process option are considered as “natural” devices. The corresponding cells in cmos065 library (cpogpnw and cpogppw) are stored in category “DoNotUse”.

Concerning simple oxide poly/well capacitors in LP process option:
- cpolpnw (simple oxide N+ Poly over Nwell capacitor) is used for general design purpose as well as in the antifuse cell (specific application):

  – In the case of the antifuse application cpolpnw does not require the presence of (MKR, VAR) (layout view)

  – For general purpose application the layer (MKR, VAR) is mandatory for the layout of cpolpnw to be correctly built and processed at mask data preparation level.

These two different situations are supported in LVS.

- cpolppw is for general application only :the layer (MKR, VAR) is mandatory

☞ natural bipolar: <TYPE><AREA><SILICIDE>

– npniso25 is N+ / Pwell / Niso fixed geometry

– npniso4 is N+ / Pwell / Niso fixed geometry

– pnps25 is P+ / Nwell / Psubstrat fixed geometry

– pnps4 is P+ / Nwell / Psubstrat fixed geometry

© STMicroelectronics - Reproduction and Communication of this document is strictly prohibited unless specifically authorized in writing by STMicroelectronics

Device	Device name in cmos065 library	CDF type	Pcell	Pins	Comment
N+/PWELL/ Deep NWELL	npniso4, npniso25	bipolar	fixed layout	c e b sub	
P+/NWELL/ Psub	pnps4, pnps25	bipolar	fixed layout	c e b	

❏ **Test points**

Device	Device name in cmos065 library	CDF type	Pcell	Pins	Comment
ebeamprobe	ebeamprobe	Testpoint	yes	probe	
microprobe	microprobe	Testpoint	yes	probe	
sealring	sealring6m4x0y1z sealring7m4x0y2z sealring7m4x1y1z sealring8m5x0y2z sealring9m6x0y2z	sealring	yes	none	for layout finishing
pg text	pgtext	pgtext	yes	none	for layout finishing
pg text DRC clean	pgtext_drc_clean	pgtext_drc_clean	yes	none	for layout finishing
ST logos	STLogo_2003 STLogo_2004 STLogo_2005 STLogo_2006	no cdf	layout fixed	none	for layout finishing

For further details concerning Layout Finishing, please refer to the chapter 5 of this document..

© STMicroelectronics - Reproduction and Communication of this document is strictly prohibited unless specifically authorized in writing by STMicroelectronics

2.2.3 cmos065 library: process part

❑ **Opus techfile for library creation**

Within Cadence FrameWorkII, a techfile is attached to each user's library. This library techfile contains both process data (layers definition, layers properties, etc...) and user's library specific data. Whenever the user wants to create a new library (or to move an existing design into the Design Kit environment), a techfile has to be specified.

❑ **Creating a user Library**

This chapter describes how to create a user library attached to the cmos090gp_6M1T_50A Design Kit product.

The aim of the Design Kit product is both:

- to ensure that all Design Kit users use consistent data (all related to up to date cmos090gp_6M1T_50A process)
- and to ensure that all Design Kit users libraries are automatically updated in case a new release of the Design Kit is installed and chosen by the user.

In order to create a library attached to Design Kit, the user can use two different Cadence menus:

- Either from the ***Library Manager*** form,
  . click on ***File->New->Lib***
  . the form ***New Library*** is opened: enter library name (ex: myLib) and directory full path name, click on OK
  . the form ***Technology File For New Library*** is opened, select the option ***Attach to an existing techfile***, click on OK
  . the form ***Attach Design Library to Technology File***, select in cyclic field the library ***cmos065*** , click on OK.

© STMicroelectronics - Reproduction and Communication of this document is strictly prohibited unless specifically authorized in writing by STMicroelectronics

– Or in the ***CIW*** ,
. click on ***File->New->Lib***
. the form ***New Library*** is opened:
. enter library name (ex: myLib) and directory full path name,
. select the option ***Attach to an existing techfile***, click on OK
. the form ***Attach Design Library to Technology File***, select in cyclic field the library ***cmos065*** , click on OK.

Any user created design library should be attached to the cmos065 library.

❑ Symbolic contacts

☞ CDS Vias : New and old contacts

New cdsVias are defined by inserting/adding an underscore in their name. They have been introduced in release 4.0 of the DK to take advantadge of more agressive rules and of Wide OD rules.

In addition of vertical stitching vias (their name contains string "_H"), another set of symbolics (their name contains string "_V") has been introduced in release 4.0 to allow Vertical direction stitching.

Those contacts are supported by vcr, ccar and wire editor.They appear in the Create->Contact cyclic. See the first column of the table below.

Obsolete cdsVia device since 3.1 and 4.0 have been integrated back in the technology file as a new device class: obsolete_cdsViaDevice_3_1 and obsolete_cdsViaDevice_4_0. They don t appear in the Create->Device cyclic because of the layout view (must be symbolic). They can be instanciated by Create->Instance.

☞ Sycontacts : New and old contacts

New Sycontacts are defined by inserting/adding an underscore in their name. They appear in the Create->Contact cyclic. See the second column of the table below.

© STMicroelectronics - Reproduction and Communication of this document is strictly prohibited unless specifically authorized in writing by STMicroelectronics

Old SyContacts to OD have been moved to a new device class: obsolete_syContact_3_3 . They appear in the Create->Device cyclic.

N.B.: From Cadence OPUS 5.1.41.USR1, the Create Device command on the Layout Editor menu is available only for creating Quick Cells in Virtuoso Layout Editor Turbo and Virtuoso XL Layout Editor. Thus, if you need to place one of the obsolete contacts, either type leHiCreateSymDev() in the CIW input line to bring up the Create Device form or use the Create Instance command.

Device class/ view/ code/ CDF avail.	**cdsViaDevice layout standard CDF**	**syContact symbolic (customized) CDF**	**Obsolete_cdsViaDevice_3_1 layout _NA_ CDF**	**Obsolete_cdsViaDevice_4_0 layout _NA_ CDF**	**Obsolete_syContact_3_3 symbolic _NA_ CDF**
OD contacts		NTAP_ PTAP_ M1__NOD M1__POD M1_NW M1__OD	M1_OD		NTAP PTAP M1_NOD M1_POD M1_NW
Poly contacts	M1__PO			M1_PO	

© STMicroelectronics - Reproduction and Communication of this document is strictly prohibited unless specifically authorized in writing by STMicroelectronics

Device class/ view/ code/ CDF avail.	cdsViaDevice layout standard CDF	syContact symbolic (customized) CDF	Obsolete_cdsViaDevice_3_1 layout _NA_ CDF	Obsolete_cdsViaDevice_4_0 layout _NA_ CDF	Obsolete_syContact_3_3 symbolic _NA_ CDF
Metal contacts	M2X_M1 M2X_M1_H M2X_M1_V MjX_MiX MjX_MiX_H MjX_MiX_V MjY_MiX MjY_MiX_H MjY_MiX_V MjY_MiY MjY_MiY_H MjY_MiY_V MjZ__MiX MjZ__MiX_H MjZ__MiX_V MjZ__MiY MjZ__MiY_H MjZ__MiY_V MjZ__MiZ MjZ__MiZ_H MjZ__MiZ_V		MjZ_MiX MjZ_MiX_H MjZ_MiY MjZ_MiY_H MjZ_MiZ MjZ_MiZ_H		
AP and MIM contacts	AP__MiZ MjZ__BOTMIM MjZ__MKTOPMIM			AP_MiZ MjZ_BOTMIM MjZ_MKTOPMIM	
Menu Create->Contact	yes	yes	no	no	no
Menu Create->Device	no	no	no	no	yes

© STMicroelectronics - Reproduction and Communication of this document is strictly prohibited unless specifically authorized in writing by STMicroelectronics

Device class/ view/ code/ CDF avail.	cdsViaDevice layout standard CDF	syContact symbolic (customized) CDF	Obsolete_cdsViaDevice_3_1 layout _NA_ CDF	Obsolete_cdsViaDevice_4_0 layout _NA_ CDF	Obsolete_syContact_3_3 symbolic _NA_ CDF
Menu Create->Instance	yes	yes	yes	yes	yes

All ICC rules supported by DK product are included in Cadence techfile (see: controls section)

❑ Symbolic pin

Following symbolic pins are present in common technology file. In option specific common technology kit some of them will be invisible according to the context.

Layer type	Symbolic pin
poly	PO_T
metal1	M1_T
thin metal	M2X_T
	M3X_T
	M4X_T
	M5X_T
	M6X_T
	M7X_T
	M8X_T
intermediate metal	M6Y_T
	M7Y_T
	M8Y_T
	M6Z_T

© STMicroelectronics - Reproduction and Communication of this document is strictly prohibited unless specifically authorized in writing by STMicroelectronics

thick metal	M7Z_T
	M8Z_T
	M9Z_T
	M10Z_T
alucap	AP_T

❑ Multipart paths

Multipart paths are path elements that contain more than one layer. These may include active, an implant, metal and contacts. These elements are also fully "choppable" which means once they are placed the user may select a section of the multipart path and remove (chop) a section of the path away. List multipart paths that are available and purpose/features are noted below.

Mpp Name	Composed from	Description
M1_PPO	M1, CONT, PO, PP	choppable M1 & CO
M1_NPO	M1, CONT, PO, NP	choppable M1 & CO
M1_NW	M1, CONT, PO, NP, NW	M1 connected to NW via CO and OD. Cmplete path with DRC clean NW line ends.
M1_NWRing	M1, CONT, PO, NP, NW	Same as M1_NW, but with flush line ends to abut start and end points; used to create an NW ring
M1_IPW	M1, CONT, PO, NP, NW	M1 connected to NW for isolated PWell regions. Used to create isolation rings (User must draw DNW shape
PPPoly	PO, PP	for more user flexibility
PPPolyGP	PO, PP, (DCO;drawing)	for more user flexibility
NPPPoly	PO, NP	for more user flexibility

© STMicroelectronics - Reproduction and Communication of this document is strictly prohibited unless specifically authorized in writing by STMicroelectronics

Mpp Name	Composed from	Description
NPPolyGP	PO, NP, (DCO;drawing)	for more user flexibility
M2X_M1		(M2; drawing) connection to M1 using (VIA1; drawing)
MjX_MiX	VIAi, Mi, Mj	(Mj;drawing) connection to (Mi; drawing) using (VIAi;drawing)
MjY_MiX	VIAi, Mi, Mj	(Mj;drawingY) connection to (Mi; drawing) using (VIAi;drawingY)
MjY_MiY	VIAi, Mi, Mj	(Mj;drawingY) connection to (Mi; drawingY) using (VIAi;drawingY)
MjZ_MiX	VIAi, Mi, Mj	(Mj;drawingZ) connection to (Mi; drawing) using (VIAi;drawingZ)
MjZ_MiY	VIAi, Mi, Mj	(Mj;drawingZ) connection to (Mi; drawingY) using (VIAi;drawingZ)
MjZ_MiZ	VIAi, Mi, Mj	(Mj;drawingZ) connection to (Mi; drawing) using (VIAi;drawingZ)
AP_MiZ	CB, Mi, AP	(AP;drawing) connection to (Mi; drawingZ) using (CB;drawing)

2.2.4 cmos065_a library

This library contains all MTP cells and HPA (High Performance Analog) MOS :

Device	Device name in cmos065 library	CDF type	Pcell	Pins	Comment
NMOS HPA LP	nhpalp	nmos	yes	d g s b	HPA option

© STMicroelectronics - Reproduction and Communication of this document is strictly prohibited unless specifically authorized in writing by STMicroelectronics

PMOS HPA LP	phpalp	pmos	yes	d g s b	HPA option
Half-silicided PMOS GO2 50A (2.5V) for MTP cell	mtpcell	pmos	yes	d g s b	MTP only
PMOS GO2 50A (2.5V) used in MTP cell	psvt25_mtp	pmos	yes	d g s b	MTP only
Unsilicided PMOS GO2 50A (2.5V) used in MTP cell	psvt25rpo_mtp	pmos	yes	d g s b	MTP only

2.2.5 cmos065_rf library

This library is only available in DK RF. It contains all RF devices, specific to ST (inductors, varactors, MOS RF). See CMOS065 RF part for further details.

© STMicroelectronics - Reproduction and Communication of this document is strictly prohibited unless specifically authorized in writing by STMicroelectronics

2.3 Layer Convention

2.3.1 Introduction

This chapter is written to allow definition of the layer convention to be used to layout cells/ macrocells/designs in the cmos090gp_6M1T_50A design kit.
Note that all implant layers have to be drawn for mos.

2.3.2 Layout Convention

Standard layout design grid is 0.005 micron for all the levels.
For all devices from the first class (refer to DRM), you can find an example of layout with the pcells.

2.3.3 Layers definition

In order to ensure reuse in cmos065 Design Kit environment on an IP designed in the TSMC environment, the GDS2 layer definitions are aligned on TSMC GDS2 specifications.

2.3.4 Layer map table for streamin/out and mask generation

Streamout is used to produce a GDSII format file from an opus Data Base layout file using the provided **Layer-Map-Table**; the command to be run for this purpose is the ***Stream Out*** command in the ***Physical*** sub menu of the ***Translators*** menu in the CIW.

Streamin is used to produce from a GDSII format file, an opus Data Base layout file using the provided **Layer-Map-Table**; the command to be run for this purpose is the ***Stream In*** command in the ***Physical*** sub menu of the ***Translators*** menu in the CIW.

Inside the cmos090gp_6M1T_50A design kit, only one layer table is given:

The cmos065.lmt: is used now for transfer of cells/macrocells between CAD systems and for layout finishing (The gdsII mask and the gdsII CAD is now the same).

© STMicroelectronics - Reproduction and Communication of this document is strictly prohibited unless specifically authorized in writing by STMicroelectronics

2.4 Management Procedures

The Design Kit includes some data such as the simulation models, the technological masks, the verification files, the mask generation tables, etc... These data are managed with a set of procedures that enables the user to set up a link between the Design Kit and the different user procedures.

These management procedures use some table of data, as shown bellow, to link each “key” to a parameter, a file, a directory or a procedure.

```
key type information documentation
process string cmos090gp_6M1T_50A “Process”
```

When the user needs to list the “key” that are defined in a Design Kit, the following commands have to be entered in the Opus or the Unix windows:

```
piGetKeys getShellEnvVar(“DKITROOT”); Opus window
piGetKeys $DKITROOT; Unix Window
```

When the user needs to get the data that have been linked to a “key”, the following commands have to be entered in the Opus or the Unix windows:

```
piGetInfo getShellEnvVar(“DKITROOT”) “process”; Opus Window
piGetInfo $DKITROOT “process”; Unix Window
```

2.5 The Menu DESIGN KIT

An Opus session launched in an account customized for Design Kit use will inherit of the Design Kit environment.

In particular, Design Kit provides for dedicated menus stored in one single "menu tree", which are accessible through the ***Design Kit*** button in the CIW banner.

© STMicroelectronics - Reproduction and Communication of this document is strictly prohibited unless specifically authorized in writing by STMicroelectronics

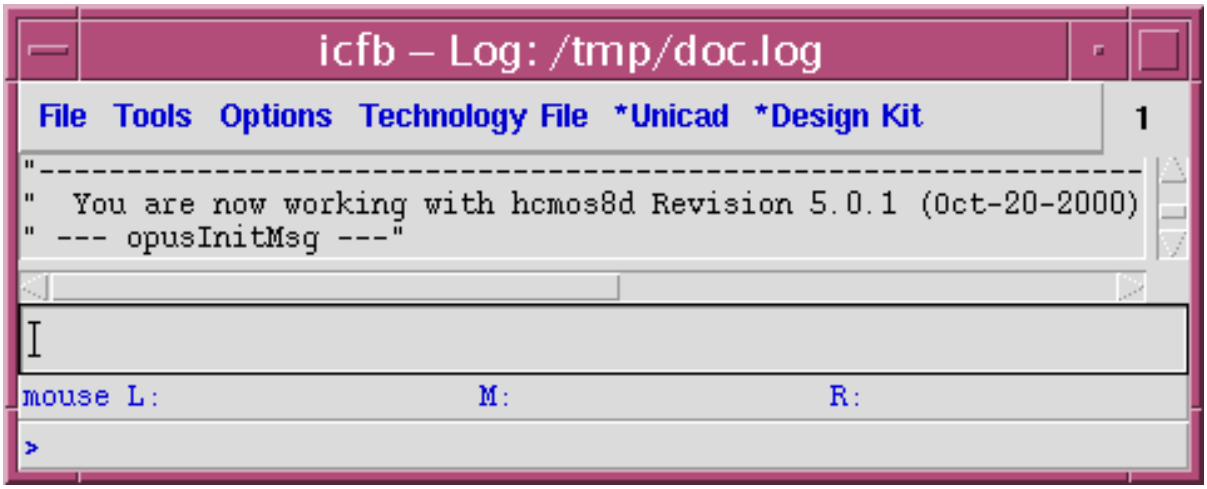


Figure 1: window that presents the design kit menus

The following sub-menus shown in figure 1 are proposed:

- Design Kit Menu:functions related to the Design Kit
- Unicad Menu:configuration of the Unicad environment

Please Note that the usual

- Design-Kit Unix InterfaceVerification Menu
- Mask GenerationMask Menu ARE NO MORE AVAILABLE

Instead dkCust, for calibre use, please consider now Interactive Calibre (menu calibre in the layout window) or calibre -gui in unix world. A batch use of calibre is possible with the -batch option.

Design Kit calibrerun tool can also be used. calibrerun is a unique command to run calibre -gui with the choosen Design Kit Rule File : either drc antennadrc lvs tiling or drc lvs tiling drcMask lvsMask tilingMask.

calibrerun allows to run calibre -gui either in interactive mode or in batch mode.

A *Design Kit menu can be found in the view windows with submenu allowing functions.

© STMicroelectronics - Reproduction and Communication of this document is strictly prohibited unless specifically authorized in writing by STMicroelectronics

3 - MIGRATION PROCEDURES

By default, when migrating an existing design to a newer design kit, schematic and layout (pcell, symoblics, fixed layouts..)views will be kept unchanged.
Nevertheless, the designer can update his old designs and migrate :

- **to the new device parameters** by using the **Design update CDF** procedure
- **to the new version of pcells** (after an impact analysis) by using the **Design update Pcells** procedure.

- to the new DRM rules or to new layers by using dedicated procedures (Wide OD procedure for example)

3.1 Design update CDF procedure

This procedure is available from the CIW: "Design Kit -> Design Update cdf". The following form will show up :

© STMicroelectronics - Reproduction and Communication of this document is strictly prohibited unless specifically authorized in writing by STMicroelectronics

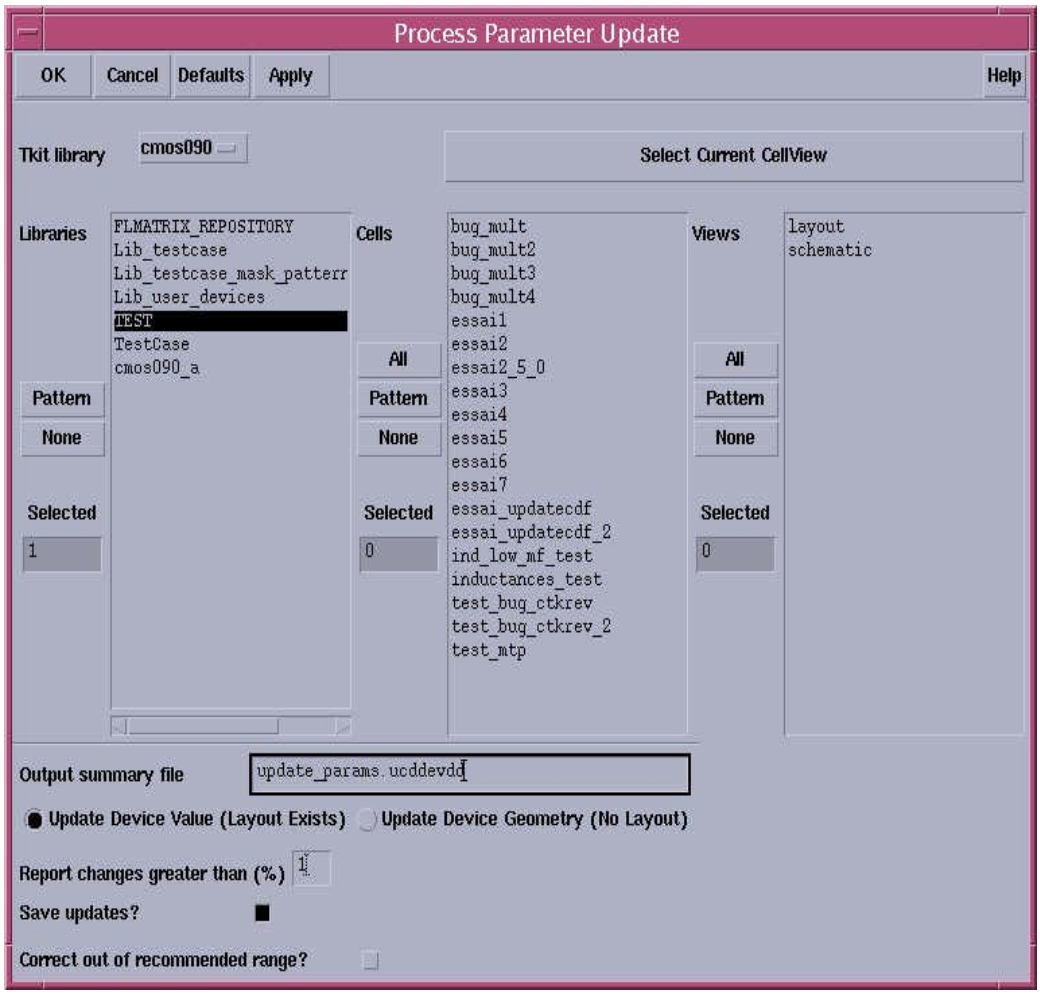


Figure 2: Design Udpate cdf form

- Set the Tkit library cyclic menu to "cmos065"

- Select the library, the cell and the view (schematic or layout) corresponding to the design you want to update

- Select whether the device values (only for resistance of resistors or capacitance of capacitors) should be recalculated and device geometries kept or whether the device geometries should be recalculated (usually when layout does not yet exist).

- Run Update cdf

© STMicroelectronics - Reproduction and Communication of this document is strictly prohibited unless specifically authorized in writing by STMicroelectronics

3.2 Design update Pcells procedure

3.2.0.1 Pcells update approach

The following statements are true only for devices supporting the Design update Pcells procedure:

Pcells feature one unique layout view containing multi-version skill functions : one skill function per version of Design Kit. Indeed, the pcell layout view contains the newest skill function, corresponding to the DK currently in use and also the skill functions corresponding to the pcells of the previous Design Kits.
Each Pcell instance features a hidden tag , called ctkrev parameter. According to this tag, the corresponding skill function is loaded and executed when opening a layout. Such an approach allows compatibility with old designs : pcells keep unchanged when migrating an existing design to a newer design kit.

The Design update Pcells procedure consists in updating the ctkrev parameter of old pcells instanciated in an existing design so that the newest Pcell skill function is loaded and the pcell updated.

Note : This update procedure applies not only to layout views but to also to schematic views of a design. It is necessary for layout XL for example :
- If the Dkit user creates a schematic with the version N of a DK
- When running Layout XL on this schematic opened in the version N+1 of the DK, layout views of DK version N will be used by Layout XL
- To use layout views of the version N+1 of the DK, user must update the schematic database of his design.

3.2.0.2 How to run Design update Pcells procedure?

This procedure is available from the CIW: "Design Kit -> Design Update Pcells". The following form will show up :

© STMicroelectronics - Reproduction and Communication of this document is strictly prohibited unless specifically authorized in writing by STMicroelectronics

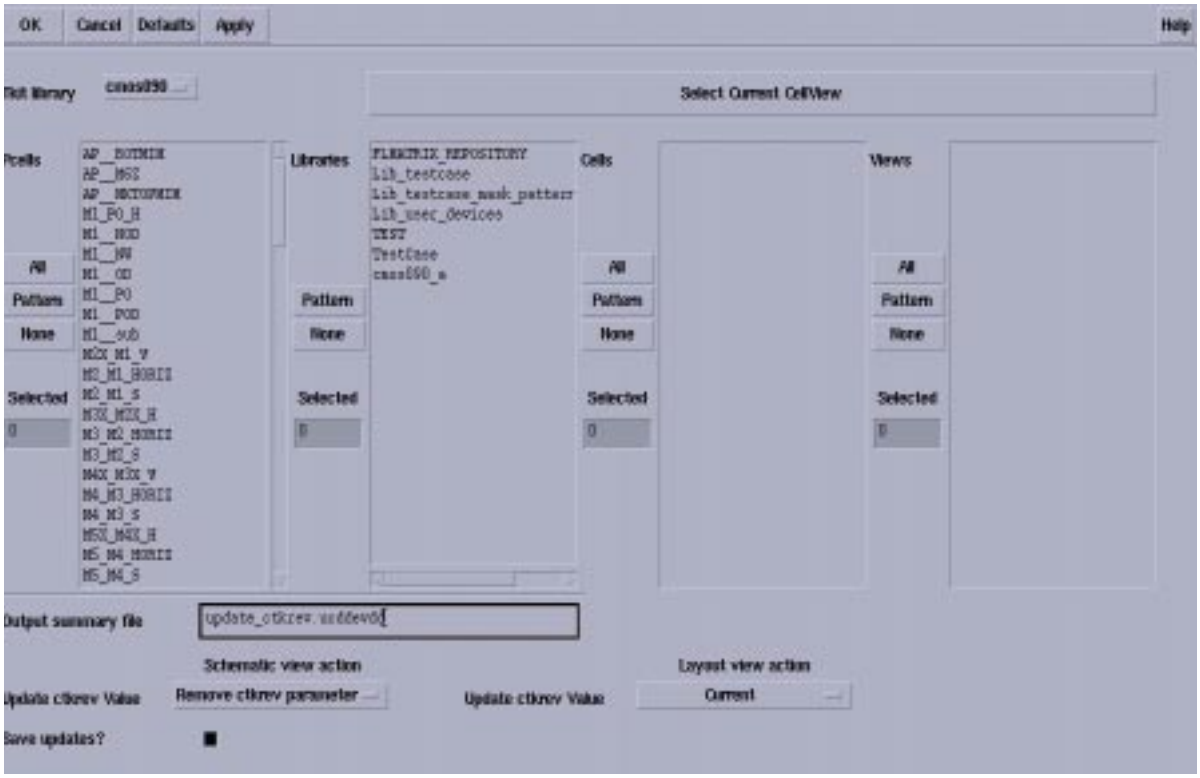


Figure 3: Design Update Pcell form

- Set the Tkit library cyclic menu to "cmos065"

- Select the pcells you want to update. Select all pcells and symbolics if you want to benefit from all updated pcells.

- Select the library, the cell and the view (schematic or layout) corresponding to the design you want to update

- Run Update Pcells

© STMicroelectronics - Reproduction and Communication of this document is strictly prohibited unless specifically authorized in writing by STMicroelectronics

3.3 Wide OD Opus procedure

The main purpose of DRM C065 revD is the update of Wide OD rules to be aligned with TSMC. The following procedure processes old layouts (before DK 4.x) and correct 'wide OD errors' corresponding to the rules updated in DRM revD.
This procedure is available from the CIW: "Design Kit -> Design Update Wide OD". The following form will show up :

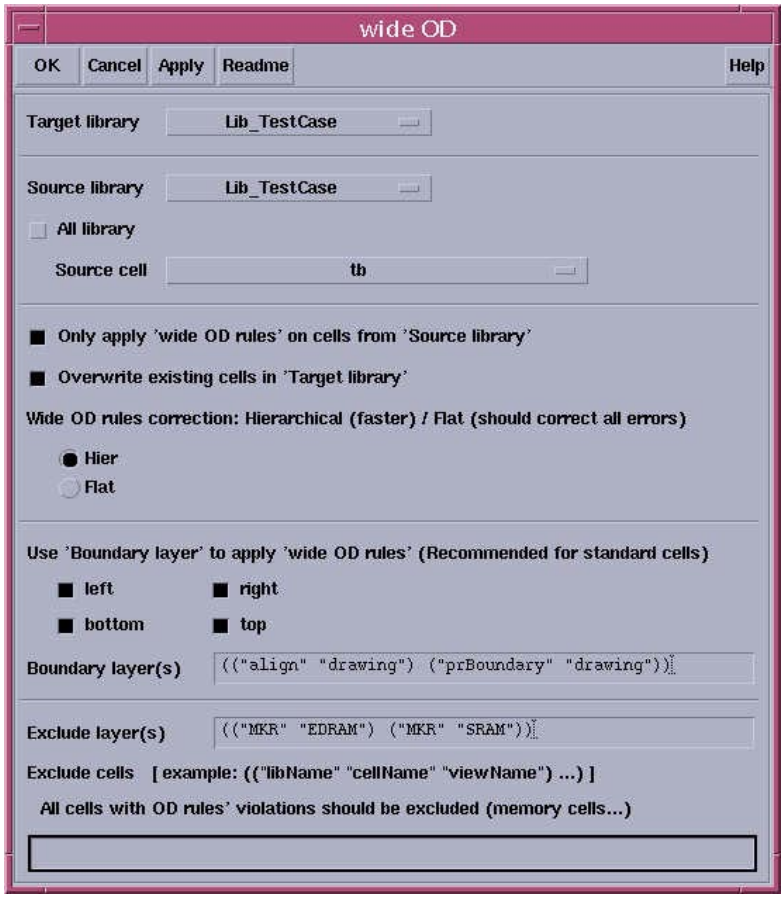


Figure 4: Wide OD form

- **Libraries**
  - Target library : Opus library in which all the 'wide OD' corrected cells will be generated (or modified in place, if same library as Source library)
  - Source library: Can be the same as Target library

© STMicroelectronics - Reproduction and Communication of this document is strictly prohibited unless specifically authorized in writing by STMicroelectronics

- Processed cells: Apply 'wide OD rules' on all cells of the 'Source library, or only on the specified cell, and its instances

❑ Options

- Apply 'wide OD script only on cells of the 'Source library (if 'Source library' and 'Target library' are different) Other cell from other libraries will only be instanciated, and not modified.
- Hierarchical way to apply 'wide OD rules'
  - If Hierarchical (recommended for standard cells), boundary layer will be used to simulate cell abutment (as if a cell with minimum spacing OD shape has been abuted to the current processed cell).
  - If Flat mode (recommended for full custom blocks), boundary layer will not be used. Original hierarchy of the design is preserved.
- Boundary layer(s) : Use 'Boundary layer' to apply 'wide OD rules (for standard cells). If boundary layer should not be used, uncheck all boxes.
- Exclude layers : OD shapes covered by these layers will not be processed with wide OD script (for example (MKR SRAM) to exclude memory cells)
- Exclude cells : These cells (from 'Source library') will not be processed with 'wide OD script', but will be copied in 'Target library (if different library). All cells with OD rules' violations should be excluded, for example, memory cells...

❑ Restrictions

- Pcell and symbolic are not corrected (depending of DKIT) and not copied from source library to target library (if different libraries)
- 45degrees OD shapes are not processed by this tool
- There can be CO enclosure errors: if before OD stretch, the OD shape is a wide one (> 0.15um), and after stretch, this is a narrow shape (<= 0.15um), a new error can appear:
  - wide OD, CO enclosure by OD >= 0.015
  - narrow OD, CO enclosure by OD >= 0.03

To correct this error, CO must be moved manually by the designer

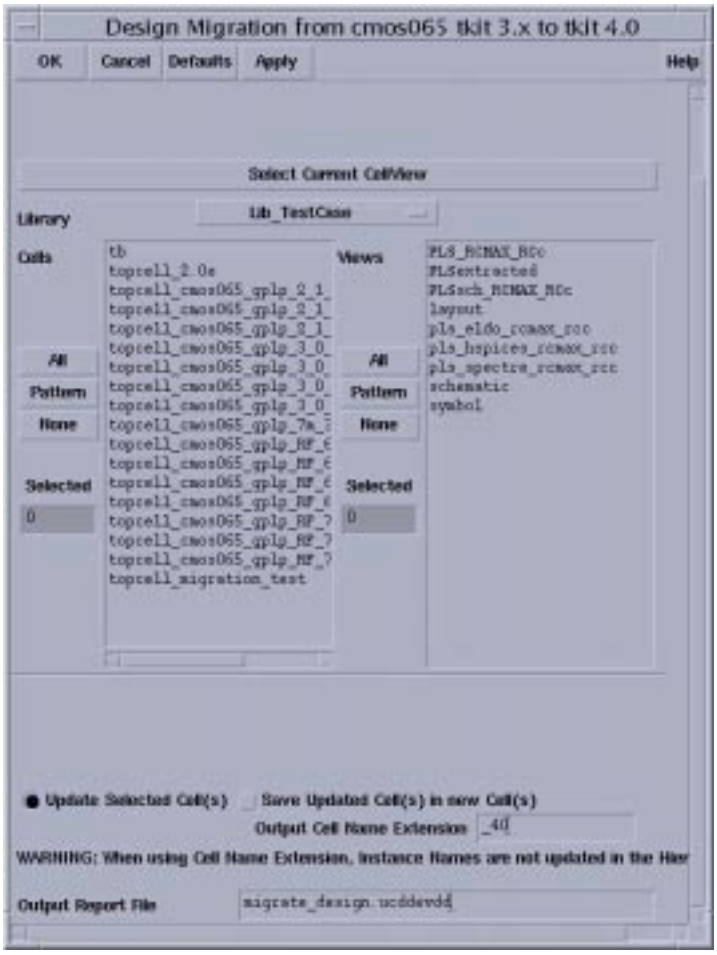
© STMicroelectronics - Reproduction and Communication of this document is strictly prohibited unless specifically authorized in writing by STMicroelectronics

3.4 MKR;GP to DCO;drawing layer migration skill

In DRM revD, the layer (MKR, GP) used to mark the GP devices (up to DRM revC) has been changed into layer (DCO, drawing). The release 4.0 of the C065 DKIT includes a skill routine aimed at moving any shape drawn on layerPurposePair (MKR, GP) to layerPurposePair (DCO, drawing), with the purpose of easying the layout rework necessary to align on DRM C065 revD.

Note that this skill routine does not modify instantiated pcells.

To launch this procedure, the user will have to type DK_cmos065_Update3x40() in the CIW. The following form will show up :



© STMicroelectronics - Reproduction and Communication of this document is strictly prohibited unless specifically authorized in writing by STMicroelectronics

- Select the library, the cell and the view (schematic or layout) corresponding to the design you want to update

- Run Design Migration

© STMicroelectronics - Reproduction and Communication of this document is strictly prohibited unless specifically authorized in writing by STMicroelectronics

4 - USER DEFINED DEVICES : BLACKBOX

The blackbox based flow has the following applications :

- to extract user device with an associated user model (modified Pcell or 3D extracted model)

- to ignore metal parasitics in a limited area

4.1 Blackbox features and Methodology

4.1.1 Symbols

The symbols associated to the blackbox based flow are box3, box4, box5, box6, box7, box8 (1 pin for substrate) proposed in STLib (See the figure below). They are X devices, they do not have auCdl view but schematic view for CDL netlisting.

Methodology:

- Inputs/outputs pins of blackbox symbols must correspond to the markers chosen in layout. Example: pin1 of a symbol must be associated to mkr;userp1 or MKR;drawing1 in layout

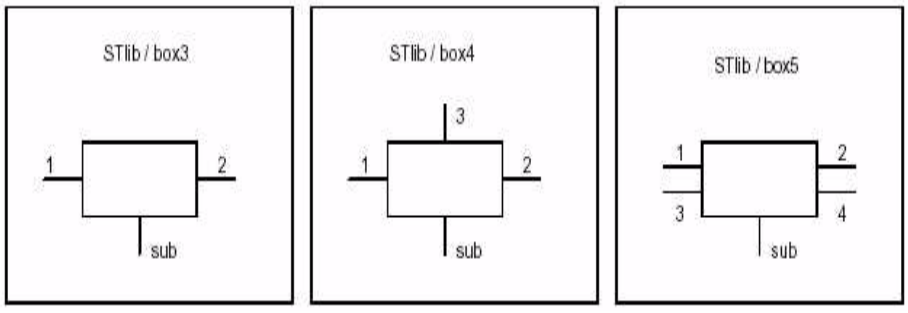


Figure 5: Bbox symbols

© STMicroelectronics - Reproduction and Communication of this document is strictly prohibited unless specifically authorized in writing by STMicroelectronics

4.1.2 Layout : CAD layers and Markers placement

The CAD layers associated to the blackbox based flow are :

- **in B7 case :** mkr;blackbox, mlabel;drawing, mkr;userp1->mkr;userp7
- **in H9 case :** blackbox;blackbox, comment;blackbox, userp1;userp1->userp7;blackbox
- **in CMOS065 case :** MKR;blackbox, MKR;label, MKR;block, MKR;drawing1->MKR; drawing7

The layer MKR;block is supported in CMOS065 only.

Methodology :

- The blackbox area must be delimited with the dedicated marker {mkr blackbox (B7) | blackbox; blackbox (H9) | MKR blackbox (CMOS065)}.

- The layer MKR block must be drawn around the active and poly areas you want to ignore (feature supported in CMOS065 only).

- Input/output pins must be identified with {mkr userp1-5 (B7) | userp1-7 blackbox (H9) | MKR drawing1-7 (CMOS065)}

- The Model name must be labelled inside blackbox with marker {mlabel dg (B7) | comment blackbox (H9) | MKR label (CMOS065)}

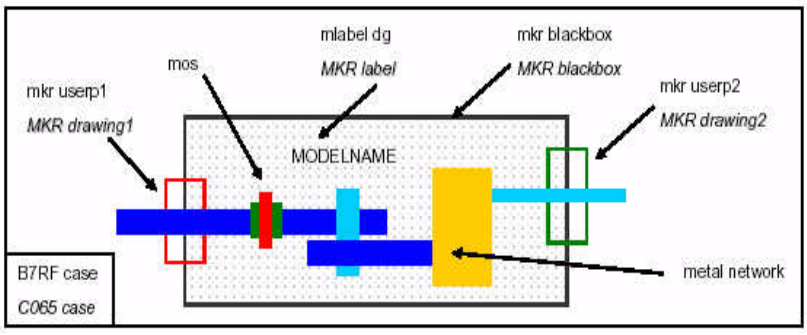


Figure 6: Bbox implementation in layout

© STMicroelectronics - Reproduction and Communication of this document is strictly prohibited unless specifically authorized in writing by STMicroelectronics

4.1.3 Layout versus schematic : example

See below an example of bbox implementation in layout and schematic.

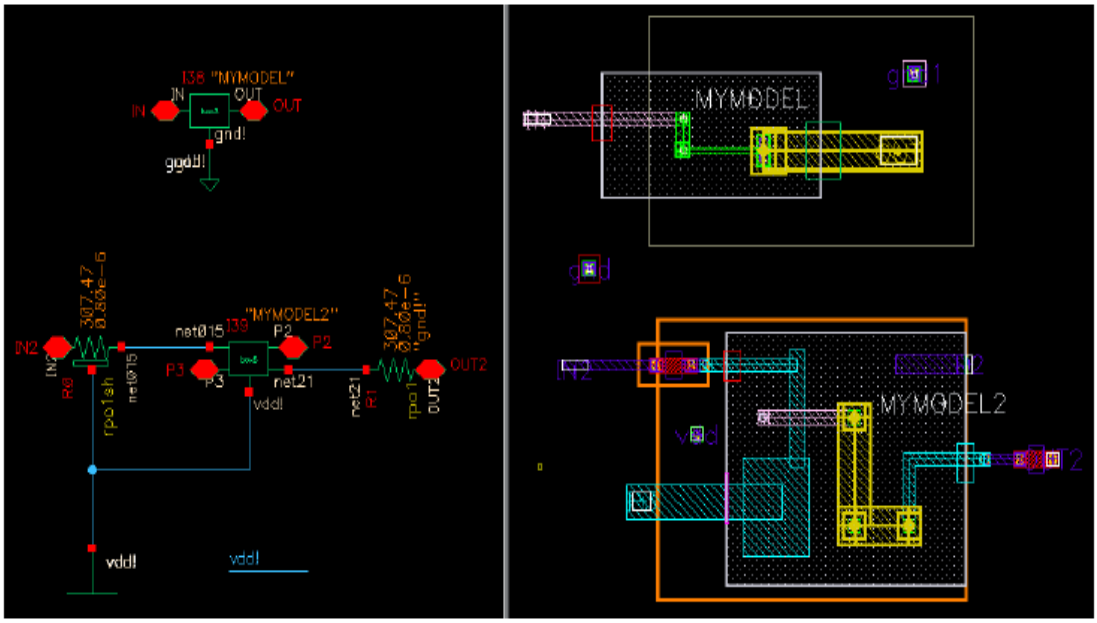


Figure 7: Bbox implementation in layout and schematic

4.2 Blackbox based flow description

4.2.1 DRC

The blackbox layer does not impact DRC: DRC is still applied inside blackbox.

4.2.2 LVS

The LVS is applied with the following rules :

- All metal levels and metal connections are ignored inside blackbox
- Active/poly grounshield is ignored inside MKR block

© STMicroelectronics - Reproduction and Communication of this document is strictly prohibited unless specifically authorized in writing by STMicroelectronics

- **Warning1 :** Active layers inside blackbox are still taken into account during LVS step. For example, mos, resistors and bipolar transistors are still extracted without metal. To ignore active and poly layers, use MKR block (supported in CMOS065 only).
- **Warning2 :** Short or opens cannot be detected through LVS as all metal connections are ignored. For example, if an open has been drawn on your inductor device by mistake, it won't be detected.

4.2.3 PLS phase2 : backannotation

To perform backannotation step during PLS phase2 (for further details on PLS phase2, please refer to TrainingPLS.pdf in $DKITROOT/doc/Manuals), the tool creates a symbol based on device name found in netlist. Therefore, any device included in the extracted netlist should have an associated symbol.

To complete a custom mapping, the user have to declare the symbols to use with its blackbox or user devices. To do so:

- Use layout or schematic menu : PLS->User Model/Device Mapping List. This menu appears when PLS phase2 form is open.

- Edit the new model / Device mapping. Model Name is the text label used in layout and the model name declared in schematic.

The backannotation will complain if this step is not done, with following message (plsintegrate_phase2.log): *Error model name has not been found for XRR0*

© STMicroelectronics - Reproduction and Communication of this document is strictly prohibited unless specifically authorized in writing by STMicroelectronics

Figure 8: PLS Model Mapping list Menu

A batch handling is also possible to run this Device mapping step :
In the case of a foreground run ("Generate Extracted View in Backgroung" button of the Simulation menu is not ticked), specific lines must be loaded in Opus CIW command line:

(let (local)
(setq local (
("MYMODELNAME"
libName "STlib"
cellName "box5"
termOrder ("box5p1" "box5p2" "box5p3" "box5p4" "box5sub") modelParameter ("macro" "MYMODELNAME")
instParameters (("a") ("np"))
)
)
)
(if (boundp UARTPlsSpfModel2DeviceUserList)
(setq UARTPlsSpfModel2DeviceUserList (,@UARTPlsSpfModel2DeviceUserList ,@local))

© STMicroelectronics - Reproduction and Communication of this document is strictly prohibited unless specifically authorized in writing by STMicroelectronics

(setq UARTPlsSpfModel2DeviceUserList local)
)
)

In this example, we have a box5 and the model name chosen is "MYMODELNAME". Be careful to chose Model names in upper case.

Warning : In the case of a Background run ("Generate Extracted View in Background" button of the Simulation menu is tick by default), these lines must be written in the local ".cdsinit". If not specified, model mapping will crash on unmaped devices.

4.2.4 Electrical simulation

To perform an electrical simulation, any bbox device should have an associated user model whose name corresponds to the one put on bbox symbol and layout.
To know how to map a device on an user model, please refer to Artist Kit documentation.

© STMicroelectronics - Reproduction and Communication of this document is strictly prohibited unless specifically authorized in writing by STMicroelectronics

5 - LAYOUT FINISHING FLOW

5.1 SealRing and Patterns

☞ Sealring

The sealring is now a rod pcell included in cmos065 library. Use the usual "Create instance" (library cmos065, cell sealring$metaloption), and fulfilled the form, as you will do whatever the pcell. The main field is the size of the circuit (not the size of the sealring) that you have to fulfilled.

To know where to instantiate the sealring: you can see the MKR sealring internally to the sealring. This is the border which have to coincide with the side of the circuit.

☞ Linename

The linename can be created using the pgtext_drc_clean, which is a pcell. Use the usual "Create instance" (library cmos065, cell pgtext_drc_clean), and fullfill the fields Text string and Text height. The Text Layer must be choosen to the TOP level metal of the process.

Warning: only size > 3.4 are DRC clean.

Just add on the linename the AP tilenot and BOTMIM tilenot if you don’t want dummies on linename. In the same way, if you don’t want the usual Metalsizing during mask generation, you can change the Metaldrawing in Metal noprocessing (option in the Form).

You must add the MKR logo on the linename to avoid DRC errors if you choose purpose noprocessing.

It is recommended to place the linename in the IO corner (cf DRM to read exact rules)

☞ STLogo

The STLogo can be found in the cmos065 library and can be instanciated in a circuit.

N.B: F and reticles numbers are no more needed.

© STMicroelectronics - Reproduction and Communication of this document is strictly prohibited unless specifically authorized in writing by STMicroelectronics

5.2 Tiling Procedure

5.2.1 Why tiling is necessary

- **OD**

The CMP (Chemical Mechanical Planarization) process for the STI (Shallow Trench Isolation) has been optimized as a trade off between junction leakage wich happens when the STI to ACTIVE step is too high, and transistor leakage (hump effect) which increases when the STI/ ACTIVE step is too negative.

However, the STI step uniformity is depending upon the ACTIVE density uniformity ; This is why insertion of dummy active areas (tiles) is mandatory if density constrainsts as described in the DRM are not reached.

- **PO**

The poly width uniformity across the wafer is depending upon the POLY density uniformity ; This is of particular interest to improve the optimization of saturation current versus leakage current.

- **Metalisation levels**

Metals used for interconnects (M1 to M9)

There are several motivations to request a minimum metal density :

- Etching processes : etching machines can overetch when the pattern density is low. There are two signatures of this problem : reduced metal width and metal residues between lines that can cause shorts and reduce the yield.

- Plasma damage (charging) problems : experience obtained on test vehicles has clearly shown that reticles with low metal density induce more charging than reticles with hiher metal density.

- Dielectric thickness uniformity across the die : the CMP planarization is a large scale planarization : it depends upon the metal density in a range of 2-5mm. The dielectric surface after CMP is higher in the areas with higher metal density. This effect is cumulative from metal1 to metal6, and it can be difficult to print vias in two areaas with different metal densities, as the depth of focus can be sufficient ; at least, it can reduce the process window, and reduce

© STMicroelectronics - Reproduction and Communication of this document is strictly prohibited unless specifically authorized in writing by STMicroelectronics

the yield and the reliability. This is why density design rules are present in the DRC (local densities)

- **ALUCAP**

Alucap is necessary on top of the bonding pads in case of Copper process. Tiling is necessary to ensure correct processing of this layer in cmos065.

5.2.2 Tiles generation

How to use the cmos065 calibre procedure to insert tiles in your design?

Tiles are generated by a calibre DRC run; indeed, calibre has the possibility to generate a gds result database.

The following steps should be followed in order to automatically insert OD, PO, METAL and ALUCAP tiles in your design:

- **Preliminary** : Add exclusion zones (optional)

Add exclusion zones in the layout view : Exclusion zones are circuit areas where tiles are not to be placed. For this, the user must draw polygons in specific layers whose objective is to drive the calibre procedure not insert tiles where drawn.
The following table lists the different layers that can be used to monitor the tiles insertion, together with their description.

Table1: Layer	Table2: MKR tileNot	Table3: OD tileNot	Table4: RPO tile	Table5: PO tileNot	Table6: M1 tileNot	Table7: M2 tileNot	Table8: M3 tileNot	Table9: M4 tileNot	Table10: M5 tileNot	Table11: M6 tileNot	Table12: M7 tileNot	Table13: M8 tileNot	Table14: M9 tileNot	Table15: AP tileNot
OD	no impact	no tile	no impact	no impact	no impact	no impact	no impact	no impact	no impact	no impact	no impact	no impact	no impact	no impact
RPO	no impact		RPO on each OD tile	no impact	no impact	no impact	no impact	no impact	no impact	no impact	no impact	no impact	no impact	no impact
PO	no tile	no tile	no impact	no tile	no impact	no impact	no impact	no impact	no impact	no impact	no impact	no impact	no impact	no impact
M1	no tile	no impact	no impact	no impact	no tile	no impact	no impact	no impact	no impact	no impact	no impact	no impact	no impact	no impact
M2	no tile	no impact	no impact	no impact	no impact	no tile	no impact	no impact	no impact	no impact	no impact	no impact	no impact	no impact

© STMicroelectronics - Reproduction and Communication of this document is strictly prohibited unless specifically authorized in writing by STMicroelectronics

Table1: Layer	Table2: MKR tileNot	Table3: OD tileNot	Table4: RPO tile	Table5: PO tileNot	Table6: M1 tileNot	Table7: M2 tileNot	Table8: M3 tileNot	Table9: M4 tileNot	Table10: M5 tileNot	Table11: M6 tileNot	Table12: M7 tileNot	Table13: M8 tileNot	Table14: M9 tileNot	Table15: AP tileNot
M3	no tile	no impact	no impact	no impact	no impact	no impact	no tile	no impact	no impact	no impact	no impact	no impact	no impact	no impact
M4	no tile	no impact	no impact	no impact	no impact	no impact	no impact	no tile	no impact	no impact	no impact	no impact	no impact	no impact
M5	no tile	no impact	no impact	no impact	no impact	no impact	no impact	no impact	no tile	no impact	no impact	no impact	no impact	no impact
M6	no tile	no impact	no impact	no impact	no impact	no impact	no impact	no impact	no impact	no tile	no impact	no impact	no impact	no impact
M7	no tile	no impact	no impact	no impact	no impact	no impact	no impact	no impact	no impact	no impact	no tile	no impact	no impact	no impact
M8	no tile	no impact	no impact	no impact	no impact	no impact	no impact	no impact	no impact	no impact	no impact	no tile	no impact	no impact
M8	no tile	no impact	no impact	no impact	no impact	no impact	no impact	no impact	no impact	no impact	no impact	no impact	no tile	no impact
ALU-CAP	no tile	no impact	no impact	no impact	no impact	no impact	no impact	no impact	no impact	no impact	no impact	no impact	no impact	no tile

- **The tiling generation is available by using Calibre run**.

A fully described procedure is available in **$DKITROOT/doc/Manuals/ calibrerunTiling_doc.pdf**

The merging of the 2 gds files obtained can also be done by calibrerun.

5.2.3 Processing of the tiles in the different CAD flows

- **DRC**

The correct placement of the tiles (OD, PO, MeTLAS, ALUCAP) is checked inside the standard cmos065 calibre DRC rule file. In particular:

- the overlap of tiles with actual design shapes in the same layer are flagged as errors,

- the space between tiles and actual design shapes in the same layer is checked,

- the design rules for tiles insertion as defined in chapter 7.4.6 of cmos065 DRM are checked.

© STMicroelectronics - Reproduction and Communication of this document is strictly prohibited unless specifically authorized in writing by STMicroelectronics

This ensures that no short circuit is done due to a METAL tile for example.cmos090 DRC rule file also includes checks aimed at flagging as errors CONTACTs or VIASs which would be placed on top of tiles (OD, PO, METALs).

- **LVS**

Thanks to the DRC checks described above, it is not necessary to take into account the tiles at LVS level. Indeed, any short, or badly formed device due to tiles is flageed as a DRC error.

Taking into account tiles at LVS level would be inefficient as far as CPU time and memory allocation is concerned (for the LVS tool); indeed, when doing so, connectivity has to be established for each single floating tile and would result in huge resulting databases and CPU times.

© STMicroelectronics - Reproduction and Communication of this document is strictly prohibited unless specifically authorized in writing by STMicroelectronics

6 - GEOMETRICAL/ELECTRICAL BASED FLOWS

From the version 3.0 of the DK , it is possible to use either the pure **geometrical** parameters or a mix of geometrical and **electrical** parameters at any step of the analog flow : schematic capture, simulation, LVS, extraction, Post Layout Simulation. The first part describes the differences between the electrical and the geometrical based flow. The second part, which is more CAD related, explains how to switch from a mode to another.

6.1 Electrical/Geometrical based flows methodology

The Geometrical/Electrical based flows concern Geometrical/Electrical devices like resistors and capacitors. Such a support implies an extension of the parameters deck for CDL netlisting, LVS, PLS and electrical simulation, as explained in the following overview :

6.1.1 CDL Netlisting

CDL netlist is extended to show all the parameters (geometrical and electrical) in order to authorize the LVS on any parameters.

Example : CDL netlist of a resistor:

R1 a b gnd rpporpo W=2 L=3 R=1K

=> Both geometrical (W, L) and electrical (R) parameters are netlisted.

6.1.2 Device extraction and LVS methodology

LVS is extended to extract, upon user request, either the geometrical parameters or the electrical parameters. LVS is done, by default, on geometrical parameters or in case of Electrical mode, on all the parameters used in the front-end netlist. This means that the CALIBRE deck is extended to add the same generic equations as the callbacks in the extraction section of the LVS command file.

© STMicroelectronics - Reproduction and Communication of this document is strictly prohibited unless specifically authorized in writing by STMicroelectronics

Example : For a resistor, the LVS is done on :
W and L parameters in geometrical mode
W and R parameters in electrical mode

All these extensions are controlled by a dedicated switch in order to preserve the current methodology as the default. This switch called "Enable Electrical comparison" is available on the LVS customization settings form, as shown on the snapshot below:

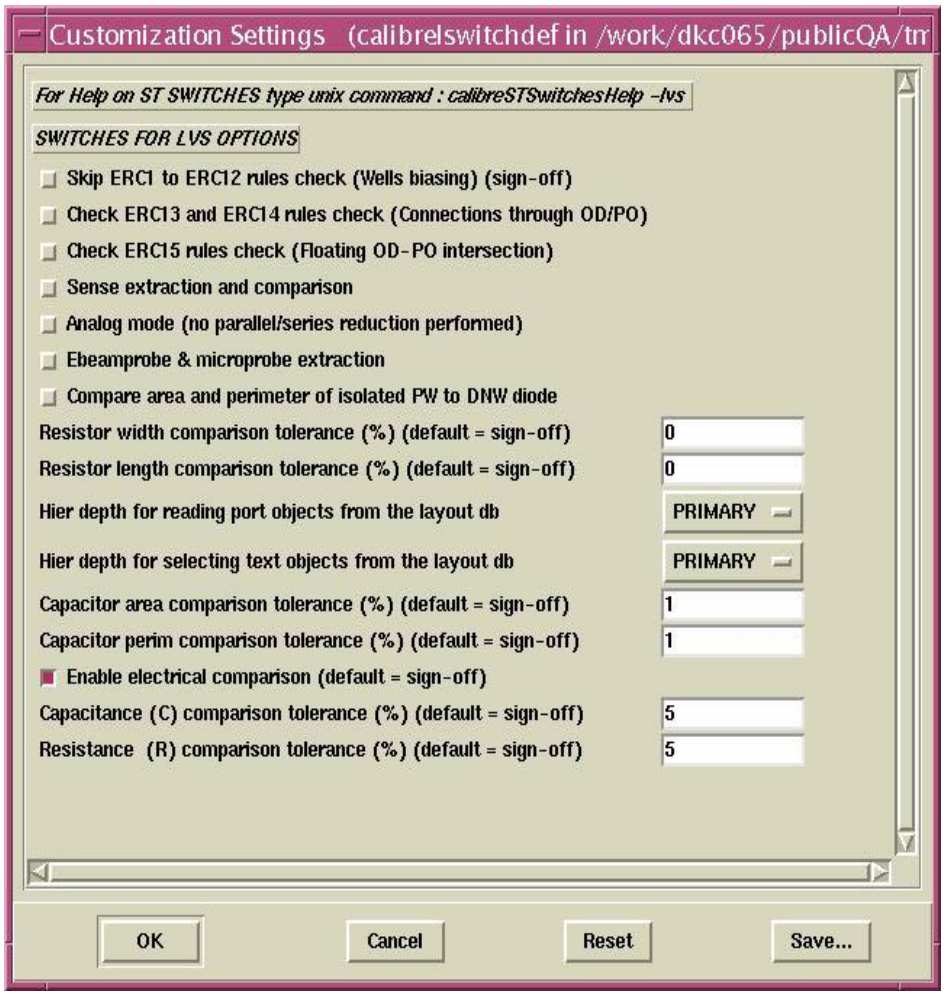


Figure 9: LVS customization settings : "Enable electrical comparison " switch

This customization switch can be selected or unselected manually like the other switches.

© STMicroelectronics - Reproduction and Communication of this document is strictly prohibited unless specifically authorized in writing by STMicroelectronics

However, its default/sign-off value depends on the netlisting mode :
It is selected in Geometrical Mode and unselected in Electrical Mode.

6.1.3 Spice Netlisting

For each supported simulator, Spice netlist is extended to show, upon user request, either the geometrical parameters or the electrical parameters.

Example : Spice netlist for a resistor :

R1 a b gnd rpporpo W=2 L=3 in geometrical mode

R1 a b gnd rpporpo W=2 R=1K in electrical mode

The netlisting mode selection is controlled by a shell variable. See paragraph 3.2 for further explanations.

6.1.4 Electrical/Geometrical devices parameters

Device	cdlparameters	lvsparameters	spiceparameters
RESISTORS rpporpo rnporpo rpodrpo rhiporpo rnpoi rpppoi	w l sense m b nhead r	**Geom:** W L SENSE **Elec:** W R SENSE	**Geom:** w l nhead mult mismatch **Elec:** w r nhead mult mismatch
Metal RESISTORS rm1 rmx rmz rap	w l r	**Geom:** W L **Elec:** W R	**Geom:** w l mult mismtach **Elec:** w r mult mismatch
Stacked metal fringe CAPACITORS cfrm1m5shz cfrm1m5shznosub	l nf m c	**Geom:** L NF **Elec:** C NF	**Geom:** l nf mult mis-match **Elec:** nf mult mismatch c

© STMicroelectronics - Reproduction and Communication of this document is strictly prohibited unless specifically authorized in writing by STMicroelectronics

Plate CAPACITORS cm1mx cmxmx cmxmz cmzmz	carea cperi toplayer m c	**Geom:** CAREA CPERI TOPLAYER **Elec:** TOPLAYER C	**Geom:** carea cperi mult mismatch **Elec:** c mult mismatch
Poly CAPACITORS cpogpnw cpolpnw cpo18nw cpo18pw cpo25nw cpo25pw	carea cperi sense m b c w	**Geom:** CAREA CPERI SENSE **Elec:** C W SENSE	**Geom:** carea cperi mult mismatch **Elec:** c w mult mismatch
MIM CAPACITORS cmimmk4x0y cmimmk4x0ynosub	carea cperi sense m b c	**Geom:** CAREA CPERI SENSE **Elec:** C SENSE	**Geom:** carea cperi mult mismatch **Elec:** c mult mismatch
STRIPE CAPACITOR cmstrstk	carea cperi botlayer toplayer m c nsp	**Geom:** CAREA CPERI BOTLAYER TOPLAYER **Elec:** BOTLAYER TOPLAYER C NSP	**Geom:** carea cperi bot-layer toplayer mult mis-match **Elec:** botlayer toplayer c nsp mult mismatch

N.B. : This feature is also supported by devices RF (inductors and varactors) in DK C065 RF. See the corresponding Electrical/Geometrical parameters table in chapter RF DEVICES LIBRARY.

6.2 Netlisting mode selection / activation

The netlist mode, electrical or geometrical based, is globally defined by a "configuration variable" (an external environment variable) called **U2DK_Netlisting_Mode** . Default mode is "Geometrical". There are different ways to switch the whole design environment from geometrical to electrical mode or from electrical to geometrical mode.

6.2.1 UNIX shell

The shell variable U2DK_Netlisting_Mode can be set manually by executing one of the following UNIX commands :
setenv U2DK_Netlisting_Mode Electrical : sets the design environment in Electrical mode
setenv U2DK_Netlisting_Mode Geometrical : sets the design environment in Geometrical mode

© STMicroelectronics - Reproduction and Communication of this document is strictly prohibited unless specifically authorized in writing by STMicroelectronics

These UNIX commands must be executed before starting Cadence to be effective.

6.2.2 Cadence opus

The netlisting mode can also be changed during a Cadence Session. Six functions relative to the U2DK_Netlisting_Mode variable are available from Cadence IC, once the DK loaded and a design opened. Each one has to be loaded in the CIW to be executed.

- **DK_NetlistingMode :** returns the current netlisting mode
- **DK_DefaultNetlistingMode :** returns the default netlisting mode, i. e. "Geometrical"
- **DK_SetNetlistingModeGeometrical :** sets the design environment in Geometrical mode
- **DK_SetNetlistingModeElectrical :** sets the design environment in Electrical mode
- **DK_IsNetlistingModeGeometrical :** returns true if the current netlisting mode is "Geometrical"
- **DK_IsNetlistingModeElectrical :** returns true if the current netlisting mode is "Electrical"

6.2.3 CDF Update step

Once the netlisting mode is selected, it is compulsory to update the technology dependant parameters of the chosen design to ensure its correct migration from geometrical to electrical (or electrical to geometrical) netlisting mode

To do that, the CDF_UPDATE tool, available from the CIW: "Design Kit -> Design Update cdf" is very helpful. To run correctly this procedure, follow the instructions below :

- Run Design Kit -> Design Update cdf from the CIW

- Select the library, the cell and the view corresponding to the design you want to update

- Tick "Update device value" (It will update the electrical parameters of the design and keep the geometrical parameters and the layout view unchanged).

- Run Update cdf

Once CDF update steps is achieved, the netlisting mode for the chosen design is effective.

© STMicroelectronics - Reproduction and Communication of this document is strictly prohibited unless specifically authorized in writing by STMicroelectronics

See further details on CDF update procedure in Migration procedures part

© STMicroelectronics - Reproduction and Communication of this document is strictly prohibited unless specifically authorized in writing by STMicroelectronics

7 - OPENACCESS SUPPORT

From the version 3.0 of the DK, both CDBA and OpenAccess (OA) databases are supported.

This means that the DK contains CMOS065 libraries and techfiles in both CDBA and OA format.

N.B : The DK libraries have the same name in OA or CDBA environment.

7.1 OA/CDBA Environment Selection

The selection of the database is controlled by an external environment variable called **opusdbtype**. This variable is set to "OpenAccess" in an OA environment and to "" in a CDBA environment.

The setting of the variable opusbdtype is automatically done by uniopus depending on the IC version used to load the DK:

- If an IC version dedicated to OA is used, the opusdbtype will be automatically set to "OpenAcces" and the OA database of the DK will be loaded.
- If an IC version dedicated to CDBA is used, the opusdbtype will be automatically set to "" and the CDBA database of the DK will be loaded.

If unipous is not used, the Design Kit will set the variable opusdbtype to its correct value only if IC tool is loaded before the Design Kit.

In the case of the variable opusdbtype is not set automatically, it can be done manually by executing one of the following UNIX command before starting a Cadence Session:

setenv opusdbtype OpenAccess : sets an OA Environment

setenv opusdbtype : sets a CDBA Environment

© STMicroelectronics - Reproduction and Communication of this document is strictly prohibited unless specifically authorized in writing by STMicroelectronics

Be careful that the IC version you use is compatible with the environment you want to load.

7.2 OA/CDBA Environment Compatibility

Do pay attention that CDBA libraries are not compatible with OA environment. To use a CDBA design in OA environment, a conversion from CDBA to OA format is needed. The CDBA2OA conversion script included in the OA IC version achieves such conversion on Libraries. The script is run by executing the following command:

cdb2oa -lib <t_libName> -cdslibpath <t_libPath> <options>

See Cadence Doc for further explanations.

© STMicroelectronics - Reproduction and Communication of this document is strictly prohibited unless specifically authorized in writing by STMicroelectronics

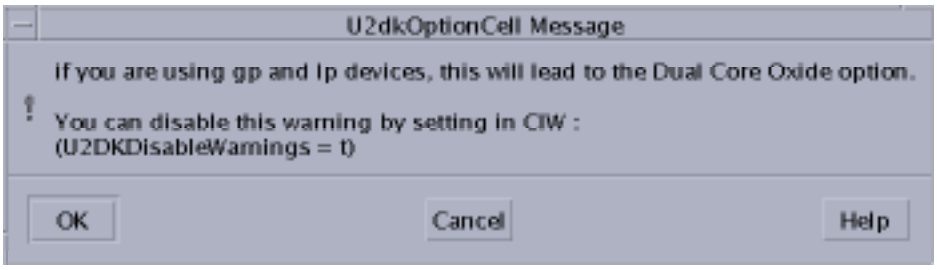
8 - DESIGN KIT EXTRA FEATURES

8.1 Option management features

8.1.1 Warnings at schematic design

Warning Messages are implemented to alert the designers about Design Configurations which are: ALLOWED (DRM revB compliant) like ALL-GO1 but no costless (additional mask):

- When instantiating a LP device, no warning is prompted, this is the default.
- When instantiating a GP device, the following warning is prompted.
  (an environment variable must be set U2DKDisableWarnings = 0 to be able to mix LP/GP)



8.1.2 Checks at layout design

Warning Messages are implemented to alert about Design Configurations which are NOT ALLOWED like ALL-GO2. Not possible to mix 1.8V & 2.5V devices.

- The ALERT/WARNING messages in that case will come at DRC phase (SIGNOFF)
  Rule : OD2.MRC.1 OD_25 and OD_18 are mutually exclusive process options: cannot be used in same die.

© STMicroelectronics - Reproduction and Communication of this document is strictly prohibited unless specifically authorized in writing by STMicroelectronics

8.2 Co Simulation

The "Co simulation" is the feature that enable the designer to load and co-simulate multiple DKs (from 65nm and beyond along with IPAD DK) in the same Analog Design Environment and DFII session (e.g.: c065_rf_hv + c045 + t2pta1). The name of DK libraries are Technology-Option based to enable the display of all design kit libraries. The following device libraries are available in the 65nm RF Design Kit:

- the cmos065 device library includes all the basic devices available in CMOS065 DRMs such as dual core oxide LP/GP MOS, GO2, active (pnp, npn) and passive devices (capacitors, resistors) .
- the cmos065_rf device library includes all the RF devices such as RF MOS, inductors, the mosfet and diode varactors

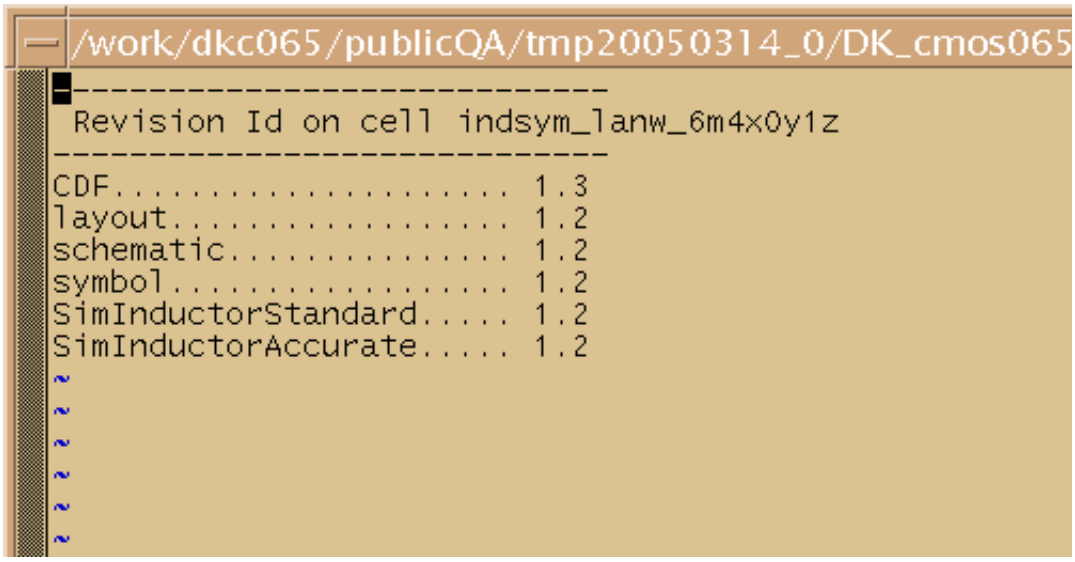
To limit the conflict between two simulation models, the Design Kit includes two set of models, one for the standard simulation and one for the "Co simulation" mode. During the simulation, the Artist Kit product will uses the correct model library.

- When the "Co simulation" mode is not found, the simulation models are taken from the <DKITROOT>/DATA/<simulator>/CORNERS path. For example, the following models are used:
  .subckt <model name>
  ...
  ...
  ...
  .ends
- When the "Co simulation" mode is found, the simulation models are taken from the <DKITROOT>/DATA/<simulator>/COSIM path. For example, the following models are used:
  .subckt <model name>_<techno name>
  ...
  ...
  ...
  .ends

© STMicroelectronics - Reproduction and Communication of this document is strictly prohibited unless specifically authorized in writing by STMicroelectronics

8.3 Device Library versionning

The device library of the Design Kit are proposed with a versionning feature. The Id textual view is proposed for each device to give the release of the proposed views. The following figure gives an example. If the current view has changed compared to the previous delivery, the change is prompt with the "new release (<- old release)" line.



© STMicroelectronics - Reproduction and Communication of this document is strictly prohibited unless specifically authorized in writing by STMicroelectronics

8.4 Design Kit Architecture

The Design Kit architecture has been update in order to meet the following description. It gives a better visibility for any user who want to get the raw design kit data such as the verification files or the simulation models.

$DKITROOT/:	
DATA/	
ADS	*ADS models*
CALIBRE_CORE/	*Calibre rule file for the core*
CALIBRE_CUSTOM/	*Calibre rule file for the option*
DATA.info	*Detailed contents of the data*
DKShared/	*Dk procedures*
DKtools/	*Dk feature for layout design*
ELDO/	*Eldo models*
HSPICE/	*Hspice models*
ICC/	*VCAR rules*
LIB/	*Device library for the core*
LIB_RF/	*Device library for the option*
PLS_CORE/	*Post layout for the core*
PLS_CUSTOM/	*Post layout for the options*
SKILL/	*Dk skill procedures*
SPECTRE/	*Spectre models*
STLIB/	*Extra library for simulation purpose*
DK_cmos065lpgp_RF_6m4x0y1z_50A28A.cdslib	*Design Kit Set Up*
DK_cmos065lpgp_RF_6m4x0y1z_50A28A.csh	*"*
DK_cmos065lpgp_RF_6m4x0y1z_50A28A.info	*"*
DK_cmos065lpgp_RF_6m4x0y1z_50A28A.loader	*"*
DK_cmos065lpgp_RF_6m4x0y1z_50A28A.ptbl	*"*
DK_cmos065lpgp_RF_6m4x0y1z_50A28A.simrc	*"*
PIGET/	*Design Kit Tables Definition*
bin/	*Binary Codes*
doc/	*Documentations*
etc/	
opusInitMsg	

8.5 Interconnects Parasitic Capacitances Modeling (ICM)

The ICM document contained in the DK (see $DKITROOT/doc/Manuals/icm_doc.pdf) is aimed at providing CMOS065 designers with raw data related to interconnects parasitic capacitances. Such raw data, applicable to specific CMOS065 layout configurations only, can be used by designers to derive estimated absolute values for wire parasitic capacitances.

© STMicroelectronics - Reproduction and Communication of this document is strictly prohibited unless specifically authorized in writing by STMicroelectronics

8.6 Mask List utility

The input of Mask List utility is either a GDS2 or a Cadence cellname.
The output is the suitable list of all Masks to help designer when filling out the final Mask Lot Request.

Please notice that this Mask List procedure is aligned with the list of mask layers from the C065 DRM (Mask Table - Process Feature Matrix) and with the correponding layers definition in DK (Layer Map Table).

Do pay attention this ML utility is aimed at helping the end-user out but it is NOT a Sign-Off tool as the final result (output) must be double-checked by project leader and techno responsible.
Thus, the DK ML utility can not be responsible for a Mask order failure.

8.6.1 How to run ML utility ?

From CDS IC session : Run Mask List from the CIW (Design Kit->Mask List). The following form shows up :

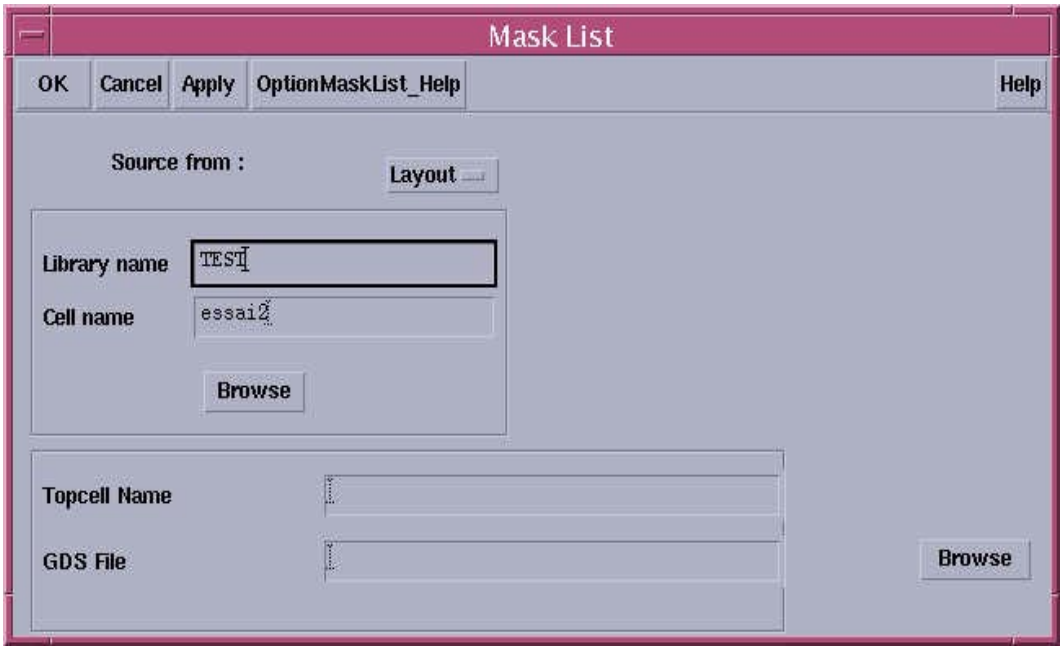


Figure 10: Mask List Tool

© STMicroelectronics - Reproduction and Communication of this document is strictly prohibited unless specifically authorized in writing by STMicroelectronics

ML (Mask List) procedure can be run on a:

- **GDS2 :**
  - Select Source from "GDS"
  - Select a GDS File by clicking on the button "Browse" and fill in the Topcell name
- **Cadence cell :**
  - Select Source from "Layout"
  - Select a Library and a Cell name by clicking on the button "Browse"

From UNIX command line (only on a GDS2 file):

- Type the following: **piGetInfo $DKITROOT dkML**
- Fill in the following prompt **:**
  - gds name: Full path/topcell.gds
  - primary cell name: topcell_name

Warning : ML utility works on Solaris only

8.6.2 Results

The ML Results are given in the directory: MASK_topcell__date_hour/. This directory contains the following files

- **DRC_CALI_RUN_topcell.log :** Calibre execution log file
- **topcell.gds :** GDS2 of the design (if ML is run from layout)
- **pipo_out_error :** stream-out execution log (if ML is run from layout)
- **maskList.topcell :** Mask list results. It lists :
  - The Core Process Mask List (Masks commanded by default)
  - The list of process options found in the GDS2 (ex: 9 metal level option). Each process option implies masks either to add or to remove from the Core Process Mask list.
  - The List of Masks to add to the Core Process Mask List
  - The List of Masks to remove from the Core Process Mask List

© STMicroelectronics - Reproduction and Communication of this document is strictly prohibited unless specifically authorized in writing by STMicroelectronics

- ☞ **FINAL MASK LIST** : resulting list of all the masks necessary to process the circuit

❑ **topcell.maskresults :** Summary of the process options used in the circuit and of the corresponding layers needed (to add) or unused (to remove).

© STMicroelectronics - Reproduction and Communication of this document is strictly prohibited unless specifically authorized in writing by STMicroelectronics

© STMicroelectronics - Reproduction and Communication of this document is strictly prohibited unless specifically authorized in writing by STMicroelectronics

9 - RF DEVICES LIBRARY

9.1 Naming Convention

- **RF MOS devices**

Naming convention : <TYPE><VT><OX_ID>[variant]_rf

The naming convention defines the type of the transistors in term of family (n or p), and performance (various VT) etc... with this following syntax:

- <TYPE>= n : nmos transistor
- <TYPE>= p : pmos transistor
- <VT>= svt : standard Vt
- <VT>= hvt : high Vt
- <VT>= lvt : low Vt
- <OX_ID>= lp,gp, double oxyde MOS (50A)

Examples: nsvtlp_rf or psvtlp_rf

Device	Device name in cmos065_rf library	CDF type	Pcell	Pins	Comment
NMOS Standard Vt LP	nsvtlp_rf	nmos	yes	d g s b	
PMOS Standard Vt LP	psvtlp_rf	pmos	yes	d g s b	
NMOS Low Vt LP	nlvtlp_rf	nmos	yes	d g s b	
PMOS Low Vt LP	plvtlp_rf	pmos	yes	d g s b	
NMOS HPA LP	nhpalp_rf	nmos	yes	d g s b	
PMOS HPA LP	phpalp_rf	pmos	yes	d g s b	
NMOS GO2 28A (1.8V)	nsvt18_rf	nmos	no	d g s b	
PMOS GO2 28A (1.8V)	psvt18_rf	pmos	no	d g s b	
NMOS GO2 50A (2.5V)	nsvt25_rf	nmos	no	d g s b	
PMOS GO2 50A (2.5V)	psvt25_rf	pmos	no	d g s b	

© STMicroelectronics - Reproduction and Communication of this document is strictly prohibited unless specifically authorized in writing by STMicroelectronics

❑ Inductor devices

- Naming convention : ind[variant]_family<TYPE>[option]

The naming convention defines the type of the inductors with this following syntax:

[variant]: symmetrical / differential

<family>: standard / choke / low area / low value

type: narrow width / multi-finger

option: 6m4x0y1z / 7m4x0y2z

Examples:

ind_stdnw_6m4x0y1z, indsym_nw_6m4x0y1z, inddif_nw_6m4x0y1z, ind_lonw_6m4x0y1z, indsym_lanw_6m4x0y1z and inddif_lanw_6m4x0y1z

Device	Device name in cmos065_rf library	CDF type	Pcell	Pins	Comment
Standard Inductor	ind_stdnw_6m4x0y1z	inductor	yes	in out sub	
	ind_stdnw_7m4x0y2z				
Symetrical narrow width Inductor	indsym_nw_6m4x0y1z	inductor	yes	in out sub	
	indsym_nw_7m4x0y2z				
Differential narrow width Inductor	inddif_nw_6m4x0y1z	inductor	yes	in mp out sub	
	inddif_nw_7m4x0y2z				
Low value Inductor	ind_lonw_6m4x0y1z	inductor	yes	in out sub	
	ind_lonw_7m4x0y2z				
Differential low value Inductor	inddif_lonw_6m4x0y1z	inductor	yes	in mp out sub	
	inddif_lonw_7m4x0y2z				
Symetrical low area Inductor	indsym_lanw_6m4x0y1z	inductor	yes	in out sub	
	indsym_lanw_7m4x0y2z				

© STMicroelectronics - Reproduction and Communication of this document is strictly prohibited unless specifically authorized in writing by STMicroelectronics

Differential narrow width inductor	inddif_lanw_6m4x0y1z inddif_lanw_7m4x0y2z	inductor	yes	in mp out sub	

❑ **RF Mos Vactor devices**

- Naming convention : cpo<Oxide><Well>_var[_option]

The naming convention defines the type of the mosfet varactors with this following syntax:

<Oxide> lp / gp / 18 / 25

<well> nwell / pwell

[Option]= 6m4x0y1z / 7m4x0y2z

Examples:

cpo25nw_var, cpo18nw_var, cpo25pw_var, cpo18pw_var

Device	Device name in cmos065_rf library	CDF type	Pcell	Pins	Comment
Varactor NMOS GO2 28A (1.8V)	cpo18nw_var	varactor	yes	in out sub	
Varactor PMOS GO2 28A (1.8V)	cpo18pw_var	varactor	yes	in nwell out sub	
Varactor NMOS GO2 50A (2.5V)	cpo25nw_var	varactor	yes	in out sub	
Varactor PMOS GO2 50A (2.5V)	cpo25pw_var	varactor	yes	in nwell out sub	

❑ **RF Diode Varactor devices**

- Naming convention : d<Type><Vt><Oxide>_var[_option]

The naming convention defines the type of the diode varactors with this following syntax:

© STMicroelectronics - Reproduction and Communication of this document is strictly prohibited unless specifically authorized in writing by STMicroelectronics

<Type> n / p

<Vt> svt / lvt / hvt

<Oxide> lp / gp / 18 / 25

[Option]= 6m4x0y1z / 7m4x0y2z

Examples: dnsvtlp_var

Device	Device name in cmos065_rf library	CDF type	Pcell	Pins	Comment
Diode varactor	dnsvtlp_var	varactor	yes	in out sub	

❑ **RF CAPACITOR devices**

- Naming convention : c<Type>_rf_<Option>

The naming convention defines the type of the diode varactors with this following syntax:

<Type> frstack/fr

[Option]= 6m4x0y1z / 7m4x0y2z

Examples: cfrstack_rf_7m4x0y2z

Device	Device name in cmos065_rf library	CDF type	Pcell	Pins	Com-ment
MOM RF without shield	cfrstack_rf_6m4x0y1z	mom	yes	minus plus psub	
	cfrstack_rf_7m4x0y2z				
MOM RF with shield	cfrstack_rf_6m4x0y1z_sh	mom	yes	minus plus psub shap	
	cfrstack_rf_7m4x0y2z_sh				

© STMicroelectronics - Reproduction and Communication of this document is strictly prohibited unless specifically authorized in writing by STMicroelectronics

9.2 Electrical/Geometrical devices parameters

The Geometrical/Electrical based flows concern inductors and varactors in RF devices library. See below their Electrical/Geometrical parameters for CDL, LVS and SPICE netlisting.

Device	cdlparameters	lvsparameters	spiceparameters
INDUCTORS indsym_nw_* indsym_lanw_* ind_stdnw_*	D W NBTURNS L LS	**Geom:** D W NBTURNS L **Elec:** W NBTURNS L LS	**Geom:** d w nbturns l fq **Elec:** w nbturns l fq ls
INDUCTORS ind_lonw_*	D W N L LS	**Geom:** D W L **Elec:** W L LS	**Geom:** d w l fq **Elec:** w l fq ls
INDUCTORS inddif_nw_* inddif_lanw_*	D W NBTURNS L MPOUT LS	**Geom:** D W NBTURNS L **Elec:** W NBTURNS L LS	**Geom:** d w nbturns l mpout fq **Elec:** w nbturns l fq mpout ls
INDUCTORS inddif_lonw_*	D W L MPOUT LS	**Geom:** D W L **Elec:** W L LS	**Geom:** d w l mpout fq **Elec:** w l fq mpout ls
MOS VARACTORS cpo18nw_var cpo18pw_var cpo25nw_var cpo25pw_var	W L NBFP C	**Geom:** W L NBFP **Elec:** W NBFP C	**Geom:** w l nbfp **Elec:** w nbfp c
DIODES VARACTORS dnsvtlp_var	WFP LFP NBFP C_0V	**Geom:** WFP LFP NBFP **Elec:** WFP NBFP C_0V	**Geom:** wfp lfp nbfp **Elec:** wfp nbfp c_0v
MOM RF cfrstack_rf_*	NF_DIRX NF_DIRY M C	**Geom:** NF_DIRX NF_DIRY **Elec:** NF_DIRX C	**Geom:** nf_dirx nf_diry mult **Elec:** c nf_diry mult

See chapter 3 for further details on the Electrical/Geometrical based flows methodology.

9.3 LVS Options

RF devices dedicated LVS options are available in Electrical and/or Geometrical modes :

© STMicroelectronics - Reproduction and Communication of this document is strictly prohibited unless specifically authorized in writing by STMicroelectronics

=> Inductors d&w comparsion tolerance (%) : **Geometrical mode (default)**

=> Inductors l comparison tolerance (%) : **Both Electrical and Geometrical modes**

=> Inductors ls comparison tolerance (%) : **Electrical mode**

=> Tolerance for mosRF W comparison (%) : **Both Electrical and Geometrical modes**

=> Tolerance for mosRF L comparison (%): **Both Electrical and Geometrical modes**

=> Varactors w&l tolerance (%) : **Geometrical mode**

=> Varactors capacitance tolerance (%) : **Electrical mode**

N.B: The electrical parameters comparison is enabled by selecting the switch "Enable Electrical comparison (default = sign-off)" switch.

For further details on LVS part, please refer to Calibre documentation (in $DKITROOT/doc/ Manuals)

© STMicroelectronics - Reproduction and Communication of this document is strictly prohibited unless specifically authorized in writing by STMicroelectronics