ECE1396H Assignment 3

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A. MOSFET switch simulation and modelling

The plot of C_{gs}+C_{sb}, C_{gd}+C_{db}, C_{off} (defined as C_{gs}+C_{sb}+C_{gd}+C_{db}), R_{on}, are given in Fig. 1 and Fig. 2, corresponding to the case where MOSFET gate and substrate impedance is equal to 0.1Ω and $10k\Omega$, respectively. The FoM is defined as the product of C_{off} and R_{on}, and are plotted in Fig. 3 for both impedance scenarios. It can be seen that for higher gate and substrate impedance, FoM is smaller, therefore providing a faster switching time. This is the motivation behind using FDSOI where the substrate is insulator that has very high impedance.

B. Switched capacitor simulation and charge injection

Fig. 4 shows the clock signal that drives the transmission gates, where a 25% duty cycle is implemented and a 500 mV input signal is fed. Noted that for PMOS the clock signal is the inverted version of the NMOS clock signal. Fig. 5 shows the waveforms at input, 'store' node, and output. Fig. 6 shows the difference between the output and signal at the 'store' node. The maximum voltage error at the output is about 315 mV. Therefore, $Q = CV = (200pF)(-315mV) = -6.3 \times 10^{-11}C$. The output spectrum is given in Fig. 7 with PSS simulations conducted. The fundamental tone is with -7.5 dB and the third harmonic is with -27.4 dB, highest among all harmonics. Therefore, SDR is about 20 dB.

Increasing the transistor size (W) will decrease the on-resistance of the switch considering it operates in the triode region. However, it will aggregate the charge injection due to larger parasitic capacitance. Consider the channel charge of a NMOS transistor in triode region:

$$|Q_{ch,n}| = W_n L_n C_{ox,n}(V_{gs} - V_{t,n}) \tag{1}$$

Increasing W will generally increase the charge injection and therefore increase the error.

Error and SDR will be worse. Because transmission gate can be more effectively 'cancel' out the overlap parasitic capacitance of NMOS and PMOS if they are matched nicely. Consider the channel charge of a NMOS transistor in triode region:

$$\begin{aligned} |Q_{ch,p}| &= W_p L_p C_{ox,p}(V_{sg} - |V_{t,p}|) \\ \Delta V_0 &= -\frac{1}{2}\frac{|Q_{ch,n}| - |Q_{ch,p}|}{C_s} \end{aligned} \tag{2}$$

Therefore, by using transmission gate, the output error caused by the charge injection can be minimized, which is not achievable by using NMOS (or PMOS) only.

C. Discrete-time bandpass filter design

Define a second-order bandpass filter as

$$H(s) = -\frac{k_1 s}{s^2 + s\frac{w_0}{Q} + w_0^2} \tag{3}$$

Given input signal frequency is 180 MHz, defining the sampling clock frequency as 10 GHz. Therefore, the normalized input frequency is

$$w_0 = \frac{(2\pi)(180MHz)}{10GHz} = 0.113rad/sample \tag{4}$$

The frequency wrapper Ω_0

$$\Omega_0 = tan(\frac{w_0}{2}) = 0.056rad/s \tag{5}$$

Therefore, the transfer function H(z) (with a gain 0.8 at the center frequency and Q = 8)

$$H(z) = -\frac{0.8\frac{\Omega_0}{Q}s}{s^2 + \frac{w_0}{Q}s + \Omega_0^2} \tag{6}$$

After many tedious math steps

$$H(z) = -\frac{0.0055z^2 - 0.0055}{z^2 - 1.97z + 1.038} \tag{7}$$

Compared to the general H(z) given by

$$H(z) = -\frac{a_2 z^2 + a_1 z + a_0}{z^2 + b_1 z + b_0} \tag{8}$$

We get: $a_2 = 0.0055$, $a_1 = 0$, $a_0 = -0.0055$, $b_1 = -1.97$, $b_0 = 1.038$. Compared to the general H(z) given by:

$$H(z) = -\frac{K_3 z^2 + (K_1K_5 + K_2K_5 - 2K_3)z + (K_3 - K_2K_5)}{z^2 + (K_4K_5 + K_5K_6 - 2)z + (1 - K_5K_6)} \tag{9}$$

Letting $K_4 = K_5$, we get: $K_4 = K_5 = \sqrt{1 + b_0 + b_1} = 0.097$, $K_1 = (a_0 + a_1 + a_2)/K_5 = 0$, $K_3 = a_2 = 0.0055$, $K_2 = (a_2 - a_0)/K_5 = 0.115$, $K_6 = (1 - b_0)/K_5 = 0.112$. For implementation, in addition to K_1, we also neglect K_3 since it is way smaller than others, and we round the rest to 0.1. The circuit topology after simplification is in Fig. 8. By taking $C_1 = C_2 = 400fF$, the smallest capacitance is 40 fF, which is still implementable in 65 nm technology. The gate width of NMOS is 6 um, and length is 0.06 um. The two-phase non-overlap sampling clock duty cycle is 25%.

Given 500 mV input signal at 180 MHz, Fig. 9 shows the frequency response of the filter by running PAC simulations. The circuit has a center frequency around 160 MHz, with a 3 dB bandwidth 18.7 MHz, and a quality factor 8.47 is achieved by the circuit. The peak gain at the center frequency is -1.62 dB, which is 0.83 in linear scale. Therefore, all results are close to the asked specifications. The input and output waveforms of the filter are plotted in Fig. 10.

Fig. 11 shows the output spectrum of the two tone test (PSS). For 100 mV input signal, it is allocated at 180 MHz (f_1), and another 10 mV signal is at 200 MHz (f_2). The third order harmonic will be at $2f_1 - f_2$, and first harmonic will be at f_2. Fig. 12 shows the input-referred IIP3 plot, which is found at 2.73 dBm. Fig. 12 shows the Cadence schematic of the filter.

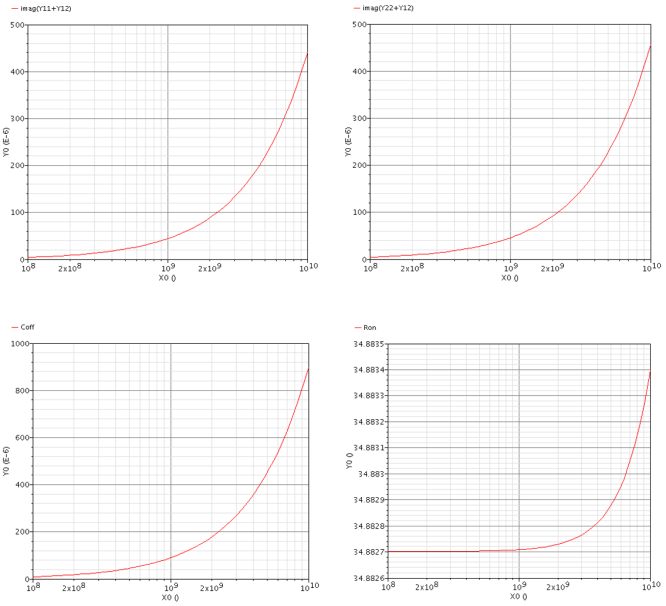

Fig. 1: Gate and substrate impedance is 0.1 Ω. Top left: C_{gs} + C_{sb}; top right: C_{gd} + C_{db}; bottom left: C_{off}; bottom right: R_{on}.

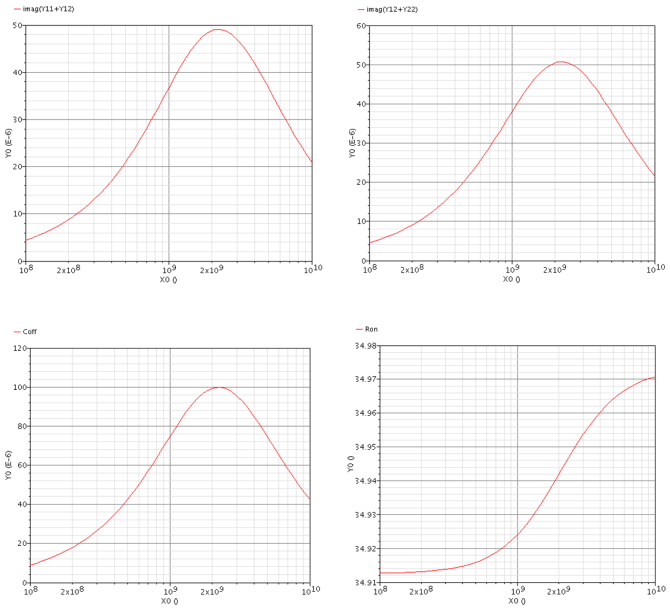

Fig. 2: Gate and substrate impedance is 10k Ω. Top left: C_{gs} + C_{sb}; top right: C_{gd} + C_{db}; bottom left: C_{off}; bottom right: R_{on}.

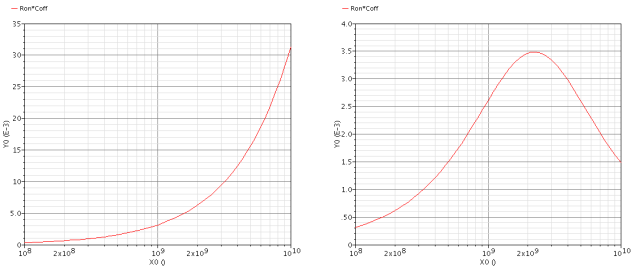

Fig. 3: $R_{on}C_{of}$. Left: gate and substrate impedance is 0.1 Ω; right: gate and substrate impedance is 0.1 Ω.

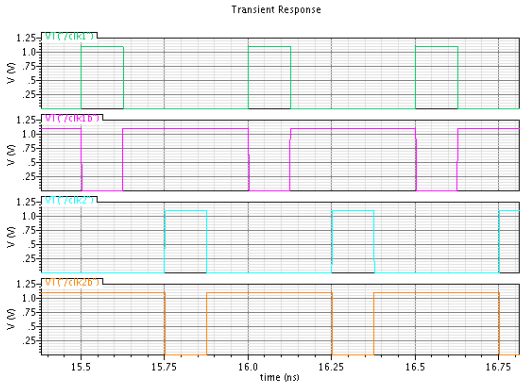

Fig. 4: Clocking signals fed to the transmission gates.

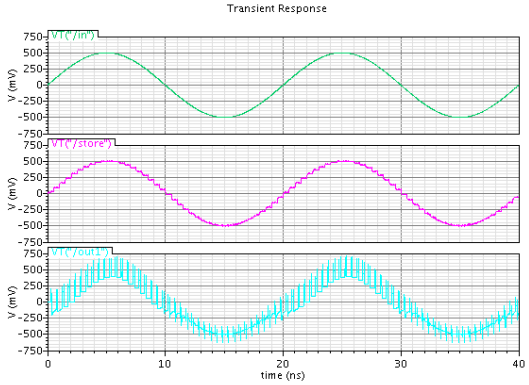

Fig. 5: Input, 'store' node, and output waveforms.

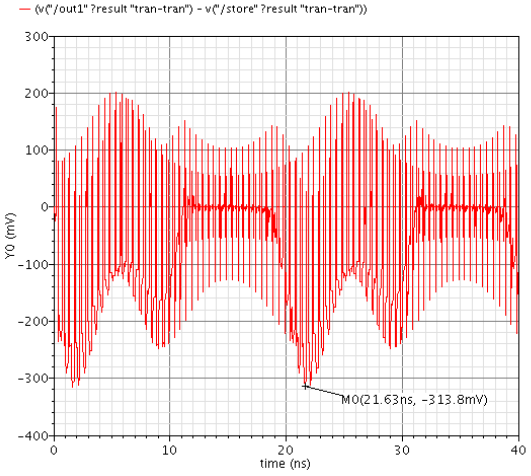

Fig. 6: Charge injection error.

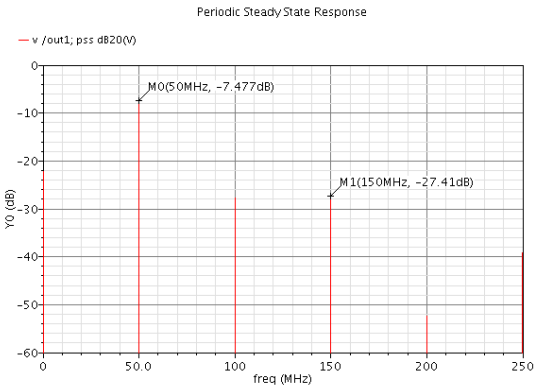

Fig. 7: Output spectrum after PSS simulation.

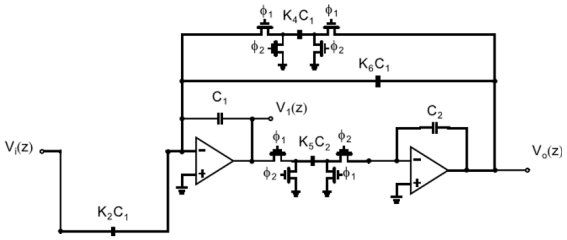

Fig. 8: Discrete-time biquad bandpass filter.

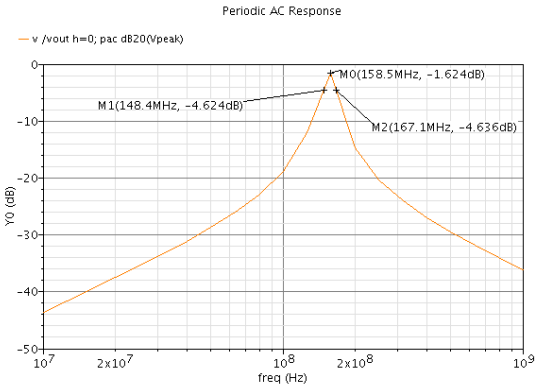

Fig. 9: Frequency response of the filter (PAC simulations).

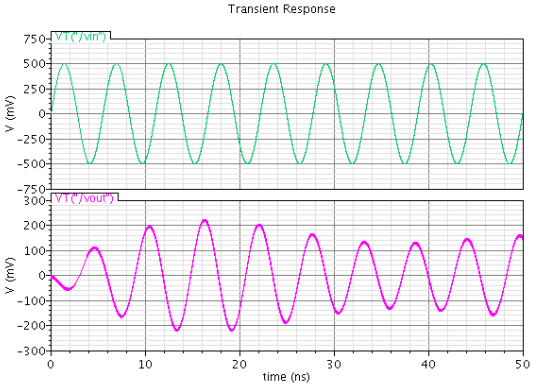

Fig. 10: Input and output waveforms of the switched capacitor bandpass filter.

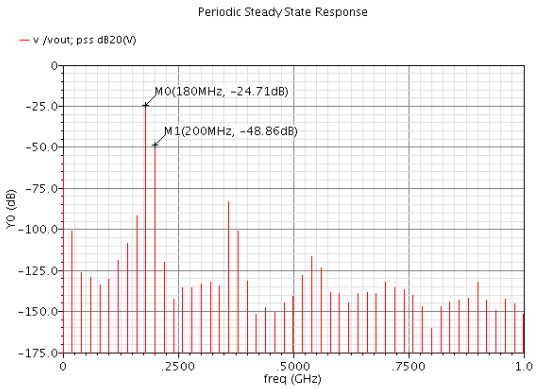

Fig. 11: Output spectrum of the filter in the two-tone test.

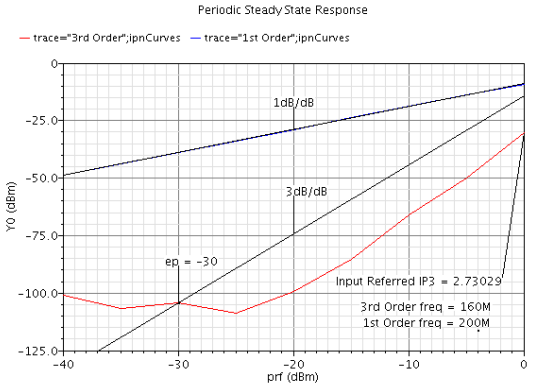

Fig. 12: Input-referred IIP3 plot of the two tone test.

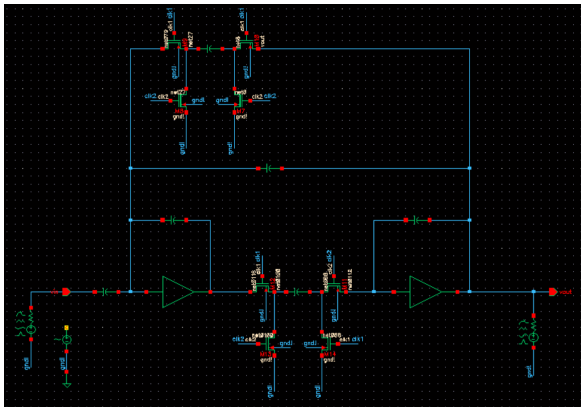

Fig. 13: Circuit schematic.