Assignment 2: Design of a low-noise phase locked loop

Objectives

- To learn how to develop a linear behavioural model of the phase vs. frequency and phase-noise vs. frequency characteristics of a PLL
- To design a low-phase noise 3rd order PLL.

1. Preparation:

Study the course material, Chapters 9 and 19 in the textbook and the course slides.

Read National Semiconductor Application Note 1001, William O. Keese, May 1996.

You may use *matlab*, *Cadence Verilog-A* or any programming language to model and design the PLL.

Cadence verilog-A PLL libraries can be modified to include phase noise if you choose that route.

To include the *pll* behavioural model libraries you must edit the cds.lib file in your design kit directory and add the following lines.

DEFINE pllLib $CDS_INST_DIR/tools/dfII/samples/artist/pllLib
DEFINE pllMMLib $CDS_INST_DIR/tools/dfII/samples/artist/pllMMLib

Save the cds.lib file and start the design kit.

2. Reference oscillator phase noise model (2 points)

Your crystal reference oscillator phase noise has a noise floor of -160 dBc/Hz at large frequency offset and a $1/f^2$ dependence elsewhere, with a phase noise of -140 dBc/Hz at 10 kHz offset.

Write the expression of the phase noise equation and determine the values of en_1, en_2, en_3 and kTF/P_{avs}.

Plot the $\mathcal{L}_{ref}$(f) characteristics in dBc/Hz vs. frequency using a logarithmic frequency axis.

3. Voltage-controlled oscillator phase noise model (2 points)

Your CMOS cross-coupled voltage-controlled oscillator phase noise has a noise floor of -140 dBc/Hz at large frequency offset and a $1/f^3$ dependence elsewhere. The VCO phase noise at 1MHz offset and K_{VCO} are specified in *Table* 1. Write the expression of the phase noise equation for your VCO and determine the values of en_1, en_2, en_3 and kTF/P_{avs}. Plot the $\mathcal{L}_{VCO}$(f) characteristics in dBc/Hz vs. frequency using a logarithmic frequency axis.

4. Third-order PLL design (16 points)

a) Find the divider ratio N, the charge pump current I_{CH} and the loop filter component values R, C_1 and C_2 such that the specification in *Table* 1 is satisfied (5 points)

b) Plot the magnitude (in dB) and phase response of the PLL loop gain in the phase domain (3 points).

c) Identify the 3dB bandwidth, the unity gain frequency, ω_t, and the phase margin (3 points).

d) Plot the $\mathcal{L}_{out}$(f) characteristics in dBc/Hz vs. frequency using a logarithmic frequency axis. Identify the main phase noise contributor at 1 MHz offset. (3 points).

e) Calculate the rms random jitter in ps and the rms phase error in degrees when the phase noise at the output of the PLL is integrated from 1 KHz to 100 MHz (2 points).

Table 1

Surname starts with	f_{osc} (GHz)	K_{VCO} [MHz/V]	L_{VCO}@1MHz	Lock time	f_{REF} (MHz)
A, B, C, D	1.9 - 2.1	250 MHz/V	-125 dBc/Hz	<20 µs	20 MHz
E, F, G, H,	0.9 – 1.0	150 MHz/V	-130 dBc/Hz	<10 µs	25 MHz
I, J, K, L	5.5 – 5.7	300 MHz/V	-120 dBc/Hz	<20 µs	20 MHz
M, N, O, P	27 – 28	1200 MHz/V	-106 dBc/Hz	<10 µs	20 MHz
Q, R, S, T	56 – 58	2200 MHz/V	-100 dBc/Hz	<5 µs	224 MHz
U,V,X,Y,Z	62 – 65	2200 MHz/V	-96 dBc/Hz	<20 µs	33.75 MHz

Supply voltage and control voltage is 1.1 V or lower.

Choose a single VCO frequency in the specified range with integer *N*.