10.8 A 56GS/s 6b DAC in 65nm CMOS with 256×6b Memory

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Modern optical systems increasingly rely on DSP techniques for data transmission at 40Gbs and recently at 100Gbs and above. A significant challenge towards CMOS TX DSP SoC integration is due to requirements for four 6b DACs (Fig. 10.8.1) to operate at 56Gs/s with low power and small footprint. To date, the highest sampling rate of 43Gs/s 6b DAC is reported in SiGe BiCMOS process [1]. CMOS DAC implementations are constraint to 12Gs/s with the output signal frequency limited to 1.5GHz [2-4]. This paper demonstrates more than one order of magnitude improvement in 6b CMOS DAC design with a test circuit operating at 56Gs/s, achieving SFDR >30dBc and ENOB>4.3b up to the output frequency of 26.9GHz. Total power dissipation is less than 750mW and the core DAC die area is less than 0.6×0.4 mm^2.

A critical element in CMOS DAC design at sampling rates *Fs* = 56Gs/s is a small footprint, so that the clock distribution and data path delays are minimized. In addition, short interconnect guarantees low load capacitance for the driver circuitry and further facilitates die size reduction with speed performance improvement. There are two key obstacles in circuit size reduction: circuit topology with relatively large devices (for an example, poly resistors in CML –style logic) and interconnect metal width. Minimum width is limited by electro-migration (EM) reliability rules. A CMOS logic topology with a minimum DC current in interconnects helps to reduce the EM factor. As a result, 56Gs/s 16:1 MUX circuitry is implemented using a combination of CMOS, pseudo-differential CMOS and transmission gate style of logic. Compactness of the 16:1 MUX design then requires clock phase alignment solution to provide the MUX with precise timing, similar to the phase calibration described in [4].

DAC architecture (Fig. 10.8.2) contains a 256×6b data memory with control register, 16:1 MUX, DAC current-steering matrix, DAC current sources, and finally clock generation and phase alignment block. The memory size provides DAC output data pattern length programmability up to 256b at 56Gs/s; sufficient for time domain 256b PRBS, or frequency domain 256-points FFT testing, such as SFDR and ENOB. The DAC current-steering structure combines two segments: 15 thermometer- encoded MSBs and 2 binary LSBs; there are 17 current sources and current-steering switches in total. Thermometer encoding improves DAC linearity and minimizes output glitch energy [5]. The 4b to 2b split in segmentation provides a balance between circuit complexity and DAC overall performance. There are different techniques to generate the remaining binary-weighted LSBs currents across the on-chip 50Ω load [4,6,7]. Two last solutions prevent the use of series inductive peaking (L1 in Fig. 10.8.2) with 50Ω load at the output. This is why the DAC uses binary-weighted currents of *Io/2* and *Io/4*, where *Io* is the unary current value. The DAC full scale single-ended output current, *FS*= *15.75·Io*. All 17 currents are generated in the DAC current sources block with 2.5V thick oxide devices. Currents are matched so they don't impair the 6b DAC DC-linearity performance. The current sources block is remotely located in the layout freeing-up space for the 56Gs/s current switches combined with the 2:1 MUX circuit (MUX-CS block in Fig. 10.8.2).

The DAC 16:1 MUX structure is similar to the one described in [4]. The DAC current-steering circuit (MUX-CS in Fig. 10.8.2) combines 2:1 MUX and a 56Gs/s current switch cell (Fig. 10.8.3). The 2:1 MUX is based on CMOS transmission gate logic. The current switch is a PMOS differential pair (M2, M3), isolated with a cascode transistor M1. That configuration makes switching performance insensitive to the interconnect length at the current input *Io* (*Io/2* or *Io/4*). The M1 gate voltage, *Vcs*, is set to guarantee reliability with maximum gate oxide and drain-source voltages. *Vcs* is critical only with regards to the required output voltage swing that is typically 300mV per differential side. The MUX-CS timing (see Fig. 10.8.3) is precisely tuned with 14GHz phase rotator located in the clock generation block. The DAC employs eight identical 4-15b binary to thermometer encoders, incorporated in a 6b to 17b encoder block (Fig. 10.8.4 left). The thermometer part is B2THERM block with 4MSBs input and 15 outputs. This block uses a similar approach as described in [8]. The two LSBs at the bottom are co-located in this block for exact delay matching at the output. The pseudo-differential 14Gs/s flip-flop in the 4:2 MUX is based on a latch (Fig. 10.8.4 right) that is a modified NMOS-only version of circuit [9]. A third logic level (SEL, SELB) is introduced to multiplex the inputs, while additional two inverters at the outputs (Q, QB) improve fan-out at required speed.

The DAC is characterized on-wafer with test platform interconnect bandwidth in excess of 40GHz. Time-domain and frequency-domain characteristics are both measured with Agilent digital scope equipped with 50GHz sampling heads and low-jitter synchronization option. Calibration of 28GHz reference clock source showed that its noise performance exceeds 7b. The 256b PRBS pattern is programmed via PC interface into the data memory, and then cyclically read to observe 56Gb/s eye (Fig. 10.8.5). The DAC offers an ability to pre-compensate the pattern for the frequency loss at its output before it reaches the sampling scope. The upper plot in Fig. 10.8.5 is obtained with no frequency compensation, while the bottom one with 10% single-pole pre-emphasis at 28GHz. In both cases the eye is wide open and symmetric despite no final re-timing operation at 56Gs/s. For the frequency domain measurements, the 256b memory is programmed to synthesize DAC output frequency, *fo=prime* (*Fs*/256), where *prime* is a prime number. The output is captured with 4× oversampling by digital scope and post-processed with 1K-FFT to obtain SFDR, ENOB (Fig. 10.8.6). The DAC ENOB is computed similarly to an ADC, where SNDR would represent all "noise and distortion" spectral components in the specified bandwidth. The ENOB and SFDR is > 5.9b and 42dBc respectively at frequencies below 1GHz, and then reduced to 4.3b and 30dBc at frequencies approaching 26.9GHz. In the frequency range close to 10GHz, ENOB >5b and SFDR > 38dBc.

The DAC is fabricated in a 65nm CMOS technology. Figure 10.8.7 shows a die micrograph of the DAC and summary of on-wafer measured performance. The DAC core occupies 600×400mm^2 area. The metal to metal and MOS decoupling capacitors are extensively used for power supply filtering, as well analog and digital parts of the circuit are powered separately. In 56Gbs/s pattern-generation mode and 400mVpp differential output eye amplitude, power dissipation including the memory is < 750mW from a dual 1.1V/2.5V supply.

Acknowledgements:
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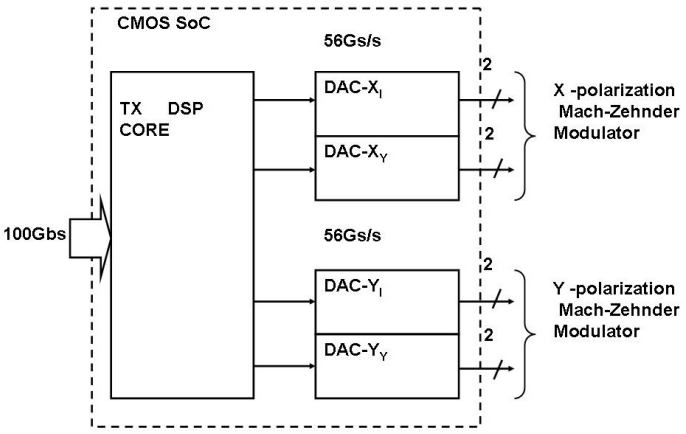

Figure 10.8.1: TX DSP SoC architecture for optical DP QPSK.

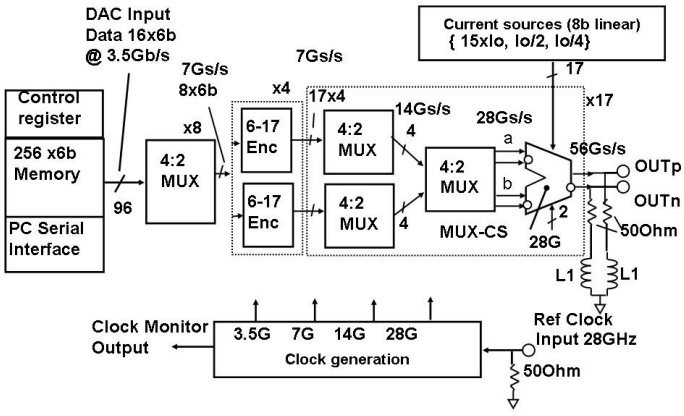

Figure 10.8.2: DAC architecture with 256×6b data memory.

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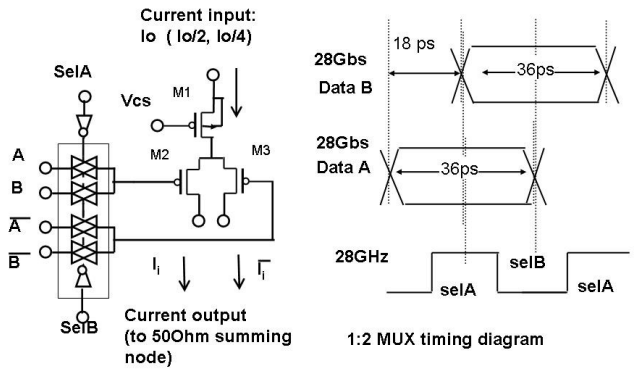


Figure 10.8.3: Unit current steering cell with 2:1 MUX.

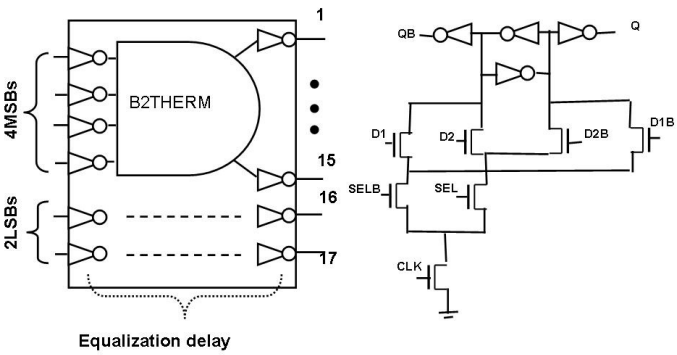


Figure 10.8.4: Block diagram of 6b to 17b encoder (left) and 14GHz 2: 1 MUX latch (right).

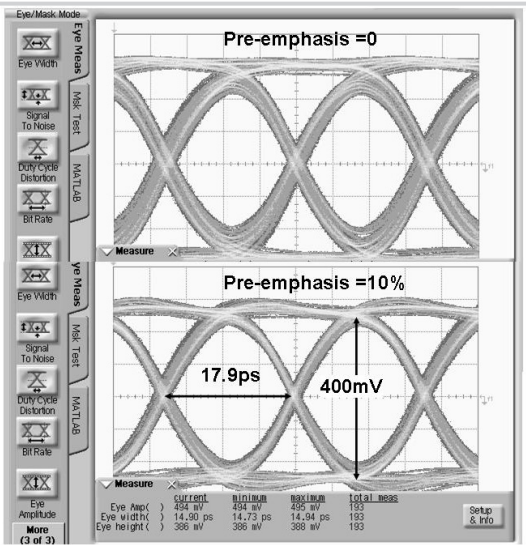


Figure 10.8.5: 56Gb/s 256b PRBS eye with 0% (top) and 10% (bottom) pre-emphasis @28GHz.

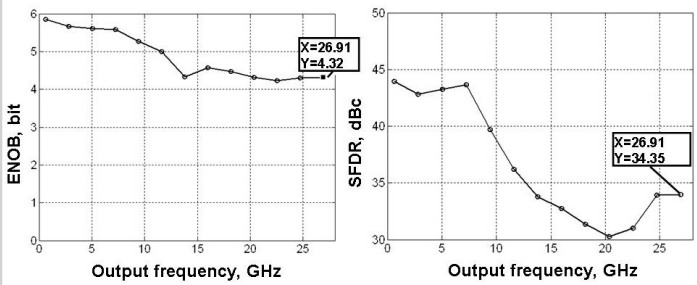
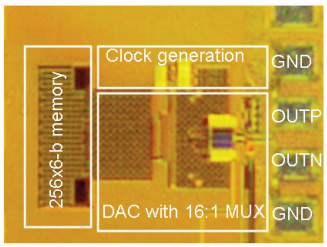


Figure 10.8.6: ENOB and SFDR versus output frequency at Fs=56GHz.



DAC on-wafer performance

Resolution	6b
Conv. Rate Output Freq	56 GS/s 26.9 GHz
Full scale	Nom 0.6 V diff.
ENOB F_{out} < 1GHz F_{out}< 10 GHz F_{out}< 26.9GHz	 > 5.9b > 5b > 4.3b
SFDR F_{out}< 10 GHz F_{out}< 26.9GHz	 38 dBc 30 dBc
Power	≤ 0.75 W
DAC core	0.6 x 0.4 mm^2
Process	65nm CMOS

Figure 10.8.7: DAC die micograph with test circuitry and performance summary

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