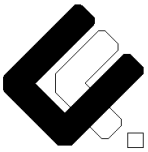
CMOS065
Interconnects Parasitic Capacitances Modeling

C065 ICM 4.0

UNICAD2.4 / February 16, 2006



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A complete list of trademark names appears in a separate "Trademark information" document

1. GENERAL PRESENTATION

1.1 Purpose

This document is aimed at providing **CMOS065** designers with raw data related to interconnects parasitic capacitances.

Such raw data, applicable to specific **CMOS065** layout configurations only, can be used by designers to derive estimated absolute values for wire parasitic capacitances.

1.2 Scope

Any designer using the **CMOS065** 7m4x0y2z or 6m4x0y1z process can use this document.

This document is dedicated to lp option. For gp option, poly values may differs.

It must be noted that the obtained absolute values must be used for estimation only; only the extraction of interconnects parasitic through dedicated CAD tools, supported in the corresponding **UNICAD** platform, can be used for sign-off verifications.

1.3 Reference Documents

Based on **DRM CMOS065 rev D**.

1.4 Definitions

- **BUS**: set of parallel wires in the same metal layer: width and space values are common to all wires.
- **COUPLING CAPACITANCE**: each individual component of the capacitance matrix (one capacitance value between each pair of wires in the considered design).
- **GROUND PLANE**: metal shape whose dimensions are large enough so that it can collect any field line going from a wire drawn in an upper metal layer towards substrate.
- **ISOLATED LINE**: wire in a specific metal layer without surrounding wires in the same metal layer (or without any surrounding wire in a close neighbourhood)
- **LUMPED CAPACITANCE**: sum of each individual component of the capacitance matrix, i.e. sum of all contributions lumped to ground.
- **PLATE**: metal shape whose dimensions are larger than any actual wire in a design.

- **IMD**: Inter Metal Dielectric. This is the dielectric beetween two consecutives metals level.

1.5 General

It is the objective of this document to provide designers with representative interconnects parasitic capacitances data, as well as data related to process corners (e.g. min or max. values for timing analysis).

This release of the document contains only **typical process values.**

All values and data presented in this document have been extracted from dedicated layout test cases using the **QUICKCAP** field solver for interconnects parasitic extraction (Release 4.1).

1.6 Safety Requirements

This document is classified “Company Internal“.

1.7 Quality Requirements

Adherence to the requirements stated in this document

1.8 Environmental / Ecological Requirements - N/A

2. CMOS065 INTERCONNECTS PARASITIC CAPACITANCE MODELING DATA

3 structures have been selected to represent the main routing layout configurations. Those structures have been extracted for min width of lines.

Please refer to paragraph "PROCES PARAMETERS" of **CMOS065** DRM revision **D** to see typical cross section of the process.

To be consistent with standard design flow, the dedicated layout test-case have been modified according to the "Isolated lines retargeting" procedure describes in the document RADCS # R009441 as mentioned in the **CMOS065** DRM revision **D**

2.1 Isolated line above a ground plane: "best design case"

This structure (see Figure 1) represents the ‘’best design case” for a line i.e. a reduced coupling environment. To evaluate the impact of the distance (H) we present the lumped capacitance for each metal combination.

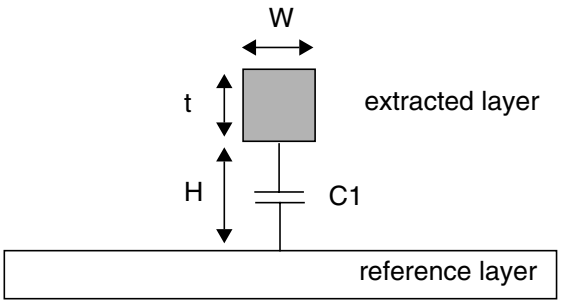

Figure 1: Best design case structure

As a general rule, the capacitance decreases when the distance H to the reference plane increases. We can look at 3 cases:

- M1 to M5X: the capacitance decreases when the distance H to the reference plane increases.
- M6Z: due to larger width of the lines, the lumped capacitance is larger than for M1 to M5X in most of the cases
- M7Z: the high altitude of M7Z level compensate the large width of the lines.

Clumped[fF/um]	Reference Layers							
Ext.Layer	PWELL	PO	M1	M2X	M3X	M4X	M5X	M6Z
M7Z	0.067	0.068	0.070	0.074	0.077	0.083	0.090	0.148
M6Z	0.076	0.078	0.083	0.091	0.100	0.115	0.149	
M5X	0.053	0.056	0.059	0.065	0.077	0.122		
M4X	0.053	0.056	0.062	0.073	0.116			
M3X	0.056	0.062	0.072	0.116				
M2X	0.063	0.074	0.115					
M1	0.077	0.117						
PO	0.094							

Table 1:Best design case lumped capacitance in fF/um

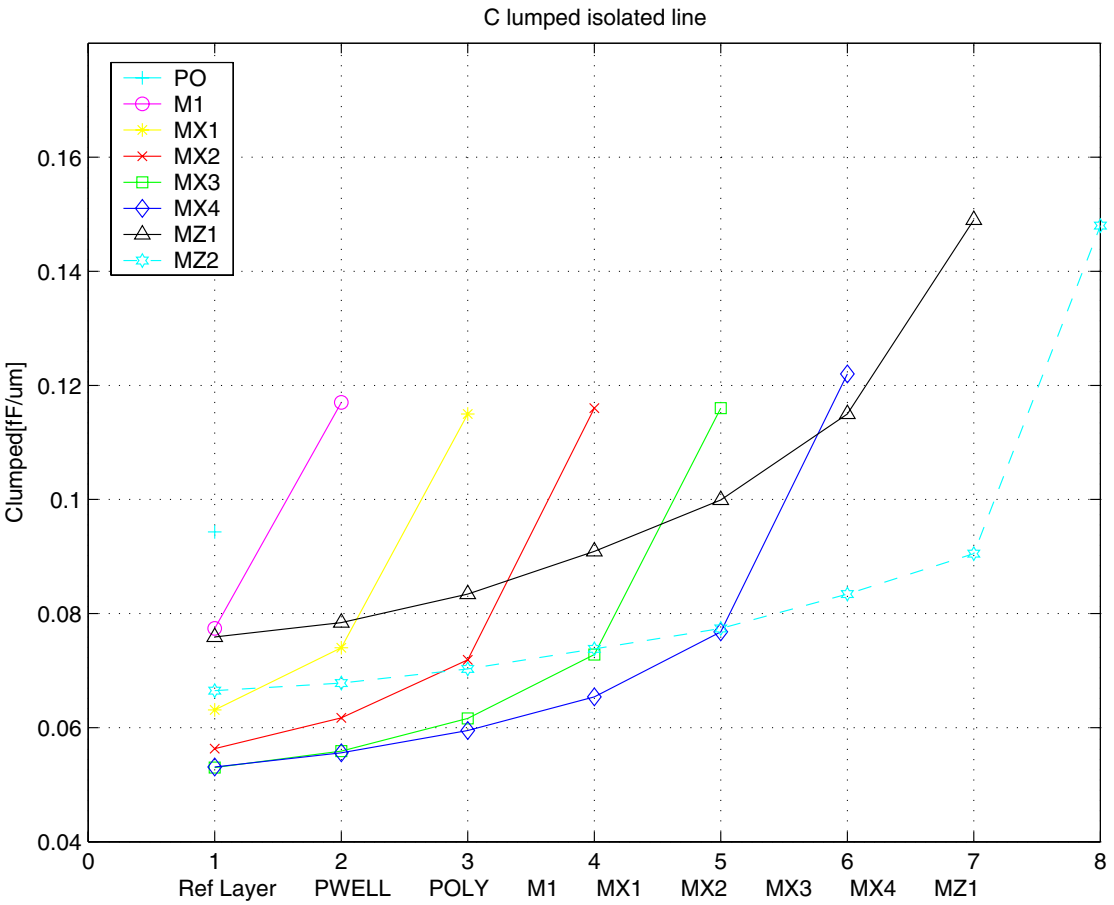

Figure 2: Best design case lumped capacitance in fF/um

2.2 Isolated line above a ground plane and below a M6Z or M7Z plate

This case completes the previous one. A fixed top metal plane (built in M6Z or M7Z) is added to represent the usual power grid (see Figure 3). The 2 following subsections respectively present cases with M6Z and M7Z top grid.

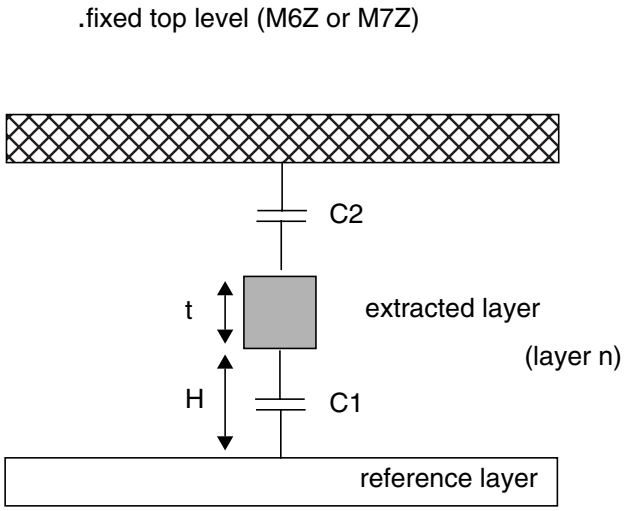

Figure 3: Isolated line with power grid structure

2.2.1 M6Z plate on top level

- Lumped Capacitance

  The global behavior of this structure is the same as the isolated line: the capacitance decreases when H increases. Nevertheless, due to the top plane the lumped capacitance of this structure is larger. This is especially true for the M5X, which exhibits the strongest capacitance. In this last case, the strong capacitance due to closed M6Z power grid controls the behavior.

Clumped[fF/um]	Reference Layers					
Ext.Layer	PWELL	PO	M1	MX1	MX2	MX3
MX4	0.083	0.083	0.085	0.089	0.095	0.134
MX3	0.068	0.069	0.072	0.080	0.121	
MX2	0.064	0.068	0.077	0.118		
MX1	0.068	0.077	0.116			
M1	0.080	0.117				
PO	0.095					

Table 2:M6Z top plate - Lumped capacitance in fF/um

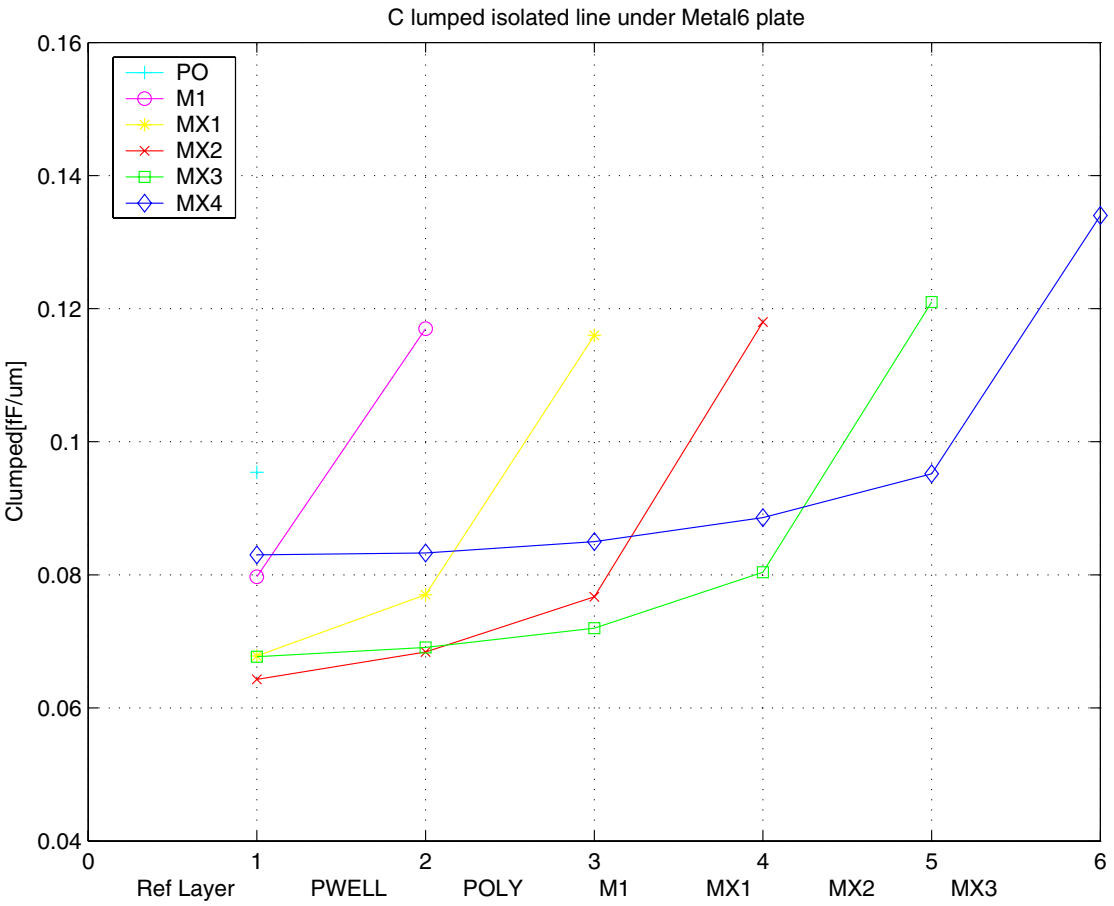

Figure 4:M6Z top plate - Lumped capacitance in fF/um

- Coupling capacitances

  Conclusion about the bottom capacitance behavior is the same as for the isolated line: C1 decreases when the distance to the reference plane H increases (see Table 3 and Figure 5). Nevertheless, compared to the isolated line, C1 has lower values. This is due to the top power grid, which captures a part of the field lines. see Table 4 and Figure 6 illustrate the top capacitance evolution. By compensation effect, the top capacitance decreases, as the reference plane is closer to the extracted level. So, M5X has the strongest C2 value.

  Relative evolution of the top and the bottom capacitances illustrates the field lines sharing between each element of the environment.

C1[fF/um]	Reference Layers					
Ext.Layer	PWELL	PO	M1	MX1	MX2	MX3
MX4	0.017	0.019	0.023	0.030	0.043	0.092
MX3	0.024	0.028	0.035	0.048	0.096	
MX2	0.032	0.039	0.052	0.100		
MX1	0.044	0.057	0.102			
M1	0.062	0.105				
PO	0.085					

Table 3:M6Z top plate - Bottom coupling capacitance C1 in fF/um

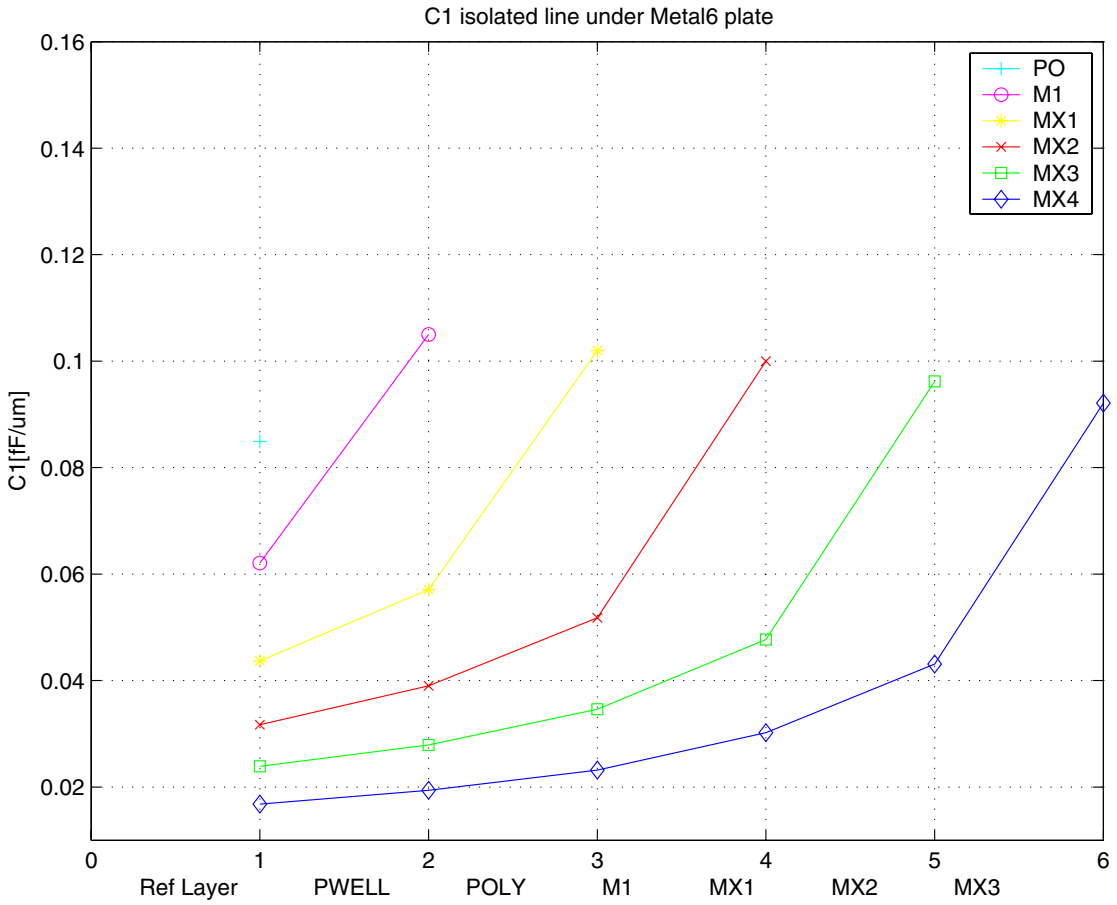

Figure 5:M6Z top plate - Bottom coupling capacitance C1 in fF/um

C2[fF/um]	Reference Layers					
Ext.Layer	PWELL	PO	M1	MX1	MX2	MX3
MX4	0.066	0.064	0.062	0.058	0.052	0.041
MX3	0.044	0.042	0.038	0.033	0.025	
MX2	0.033	0.030	0.025	0.018		
MX1	0.024	0.020	0.015			
M1	0.018	0.012				
PO	0.011					

Table 4:M6Z top plate - Top coupling capacitance C2 in fF/um

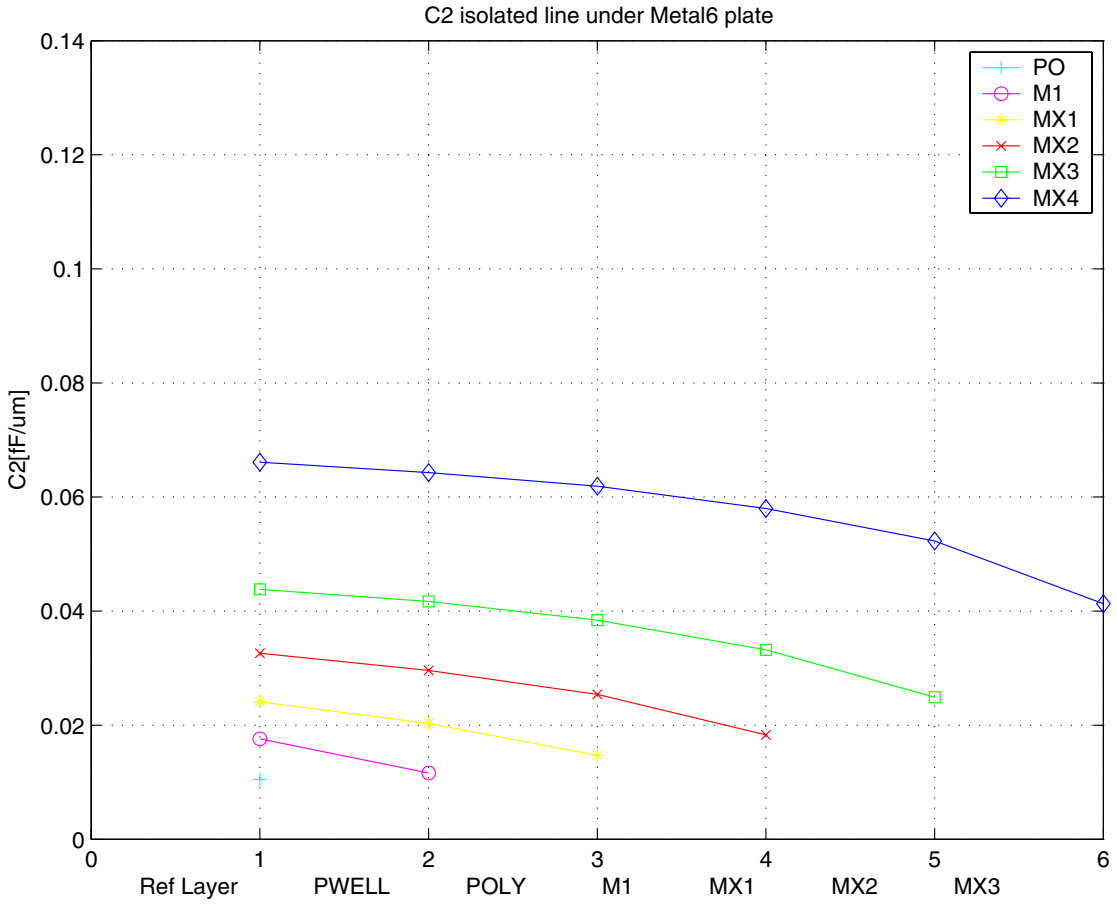

Figure 6:M6Z top plate - Top coupling capacitance C2 in fF/um

2.2.2 M7Z plate on top level

This structure uses the same principle as the previous one. The only difference is the top grid, which is built in M7Z instead of M6Z. So the same conclusions are valid. Due to the larger width of the M6Z lines, the lumped and coupling capacitances for M6Z is larger than for M1 to M5X.

- Lumped capacitance

Clumped[fF/um]	Reference Layers						
Ext.Layer	PWELL	PO	M1	MX1	MX2	MX3	MX4
MZ1	0.156	0.156	0.159	0.162	0.168	0.178	0.205
MX4	0.062	0.064	0.066	0.071	0.081	0.123	
MX3	0.059	0.061	0.065	0.075	0.117		
MX2	0.060	0.064	0.074	0.117			
MX1	0.065	0.075	0.116				
M1	0.079	0.117					
PO	0.095						

Table 5:M7Z top plate - Lumped capacitance in fF/um

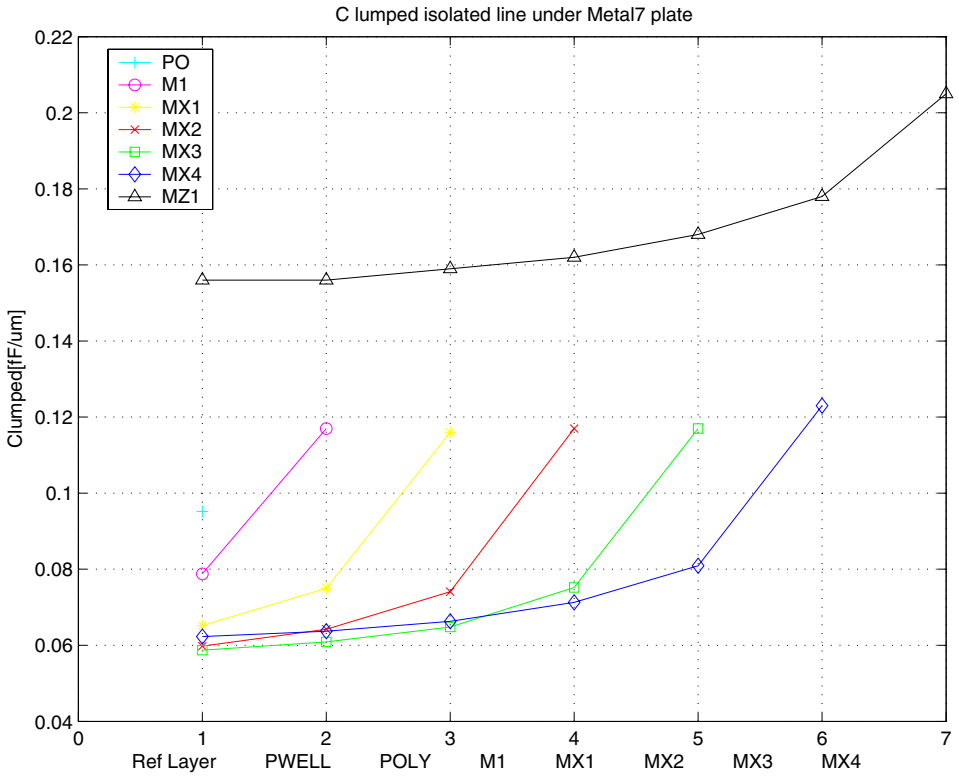

Figure 7: M7Z top plate - Lumped capacitance in fF/um

- Coupling capacitances

C1[fF/um]	Reference Layers						
Ext.Layer	PWELL	PO	M1	MX1	MX2	MX3	MX4
MZ1	0.028	0.032	0.035	0.042	0.051	0.068	0.100
MX4	0.027	0.030	0.035	0.043	0.058	0.107	
MX3	0.032	0.036	0.043	0.057	0.105		
MX2	0.038	0.045	0.058	0.106			
MX1	0.049	0.062	0.107				
M1	0.066	0.109					
PO	0.088						

Table 6:M7Z top plate - Bottom coupling capacitance C1 in fF/um

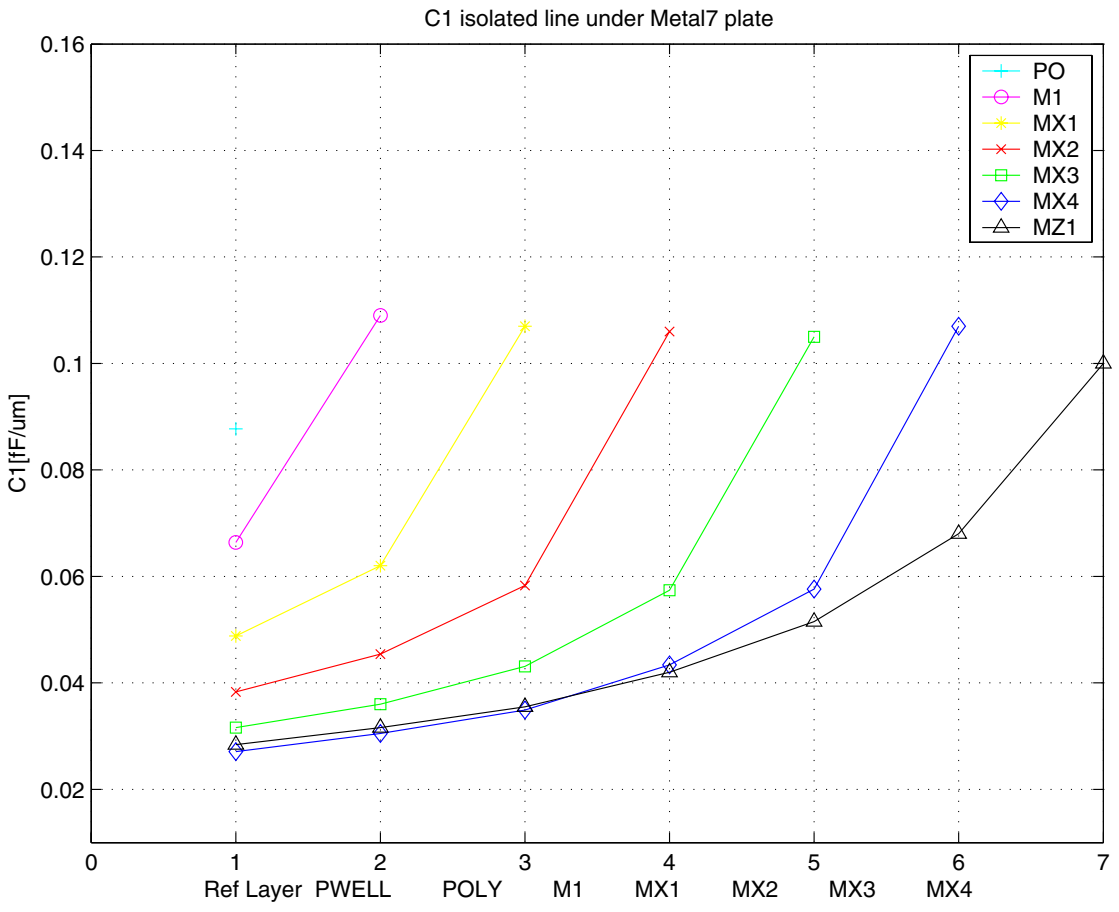

Figure 8:M7Z top plate - Bottom coupling capacitance C1 in fF/um

C2[fF/um]	Reference Layers						
Ext.Layer	PWELL	PO	M1	MX1	MX2	MX3	MX4
MZ1	0.128	0.125	0.123	0.120	0.116	0.111	0.103
MX4	0.035	0.033	0.031	0.028	0.023	0.016	
MX3	0.027	0.025	0.022	0.018	0.013		
MX2	0.021	0.019	0.016	0.011			
MX1	0.016	0.013	0.009				
M1	0.012	0.007					
PO	0.007						

Table 7:M7Z top plate - top coupling capacitance C2 in fF/um

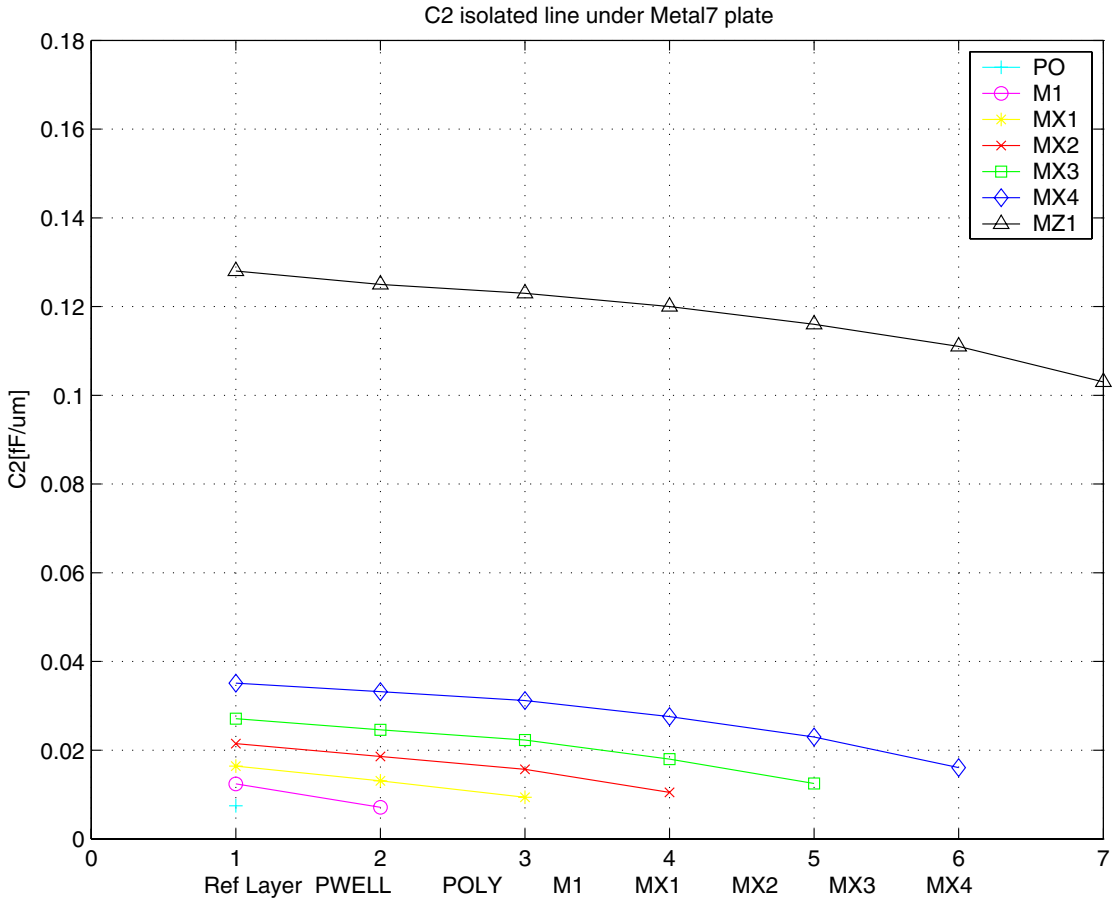

Figure 9:M7Z top plate - top coupling capacitance C2 in fF/um

2.3 Coupled lines between two buses: "realistic worst case"

This structure represents a realistic design worst case: the extracted bus is embedded between 2 perpendicular buses (top & bottom).

The top and bottom buses are drawn with the next upper and next lower metal level. (see Figure 10). Take care that M1 is confined between PO and M2X buses.

Furthermore, the top and bottom buses cover the total length of the extracted bus.

In the tables below, the capacitances related to the central line of the embedded bus (in black on Figure 10) are presented.

2.3.1 Bus1: top & bottom buses with fixed space

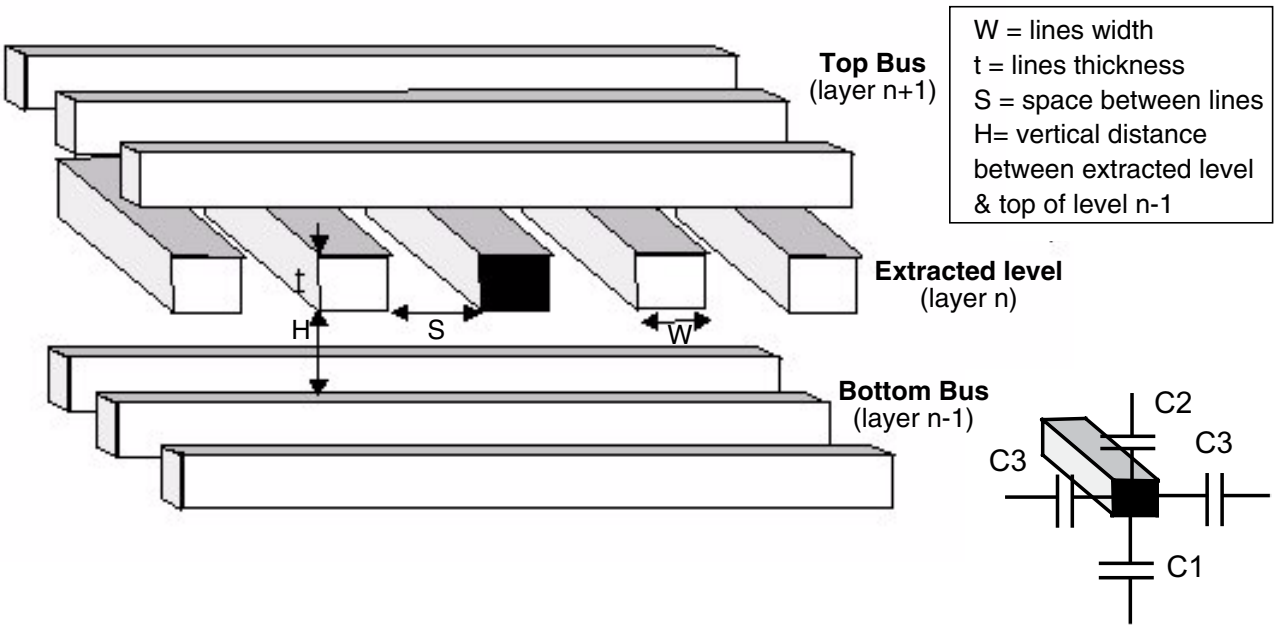

Figure 10: Bus1 configuration

- Description
  - Minimum width is applied for extracted level, lower and upper buses
  - Minimum space is fixed for lower and upper buses
  - Space of the extracted level varies from 1x min. space to 3x min. space The following table gives the space (design) values used for each extracted level.

space[um]	Level					
n	M1	MX1	MX2	MX3	MX4	MZ1
1	0.09	0.1	0.1	0.1	0.1	0.4
1.5	0.135	0.15	0.15	0.15	0.15	0.6
2	0.18	0.2	0.2	0.2	0.2	0.8
2.5	0.225	0.25	0.25	0.25	0.25	1
3	0.27	0.3	0.3	0.3	0.3	1.2

Table 8:Bus 1 design space values (*n = multiple of the minimum space)

Note: On layout, width and space values are typical but an oversizing is applied during extraction step to represent silicon real values. It leads to larger w and smaller s.

As illustrated by Figure 10, only capacitances related to the central line (in black on Figure 10) are represented.

Following charts show lumped capacitance variations vs. space for each metal level.

- Lumped capacitance

Clumped[fF/um]	Extracted Level					
n	M1	MX1	MX2	MX3	MX4	MZ1
1.0	0.203	0.191	0.192	0.191	0.181	0.260
1.5	0.179	0.177	0.173	0.174	0.160	0.228
2.0	0.173	0.166	0.168	0.168	0.151	0.218
2.5	0.170	0.164	0.163	0.163	0.146	0.209
3.0	0.166	0.160	0.162	0.160	0.140	0.207

Table 9:Bus1 Lumped capacitance vs. space in fF/um

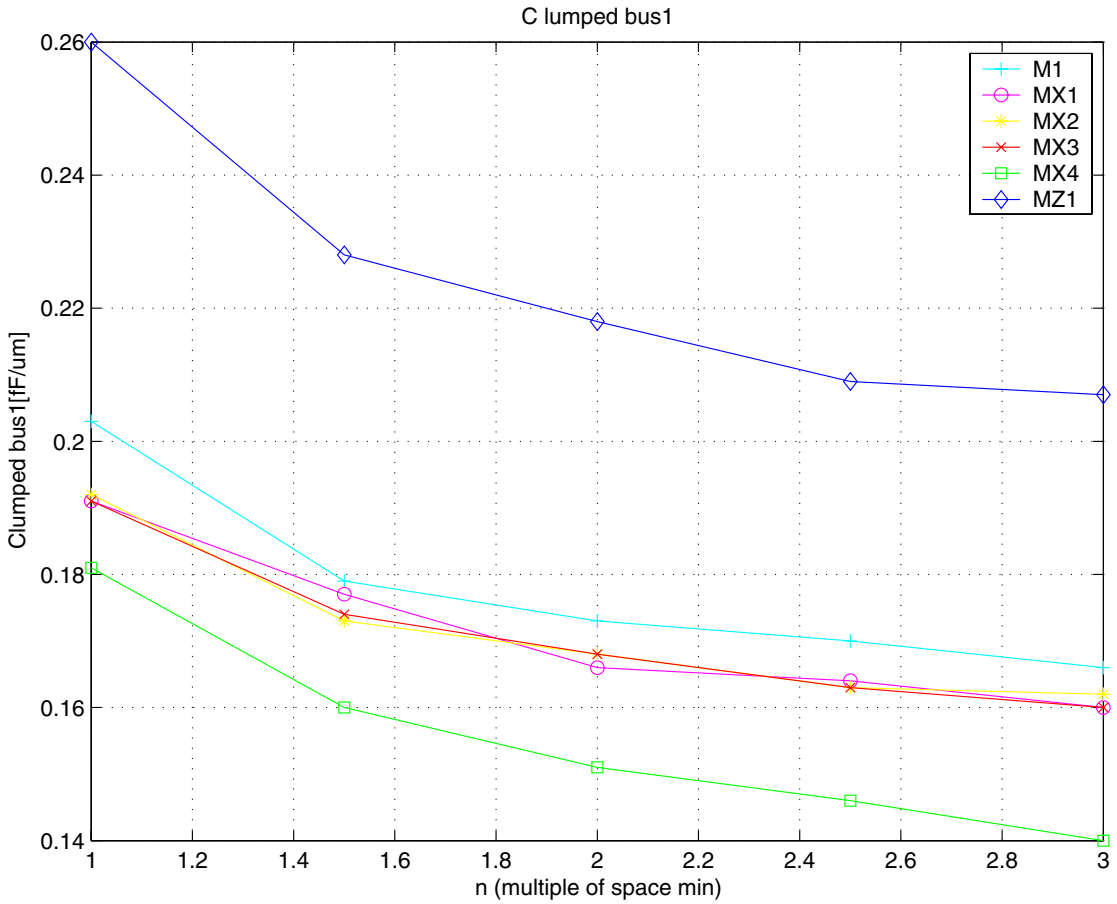

Figure 11: Bus1 Lumped capacitance vs. space in fF/um

As expected, the lumped capacitance decreases with the space and converges to a constant value. So, in this case a compromise can be found between capacitance reduction and integration. We define a figure of merit (g) as the ratio between the capacitance reduction and the multiple of the space:

g = R / n with R= % of reduction from min. space (n=1) to current space (n=1.5 to 3)

An optimum is defined as the absolute maximum value of g.

see Table 10 illustrates evolution of the optimum and shows that n between 1.5 and 2 is the best compromise between integration and lumped capacitance reduction. see Table 11 illustrates the capacitance reduction for n=2.

g	**%**					
n	M1	MX1	MX2	MX3	MX4	MZ1
1.0	0.0	0.0	0.0	0.0	0.0	0.0
1.5	-7.9	-4.9	-6.6	-5.9	-7.7	-8.2
2.0	-7.4	-6.5	-6.2	-6.0	-8.3	-8.1
2.5	-6.5	-5.7	-6.0	-5.9	-7.7	-7.8
3.0	-6.1	-5.4	-5.2	-5.4	-7.6	-6.8

Table 10:Figure of merit for C lumped reduction

R%	**M1**	**MX1**	**MX2**	**MX3**	**MX4**	**MZ1**
n						
2.0	-14.8	-13.1	-12.5	-12.0	-16.6	-16.2

Table 11:Percentage of Lumped capacitance reduction between n=1 and n=2

Sharing capacitances vs. metal level have to be detailed:

In **CMOS065** technology due to a similar environment, all capacitances related to M2X, M3X and M4X are nearly identical (see see Table 9).

M1 case exhibit slightly higher lumped capacitances than M2X, M3X & M4X ones. The smaller width of M1 and PO lines and the higher thickness of PO/M1 dielectric will tend to decrease the lumped capacitance. But these effects are compensated by the higher permittivity of the PO/M1 dielectric stack (nitride + oxide) and by the bottom lateral M1 nitride.

M5X case exhibit higher capacitances than M4X, M3X & M2X ones. The higher thickness of M5X/M6Z oxide will tend to decrease the lumped capacitance. But this effect is compensated by the higher permittivity of the M5X/M6Z dielectric, by the larger width of the M6Z lines and by the bottom lateral M6Z nitride.

M6Z case exhibit higher capacitances than all others. It is due to the larger width of the M6Z and M7Z lines and to the M6Z and M7Z bottom lateral nitride.

- Lateral Coupling Capacitances

As observed on the lumped capacitance, the lateral capacitance C3 severely decreases with the space. In this case, the convergence value will be zero for an infinite space. Nevertheless, for the optimum value observed on Clumped (n=2) the coupling capacitance is roughly divided by 2.

M1 case exhibit slightly higher lateral coupling capacitances (C3) than M2X, to M4X ones. The smaller height of M1 lines will tend to decrease the lateral coupling capacitance (C3). But this effect is compensated by the bottom lateral M1 nitride and by the smaller min space.

M5X lateral coupling capacitance (C3) is also slightly higher than for M2X to M4X level. This is due to the high distance between M5X and top M6Z bus that will favor M5X lateral coupling capacitance (C3) and to the higher thickness of the nitride on top of M5X.

M6Z lateral coupling capacitance (C3) is also slightly higher than for M2X to M4X level. Some parameters will favor M6Z lateral coupling capacitance:
- the higher height of M6Z lines.
- the higher thickness of M6Z/M7Z dielectric.
- the higher thickness and permittivity of the nitride on top of M6Z.
- the M6Z bottom lateral nitride.

Some parameters will unfavor M6Z lateral coupling capacitance:
- the large space between M6Z lines.

C3[fF/um]	Extracted Level					
n	M1	MX1	MX2	MX3	MX4	MZ1
1.0	0.093	0.081	0.079	0.080	0.089	0.112
1.5	0.064	0.056	0.055	0.055	0.064	0.071
2.0	0.052	0.041	0.042	0.041	0.050	0.049
2.5	0.042	0.031	0.031	0.031	0.041	0.036
3.0	0.033	0.023	0.023	0.024	0.034	0.026

Table 12:Bus1 lateral coupling capacitance vs. space: C3 in fF/um

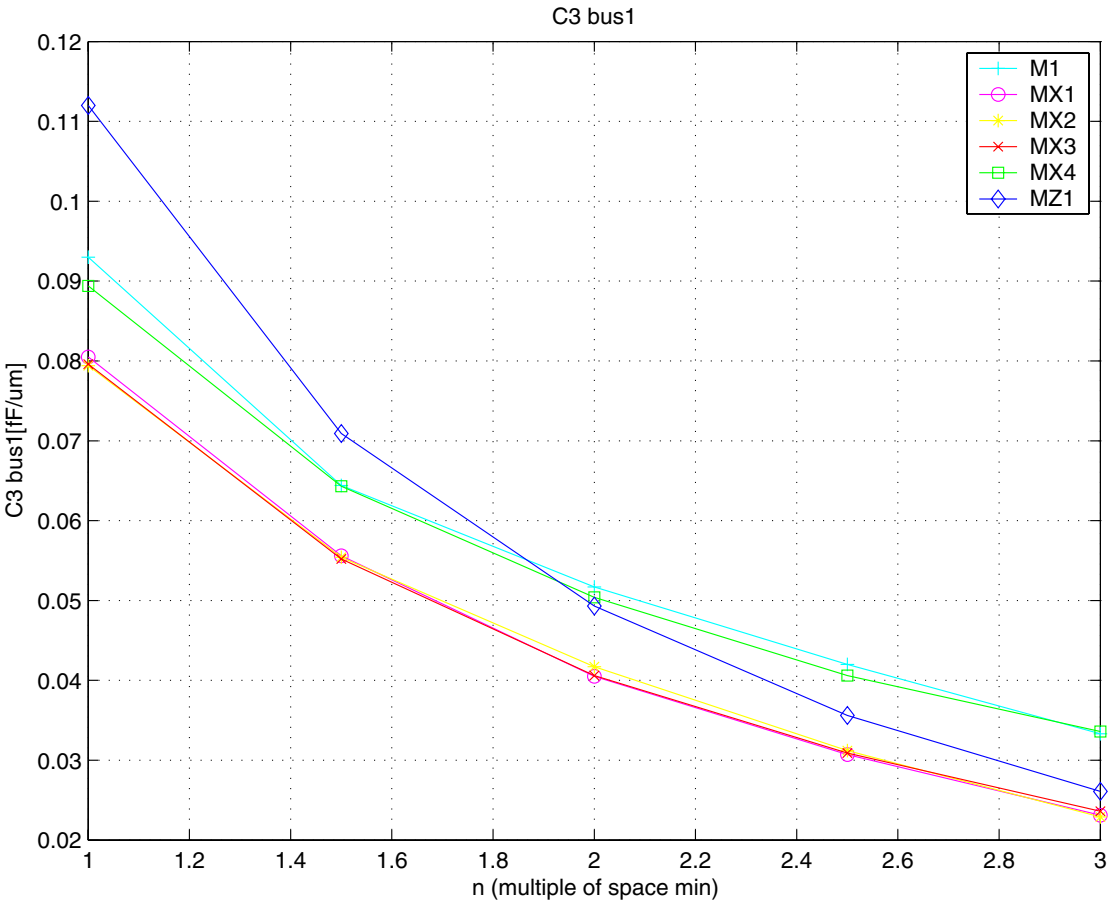

Figure 12:Bus1 lateral coupling capacitance vs.space: C3 in fF/um

- Vertical Coupling Capacitances

C1[fF/um]	Extracted Level					
n	M1	MX1	MX2	MX3	MX4	MZ1
1.0	0.052	0.055	0.055	0.055	0.062	0.074
1.5	0.055	0.059	0.058	0.059	0.065	0.078
2.0	0.059	0.062	0.062	0.062	0.069	0.084
2.5	0.061	0.066	0.064	0.065	0.072	0.086
3.0	0.065	0.068	0.068	0.068	0.074	0.091

Table 13:Bus1 bottom vertical coupling capacitance vs. space: C1 in fF/um

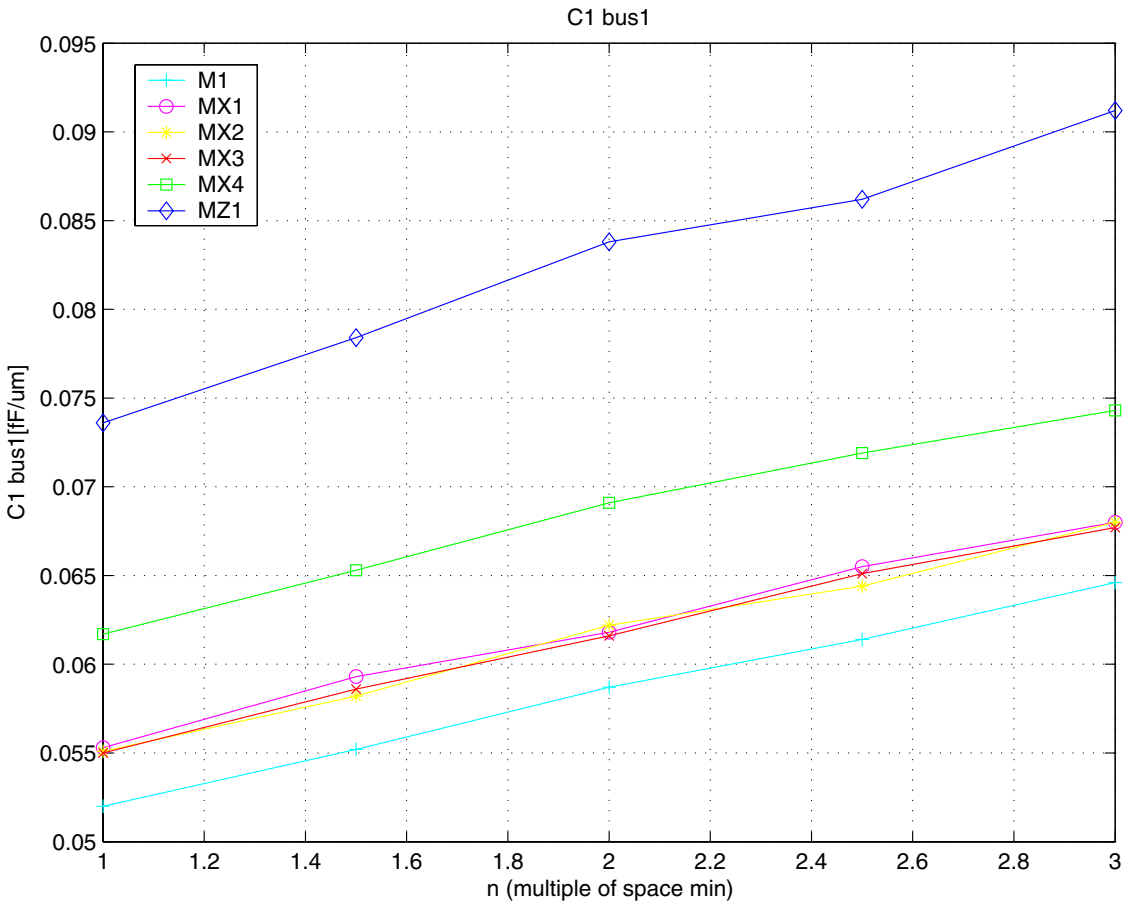

Figure 13:Bus1 bottom vertical coupling capacitance vs. space: C1 in fF/um

C2[fF/um]	Extracted Level					
n	M1	MX1	MX2	MX3	MX4	MZ1
1.0	0.055	0.056	0.056	0.056	0.026	0.074
1.5	0.058	0.060	0.060	0.060	0.027	0.079
2.0	0.062	0.063	0.063	0.064	0.029	0.083
2.5	0.065	0.067	0.067	0.066	0.030	0.086
3.0	0.068	0.069	0.069	0.069	0.031	0.090

Table 14:Bus1 top vertical coupling capacitance vs. space: C2 in fF/um

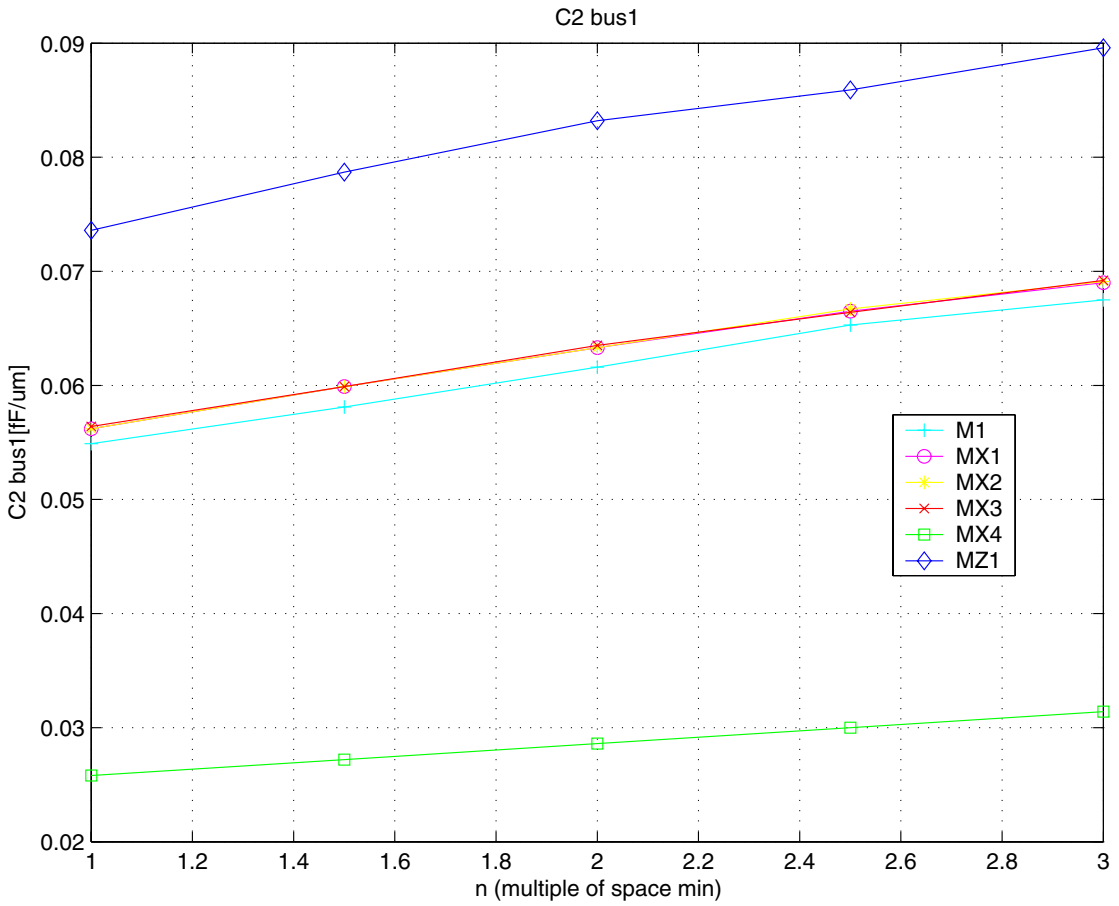

Figure 14:Bus1 top vertical coupling capacitance vs. space: C2 in fF/um

As a general rule the vertical capacitances (C1 & C2) increase with the space. This is due to the reduction of the lateral capacitance with the space: the upper and the lower buses now capture a part of the field lines. As for lateral coupling capacitances, sharing of C1 & C2 vs. Metal level can be explained by the structure environment:

- M2X, M3X,M4X:
  - C1 and C2 are the same because the structure is symetrical .
- M1:
  - C1 and C2 capacitances are slightly lower than M2X to M4X ones. This is due to the high lateral coupling capacitance.
- M5X:

- C1 capacitance is higher than M2X to M4X ones. This is due to the high lateral coupling capacitance.
- C2 capacitance is lower than M2X to M4X ones. This is due to the high lateral coupling capacitance and the high thickness of the M5X/M6Z dielectric.

- M6Z:
  - C1 and C2 are higher than for M2X to M4X level. This is due to the large width of M6Z lines and the high permittivity of M5X/M6Z dielectric that compensate the high thickness of the M5X/M6Z dielectric.

As a general rule for all metal levels,when we increase the space between metals, the combination of C1, C2 increased with C3 reduction. This explains the reduction of the lumped capacitance (less metals implies less parasitics).

Note: C3 should be applied on each side of the central line

2.3.2 Bus2: top & bottom buses with variable space

- Description
  - Minimum width is applied for all buses.
  - Space of all levels varies simultaneously from 1x min. space to 3x min. space.

The following table gives the space values used for each extracted level (M1 to M6Z) & buses (PO to M7Z)

space[um]	Level							
n	PO	M1	MX1	MX2	MX3	MX4	MZ1	MZ2
1	0.12	0.09	0.1	0.1	0.1	0.1	0.4	0.4
1.5	0.18	0.135	0.15	0.15	0.15	0.15	0.6	0.6
2	0.24	0.18	0.2	0.2	0.2	0.2	0.8	0.8
2.5	0.3	0.225	0.25	0.25	0.25	0.25	1	1
3	0.36	0.27	0.3	0.3	0.3	0.3	1.2	1.2

Table 15: Bus2 space values (*n = multiple of the space)

Next charts show coupling & lumped capacitances variation vs. space for each metal level.

for n=1 bus1 and bus2 are identical. Consequently, the comparisons are related to the other points.

- Lumped Capacitances

This structure has a behavior more complicated than the bus1 (see previous section). Indeed we have to consider the simultaneous space increase on all levels.

In comparison with previous case (bus1) bus2 exhibits a slightly lower lumped capacitance (see Figure 15 and see Table 16). This is due to the intrinsic building of the structure: the number of lines included in the top and the bottom buses decreases when n increases. Detailed explanation of the structures is presented in Annex1.

On another hand, specific remarks done on M1, M5X and M6Z are still valid.

Clumped[fF/um]	Extracted Level					
n	M1	MX1	MX2	MX3	MX4	MZ1
1.0	0.203	0.191	0.192	0.191	0.181	0.260
1.5	0.178	0.172	0.173	0.172	0.159	0.227
2.0	0.168	0.164	0.164	0.164	0.149	0.212
2.5	0.162	0.157	0.156	0.157	0.140	0.204
3.0	0.157	0.154	0.152	0.151	0.135	0.196

Table 16: Bus2 lumped capacitance vs. space in fF/um

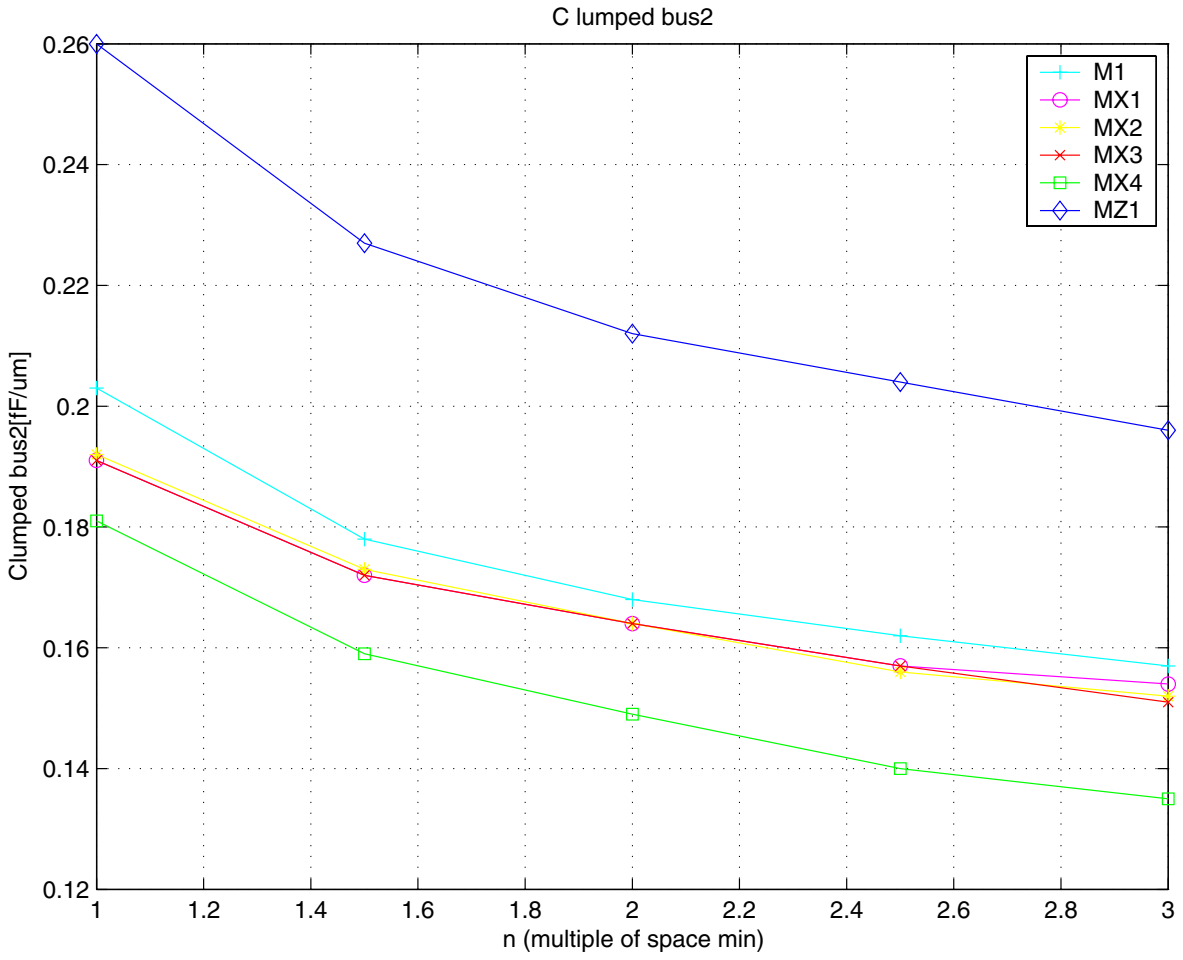

Figure 15: Bus2 lumped capacitance vs. space in fF/um

- Lateral Coupling Capacitances

  Compared to bus1 structure, bus2 increases slightly lateral coupling capacitances. Because of the space increase on top & bottom buses, they act as less efficient ground planes and the lateral coupling is favored.

  Bus1 specific remarks on capacitances sharing vs. metal level are still valid for bus2.

C3[fF/um]	Extracted Level					
n	M1	MX1	MX2	MX3	MX4	MZ1
1.0	0.093	0.081	0.079	0.080	0.089	0.112
1.5	0.065	0.056	0.056	0.055	0.065	0.072
2.0	0.053	0.042	0.043	0.042	0.052	0.050
2.5	0.044	0.032	0.032	0.032	0.042	0.037
3.0	0.036	0.025	0.025	0.025	0.036	0.028

Table 17:Bus2 lateral coupling capacitance vs. space: C3 in fF/um

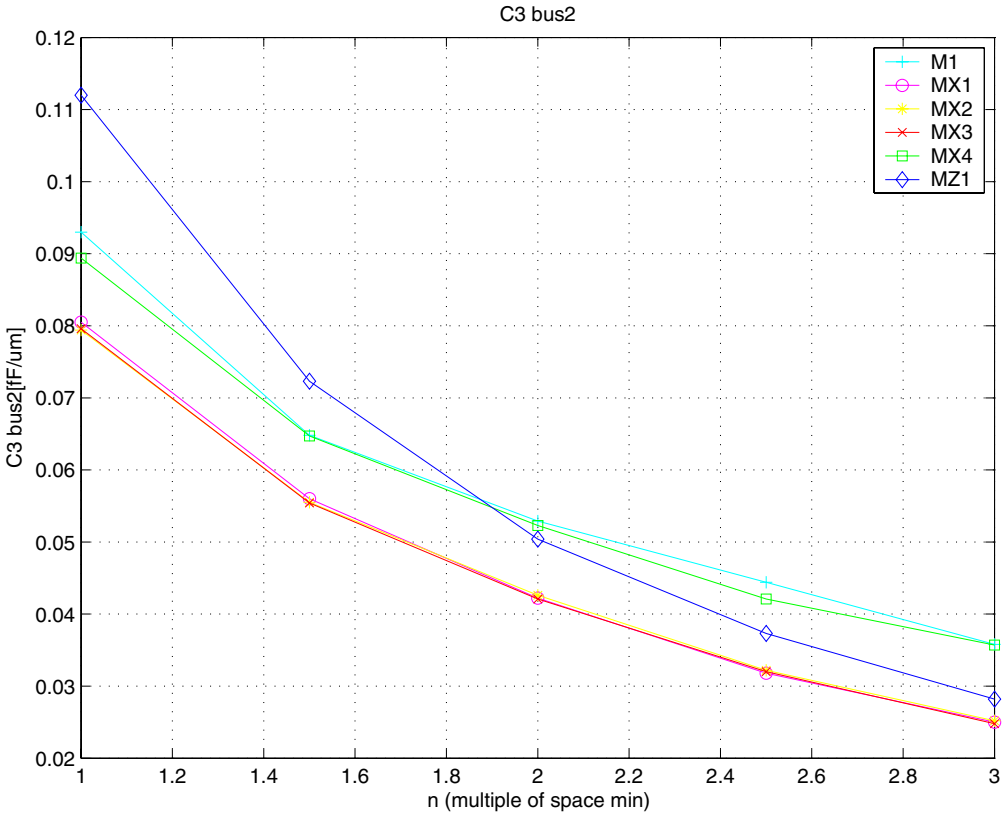

Figure 16:Bus2 lateral coupling capacitance vs. space: C3 in fF/um

- Vertical Coupling Capacitances

  Explanations about specific behavior on M1, M5X and M6Z due to process configuration are the same as bus1.

C1[fF/um]	Extracted Level					
n	M1	MX1	MX2	MX3	MX4	MZ1
1.0	0.052	0.055	0.055	0.055	0.062	0.074
1.5	0.054	0.057	0.058	0.058	0.064	0.079
2.0	0.055	0.060	0.060	0.060	0.066	0.082
2.5	0.055	0.063	0.062	0.062	0.068	0.086
3.0	0.055	0.064	0.062	0.062	0.070	0.087

Table 18:Bus2 bottom vertical coupling capacitance vs. space: C1 in fF/um

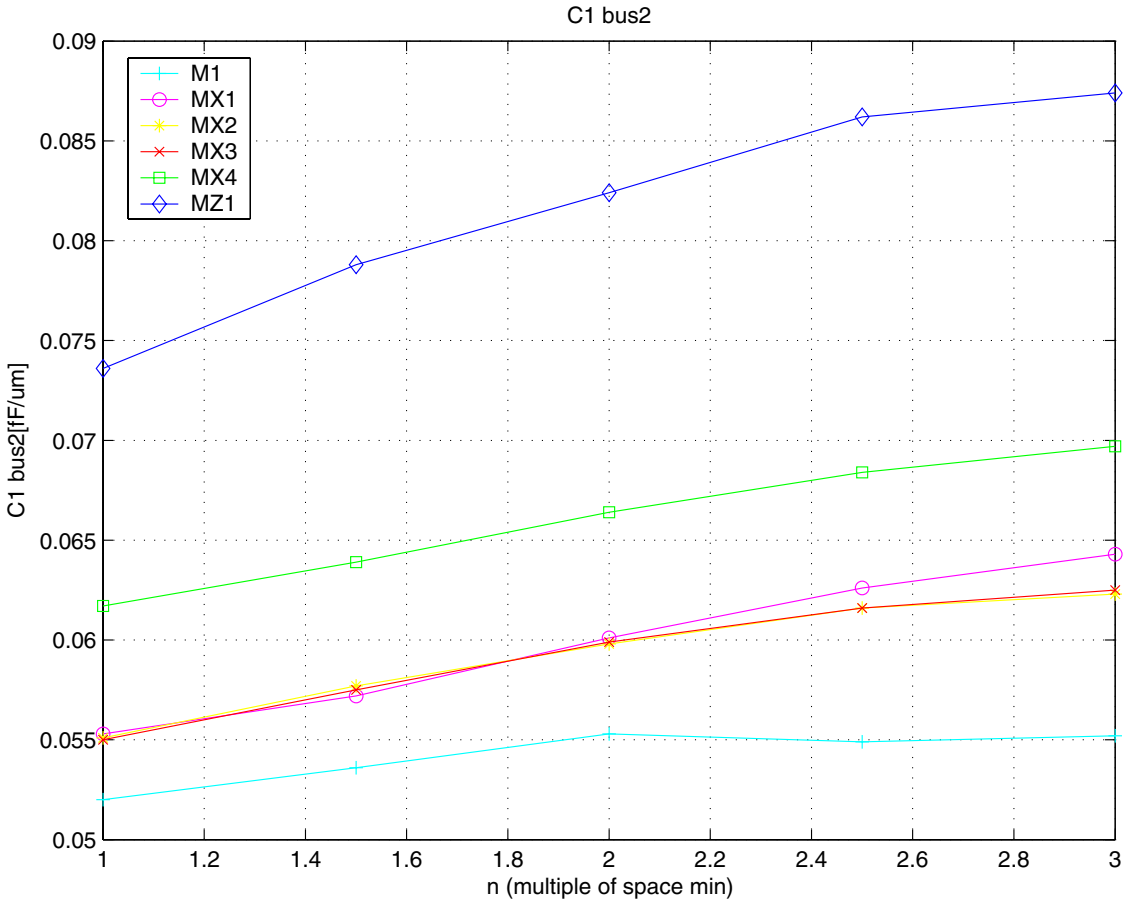

Figure 17:Bus2 bottom vertical coupling capacitance vs. space: C1 in fF/um

C2[fF/um]	Extracted Level					
n	M1	MX1	MX2	MX3	MX4	MZ1
1.0	0.055	0.056	0.056	0.056	0.026	0.074
1.5	0.057	0.058	0.059	0.058	0.026	0.076
2.0	0.059	0.060	0.061	0.061	0.027	0.078
2.5	0.061	0.062	0.062	0.062	0.028	0.079
3.0	0.062	0.063	0.063	0.063	0.027	0.080

Table 19:Bus2 top vertical coupling capacitance vs. space: C2 in fF/um

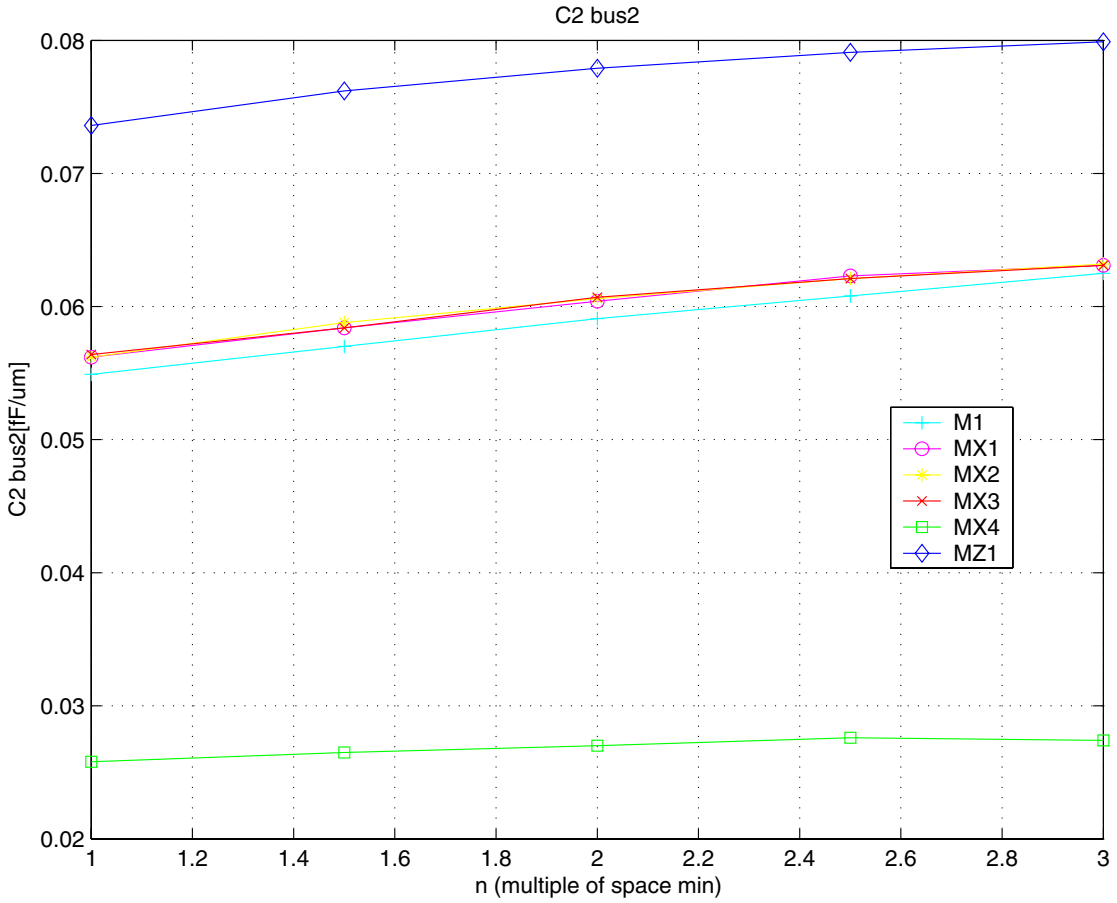

Figure 18:Bus2 top vertical coupling capacitance vs. space: C2 in fF/um

Appendix A - bus2 structure

The constraints to build bus2 are:

- Top & bottom buses cover the total length of the extracted bus;
- The total length of the extracted bus is fixed: L =100um;
- The space is multiplied by the same coefficient n on all level;

So, when the space (n) increases from 1 to 3, the number of lines on top & bottom buses is reduced. Figure 19 illustrates this evolution. The number of lines N by metal level is obtained by:

$$N \geq L / (W + n.S)$$

For example on MX4 top bus we found: N = 500 for n=1 and N = 250 for n= 3.

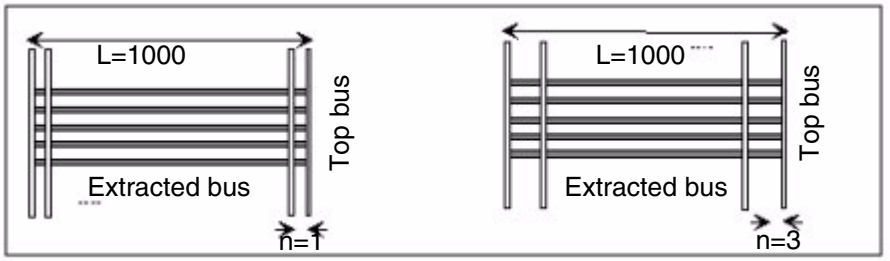

Figure 19: Top view of bus2 structure

To summarize, when the space increase, the number of lines within the top & bottom buses is reduced and capacitances C1&C2 decrease.