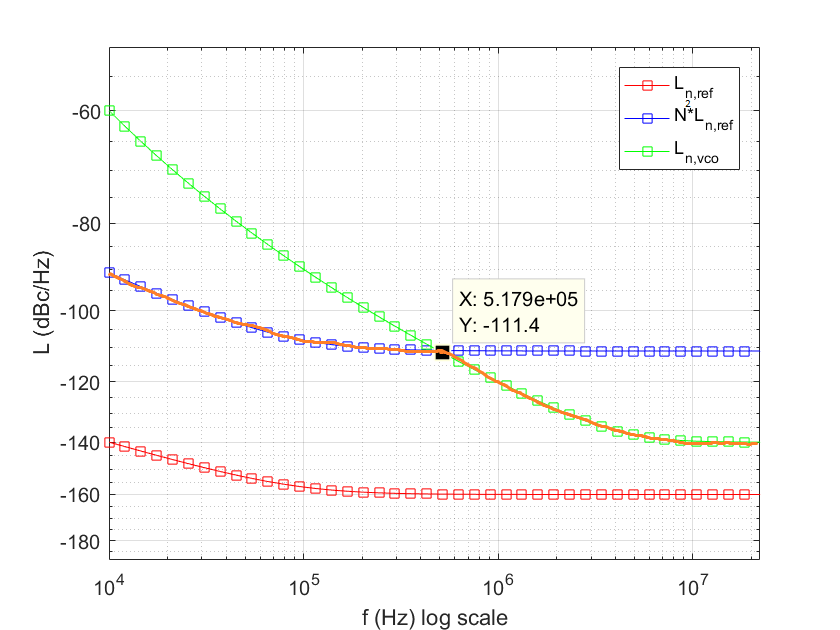
2.

Since only is considered here

Therefore

3.

4.



Take the larger as the worst-case scenario for noise calculation

For 3rd order PLL:

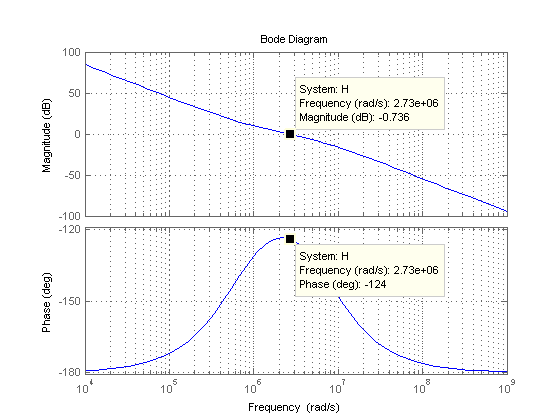
Since

Therefore

Therefore, it introduces one more pole:

Therefore

Phase margin is about 60 degrees.



At 1 MHz, the main noise contributor is VCO.

The rms phase error from 1 kHz – 100 MHz:

From 1 kHz to 100 kHz: dominate the noise source, specifically, noise; from 100 kHz to kHz, dominate the noise source, specifically, noise; from kHz to 10 MHz, dominate the noise source, specifically, noise; from 10 MHz to 100 MHz, dominate the noise source, specifically, noise.

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=0.013 rad = 0.745 deg