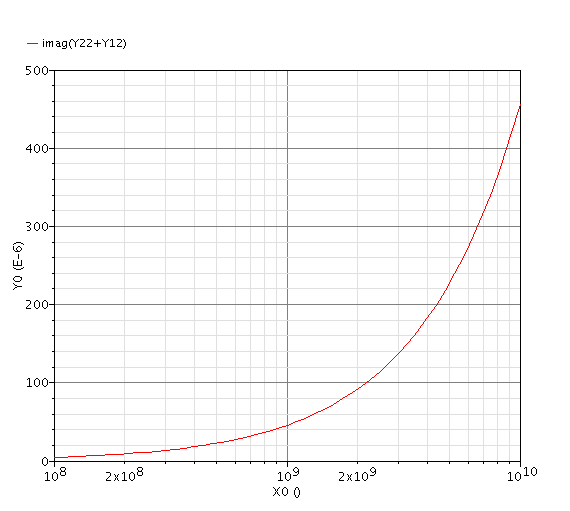
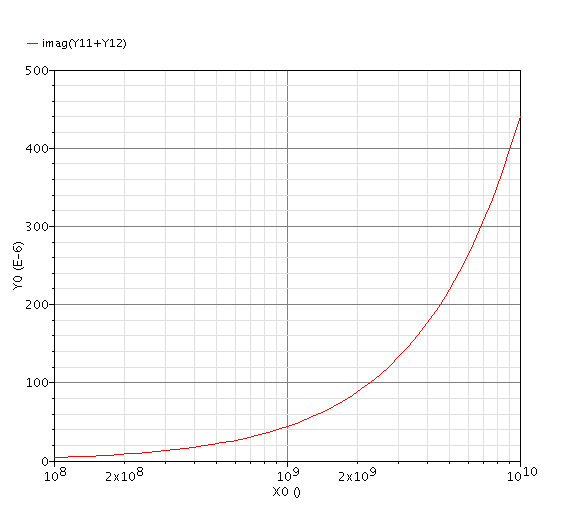
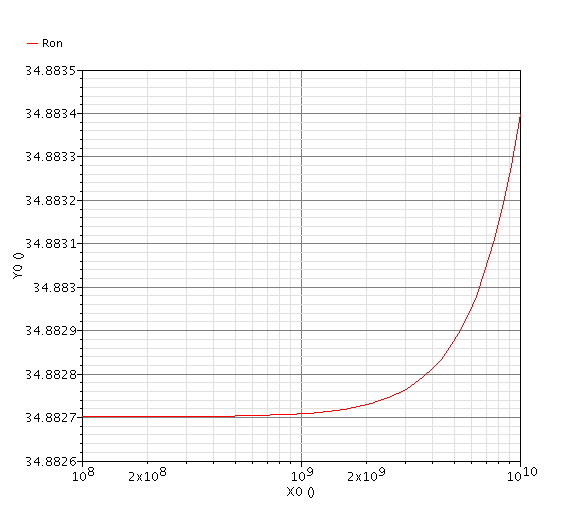
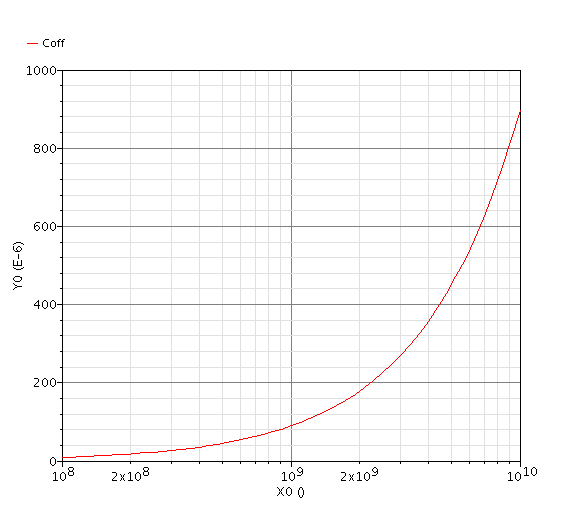
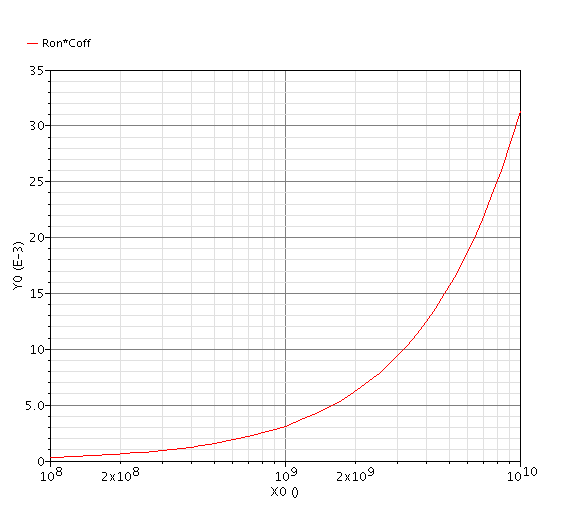
2.

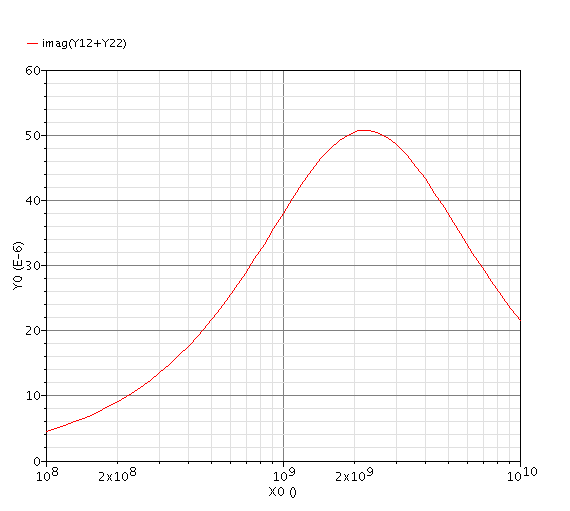
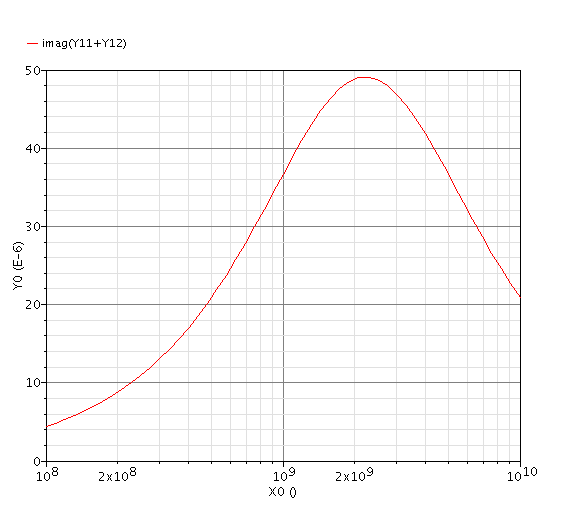
Rg = Rsub = 0.1

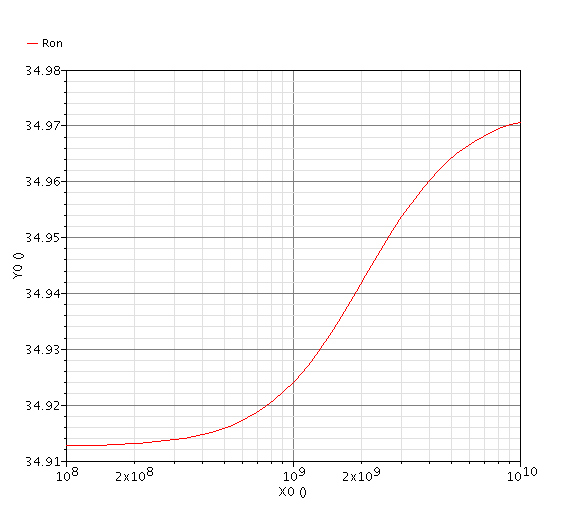
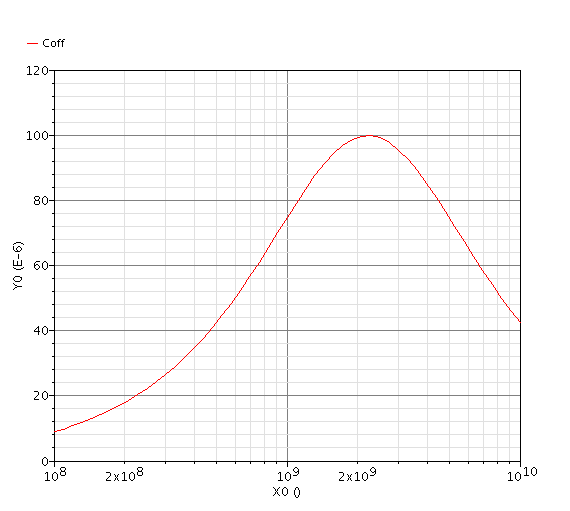


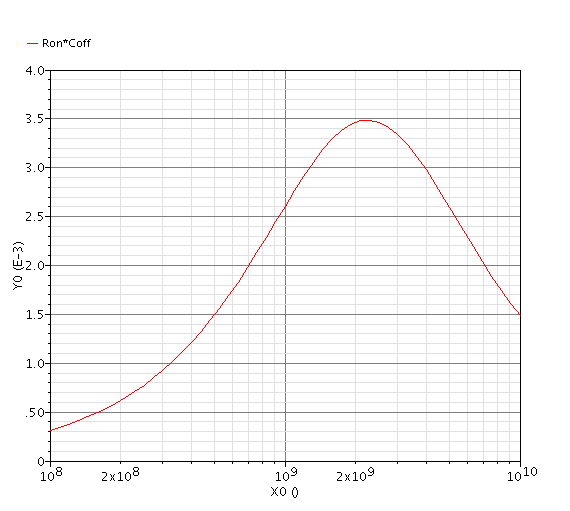


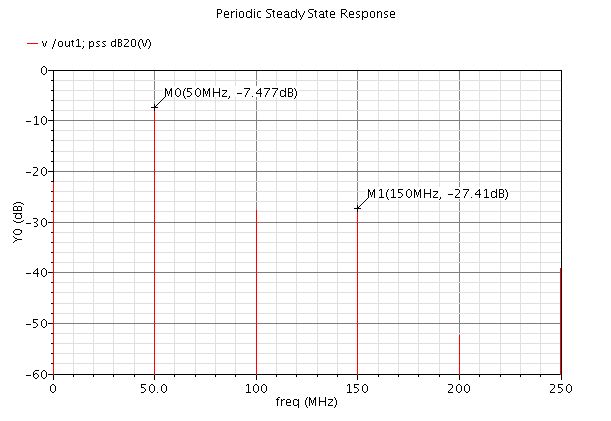
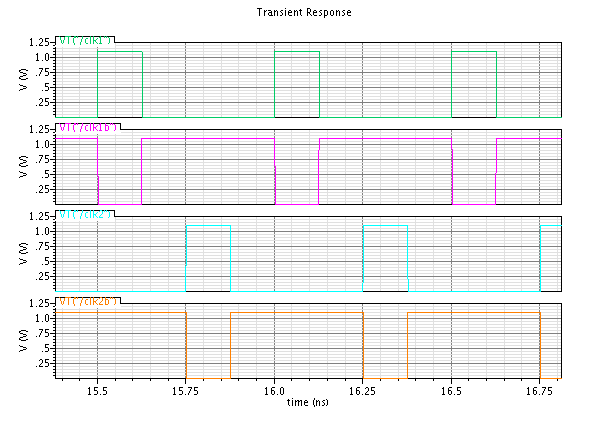


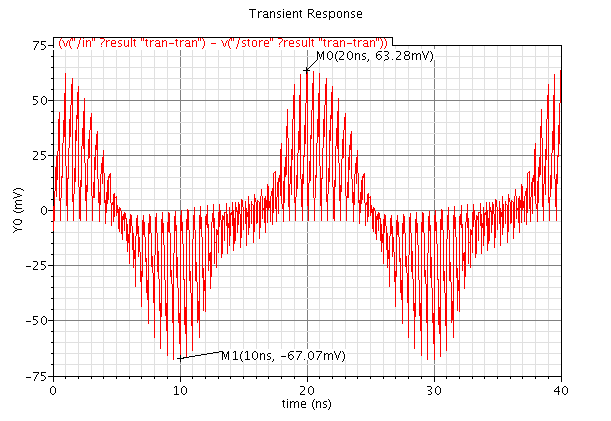
Rg = Rsub = 10k

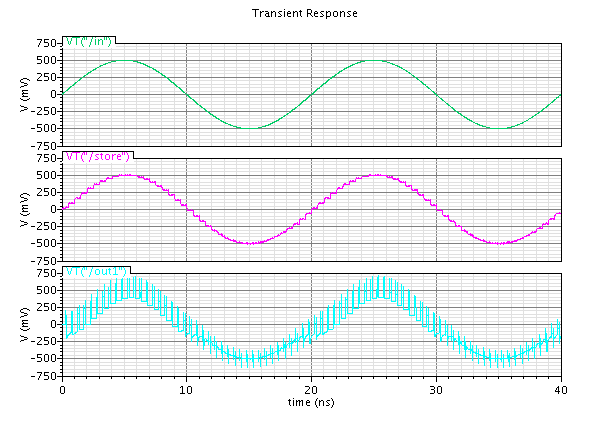






2. 





3.

Increase the transistor size (W) will decrease the on-resistance of the switch considering it operates in the triode region. However, it will aggregate the charge injection due to larger parasitic capacitance. Consider the channel charge of a NMOS transistor in triode region:

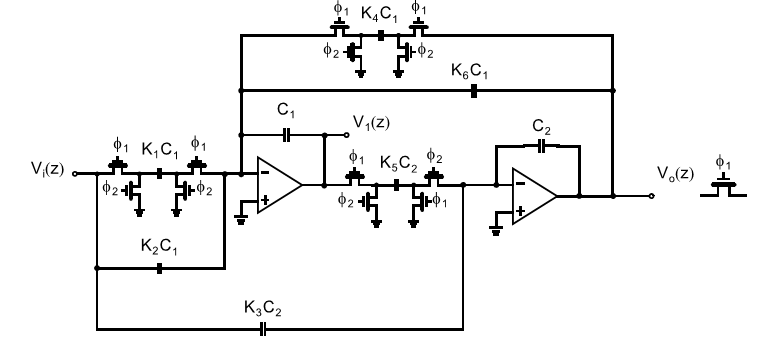
Increasing will generally increase the charge injection and therefore increase the error.

4.

It will be worse. Because transmission gate can be more effectively “cancel” out the overlap parasitic capacitance of NMOS and PMOS if they are matched nicely. Consider the channel charge of a NMOS transistor in triode region:

Therefore, by using transmission gate, , which is the output error caused by the charge injection can be minimized, which is not achievable by using NMOS (or PMOS) only.

4.



Pay attention to the minus sign here, it is there because for negative feedback inverting configuration op-amp implementation

Therefore

By substituting into where is the sampling frequency and selected as 10 GHz (≫ signal frequency)

Therefore:

Therefore:

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| K1 | K2 | K3 | K4 | K5 | K6 |
| 0 | 0.115 | 0.0056 | 0.097 | 0.097 | 0.112 |

The smallest capacitance is . If is 400fF, neglect K3, and round K1, K4, K5, K6 to 0.1. The smallest 40fF is still achievable in 65nm technology.

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| W | L |  |  |  |  |  |  |
| 6um | 0.06um |  |  |  |  |  |  |

SEE dt\_bp\_backup2

Approximating it to first order: