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Dual-Vth leakage power optimization

SYNTHESIS AND OPTIMIZATION OF DIGITAL SYSTEMS

The aim of this project is to write a plug-in for PrimeTime that implements a post-synthesis power minimization procedure. At the beginning the design is synthesized with cell configured as LVT. Configuring all cells as LVT, we have the maximum leakage power dissipation and higher slack. In the other hand the configuration with all cells as HVT leads to a lower power dissipation and the smaller slack (it can be negative in this configuration).
The algorithm starts by ordering the cells of the design is a sorted list. The parameter used to order the cells is given by:

$$K = \frac{P_{HVT} - P_{LVT}}{D_{HVT} - D_{LVT}}$$

P_{HVT} is the power dissipated by a cell that has been configured as HVT
P_{LVT} is the power dissipated by a cell that has been configured as LVT
D_{HVT} is the maximum delay through a cell configured as HVT
D_{LVT} is the maximum delay through a cell configured as LVT
The cells are ordered w.r.t the decreasing value of K which in this case is negative due to the bigger power of LVT cells. The bigger the absolute value of K for a given cell, the higher the priority of that cell to be swapped to HVT with the minimum slack penalty.
The algorithm we used is a *binary search-like*.
The ordered list of cells is progressively divided by two where half of the list is swapped to HVT. If the requirements are not met, another half of the LVT cells are swapped to HVT. If the savings are more than the user request, then half of the newly swapped cells are swapped back to LVT. This algorithm is repeated iteratively until the optimum number of cells is found with the minimum impact on the slack.