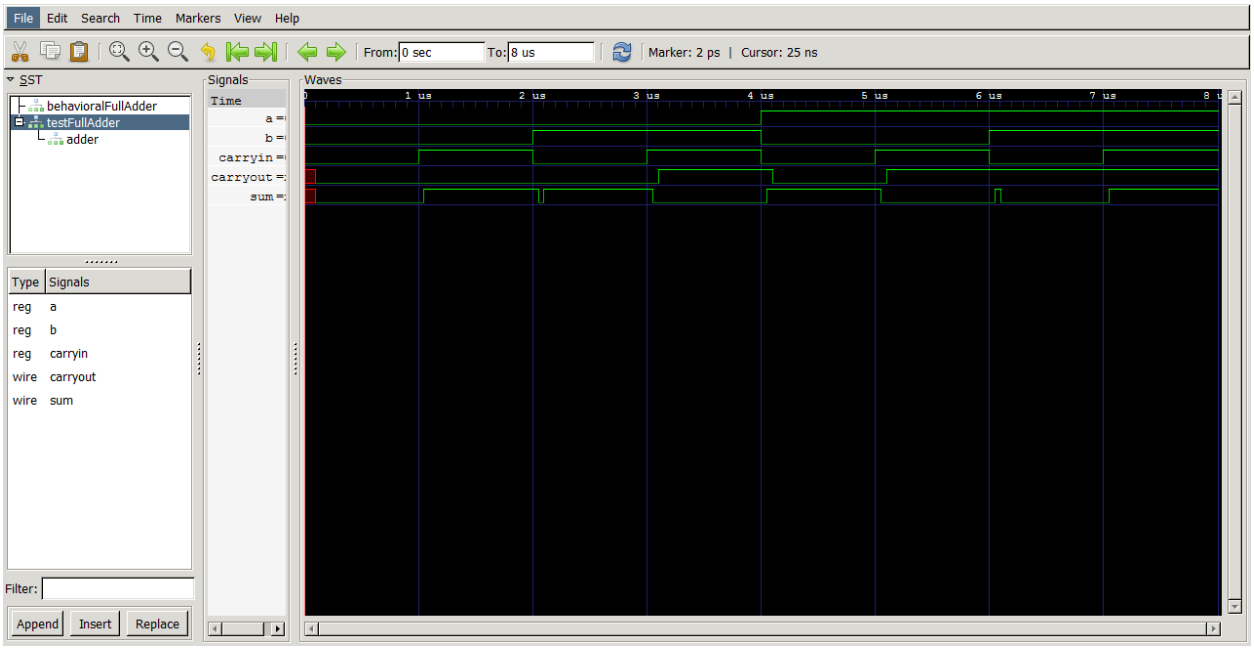
Chris Aring

Computer Architecture HW 2

1-bit Full Adder:



A	B	CIn	Sum	COut	Expected Output
0	0	0	0	0	0 0
0	0	1	1	0	1 0
0	1	0	1	0	1 0
0	1	1	0	1	0 1
1	0	0	1	0	1 0
1	0	1	0	1	0 1
1	1	0	0	1	0 1
1	1	1	1	1	1 1

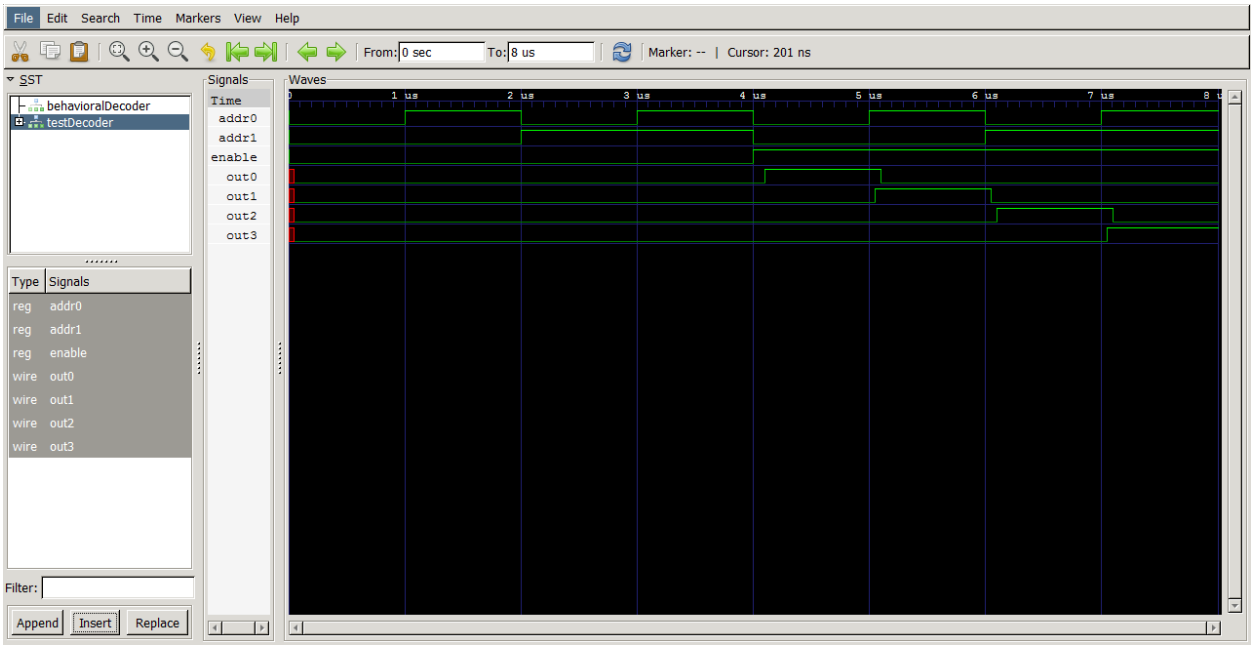
Behavioral Adder

A	B	CIn	Sum	COut	Expected Output
0	0	0	0	0	0 0
0	0	1	1	0	1 0
0	1	0	1	0	1 0
0	1	1	0	1	0 1
1	0	0	1	0	1 0
1	0	1	0	1	0 1
1	1	0	0	1	0 1
1	1	1	1	1	1 1

Structural Adder

$iverilog –o adder adder.t.v
$vvp adder
$wavegtk adder.vcd

2-bit Decoder with Enable:



En	A0	A1	O0	O1	O2	O3	Expected Output
0	0	0	0	0	0	0	All false
0	1	0	0	0	0	0	All false
0	0	1	0	0	0	0	All false
0	1	1	0	0	0	0	All false
1	0	0	1	0	0	0	O0 Only
1	1	0	0	1	0	0	O1 Only
1	0	1	0	0	1	0	O2 Only
1	1	1	0	0	0	1	O3 Only

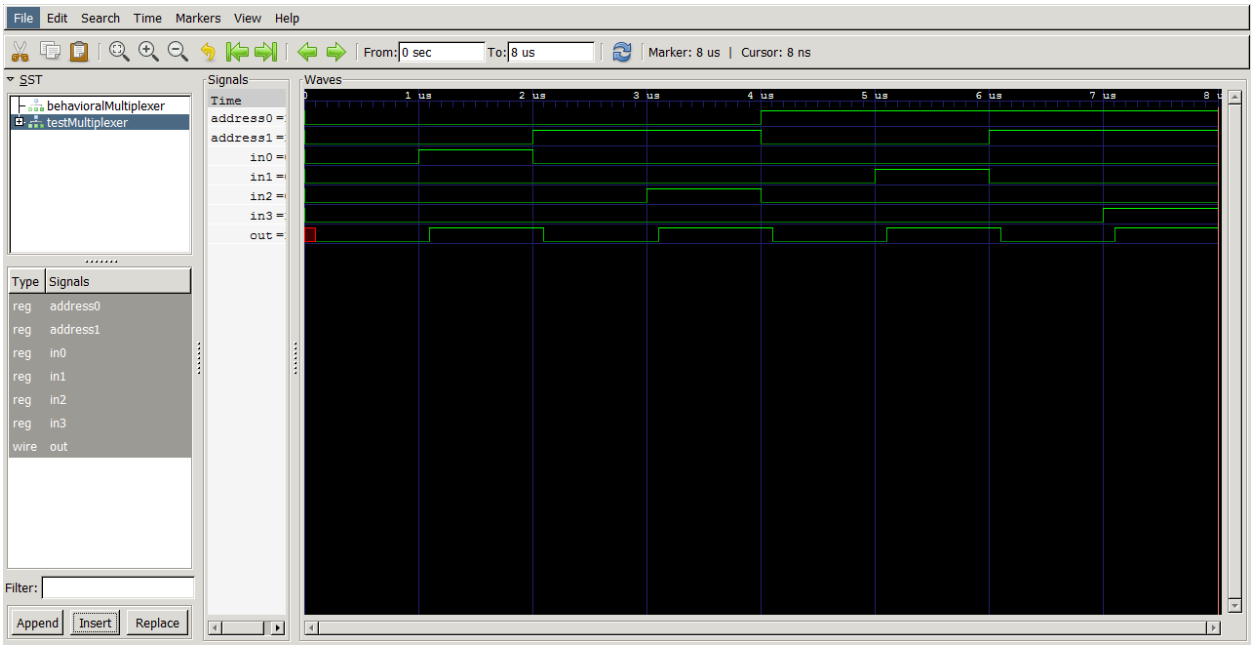
Behavioral Decoder

En	A0	A1	O0	O1	O2	O3	Expected Output
0	0	0	0	0	0	0	All false
0	1	0	0	0	0	0	All false
0	0	1	0	0	0	0	All false
0	1	1	0	0	0	0	All false
1	0	0	1	0	0	0	O0 Only
1	1	0	0	1	0	0	O1 Only
1	0	1	0	0	1	0	O2 Only
1	1	1	0	0	0	1	O3 Only

Structural Decoder

$iverilog –o decoder decoder.t.v
$vvp decoder
$wavegtk decoder.vcd

4 Input Multiplexer:



A0	A1	In0	In1	In2	In3	Out	Expected Output
0	0	0	0	0	0	0	0
0	0	1	0	0	0	1	1
0	1	0	0	0	0	0	0
0	1	0	0	1	0	1	1
1	0	0	0	0	0	0	0
1	0	0	1	0	0	1	1
1	1	0	0	0	0	0	0
1	1	0	0	0	1	1	1

Behavioral Multiplexer

A0	A1	In0	In1	In2	In3	Out	Expected Output
0	0	0	0	0	0	0	0
0	0	1	0	0	0	1	1
0	1	0	0	0	0	0	0
0	1	0	0	1	0	1	1
1	0	0	0	0	0	0	0
1	0	0	1	0	0	1	1
1	1	0	0	0	0	0	0
1	1	0	0	0	1	1	1

Structural Multiplexer

$iverilog –o multiplexer multiplexer.t.v
$vvp multiplexer
$wavegtk multiplexer.vcd