Hi3231 V530 芯片简介

Key specifications

- 4K x 2K@60 Hz TCON
- 4K x 2K@120 Hz TCON (2 chips cascaded)
- EPAD-LQFP128 package

High-speed input interface

- 8 lane V-by-One (VBO) RX video interface
- 4K x 2K@60 Hz 8-/10-bit video data
- DE only mode
- 1/2 partition input format

High-speed output interface

- P2P/mini-LVDS TX interface
- 4K x 2K@60 Hz or 4K x 1K@120 Hz output
- Up to 12-pair P2P output
- All mainstream P2P protocols
- Adjustable pre-emphasis and swing

Professional HiSilicon graphics engine

- Hi-Imprex, embedded image enhancement engine
- High-order color management
- 12-bit programmable gamma LUT
- Demo-mode PQ algorithms

TCON functions

- Configurable driver timing control
- Configurable GOA timing control
- OD/MOD
- Demura
- Wide-angle processing
- High-performance multi-partition line OD compensation
- Pre-charging
- 1D1G, dual-gate, and tri-gate
- Scan and reverse scan
- Flexible POL n+m line inversion
- PDF

Memory control interfaces

- One embedded DDR memory
- TCON flash and demura flash accesses

System and peripheral interfaces

- Embedded high-performance RISC CPU
- I^2C interface
- UART interface
- Multiple groups of GPIO ports
- Integrated POR module
- Multiple aging modes

Other

- Download and execution of the boot program through the chip interface

Output spread spectrum

- ±3% spread spectrum configurable
- 30–300 kHz modulation frequencies

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版本：01
日期：2019-04-23