Hi3520D V300 H.264 CODEC Processor

Brief Data Sheet

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Hi3520D V300 H.264 CODEC Processor

Key Specifications

Processor Core

- ARM Cortex A7@maximum 800 MHz
  - 32 KB L1 I-cache, 32 KB L1 D-cache
  - 128 KB L2 cache
  - NEON and FPU

Video Encoding/Decoding Protocols

- H.264 baseline/main/high profile L4.2
- MJPEG/JPEG baseline

Video Encoding/Decoding

- H.264&JPEG encoding and decoding of multiple streams
  - 4x720p@30 fps H.264 encoding+4xCIF@30 fps H.264 encoding+4x720p@30 fps H.264 decoding+4x720p@2 fps JPEG encoding
  - 8x960H@30 fps H.264 encoding+8xCIF@30 fps H.264 encoding+1x960H@30 fps H.264 decoding+8x960H@2 fps JPEG encoding
  - 8xD1@30 fps H.264 encoding+8xCIF@30 fps H.264 encoding+4xD1@30 fps H.264 decoding+8xD1@2 fps JPEG encoding
  - 4x1080p@30 fps H.264 decoding
  - 4x720p@30 fps H.264 decoding
  - 4x720p@30 fps JPEG decoding
- Constant bit rate (CBR) mode, variable bit rate (VBR) mode, FixQp mode, and adaptive variable bit rate (AVBR) mode, with the bit rate ranging from 16 kbit/s to 40 Mbit/s
- Fixed QP
- Encoding frame rate ranging from 1/16 fps to full frame rate
- ROI encoding
- Color-to-gray encoding

Intelligent Video Analysis

- Integrated IVE, supporting various intelligent analysis applications such as motion detection, perimeter defense, and video diagnosis

Video and Graphics Processing

- Deinterlacing, sharpening, 3D denoising, dynamic contrast improvement, and demosaic
- Anti-flicker for output videos and graphics
- 1/15x to 16x video scaling
- 1/2x to 2x graphics scaling
- Four Cover regions
- OSD overlaying of eight regions

Audio Encoding/Decoding

- ADPCM, G.711, and G.726 hardware audio encoding
- Software audio encoding and decoding complying with multiple protocols

Security Engine

- AES, DES, and 3DES algorithms implemented by hardware

Video Interfaces

- VI interfaces
  - Two 8-bit interfaces or one 16-bit interface
  - 108 MHz/144 MHz 4xD1/960H TDM inputs for each 8-bit interface (8xD1/8x960H real-time video inputs in total)
  - 144 MHz/148.5 MHz 2x720p TDM inputs for each 8-bit interface (4x720p@30 fps real-time video inputs in total)
  - 4x720p TDM inputs through 148.5 MHz dual-edge sampling or 297 MHz single-edge sampling for each 8-bit interface (8x720p@30 fps real-time video inputs in total)
  - 2x1080p TDM inputs through 148.5 MHz dual-edge sampling or 297 MHz single-edge sampling for each 8-bit interface (4x1080p@30 fps real-time video inputs in total)
  - 148.5 MHz BT.1120 Y/C interleaved mode for each 8-bit interface (2x1080p@30 fps real-time video inputs in total)
  - 148.5 MHz BT.1120 standard mode for the 16-bit interface (1x1080p@60 fps real-time video inputs in total)
- VO interfaces
  - HDMI 1.4+VGA+CVBS video outputs
  - HDMI and VGA outputs from the same source
  - Maximum 1080p@60 fps resolution for HDMI or VGA
  - One HD graphics layer and one SD graphics layer in ARGB1555 or ARGB8888 format
  - One hardware cursor layer in ARGB1555 or ARGB8888 format, with the maximum resolution of 128 x 128
  - Alpha blending of the video layer, graphics layer, and cursor layer

Audio Interfaces

- Three unidirectional I^{2}S/PCM interfaces
  - Two input interfaces, supporting 16 multiplexed inputs
  - One output, supporting dual-channel multiplexed output
  - 16-bit audio inputs and outputs

Ethernet Ports

- One gigabit Ethernet port
  - RGMII, RMII, and MII modes
  - 10/100 Mbit/s half-duplex or full-duplex
  - 1000 Mbit/s full-duplex
  - TSO for reducing the CPU usage

Peripheral Interfaces

- Two SATA 2.0 interfaces
  - PM
  - eSATA
- Two USB 2.0 host ports, supporting the hub
- Three UART interfaces, one of which supporting four wires

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- One SPI, supporting one CS
- One IR interface
- One I^{2}C interface
- Multiple GPIO interfaces

Memory Interfaces

- One 16-bit DDR3/DDR3L SDRAM interface
  - Maximum frequency of 800 MHz
  - ODT
  - Maximum capacity of 512 MB
  - Automatic power consumption control
- SPI NOR/NAND flash interface
  - 1-/2-/4-bit SPI NOR/NAND flash
  - Two CSs, connected to different flash memories
  - Maximum capacity of 32 MB for each CS (only for the NOR flash)
  - Maximum capacity of 4 GB for each CS (only for the SPI NAND flash)
  - 2 KB/4 KB page size (only for the SPI NAND flash)
  - 8-bit/24-bit/1 KB ECC (only for the SPI NAND flash)
- Embedded 4 KB BOOTROM and 16 KB SRAM

RTC with an Independent Power Supply

- Independent battery for supplying power to the RTC

Configurable Boot Modes

- Booting from the BOOTROM
- Booting from the SPI NOR flash
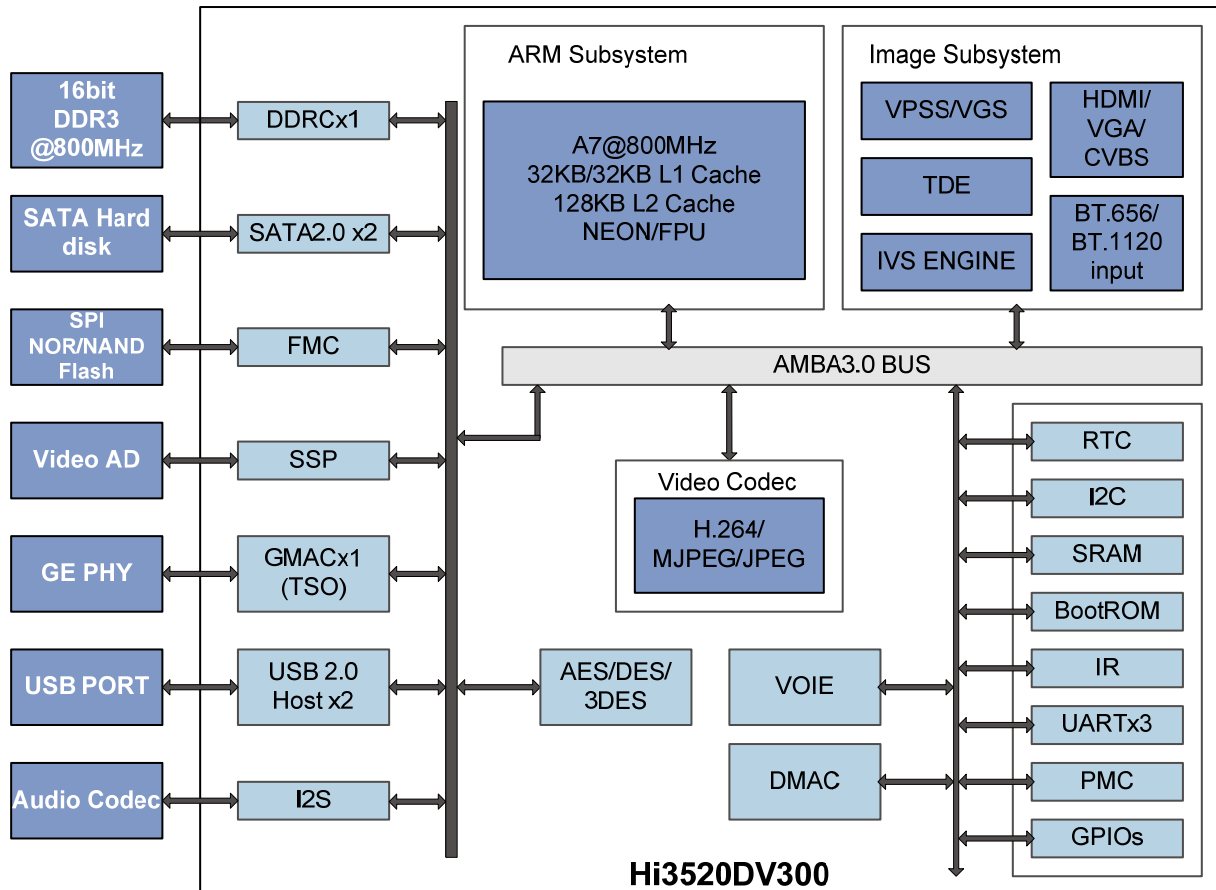- Booting from the SPI NAND flash

SDK

- Linux 3.10-based SDK
- Audio encoding and decoding libraries complying with various protocols
- High-performance H.264 PC decoding library

Physical Specifications

- Power consumption
  - Typical power consumption of 2.5 W
  - Multi-level power consumption control
- Operating voltages
  - 1.15 V core (including the CPU) voltage
  - 3.3 V I/O voltage
  - 1.5 V DDR3 SDRAM interface voltage
- Package
  - RoHS, Epad-LQFP256
  - Lead pitch of 0.4 mm (0.02 in.)
  - Body size of 28 mm x 28 mm (1.10 in. x 1.10 in.)
- Operating temperature ranging from 0°C (32°F) to 70°C (158°F)

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Functional Block Diagram

Hi3520D V300 is a professional SoC targeted for the multi-channel HD (1080p/720p) or SD (D1/960H) DVR. Hi3520D V300 provides an ARM A7 processor, a high-performance H.264 video encoding/decoding engine, a high-performance video/graphics processing engine with various complicated graphics processing algorithms, HDMI/VGA HD outputs, and various peripheral interfaces. These features enable Hi3520D V300 to provide high-performance, high-picture-quality, and low-cost analog HD/SDI solutions for customers' products while reducing the eBOM cost.

DVRs (Each with a Hi3520D V300)

4x1080p DVR (Non-real-time)
- 4x1080p@12 fps H.264 encoding+4xCIF@12 fps H.264 encoding+4x1080p@12 fps H.264 decoding+4x1080p@2 fps JPEG encoding
- HDMI+VGA 1080p@60 fps outputs from the same source+CVBS outputs

4x720p DVR
- 4x720p@30 fps H.264 encoding+4xCIF@30 fps H.264 encoding+4x720p@30 fps H.264 decoding+4x720p@2 fps JPEG encoding
- HDMI+VGA 1080p@60 fps outputs from the same source+CVBS outputs

8x720p DVR (Non-real-time)
- 8x720p@15 fps H.264 encoding+8xCIF@15 fps H.264 encoding+4x720p@15 fps H.264 decoding+8x720p@2 fps JPEG encoding
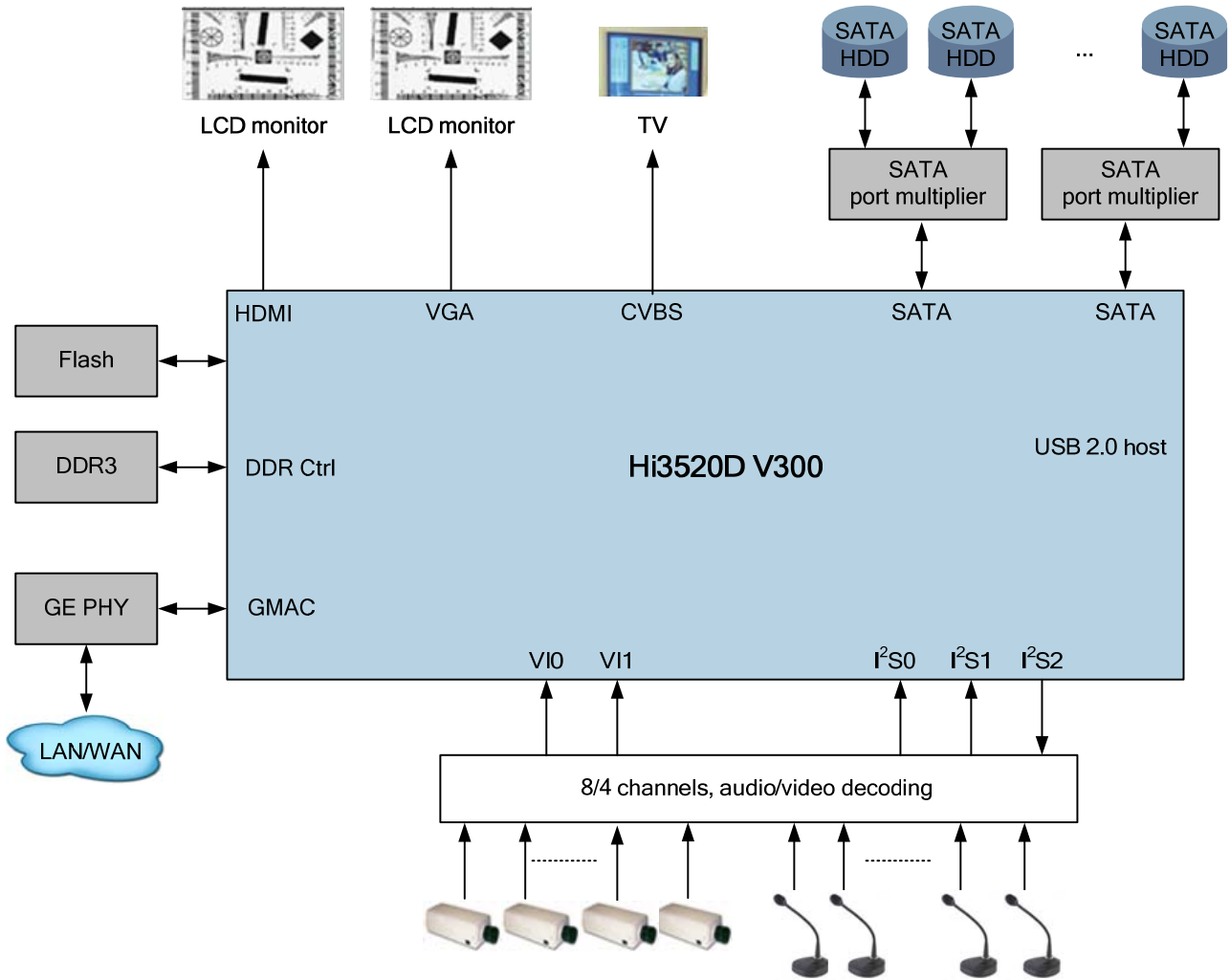- HDMI+VGA 1080p@60 fps outputs from the same source+CVBS outputs

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8x960H DVR

- 8x960H@30 fps H.264 encoding+8xCIF@30 fps H.264 encoding+4x960H@30 fps H.264 decoding+8x960H@2 fps JPEG encoding
- HDMI+VGA 1080p@60 fps outputs from the same source+CVBS outputs

8xD1 DVR

- 8xD1@30 fps H.264 encoding+8xCIF@30 fps H.264 encoding+8xD1@30 fps H.264 decoding+8xD1@2 fps JPEG encoding
- HDMI+VGA 1080p@60 fps outputs from the same source+CVBS outputs

Acronyms and Abbreviations

3DES	triple data encryption standard
ADPCM	adaptive differential pulse code modulation
AES	advanced encryption standard
CBR	constant bit rate
CS	chip select
CVBS	composite video broadcast signal
DCI	dynamic contrast improvement
DDR	double data rate
DES	data encryption standard
DVR	digital video recorder
eBOM	engineering bill of materials
ECC	error correcting code
eSATA	external serial advanced technology attachment
GPIO	general-purpose input/output
HD	high definition
HDMI	high definition multimedia interface
I^2C	inter-integrated circuit
I^2S	inter-IC sound
IR	infrared
IVE	intelligent video engine
MII	media independent interface
ODT	on-die termination
OSD	on-screen display
PCM	pulse code modulation
PM	port multiplexer
QP	quantization parameter
RGMII	reduced gigabit media independent interface
RMII	reduced media independent interface
RoHS	Restriction of Hazardous Substances
ROI	region of interest
RTC	real-time clock
SATA	serial advanced technology attachment
SD	standard definition
SDI	serial digital interface
SDK	software development kit
SDRAM	synchronous dynamic random access memory
SoC	system-on-chip
SPI	serial peripheral interface
SRAM	static random access memory
TDM	time division multiplexing
TSO	TCP segmentation offload
UART	universal asynchronous receiver transmitter
VBR	variable bit rate
VGA	video graphics array
VI	video input
VO	video output