Computer Arch

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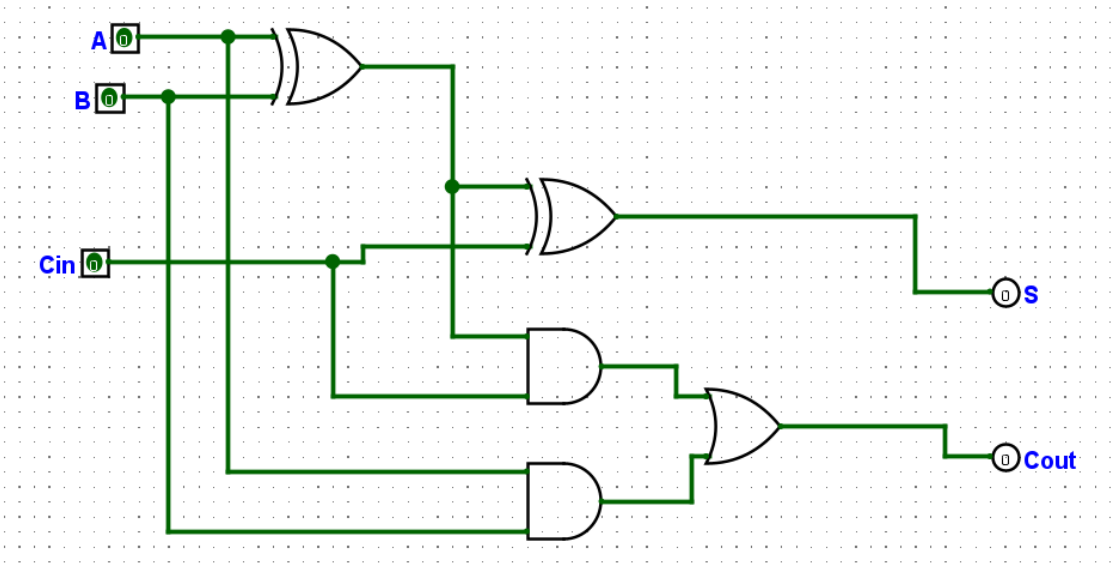
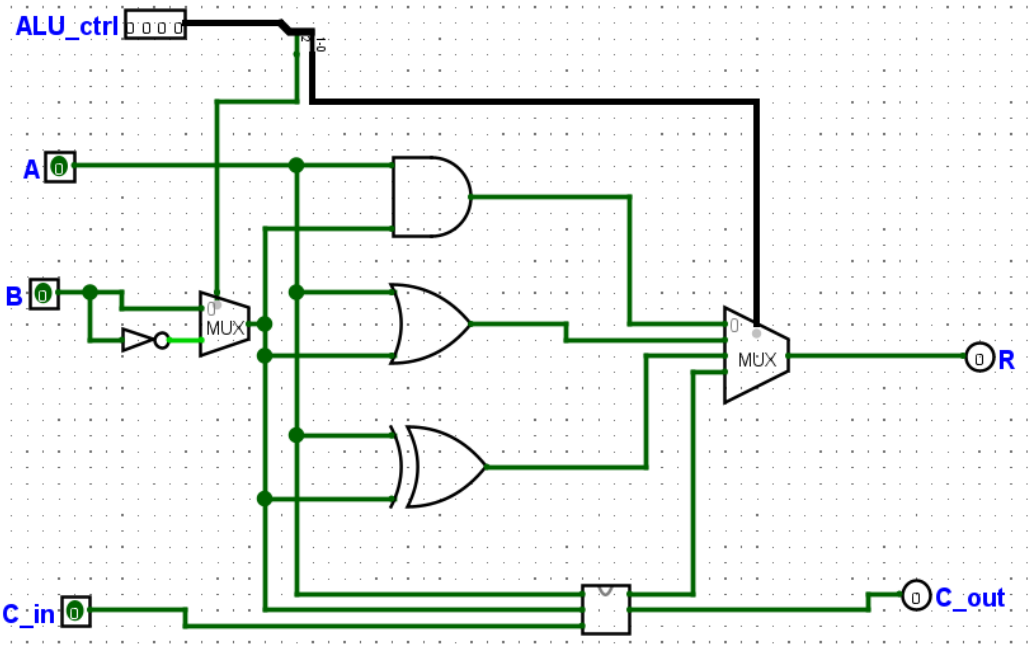
Milestone 1

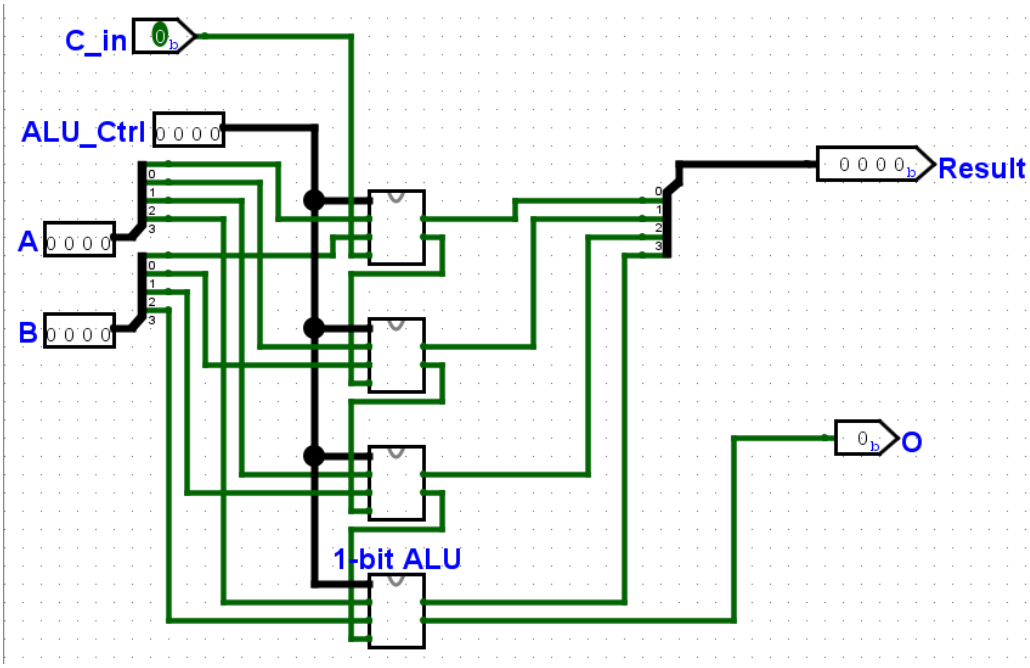
1-Bit Adder



1-Bit ALU

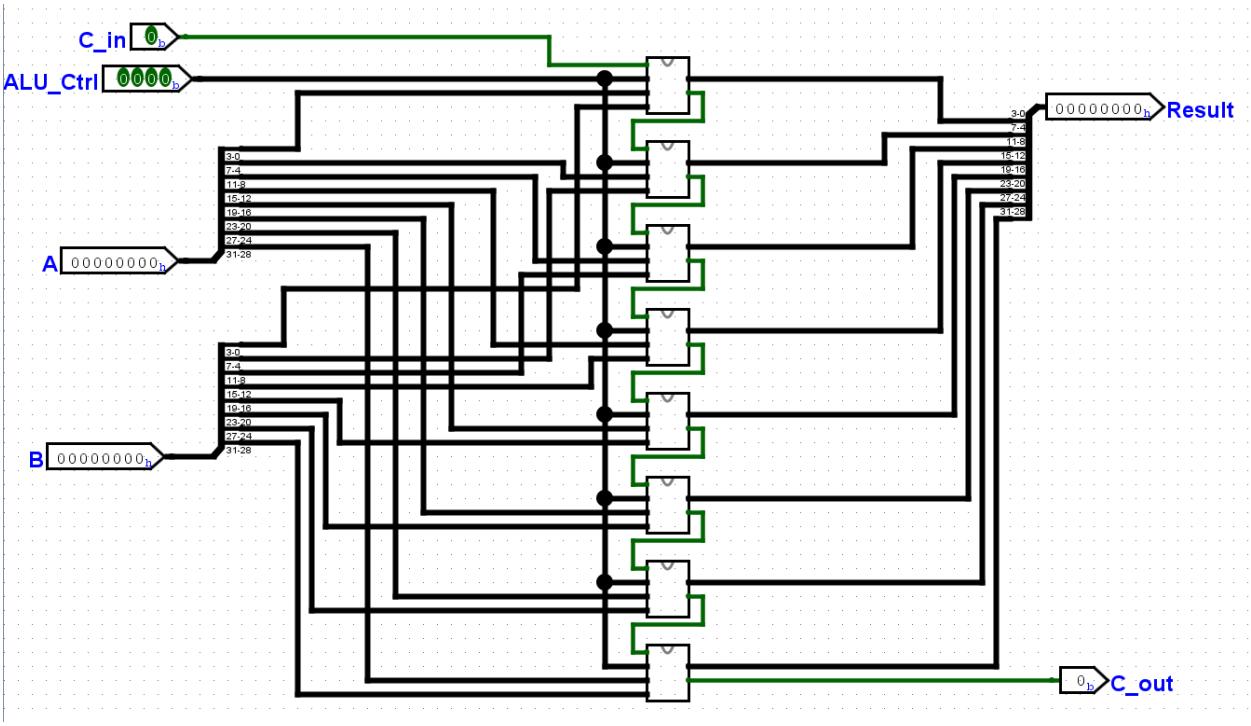


4-Bit ALU



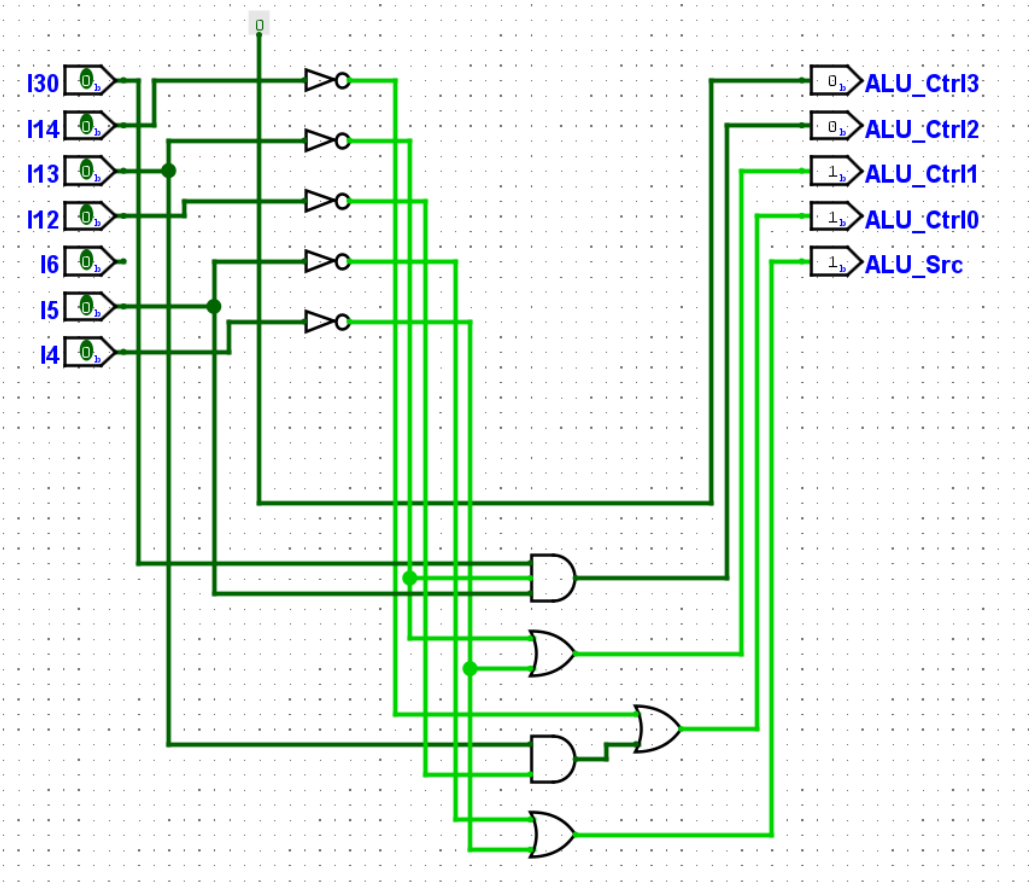
32-Bit ALU

-Each box is a 4-bit ALU. Logisim did not allow me to put the label names on them.



ALU_Ctrl

Inst'n	I30	I14	I13	I12	I6	I5	I4	ALU_Ctr3	ALU_Ctrl2	ALU_Ctrl1	ALU_Ctrl0	ALU_Src
AND	0	1	1	1	0	1	1	0	0	0	0	0
OR	0	1	1	0	0	1	1	0	0	0	1	0
XOR	0	1	0	0	0	1	1	0	0	1	0	0
ADD	0	0	0	0	0	1	1	0	0	1	1	0
SUB	1	0	0	0	0	1	1	0	1	1	1	0
ANDI	X	1	1	1	0	0	1	0	0	0	0	1
ORI	X	1	1	0	0	0	1	0	0	0	1	1
XORI	X	1	0	0	0	0	1	0	0	1	0	1
ADDI	X	0	0	0	0	0	1	0	0	1	1	1
LW	X	0	1	0	0	0	0	0	0	1	1	1
SW	X	0	1	0	0	1	0	0	0	1	1	1



ImmGen:

EXTRA: I decided to finish the ImmGenerator. Professor Moore said to finished it earlier, so I decided to complete that circuit.