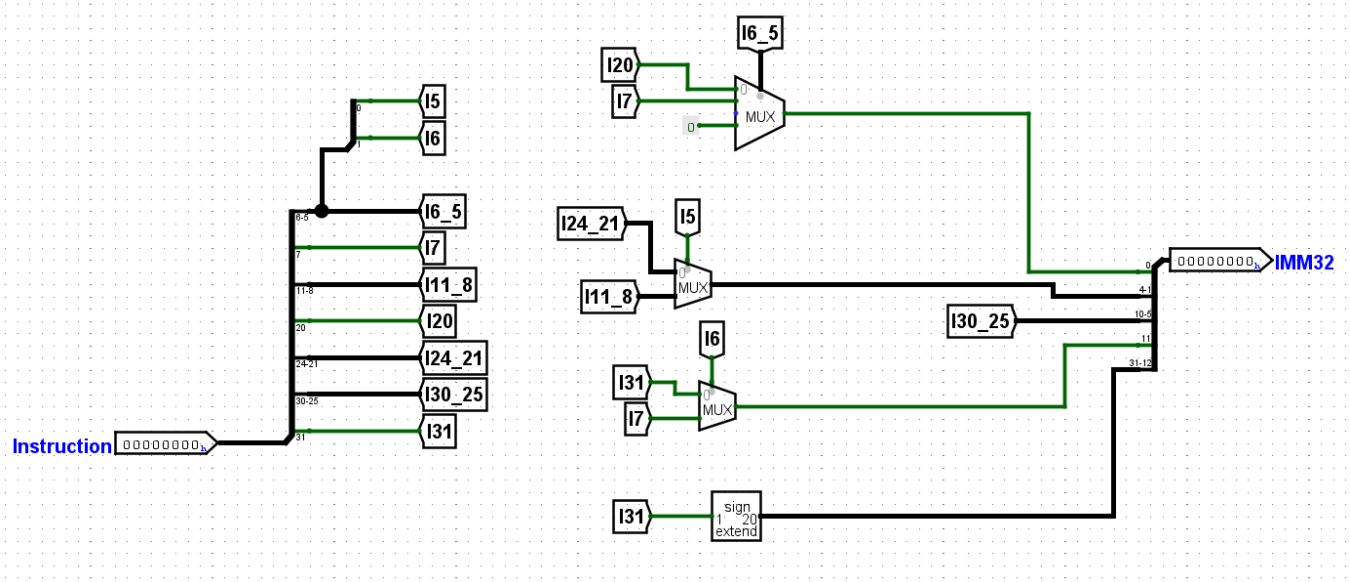
Computer Arch

Christian Gomez

4/20/22

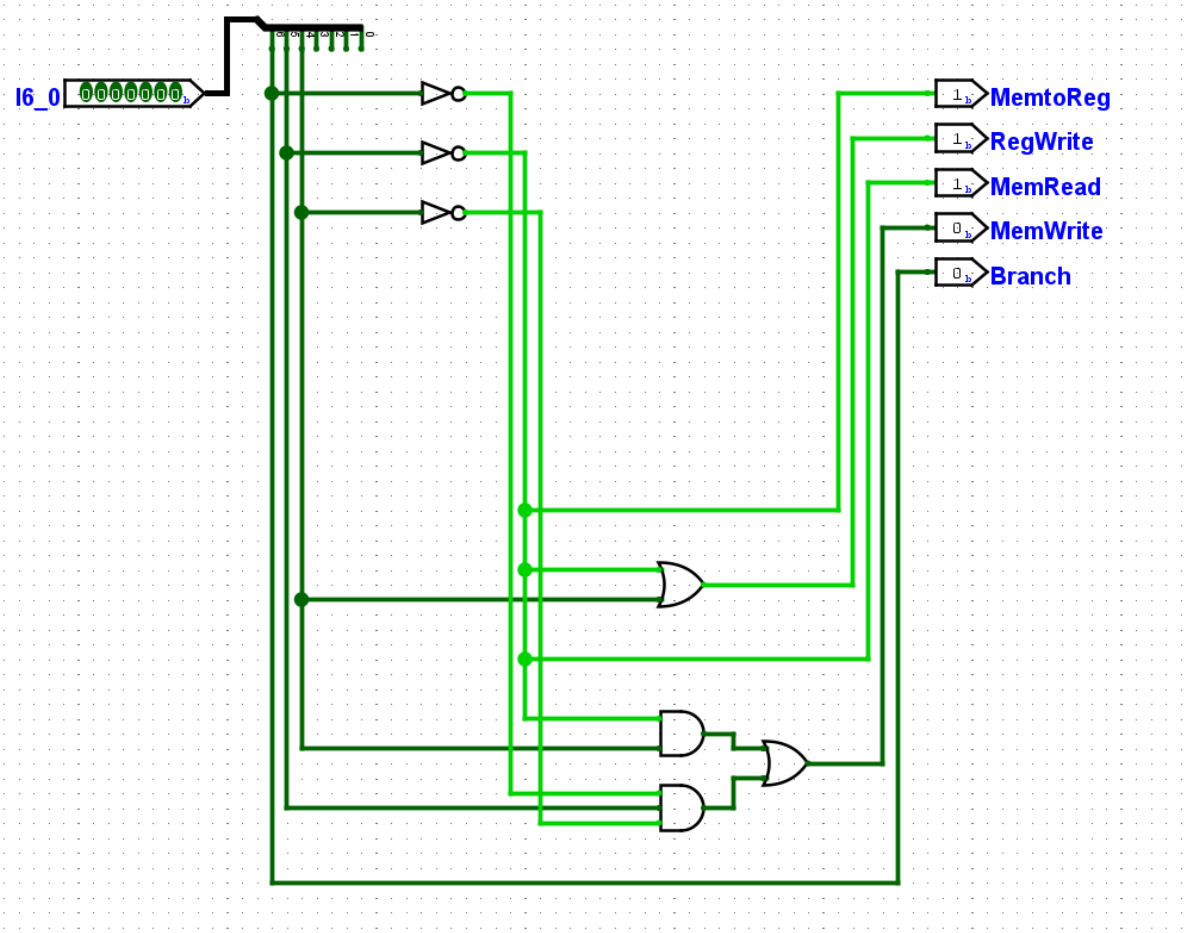
Milestone 1

ImmGen:

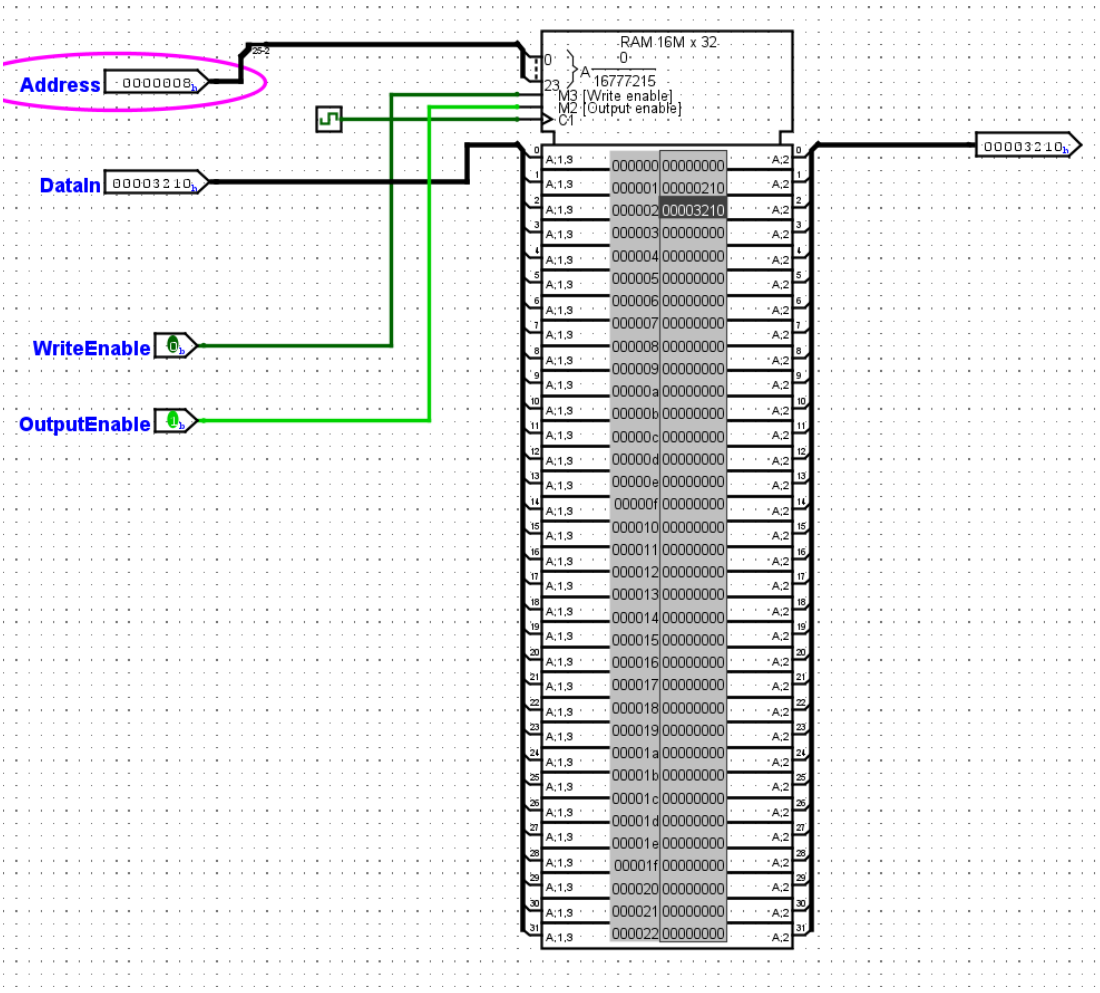


Control:

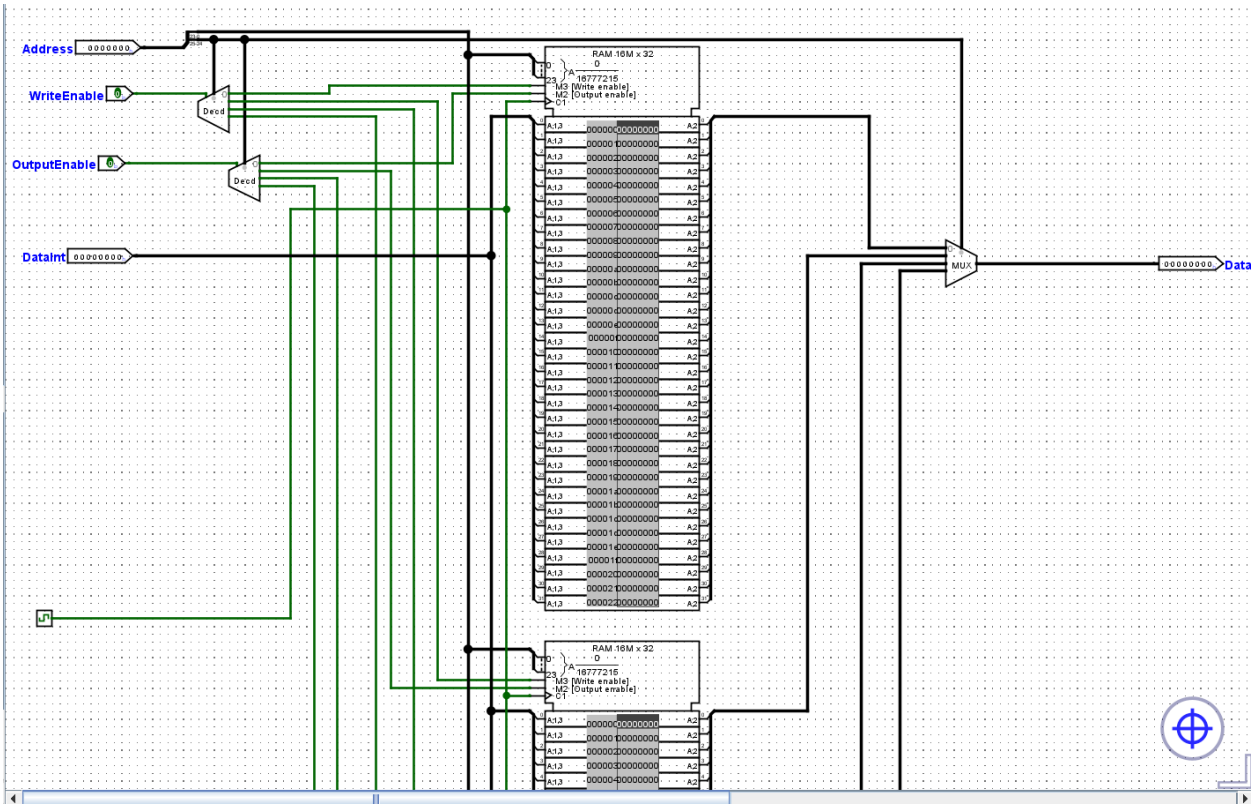
	Signal Name	R-Format	I-Format	LW	SW	BEQ
Inputs	I6	0	0	0	0	1
	I5	1	0	0	1	1
	I4	1	1	0	0	0
	I3	0	0	0	0	0
	I2	0	0	0	0	0
	I1	1	1	1	1	1
	I0	1	1	1	1	1
Outputs	Memtoreg	0	1	1	X	X
	RegWrite	1	1	1	0	0
	MemRead	0	1	1	0	0
	MemWrite	0	1	0	1	0
	Branch	0	0	0	0	1


I6_0
0000000
1
MemtoReg
1
RegWrite
1
MemRead
0
MemWrite
0
Branch

DRAM 16Mx32:


RAM 16M x 32
Address
DataIn
WriteEnable
OutputEnable
M3 [Write enable]
M2 [Output enable]
C1
16777215
00003210

DRAM 64Mx32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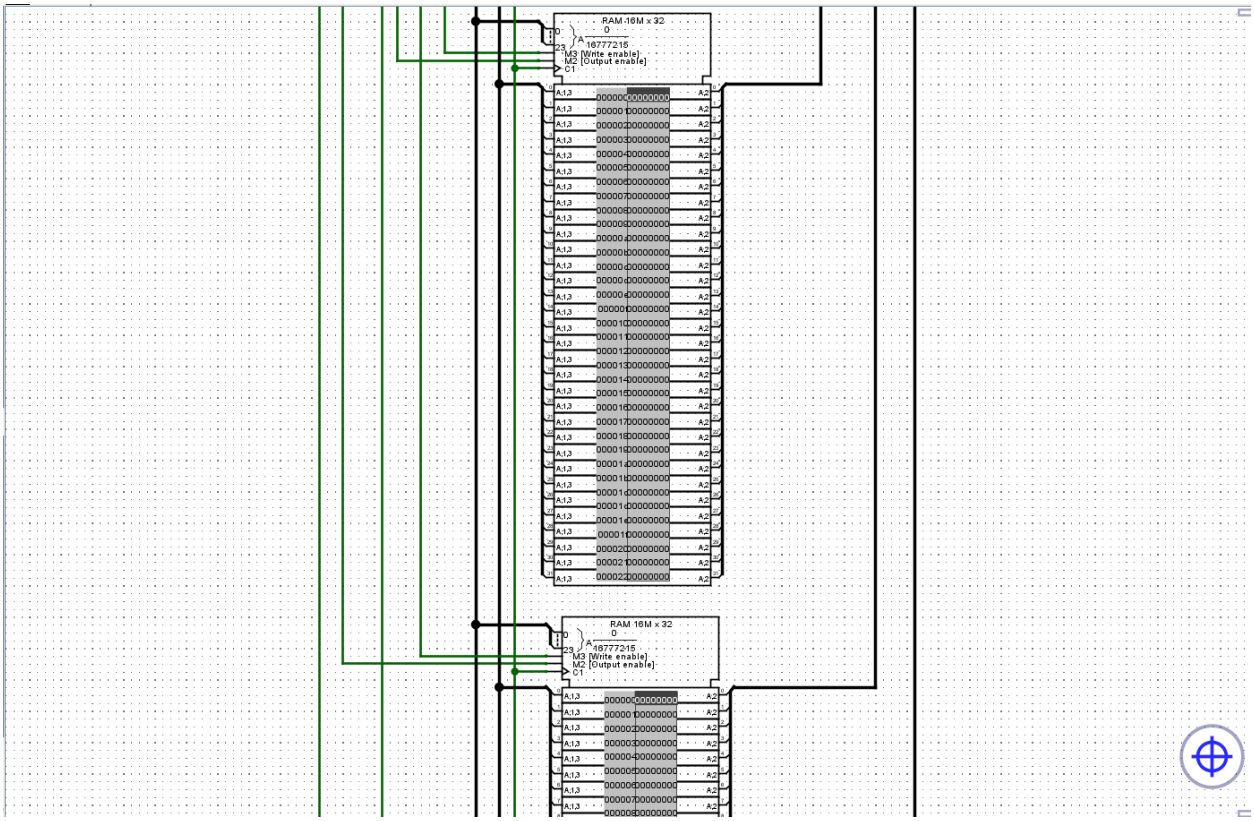
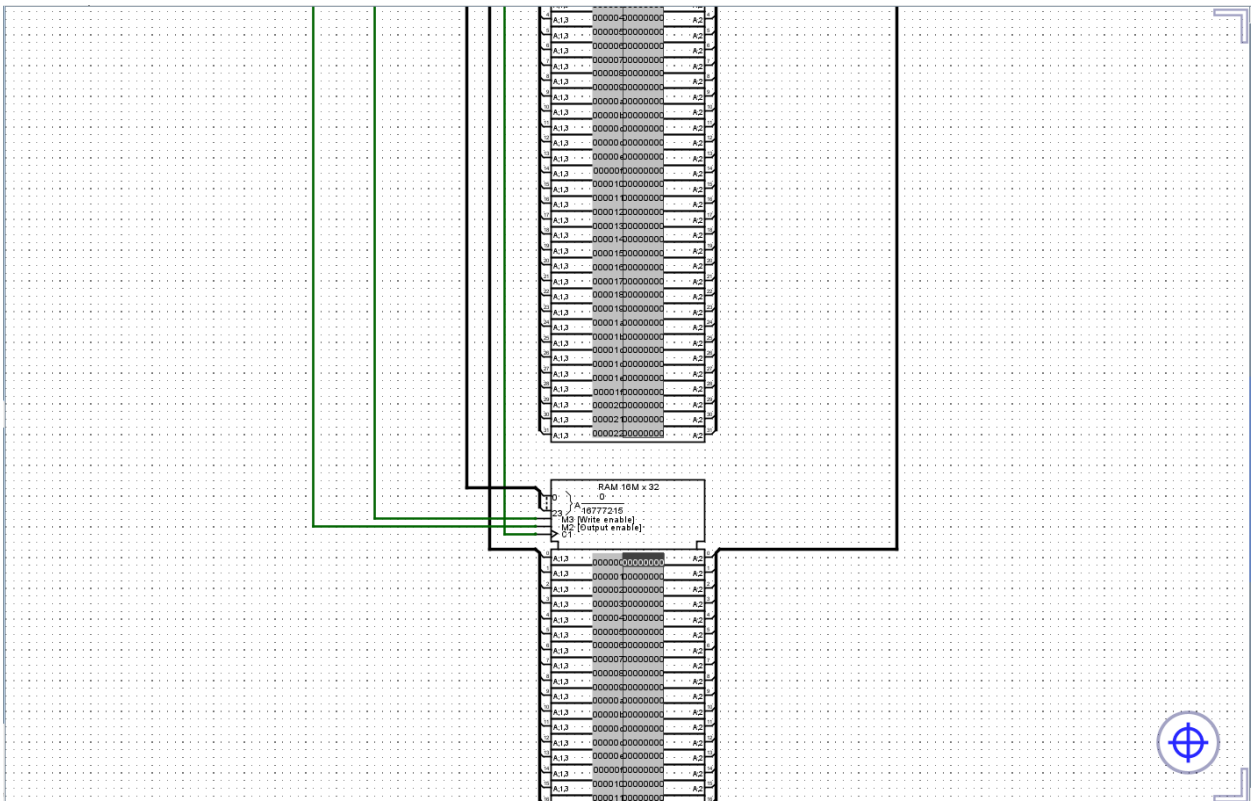
OutputEnable
DataInt
Decd
Decd
RAM 16M x 32
MUX
Data


RAM 16M x 32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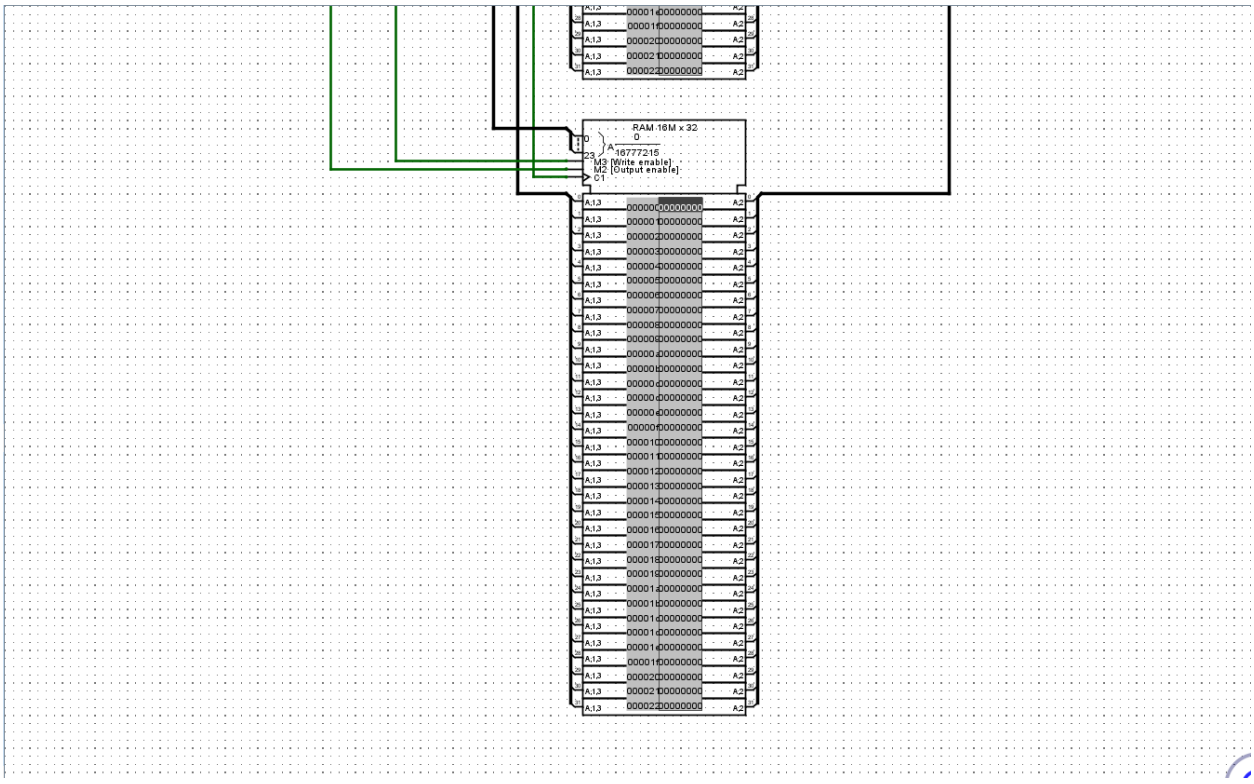
RAM 16M x 32
0
A
16777215
M3 [Write enable]
M2 [Output enable]
C1