UNIVERSITY OF SOUTHAMPTON

COMP2323

Computer Systems II Logbook

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Contents

Week X: Example Topic

1.1 Task Outline

Objective: [e.g., Sampling the potentiometer at 10kHz.]

Design Decision

[Explain your choice here. e.g.:]

- **Selected Mode:** Circular Buffer DMA.
- **Justification:** Polling would consume 100% CPU at this sample rate. DMA allows the CPU to sleep, reducing power.

1.2 Implementation

[Brief note on register setup, e.g., "ADC1 is triggered by TIM3 TRGO event."]

```c
// src/week-01/example.c
#include <stdio.h>

int main(void) {
    // Placeholder for Task 1
    return 0;
}
```

Listing 1.1: Register-Level Driver

1.3 Verification & Constraints

placeholder_trace.png

Figure 1.1: Logic analyzer trace showing 100us sample interval.

Note for Exam

- **Bug Found:** The ADC value drifted when WiFi was enabled.
- **Fix:** Added a 0.1uF decoupling capacitor to the VREF pin.
- **Constraint:** Maximum sampling frequency is 2.4 MSPS on this bus.

Exam Quick Reference

A.1 Bitwise Cheat Sheet

- **Set Bit 3:** `REG |= (1 << 3);`
- **Clear Bit 3:** `REG &= ~(1 << 3);`
- **Toggle Bit 3:** `REG ^= (1 << 3);`
- **Check Bit 3:** `if (REG & (1 << 3))`

A.2 Common Register Maps

```
#define GPIOA_MODER  (*((volatile uint32_t *) 0x48000000))
#define RCC_AHB1ENR  (*((volatile uint32_t *) 0x40023830))
```