# Lab 2 Report

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**Section: 15300**

## Checklist:

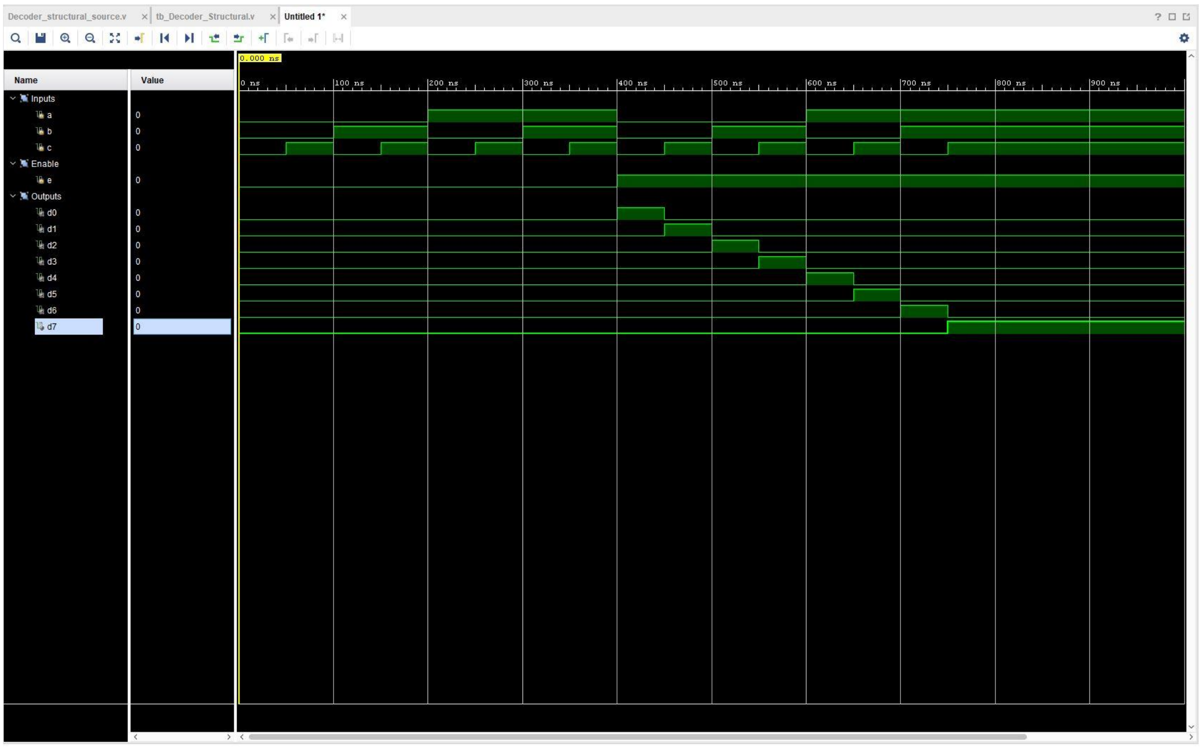
**Part 1 –**

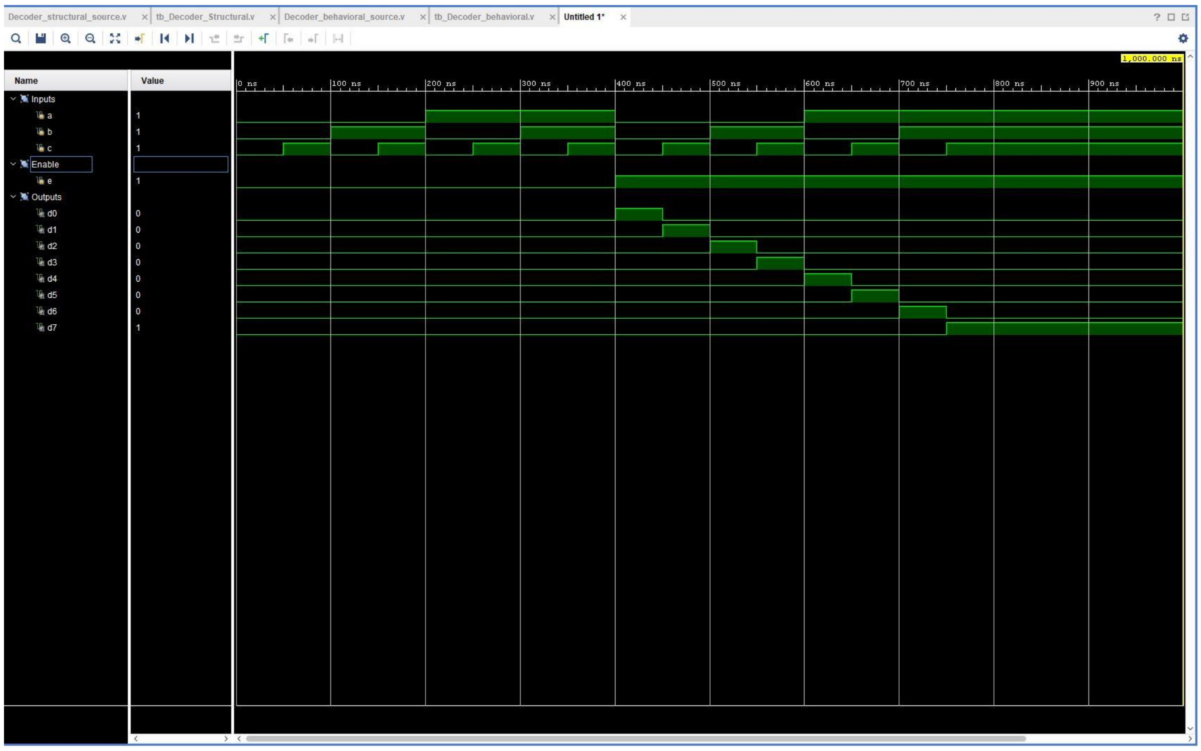
i. Simulation waveforms for Part 1 for Structural as well as Behavioral modelling (Screenshots)

**Part 2 –**

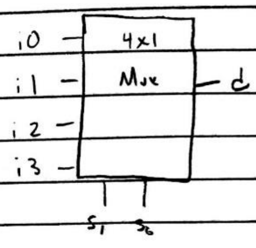
ii. Truth table of the function
iii. Algebraic expression of the logic function
iv. Logic circuit schematic
v. Verilog codes for module and testbench for structural modelling
vi. Simulation waveform for structural modelling (Screenshot)
vii. Verilog codes for module and testbench for behavioral modelling
viii. Simulation waveform for behavioral modelling (Screenshot)

***Note** –> The Verilog codes should be copied in your lab report, and the actual Verilog (.v) files need to be zipped and submitted as well on Canvas. You are not allowed to change your Verilog codes after final submission as the TAs may download the submitted codes from Canvas during checkouts. For the truth table, algebraic expression and circuit schematic, you are free to draw it on paper and then put the pictures in your lab report, but please make sure it is legible for the TAs to grade it properly.*

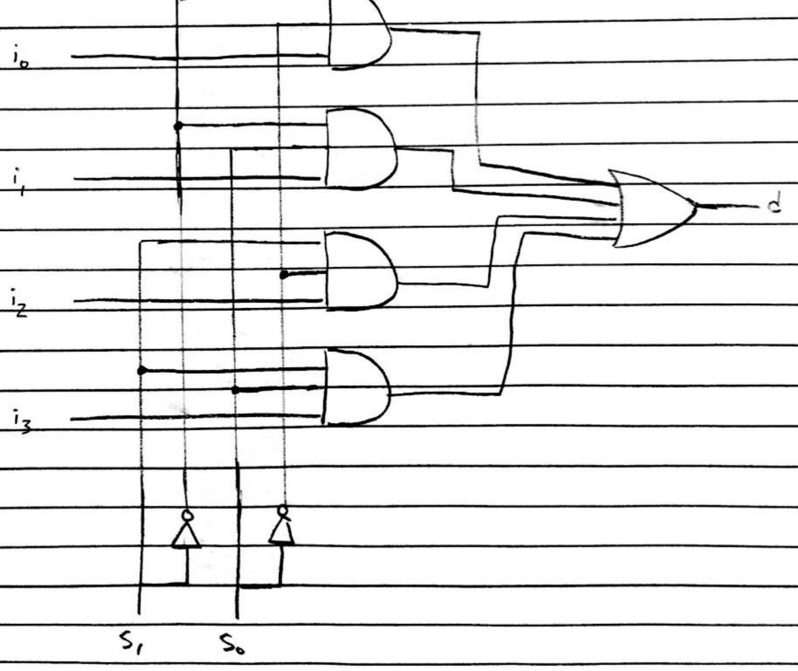

Decoder_structural_source.v
tb_Decoder_Structural.v
Untitled 1*
0.000 ns
Name
Value
Inputs
a 0
b 0
c 0
Enable
e 0
Outputs
d0 0
d1 0
d2 0
d3 0
d4 0
d5 0
d6 0
d7 0
0 ns
100 ns
200 ns
300 ns
400 ns
500 ns
600 ns
700 ns
800 ns
900 ns


Decoder_structural_source.v
tb_Decoder_Structural.v
Decoder_behavioral_source.v
tb_Decoder_behavioral.v
Untitled 1*
1,000.000 ns
Name
Value
Inputs
a 1
b 1
c 1
Enable
e 1
Outputs
d0 0
d1 0
d2 0
d3 0
d4 0
d5 0
d6 0
d7 1
0 ns
100 ns
200 ns
300 ns
400 ns
500 ns
600 ns
700 ns
800 ns
900 ns

| $S_1$ | $S_0$ | $I_0$ | $I_1$ | $I_2$ | $I_3$ | d |
|---|---|---|---|---|---|---|
| 0 | 0 | 0 | x | x | x | 0 |
| 0 | 0 | 1 | x | x | x | 1 |
| 0 | 1 | x | 0 | x | x | 0 |
| 0 | 1 | x | 1 | x | x | 1 |
| 1 | 0 | x | x | 0 | x | 0 |
| 1 | 0 | x | x | 1 | x | 1 |
| 1 | 1 | x | x | x | 0 | 0 |
| 1 | 1 | x | x | x | 1 | 1 |



$d = s_1's_0'\,i0 + s_1's_0\,i1 + s_1s_0'\,i2 + s_1s_0\,i3$



**Structural Module**

```
`timescale 1ns / 1ps
module Mux_structural(
   input s1,
   input s0,
   input i0,
   input i1,
   input i2,
   input i3,
   output d
   );

   //defining wires for not signals
   wire s1_not, s0_not;
   //defining wires into or gate
   wire d0, d1, d2, d3;

   //instantiating not gates as per the schematic
   not n0 (s0_not, s0);
   not n1 (s1_not, s1);

   //instantiating and gates as per the schematic
   and g0 (d0, i0, s1_not, s0_not);
   and g1 (d1, i1, s1_not, s0);
   and g2 (d2, i2, s1, s0_not);
   and g3 (d3, i3, s1, s0);
   or g4 (d, d0, d1, d2, d3);

endmodule
```

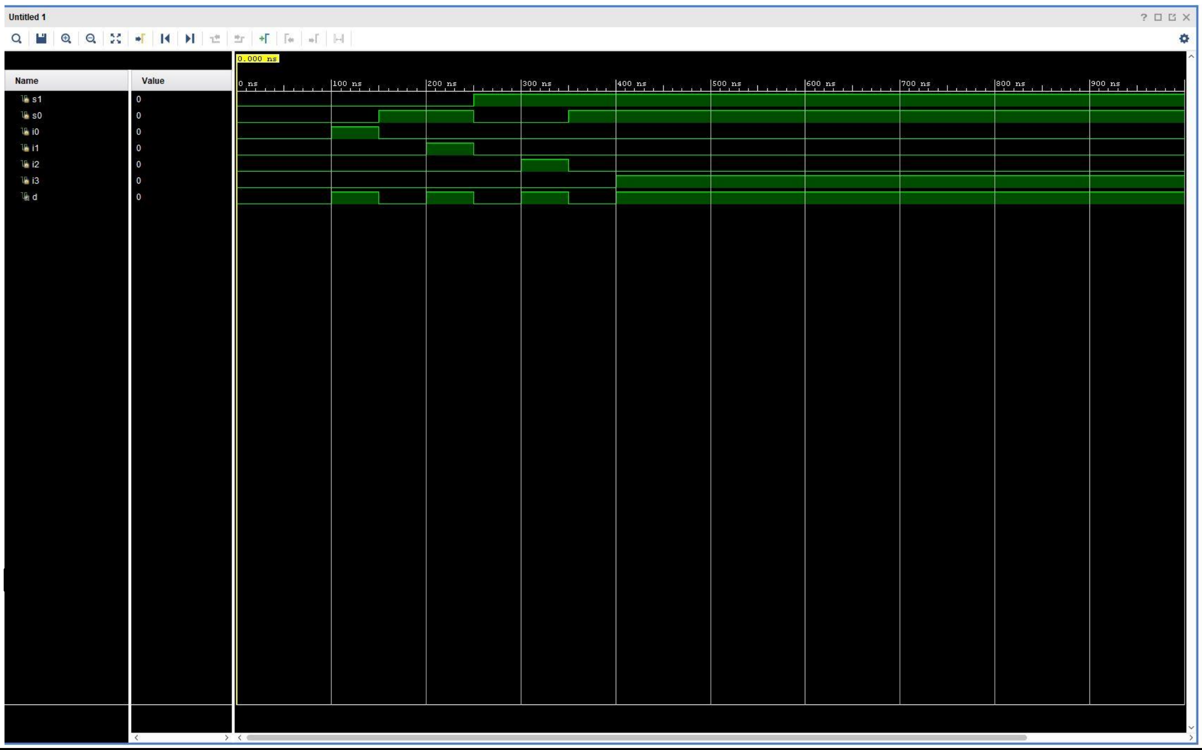
**Structural Testbench**

```
`timescale 1ns / 1ps

module tb_Mux_structural;

// Inputs to be defined as registers
reg s1;
reg s0;
reg i0;
reg i1;
reg i2;
reg i3;

// Outputs to be defined as wires
wire d;

// Instantiate the Unit Under Test (UUT)
Mux_structural uut (
   .s1(s1),
   .s0(s0),
   .i0(i0),
   .i1(i1),
   .i2(i2),
   .i3(i3),
   .d(d)
);
```

```
initial begin
// initialize inputs
s1 = 0;
s0 = 0;
i0 = 0;
i1 = 0;
i2 = 0;
i3 = 0;

// wait 50ns for global reset to finish
#50;

s1 = 0;
s0 = 0;
i0 = 0;
i1 = 0;
i2 = 0;
i3 = 0;
#50;

s1 = 0;
s0 = 0;
i0 = 1;
i1 = 0;
i2 = 0;
i3 = 0;
#50;
```

```
s1 = 0;
s0 = 1;
i0 = 0;
i1 = 0;
i2 = 0;
i3 = 0;
#50;

s1 = 0;
s0 = 1;
i0 = 0;
i1 = 1;
i2 = 0;
i3 = 0;
#50;

s1 = 1;
s0 = 0;
i0 = 0;
i1 = 0;
i2 = 0;
i3 = 0;
#50;

s1 = 1;
s0 = 0;
i0 = 0;
i1 = 0;
i2 = 1;
i3 = 0;
```

```
#50;

s1 = 1;
s0 = 1;
i0 = 0;
i1 = 0;
i2 = 0;
i3 = 0;
#50;

s1 = 1;
s0 = 1;
i0 = 0;
i1 = 0;
i2 = 0;
i3 = 1;
#50;

end
endmodule
```



**Behavioral Module**

```
`timescale 1ns / 1ps
module Mux_behavioral(
    input s1,
    input s0,
    input i0,
    input i1,
    input i2,
    input i3,
    output reg d
    );

    always @(s1, s0, i0, i1, i2, i3)
    begin

    case ({s1, s0})
        2'b00 : d = i0;
        2'b01 : d = i1;
        2'b10 : d = i2;
        2'b11 : d = i3;
    endcase

    end

endmodule
```

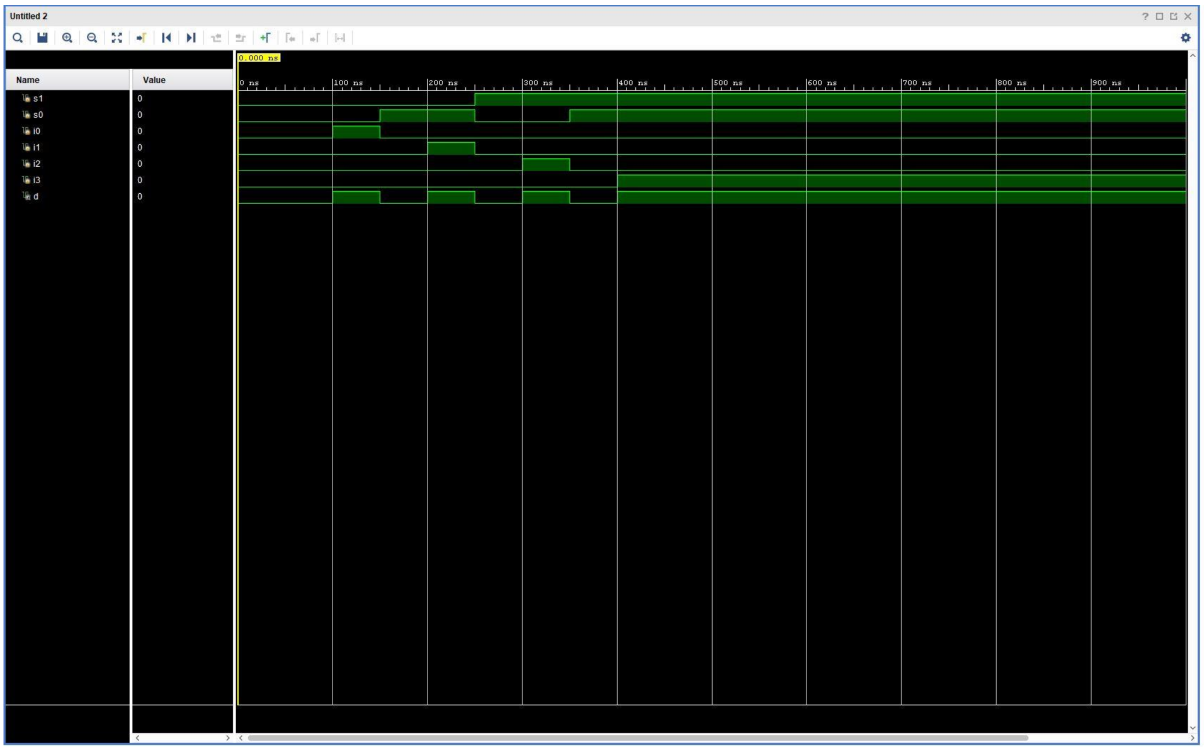
**Behavioral Testbench**

```
`timescale 1ns / 1ps

module tb_Mux_behavioral;

// Inputs to be defined as registers
reg s1;
reg s0;
reg i0;
reg i1;
reg i2;
reg i3;

// Outputs to be defined as wires
wire d;

// Instantiate the Unit Under Test (UUT)
Mux_behavioral uut (
   .s1(s1),
   .s0(s0),
   .i0(i0),
   .i1(i1),
   .i2(i2),
   .i3(i3),
   .d(d)
);
```

```
initial begin
// initialize inputs
s1 = 0;
s0 = 0;
i0 = 0;
i1 = 0;
i2 = 0;
i3 = 0;


// wait 50ns for global reset to finish
#50;

s1 = 0;
s0 = 0;
i0 = 0;
i1 = 0;
i2 = 0;
i3 = 0;
#50;

s1 = 0;
s0 = 0;
i0 = 1;
i1 = 0;
i2 = 0;
i3 = 0;
#50;
```

```
s1 = 0;
s0 = 1;
i0 = 0;
i1 = 0;
i2 = 0;
i3 = 0;
#50;

s1 = 0;
s0 = 1;
i0 = 0;
i1 = 1;
i2 = 0;
i3 = 0;
#50;

s1 = 1;
s0 = 0;
i0 = 0;
i1 = 0;
i2 = 0;
i3 = 0;
#50;

s1 = 1;
s0 = 0;
i0 = 0;
i1 = 0;
i2 = 1;
i3 = 0;
```

```
#50;

s1 = 1;
s0 = 1;
i0 = 0;
i1 = 0;
i2 = 0;
i3 = 0;
#50;

s1 = 1;
s0 = 1;
i0 = 0;
i1 = 0;
i2 = 0;
i3 = 1;
#50;
end
endmodule
```


Untitled 2
0.000 ns
Name
Value
s1 0
s0 0
i0 0
i1 0
i2 0
i3 0
d 0
0 ns
100 ns
200 ns
300 ns
400 ns
500 ns
600 ns
700 ns
800 ns
900 ns