Technical University of Denmark

31352 Power Electronics 1

Final Report

Design of 30 W Laboratory Power Supply

Group 2
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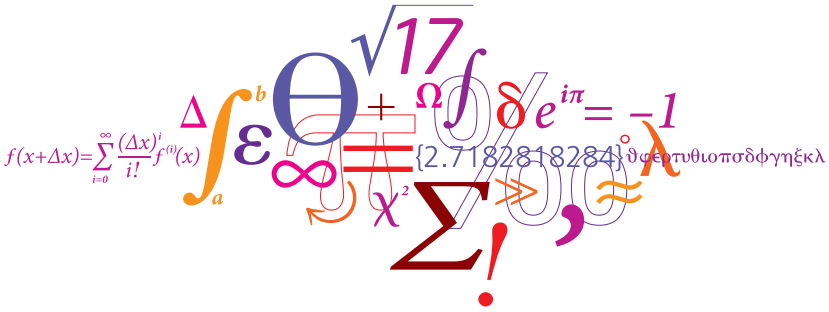

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1 | Preface (SK, CL & TK)

The aim of this project was to design an isolated laboratory power supply. The converter's efficiency and performance is for the most part considered more important than the size and weight of the laboratory supply. Firstly, four possible converter topologies are analyzed and compared for a final selection of a topology for further design. The analysis includes waveforms, modes of operation and component stress factors. For the chosen topology the magnetics are dimensioned and designed. This includes the physical configuration of windings and selection of core. This also includes an estimation of the winding and core losses based on more accurate current waveforms. An input and output filter of the converter is added to satisfy the specifications in table 1.1 while the impedance changes of the converter must also satisfy Middlebrook's stability theorem. The design of the control loop of the converter using a peak current controller to achieve desired performance, and frequency analysis of the stability is done. Finally the report includes a review and summary of the work with a conclusion.

1.1 Specifications

	Condition	Minimum	Maximum
V_{in}	-	20 V	40 V
V_{out}	-	5 V	30 V
I_{out}	-	-	1 A
$\Delta V_{out_{max}}$	Steady state	-	50mV
$\Delta V_{out_{max}}$	Load step	-	3 % of V_{out}
Input current harmonics	Steady state	-	*CISPR 13* average
Inrush current spike	-	-	*ETSI EN 300132-2*

Table 1.1: Converter Specifications.

2 | Topology Selection

In this chapter, 4 different topologies for DC-DC switch mode converters are introduced and waveforms are analyzed with ideal components. The transformer ratios are determined from an analysis of the range of duty cycles required to meet the specifications in table 1.1. The stress factors of the components in the different topologies are calculated and finally a topology is chosen for the design of the laboratory power supply.

2.1 Transformer Turns Ratio (SK, CL & TK)

M is the DC conversion ratio.

$$M = \frac{V_{out}}{V_{in}} \tag{2.1}$$

From the specifications it is seen that the minimum and maximum DC conversion ratios are:

$$M_{min} = \frac{5\text{V}}{40\text{V}} = 0.125 \tag{2.2}$$

$$M_{max} = \frac{30\text{V}}{20\text{V}} = 1.5 \tag{2.3}$$

As derived later, the conversion ratios of each converter are given by:

$$M_{flyback} = M_{SEPIC} = M_{cuk} = \frac{nD}{1-D} \tag{2.4}$$

$$M_{push-pull} = nD \tag{2.5}$$

Where D is the duty cycle and n is the transformer ratio $\frac{n_s}{n_p}$. Expressions for the maximum and minimum duty cycles can be derived by using these formulas along with the minimum and maximum conversion ratios listed in equations (2.3) and (2.3).

$$D_{flyback_{min}} = D_{SEPIC_{min}} = D_{cuk_{min}} = \frac{M_{min}}{n + M_{min}} = \frac{0.125}{n + 0.125} \tag{2.6}$$

$$D_{flyback_{max}} = D_{SEPIC_{max}} = D_{cuk_{max}} = \frac{M_{max}}{n + M_{max}} = \frac{1.5}{n + 1.5} \tag{2.7}$$

$$D_{push-pull_{min}} = \frac{n}{M_{min}} = \frac{0.125}{n} \tag{2.8}$$

$$D_{push-pull_{max}} = \frac{n}{M_{max}} = \frac{1.5}{n} \tag{2.9}$$

From this it is seen that the range of duty cycles depends on the choice of transformer turns ratio. The limitations on the duty cycle are that it cannot be higher than 1 or lower than 0. One could argue that going close to zero duty cycle is preferable compared to going close to unity, because of the risk for shoot-through. But in this report, it is decided to place the range of duty cycles symmetrically. I.e. D_{max} should be as close to 1 as D_{min} is to 0.

$$D(M_{min}) = 1 - D(M_{max}) \tag{2.10}$$

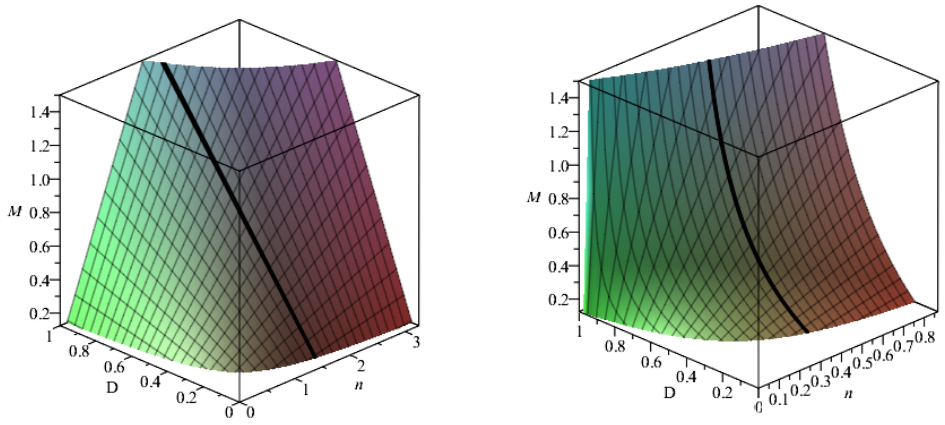
Thus equation 2.6 and 2.7 are solved for the buck-boost types with the condition of equation 2.10. Similarly for the push-pull 2.8 and 2.9 are solved with the same conditions. The results are:

$$n_{flyback} = n_{SEPIC} = n_{cuk} = 0.433 \tag{2.11}$$
$$n_{push-pull} = 1.63 \tag{2.12}$$

Which gives the following duty cycle ranges.

$$D_{flyback} = D_{SEPIC} = D_{cuk} \in [22\%, 78\%] \tag{2.13}$$
$$D_{push-pull} \in [7.7\%, 92\%] \tag{2.14}$$

These transformer turns ratios are now chosen for the converters. Fig. 2.1 illustrates how the chosen values allow for a symmetric duty cycle to produce the needed minimum and maximum DC conversion ratios.



(a) $M(n, D) = nD$

(b) $M(n, D) = \dfrac{nD}{1 - D}$

Figure 2.1: The two cases of conversion ratios with the chosen transformer turns ratios marked as black curves.

2.2 Flyback Converter (BW)

2.2.1 Schematic & Operation

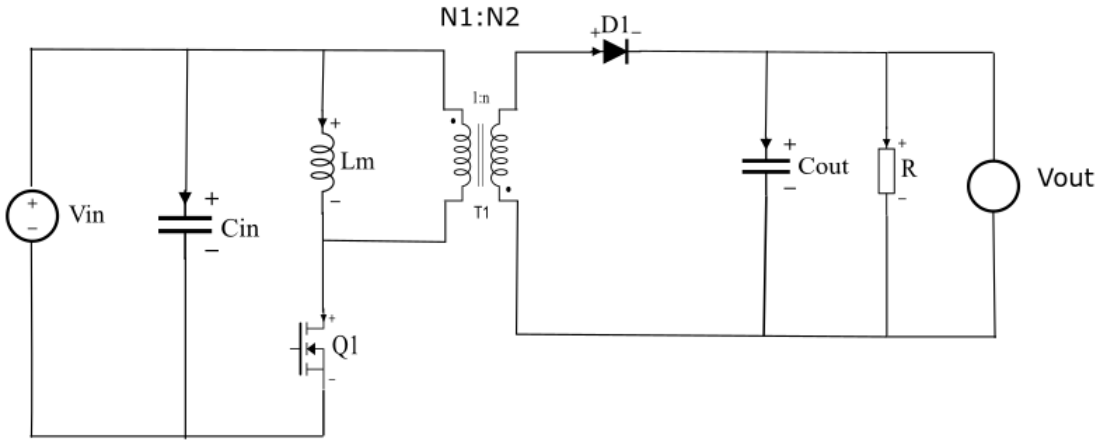


Figure 2.2: Flyback converter

The basic topology of flyback converter for the laboratory power supply is shown in Fig 2.2. According to introduction, the ratio is N1:N2= 1:n. There are two sub intervals in a duty circle. In the first interval, switch Q1 is turned on. The current flows from the source to the primary side of the transformer into the dot and then down to the Q1. The energy is stored into the transformer. In the secondary side, the current flows from the capacitor to the output and then go back to the capacitor. The diode D1 is in reverse bias in this condition so there is no current in D1.

In the second period, switch Q1 is turned off. The current flowing from the source to the input capacitor. And the voltage potential across Lm changes the direction. The current flowing through the primary side induces a current in the secondary side flowing from the transformer to D1, Cout, Rload and then back to the dot.

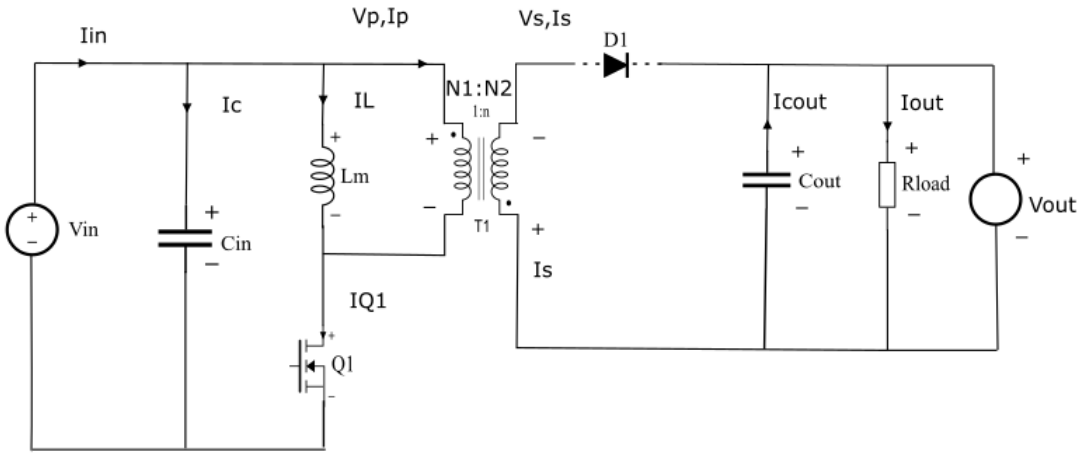


Figure 2.3: First subinterval of flyback converter

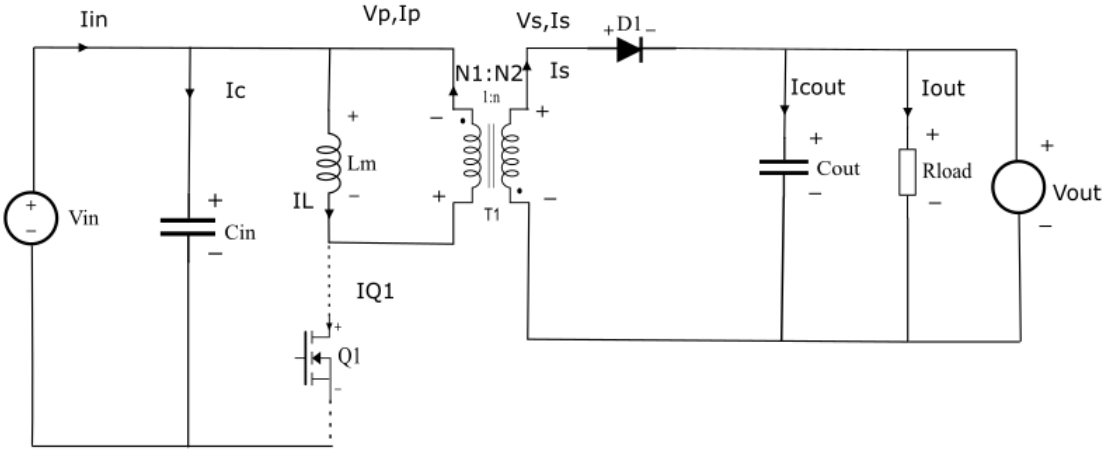


Figure 2.4: Second subinterval of flyback converter

2.2.2 Voltage & Current Plots

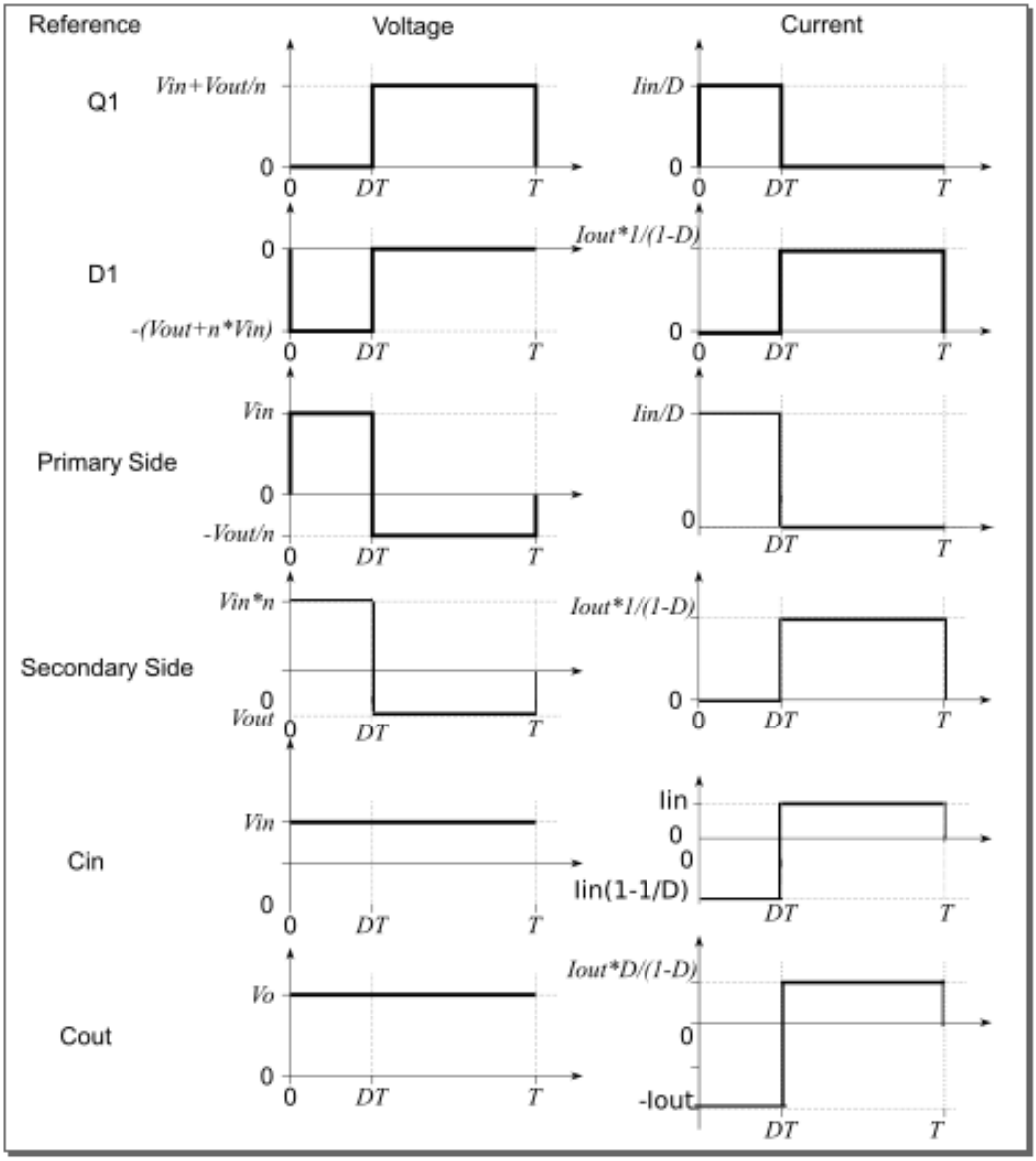


Figure 2.5: Waveforms of Flyback Converter

2.2.3 Derivation of Equations

The calculation in the below are based on the CCM and the output voltage is 30V; output current is 1A. According to the Introduction, when the transformer turns ratio $n = 0.43$, the range of $D_{flyback}$ is from 0.22 to 0.78.

Duty cycle and Transformer turns calculations:

From the voltage balance equation of primary windings the function can be got:

$$V_{in} * DT = (V_o/n)(1 - D) * T \tag{2.15}$$

$$\frac{V_o}{V_{in}} = \frac{nD}{1 - D} \tag{2.16}$$

$$D = \frac{V_o}{V_{in} * n + V_o} \tag{2.17}$$

when V_{in} =40 V:

$$D = \frac{V_o}{V_{in} * n + V_o} = \frac{30}{40 * 0.43 + 30} = 0.63 \tag{2.18}$$

when V_{in} =20 V:

$$D = \frac{V_o}{V_{in} * n + V_o} = \frac{30}{20 * 0.43 + 30} = 0.78 \tag{2.19}$$

Input current calculations:

Because all components are consider to be ideal, therefore the input power is equal to the output power:

$$V_{in} * I_{in} = V_o * I_{out} \tag{2.20}$$

$$I_{in} = \frac{V_o * I_{out}}{V_{in}} \tag{2.21}$$

when V_{in} =40 V:

$$I_{in} = \frac{30 * 1}{40} = 0.75\,\text{A} \tag{2.22}$$

when V_{in} =20 V:

$$I_{in} = \frac{30 * 1}{20} = 1.5\,\text{A} \tag{2.23}$$

Switch voltages and currents calculations:

As it could be seen from the wave,

$$V_{rms} = \sqrt{\frac{1}{T}(\int_{DT}^{T}((V_o/n) + V_{in})^2 dt} = V_{in}D\sqrt{\frac{1}{1 - D}} \tag{2.24}$$

$$I_{rms} = \sqrt{\frac{1}{T}(\int_{0}^{DT}(\frac{I_{in}}{D})^2 dt)} = \frac{I_{in}}{\sqrt{D}} \tag{2.25}$$

Diode voltages and currents calculations

$$V_{rms} = \sqrt{\frac{1}{T}(\int_0^{DT}(-(V_o + n * V_{in}))^2 dt} = V_{out}\frac{1}{\sqrt{D}} \tag{2.26}$$

$$V_{max} = V_o + n * V_{in} \tag{2.27}$$

$$I_{rms} = \sqrt{\frac{1}{T}(\int_{DT}^{T}(I_{out} * (\frac{1}{1-D}))^2 dt)} = I_{out}\sqrt{\frac{1}{1-D}} \tag{2.28}$$

Primary Windings voltages and currents calculations

$$V_{rms} = \frac{1}{T}[(\int_0^{DT}(V_{in})dt + \int_{DT}^{T}(V_o/n)dt] = 2V_{out}\frac{1-D}{n} \tag{2.29}$$

$$I_{rms} = \sqrt{\frac{1}{T}(\int_0^{DT}(\frac{I_{in}}{D})^2 dt} = I_{in}\frac{1}{\sqrt{D}} \tag{2.30}$$

Secondary Windings voltages and currents calculations

$$V_{rms} = \frac{1}{T}(\int_{DT}^{T}(V_{in} * n)dt + \int_{DT}^{T}\|V_o\|dt) = 2V_o(1-D) \tag{2.31}$$

$$I_{rms} = \sqrt{\frac{1}{T}(\int_{DT}^{T}(I_{out} * \frac{1}{1-D})^2 dt)} = I_{out}\sqrt{\frac{1}{1-D}} \tag{2.32}$$

C_{in} Voltages and currents calculations

$$V_{max} = V_{in} \tag{2.33}$$

$$I_{rms} = I_{rms} = \sqrt{\frac{1}{T}(\int_{DT}^{T}(I_{in}(1-\frac{1}{D}))^2 dt + \int_{DT}^{T}(I_{in})^2 dt)} = I_{in}\sqrt{\frac{1-D}{D}} \tag{2.34}$$

C_{out}Voltages and currents calculations

$$V_{max} = V_{out} \tag{2.35}$$

$$I_{rms} = \sqrt{\frac{1}{T}[(\int_0^{DT}(-I_{out})^2 dt + \int_{DT}^{T}(I_{out} * (\frac{D}{1-D}))^2 dt]} = I_{out}\sqrt{\frac{D}{1-D}} \tag{2.36}$$

2.2.4 Summary of Formulas

	Symbol	Unit	Case 1	Case 2	Case 3	Case 4	Maximum	Expression
Turns ratio	n	-	0.43	0.43	0.43	0.43	0.43	-
Output voltage	V_{out}	V	5.00	30.00	5.00	30.00	30.00	-
Output current	I_{out}	A	1.00	1.00	1.00	1.00	1.00	-
Input voltage	V_{in}	V	20.00	20.00	40.00	40.00	40.00	-
Input current	I_{in}	A	0.25	1.50	0.13	0.75	1.50	$\frac{V_{out}I_{out}}{V_{in}}$
Duty-cycle	D	-	0.37	0.78	0.23	0.63	0.78	$\frac{V_{out}}{V_{in} \cdot n + Vo}$
FET Q1	max(VQ1)	V	31.63	89.77	51.63	109.77	109.77	$\frac{V_o}{n} + V_{in}$
	RMS(IQ1)	A	0.41	1.70	0.26	0.94	1.70	$\frac{I_{in}}{\sqrt{D}}$
Diode D1	|max(VD1)|	V	13.60	38.60	22.20	47.20	47.20	$Vout + nV_{in}$
	RMS(ID1)	A	1.26	2.12	1.14	1.66	2.12	$I_{out}\sqrt{\frac{1}{1-D}}$
Primary Winding	<|Vprim|>	V	14.17	31.09	18.02	50.85	50.85	$2V_{out}(\frac{1-D}{n})$
	RMS(Iprim)	A	0.41	1.70	0.26	0.94	1.70	$I_{in}\sqrt{\frac{1}{D}}$
Secondary Winding	<|Vsec|>	V	6.32	13.37	7.75	21.86	21.86	$2V_o(1-D)$
	RMS(Isec)	A	1.26	2.12	1.14	1.66	2.12	$I_{out}\sqrt{\frac{1}{1-D}}$
Capacitor Cin	max(Vcin)	V	20.00	20.00	40.00	40.00	40.00	Vin
	RMS(Icin)	A	0.33	0.80	0.23	0.57	0.80	$I_{in}\sqrt{\frac{1-D}{D}}$
Capacitor Cout	max(Vcout)	V	5.00	30.00	5.00	30,00	30,00	$Vout$
	RMS(Icout)	A	0.76	1.87	0.54	1.32	1.87	$I_{out}\sqrt{\frac{D}{1-D}}$
	Q1 CSF						38.76	
	D1 CSF						11.11	
	SCSF total						49.87	
	Lprim CSF						8.32	
	Lsec CSF						2.38	
	WCSF total						10.7	
	Cin CSF						1.15	
	Cout CSF						3.49	
	CCSF total						4.64	

Table 2.1: Maximum, RMS and Average absolute values for the Components

2.2.5 Components Stress Factor

SCSF voltages and currents calculations:

$$SCSF_{Q1} = \frac{max(v_{Q1})^2 * RMS(I_{Q1})^2}{P^2} = 38.76 \tag{2.37}$$

$$SCSF_{D1} = \frac{max(v_{D1})^2 * RMS(I_{D1})^2}{P^2} = 11.11 \tag{2.38}$$

$$SCSF_{total} = 49.87 \tag{2.39}$$

WCSF voltages and currents calculations

$$WCSF_{Lpri} = \frac{< |(v_{Lpri}| >^2 * RMS(I_{Lpri})^2}{P^2} = 8.32 \tag{2.40}$$

$$WCSF_{Lsec} = \frac{< |(v_{Lsec}| >^2 * RMS(I_{Lsec})^2}{P^2} = 2.38 \tag{2.41}$$

$$WCSF_{total} = 10.70 \tag{2.42}$$

CCSF voltages and currents calculations

$$CCSF_{C_{in}} = \frac{(V_{C_{in}})^2 * RMS(I_{C_{in}})^2}{P^2} = 1.15 \tag{2.43}$$

$$CCSF_{C_o} = \frac{(V_{C_o})^2 * RMS(I_{C_o})^2}{P^2} = 3.49 \tag{2.44}$$

$$CCSF_{total} = 4.64 \tag{2.45}$$

2.2.6 Advantages

- Compared with other three topologies the circuit of flyback converter is made up with fewer components which also decrease the size and the cost of the converter.
- Lower voltage rating on secondary components

2.2.7 Advantages

- Usually used in low power supply situation.
- Because of leakage inductance, the spike and ringing of current wave is high increasing the power loss.
- Half of core material B-H loop is utilized

2.3 SEPIC Converter (SK)

2.3.1 Schematic & Operation

The schematic of the SEPIC converter can be seen in fig 2.6. The operation mode of the converter when the switch is on can be seen in fig 2.7 and when the switch is off in fig 2.8.

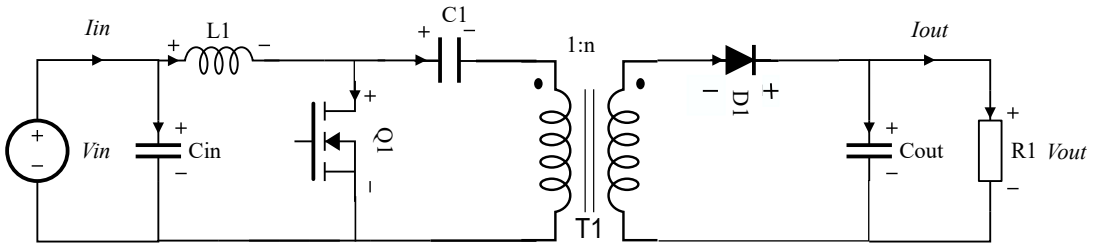


Figure 2.6: The schematic of the SEPIC converter

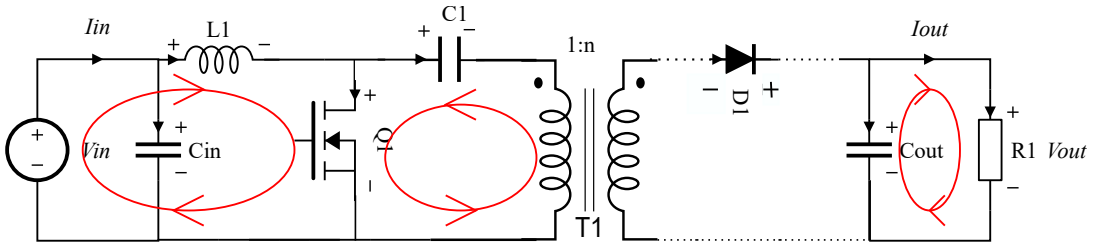


Figure 2.7: First interval. $Q1$ is closed, $D1$ is blocking

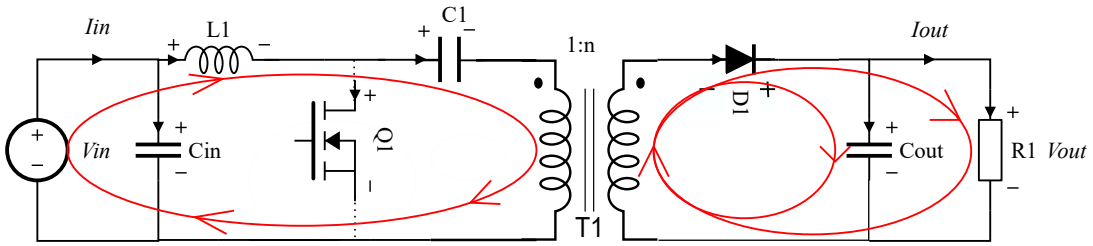


Figure 2.8: Second interval. $Q1$ is open, $D1$ is conducting

The analysis and calculations of the SEPIC is based on the model where the transformer primary side is replaced by an ideal transformer where all current and voltage is transformed to the secondary winding, in parallel with an ideal magnetisation inductor. This is seen in fig 2.9. The currents used for the analysis are labelled. I1 is the input current through L1 and i2 is the inductor current in LM. Both currents are assumed constant as capacitors and inductors in this analysis is assumed ideal. Is is the current through the diode on the secondary side. All currents are in the directions of the arrows in the figure.

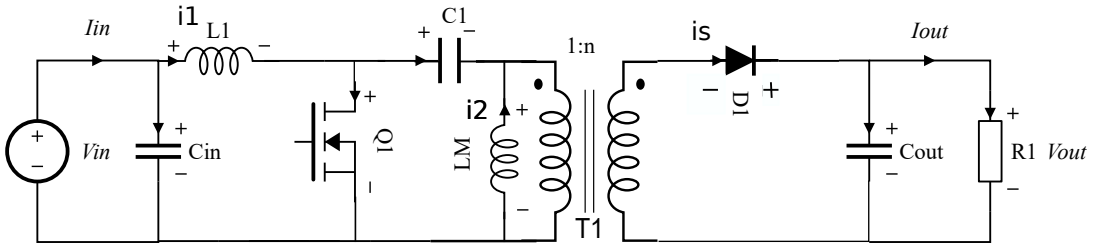


Figure 2.9: Converter with LM

2.3.2 Voltage & Current Plots

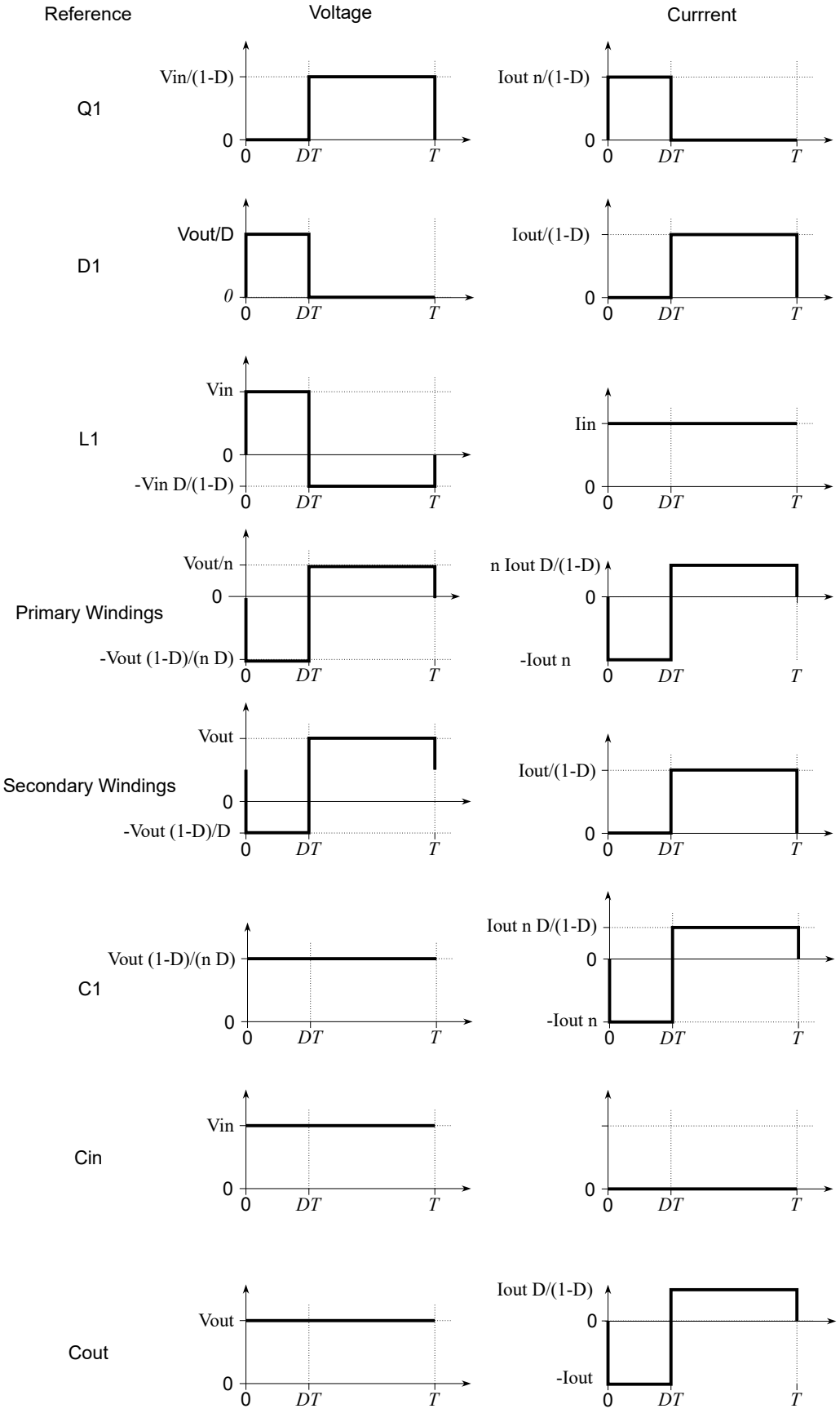


Figure 2.10: Waveforms of the isolated SEPIC converter

2.3.3 Derivation of Equations

The currents in the circuit were analyzed using the model of the transformer where there is a magnetization inductor in parallel with the primary windings of the transformer and then the currents are defined:

i1=Iin is the current in L1, i2 is the current in LM; the magnetisation inductor, Is is the current in the diode when it is conducting and Iout is the output current. Later the windings are just treated as the transformer in series with the capacitor; the current through C1 is equal to the current in the primary side, but when the diode is blocking on the secondary side a current still flows in the primary side, just only affecting LM.

Iin,i1,i2,Is are related to Iout:

$$i1 = \frac{nD \cdot Iout}{1-D} \tag{2.46}$$

$$i2 = Iout \cdot n \tag{2.47}$$

$$Is = \frac{Iout}{1-D} \tag{2.48}$$

$$Iin = i1 \tag{2.49}$$

When the switch is on the voltage across it is Vin. The voltage across the switch when it is off is found by using the voltage balance on L1, and is found to be:

$$VinD + (1-D)(Vin - V_{q1,off}) = 0 \tag{2.50}$$

$$\Updownarrow \tag{2.51}$$

$$V_{q1,off} = \frac{Vin}{1-D} \tag{2.52}$$

During the switch's off-time the diode conducts; the voltage across it is 0. The voltage across the primary windings are equal to the output voltage divided by the turns ratio. The voltage across C1 is equal to $V_{q1,off}$ since the average voltage across the windings must be 0.

$$\frac{Vin}{1-D} - Vin = \frac{Vout}{n} \tag{2.53}$$

$$\Updownarrow \tag{2.54}$$

$$D = \frac{Vout}{nVin + Vout} \tag{2.55}$$

RMS of currents

$$Iq1RMS = \sqrt{\frac{1}{T}\int_0^T iq1^2 dt} = \sqrt{\frac{1}{T}\int_0^{DT} (i1+i2)^2 dt + \frac{1}{T}\int_{DT}^T 0 dt} = \sqrt{D}\frac{Ioutn}{1-D} \tag{2.56}$$

$$Id1RMS = \sqrt{\frac{1}{T}\int_0^T id1^2 dt} = \sqrt{\frac{1}{T}\int_0^{DT} 0 dt + \frac{1}{T}\int_{DT}^T \left(\frac{i1+i2}{n}\right)^2 dt} = \sqrt{\frac{Iout^2}{1-D}} \tag{2.57}$$

$$ICoutRMS = \sqrt{\frac{1}{T}\int_0^T Icout^2 dt} = \sqrt{\frac{1}{T}\int_0^{DT} (-Iout)^2 dt + \frac{1}{T}\int_{DT}^T (Is - Iout)^2 dt} = Iout\sqrt{\frac{D}{1-D}} \tag{2.58}$$

$$IC1RMS = \sqrt{\frac{1}{T}\int_0^T IC1^2 dt} = \sqrt{\frac{1}{T}\int_0^{DT} i2^2 dt + \frac{1}{T}\int_{DT}^T i1^2 dt} = nIout\sqrt{\frac{D}{1-D}} \tag{2.59}$$

The primary windings are in series with C1 so they have the same currents, and the secondary windings are in series with D1 so they have the same currents. L1 is in series with the source so the RMS current is equal to the DC current Iin.

Average absolute voltage across inductors

$$\frac{1}{T}\int_0^T |vL1|dt = \frac{1}{T}\int_0^{DT} |Vin|dt + \frac{1}{T}\int_{DT}^T \left|-Vin\frac{D}{1-D}\right| dt = \frac{2Vout(1-D)}{n} \tag{2.60}$$

$$\frac{1}{T}\int_0^T |vprim|dt = \frac{1}{T}\int_0^{DT} \left|-\frac{Vout(1-D)}{nD}\right| dt + \frac{1}{T}\int_{DT}^T \left|\frac{Vout}{n}\right| = \frac{2Vout(1-D)}{n} \tag{2.61}$$

Since the voltage on the secondary side is transformed from the primary side the voltage is equal to the primary multiplied by n.

$$\frac{1}{T}\int_0^T |vsec|dt = 2Vout(1-D) \tag{2.62}$$

2.3.4 Summary of Formulas and Component Stress Factors

A summary of the expressions for the different voltages and currents are listen below. The component stress factor is calculated from the values in the table based on the following equations, where P is the maximum output power of 30W. The maximum values are used.

Semiconductor component stress factor:

$$SCSF = \frac{v_{pk}^2 \cdot I_{RMS}^2}{P^2} \tag{2.63}$$

Winding component stress factor:

$$WCSF = \frac{<|v|>^2 \cdot I_{RMS}^2}{P^2} \tag{2.64}$$

Capacitor component stress factor:

$$CCSF = \frac{v_{pk}^2 \cdot I_{RMS}^2}{P^2} \tag{2.65}$$

Table 2.2: Summary of the 4 corner cases

	Symbol	Unit	Case 1	Case 2	Case 3	Case 4	Max	CSF	Expression
Turns ratio	n		0,43	0,43	0,43	0,43	0,43		
Output voltage	Vo	V	5,00	5,00	30,00	30,00	30,00		
Output current	Io	A	1,00	1,00	1,00	1,00	1,00		
Input voltage	Vin	V	20,00	40,00	20,00	40,00	40,00		
Input current	Iin	A	0,25	0,13	1,50	0,75	1,50		$\frac{Vout \cdot Iout}{Vin}$
Duty cycle	D		0,37	0,22	0,78	0,63	0,78		$\frac{Vout}{Vin \cdot n + Vout}$
FET Q1	max(VQ1)	V	31,55	51,55	89,28	109,28	109,28	38,48	$\frac{Vin}{1-D}$
	RMS(IQ1)	A	0,41	0,26	1,70	0,94	1,70		$\frac{\sqrt{D} \cdot n \cdot Iout}{1-D}$
Diode D1	max(VD1)	V	13,66	22,32	38,66	47,32	47,32	11,11	$\frac{Vout}{D}$
	RMS(ID1)	A	1,26	1,14	2,11	1,65	2,11		$\frac{Iout}{\sqrt{1-D}}$
Inductor L1	<|VL1|>	V	14,64	17,92	31,04	50,72	50,72	6,43	$\frac{2(1-D) \cdot Vout}{n}$
	RMS(IL1)	A	0,25	0,13	1,50	0,75	1,50		Iin
Primary	<|Vprim|>	V	14,64	17,92	31,04	50,72	50,72	12,76	$\frac{2(1-D) \cdot Vout}{n}$
Winding	RMS(Iprim)	A	1,26	1,14	2,11	1,65	2,11		$n \cdot Iout \cdot \sqrt{\frac{D}{1-D}}$
Secondary	<|Vsec|>	V	6,34	7,76	13,44	21,96	21,96	2,39	$2(1-D) \cdot Vout$
Winding	RMS(Isec)	A	1,26	1,14	2,11	1,65	2,11		$\frac{Iout}{\sqrt{1-D}}$
Capacitor	max(Vcin)	V	20,00	40,00	20,00	40,00	40,00	0,00	Vin
Cin	RMS(Icin)	A	0,00	0,00	0,00	0,00	0,00		0
Capacitor	max(Vcout)	V	5,00	5,00	30,00	30,00	30,00	3,46	$Vout$
Cout	RMS(Icout)	A	0,76	0,54	1,86	1,32	1,86		$Iout \cdot \sqrt{\frac{D}{1-D}}$
Capacitor	max(VC1)	V	20,00	40,00	20,00	40,00	40,00	1,15	Vin
C1	RMS(IC1)	A	0,33	0,23	0,81	0,57	0,81		$n \cdot Iout \cdot \sqrt{\frac{D}{1-D}}$

The total component stress factor is the sum of the individual CSF:
Semiconductor component stress factor (SCSF) is 49.58
Winding component stress factor (WCSF) is 21.58
Capacitative component stress factor (CCSF) is 4.62

2.3.5 Advantages

Buck-boost type converter. The input can be both higher and lower than the output.

The output is non-inverting.

Few active components.

The FET is lowside making it easier to control.

2.3.6 Disadvantages

All energy is transfered through a series capacitor which in turn must be able to handle the current.

Ringing is likely.

Rather high winding stresses.

Pulsating output current.

2.4 Ćuk Converter - (CL)

The chapter is dedicated to the analysis of using an isolated Ćuk converter for a lab power supply with specifications as described in the introduction. For the sake of simplicity, it is assumed that all capacitors and inductors are of infinite size, and all other components are considered ideal.

2.4.1 Schematic & Operation

The Ćuk converter is shown in its isolated form in Fig. 2.11, where labels and directions of voltages and currents used throughout the analysis are defined.

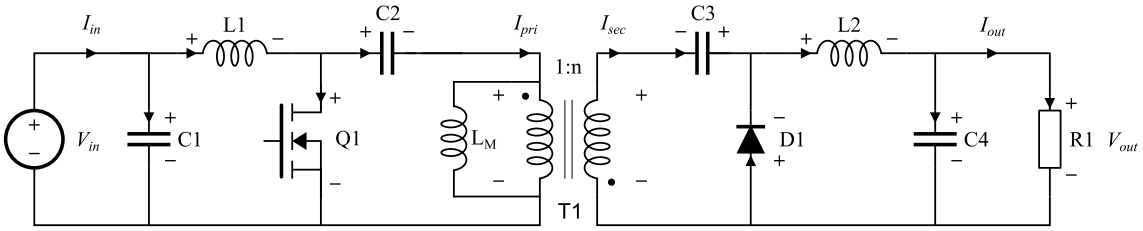


Figure 2.11: Isolated Ćuk converter with definitions of voltages and currents.

When the MOSFET is on (conducting), the circuit operates as shown in Fig. 2.12, where the diode is reverse biased and hence not conducting. In Fig. 2.13 the circuit operation with the MOSFET off is illustrated, in which case the diode is conducting.

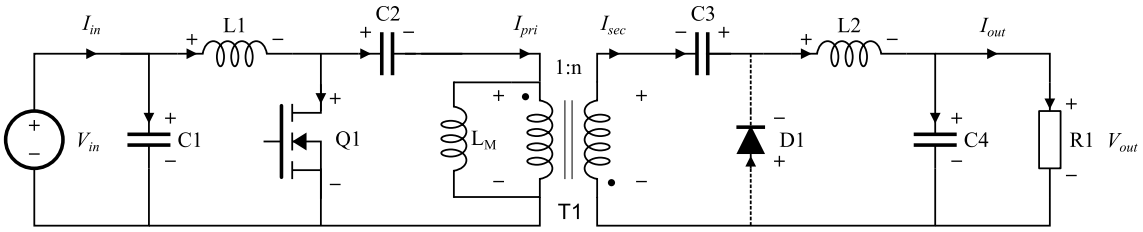


Figure 2.12: Isolated Ćuk converter with MOSFET on.

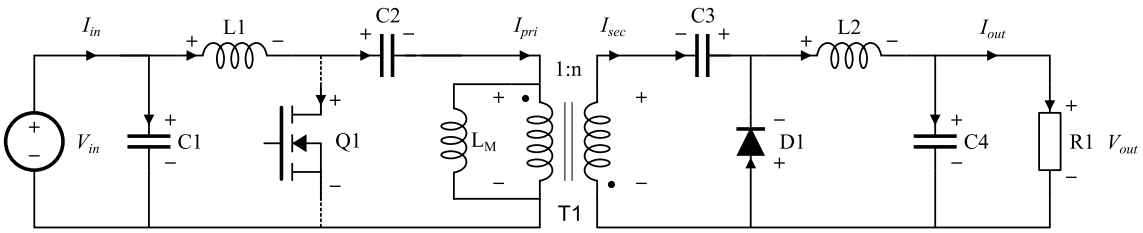


Figure 2.13: Isolated Ćuk converter with MOSFET off.

Since it is assumed that the inductors are infinitely large, the current through both L1 and L2 will be constant, and hence the capacitors C1 and C4 will never be charged or discharged during steady state operation. These capacitors will therefore be neglected for the rest of the analysis.

2.4.2 Voltage & Current Plots

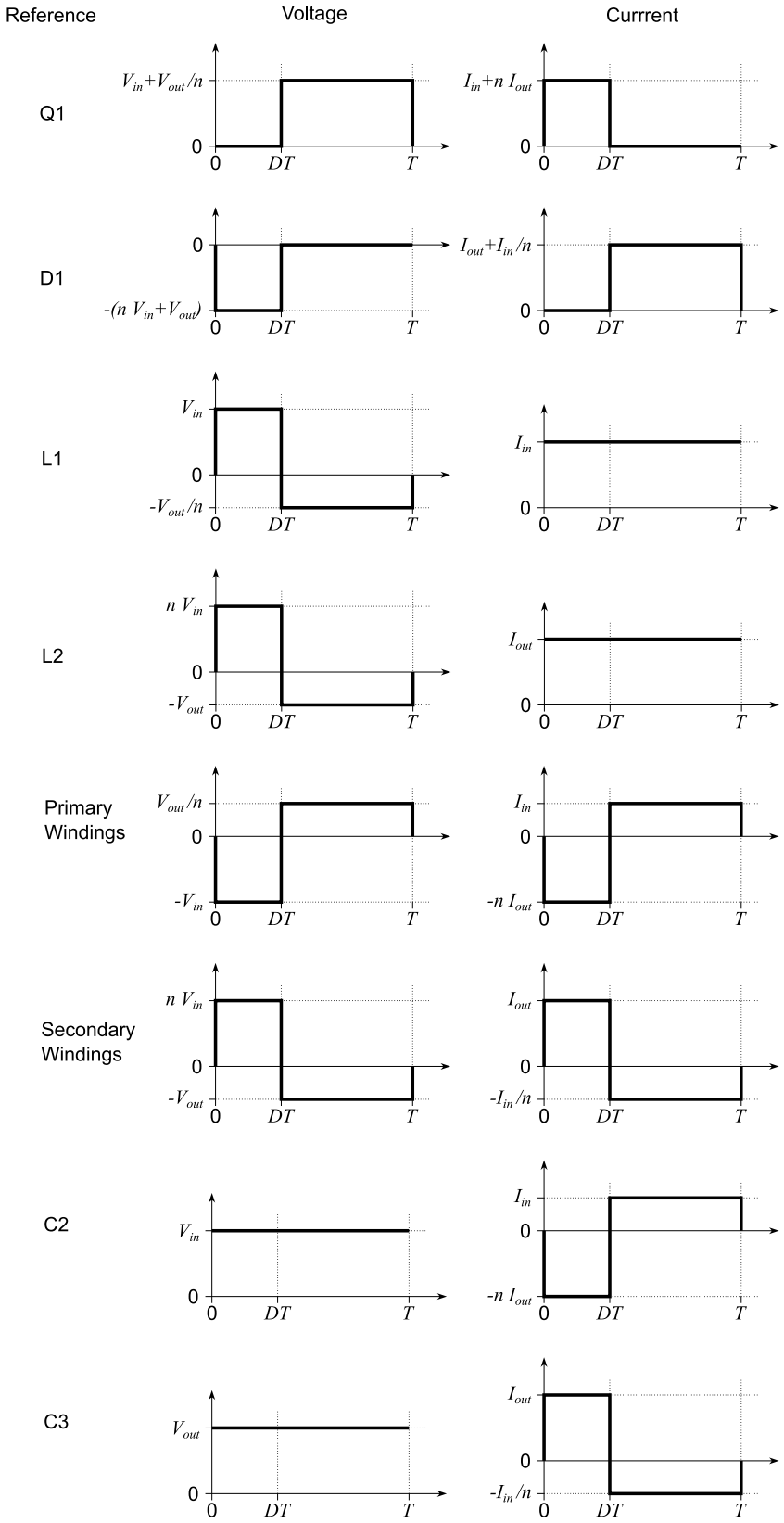


Figure 2.14: Voltages and currents of the components in the Ćuk converter.

2.4.3 Derivation of Equations

Definitions

RMS Current

$$RMS(i(t)) = \sqrt{\frac{1}{T}\int_0^T i(t)^2 dt} \tag{2.66}$$

Average Absolute Voltage

$$< |v(t)| >_T = \frac{1}{T}\int_0^T |v(t)| dt \tag{2.67}$$

As the converter is assumed to have ideal components and 100% efficiency the power in must equal the power out. The input current is then:

$$I_{in} = \frac{V_{out} I_{out}}{V_{in}} \tag{2.68}$$

Conversion Ratio

The principle of volt-second balance is applied to the inductor L_2, see waveform in Fig. 2.14.

$$\begin{gathered} nV_{in}DT - V_{out}(-DT + T) = 0 \\ \Updownarrow \\ M(n, D) = \frac{V_{out}}{V_{in}} = \frac{n\,D}{1 - D} \end{gathered} \tag{2.69}$$

Reapplying the principle of conservation of power in an ideal converter, yields the following relation between input and output current, which will be used repeatedly to determine RMS currents expressed as functions of only I_{out}, n and D.

$$I_{in} = \frac{V_{out}}{V_{in}} I_{out} = \frac{n\,D}{1 - D} I_{out} \tag{2.70}$$

RMS Currents

The following calculations of RMS currents are based on the waveforms shown in Fig. 2.14.

Inductor L1

$$\sqrt{\frac{1}{T}\int_0^T i_{L1}(t)^2 dt} = I_{in} = \frac{n\,D}{1 - D} I_{out} \tag{2.71}$$

Inductor L2

$$\sqrt{\frac{1}{T}\int_0^T i_{L2}(t)^2 dt} = I_{out} \tag{2.72}$$

Primary Winding

$$\sqrt{\frac{1}{T}\int_0^T i_{Lpri}(t)^2 dt} = \sqrt{\frac{1}{T}\left(\int_0^{DT} (-nI_{out})^2 dt + \int_{DT}^T I_{in}^2 dt\right)} = nI_{out}\sqrt{\frac{D}{1 - D}} \tag{2.73}$$

Secondary Winding

$$\sqrt{\frac{1}{T}\int_0^T i_{Lsec}(t)^2 dt} = \sqrt{\frac{1}{T}\left(\int_0^{DT} I_{out}^2 dt + \int_{DT}^T \left[\frac{-I_{in}}{n}\right]^2 dt\right)} = I_{out}\sqrt{\frac{D}{1-D}} \tag{2.74}$$

Switch Q1

$$\sqrt{\frac{1}{T}\int_0^T i_{Q1}(t)^2 dt} = \sqrt{\frac{1}{T}\left(\int_0^{DT} (I_{in} + nI_{out})^2 dt + \int_{DT}^T 0^2 dt\right)} = nI_{out}\frac{\sqrt{D}}{1-D} \tag{2.75}$$

Diode D1

$$\sqrt{\frac{1}{T}\int_0^T i_{D1}(t)^2 dt} = \sqrt{\frac{1}{T}\left(\int_0^{DT} 0^2 dt + \int_{DT}^T \left[I_{out} + \frac{I_{in}}{n}\right]^2 dt\right)} = \frac{I_{out}}{\sqrt{1-D}} \tag{2.76}$$

Capacitor C2

$$\sqrt{\frac{1}{T}\int_0^T i_{C2}(t)^2 dt} = \sqrt{\frac{1}{T}\left(\int_0^{DT} (-nI_{out})^2 dt + \int_{DT}^T I_{in}^2 dt\right)} = nI_{out}\sqrt{\frac{D}{1-D}} \tag{2.77}$$

Capacitor C3

$$\sqrt{\frac{1}{T}\int_0^T i_{C3}(t)^2 dt} = \sqrt{\frac{1}{T}\left(\int_0^{DT} I_{out}^2 dt + \int_{DT}^T \left[\frac{-I_{in}}{n}\right]^2 dt\right)} = I_{out}\sqrt{\frac{D}{1-D}} \tag{2.78}$$

2.4.4 Summary of Formulas

The four most extreme combinations of input and output voltages are considered here.

	Symbol	Unit	Case 1	Case 2	Case 3	Case 4	Max	Expression
Turns ratio	n	-	0.433	0.433	0.433	0.433	0.433	
Output voltage	V_{out}	V	5.00	30.00	5.00	30.00	30.00	
Output current	I_{out}	A	1.00	1.00	1.00	1.00	1.00	
Input voltage	V_{in}	V	20.00	20.00	40.00	40.00	40.00	
Input current	I_{in}	A	0.25	1.50	0.13	0.75	1.50	$\frac{V_{out}I_{out}}{V_{in}}$
Duty-cycle	D	-	0.37	0.78	0.22	0.63	0.78	$\frac{V_{out}}{nV_{in}+V_{out}}$
L1	$<\lvert V_{L1}\rvert>$	V	14.64	31.04	17.92	50.72	50.72	$DV_{in}+\frac{V_{out}(1-D)}{n}$
	RMS(I_{L1})	A	0.25	1.5	0.13	0.75	1.50	$\frac{nD}{1-D}I_{out}$
L2	$<\lvert V_{L2}\rvert>$	V	6.34	13.44	7.76	21.96	21.96	$nDV_{in}+V_{out}(1-D)$
	RMS(I_{L2})	A	1	1	1	1	1	I_{out}
L_{pri}	$<\lvert V_{Lpri}\rvert>$	V	14.64	31.04	17.92	50.72	50.72	$DV_{in}+\frac{V_{out}(1-D)}{n}$
	RMS(I_{Lpri})	A	0.33	0.81	0.23	0.57	0.81	$nI_{out}\sqrt{\frac{D}{(1-D)}}$
L_{sec}	$<\lvert V_{Lsec}\rvert>$	V	6.34	13.44	7.76	21.96	21.96	$nDV_{in}+V_{out}(1-D)$
	RMS(I_{Lsec})	A	0.76	1.86	0.54	1.32	1.86	$I_{out}\sqrt{\frac{D}{1-D}}$
Q1	max(V_{Q1})	V	31.55	89.28	51.55	109.28	109.28	$V_{in}+\frac{v_{out}}{n}$
	RMS(I_{Q1})	A	0.41	1.7	0.26	0.94	1.7	$nI_{out}\frac{\sqrt{D}}{1-D}$
D1	max($-V_{D1}$)	V	13.66	38.66	22.32	47.32	47.32	$nV_{in}+V_{out}$
	RMS(I_{D1})	A	1.26	2.11	1.14	1.65	2.11	$\frac{I_{out}}{\sqrt{1-D}}$
C2	max(V_{C2})	V	20	20	40	40	40	V_{in}
	RMS(I_{C2})	A	0.33	0.81	0.23	0.57	0.81	$nI_{out}\sqrt{\frac{D}{1-D}}$
C3	max(V_{C3})	V	5.00	30.00	5.00	30.00	30.00	V_{out}
	RMS(I_{C3})	A	0.76	1.86	0.54	1.32	1.86	$I_{out}\sqrt{\frac{D}{1-D}}$

Table 2.3: Maximum, RMS and average absolute values for the converter components.

2.4.5 Component Stress Factor

The component stress factors are calculated from the results summarized in Table 2.3, while ignoring the weighting between components by setting the weighting fraction to unity in each term. The power used in these calculations is the highest output power, which is 30 W.

Winding Stress Factor

$$WCSF_{L1} = \frac{< |(v_{L1}| >^2 \cdot RMS(I_{L1})^2}{P^2} = 6.43 \tag{2.79}$$

$$WCSF_{L2} = \frac{< |(v_{L2}| >^2 \cdot RMS(I_{L2})^2}{P^2} = 0.54 \tag{2.80}$$

$$WCSF_{Lpri} = \frac{< |(v_{Lpri}| >^2 \cdot RMS(I_{Lpri})^2}{P^2} = 1.88 \tag{2.81}$$

$$WCSF_{Lsec} = \frac{< |(v_{Lsec}| >^2 \cdot RMS(I_{Lsec})^2}{P^2} = 1.85 \tag{2.82}$$

$$WCSF_{total} = 10.7 \tag{2.83}$$

Semiconductor Stress Factor

$$SCSF_{Q1} = \frac{max(v_{Q1})^2 \cdot RMS(I_{Q1})^2}{P^2} = 38.3 \tag{2.84}$$

$$SCSF_{D1} = \frac{max(v_{D1})^2 \cdot RMS(I_{D1})^2}{P^2} = 11.1 \tag{2.85}$$

$$SCSF_{total} = 49.4 \tag{2.86}$$

Capacitor Stress Factor

$$CCSF_{C2} = \frac{(v_{C2_{peak}})^2 \cdot RMS(I_{C2})^2}{P^2} = 1.2 \tag{2.87}$$

$$CCSF_{C3} = \frac{(v_{C3_{peak}})^2 \cdot RMS(I_{C3})^2}{P^2} = 3.5 \tag{2.88}$$

$$CCSF_{total} = 4.7 \tag{2.89}$$

2.4.6 Advantages & Disadvantages

Some advantages and disadvantages of the Ćuk converter are:

Advantages

- Single low-side switch
- Inductors in series with input and output gives small current ripple, e.g. good for batteries

Disadvantages

- High switch blocking voltage
- Multiple LC-networks to cause resonance
- Both input and output current is transferred through capacitors, which means that they must be capable of handling quite a lot of current

2.5 Push-Pull Converter (TK)

The push-pull converter is a buck type isolated converter unlike the other topologies discussed here.

2.5.1 Schematic & Operation

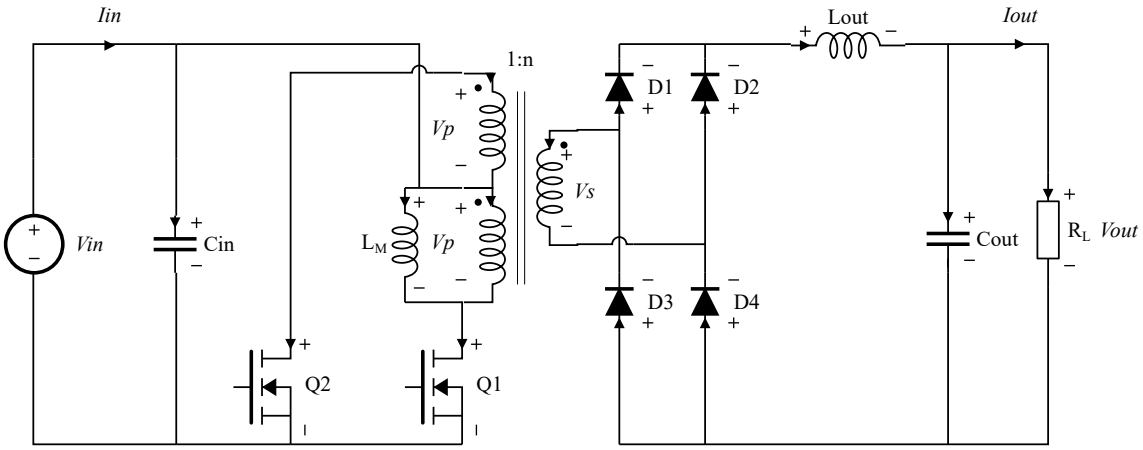


Figure 2.15: Push-Pull converter with voltage and current definitions

The push-pull converter have two switches. The operation can be divided into four intervals. One where $Q1$ is closed, two where both are open and one where $Q2$ is closed. No current ever runs through the output capacitor because of the assumed constant inductor current.

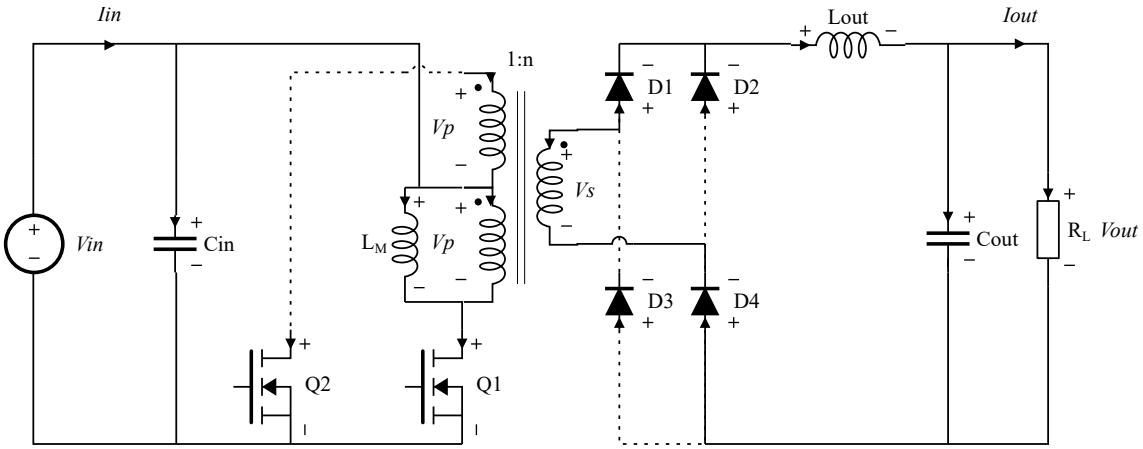


Figure 2.16: First interval. $Q1$ is closed

When Q_1 is closed, the voltage V_p over the primary winding is V_{in}. This voltage is transformed to the secondary side, $V_s = nV_{in}$. This voltage forward biases $D1$ and $D4$ which makes it possible for a current to run ($D2$ and $D3$ are reverse biased). A current now runs from the voltage source and input capacitor and into the lower primary winding. The primary side current is transformed to the secondary winding with a factor $\frac{1}{n}$. This current runs through $D1$, $D4$, the output inductor and through the load.

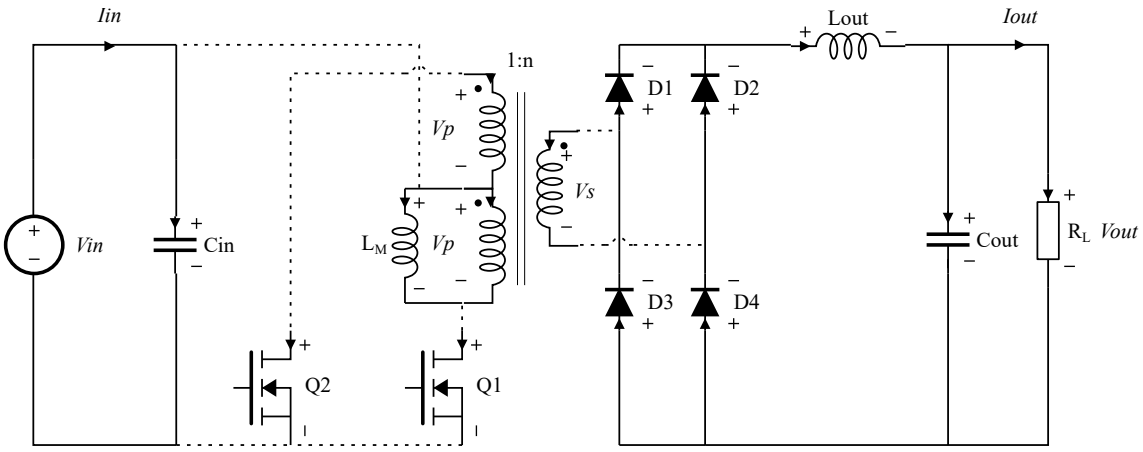


Figure 2.17: Second and fourth interval. Both switches are open.

Both switches are open in the second interval. The output inductor causes a freewheeling current to go through all diodes and to the output. No currents are running through the transformer windings.

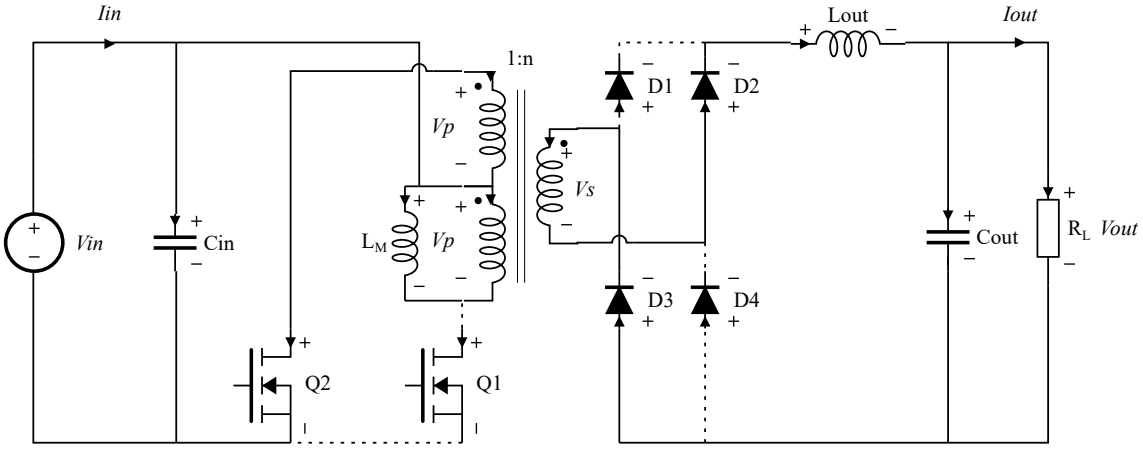


Figure 2.18: Third interval. $Q2$ is closed.

In the third interval the second switch is closed. The primary winding voltage V_p is $-V_{in}$. The volt-second balance for the transformer is achieved by keeping both switches closed an equal amount of time. Interval 3 and 4 are quite similar to 1 and 2 except for the opposite transformer voltages.

2.5.2 Voltage & Current Plots

$Q1$ is closed in the interval $[0, DT]$ and $Q2$ is closed in the interval $[T, T + DT]$.

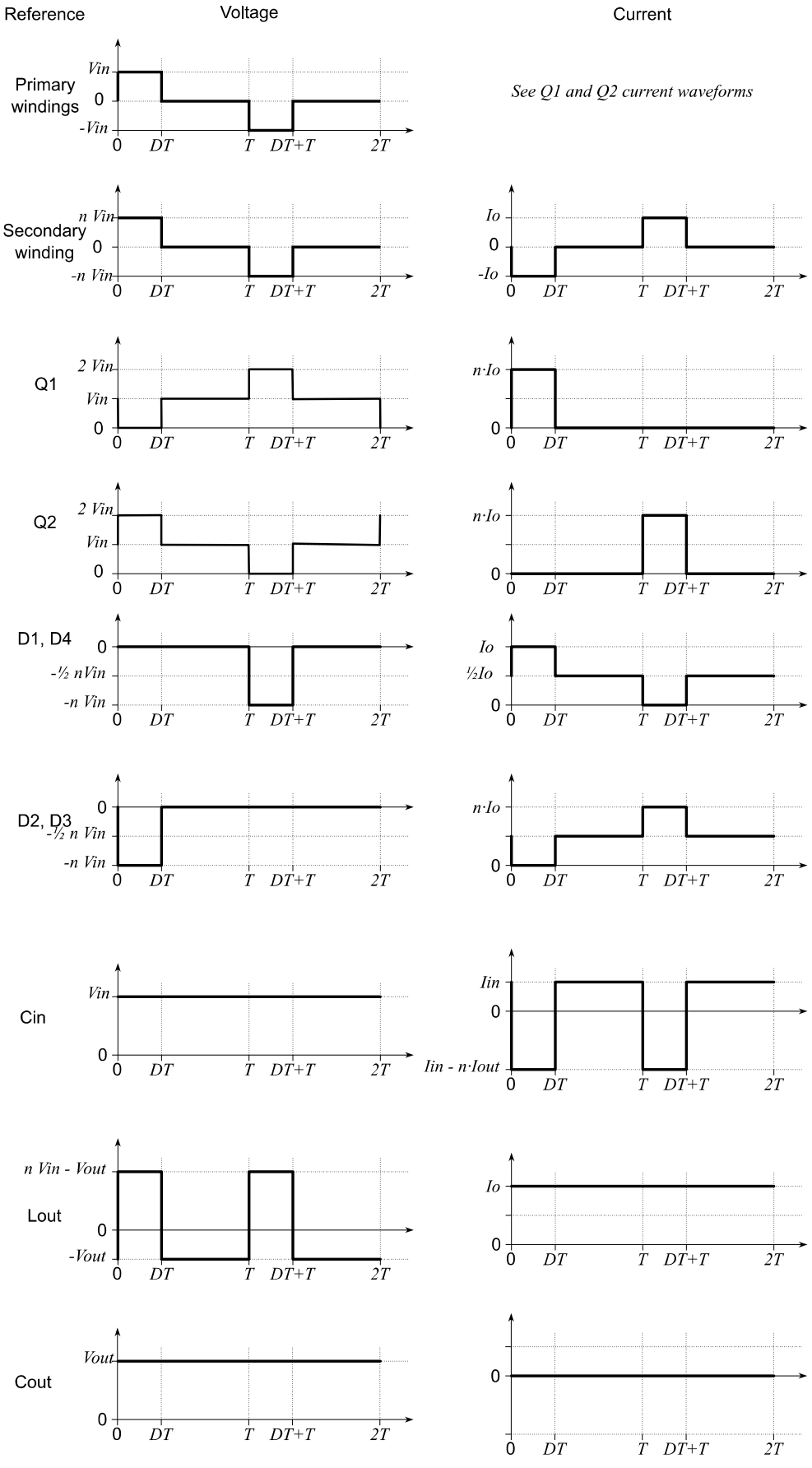


Figure 2.19: Current and voltage waveforms

2.5.3 Derivations of Equations

RMS Current Definition

$$RMS(i(t)) = \sqrt{\frac{1}{T}\int_0^T i(t)^2 dt} \tag{2.90}$$

Average Absolute Voltage Definition

$$< |v(t)| >_T = \frac{1}{T}\int_0^T |v(t)| dt \tag{2.91}$$

Input current

As the converter is assumed to have ideal components and 100% efficiency the power in must equal the power out. The input current is then:

$$I_{in} = \frac{V_{out} I_{out}}{V_{in}} \tag{2.92}$$

Conversion ratio M(D)

The principle of volt-second balance is applied to the output inductor. When one of the switches are closed its voltage is $nV_{in} - V_{out}$. When all switches are open its voltage is $-V_{out}$.

$$D(nV_{in} - V_{out}) = (1 - D)(-V_{out}) \tag{2.93}$$

$$\Longleftrightarrow$$

$$M(D) = \frac{V_{out}}{V_{in}} = nD \tag{2.94}$$

Primary Winding Average Absolute Voltages

This is the same for the upper and lower primary windings.

$$< |V_p| >_T = \frac{1}{T}\int_0^{DT} V_{in} dt = DV_{in} \tag{2.95}$$

RMS Current of Switches and Primary Windings

The current through the lower primary winding equals the current through Q1. The same is valid for the upper primary winding and Q2, except for the sign change. Furthermore, since both switches are closed an equal amount of time, their RMS currents will be the same.

$$RMS(I_{Q2}) = RMS(I_{Q1}) = \sqrt{\frac{1}{2T}\int_0^{DT} (nI_{out})^2 dt} = \sqrt{\frac{D}{2}} nI_{out} \tag{2.96}$$

Secondary Winding Average Absolute Voltage

$$< |V_s| >_T = nDV_{in} \tag{2.97}$$

Secondary Winding RMS Current

$$RMS(I_s) = \sqrt{\frac{1}{T}\int_0^{DT} (I_{out})^2 dt} = \sqrt{D} I_{out} \tag{2.98}$$

RMS Currents of Diodes

The notation Dx is used as the RMS currents are identical for all four diodes.

$$RMS(I_{Dx}) = \sqrt{\frac{1}{2T}(\int_0^{DT} I_{out}^2 dt + 2\int_{DT}^{T}(\frac{I_{out}}{2})^2 dt)} = \sqrt{\frac{D}{2}I_{out}^2 + (1-D)(\frac{I_{out}}{2})^2}$$
$$\Longleftrightarrow$$
$$RMS(I_{Dx}) = \frac{I_{out}}{2}\sqrt{D+1} \tag{2.99}$$

Input Capacitor RMS Current

The expression for I_{out} in (2.92) is used here.

$$RMS(I_{C_in}) = \sqrt{\frac{1}{T}\int_0^{DT}(I_{in} - nI_{out})^2 dt + \int_{DT}^{T} I_{in}^2 dt}$$
$$\Longleftrightarrow$$
$$RMS(I_{C_in}) = I_{out}\sqrt{Dn^2 - \frac{2DV_{out}n}{V_{in}} + \frac{V_{out}^2}{V_{in}^2}} \tag{2.100}$$
$$\Longleftrightarrow$$
$$RMS(I_{C_in}) = I_{out}\sqrt{\frac{V_{out}\cdot n}{V_{in}} - \frac{V_{out}^2}{V_{in}^2}} \tag{2.101}$$

Output Inductor Average Absolute Voltage

$$< |V_{L_{out}}| >_T = \frac{1}{T}(\int_0^{DT} |nV_{in} - V_{out}| dt + \int_{DT}^{T} |-V_{out}| dt)$$
$$\Longleftrightarrow$$
$$< |V_{L_{out}}| >_T = D\cdot(nV_{in} - V_{out}) + (1-D)\cdot V_{out}$$
$$\Longleftrightarrow$$
$$< |V_{L_{out}}| >_T = (nV_{in} - 2V_{out})D + V_{out} \tag{2.102}$$
$$\Longleftrightarrow$$
$$< |V_{L_{out}}| >_T = -2\frac{V_{out}^2}{n\cdot V_{in}} \tag{2.103}$$

Output Capacitor RMS Current

The current through the output capacitor is zero because the output current and output inductor current are constant.

2.5.4 Summary of Formulas

The four most extreme combinations of input and output voltages are considered here.

	Symbol	Unit	Case 1	Case 2	Case 3	Case 4	Maximum	Expression
Turns ratio	n	-	1.63	1.63	1.63	1.63	1.63	-
Output voltage	V_{out}	V	5.00	30.00	5.00	30.00	30.00	-
Output current	I_{out}	A	1.00	1.00	1.00	1.00	1.00	-
Input voltage	V_{in}	V	20.00	20.00	40.00	40.00	40.00	-
Input current	I_{in}	A	0.25	1.50	0.13	0.75	1.50	$\frac{V_{out}I_{out}}{V_{in}}$
Duty-cycle	D	-	0.15	0.92	0.08	0.46	0.92	$\frac{V_{out}}{nV_{in}}$
Primary windings	$<\|Vp\|>$	V	3.08	18.46	3.08	18.46	18.46	DV_{in}
Upper primary winding	RMS(I_pu)	A	0.45	1.10	0.32	0.78	1.10	$\sqrt{\frac{D}{2}}nI_{out}$
Lower primary winding	RMS(I_pl)	A	0.45	1.10	0.32	0.78	1.10	$\sqrt{\frac{D}{2}}nI_{out}$
Secondary winding	$<\|Vs\|>$	V	5.00	30.00	5.00	30.00	30.00	nDV_{in}
	RMS(I_s)	A	0.39	0.96	0.28	0.68	0.96	$\sqrt{D}I_{out}$
Switches Qx	max($-V_{Qx}$)	V	40.00	40.00	80.00	80.00	80.00	$2V_{in}$
	RMS(I_{Qs})	A	0.45	1.10	0.32	0.78	1.10	$\sqrt{\frac{D}{2}}nI_{out}$
Diodes Dx	max(V_{Dx})	V	32.50	32.50	65.00	65.00	65.00	nV_{in}
	RMS(I_{Dx})	A	0.54	0.69	0.52	0.60	0.69	$\frac{1}{2}I_{out}\sqrt{D+1}$
Input capacitor	max(V_{Cin})	V	20.00	20.00	40.00	40.00	40.00	V_{in}
	RMS(I_{Cin})	A	0.59	0.43	0.43	0.81	0.81	$I_{out}\sqrt{\frac{V_{out}\cdot n}{V_{in}}-\frac{V_{out}^2}{V_{in}^2}}$
Output inductor	$<\|V_{Lout}\|>$	V	8.46	4.62	9.23	32.31	32.31	$-2\frac{V_{out}^2}{n\cdot V_{in}}$
	RMS(I_{Lout})	A	1.00	1.00	1.00	1.00	1.00	I_{out}
Output capacitor	max(V_{cout})	V	5.00	30.00	5.00	30.00	30.00	V_{out}
	RMS(I_{Cout})	A	0.00	0.00	0.00	0.00	0.00	0

Table 2.4: Maximum, RMS and average absolute values for the converter components

2.5.5 Component Stress Factor

The weigth factor $\frac{\sum_j W_j}{W_i}$ is set to 1 for all calculations. P is the maximum total power processed $P = max(I_{out}) \cdot max(V_{out})$. The total stress factors are the sums of the individual stress factor in each category.

Semiconductor Stress Factor

The two switches experience the same stress. The same holds for the four diodes.

$$SCSF_{Qx} = \frac{max(v_{Qx})^2 \cdot RMS(I_{Qx})^2}{P^2} = 8.67 \tag{2.104}$$

$$SCSF_{Dx} = \frac{max(v_{Dx})^2 \cdot RMS(I_{Dx})^2}{P^2} = 2.26 \tag{2.105}$$

$$SCSF_{total} = 26.36 \tag{2.106}$$

Winding Stress Factor

There are here four parts. The three windings on the transformer and the inductor.

$$WCSF_p = 2\frac{< |v_p| >^2 \cdot RMS(I_p)^2}{P^2} = 0.92 \tag{2.107}$$

$$WCSF_s = \frac{< |v_s| >^2 \cdot RMS(I_s)^2}{P^2} = 0.92 \tag{2.108}$$

$$WCSF_{Lout} = \frac{< |v_{Lout}| >^2 \cdot RMS(I_{Lout})^2}{P^2} = 1.16 \tag{2.109}$$

$$WCSF_{total} = 3.01 \tag{2.110}$$

Capacitor Stress Factor

Input and output capacitors.

$$CCSF_Cin = \frac{(v_{Cin_{peak}})^2 \cdot RMS(I_{Cin})^2}{P^2} = 1.17 \tag{2.111}$$

$$CCSF_Cout = \frac{(v_{Cout_{peak}})^2 \cdot RMS(I_{Cout})^2}{P^2} = 0.00 \tag{2.112}$$

$$CCSF_{total} = 1.17 \tag{2.113}$$

2.5.6 Advantages

- Can utilize entire BH-loop
- Can operate at duty cycles close to unity
- Linear conversion ratio M(D)
- Switches are referenced to ground

2.5.7 Disadvantages

- Large transformer due to two set of windings on primary side
- Diodes on secondary side gives losses due to forward voltage drop
- Advanced control is needed to avoid transformer saturation
- Wide duty cycle range for this set of specifications
- Two switches
- High voltages over switches

The issue of forward voltage drop can be reduced by having two secondary windings and only two diodes, not four. But this would result in a larger transformer.

2.6 Summary & Selection (TK, BW, CL & SK)

2.6.1 Influence of Semiconductor Forward Voltage

The forward voltage drop of the diodes results in lowered output voltages for all converters except the Ćuk. This causes the duty cycle to be increased when feedback is applied. Because of this it might be necessary to design the converters with a higher turns ratio n. A conduction voltage in the switches (caused by on-resistance) will have the same effect. Additionally, these effects cause conduction losses of $P_D = V_f \cdot I_D$ per diode and $P_{SW} = I_{SW}^2 R_{DSON}$ per switch in the case of a constant current.

2.6.2 Topology Comparison

	Flyback	Sepic	Ćuk	Push-pull
SCSF	49.87	49.58	49.4	26.36
WCSF	10.7	21.58	10.7	3.01
CCSF	4.64	4.62	4.7	1.17
Sum CSF	65.21	75.78	64.8	30.54
Duty Cycle Range	22% - 78%	22% - 78%	22% - 78%	7.7% - 92%

Table 2.5: Numerical comparison

From table 2.5 it is seen that the push-pull converter have the drawback of a duty cycle range close to 0 and 100%. This might be hard to realize in practice as the duty cycle depends on load etc. This wide range is caused by the fact that the push-pull is a buck-type converter, and this application is a typical buck-boost application. The push-pull was analyzed anyways, since a correct choice of turns ratio can make a buck-type topology work. Another drawback of the push-pull is that it has one more switch than the other topologies. The reason for the low stress factor is probably that it utilizes the available duty cycle range greatly. This causes many of the RMS currents to become small.

Compared with SEPIC converter, flyback converter has lower component stress factors, and on the other hand, the number of the components in this type of converter is less than Ćuk converter and SEPIC converter. Its main disadvantage is ringing issues.

The SEPIC and Ćuk converters are complex with many components compared to the flyback. The calculations also suggests that their component stress is higher, which suggest a low efficiency. One might argue that the simplified use of CSF, with weighting factor 1, gives topologies with many components an unreasonably bad figure.

One advantage for the SEPIC and Ćuk converters are that they have a capacitor in series with the transformer which removes any DC voltage offset on the windings. This makes it easier to avoid transformer core saturation.

The SEPIC and Ćuk topologies are now disregarded as efficiency is the number one priority in this course. This leaves the flyback and push-pull. And since the push-pull converter has a wide duty cycle range, the flyback is considered the best choice.

3 | Magnetic Design (CL, SK, BW & TK)

In Chapter 2 the Flyback topology was chosen as the best converter for the task at hand. This chapter serves to describe the design process for the transformer, which is the only magnetic component in a Flyback converter. The Flyback transformer functions as both galvanic isolation and energy storage - it's a coupled inductor. This property complicates the design a bit, as will be obvious in the following sections. Note, as customary in discussions of Flyback converters, we will use the terms *coupled inductor* and *transformer* interchangeably throughout this work.

3.1 Non-Ideal Circuit Operation

In the previous analysis of the Flyback converter, a simplified ideal circuit operation with no ripple was assumed. For the magnetic design, however, current ripple must be taken into account as this will be a design parameter. Hence, the converter is analyzed once more, and the schematic with definitions of component labels, voltage polarities and current directions is repeated in Fig. 3.1 for the reader's convenience.

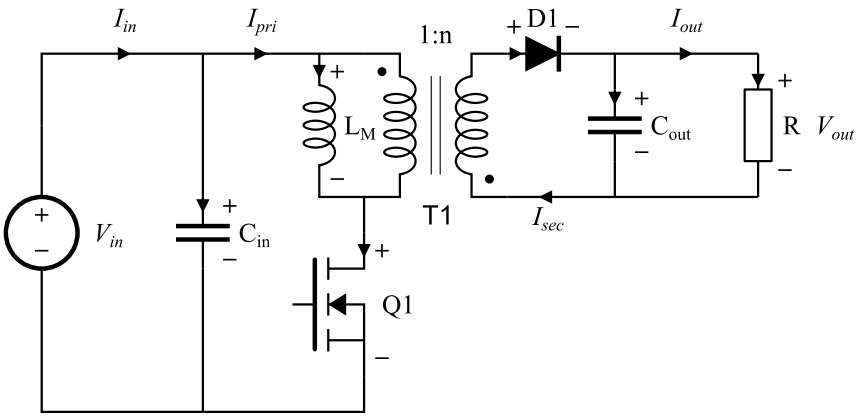


Figure 3.1: Flyback converter with definitions of labels, polarities and directions.

With these definitions the circuit operation (voltage and current waveforms) including current ripple is depicted in Fig. 3.3. From the current waveforms of the primary and secondary windings, it can be shown that the magnetic flux density in the coupled inductor behaves according to the waveform in Fig. 3.2.

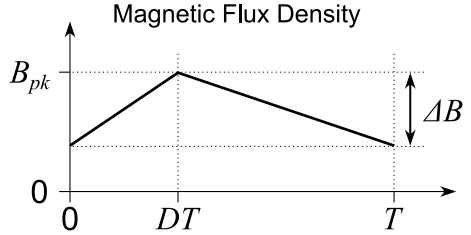


Figure 3.2: Magnetic flux density in the coupled inductor.

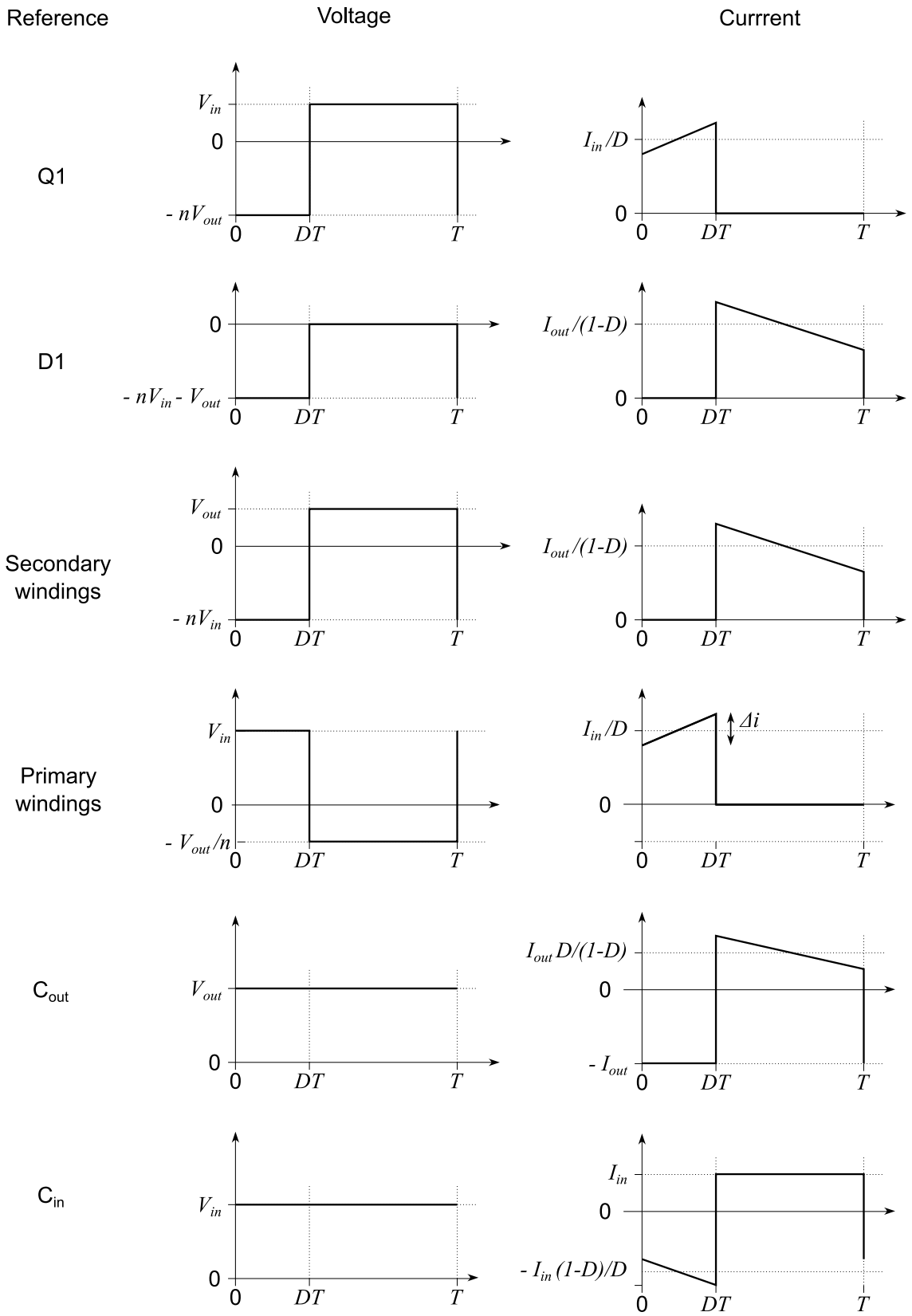


Figure 3.3: Voltage and current waveforms.

3.2 Numerical Solution for Optimal Design

Design of magnetic components has no obvious optimal design, since most configuration decisions are in practice a trade-off between lowering one cause of losses while increasing another. For instance, increasing core size usually results in room for thicker wires with lower copper loss, while also increasing the cores loss. Likewise, decreasing the number of winding layers leads to fewer losses due to the proximity effect, but also decrease the wire diameter for the same number of turns, which is a cause for increasing losses. Furthermore, the parasitic components of the transformer are highly dependent on physical construction of the device. Hence, choosing the best design (or even just an acceptable one) is a task of evaluation advantages and disadvantages for the specific use case. For this design, we will mainly focus on reducing power loss in the transformer, while keeping in mind that using a physically large core has disadvantages such as increasing production costs and product weight.

To get a good result for the transformer design, it was decided to do a numerical search for the optimal solution to these trade-offs by brute force evaluation of all possible configurations within some predetermined limiting parameters. This evaluation of all solutions was done using MATLAB scripting to handle an arbitrary (and large) amount of configurations, which depends on the chosen design limitations. Throughout the following sections, it is described, how the design theory was implemented in the script, whenever this is relevant for arguing to the validity of the calculations and thereby the comparability of the results.

3.3 Core Shape & Material

The core shape of interest was selected based on the following:

- *EPCOS* recommends the use of U or E-type core shapes for Flyback converters, [1] p. 156.
- Only E-type and RM core shapes are considered in this course.
- The RM, ER and ETD shapes have the advantage of round core centers, which gives most turns per wire length resulting in lower winding losses.

Thus the ETD core shape was selected. Furthermore, the N87 core material was selected, since this is recommended for use in flyback converters where low losses are of high priority, [1] p. 156.

The core dependent parameters l_e, A_e, V_e, μ_e and R_{th} as well as coil former window size and center diameter was extracted from the manufacturer's databook[1] into the MATLAB script for each of the considered cores. The three smallest available ETD cores (29/16/10, 34/17/11 and 39/20/13) were chosen for the analysis to keep the component cost and weight low. Experience from similar analysis of larger cores has shown that increasing cores sizes further has negligible efficiency improvements.

The ETD 29/16/10 is used to exemplify the automated calculations performed for each core. The above mentioned parameters for this core and the appropriate coil former are summarized in Table 3.1 with size definitions as in Fig. 3.4. These parameters are based on the information given in the manufacturer's databook [1].

l_e	A_e	V_e	μ_e	R_{th}	h	w	$\oslash_{cf}$
70.4 mm	76 mm^2	5350 mm^3	1610	28 °C/W	19.4 mm	5 mm	11.8 mm

Table 3.1: ETD 29/16/10 parameters for N87 material.

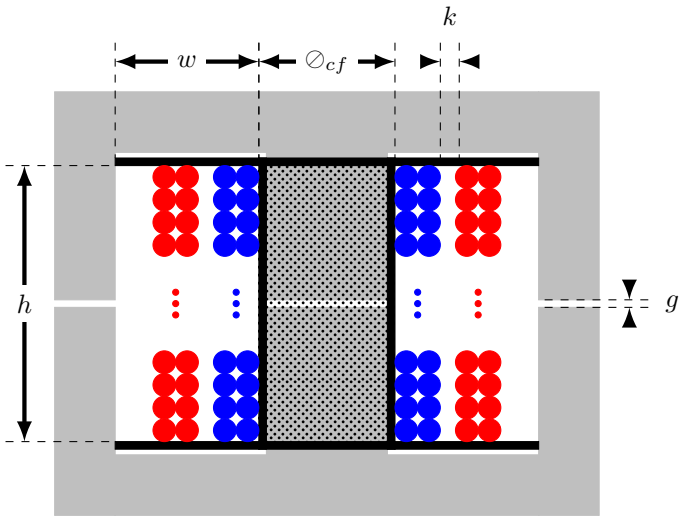


Figure 3.4: ETD-core and coil former dimension definitions.

Note that the air gap in Fig. 3.4 is identical for all core legs, which is contrary to how gapped cores are usually produced by the manufacturer. This implementation model was used to enable precise air gap sizing by stacking pieces of paper in between the two cores pieces. Hence, we could choose from a large set of gap sizes rather than the restrictive number of configurations offered by the manufacturer. Obviously, this approach is not feasibly for mass production, but it enables an easily automated and thorough first approximation of many designs.

3.4 Winding Configuration

3.4.1 Minimum Inductance

The range of possible number of primary windings have minimum and maximum bounds respectively determined by: Getting enough inductance to keep the current ripple below a certain point while still avoiding saturation of the core by keeping the flux density below an acceptable level. Based on experience from preliminary and approximating calculations, we were quite certain that adding an air gap the size of a single piece of paper (100 µm thickness) would keep the core from saturating within reasonable limits for winding configurations. Hence, we first addressed the satisfaction of minimum inductance requirement, knowing that the configuration chosen based on these findings would subsequently have to be checked against the non-saturation requirement. The design process for the former criteria is outlined in the following.

The minimum inductance needed to keep the primary winding ripple current smaller than some predefined level Δi (peak to peak) for a certain value of the input voltage, duty cycle and switching frequency is given by eq. 3.2.

$$V_L = L\,\frac{di(t)}{dt} = L\,\frac{\Delta i}{D\,T}\bigg|_{V_L = V_{in}} \tag{3.1}$$

$$\Downarrow$$

$$L \geq V_{in}\,\frac{D}{f\,\Delta i} \tag{3.2}$$

We wish to design for a ripple factor of 2. Referring to the Δi definition on the primary winding current waveforms of Fig. 3.3, this criteria leads to eq. 3.3.

$$i_{in,pk} = 2\,\Delta i \tag{3.3}$$

Furthermore, eq. 3.4 is derived from the fact that input current must be equal to the primary winding current.

$$I_{in} = \frac{1}{T}\int_0^{D\,T} i_{in}(t)\;dt + \frac{1}{T}\int_{D\,T}^{T} 0\;dt = \frac{1}{T}\int_0^{D\,T} i_{in,pk} - \Delta i + \frac{\Delta i}{D\,T}\,t\;dt \tag{3.4}$$

Substituting eq. 3.3 into eq. 3.4 show that the maximum allowable Δi to satisfy the ripple ratio criteria (or better) is dependent on the average input current and duty cycle by the relation:

$$\Delta i_{max} = \frac{2}{3}\frac{I_{in}}{D} \tag{3.5}$$

Hence, the ripple current can be determined for a given input/output scenario using the DC conversion ratio and ideal power transfer assumption, eq. 3.6 and 3.7 respectively.

$$M(D) = \frac{V_{out}}{V_{in}} = \frac{n\,D}{1-D} \Leftrightarrow D = \frac{V_{out}}{V_{in}\,n + V_{out}} \tag{3.6}$$

$$I_{in} = \frac{V_{out}\,I_{out}}{V_{in}} \tag{3.7}$$

The minimum inductance requirement in eq. 3.2 can now be plotted as a function of the input voltage (assuming maximum output power) to determine the worst case scenario, see figure 3.5.

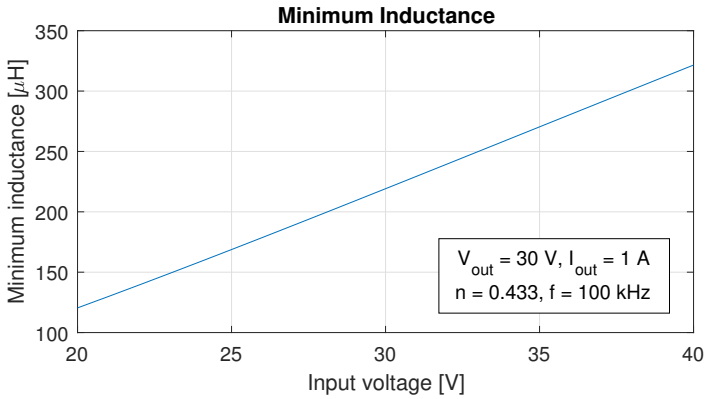


Figure 3.5: Minimum inductance to satisfy ripple current ratio.

The worst case value of the inductance is obviously for the input voltage $V_{in} = 40\,\mathrm{V}$. The minimum inductance is calculated by evaluating eq. 3.2 and eq. 3.5 through 3.7 under this condition. Note that the desired turns ratio $n = 0.433$ (see section 2.1) is assumed in this initial analysis, before the actual turns ratio is decided.

$$D_{40} = \frac{30\,\mathrm{V}}{40\,\mathrm{V} \cdot 0.433 + 30\,\mathrm{V}} = 0.63 \tag{3.8}$$

$$I_{in,40} = \frac{30\,\mathrm{V} \cdot 1\,\mathrm{A}}{40\,\mathrm{V}} = 0.75\,\mathrm{A} \tag{3.9}$$

$$\Delta i_{max} = \frac{2}{3}\frac{0.75\,\mathrm{A}}{0.63} = 0.79\,\mathrm{A} \tag{3.10}$$

$$\Downarrow$$

$$L \geq 40\,\mathrm{V}\,\frac{0.63}{100\,\mathrm{kHz} \cdot 0.79\,\mathrm{A}} = 321\,\mu\mathrm{H} \tag{3.11}$$

3.4.2 Minimum Number of Turns

Next, the goal is to figure out a minimum number of windings that will provide the required inductance. Since the minimum inductance was calculated using primary side current ripple conditions, the number of windings as calculated below must be used to determine the primary winding configuration. The inductance and number of windings are related by reluctance:

$$L = \frac{N^2}{\mathcal{R}} \tag{3.12}$$

With reluctance as defined in eq. 3.13 and taking into an added air gap, the total reluctance can be calculated by eq. 3.14. In the latter, the magnetic path cross section area of the air gap is assumed to be equal to that of the core by ignoring the fringing effect.

$$\mathcal{R} = \frac{l_e}{\mu_e\, A_e} \tag{3.13}$$

$$\mathcal{R}_{total} = \mathcal{R}_{core} + \mathcal{R}_{gap} = \frac{l_{core}}{\mu_{core}\, A_{core}} + \frac{2\,g}{\mu_{air}\, A_{core}} \tag{3.14}$$

For the ETD 29/16/10 core, the total reluctance is evaluated using $\mu_{air} = \mu_0 = 4\,\pi\,10^{-7}\,\mathrm{H/m}$:

$$\mathcal{R}_{total} = \frac{70.4\,\mathrm{mm}}{1610 \cdot 4\,\pi\,10^{-7}\,\mathrm{H/m} \cdot 76\,\mathrm{mm}^2} + \frac{2 \cdot 100\,\mu\mathrm{m}}{4\,\pi\,10^{-7}\,\mathrm{H/m} \cdot 76\,\mathrm{mm}^2} = 2.55 \cdot 10^6\,\mathrm{H}^{-1} \tag{3.15}$$

Next, this result is validated by comparing with EPCOS's similarly gapped core [1] p. 518. They have specified the relative effective permeability including air gap as $\mu_e = 281\,\mathrm{H/m}$. Solving for permeability in eq. 3.13 leads to eq. 3.16, which can be used to calculate the permeability of our gapped core.

$$\mu_{total} = \frac{l_{total}}{\mathcal{R}_{total}\, A_{core}} = \frac{l_{core} + 2\,g}{\left(\dfrac{l_{core}}{\mu_{core}\, A_{core}} + \dfrac{2\,g}{\mu_{air}\, A_{core}}\right) A_{core}} = \frac{\mu_{air}\,\mu_{core}(2\,g + l_{core})}{l_{core}\,\mu_{air} + 2\,g\,\mu_{core}} \tag{3.16}$$

For the ETD 29/16/10 with an air gap of $g = 100\,\mu\mathrm{m}$, the absolute and relative permeability is evaluated in eq. 3.17 and 3.18 respectively.

$$\mu_{total} = \frac{\left(4\,\pi\,10^{-7}\,\mathrm{H/m}\right)^2 \cdot 1610 \cdot (2 \cdot 100\,\mu\mathrm{m} + 70.4\,\mathrm{mm})}{70.4\,\mathrm{mm} \cdot 4\,\pi\,10^{-7}\,\mathrm{H/m} + 2 \cdot 100\,\mu\mathrm{m} \cdot 1610 \cdot 4\,\pi\,10^{-7}\mathrm{H/m}} = 364\,\mu\mathrm{H/m} \tag{3.17}$$

$$\mu_{r,total} = \frac{\mu_{total}}{\mu_0} = \frac{364\,\mu\text{H/m}}{4\,\pi\,10^{-7}\,\text{H/m}} = 289.7 \tag{3.18}$$

The calculated relative permeability is very close to EPCOS's value of a similar core construction, and hence it is concluded that the calculated reluctance is correct. Using eq. 3.12 as well as the results in eq. 3.11 and 3.15, the minimum number of primary windings is determined:

$$N_p \geq \sqrt{321\,\mu\text{H} \cdot 2.55 \cdot 10^6\,\text{H}^{-1}} = 28.6 \tag{3.19}$$

For the subsequent calculations used to exemplify the method, $N_p = 30$ will be used. Furthermore, the number of secondary windings $N_s = 13$ is used, which results in turns ratio $n = 0.433$.

However, the automated scripted solutions considers all possible number of primary windings from the calculated minimum up to some reasonable limiting value that is manually defined. The range of considered secondary side windings is determined by a specified turns ratio deviation from the desired value, which sets min and max secondary windings as a function of the number of primary windings. Hence, many possible configurations are considered for a large allowable turns ratio deviation, and very few are considered for a strict deviation requirement.

3.4.3 Wire Diameters & Lengths

The wire diameters of both primary and secondary side windings has significant influence on the power loss of the transformer. Hence, it is generally desirable to maximize wire diameters, but the size of the coil former window limits the design freedom somewhat as explained in the following. Refer to Fig. 3.4 and table 3.1 for dimension definitions and values for the ETD 29/16/10 core.

In general, the wire diameters are determined by the conditions:

- Each layer of the windings must almost perfectly fill the whole window height (h), i.e. no partially filled layers.
- When all layers are wound on top of each other, there should still be some room left in in the window width (w) to allow for insulation tape between primary and secondary layers (k).
- The majority of the window area should be used for secondary side windings, which has greater current than the primary side windings.

The determination of feasible wire diameter for each core with each considered N_p/N_s configuration was carried out using the following method:

1. Assume number of primary and secondary layers.
2. Calculate number of windings per layer. If they cannot be divided equally, reject the current considered configuration as unsuitable.
3. Determine the largest wire diameter incl. insulation that fits inside the window height for both primary and secondary windings. A discrete set of wire diameters is considered (Von Roll, IEC 60317-0-1, grade 1 [2] p. 5).
4. Add up the widths of all layers. If the sum is greater than $w - k$ (i.e. there is not enough room in the window width for windings and insulation tape), reject the current considered configuration as unsuitable.

For the ETD 29/16/10 core with 30 primary windings in 2 layers, 13 windings in 1 secondary layer and $k_{min} = 200\,\mu\text{m}$, the above method results in the wire diameters:

$$\oslash_{outer,p} = 1.246\,\text{mm} \;\;,\;\; \oslash_{cu,p} = 1.18\,\text{mm} \tag{3.20}$$
$$\oslash_{outer,s} = 1.468\,\text{mm} \;\;,\;\; \oslash_{cu,s} = 1.4\,\text{mm} \tag{3.21}$$

The resulting window height and width margins (not considering insulation tape) are:

$$h_{margin,p} = 710\,\mu\text{m} \tag{3.22}$$
$$h_{margin,s} = 316\,\mu\text{m} \tag{3.23}$$
$$w_{margin} = 1.04\,\text{mm} \tag{3.24}$$

The copper cross section areas of the selected wires are:

$$A_{cu,p} = 1.094\,\text{mm}^2 \tag{3.25}$$
$$A_{cu,s} = 1.539\,\text{mm}^2 \tag{3.26}$$

Finally, the winding lengths must be determined for later use in resistance calculations. The insulation tape is not taken into account for this calculation, as its thickness is assumed to have negligible influence. The length of the primary wire is given by eq. 3.27 and evaluated for the ETD 29/16/10 core in eq. 3.28.

$$l_{winding,p} = \sum_{i=1}^{n_{layers,p}} \pi \left(\oslash_{cf} + i \oslash_{outer,p}\right) \frac{N_p}{n_{layers,p}} \tag{3.27}$$

$$l_{winding,p} = \sum_{i=1}^{2} \pi \left(11.8\,\text{mm} + i \cdot 1.246\,\text{mm}\right) \frac{30}{2} = 128.8\,\text{cm} \tag{3.28}$$

Similarly, the secondary wire length is given by 3.29 and evaluated in eq. 3.30.

$$l_{winding,s} = \sum_{i=1}^{n_{layers,s}} \pi \left(\oslash_{cf} + 2\ \oslash_{outer,p}\ n_{layers,p} + i \oslash_{outer,n}\right) \frac{N_s}{n_{layers,s}} \tag{3.29}$$

$$l_{winding,s} = \sum_{i=1}^{1} \pi \left(11.8\,\text{mm} + 2 \cdot 1.246\,\text{mm} \cdot 2 + i \cdot 1.468\,\text{mm}\right) \frac{13}{1} = 74.5\,\text{cm} \tag{3.30}$$

Based on the determined winding configuration as well as wire diameter and length, the transformer's winding and core losses can be calculated as described in the following sections.

3.5 Winding Losses

AC Resistance - Dowell

Dowell's formula[3] is used to estimate the AC-resistance at the switching frequency (100kHz). Here, the presence of harmonic currents are ignored.
Dowell's formula gives an estimate based on the number of layers p and φ. φ is the ratio between foil thickness and skin depth. But as round wires are to be used, the φ must be modified[3]. The following expression is then found.

$$Dowell(\varphi, p) = \varphi \cdot \left(\frac{sinh(2\varphi) + sin(2\varphi)}{cosh(2\varphi) - cos(2\varphi)} + \frac{2(p^2-1)}{3} \frac{sinh(\varphi) - sin(\varphi)}{cosh(\varphi) + cos(\varphi)} \right) \tag{3.31}$$

$$R_{AC} = Dowell(\varphi, p) \cdot R_{DC} \tag{3.32}$$

$$\varphi = \frac{\sqrt{\eta} \cdot \sqrt{\frac{\pi}{4}} \cdot \oslash}{\delta} \tag{3.33}$$

$$\eta = \frac{\sqrt{\frac{\pi}{4}} \cdot \oslash \cdot n_{windings\,per\,layer}}{h} \tag{3.34}$$

$$R_{DC} = \frac{l_{wire} \cdot \rho}{A_{wire}} \tag{3.35}$$

Here $\oslash$ is the copper wire diameter, η is the porosity factor, *delta* is the skin depth, A_{wire} is the wire cross section area, h_{window} is the height of the magnetic window and l_{wire} is the length of the winding. This is calculated for both the primary side and the secondary side winding. The resistivity is $\rho = 1.68 \cdot 10^{-8} \Omega\,\mathrm{m}$ (copper at 20°C). The length and wire areas are given in eq. 3.25 to 3.30. The skin depth at 100kHz is 237µm.
The resistances for both windings are now found

$$R_{DC_p} = \frac{128.8\,\mathrm{cm} \cdot 1.68 \cdot 10^{-8} \Omega\,\mathrm{m}}{1.094\,\mathrm{mm}^2} = 19.8\mathrm{m}\Omega \tag{3.36}$$

$$R_{DC_s} = \frac{74.5\,\mathrm{cm} \cdot 1.68 \cdot 10^{-8} \Omega\,\mathrm{m}}{1.539\,\mathrm{mm}^2} = 8.13\mathrm{m}\Omega \tag{3.37}$$

$$\eta_p = \frac{\sqrt{\frac{\pi}{4}} \cdot 1.18\,\mathrm{mm} \cdot 2}{19.4\mathrm{mm}} = 0.809 \tag{3.38}$$

$$\eta_s = \frac{\sqrt{\frac{\pi}{4}} \cdot 1.40\,\mathrm{mm} \cdot 1}{19.4\mathrm{mm}} = 0.831 \tag{3.39}$$

$$\varphi_p = \frac{\sqrt{0.809} \cdot \sqrt{\frac{\pi}{4}} \cdot 1.18\,\mathrm{mm}}{237\mu\mathrm{m}} = 3.97 \tag{3.40}$$

$$\varphi_s = \frac{\sqrt{0.831} \cdot \sqrt{\frac{\pi}{4}} \cdot 1.40\,\mathrm{mm}}{237\mu\mathrm{m}} = 4.77 \tag{3.41}$$

$$R_{AC_p} = Dowell(3.97, 2) \cdot 19.8\mathrm{m}\Omega = 12.3 \cdot 19.8\mathrm{m}\Omega = 244\mathrm{m}\Omega \tag{3.42}$$

$$R_{AC_s} = Dowell(4.77, 1) \cdot 8.13\mathrm{m}\Omega = 4.77 \cdot 8.13\mathrm{m}\Omega = 38.8\mathrm{m}\Omega \tag{3.43}$$

RMS currents

The maximum losses are in the case of the biggest inductor currents and output power which is at 20V in and 30V out. The winding loss is the sum of the DC and AC loss for both sides. The DC current is the average current in the winding. $i_{DC_p} = i_{in} = 1.5\mathrm{A}$, and $i_{DC_s} = i_{out} = 1\mathrm{A}$.
The AC current is found by using the following relationship:

$$i_{RMS}^2 = i_{DC}^2 + i_{AC_{RMS}}^2 \tag{3.44}$$

$$\Updownarrow$$

$$i_{AC_{RMS}} = \sqrt{i_{RMS}^2 - i_{DC}^2} \tag{3.45}$$

The DC currents are known as the input current on the primary side and the output current on the secondary side. The total RMS current is found by calculating the root mean square of the

signal over a period, where it is changing with a ripple current subtracted from the peak current. The expression is simplified as the peak current where the ripple current is substracted during the on period for both sides, as this gives the same RMS as the actual waveform but is a simpler expression. The expressions for the peak current and ripple current are described in subsection 3.7.2.

$$i_{p,RMS} = \sqrt{\frac{1}{T}\int_0^{DT}\left(i_{p,pk} - \frac{\Delta i_p}{DT}\cdot t\right)dt} \tag{3.46}$$

$$i_{s,RMS} = \sqrt{\frac{1}{T}\int_0^{(1-D)T}\left(\frac{i_{p,pk}}{n} - \frac{\Delta i_p}{n(1-D)T}\cdot t\right)dt} \tag{3.47}$$

Using equation 3.46 and 3.47 in equation 3.45 with the known DC currents the AC rms currents can be calculated for the primary side:

$$i_{AC_{p,RMS}} = \frac{1}{6}\sqrt{\frac{3(D^4T^2V_{in} + 12I_{in}^2 Lm, p^2)}{L_{m,p}^2 n^2 D^2} - 36I_{in}^2} \tag{3.48}$$

$$= \frac{1}{6}\sqrt{\frac{3(0.78^4\cdot(10\mu s)^2\cdot 20V + 12(1.5A)^2\cdot(352\mu H)^2)}{(352\mu H)^2\cdot 0.78^2} - 36(1A)^2} = 0.814A \tag{3.49}$$

Similarly the $i_{AC_{RMS}}$ is calculated for the secondary side.

$$i_{AC_{s,RMS}} = \frac{1}{6}\sqrt{\frac{3(1-D)(D^4T^2V_{in} + 12I_{in}^2 Lm, p^2)}{L_{m,p}^2 n^2 D^2} - 36I_{out}^2} \tag{3.50}$$

$$= \frac{1}{6}\sqrt{\frac{3(1-0.78)(0.78^4\cdot(10\mu s)^2\cdot 20V + 12(1.5A)^2\cdot(352\mu H)^2)}{(352\mu H)^2\cdot 0.43^2\cdot 0.78^2} - 36(1A)^2} = 1.865A \tag{3.51}$$

Calculation of Winding Loss

The winding loss is then estimated by the sum of the AC and DC losses in the primary and secondary side.

$$P_{winding} = P_{DC,p} + P_{AC,p} + P_{DC,s} + P_{AC,s} \tag{3.52}$$

$$\begin{aligned} P_{winding} &= R_{DC,p}\cdot i_{DC,p}^2 + R_{AC,p}\cdot i_{RMS_{AC,p}}^2 + R_{DC,s}\cdot i_{DC,s}^2 + R_{AC,s}\cdot i_{RMS_{AC,s}}^2 \\ &= 19.8m\Omega\cdot(1.5A)^2 + 244m\Omega\cdot(0.814A)^2 + 8.13m\Omega\cdot(1A)^2 + 38.8m\Omega\cdot(1.865A)^2 \\ &= 349mW \end{aligned} \tag{3.53}$$

3.6 Core Losses

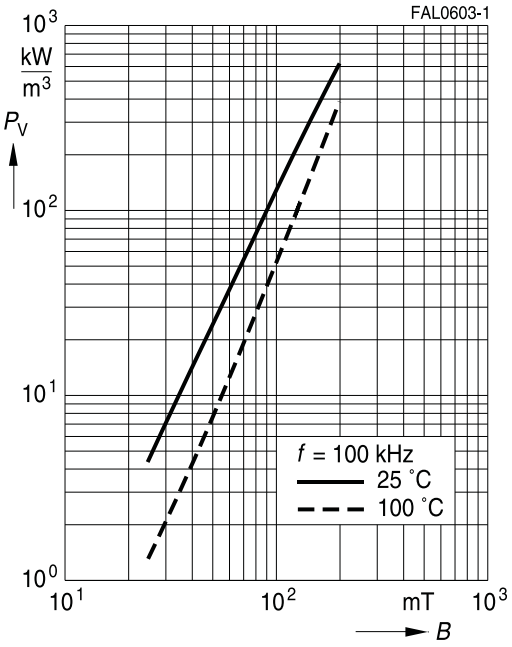


Figure 3.6: Relative core losses versus AC field flux density for N87, [1] p. 83.

The worst case scenario of 25 degrees is used and regression is performed on the solid line in Fig. 3.6. This give the following formula for core losses.

$$P_c = 34 \cdot 10^6 \, V_e \, \Delta B_{max}^{2.42} \tag{3.54}$$

Here, V_e is the effective volume of the core.

For the selected design: $\Delta i_p = \dfrac{20\text{V}}{352\mu\text{H}} \cdot 0.776 \cdot 10^{-5} s = 0.441\text{A}$ (formula explained in subsection 3.7.2). This gives:

$$\Delta B = \frac{N_p \cdot \Delta i_p \cdot \mu}{l_{total}} = \frac{30 \cdot 0.441\text{A} \cdot 290 \cdot 4\pi \cdot 10^{-7}}{70.6\text{mm}} = 68.0\text{mT} \tag{3.55}$$

$$P_c = 34 \cdot 10^6 \cdot 5350\text{mm}^3 \cdot (68.0\text{mT})^{2.42} \tag{3.56}$$

$$P_c = 272\text{mW} \tag{3.57}$$

This gives a total loss for the coupled inductor and a temperature of:

$$P_{magnetic} = P_c + P_w = 272\text{mW} + 349\text{mW} = 621\text{mW} \tag{3.58}$$

$$T_{inductor} = T_a + P_{magnetic} \cdot R_{th} = 25°\text{C} + 621\text{mW} \cdot 28°\text{C/W} \tag{3.59}$$

$$T_{inductor} = 43.4°\text{C} \tag{3.60}$$

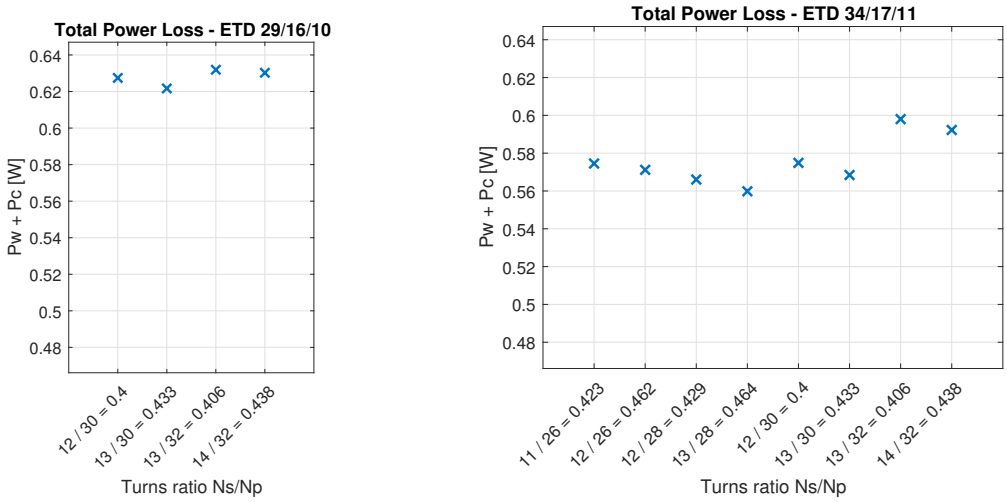
3.7 Selection of Core & Configuration

Determination of realizable winding configurations, winding losses and core losses was determined for several ETD-cores using an automated script as exemplified in the previous sections of this chapter. Table 3.2 summarizes the conditions under which the analysis was performed.

Primary layers	2
Secondary layers	1
Max primary windings	32
Air gap (each leg)	100 µm
Ideal turns ratio	0.433
Max turns ratio deviation	0.033
Primary/secondary insulation	200 µm

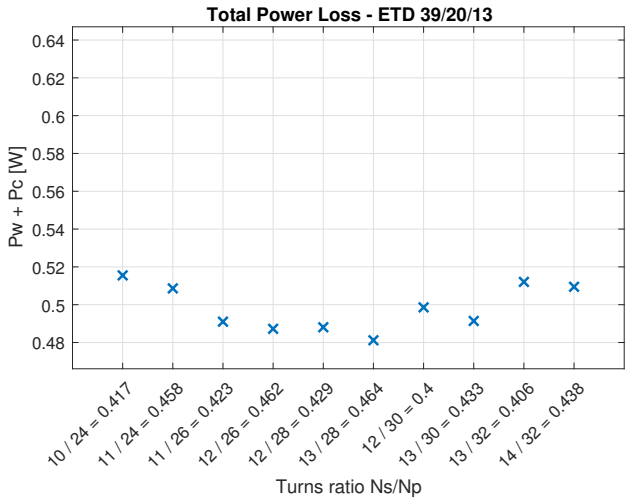
Table 3.2: Conditions for determination of transformer configuration.

The resulting total power loss for each of the considered cores is plotted for varying winding configurations in Fig. 3.7. Another analysis of the ETD-cores was performed with doubled air gap and similar calculations were performed for several E-cores (taking into account the different physical construction of these core). Plots from these other analyses can be found in Appendix A and B respectively.



(a)

(b)



(c)

Figure 3.7: Realizable ETD-core configurations with 2 primary layers.

From Fig. 3.7 it is obvious that increased core size reduces losses. Similar behaviour is observed for the results of the other analyses in appendix A and B. However, efficiency is not the only parameter of importance in the process of selecting the transformer core. It must also be noted that the larger cores has disadvantages such as increased production cost as well as product volume and weight. Hence, since the difference between the lowest power loss of the largest and smallest considered ETD-cores is only around 140 mW, which is less than 0.5 % of the max output power, the disadvantages of a large core is deemed to be of greater importance. Therefore, the ETD 29/16/10 with 30 primary windings and 13 secondary windings is chosen for the transformer. This design is shown in Fig. 3.8. The illustration is taken from *ANSYS PEmag* were the correct core, bobbin, and wire sizes are selected. This confirms that the calculations regarding size are correct.

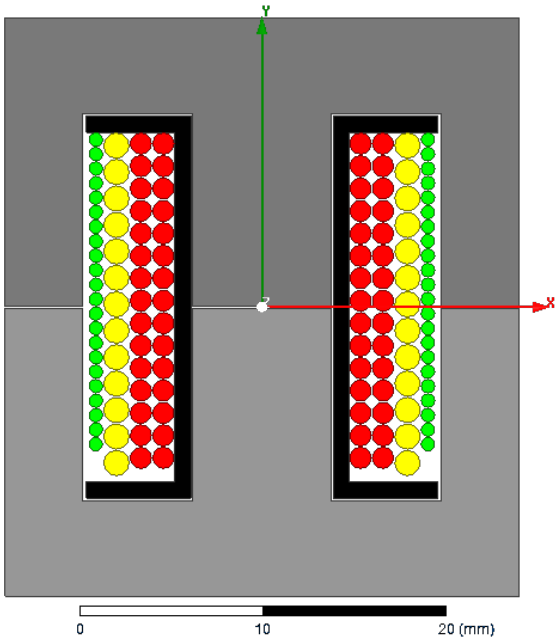


Figure 3.8: Cross section transformer. Grey: Core, Black: Bobbin, Red: Primary windings, Yellow: Secondary windings, green: tertiary windings

Note: The tertiary winding in this illustration is explained in section 5.4.1 in the control chapter.

3.7.1 Resulting Inductance

Eq. (3.11) gives a minimum inductance of 321 µH. Using the relation from eq. (3.12) and the calculated reluctance from eq. (3.15) the actual primary side magnetizing inductance can be found:

$$L_{mp} = \frac{N_p^2}{\mathcal{R}_{total}} = \frac{30^2}{2.55 \cdot 10^6\,\mathrm{H}^{-1}} \tag{3.61}$$

$$L_{mp} = 352\mu\mathrm{H} \tag{3.62}$$

3.7.2 Avoidance of Saturation

Primary Side Peak Current

The peak current at the primary side is found by assuming $P_{in} = V_{in}$ and that the shape of this current is a square with a triangle on top:

$$I_{in} = \frac{V_{out} \cdot I_{out}}{V_{in}} \tag{3.63}$$

$$I_{p,pk} = \frac{I_{in}}{D} + \Delta i_p \tag{3.64}$$

$$\Delta i_p = \frac{V_{in}}{L_{m,p}} \cdot D \cdot T \tag{3.65}$$

$$\Updownarrow \tag{3.66}$$

$$I_{p,pk} = \frac{V_{out} \cdot I_{out}}{D \cdot V_{in}} + \frac{V_{in}}{L_{m,p}} \cdot D \cdot T \tag{3.67}$$

$$\tag{3.68}$$

Furthermore, the relation $D = \dfrac{V_{out}}{n \cdot V_{in} + V_{out}}$ is used. The worst case is now calculated:

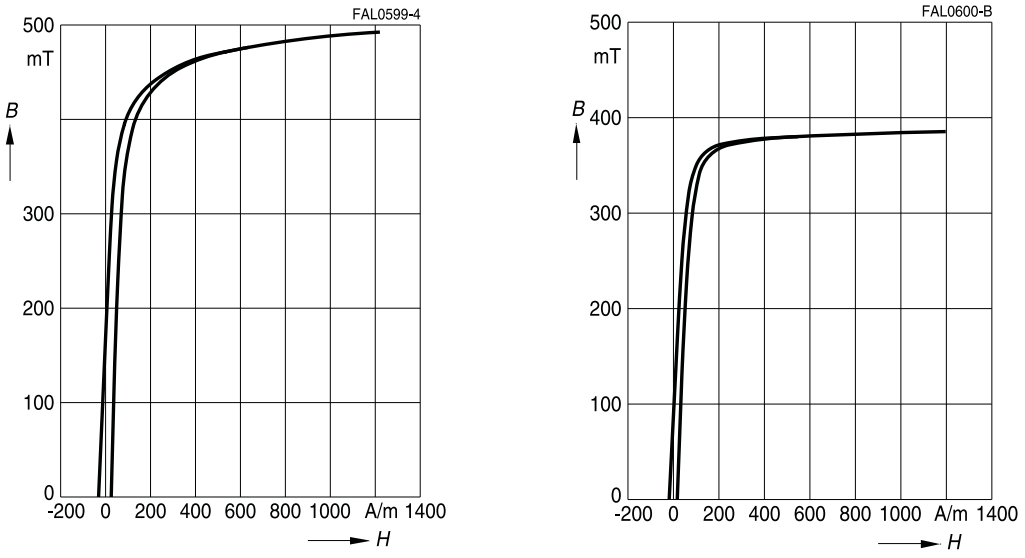
$$D = \frac{30\text{V}}{0.433 \cdot 20\text{V} + 30\text{V}} = 0.776 \tag{3.69}$$

$$I_{p,pk} = \frac{30\text{V} \cdot 1\text{A}}{0.776 \cdot 20\text{V}} + \frac{20\text{V}}{352\mu\text{H}} \cdot 0.776 \cdot 10^{-5}s \tag{3.70}$$

$$I_{p,pk} = 2.37\text{A} \tag{3.71}$$

Peak Magnetic Flux Density

The maximum allowable peak magnetic flux density is found by looking at the figures below. This shows the saturation of the core. As shown earlier, the transformer losses only cause a small temperature rise. This makes it most relevant to look at the 25 °C.



(a) 10 kHz, 25 °C

(b) 10 kHz, 100 °C

Figure 3.9: Magnetization curves for N87, [1] p. 82.

The peak magnetic flux density B_{pk} is found by using the effective permeability and the peak current:

$$B_{p,k} = \frac{N_p \cdot I_{p,pk} \cdot \mu_{total}}{l_{total}} \tag{3.72}$$

Where $l_{total} = 70.4\text{mm}$ is the magnetic length of the transformer.

$$B_{p,k} = \frac{30 \cdot 2.37\text{A} \cdot 289 \cdot 4\pi \cdot 10^{-7}\text{H/m}}{70.4\text{mm}} \tag{3.73}$$

$$B_{p,k} = 365\text{mT} \tag{3.74}$$

By looking at Fig. 3.9a it is seen that the worst case of 365mT still is less than what is required to saturate the core.

3.8 Summary

The selected design uses a TDK EPCOS 29/16/10 N87 core with a turns ratio of 30 : 13 : 22 ($n = 0.433$). The number of layers for each winding is 2:1:1.

With the chosen design, the magnetic flux density reaches a worst case peak value of 365mT which gives a margin to avoid saturation. The inductor power dissipation of 621mW results in a core temperature of 43.4°C which is far below it's temperature rating. The primary side magnetizing inductance is $L_{m\,p} = 352\mu\text{H}$.

4 | Filter Design

4.1 Introduction (CL, SK, BW & TK)

In order to attenuate the switching harmonics and eliminate the ripples, input and output filters need to be added to the converter. The converter must meet the specifications of the introduction also repeated here.

	Condition	Minimum	Maximum
V_{in}	-	20 V	40 V
V_{out}	-	5 V	30 V
I_{out}	-	-	1 A
$\Delta V_{out_{max}}$	Steady state	-	50mV
$\Delta V_{out_{max}}$	Load step	-	3 % of V_{out}
Input current harmonics	Steady state	-	*CISPR 13* average
Inrush current spike	-	-	*ETSI EN 300132-2*

Table 4.1: Converter Specifications.

The transformer parameters in table 4.2 was determined from the magnetic design in Chapter 3.

Parameter	Symbol	Value
Number of primary side turns	N_p	30*
Number of secondary side turns	N_s	13*
Turns ratio	n	0.433*
Primary side inductance	L_{M_p}	352 µH*
Secondary side inductance	L_{M_s}	66 µH*

Table 4.2: Summary of transformer parameters.

*These are the values of the final design however some simulations prior to this decision was made with the values $N_p = 26, N_s = 12, n = 0.462, L_{M_p} = 264.9\mu H$ and $L_{M_s} = 56.4\mu H$.

The following figure shows the placement of the inrush limiting circuit, input filter and output filter.

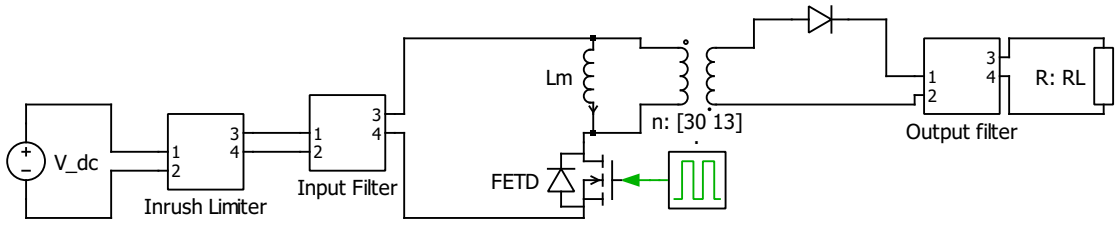


Figure 4.1: Filter design overview

4.2 Output Filter (CL, SK, BW & TK)

Normally, the only design parameters in the output filter of a flyback converter are the output capacitance and its ESR. But in this case it might be necessary with an extra filter due to the strict output ripple limitation.

4.2.1 Steady State Ripple

The steady state voltage ripple is caused by both the charging and discharging of the output capacitance and the corresponding current going through its ESR. First the minimum capacitance is found, then the maximum ESR. Since the ripple voltage is the sum of the two components, the implemented design must be stricter than these individual calculated restrictions.

$$\Delta v_{out} = \Delta v_{out_C} + \Delta v_{out_{ESR}} \tag{4.1}$$

The output capacitor supplies the output with current when the diode is reverse biased. Thus, in the interval $0 < t < DT$, the capacitor current is $-I_{out}$. Using the following equation, an expression for the minimum output capacitance is found.

$$\Delta v_{out_C} = \frac{1}{C_{out}} \int_0^{DT} i_{C_{out}} dt \tag{4.2}$$

In our case, $\Delta V_{max} = 50\,\text{mV}$. And $i_{C_{out}} = -I_{out}$ when the diode is reverse biased ($0 < t < DT$). These values are set into (4.2) and it is solved for the capacitance. The expression for minimum capacitance is given below.

$$C_{min} = \frac{I_{out} \cdot D}{\Delta V \cdot f_s} = \frac{1\text{A} \cdot 0.765}{50\text{mV} \cdot 100\text{kHz}} = 153\mu\text{F} \tag{4.3}$$

The maximum ESR can be found by using the peak to peak ripple current going through the outpu capacitor.

$$\Delta v_{out_{ESR}} = I_{p2p\,Cout} \cdot ESR \tag{4.4}$$

The peak to peak current in the capacitor is the same as the peak to peak current in the output diode. This is valid when assuming a constant load current. By looking at the diode current shape it can be seen that:

$$I_{p2p\,Cout} = I_{p2p\,Diode} = \frac{I_{out}}{1-D} + \frac{1}{2}\frac{V_{out}}{L_{ms}} \cdot (1-D)T \tag{4.5}$$

This gives a worst case scenario of $I_{p2p\,Cout} = 5.0\text{A}$ (validated by simulating). Combining this with equation (4.4) gives a maximum ESR of:

$$ESR_{max} = 10\text{m}\Omega \tag{4.6}$$

4.2.2 Loadstep Consideration

In the load step, the output current instantly changes from 1 A to 0.5 A. The voltage overshoot is calculated based on the fact that the total stored energy cannot change instantly, and hence the energy of the inductor must be transferred to the capacitor, when the output current is halved. The inductor peak current is used as a worst case scenario.

Before step:

$$E_{TOT} = E_C + E_L = \frac{1}{2} \cdot C_{out} \cdot {V_{out}}^2 + \frac{1}{2} \cdot L_s \cdot {I_{pks}}^2 \tag{4.7}$$

After step:

$$E_{TOT'} = E_{C'} + E_{L'} = \frac{1}{2} \cdot C_{out} \cdot (V_{out} + V_{ov})^2 + \frac{1}{2} \cdot L_s \cdot (I_{pks} - \frac{1}{2} \cdot I_{out})^2 \tag{4.8}$$

According to previous report:

$$I_{pks} = \frac{I_{out}}{1-D} + \frac{V_{out} \cdot (1-D)}{2 \cdot L_s \cdot fs} \tag{4.9}$$

$$L_s = 56.4\,\mu\text{H} \tag{4.10}$$

With a restriction of $V_{ov} = 3\% \cdot V_{out}$ the minimum value of C_{out} can be derived.

$$C_{out_{min}} = \frac{L_s I_{out} \cdot \left(\frac{4I_{out}}{1-D} - \frac{2V_{out}(1-D)}{L_s \cdot f_s} + I_{out} \right)}{4V_{ov}(2V_{out} + V_{ov}}) \tag{4.11}$$

Here, the duty cycle is a function of the voltages. This expression for the capacitance is plotted for the ranges of input and output voltages in Fig. 4.2.

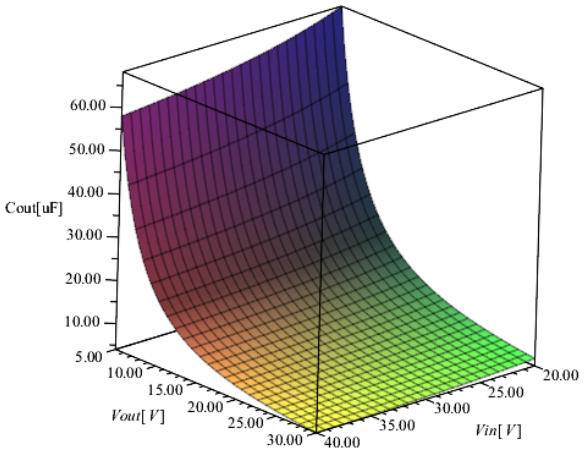


Figure 4.2: Minimum output capacitance, $C_{out_{min}}$ [µF], as a function of V_{in} and V_{out}.

As seen in figure 4.2, the worst case design situation, which has the largest necessary output capacitor requirement, occurs for the conditions $V_{in} = 20\,\text{V}$, $V_{out} = 5\,\text{V}$, where $D = 0.35$ Hence, the minimum output capacitance is:

$$C_{out_{min}} = \frac{56.4\mu\text{H} \cdot 1\text{A} \cdot \left(\frac{4 \cdot 1\text{A}}{1-0.35} - \frac{2 \cdot 5\text{V}(1-0.35)}{56.4\mu\text{H} \cdot 100\text{kHz}} + 1\text{A} \right)}{4 \cdot 0.15\text{V}(2 \cdot 5\text{V} + 0.15\text{V})} = 58.5\mu\text{F} \tag{4.12}$$

4.2.3 Equivalent Series Resistance Calculation

The maximum ESR for a loadstep from from 100% to 50% is obtained from the maximum voltage overshoot and the current change in the secondary winding.

$$ESR_{max} = \frac{V_{ov}}{I_{out_{step\,change}}} = \frac{0.03 \cdot V_{out}}{I_{pks} - 0.5 I_{out_{max}}} \tag{4.13}$$

The maximum ESR is obtained when $V_{in} = 40V$ and $V_{out} = 30V$:

$$ESR_{max} = \frac{0.15\text{V}}{3.68\text{A} - 0.5 \cdot 1\text{A}} = 287\text{m}\Omega \tag{4.14}$$

It is seen that this ESR requirement is less strict than the steady state requirement.

4.2.4 Output Capacitor Selection

Based on this, six parallel connected 50V, 405mA rated Panasonic 56µF electrolytic capacitors[4] are chosen. This gives an ESR of 67mΩ and a current rating of 2.43A as the calculations below show:

$$ESR_{each} = \frac{tan(\delta)}{2\pi f_{datasheet} C_{out}} = \frac{0.10}{2\pi \cdot 120\text{Hz} \cdot 330\mu\text{F}} = 400\text{m}\Omega \tag{4.15}$$

$$ESR_{out1} = \frac{ESR_{each}}{6} = \frac{400\text{m}\Omega}{6} = 67\text{m}\Omega \tag{4.16}$$

$$I_{capabillity} = 6 \cdot I_{rated\,each} = 6 \cdot 405\text{mA} = 2.43\text{A} \tag{4.17}$$

The ESR requirement of 10mΩ is difficult to satisfy with electrolytic capacitors only. Therefore an extra second order filter is added at the output. It is placed sufficiently low in frequency so that it gives around 20dB of attenuation.

$$C_{out2} = 122\mu\text{F}\,(2 \times 56\mu\text{F}\,(electrolytic) + 10\mu\text{F}\,(ceramic)) \tag{4.18}$$

$$L_{out2} = 2.2\mu\text{H} \tag{4.19}$$

$$ESR_{out2} = 200\text{m}\Omega \tag{4.20}$$

At the end of this chapter, the RMS currents in the capacitors will be simulated and compared to their current ratings. This extra second order filter is assumed to not alter the input characteristics noticeably, and is therefore not considered in the rest of this chapter.

4.3 Input Filter (CL, SK & TK)

4.3.1 Simulated Input Harmonics

The conducted EMI is investigated by simulating the flyback converter in *PLECS* and measuring the input current. First simulations is done without an input filter. See Fig. 4.3. This simulation is done for all four corner cases as listed in table 4.3.

Case	V_{in}	V_{out}	I_{out}	D
1	20V	30V	1A	0.76
2	40V	30V	1A	0.62
3	40V	5V	1A	0.21
4	20V	5V	1A	0.35

Table 4.3: The four corner cases of operation

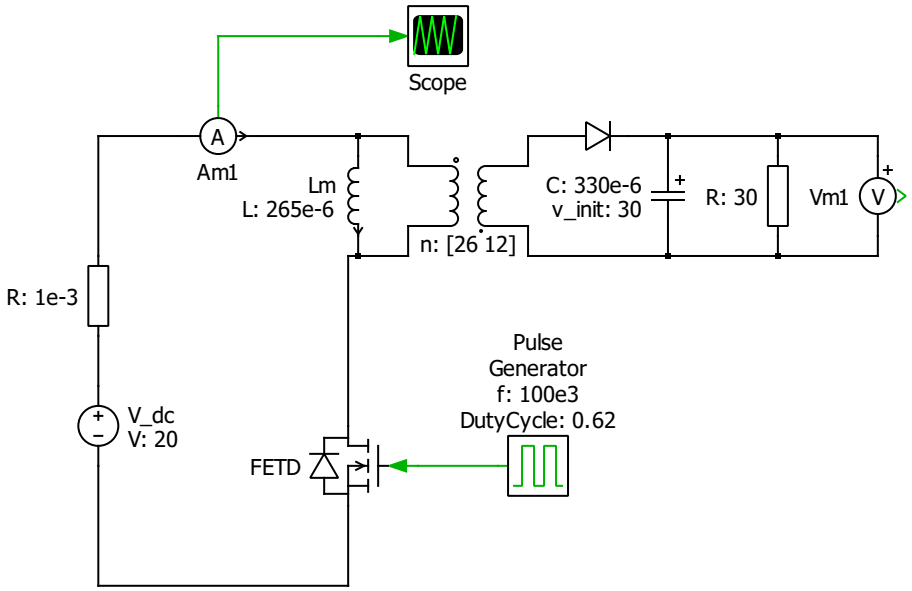


Figure 4.3: PLECS simulation setup. Without input filter.

The current simulation results is exported to *MATLAB* where a FFT is performed. The time sample is 0.1µs long, which results in a spectral resolution of 10kHz. This is more than sufficient as the fundamental frequency is ten times as large. Now the current is converted to dB µV. This is done to simulate a LISN network measurement. The following formula is used.

$$V_{LISN} = 20 \cdot log10(|I_{in}| \cdot \frac{50\Omega}{1\mu V}) \tag{4.21}$$

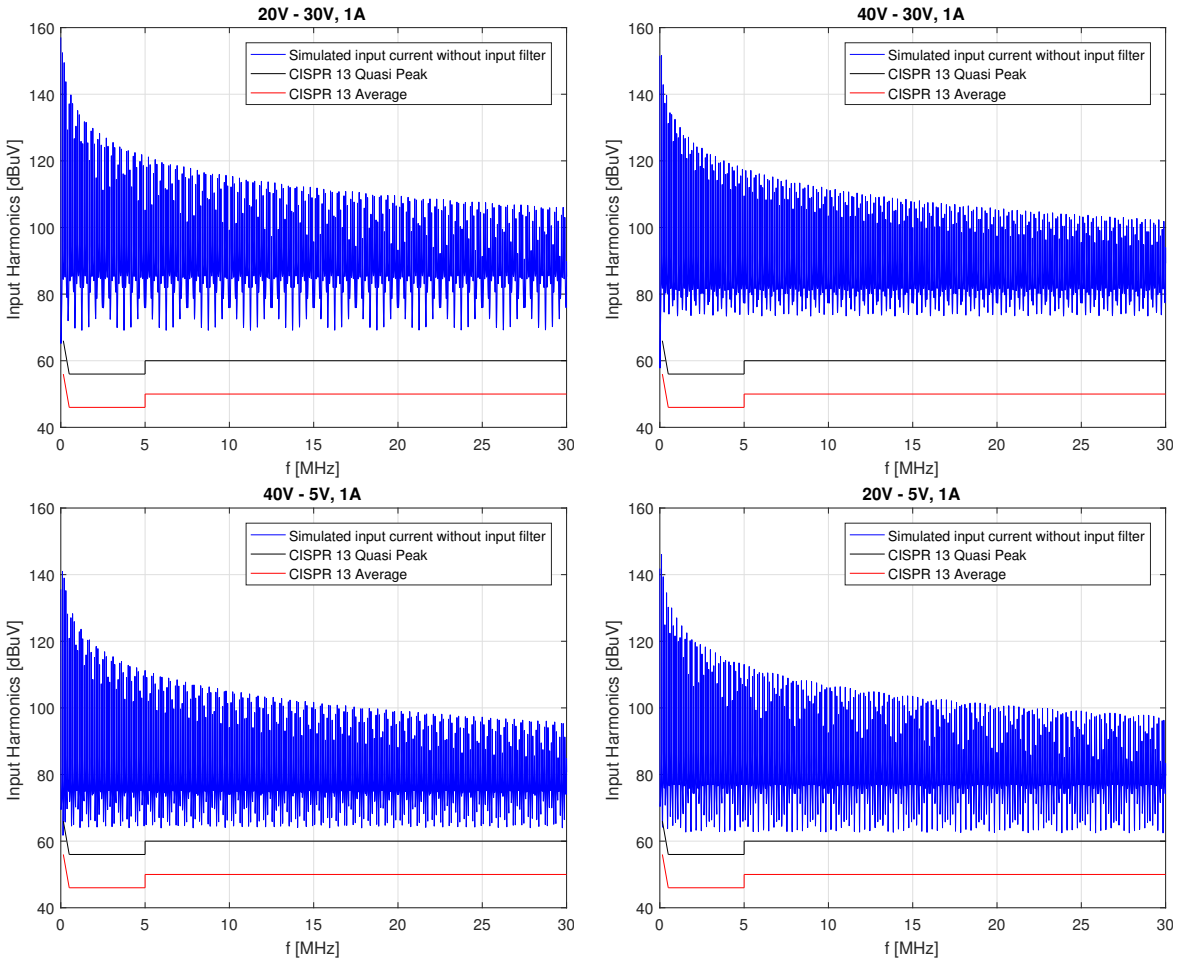


Figure 4.4: Input Harmonics and CISPR 13 limits

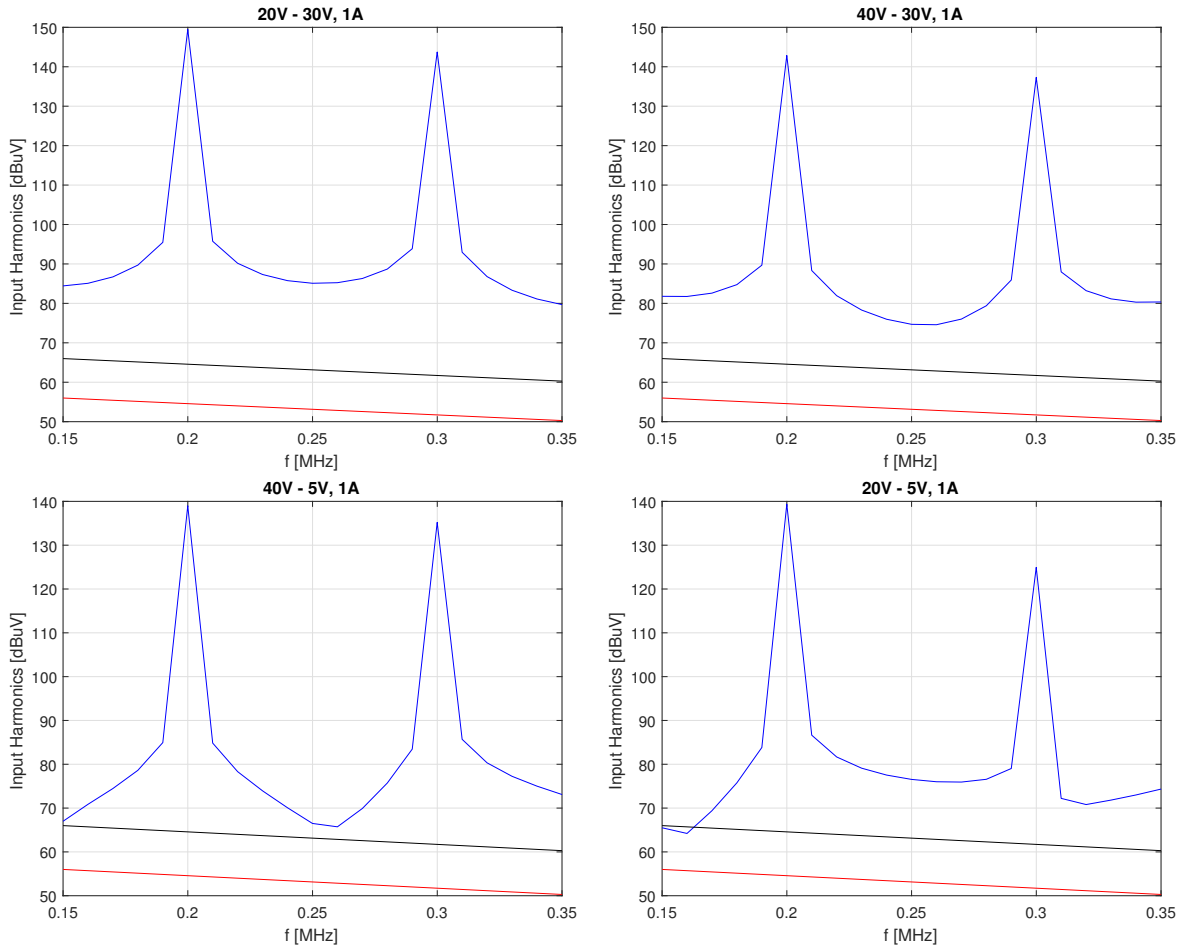


Figure 4.5: Input Harmonics and CISPR 13 limits, zoomed in at the second and third harmonics. Same colors as previous figure.

It is obvious that the input side must have a filter in order to meet the *CISPR 13* limits. The worst violation is at the second harmonic (200kHz) for the first case. As seen in the first part of Fig. 4.5, a damping of 149.5dB − 54.5dB = 95dB is required.

4.3.2 Designing the filter

Undamped Filter

Three second order low pass filters are cascaded in order to achieve enough dampening. One second-order filter can achieve 40dB dampening per decade but by placing the cut-off frequency at very low frequency requires very big components so it was decided that cascading several would be a better choice.

It is the current from the converter to the source that requires dampening. The transfer function of this is equal to the voltage transfer function from the source (the opposite way).

The first filter from the left has the highest cut-off frequency because then the gain and phase of a signal at lower frequency is approximately unchanged. However this is just a simplification for placing the designing the component values, as there is current flowing in between the second-order filters their transfer functions cannot be cascaded and need to calculated for the entire filter. But resonances of the sixth-order filter is made by cascading three second-order filters with descending cut-off frequency spaced sufficiently apart to lower the affect they have on each other.

As mentioned a damping of 95dB is required at 200kHz. If this requirement is fulfilled the nature of the filter also satisfies all other requirements of dampening, as higher frequencies are damped more and the required damping from 150kHz to 200kHz are low.

The cutoff frequency of the individual second-order filters are $10^{0.5}$ apart. The first filter is designed to give roughly 60dB attenuation the second filter to give 40dB attenuation and the the 3rd filter 20dB attenuation. This should give enough attenuation for the overall filter.

Damped Filter

R_f - L_b parallel damping is chosen as it requires smaller components than R_f - C_b damping[5](chapter 10.4).

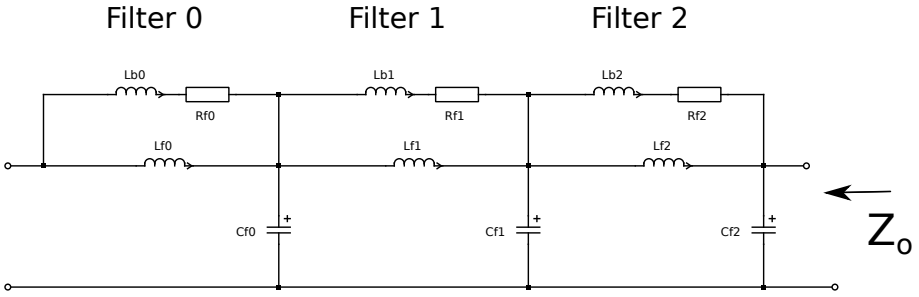


Figure 4.6: Input filter topology

Now, the stability of the filter is investigated. The output impedance of the filter must be meet *Middlebrooks's* impedance inequalities.

$$||Z_o|| \ll ||Z_D|| \tag{4.22}$$

$$||Z_o|| \ll ||Z_N|| \tag{4.23}$$

While the output impedance is calculated by shorting the input side of the filter, Z_N and Z_D is found from the small signal model of the Flyback converter. This model is given in Erickson[5]. Repeated here for convenience:

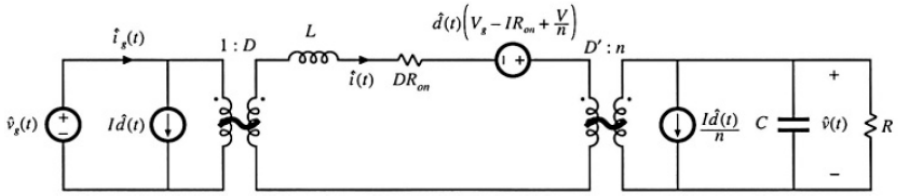


Figure 4.7: Small signal model of the Flyback converter

All components, currents and voltages is transformed into the middle of this converter in order to remove the transformers. Furthermore, the on-resistance of the switch is neglected. Z_D is now found as the input impedance with the duty cycle perturbation $\hat{d}$ set to zero. Z_N is found as the input impedance when $\hat{d}$ is adjusted such that the output perturbation $\hat{v}$ is zero. These impedances were found by solving KVL and KCL equations.

$$Z_D = \frac{D'^2 \cdot R_L}{D^2(1 + s \cdot R_L \cdot C_{out})}\left(\frac{1}{n^2} + s \cdot \frac{L_{M_p}}{D'^2 R_L} + s^2 \frac{L_{M_p} \cdot C_{out}}{D'^2}\right) \tag{4.24}$$

$$Z_N = -\frac{R_L \cdot D'^2}{D^2}\left(\frac{1}{n^2} - s \cdot \frac{D \cdot L_{M_p}}{R_L \cdot D'^2}\right) \tag{4.25}$$

These expressions fits with the expression for the Buck-Boost converter[5] when the turns ratio is set to $n = 1$.
When damping the filter there is a trade-off between the amount of damping and the degradation of the HF attenuation of the filter. The following procedure is used to obtain the optimal damping (selecting L_b and R_f according to section 10.4.2 in Erickson). This is done for all three filters separately. Then the stability is analyzed for the combined filter.

1. Finding the lowest of Z_N and Z_D at the resonance frequency of the undamped filter.
2. Setting maximum impedance, $||Z_o||_{mm}$, 20dB lower than this to achieve a margin.
3. Calculating $n = \dfrac{L_b}{L_f}$ according to eq. 10.35 and 10.26 in Erickson.
4. Setting $L_b = n \cdot L_f$
5. Calculating the optimal R_{f0} from eq. 10.37 in Erickson.

Z_N and Z_D are plotted for the four corner cases as they are affected by the duty cycle. The following plots show the stability analysis for the three filters.

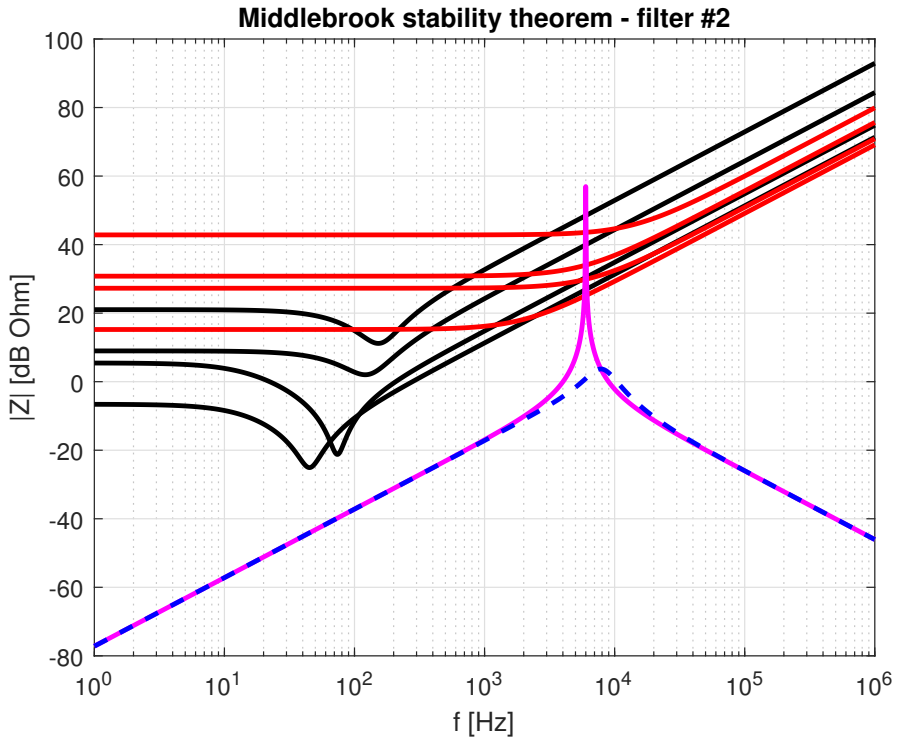


Figure 4.8: Impedance comparison for filter 2. Red: Z_N, Black: Z_D, Magenta: $Z_{o_{2(undamped)}}$, Blue: Z_{o_2}

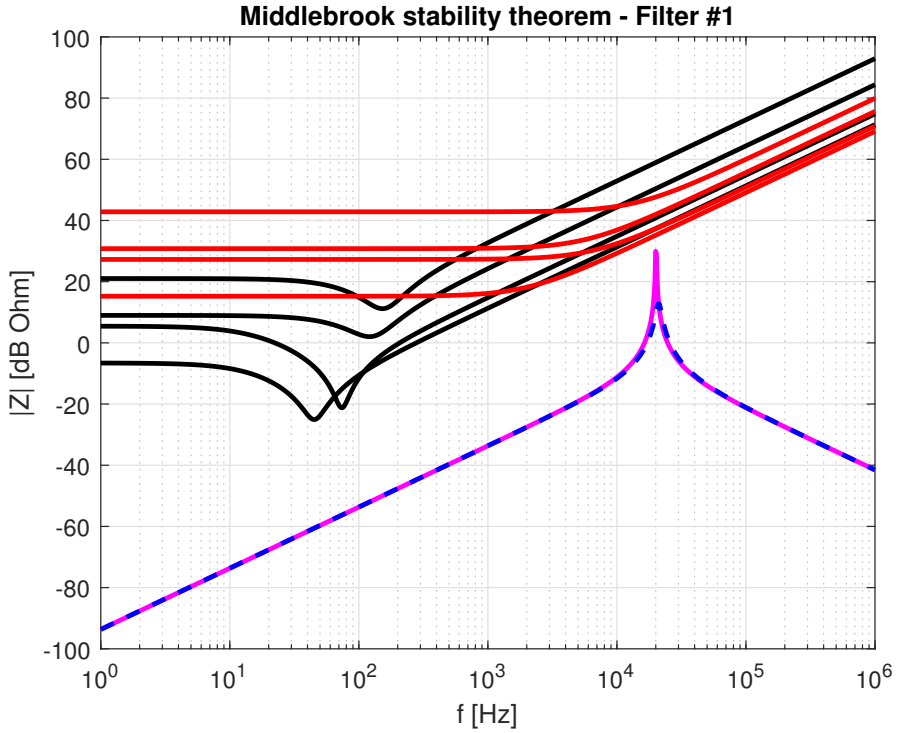


Figure 4.9: Impedance comparison for filter 1. Red: Z_N, Black: Z_D, Magenta: $Z_{o_{1(undamped)}}$, Blue: Z_{o_1}

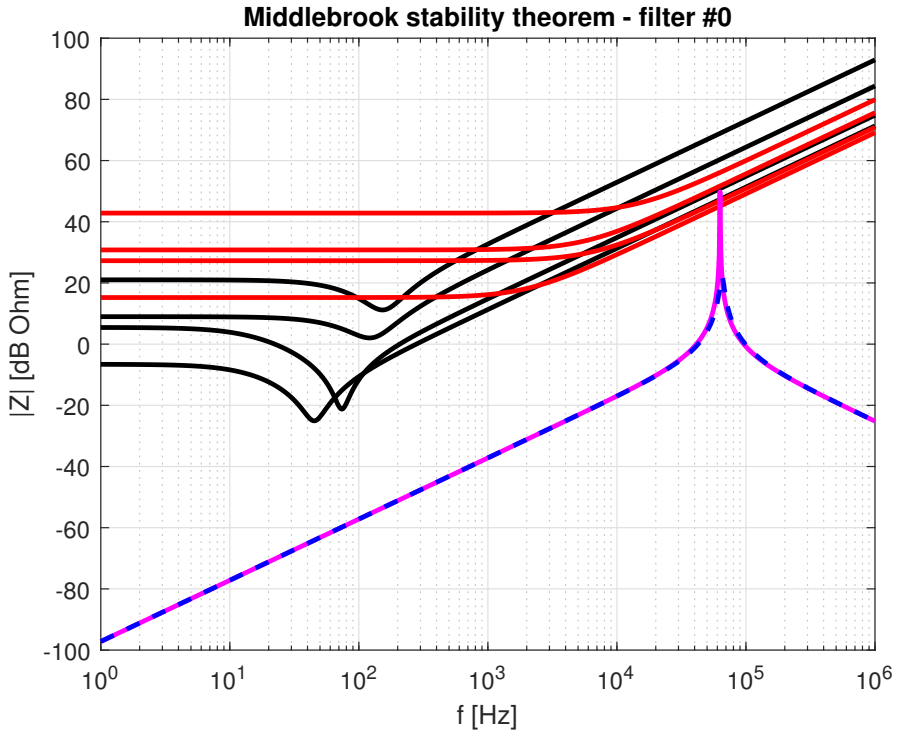


Figure 4.10: Impedance comparison for filter 0. Red: Z_N, Black: Z_D, Magenta: $Z_{o_{0(undamped)}}$, Blue: Z_{o_0}

4.3.3 Validation of the Filter

Stability

The combined filter (filter 2, filter 1 and filter 0 cascaded) output impedance is now used to check *Middlebrook's stability theorem.*

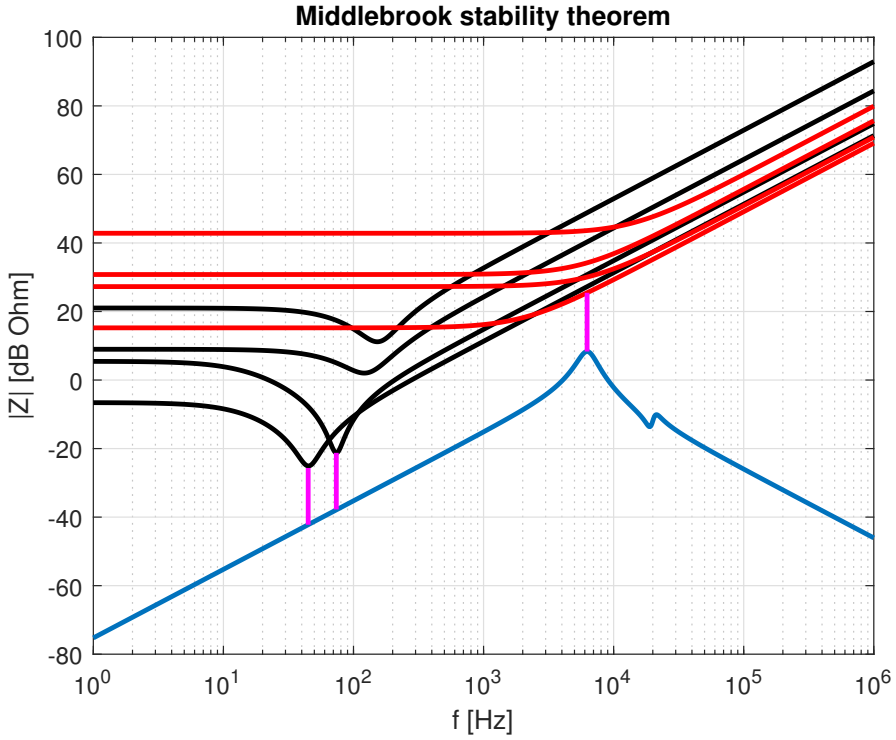


Figure 4.11: Impedance comparison for entire filter. Red: Z_N, Black: Z_D, Blue: Z_o, Magenta: Margins

Fig. 4.11 shows the stability margins. They are 16.6dB, 16.5dB and 17.1dB from left to right.

Calculated Harmonics Damping

The transfer function of the designed filter is now calculated without using the independent filter assumption. Its gain and phase are plotted below.

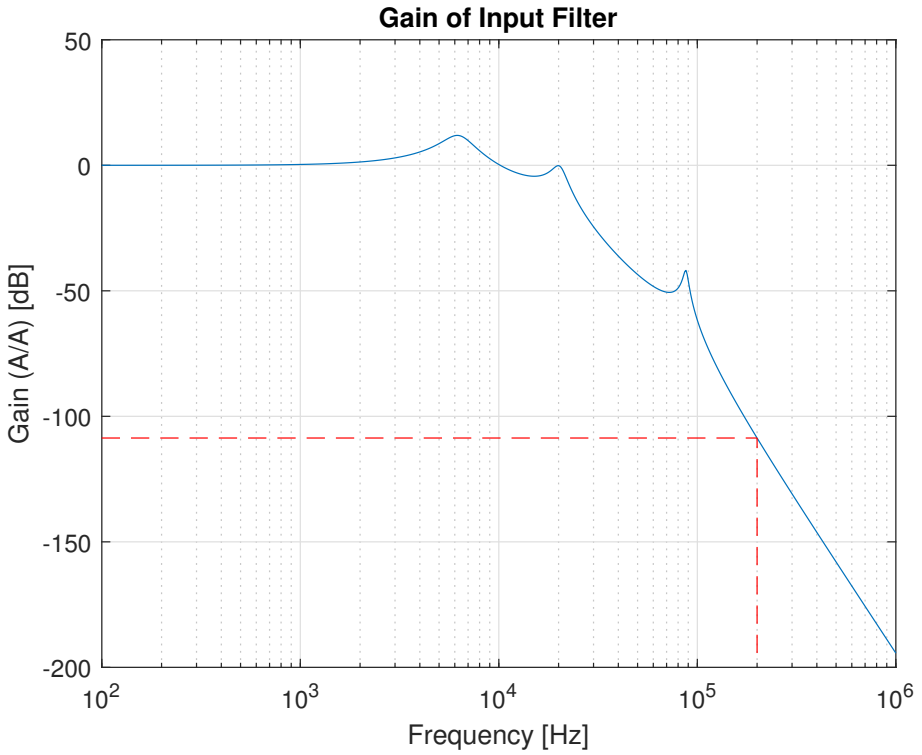


Figure 4.12: Filter gain, from transfer function, with the 200kHz point marked

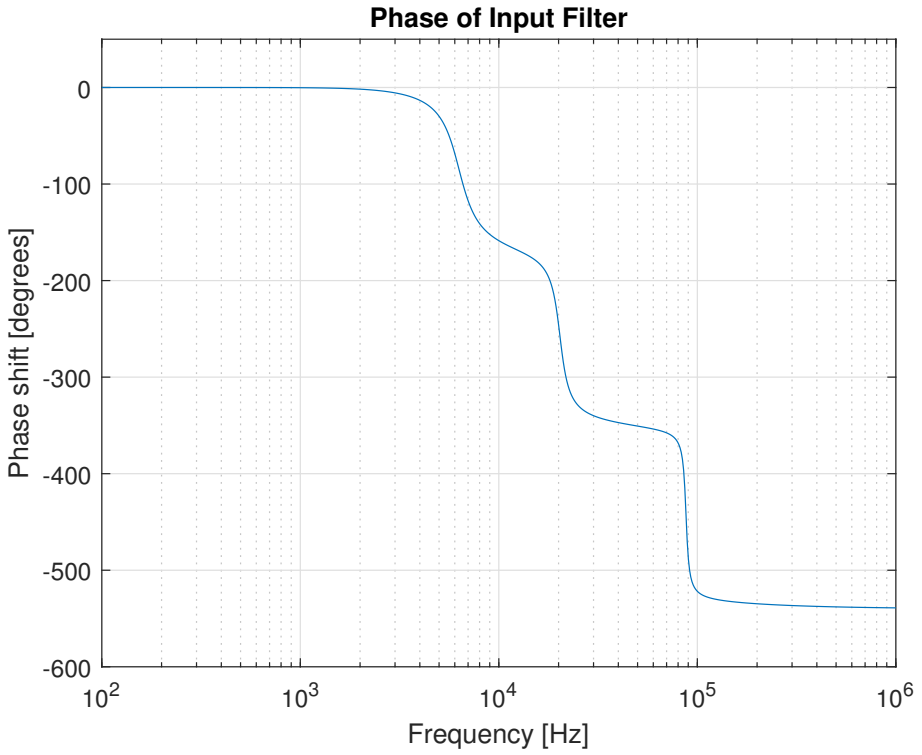


Figure 4.13: Filter phase, from transfer function

From this it is seen that the attenuation at 200kHz is 108.6dB which is more than the required 95dB.

Simulated Harmonics Damping

The input filter is now added to the *PLECS* simulation. The harmonics are measured the same way as without the filter. Fig. 4.14 show the simulation setup.

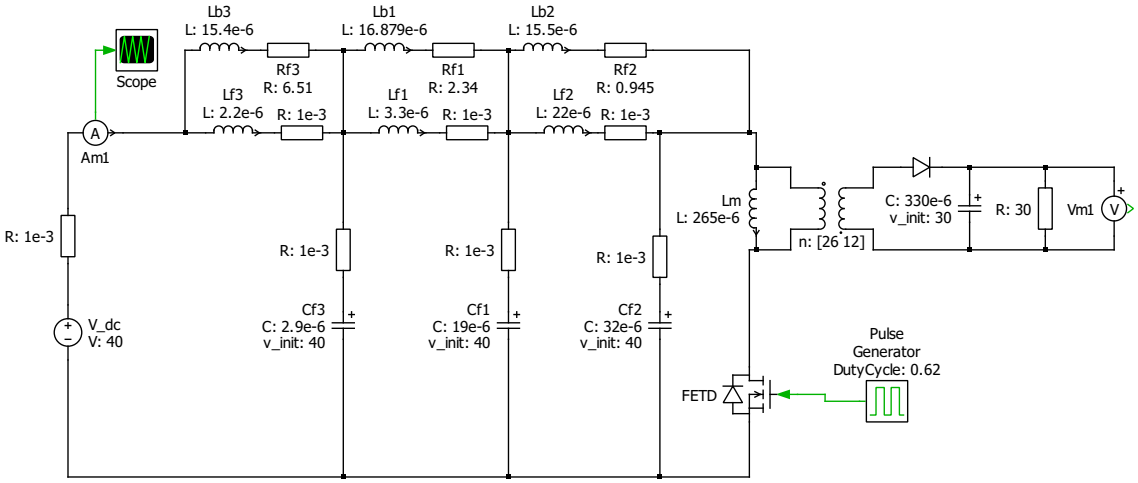


Figure 4.14: PLECS simulation setup with input filter.

The simulations results are shown in the following two figures.

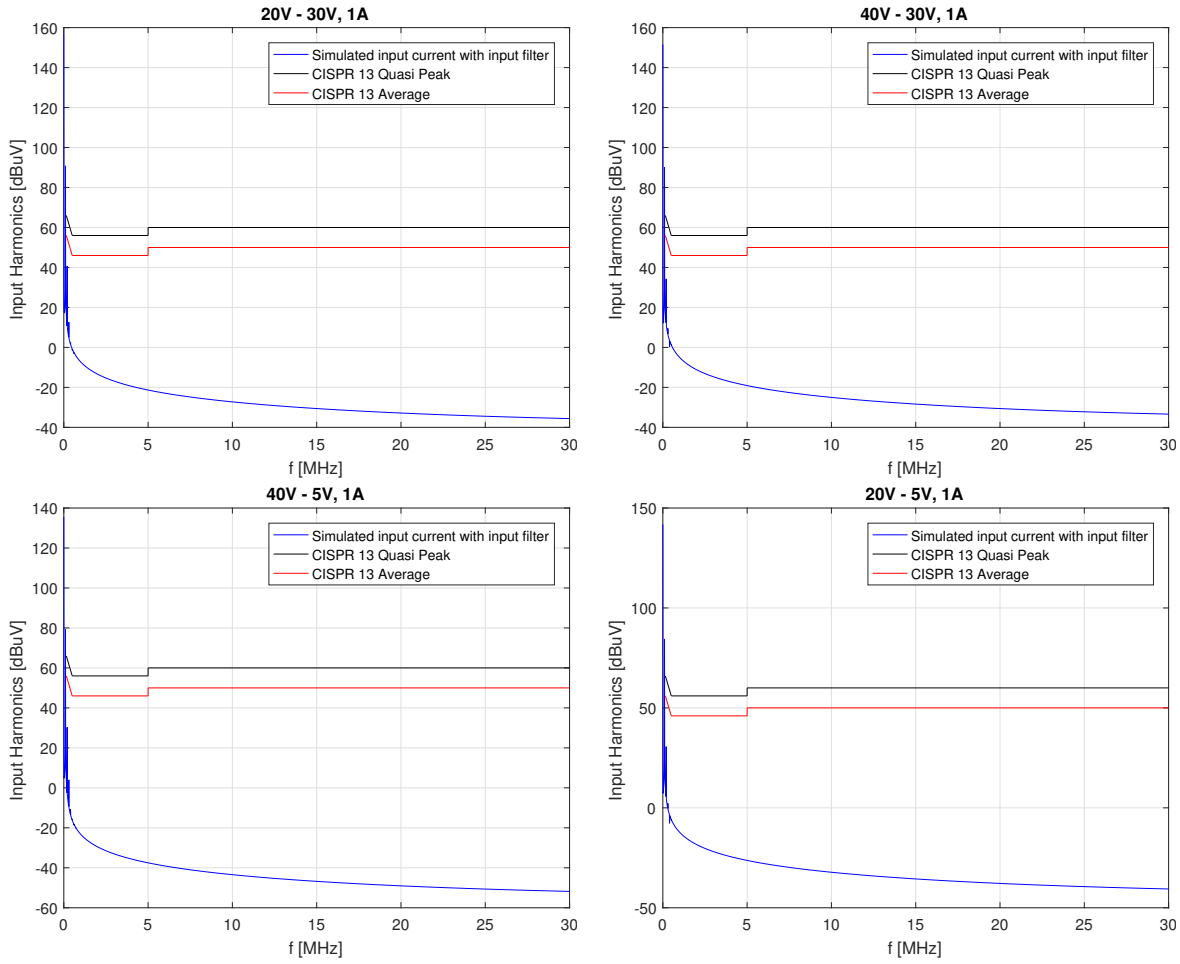


Figure 4.15: Input Harmonics and CISPR 13 limits with input filter

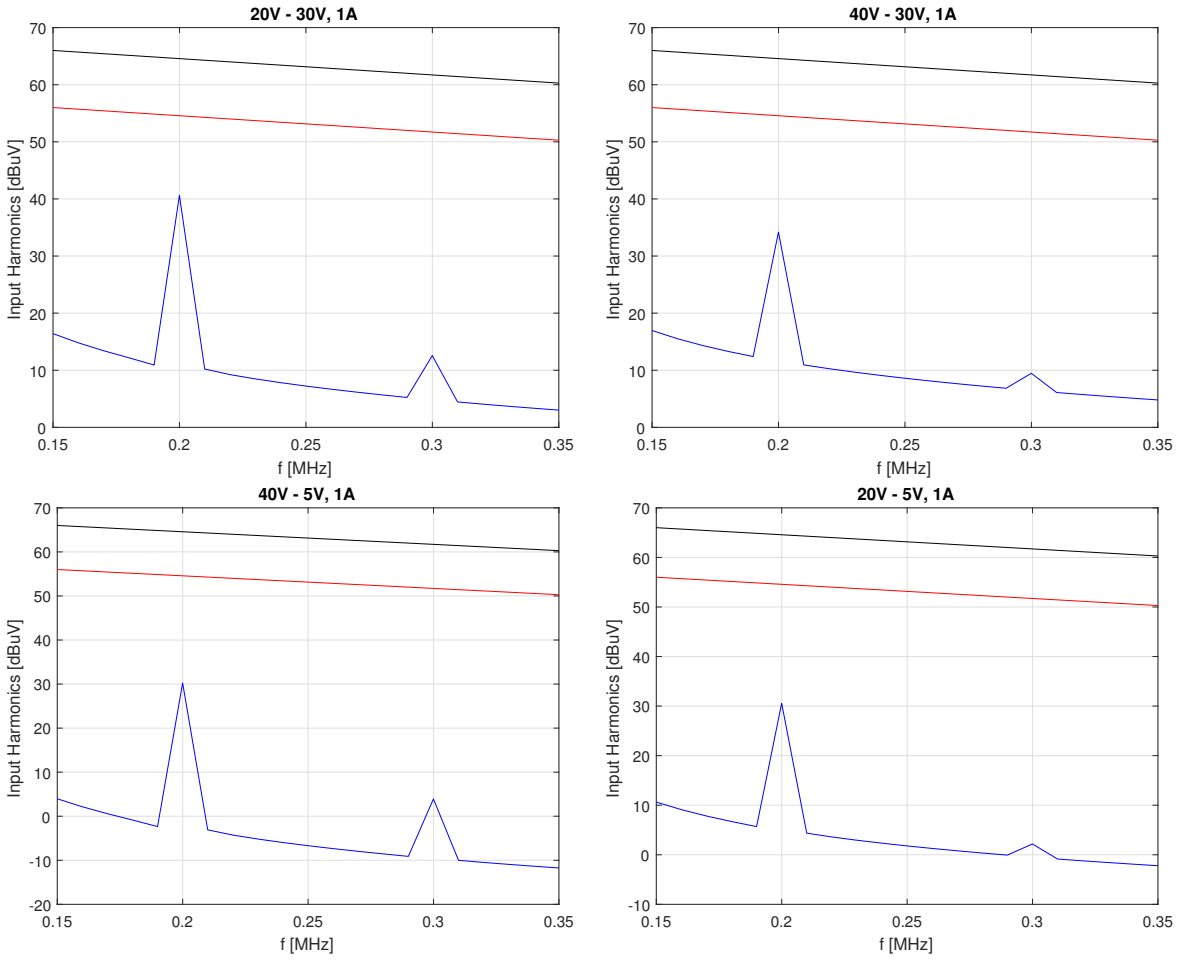


Figure 4.16: Input Harmonics and CISPR 13 limits with filter, zoomed in at the second and third harmonics. Same colors as previous figure.

From this it is seen that the harmonics now are below the *CRISPR 13* limits. The smallest margin is again for case 1, now with a margin of 14dB.

Inrush Current

There will be two significant spikes in the input current. One when connecting the converter to the DC supply voltage. This will be because of the rapid charging of the capacitors at the input side of the DC-DC converter. Likewise, there will be a spike when starting up the converter. Then the output side capacitor is charged. Both spikes are investigated according to the *ETSI EN 300132-2*[6] standard. Here the input current is normalized to the maximum nominal current of the converter which for our case is 1.5A.

Starting the Converter

The worst case for this current spike is when the output voltage is high and the load current is high. Two cases are tested, one with low and one with high input voltage. The load is assumed to be purely resistive.

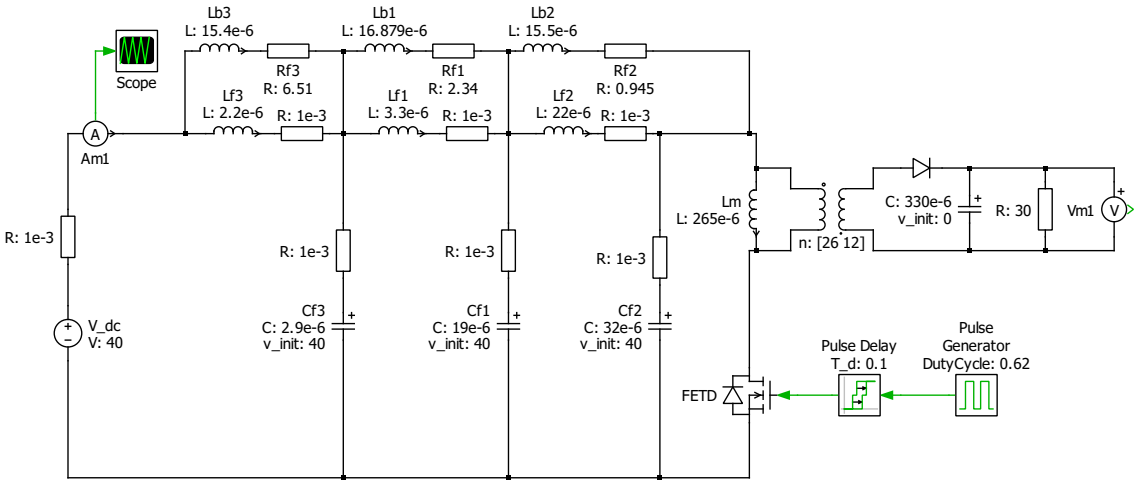


Figure 4.17: PLECS simulation setup for inrush current when starting the converter.

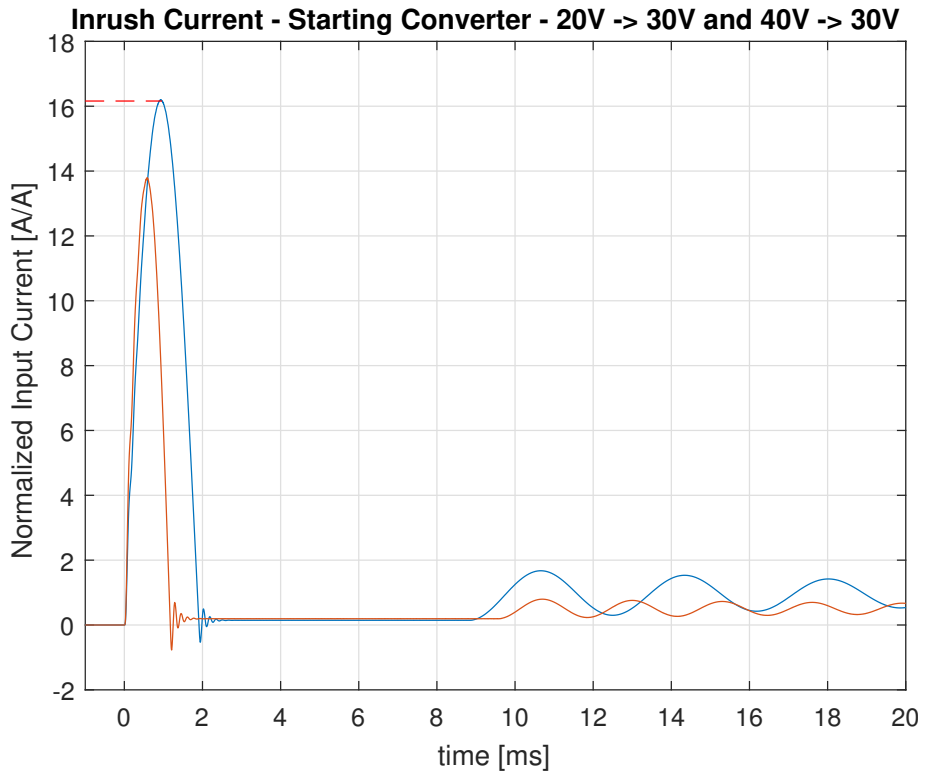


Figure 4.18: Inrush current simulation results when starting the converter (at $t = 0$). Simulated for two different input voltages.

The oscillations are some short term resonance in the input filter.

Connecting the Converter

The worst case for this current spike is when the input voltage is high. Because of this, the case of $V_{in} = 40\text{V}$ is simulated. The switch is removed and the initial capacitor voltages and inductor

currents are set to zero. Then the voltage supply is suddenly connected. The following figures show the simulation setup and results.

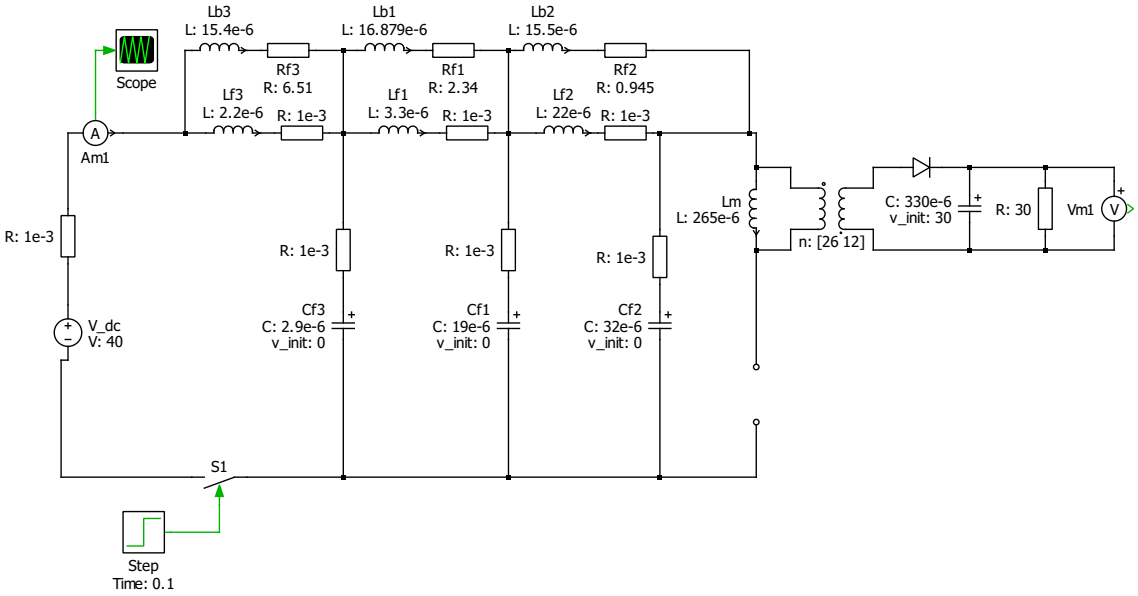


Figure 4.19: PLECS simulation setup for inrush current when connecting the converter.

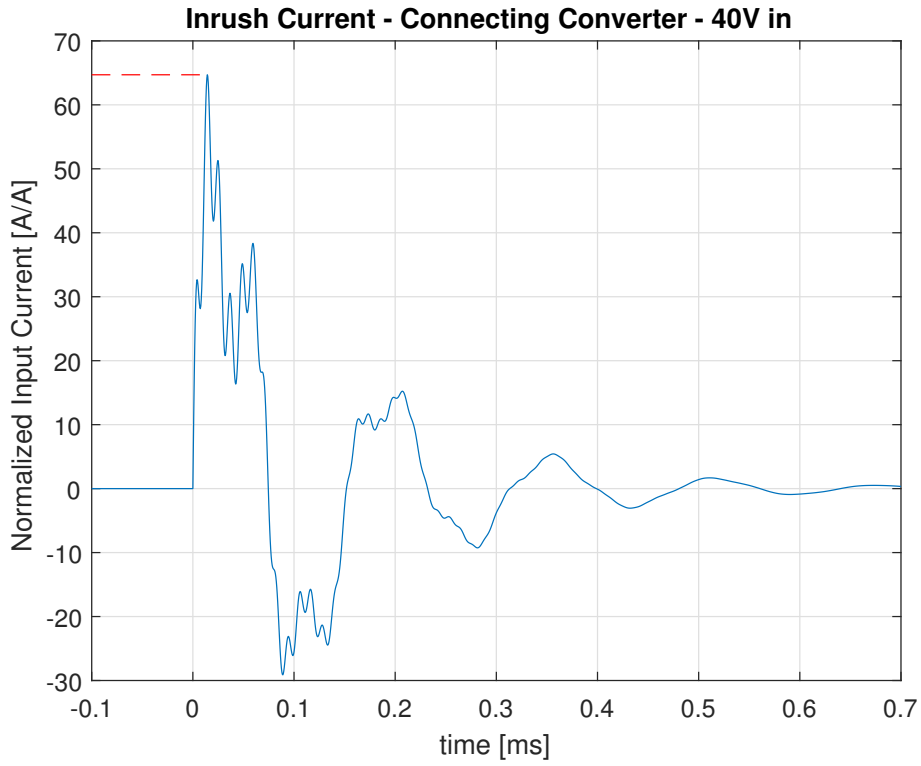


Figure 4.20: Inrush current simulation results when connecting the converter.

Here it is seen that the input current spikes to 65 times the nominal maximum input current. This is above the maximum of 48 given by *ETSI EN 300132-2*. Anyway, it is interesting to see that the

fundamental frequency of the waveform in Fig. 4.20 fits with the dominating resonance frequency of the input filter (6kHz).

Inrush Limiting Circuit

The simulations showed that some sort of inrush limiting is needed. However, the power loss should still be low. Because of this it is decided to place an NMOS with a low $R_{DS_{ON}}$ in the negative lead of the input terminals. This switch will close when a capacitor at its gate is charged. A zener diode is used to limit the gate voltage. The *FDD8444_F085TR-ND* MOSFET[7] is selected due to its low on resistance of $R_{DS_{ON}} = 5.2\text{m}\Omega$. The zener diode is set to 11volt to keep the MOSFET conducting.

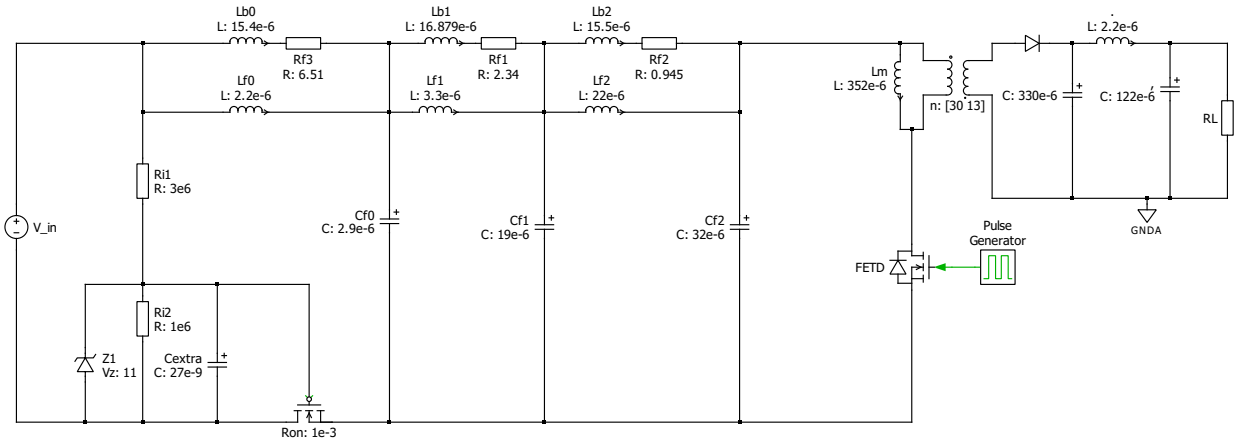


Figure 4.21: Complete circuit with inrush limiter

Simulations of the new inrush current were performed in *LTSpice* due to *PLECS* limitations. These simulations show sufficient limitation of inrush current spike (4A) and a steady state loss of $\approx$ 2mW. Fig. 4.22 show the normalized current spike when connecting the converter to the DC source.

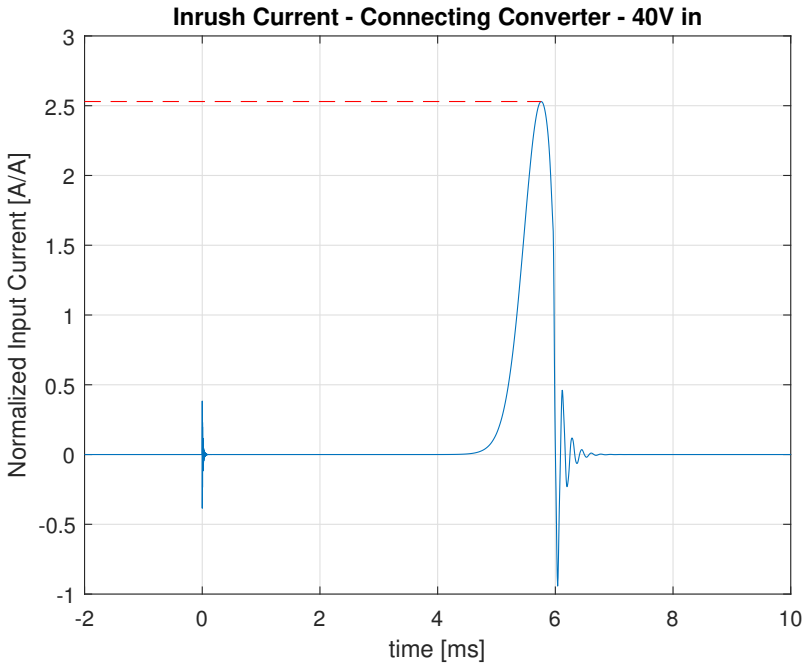


Figure 4.22: Input current spike when connecting the converter. With inrush limiter

4.3.4 Selection of Components

All capacitors at the input side are chosen to be ceramic capacitors. This is done because they have a small ESR. This is important as ESR in the input filter changes the filter behaviour. Furthermore, ceramic capacitors are small in size. But as the small signal capacitance deteriorates with the bias voltage, 100V rated capacitors are chosen for the input filter.

4.4 RMS Currents of Capacitors (CL, SK & TK)

The RMS currents of the capacitors closest to the transformer are investigated by simulation in the four cases.

Case	V_{in}	V_{out}	I_{out}	I_{Cf2RMS}	$I_{CoutRMS}$
1	20V	30V	1A	0.818A	1.75A
2	40V	30V	1A	0.342A	0.745A
3	40V	5V	1A	0.238A	0.539A
4	20V	5V	1A	0.635A	1.34A

Table 4.4: Capacitor RMS currents

The worst cases for the input side and output side capacitor currents are 0.818A and 1.75A respectively.
Thus, it would for example be sufficient to have the selected capacitor at the output.[4]. Furthermore, the capacitor current is no issue in the primary side capacitor C_{f_2} as ceramic capacitors are chosen. (Lower ESR gives lower power losses).

4.5 Filter Design Summary (CL, SK, BW & TK)

This summarizes the design of the input and output filter of the Flyback converter. A single capacitor was selected as an output filter. Three low-pass filters were cascaded as input filters. They were R_f-L_b parallel damped in order to meet Middlebrook's stability theorem. Additionally, small value ceramic capacitors will be used for HF damping. Finally ,an inrush limiting circuit is used.

Parameter	Value
C_{out_1}	$6 \times 56\mu F$
C_{out_2}	$2 \times 56\mu F + 1 \times 10\mu F$
L_{out_2}	$2.2\mu H$
C_{f_2}	$32\mu F$
L_{f_2}	$22\mu H$
R_{f_2}	0.95Ω
L_{b_2}	$155\mu H$
C_{f_1}	$19\mu F$
L_{f_1}	$3.3\mu H$
R_{f_1}	2.3Ω
L_{b_1}	$16.9\mu H$
C_{f_0}	$2.9\mu F$
L_{f_0}	$2.2\mu H$
R_{f_0}	6.5Ω
L_{b_0}	$15.4\mu H$
R_{i_1}	$3M\Omega$
R_{i_2}	$1M\Omega$
V_z	11V
C_{extra}	27nF

Table 4.5: Filter Parameters. See Fig. 4.21.

Simulations show that the design criteria given in table 4.1 are met. Furthermore, the filters are not unreasonably large in size as a higher order filter were used.

5 | Control Circuit (CL, SK & TK)

5.1 Control Scheme

Current mode control is chosen. This makes a type 2 compensator favorable compared to type 1 and 3. Type 2 has better phase margin than type 1, with a phase boost of 90 degrees. Type 3 is not necessary as type 2 gives sufficient phase margin.
To regulate the output voltage a TLVH431 shunt regulator is used as an error amplifier. This compares the output voltage with a reference voltage of 1.24V. The output voltage is changed by varying the lower resistor in the voltage divider. The reason for using this instead of the standard TLV431 is that it allows for a wider voltage swing.
When the output voltage is too large and the divided voltage is larger than 1.24V the regulator passes more current. Which in turn causes a larger current to flow through the optocoupler. Increased current causes a lowered voltage at the output of the optocoupler. This lowered voltage gives a lower reference current to the peak current controller. This reduces the duty cycle which causes an reduction in the output voltage. Thus, the converter will be stable if only the phase margin is sufficiently large.
The optocoupler makes it possible to keep the primary side isolated from the secondary side. The FET current is measured with a series resistor which gives a voltage to the peak current controller. When this current measurement is larger than the limit set by the signal from the optocoupler, the FET switches off until the next switching period. Furthermore, subharmonic oscillation is avoided by using slope compensation.

5.2 Open Loop Analysis and Compensator Design

5.2.1 Plant Analysis

1. Analyse plant
2. Set wanted crossover frequency
3. Place poles and zeros to give desired phase behavior
4. Adjust gain to get wanted crossover frequency
5. Double check phase margin

The duty cycle to output voltage transfer function of a flyback can be derived from the small signal model given by Erickson.[5] The transfer function has a low frequency horizontal asymptote, an LC resonance peak and a second order decaying high frequency asymptote. However, the algebraic expression is not used as open loop characteristics can be analyzed in PLECS simulations.
As a rule of thumb, the crossover frequency can be set to a 10th of the switching frequency or a bit lower. This frequency should be high enough to have a quick system, but low enough so that noise doesn't influence the performance. Another possible way is to decide the crossover frequency based on the converters output impedance and the maximum undershoot at a given load step. For this application it is decided to set it to 2kHz and then simulate the closed loop behaviour. Also, it is desired to boost the phase around this frequency to achieve a phase margin of at least 45°.

5.2.2 Compensator Design

The compensation is achieved by adding a network of resistors and capacitors around the *TLV431* as seen in Fig. 5.1.

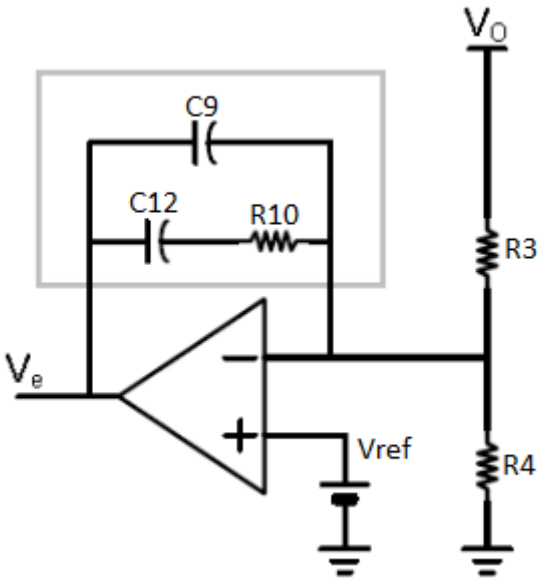


Figure 5.1: The TLV431 and the compensation network

Here, the pole caused by the output capacitance of the optocoupler is not considered. However, it is considered when simulating. The presence of this pole causes some extra high frequency damping. The transfer function of the type 2 compensator is

$$G(s) = -\frac{1 + sR_{10}C_{12}}{sR_3(C_{12} + C_9)\left(1 + sR_{10}\dfrac{C_{12}C_9}{C_{12} + C_9}\right)} \tag{5.1}$$

The transfer function of the type 2 compensator consists of a zero and a pole, a pole at origin and a gain. The pole at origin will give the compensator a 90 degree phase lag at low and high frequencies. If the zero is placed before the pole it will shift the phase towards 0 degrees before the pole will the shift it back towards 90 degrees.

The pole and zero are placed such that the phase is boosted at the desired crossover frequency. If $C_{12} >> C_9$ the pole and zero of the compensator are:

$$\omega_{p1} = \frac{1}{R_{10}C_9} \tag{5.2}$$

$$\omega_{z1} = \frac{1}{R_{10}C_{12}} \tag{5.3}$$

Changing R_3 changes the gain across all frequencies. ω_{z1} is placed lower than the crossover frequency to boost the phase and ω_{p1} at higher frequencies. A zero at $\omega_{z1} = 50\text{rad/}sandapoleat\omega_{p1} = 10{\cdot}10^3\text{rad/s}$ achieves a phase boost around the desired crossover frequency. Choosing $R_{10} = 160\text{k}\Omega$ and solving eq. 5.2 and 5.3 with the chosen values of $\omega_{z1}and\omega_{p1}$ The capacitances are calculated to be $C_{12} = 20\text{nF}$ and $C_9 = 100\text{pF}$. The gain is then adjusted to achieve the desired crossover frequency with $R_3 = 800\text{k}\Omega$. The bode plot of the designed compensator is shown in figure 5.2.

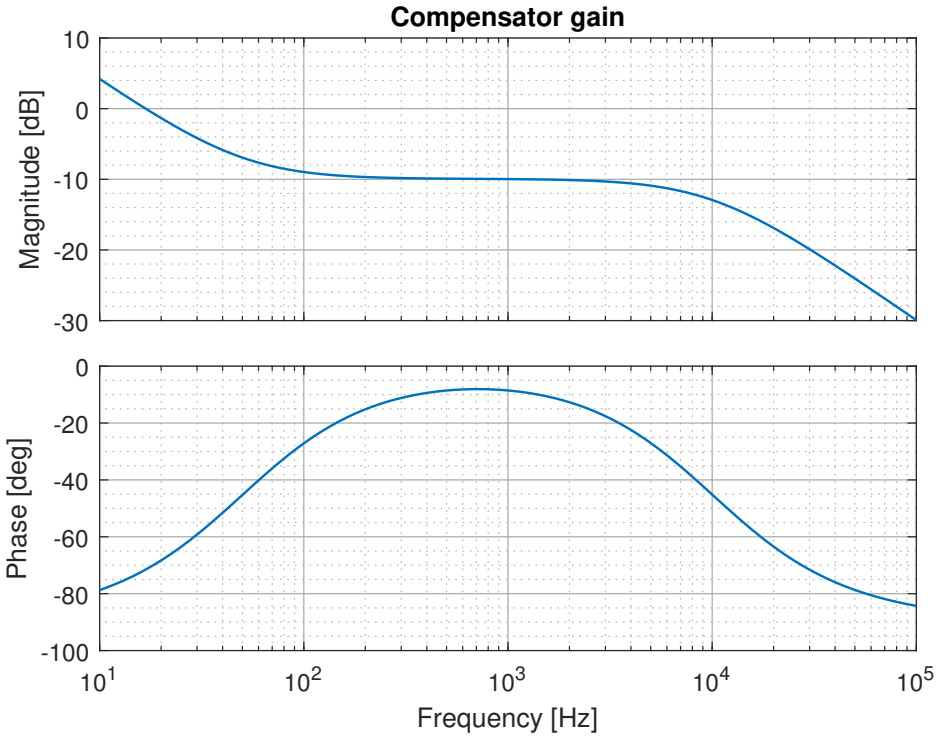


Figure 5.2: Frequency response of the designed type 2 compensator

The chosen components are now used to simulate the open loop behaviour in PLECS. Fig. 5.3 shows the simulation setup. Here a loop gain meter is used. It finds the closed loop operating point and then performs an open loop measurement.

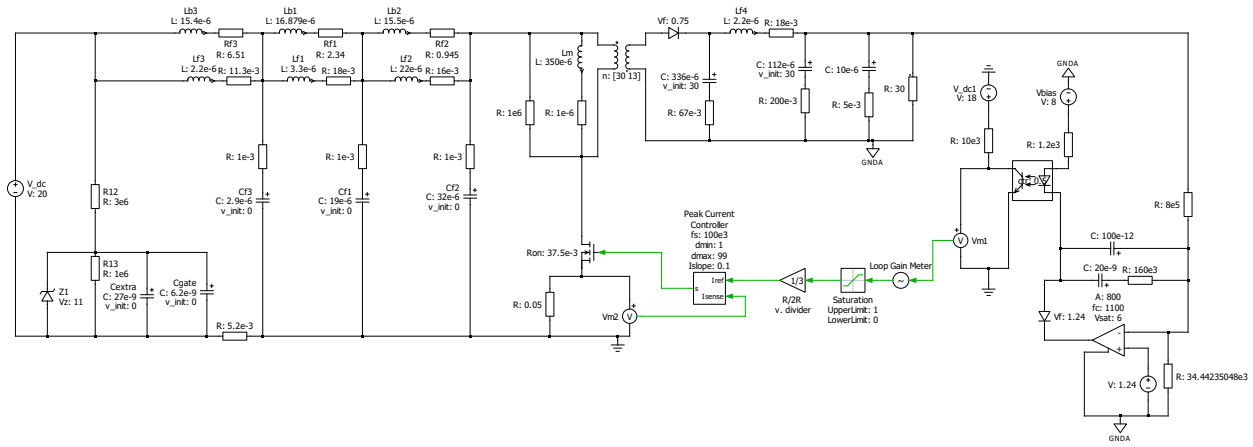


Figure 5.3: Model for loop response simulation in PLECS. Resistive parasitics are included in this model

The simulated loop gain (both plant and feedback) is shown in fig. 5.4 in the 4 corner cases (max load). The crossover frequency varies from ≈ 1kHz to 3.4kHz and the phase margin is 60 degrees for the worst case.

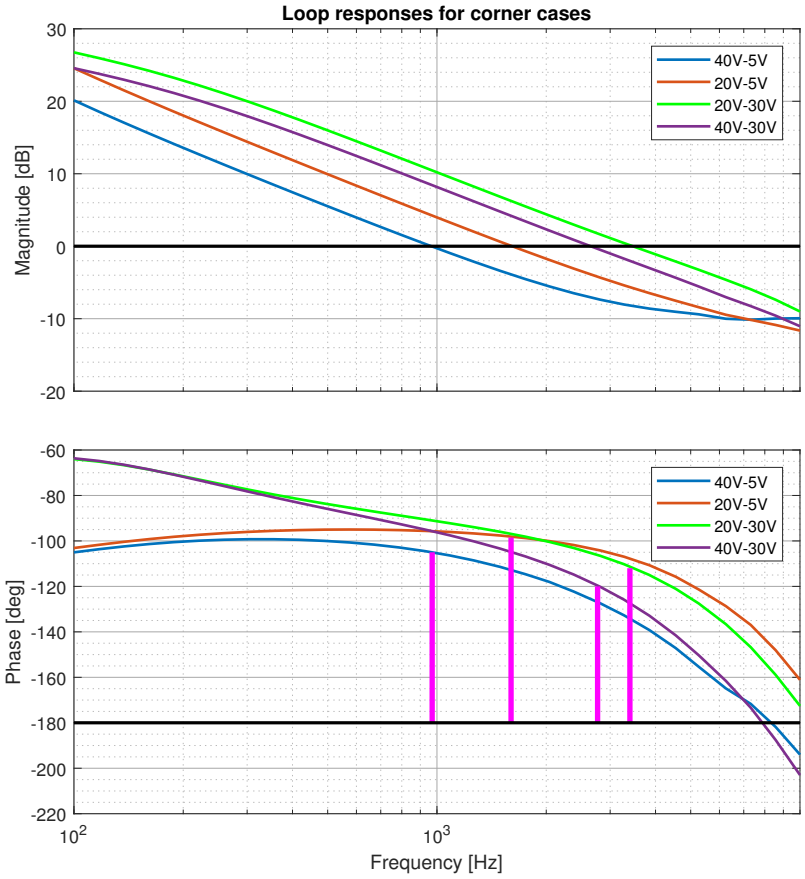


Figure 5.4: Loop response of converter in the 4 corner cases in the case of the PLECS setup in 5.3. The vertical magenta lines are phase margins

5.3 Closed Loop Performance

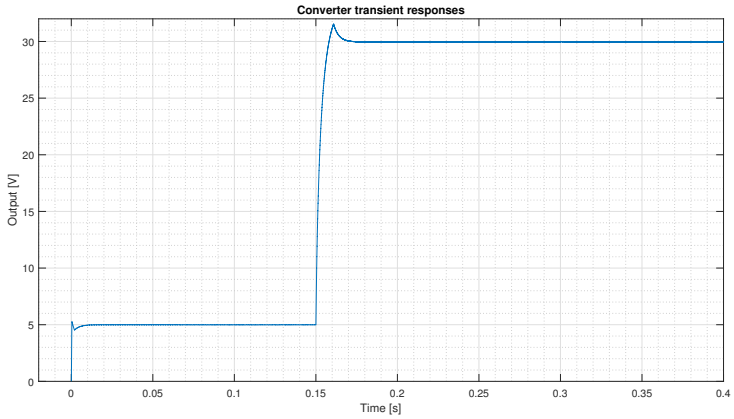


Figure 5.5: The converter's transient responses

In fig 5.5 the transient responses of the converter can be seen. At $t = 0$ the converter is turned on with a reference that should give 5V on the output. At $t = 0.15s$ the reference is stepped to 30V and at $t = 0.3s$ the load is stepped from 50% to 100%. As the figure shows the response is fast with a negligible steady state error, and the loadstep is barely detectable.

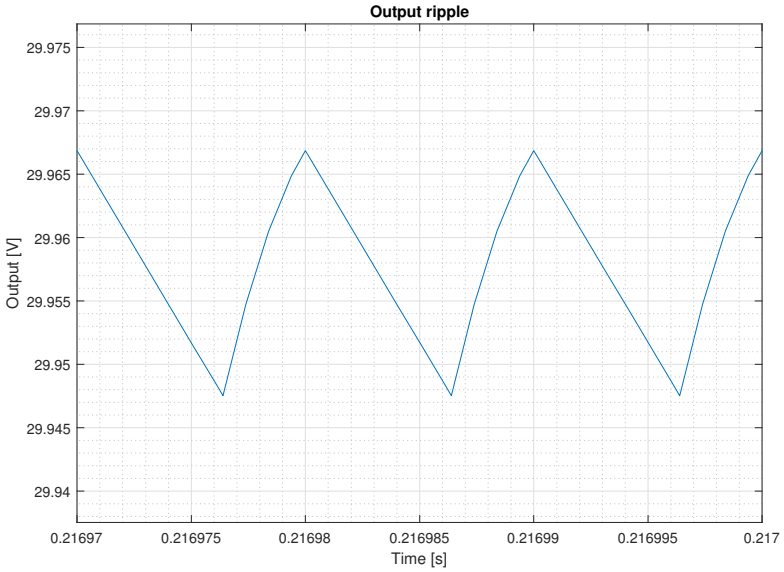


Figure 5.6: The steady state ripple at output

In Fig. 5.6 the output ripple with input of 40V and an output of $30\text{V}, 1\text{A}$ is seen. The peak to peak voltage is 20mV.

5.4 Implementation

5.4.1 Powering the active components

The control circuitry on the primary side is supplied with 18V from a linear regulator (TPS79801-Q1) which uses the input voltage as supply. As the current controller has a built in gate driver this will also be the voltage which will be used to switch the MOSFET. 18V is chosen as it gives a low ON-resistance.

The circuitry on the secondary side is powered by the same type of linear regulator as above, except that this is supplied by a tertiary winding in the transformer ($N_{tertiary} = 22$ turns). The tertiary winding is connected to a rectifying diode and a smoothing capacitor. The windings would not take up much space in the transformer window since almost no power is required for the control circuit and very thin wires can be used without significant winding loss. A tertiary winding is used to get high enough voltage, and a voltage regulator is used to keep the feedback gain independent of the output voltage. The linear regulator delivers a voltage of 8V from an input of 8.3V to 49.8V.

5.4.2 MOSFET - BSF450NE7NH3

This 75V, 15A rated Infineon Optimos MOSFET[8] is chosen as it has an excellent figure of merit (FOM). As the switching frequency here is rather low, emphasis is here on having a low R_{dson}, which is also quite good (45mΩ).

5.4.3 Optocoupler - 4N35-37

Isolation of the signal feedback to the current controller is obtained by using an optocoupler to transfer the control signals from the isolated output to the control circuit on the input side. This is found to have a current transfer ratio of $0.50mA/mA$.

5.4.4 Peak Current Controller - UC3842AD8TR

Current sensing

A current spike can happen on when switching in the flyback converter and since we're using peak current control such a spike would interfere with the control. A lowpass filter is therefore applied to the current sensing resistor. It is dimensioned such that the filter's time constant is equal to 5% of the switching period, as that is a rough estimate to the current spike we want to dampen.

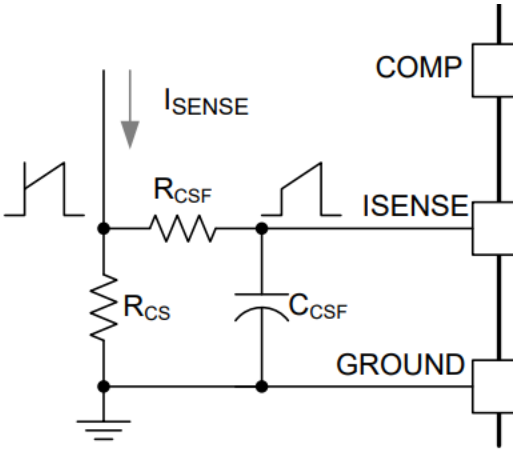


Figure 5.7: Low pass filter for current sensing[9]

Furthermore, the current sense resistor is selected to be $R_{sense} = 50\text{m}\Omega$ (called R_{cs} in Fig. 5.7). This low value is selected so that the losses are low and the peak current controller does not saturate. The filter components are set to be $R_{lp} = 10\text{k}\Omega$ and $C_{lp} = 50\text{pF}$ (called R_{csf} and R_{csf} in the figure).

Slope Compensation

Slope compensating is necessary as the duty cycle will go higher than 0.5. The compensating slope is set to $m = m_2 = 464\text{kA/s}$ which ensures no subharmonic oscillation. Here, m_2 is the falling slope of the inductor current transformed to the primary side.

$$m_2 = \frac{V_{out,max}}{L_s \cdot n} \tag{5.4}$$

This compensation is implemented as adding a slope to the voltage feedback (from the optocoupler). This is done by connecting a resistor from the "RT/CT" timing port of the controller. Fig. 5.8 show this circuit.

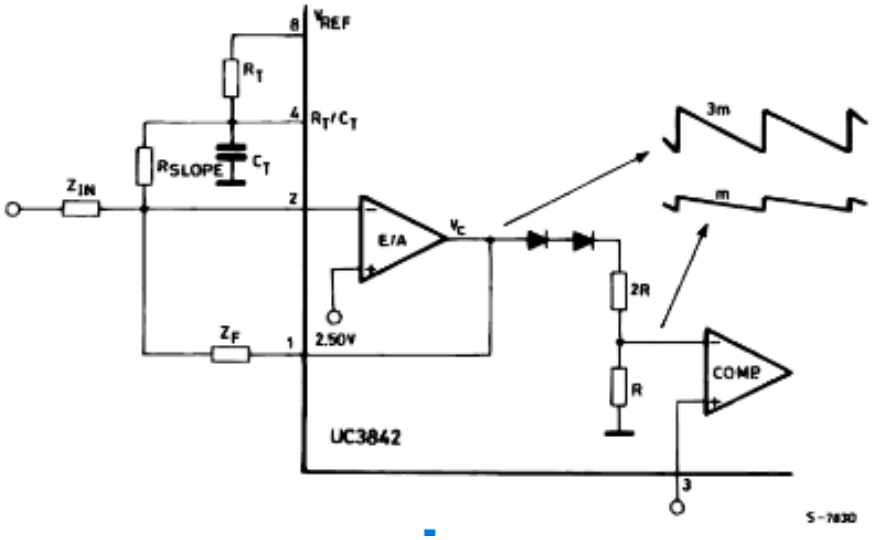


Figure 5.8: Compensating circuit[10]

The impedance Z_f and Z_{in} are set to $R_f = R_{in} = 50\text{k}\Omega$. This gives unity gain of the internal inverting amplifier. Now, R_{slope} is found[10]:

$$R_{slope} = \frac{2.2 \cdot m_v Z_f}{f_{sw}} = 24.3\text{k}\Omega \tag{5.5}$$

Here, m_v is the current compensating slope multiplied with the sense resistor, $m_v = R_{sense} \cdot m$.

Frequency of Operation

In order to achieve 100kHz operation of the switch, equation 5.6 must be satisfied.

$$f_{osc} = \frac{1.72}{R_T \cdot C_T} = 100\text{kHz} \tag{5.6}$$

Where R_T is kept much smaller than R_{slope} to keep the compensating ramp linear.[10] $R_T = 1\text{k}\Omega$ and $C_T = 17.2\text{nF}$ is chosen. When implementing, the value of C_T can be adjusted to get exactly the desired frequency.

Drive capabilities

The chosen MOSFET will draw an average gate current of $Q_g \cdot f_{sw}$. With a gate charge of maximum 10nC[8] the current becomes 1mA, which is smaller than the maximum drive capability of 200mA. Thus it is not required to have an external gate driver IC.

5.4.5 Over Current Limiter

The converter is designed such that the core should not saturate. Nevertheless, a protective circuit is added as the current is measured anyways. This is done with a op-amp that compares the measurement voltage to a voltage that corresponds to a current of 5A (twice the worst case peak current). If the current goes above this limit, the op-amps output goes high which enables an MOSFET which in turn forces the *COMP* pin to ground. This shuts down the current controller, until the current is below this threshold again.

5.5 Control Design Discussion

5.5.1 Sense Resistor

The small size of the current sense resistor makes the measured voltage susceptible to noise as the voltage level is low. It might become necessary to use a differential amplifier to reduce the influence of noise. Furthermore, simulations show that close to 0.2W is dissipated in this resistor in the worst case. This is below the common rating of 0.25W.

5.5.2 Results

The designed control scheme gives promising simulation results with a phase margin of 60 degrees for the worst case, zero steady state offset and a steady state ripple of 20mV.

5.5.3 Schematic

The final schematic of the converter is seen in fig. 6.1 in chapter 6.

6 | Circuit Diagram and Bill of Materials (CL, SK, BW & TK)

6.1 Bill of Materials

1 x TDK EPCOS ETD 29/16/10 N87 Transformer core

1 x TDK EPCOS ETD 29/16/10 Transformer coil former (magnetic axis horizontal)

2 x TDK EPCOS ETD 29/16/10 Transformer yoke

50 cm 30mm kapton tape

200 cm Von Roll 0317-0-1 grade 1, $\oslash = 1.18$mm Copper wire

100 cm Von Roll 0317-0-1 grade 1, $\oslash = 1.40$mm Copper wire

8 x 56µF, 50V Panasonic EEU-FM1H560, Electrolytic Capacitor

5 x 10µF, 100V TDK CGA9N3X7S2A106K230KB Ceramic Capacitor

3 x 1µF, 100V TDK C3216X7R2A105K160AA Ceramic Capacitor

2 x 2.2µH, Wurth 744316220 Power Inductor

1 x 3.3µH, Delevan SPD127R-332M Power Inductor

1 x 22µH, Wurth 744750460220 Power Inductor

2 x 15µH, SC63LCB-150 Signal Inductor

1 x 17µH, Sumida CLS4D23B-170NC Signal Inductor

2 x TPS79801-Q1 Linear Regulators

1 x 4N35(Short) Optocoupler

1 x TLVH431IDBZT Shunt Regulator

1 x UC3842AD8TR Current Mode PWM Controller

1 x IN4741A Zener diode

1 x IN4148W Diode

1 x CDBB5100 Diode

1 x LM293D Operational Amplifier

1 x 2N7002 NMOS

1 x FDD8444_F085TR-ND NMOS

1 x BSF450NE7NH3 Power NMOS

1 x NKK G3T12AH-R SPDT signal switch

1 x 300k Rotary Potentiometer

4 x 4mm Banana Jack Connector

4 x 200mΩ, 125mW Resistors

The rest of the components are generic components (0805 SMD capacitors and resistors) which are available in most electronics labs.

6.2 Circuit Diagram

See the following page for a full size schematic of the converter.

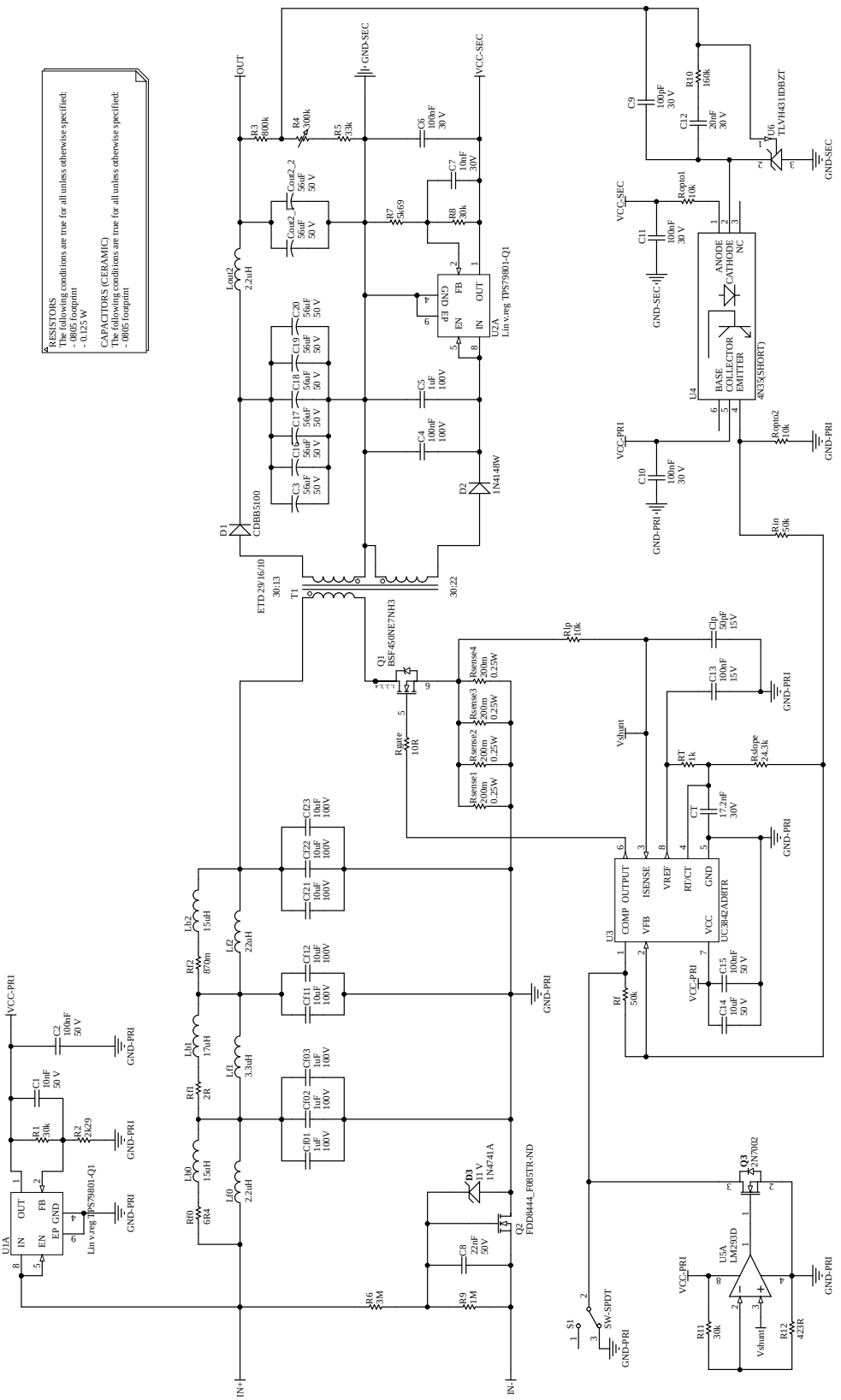


Figure 6.1: Final circuit schematic

7 | Performance Analysis (CL, SK & TK)

An estimate of the converter efficiency is found by using a combination of calculated losses and simulated losses. The transformer losses calculated for the worst case operating point in the magnetic section is used together with a PLECS simulation. The simulation accounts for the losses in the filters, the MOSFET and most of the logic. The following formulas show how the efficiency are estimated.

$$\eta = \frac{P_{out}}{P_{in}}$$

$$\eta_{estimated} = \frac{P_{out\,simulated}}{P_{in\,simulated} + P_{transformer\,loss\,calculated} + P_{extra\,loss\,simulated}} \tag{7.1}$$

Where $P_{transformer\,loss\,calculated}$ is the sum of core and winding losses, $P_{extra\,loss\,simulated}$ represent the logic and switching losses. The switching losses are approximated by simulating a switching of the capacitances C_{iss} and C_{oss} from 0V to 18V and V_{in} respectively.
Figure 7.1 shows a part the simulation setup. For the entire simulation circuit and values of component parasitics, see appendix C.

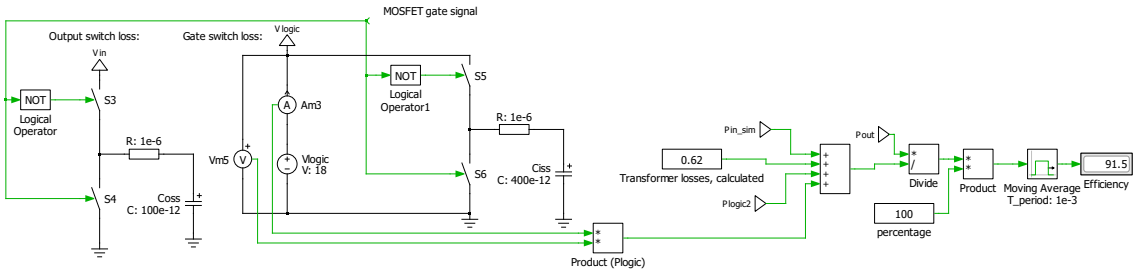


Figure 7.1: Efficiency estimation in PLECS. Based on eq. 7.1.

This simulation results in an estimated efficiency of $\eta_{estimated} = 92\%$ for the case of $V_{in} = 20$V, $V_{out} = 30$V and $I_{out} = 1$A.

8 | Specification Comparison (CL, SK & TK)

Here, the final converter design is tested with intrinsic parameters (ESR of capacitors, DCR of inductors etc.). Inrush current and input current harmonics are not tested again, as it seems unlikely that the damping of the input current degrades with extra resistances.
The same simulation setup is used as in the performance analysis (schematic in appendix C). A transient analysis is performed in PLECS to see steady state ripples and responses of load steps.

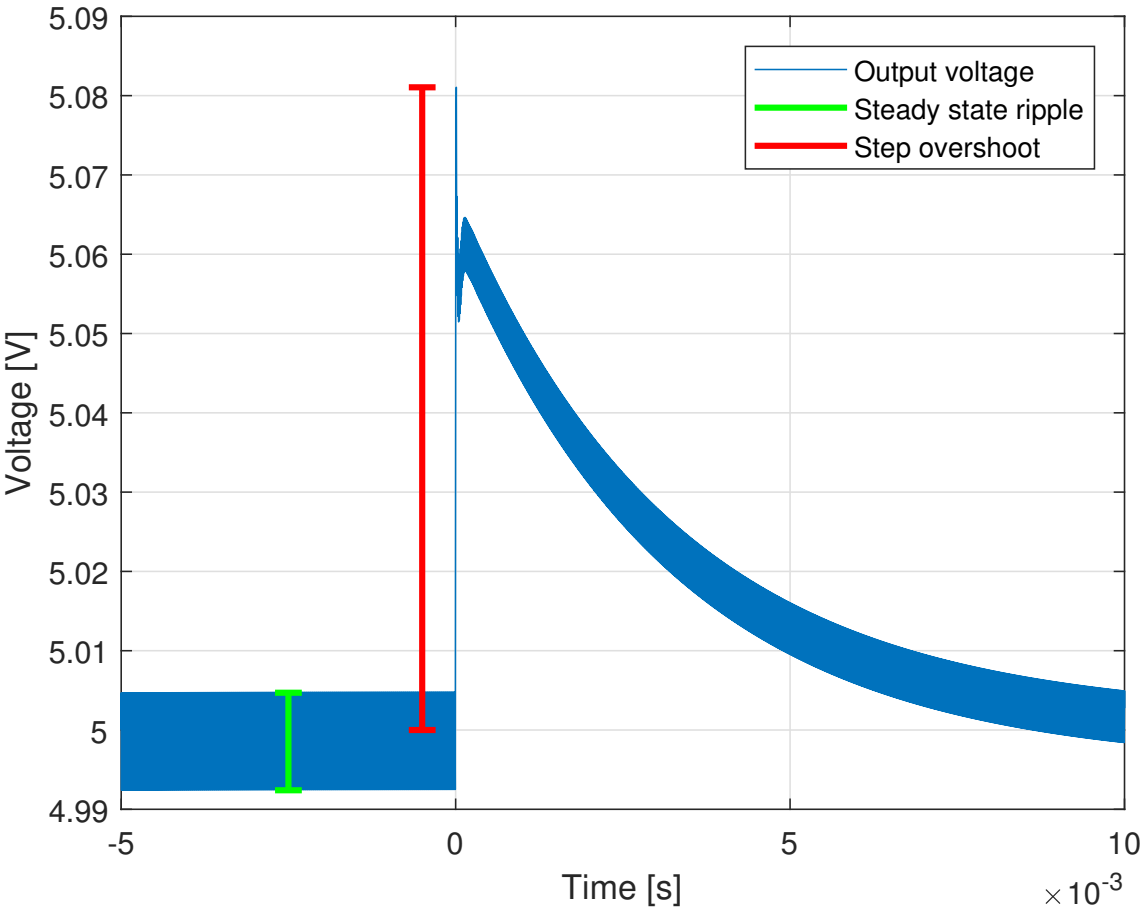


Figure 8.1: Output voltage during load step at 5V

Steady state ripple of 12.7mV, step overshoot of 81.1mV (1.62%).

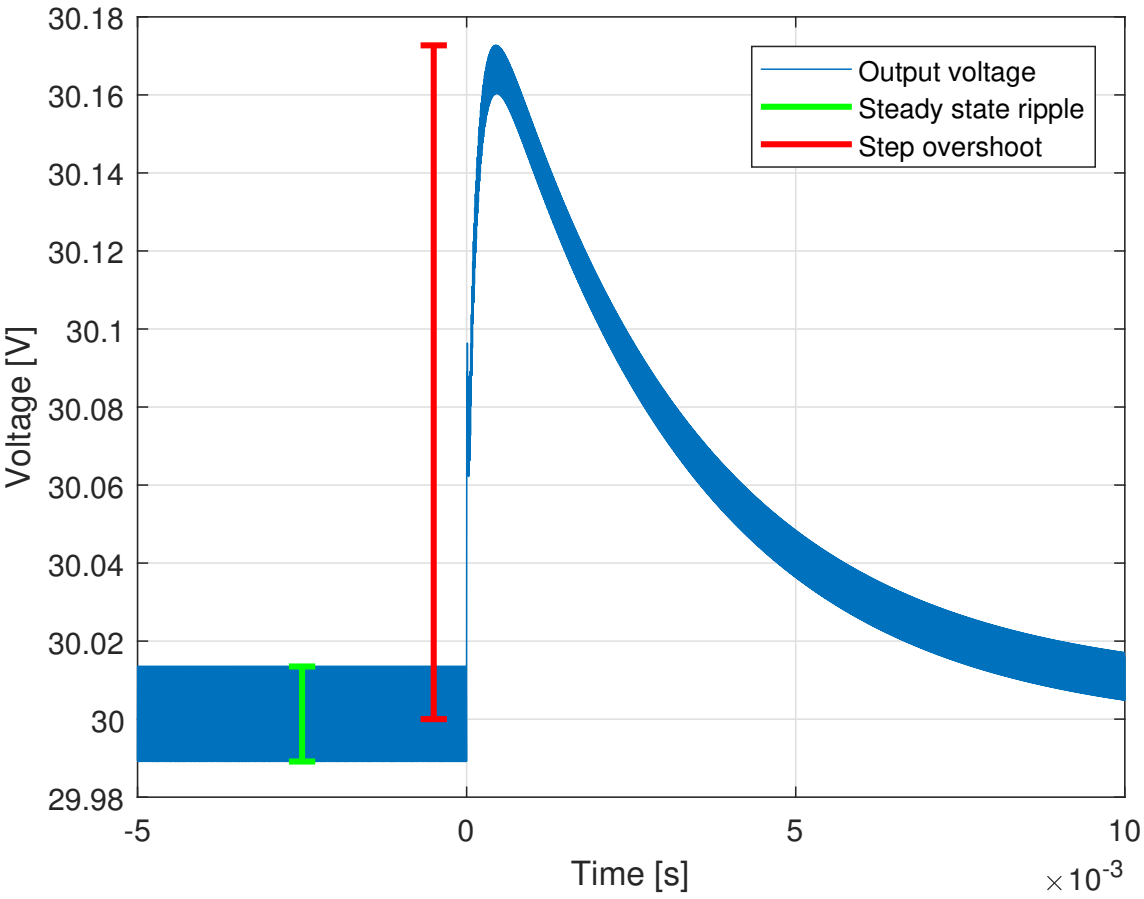


Figure 8.2: Output voltage during load step at 30V

Steady state ripple of 24.4mV, step overshoot of 172mV (0.573%).

	Condition	Minimum	Maximum	Achieved (detailed simulation)
V_{in}	-	20 V	40 V	✓
V_{out}	-	5 V	30 V	✓
I_{out}	-	-	1 A	✓
$\Delta V_{out_{max}}$	Steady state	-	50mV	24.4mV
$\Delta V_{out_{max}}$	Load step	-	3 % of V_{out}	1.62%

Table 8.1: Converter Results.

9 | Discussion (CL, SK & TK)

Several assumptions and approximations are done during this work. Some of them might have been less valid than initially expected. This might not give any consequences as all design choices include safety margins. For example: In the filter design chapter, an extra filter was added at the output of the converter. When doing this it was assumed that this did not change the converter's "input impedance" Z_D significantly. In reality it is probably lowered a bit. But as the stability margins (Middlebrook) are large it will probably not cause any issues.

Some design choices could also have been done differently. An differential amplifier can be added to the current sensing resistor for improved noise rejection. One might also argue that a smaller magnetic core with more turns and larger airgap might be wiser although the calculations here indicate that this would lower the efficiency.

One important thing to consider is if the circuit is able to start when the secondary side logic is unpowered. When the secondary side is unpowered, no current runs through the optocoupler and thus the voltage is 0 at the VFB pin of the controller IC. This will probably cause this IC to start switcing the FET as the VFB is connected to the negative input of an internal amplifier.

10 | Conclusion (CL, SK & TK)

The converter has an estimated efficiency of 92% at maximum load, which is promising. The transient, stability and steady state analyses have been thorough, and the analyses has considered intrinsic resistances for the relevant components. Furthermore, parasitic MOSFET capacitances are considered to account for switching losses at the gate and drain. This suggest that the design is realizable with a performance close to the estimated one.

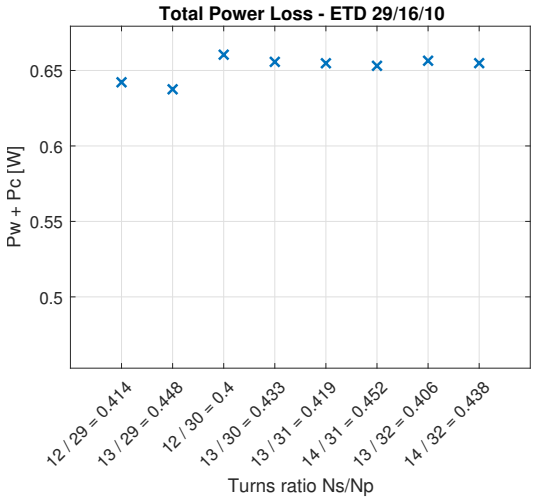
A | Magnetic Design: ETD-Cores

The following contains considerations of using ETD-cores for the transformer design. A MATLAB script was used to conduct a comprehensive investigation of all the available ETD-cores up to size 39/20/13 and related coil formers listed in [1] as well as all the possible wire diameters in [2] taking into account the insulation of the wires. The procedure for determining whether or not a certain configuration would be practically realizable was identical to the one described in Chapter 3. The conditions in Table A.1 set the limits of the design parameters.

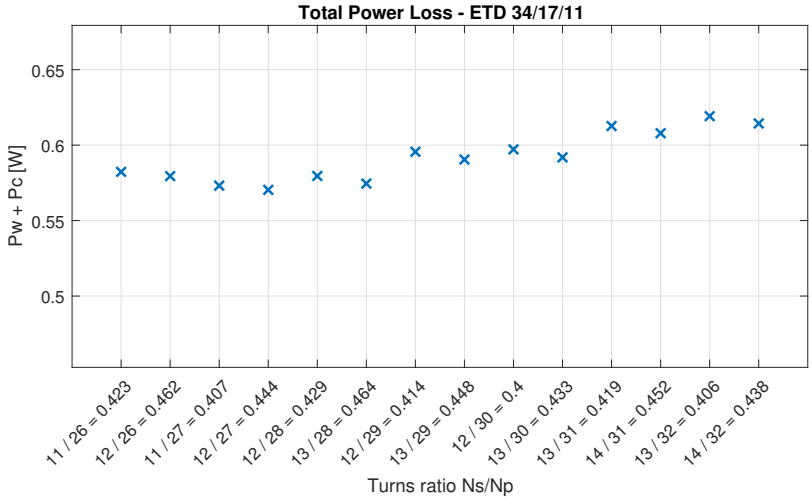
Primary layers	1
Secondary layers	1
Max primary windings	32
Air gap (each leg)	100 µm
Ideal turns ratio	0.433
Max turns ratio deviation	0.033

Table A.1: Conditions for determination of configurations in Fig. A.1.

The results of this analysis are shown in Fig. A.1.



(a)



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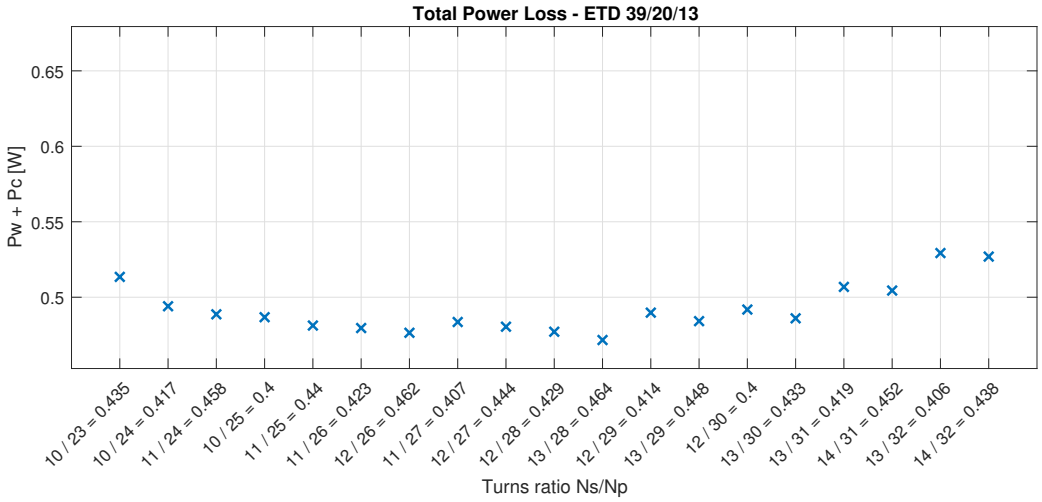


(c)

Figure A.1: Realizable E-core configurations with 1 primary layer.

B | Magnetic Design: E-Cores

The following contains considerations of using E-cores for the transformer design. A MATLAB script was used to conduct a comprehensive investigation of all the available E-cores smaller up to size 36/18/11 and related coil formers listed in [1] as well as all the possible wire diameters in [2] taking into account the insulation of the wires. The procedure for determining whether or not a certain configuration would be practically realizable was identical to the one described for ETD-cores in Chapter 3. However, the script was modified to take into account the square coil former center leg when calculating winding lengths. Furthermore, the calculations were done using both 1 and 2 primary layers with the condition of Table B.1 and Table B.2 setting the limits of the design parameters.

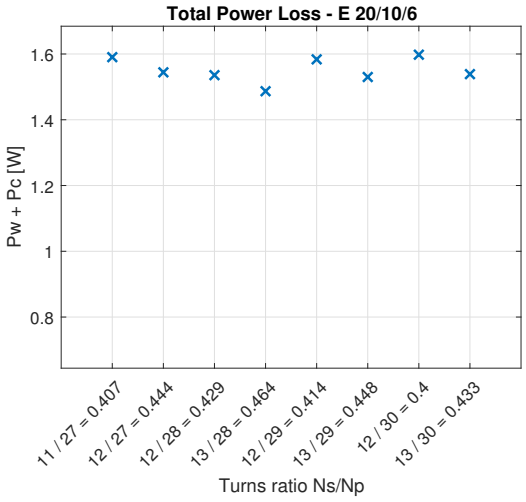
Primary layers	1
Secondary layers	1
Max primary windings	30
Air gap (each leg)	100 µm
Ideal turns ratio	0.433
Max turns ratio deviation	0.033

Table B.1: Conditions for determination of configurations in Fig. B.1.

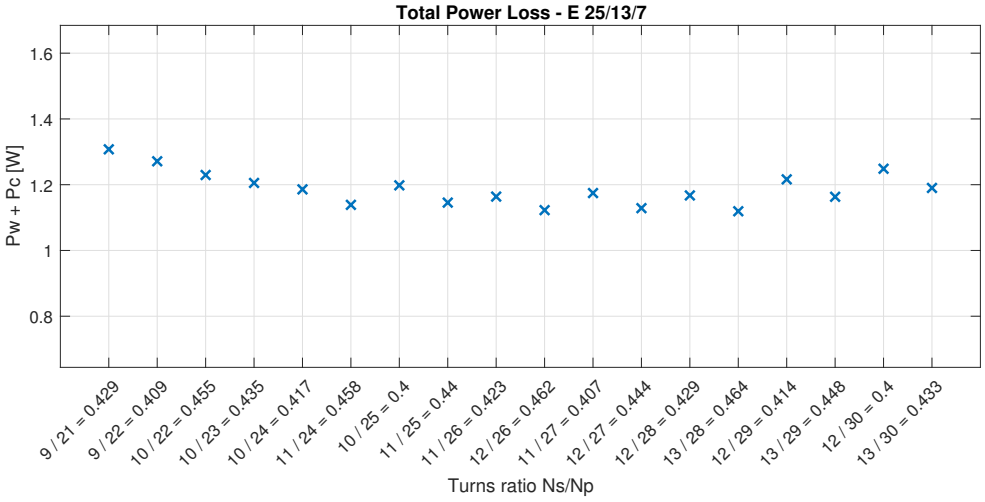
Primary layers	2
Secondary layers	1
Max primary windings	30
Air gap (each leg)	100 µm
Ideal turns ratio	0.433
Max turns ratio deviation	0.033

Table B.2: Conditions for determination of configurations in Fig. B.2.

The results of these analyses are shown in Fig. B.1 and Fig. B.2. This figure contains the possible solutions for five cores, which is less than the number of E-cores in the EPCOS Databook, but the cores not shown have no realizable solutions that fits the limiting parameters of Table B.1 and Table B.2.



(a)



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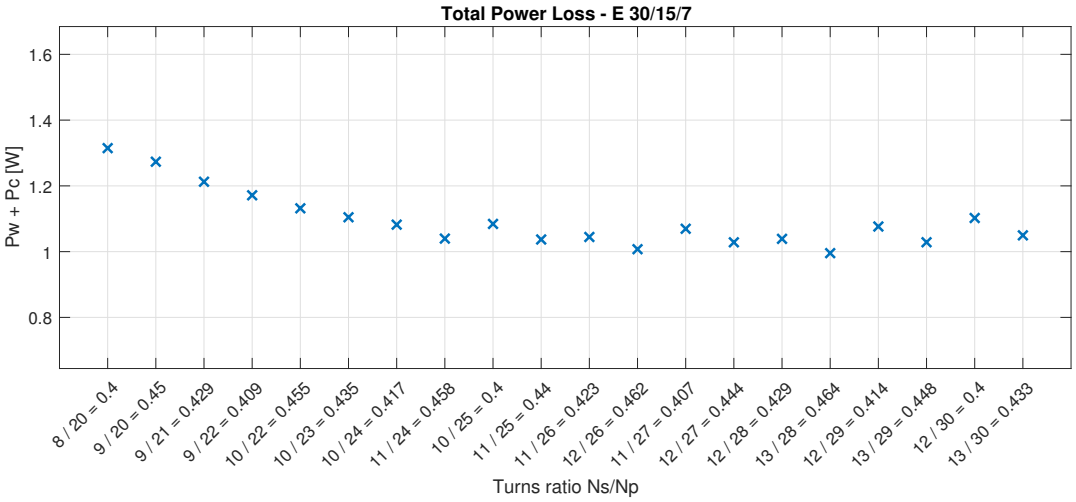
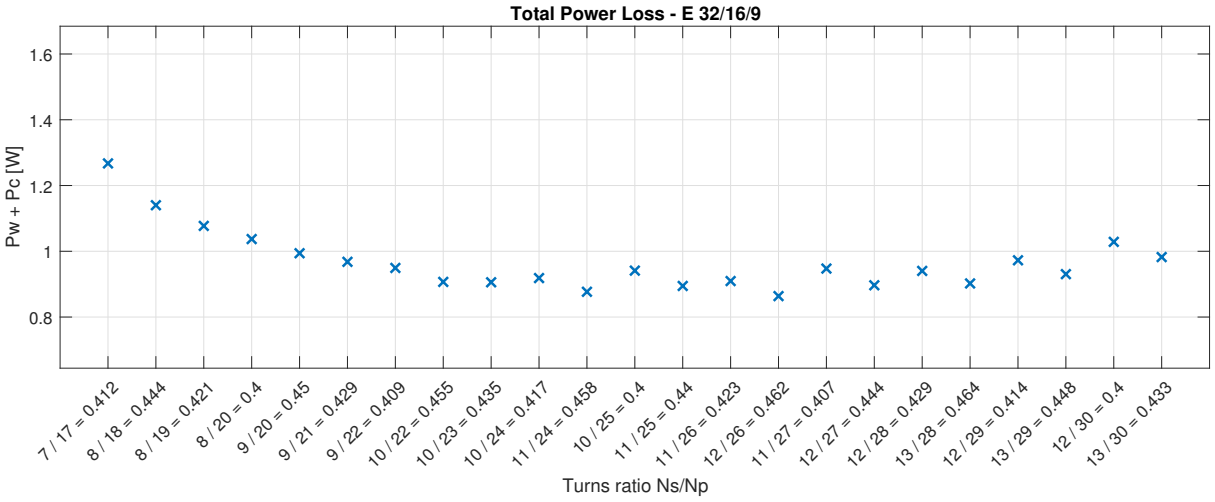
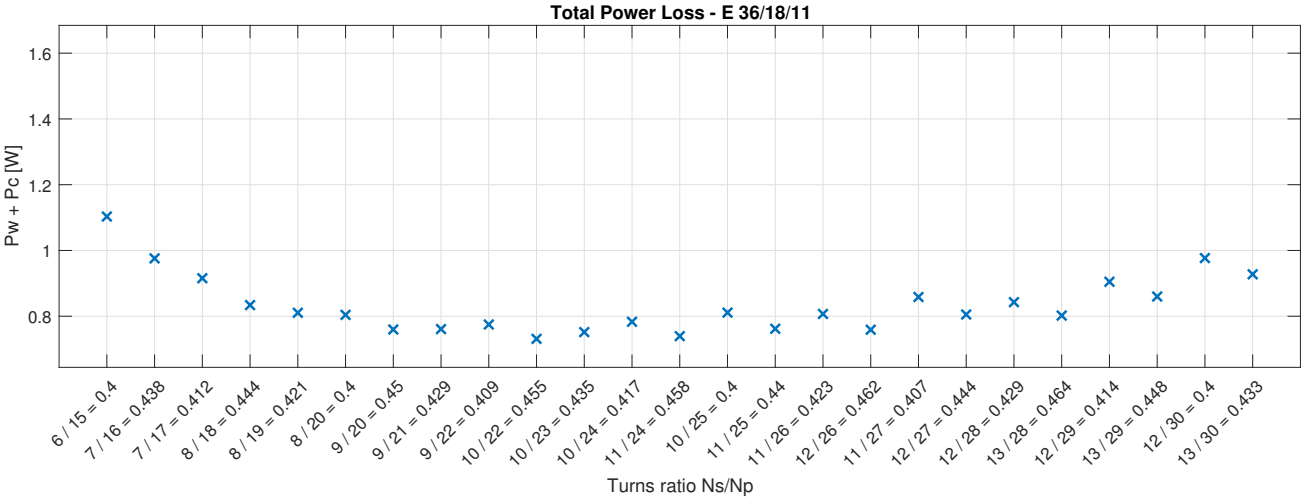


(c)

Figure B.1: Realizable E-core configurations with 1 primary layer.

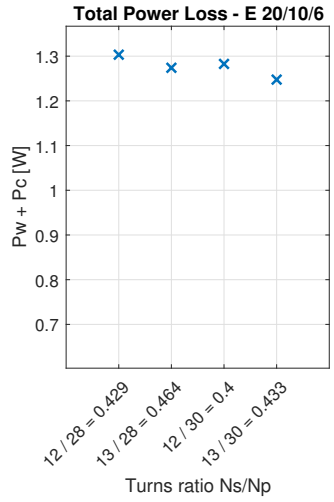


(d)

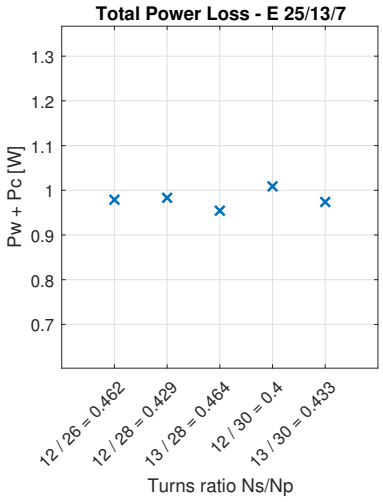


(e)

Figure B.1: Realizable E-core configurations with 1 primary layer.



(a)



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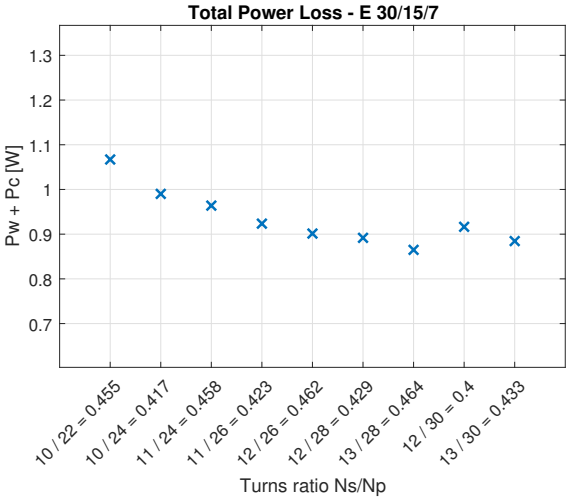

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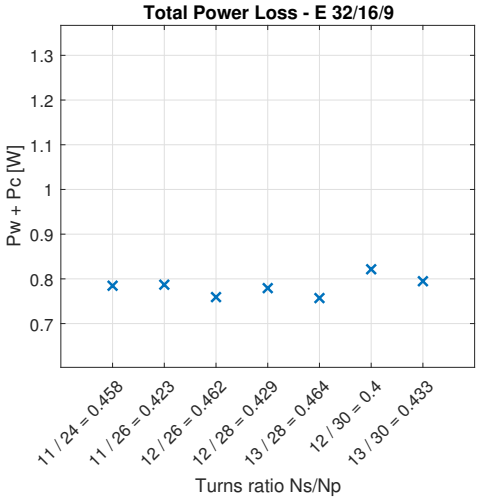

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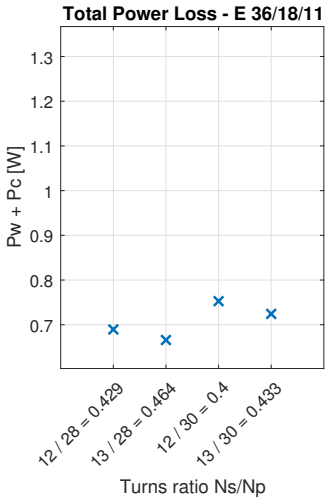

(e)

Figure B.2: Realizable E-core configurations with 2 primary layers.

C | Efficiency Simulation Setup

C.1 Component Parasitic Parameters

The following parameters are found in the components datasheets.

C.1.1 FET

$RDSON = 37.5\text{m}\Omega$ $Ciss = 400\text{pF}$ $Coss = 100\text{pF}$ Simulating Ciss and Coss.

C.1.2 Output Diode

CDBB5100-HF
$V_f = 0.75\text{V}$.
Probably smaller than this.

C.1.3 Output Capacitor

$|Z|_100k = 22\text{m}\Omega$
Dissipation factor: $tan(\delta) = 0.10$@120Hz
$$ESR = \frac{0.10}{2\pi f_{datasheet} C_{out}} = \frac{0.10}{2\pi \cdot 120 \cdot 330 \cdot 10^{-6}}\Omega = 0.40\Omega$$
$$ESR_combined = \frac{ESR}{6} = 67\text{m}\Omega$$

C.1.4 Input Filter

DC resistance for three of the filter inductances. These are the three which have the most current flowing through them. $DCR_{Lf0} = 11.3\text{m}\Omega$
$DCR_{Lf1} = 18\text{m}\Omega$
$DCR_{Lf2} = 16\text{m}\Omega$

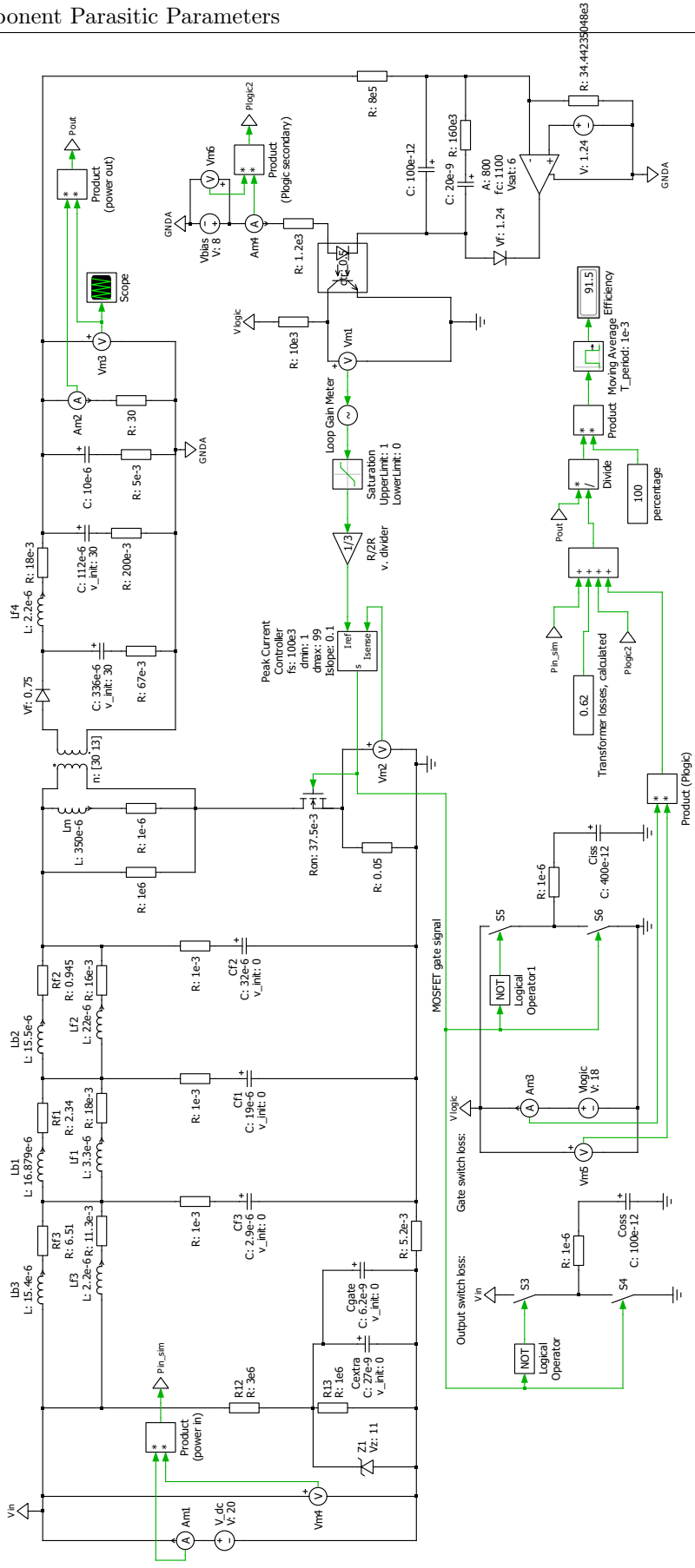

Figure C.1: Complete circuit schematic for simulating efficiency, ripples and load steps