DTU Electrical Engineering
Department of Electrical Engineering

Isolated 45W Lab Supply

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1 Specifications

Isolated 100 kHz SMPS Flyback topology.

Input voltage:	20-40 V
Input current:	Inrush $\leq$ *ETSI EN 300132-2*
Output Voltage:	Variable 5-30 V
	Steady state ripple $\leq$ 190 mV_{pp}
	50% load step $\rightarrow$ 6.7% overshoot
Output current:	At least 1 A across voltage range

2 Key Features

- Peak efficiency of 88.4 %
- Fine and coarse adjustment of output voltage
- Maximum 45 °C temperature rise
- Complete isolated operation from single supply
- Current mode control
- Rapid load change response

3 Implementation

The converter was implemented on a Manhattan style board as shown in Fig. 1 with an *ETD 29/16/10* coupled inductor.

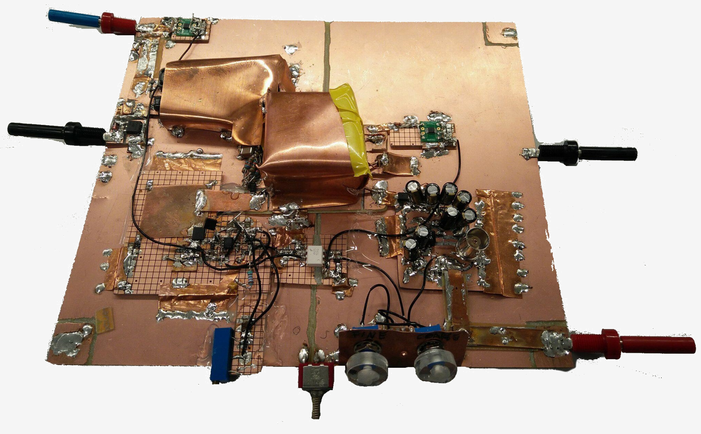
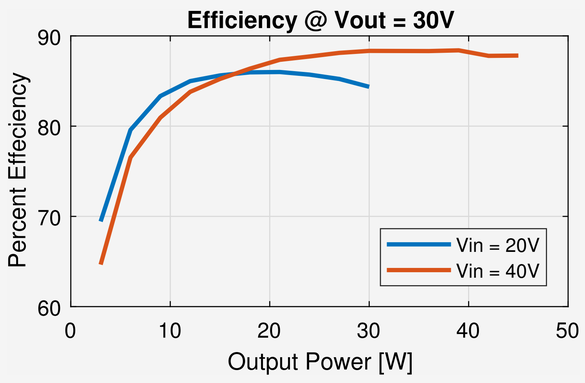


Figure 1: Implemented Flyback

Copper foil was applied as an EMI shield. The result was a drastic reduction in measurement and feedback noise.
The control voltages are supplied from linear regulators. The secondary side regulator gets it voltage from a tertiary winding on the transformer (8.3V – 50V).

4 Experimental Results

Full load operation is achievable for the entire output voltage range. Total system efficiency is shown in Fig. 4.



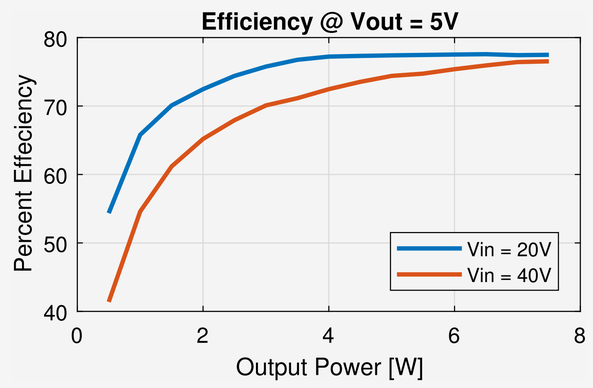


Figure 2: Converter efficiency.

The hottest component was the output diode (70 °C at max. load). The FET never increased more than 12 °C above ambient.

Steady State Ripple The steady state output voltage ripple is highly dependent on the load current. Maximum ripple was measured at 190 mV. Typical voltage ripple is shown in Fig. 3.

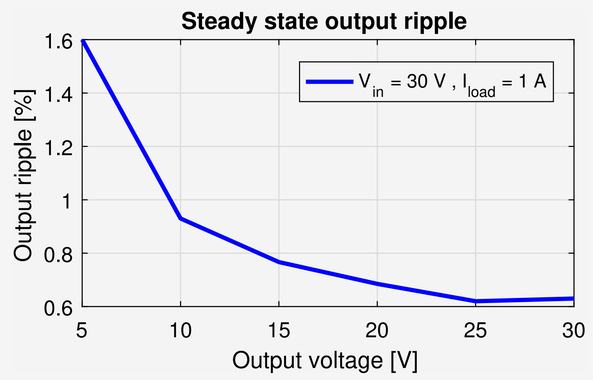


Figure 3: Output voltage ripple

Inrush Current Limiter An inrush limiting circuit was implemented in order to reduce the current spike caused by initial charging of the converter's capacitors. The input current spike is reduced by a factor of more than 18, as seen in Fig. 4.

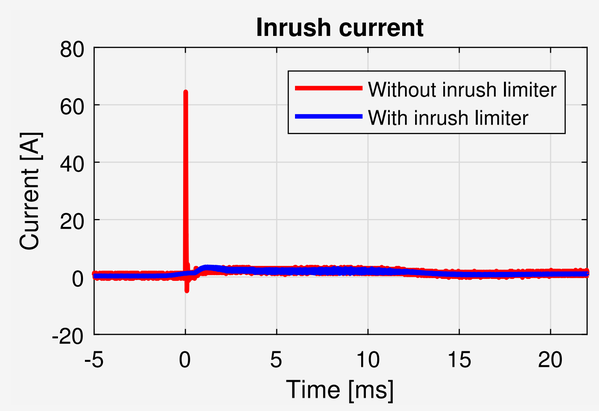


Figure 4: Inrush current, $V_{in} = 40V$

Load Step The response of the control loop was tested with a load step from 1 A to 0.5 A during a 30 μs transient.

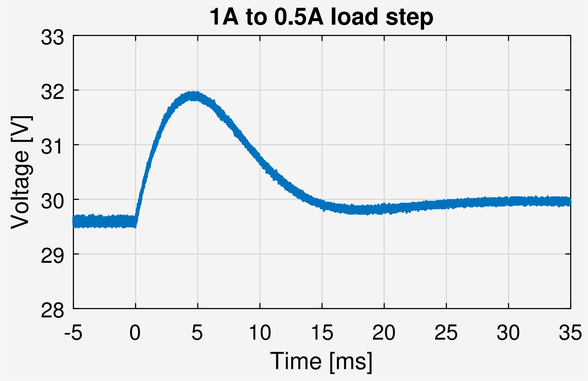


Figure 5: Load step, $V_{out} = 30V$

The results was an overshoot of 6.7 %. This can be reduced by adding more electrolytic capacitors in the output filter.

Conducted EMI A 6th order input filter was designed to attenuate the noise current according to CISPR-13 requirements. LISN tests in the EMC chamber was performed.

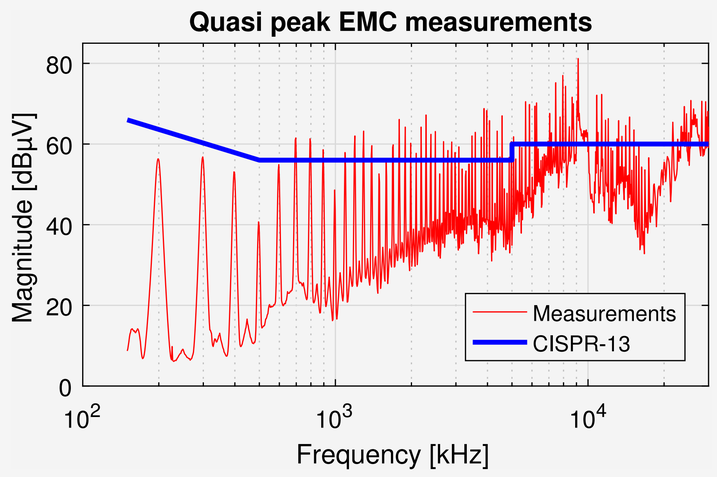


Figure 6: Input current harmonics

The reason that the noise is not attenuated properly is most likely due to the intrinsic inductance in the long ground paths and frequency dependent component variations.

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