Specification and Simulation of Digital Systems

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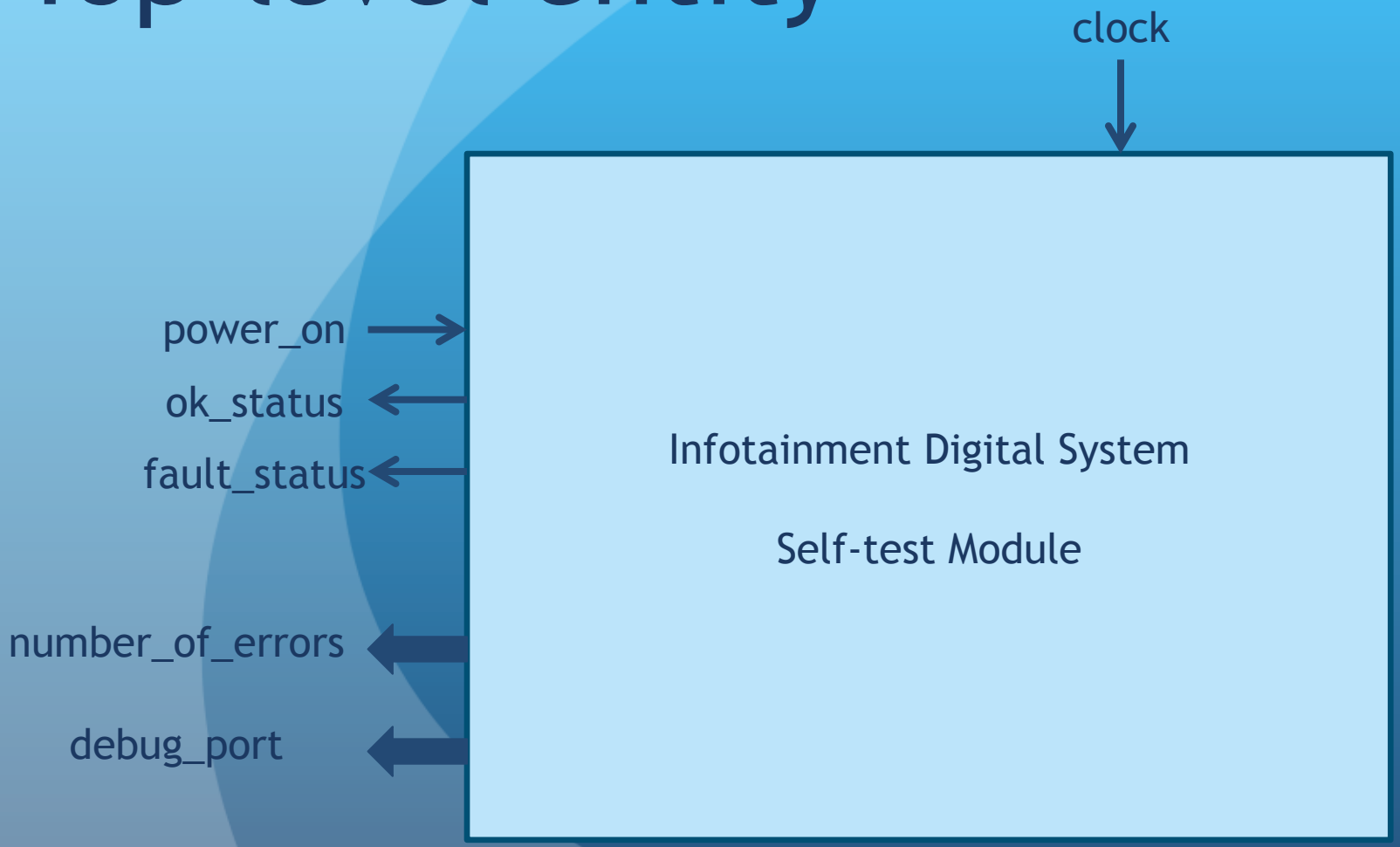
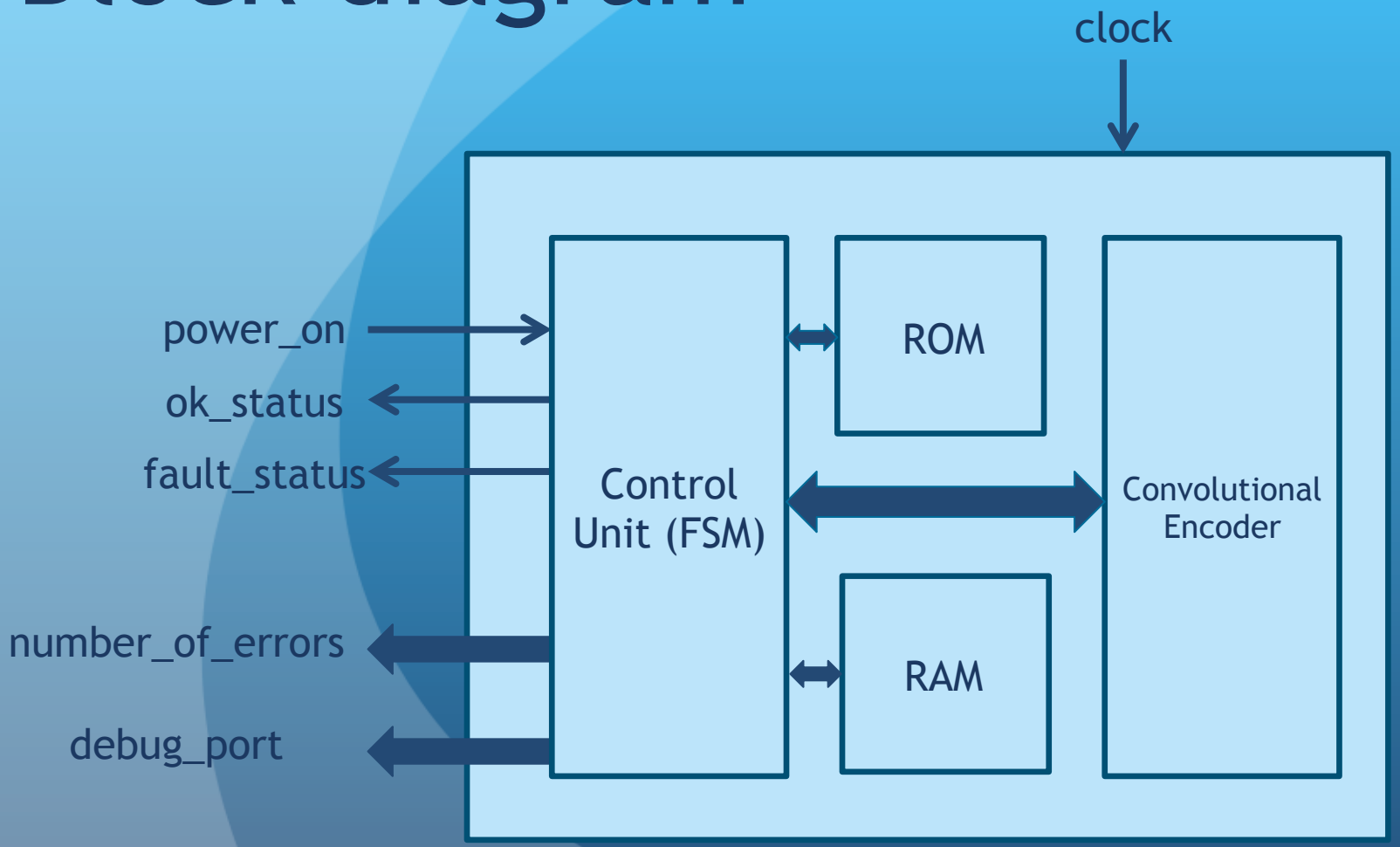
Overview

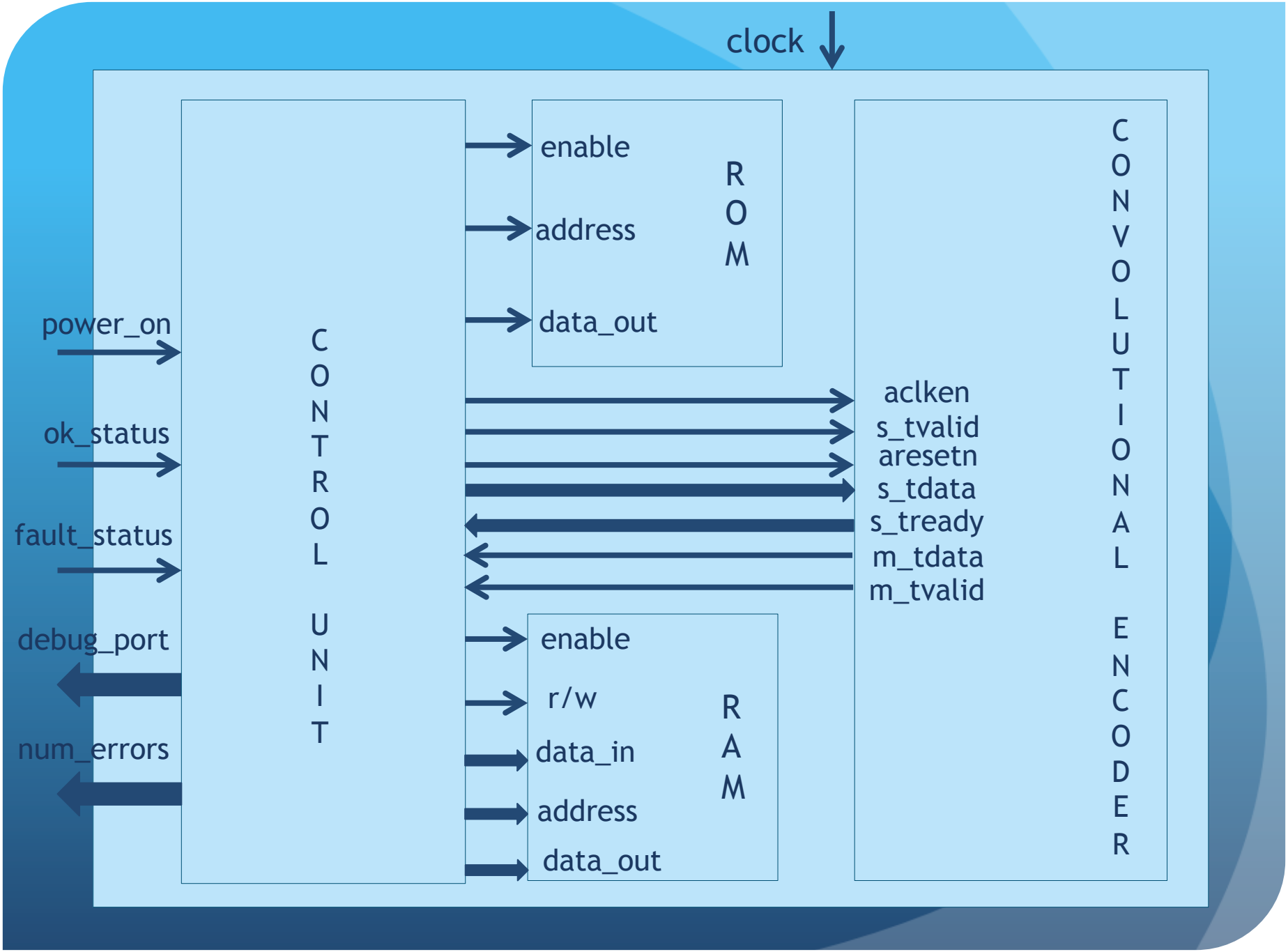
- Design and implementation of a Self Test Module based on assigned specifications
- Design details: functional entities and choice of patterns
- Timing behaviour
- Simulation of the overall system

Top-level entity



Block diagram



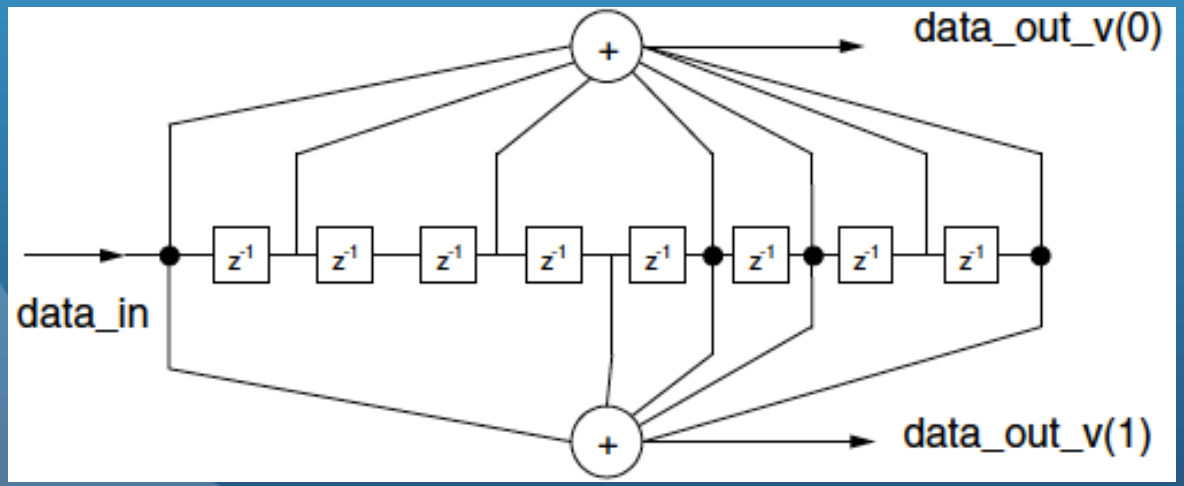

clock
CONTROL UNIT
power_on
ok_status
fault_status
debug_port
num_errors
ROM
enable
address
data_out
RAM
enable
r/w
data_in
address
data_out
CONVOLUTIONAL ENCODER
aclken
s_tvalid
aresetn
s_tdata
s_tready
m_tdata
m_tvalid

Convolutional Encoder

The LogiCORE IP Convolutional Encoder v8.0 is an 8-bit SIPO shift register: the incoming data is brought into the register one bit at a time; the output bits are generated by a logic XOR of some bits from the register.

The bits to be XOR'd are selected by these convolution codes:

- 101110001
- 111101011
- 010011101

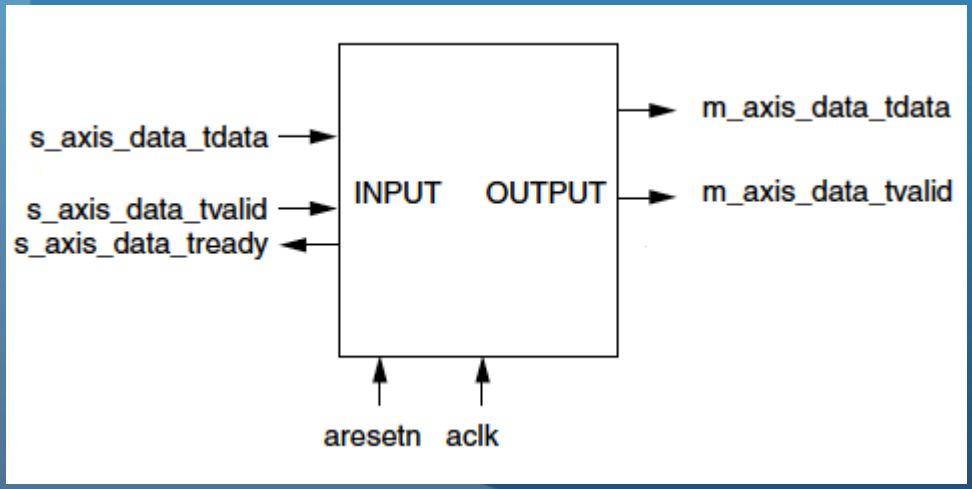


Core interface

The s_axis_data_tdata is on 8 bits, with 7 padding bits and the least significant bit defined by the user.

The m_axis_data_tdata is on 8 bits, with 5 padding bits and the least 3 significant bits produced by the core.

Finally, the core constraint lenght is equal to 9 (register width + 1).



Input patterns

- How many? 2^{14} (16384) input patterns have been chosen for testing
- Why so much? Because 2^{14} is the maximum number of stimuli that fulfills the assigned timing requirements
- What kind of patterns? 8-bit data words with 7 zeros and a randomly generated least significant bit

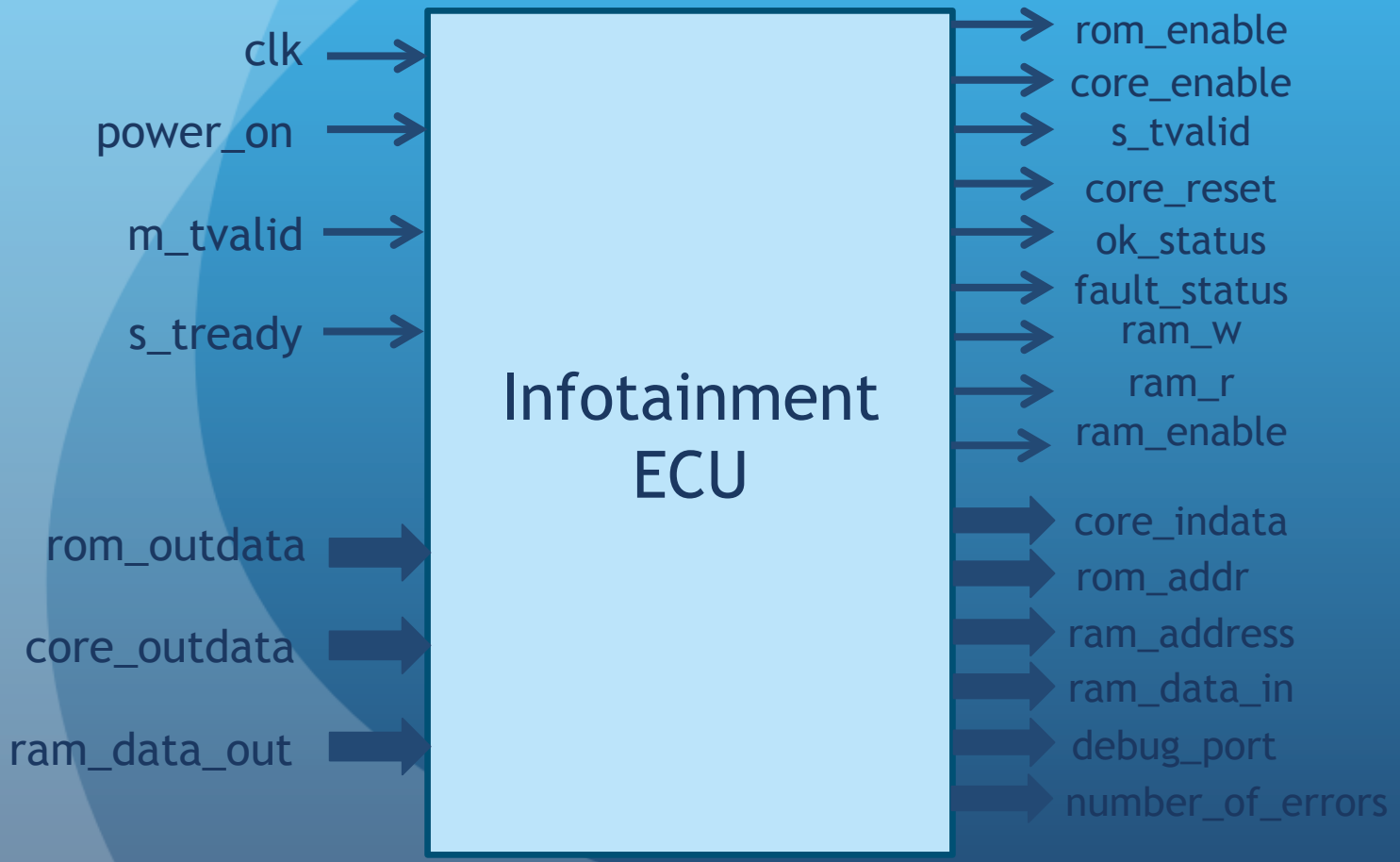
Memories

- One synchronous single port RAM
- One synchronous single port ROM reading the data directly from a .txt file

RAM, ROM

- The ROM is divided into a lower half containing the input patterns to be sent to the core and an upper (golden) half containing the expected results (in the faulted simulation this half has been modified voluntarily with incorrect results)
- It's made up of 2^{15} (32768) 8-bit words
- The RAM is made up of 2^{14} (16384) 8-bit words and contains only erroneous results from the core (if any)

Control Unit



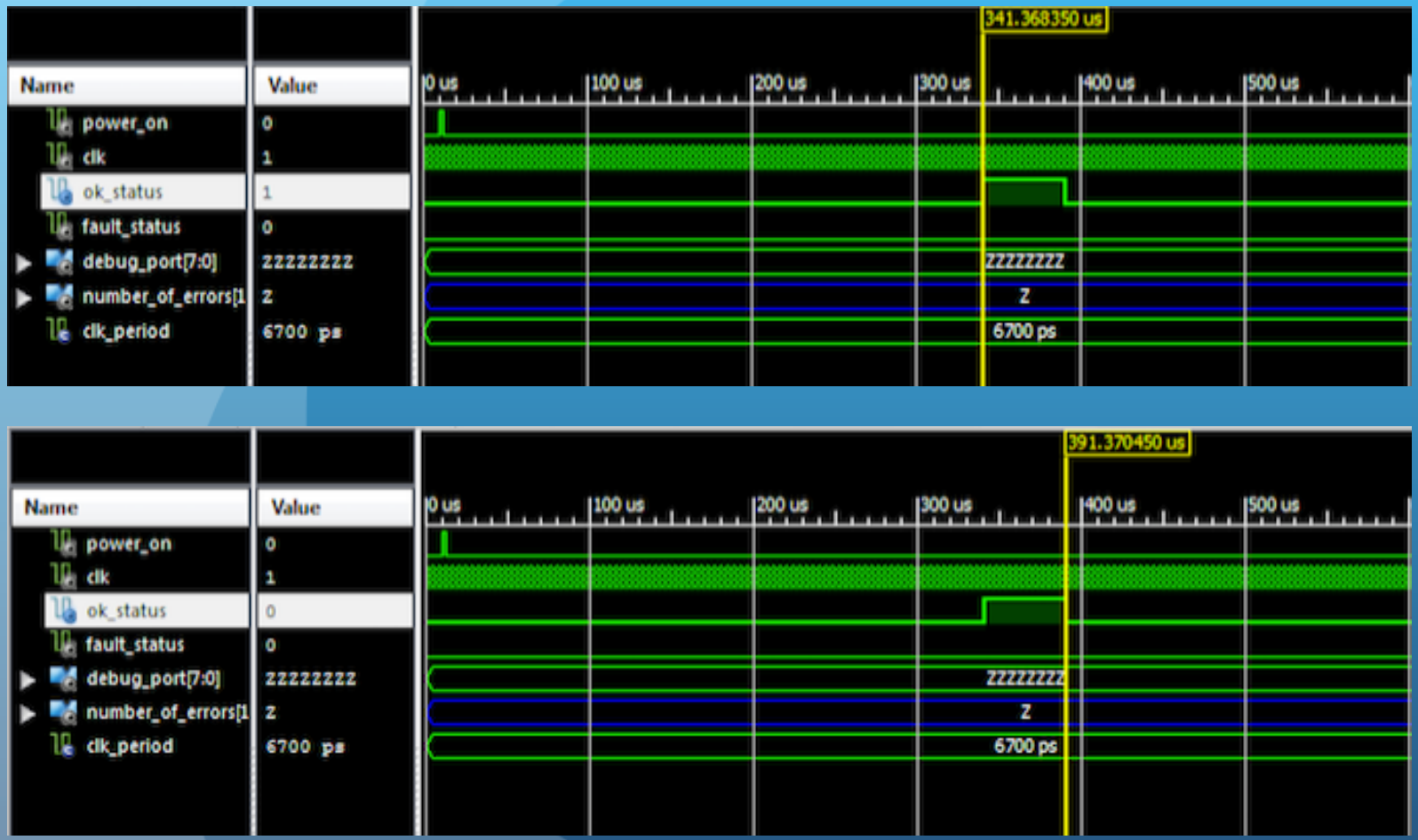
Control Unit

- It is a FSM with two processes: state_proc and func_proc
- It is made of 14 states
- An 8-bit data word is taken from the first half of the ROM and is fed to the core; then, the core output is compared with the corresponding result stored in the second half of the ROM; in case of a mismatch, the erroneous result is stored into the RAM
- Two possible scenarios:
  - no errors (ok status)
  - at least one error (fault status)

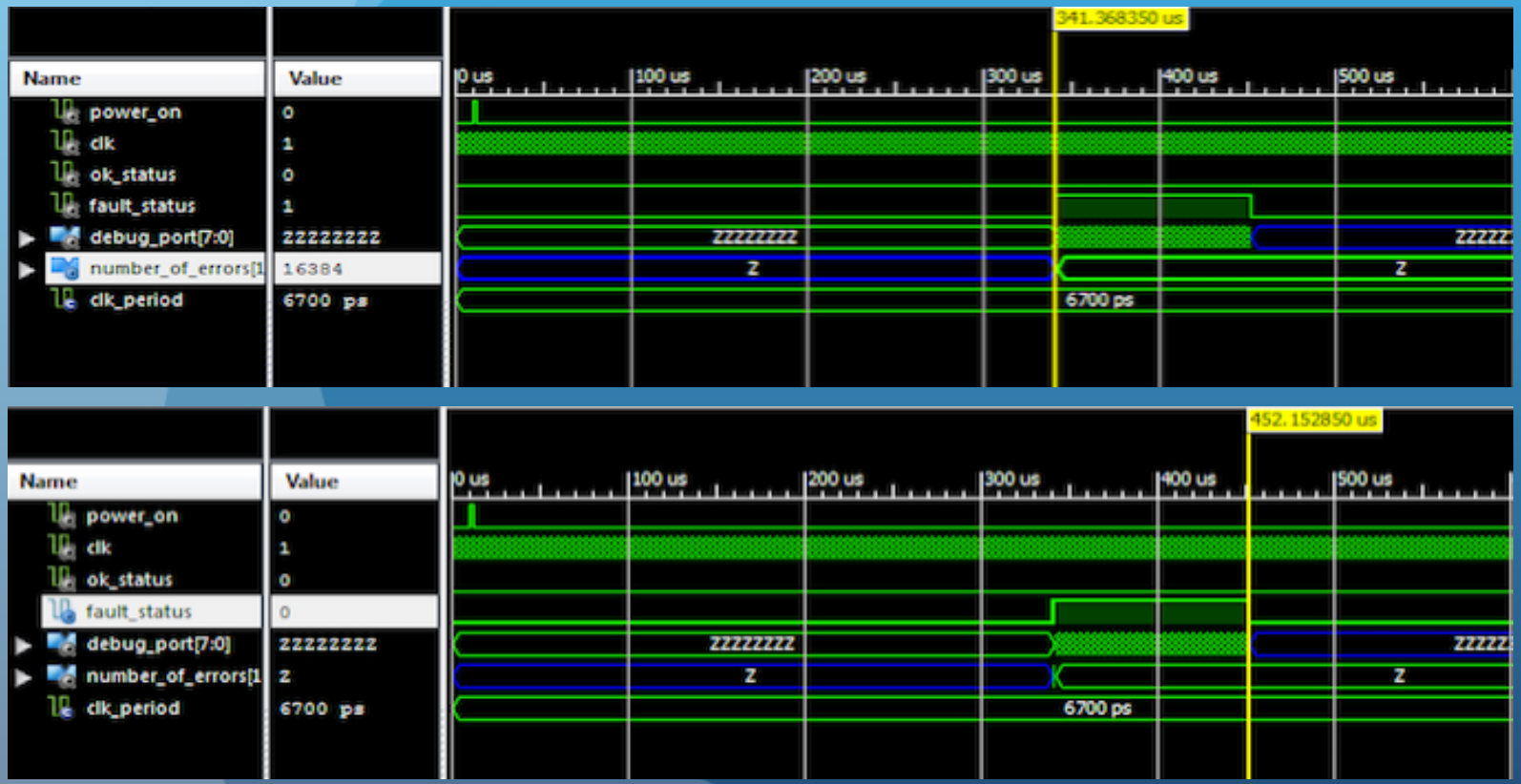
Timing behaviour

- With a 150 MHz clock signal, a 6.67 ns clock period has been selected in the testbench
- The power_on signal is active for 2 μs
- The test is successfully performed within 500 μs

- If there isn't any erroneous result, the ok_status signal remains high for 50 μs



- If there is at least one erroneous result, the fault_status signal remains active until all the debug information are transmitted on the output:
  - Numbers of erroneous results: 1 µs
  - Erroneous results: pattern dependent



Simulation of the overall system

Let’s see how it works!