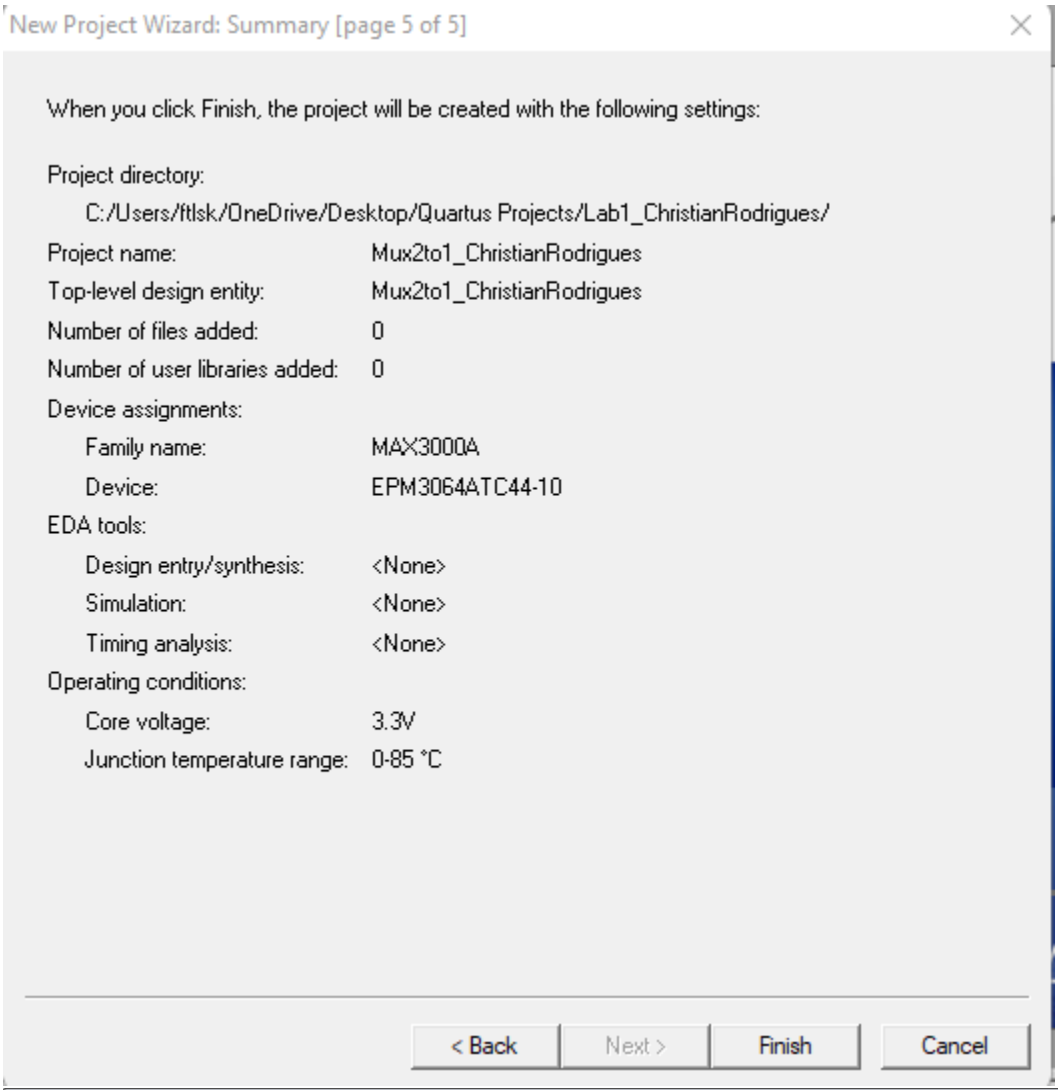
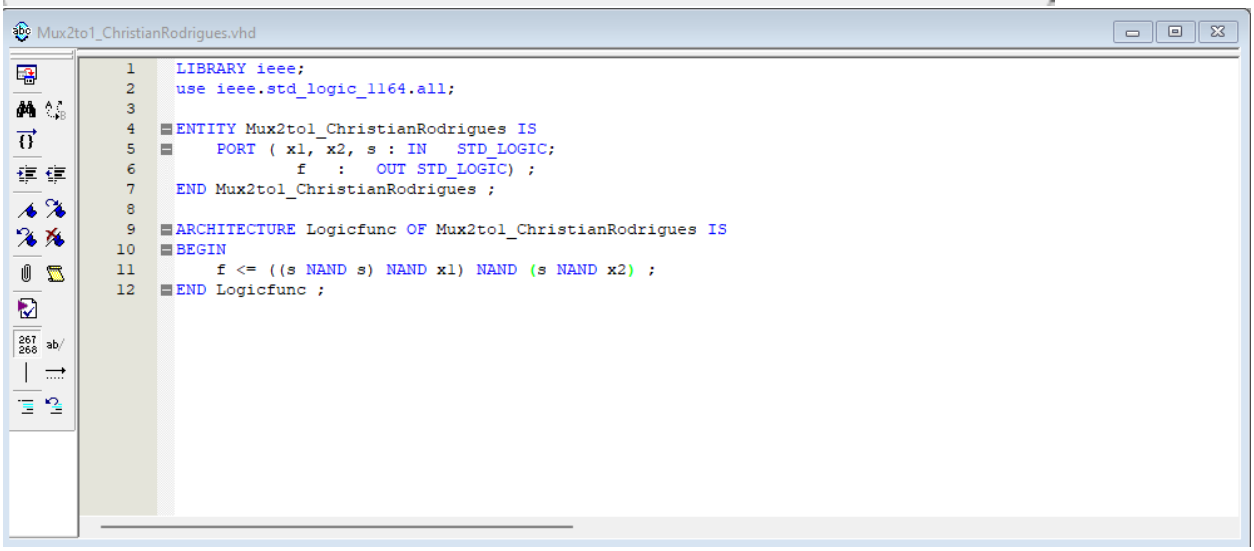
LAB1

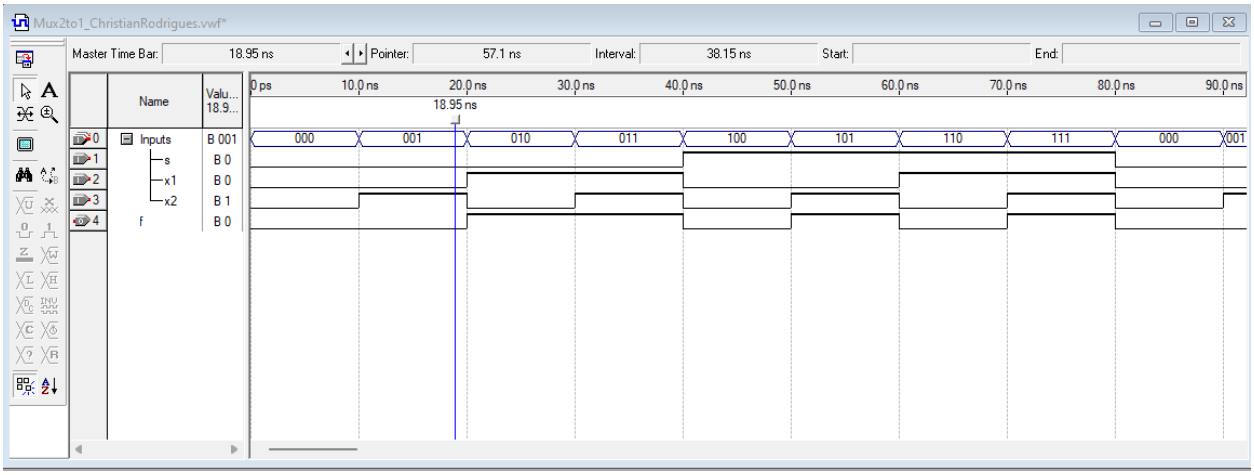
The purpose of this lab is to create a 2 to 1 multiplexer and utilize it as a component to create a 4 to 1, 8 to 1, and 16 to 1 multiplexer.

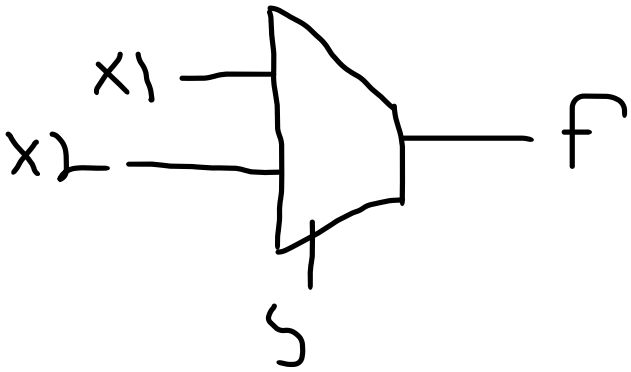
Christian Rodrigues –
Petrie CDA3203 –
10/21/2022

2 to 1 Mux

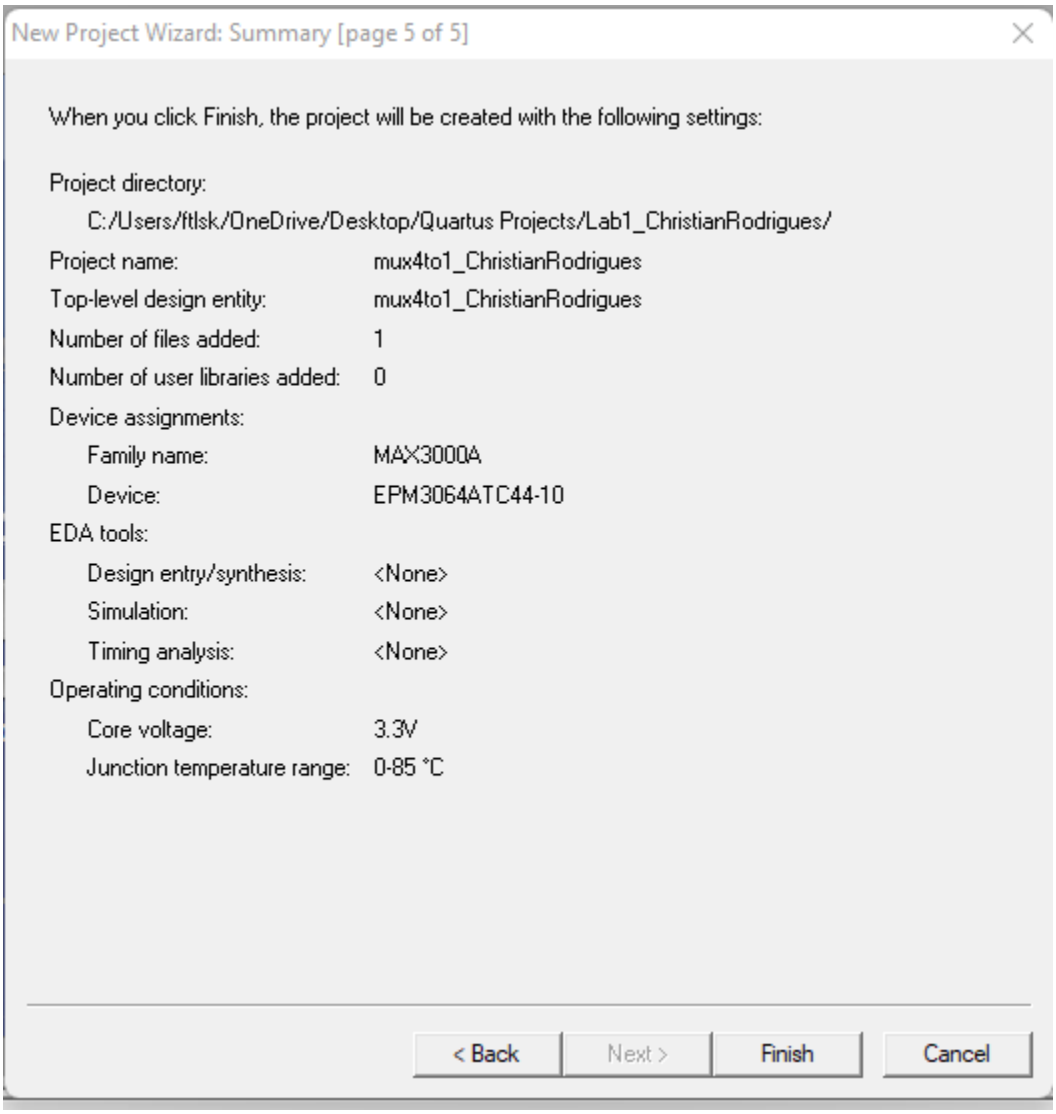

New Project Wizard: Summary [page 5 of 5]
When you click Finish, the project will be created with the following settings:
Project directory:
C:/Users/ftlsk/OneDrive/Desktop/Quartus Projects/Lab1_ChristianRodrigues/
Project name: Mux2to1_ChristianRodrigues
Top-level design entity: Mux2to1_ChristianRodrigues
Number of files added: 0
Number of user libraries added: 0
Device assignments:
Family name: MAX3000A
Device: EPM3064ATC44-10
EDA tools:
Design entry/synthesis: <None>
Simulation: <None>
Timing analysis: <None>
Operating conditions:
Core voltage: 3.3V
Junction temperature range: 0-85 °C
< Back
Next >
Finish
Cancel


Mux2to1_ChristianRodrigues.vhd
1 LIBRARY ieee;
2 use ieee.std_logic_1164.all;
3
4 ENTITY Mux2to1_ChristianRodrigues IS
5 PORT (x1, x2, s : IN STD_LOGIC;
6 f : OUT STD_LOGIC) ;
7 END Mux2to1_ChristianRodrigues ;
8
9 ARCHITECTURE Logicfunc OF Mux2to1_ChristianRodrigues IS
10 BEGIN
11 f <= ((s NAND s) NAND x1) NAND (s NAND x2) ;
12 END Logicfunc ;


Mux2to1_ChristianRodrigues.vwf*
Master Time Bar: 18.95 ns
Pointer: 57.1 ns
Interval: 38.15 ns
Start:
End:
Name
Valu...
18.9...
0 ps
10.0 ns
20.0 ns
30.0 ns
40.0 ns
50.0 ns
60.0 ns
70.0 ns
80.0 ns
90.0 ns
18.95 ns
Inputs
B 001
s
B 0
x1
B 0
x2
B 1
f
B 0
000
001
010
011
100
101
110
111
000
001


x1
x2
f
s

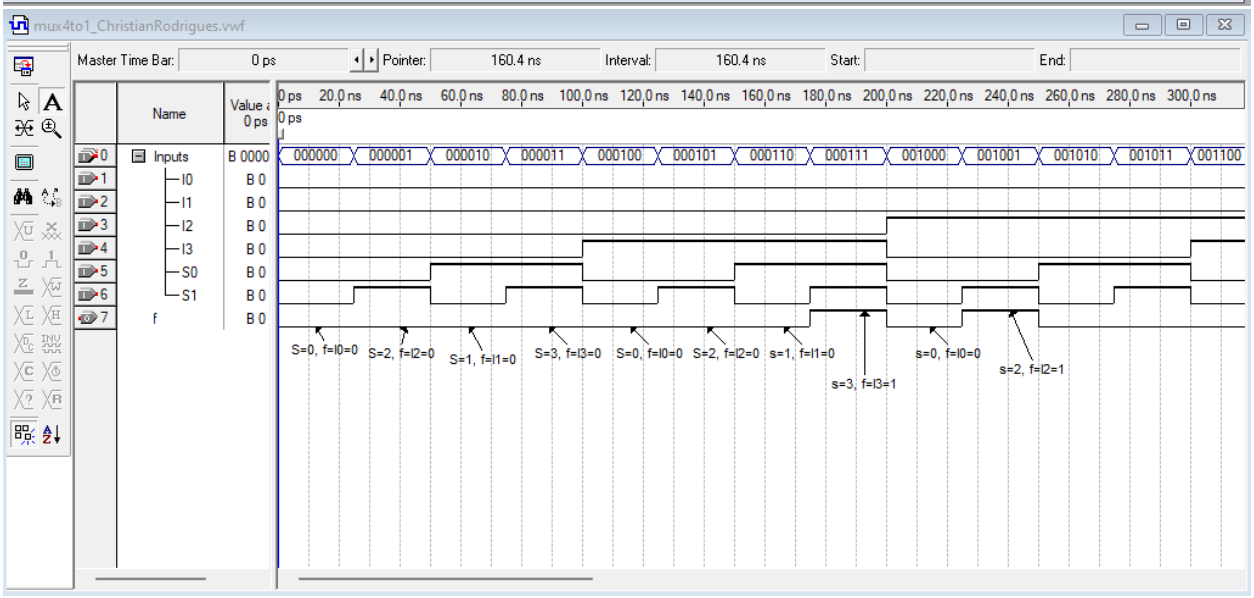
4 to 1 Mux

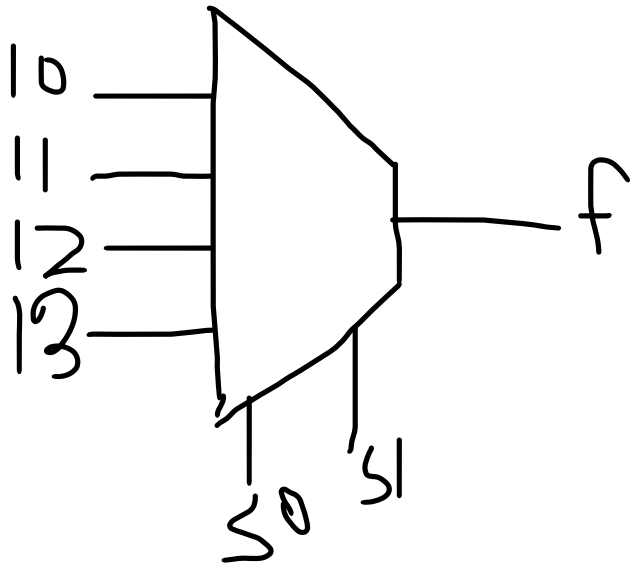

New Project Wizard: Summary [page 5 of 5]
When you click Finish, the project will be created with the following settings:
Project directory:
C:/Users/ftlsk/OneDrive/Desktop/Quartus Projects/Lab1_ChristianRodrigues/
Project name: mux4to1_ChristianRodrigues
Top-level design entity: mux4to1_ChristianRodrigues
Number of files added: 1
Number of user libraries added: 0
Device assignments:
Family name: MAX3000A
Device: EPM3064ATC44-10
EDA tools:
Design entry/synthesis: <None>
Simulation: <None>
Timing analysis: <None>
Operating conditions:
Core voltage: 3.3V
Junction temperature range: 0-85 °C
< Back
Next >
Finish
Cancel

mux4to1_ChristianRodrigues.vhd

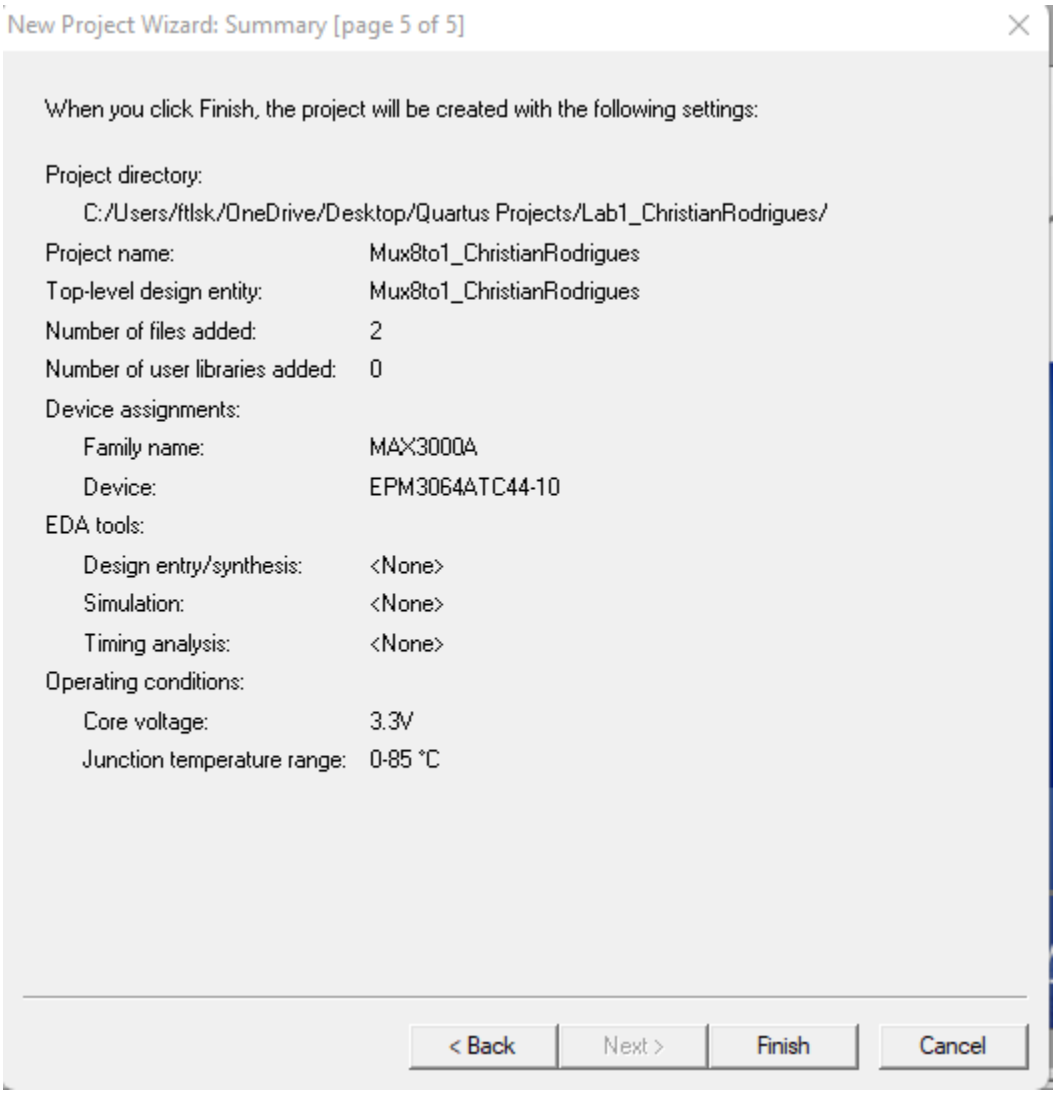
```
1   LIBRARY ieee;
2   USE ieee.std_logic_1164.all;
3   ENTITY mux4tol_ChristianRodrigues IS
4       PORT (I0, I1, I2, I3, S1, S0 : IN STD_LOGIC;
5             f : OUT STD_LOGIC);
6   END mux4tol_ChristianRodrigues;
7
8   ARCHITECTURE LogicFunc OF mux4tol_ChristianRodrigues IS
9   SIGNAL f1, f2 : STD_LOGIC;
10  COMPONENT mux2tol_ChristianRodrigues IS
11      PORT (x1, x2, s : IN STD_LOGIC;
12            f : OUT STD_LOGIC);
13  END COMPONENT;
14
15  BEGIN
16  mux0: mux2tol_ChristianRodrigues PORT MAP (I0, I1, S0, f1);
17  mux1: mux2tol_ChristianRodrigues PORT MAP (I2, I3, S0, f2);
18  mux2: mux2tol_ChristianRodrigues PORT MAP (f1, f2, s1, f);
19  END LogicFunc;
20
21
```

mux4to1_ChristianRodrigues.vwf



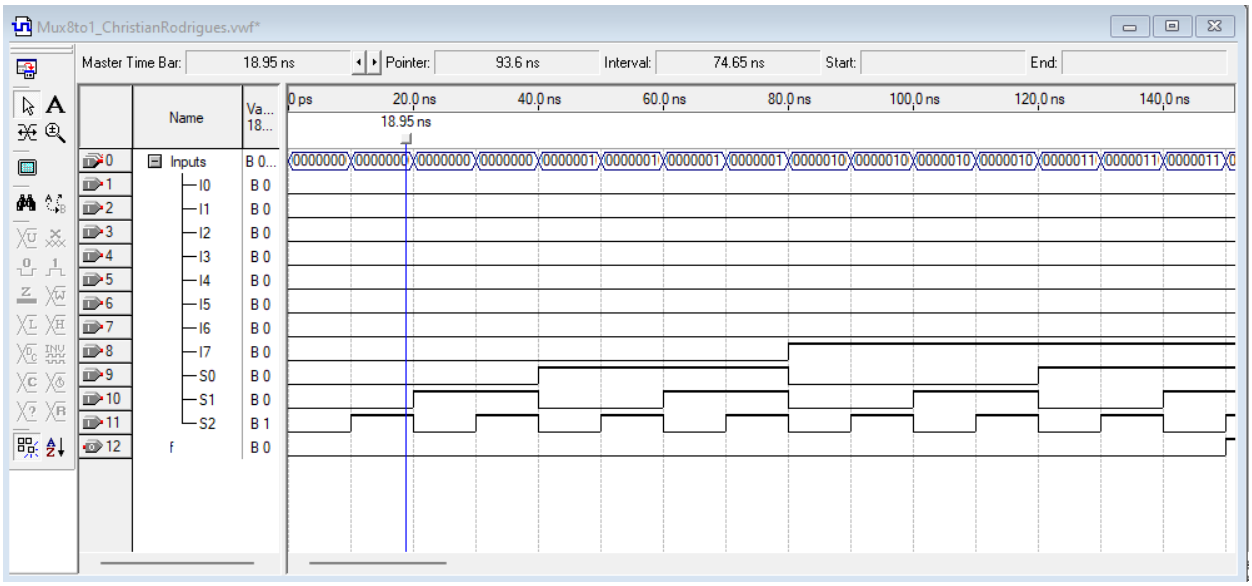


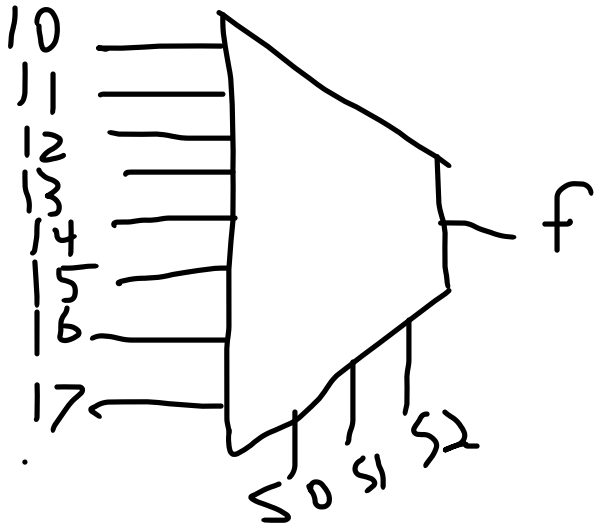
8 to 1 Mux


New Project Wizard: Summary [page 5 of 5]
When you click Finish, the project will be created with the following settings:
Project directory:
C:/Users/ftlsk/OneDrive/Desktop/Quartus Projects/Lab1_ChristianRodrigues/
Project name: Mux8to1_ChristianRodrigues
Top-level design entity: Mux8to1_ChristianRodrigues
Number of files added: 2
Number of user libraries added: 0
Device assignments:
Family name: MAX3000A
Device: EPM3064ATC44-10
EDA tools:
Design entry/synthesis: <None>
Simulation: <None>
Timing analysis: <None>
Operating conditions:
Core voltage: 3.3V
Junction temperature range: 0-85 °C
< Back
Next >
Finish
Cancel

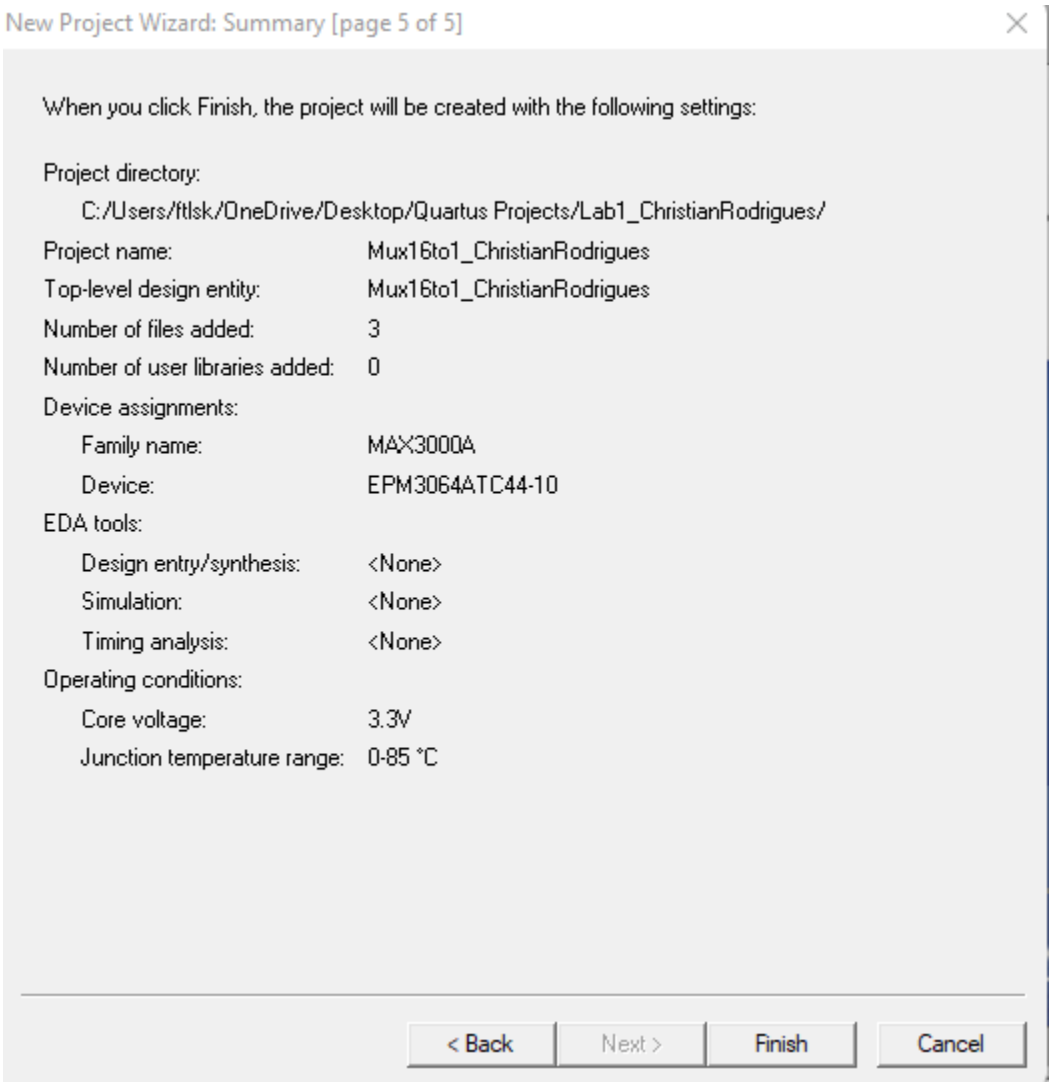
Mux8to1_ChristianRodrigues.vhd

```
1   LIBRARY ieee;
2   use ieee.std_logic_1164.all;
3
4   ENTITY Mux8to1_ChristianRodrigues IS
5       PORT (I0, I1, I2, I3, I4, I5, I6, I7, S0, S1, S2 : IN STD_LOGIC;
6             f : OUT STD_LOGIC);
7   END Mux8to1_ChristianRodrigues;
8
9   ARCHITECTURE LogicFunc OF Mux8to1_ChristianRodrigues IS
10      COMPONENT mux4to1_ChristianRodrigues IS
11      PORT (I0, I1, I2, I3, S0, S1 : IN STD_LOGIC;
12            f  : OUT STD_LOGIC);
13  END COMPONENT;
14
15  COMPONENT Mux2to1_ChristianRodrigues IS
16          PORT (x1, x2, s : IN STD_LOGIC;
17                f   : OUT STD_LOGIC);
18  END COMPONENT;
19
20  SIGNAL f1, f2 : STD_LOGIC;
21  BEGIN
22  mux0: Mux4to1_ChristianRodrigues PORT MAP (I0, I1, I2, I3, S0, S1, f1);
23  mux1: Mux4to1_ChristianRodrigues PORT MAP (I4, I5, I6, I7, S0, S1, f2);
24  mux2: Mux2to1_ChristianRodrigues PORT MAP (f1, f2, S2, f);
25  END LogicFunc;
```





16 to 1 Mux


New Project Wizard: Summary [page 5 of 5]
When you click Finish, the project will be created with the following settings:
Project directory:
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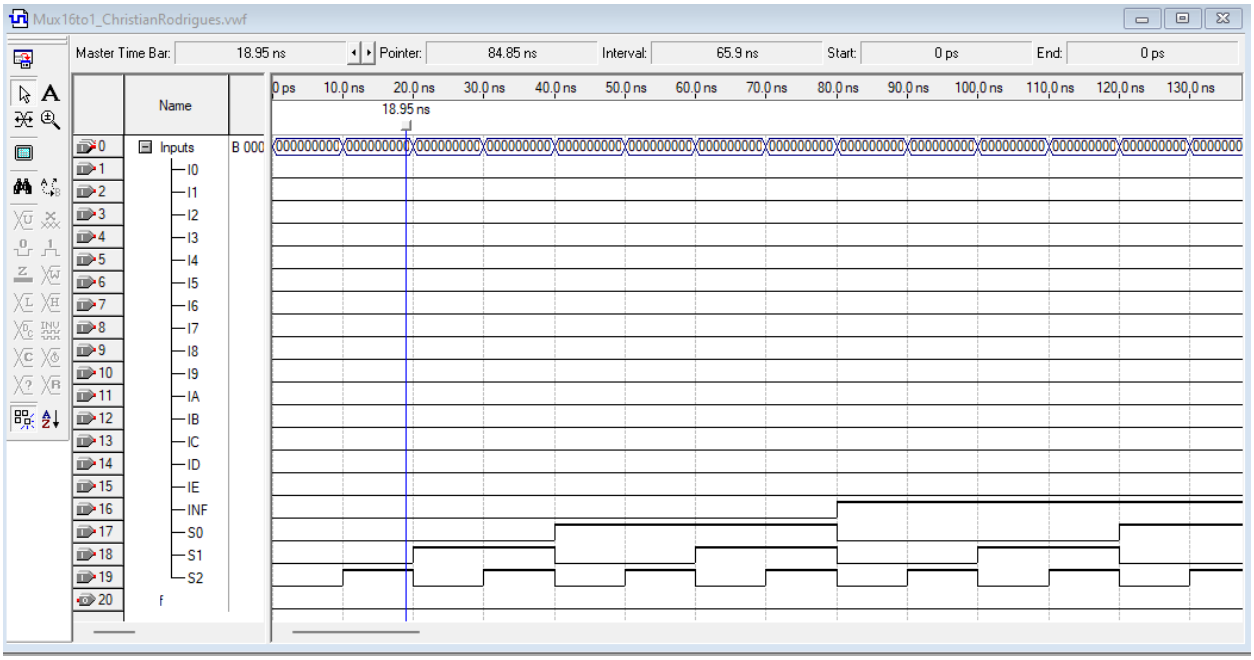
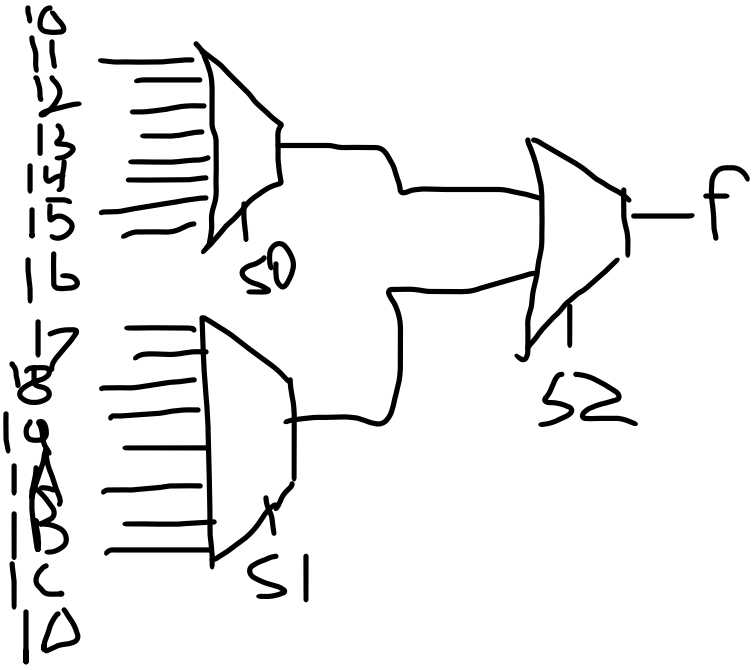
Project name: Mux16to1_ChristianRodrigues
Top-level design entity: Mux16to1_ChristianRodrigues
Number of files added: 3
Number of user libraries added: 0
Device assignments:
Family name: MAX3000A
Device: EPM3064ATC44-10
EDA tools:
Design entry/synthesis: <None>
Simulation: <None>
Timing analysis: <None>
Operating conditions:
Core voltage: 3.3V
Junction temperature range: 0-85 °C
< Back
Next >
Finish
Cancel

Mux16to1_ChristianRodrigues.vhd

```
1  LIBRARY ieee;
2  use ieee.std_logic_1164.all;
3
4  ENTITY Mux16tol_ChristianRodrigues IS
5      PORT (I0, I1, I2, I3, I4, I5, I6, I7, I8, I9, IA, IB, IC, ID, IE, INF, S0, S1, S2 : IN STD_LOGIC;
6            f  : OUT STD_LOGIC);
7  END Mux16tol_ChristianRodrigues;
8
9  ARCHITECTURE LogicFunc OF Mux16tol_ChristianRodrigues IS
10 COMPONENT Mux8tol_ChristianRodrigues IS
11     PORT (I0, I1, I2, I3, I4, I5, I6, I7, S0, S1, S2 : IN STD_LOGIC;
12           f   : OUT STD_LOGIC);
13 END COMPONENT;
14
15 COMPONENT Mux2tol_ChristianRodrigues IS
16     PORT (x1, x2, s : IN STD_LOGIC;
17           f   : OUT STD_LOGIC);
18 END COMPONENT;
19
20 SIGNAL f1, f2 : STD_LOGIC;
21
22 BEGIN
23 mux0: Mux8tol_ChristianRodrigues PORT MAP (I0, I1, I2, I3, I4, I5, I6, I7, S0, S1, S2, f1);
24 mux1: Mux8tol_ChristianRodrigues PORT MAP (I8, I9, IA, IB, IC, ID, IE, INF, S0, S1, S2, f2);
25 mux2: Mux2tol_ChristianRodrigues PORT MAP (f1, f2, S2, f);
26 END LogicFunc;
```

Mux16to1_ChristianRodrigues.vwf





CDA 3203 – Computer Logic Design **Name** Christian Rodrigues
Fall 2022 – Dr. Petrie **Lab 1** **__/100 pts**

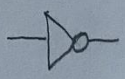
Lab 1: The objectives of this lab are:

1) *Design circuit equivalents for all the logic gates using NOT-AND-OR gates and design equivalent circuits using only one of the universal gates: NAND or NOR. We will design all-NAND equivalent circuits.*
2) *Design the circuit using Altera Quartus II 9.1 Web Edition, and verify the circuit is correct by comparing the Timing Diagram results to the Truth Table of the circuit.*
3) *Design and simulate an Active-Low Decoder, (DMux) circuit.*
4) *Design and simulate a Multiplexer (Mux) circuit.*

Part 1.
HANDWORK:

1. **[40 pts.] Design 9 circuits** by completing below: Draw the symbol for the gate, its Truth Table, its Simplest Sum of Products Expression, draw its NOT-AND-OR Equivalent Circuit, its all-NAND Equivalent Circuit.

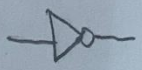
1.1 Draw **NOT** gate:



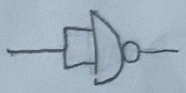
Truth Table:

A	NOT(A)
0	1
1	0

NOT-AND-OR Equivalent Circuit

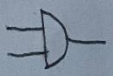


all-NAND Equivalent Circuit:



Y1= A'

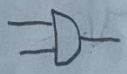
1.2 Draw **AND** gate:



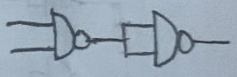
Truth Table:

A	B	AND(A,B)
0	0	0
0	1	0
1	0	0
1	1	1

NOT-AND-OR Equivalent Circuit

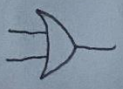


all-NAND Equivalent Circuit:



Y2= AB

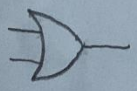
1.3 Draw **OR** gate:



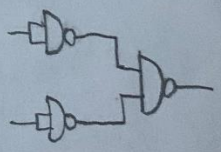
Truth Table:

A	B	OR(A,B)
0	0	0
0	1	1
1	0	1
1	1	1

NOT-AND-OR Equivalent Circuit

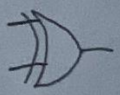


all-NAND Equivalent Circuit:



Y3= A+B

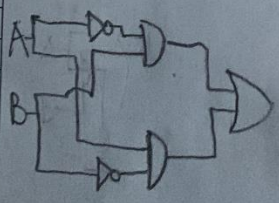
1.4 Draw **XOR** gate:



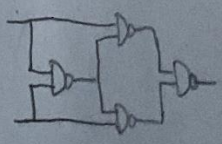
Truth Table:

A	B	XOR(A,B)
0	0	0
0	1	1
1	0	1
1	1	0

NOT-AND-OR Equivalent Circuit:

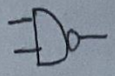


all-NAND Equivalent Circuit:

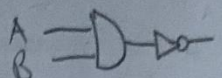


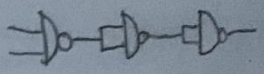
Y4= A⊕B

1.5 Draw **NAND** gate: **Truth Table:** **NOT-AND-OR Equivalent Circuit:** **all-NAND Equivalent Circuit:**



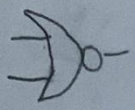
A	B	NAND(A,B)
0	0	1
0	1	1
1	0	1
1	1	0



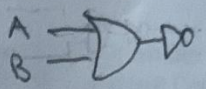


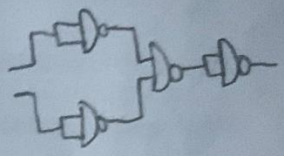
Y5= A'B'

1.6 Draw **NOR** gate: **Truth Table:** **NOT-AND-OR Equivalent Circuit:** **all-NAND Equivalent Circuit:**



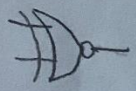
A	B	NOR(A,B)
0	0	1
0	1	0
1	0	0
1	1	0



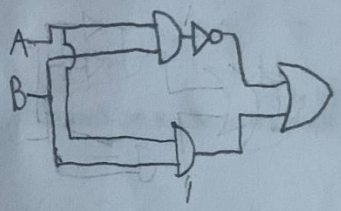


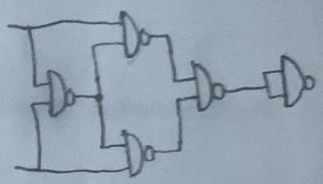
Y6= A' + B'

1.7 Draw **XNOR** gate: **Truth Table:** **NOT-AND-OR Equivalent Circuit:** **all-NAND Equivalent Circuit:**



A	B	XNOR(A,B)
0	0	1
0	1	0
1	0	0
1	1	1

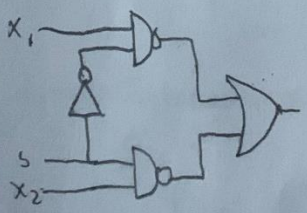


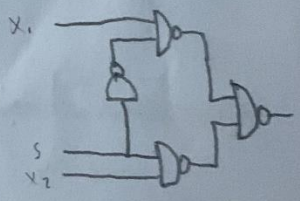


Y7= A' ⊕ B'

1.8 **2-to-1 Encoder** or **Multiplexer (Mux)**: Truth Table: NOT-AND-OR Equivalent Circuit: all-NAND Equivalent

s	X_1	X_0	mux
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	1





Y8= $S'X_1 + SX_0$

1.9 Draw **2-to-4-Decoder** or **Demultiplexer (DMux)**: **Truth Table:** **NOT-AND-OR Equivalent Circuit:** **all-NAND Equivalent Circuit:**

X_1	X_0	F_3	F_2	F_1	F_0
0	0	0	0	0	1
0	1	0	0	1	0
1	0	0	1	0	0
1	1	1	0	0	0

Y9=