LAB 3

The goal of this lab is to create a flip flops, registers, RAM and various other forms of memory using behavioral architectures

Christian Rodrigues –
Petrie CDA 3203 –
12/4/2022

Handwork

CDA 3203 – Computer Logic Design **Name** Christian Rodrigues
Fall 2022 – Dr. Petrie **Lab 3** **__/100 pts**

Lab 3: The objectives of this lab are:

1) *16 pts. Truth Table, Timing Diagram and Excitation Tables that describe the behavior of D, T, S-R and J-K Flip Flops.*
2) *20 pts. Simulate in Altera Quartus a Flip Flop in VHDL using Behavioral Architecture.*
3) *20 pts. Design and simulate a 1-bit register component.*
4) *20 pts. Design and simulate a 16-bit register component.*
5) *20 pts. Design and simulate a RAM with 8 registers.*
6) *20 pts. Design and simulate a program counter.*

Submit a Lab Report with the required documentation.

1. 16 pts. Handwork

Complete Truth Table and Timing Diagram for each Flip Flops, **all inputs are active high, clock is positive-edge triggered** (rising edge)

1.1 D Flip Flop

D	Q	Command	Q+
0	0	Make Q=0	0
	1		0
1	0	Make Q=1	1
	1		1

1.2 T Flip Flop

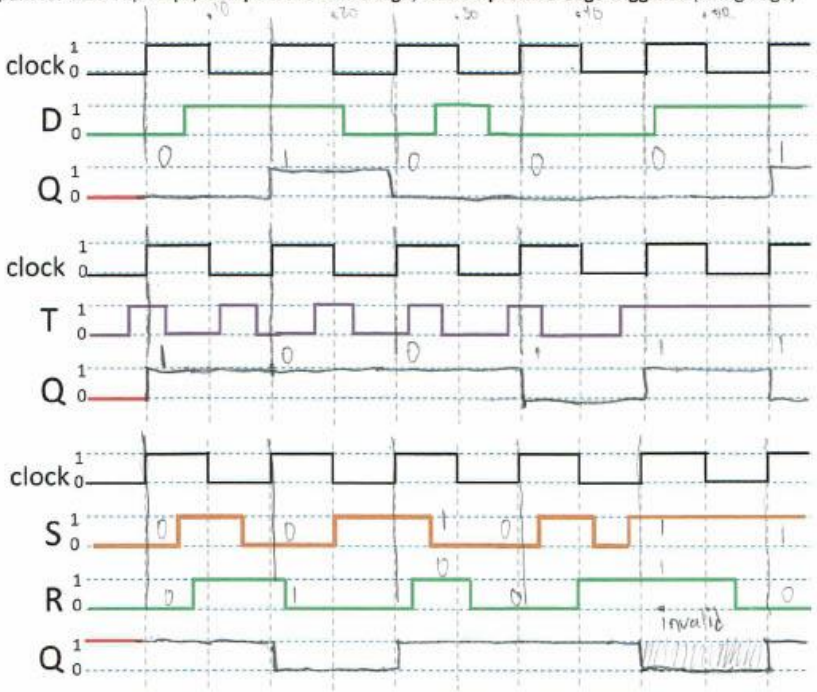
T	Q	Command	Q+
0	0	Hold	0
	1		1
1	0	Toggle	1
	1		0

1.3 S-R Flip Flop

S	R	Q	Command	Q+
0	0	0	Hold	0
		1		1
0	1	0	Reset	0
		1		0
1	0	0	Set	1
		1		1
1	1	0	Invalid	?
		1		?

1.4 J-K Flip Flop

J	K	Q	Command	Q+
0	0	0	Hold	0
		1		1
0	1	0	Reset	0
		1		0
1	0	0	Set	1
		1		1
1	1	0	Toggle	1
		1		0



1.5 Excitation Tables are used to figure out what you need to place on the input of a flip flop to force Q to the desired transition. Look at Truth Tables in the previous page to find what commands and flip flop input values are needed to force next transition.
Note : all inputs of the flip-flopss are **active high**

Q→Q⁺	Command	D
0→0	Make Q=0	0
0→1	Make Q=1	1
1→0	Make Q=0	0
1→1	Make Q=1	1

Q→Q⁺	Command	T
0→0	Hold	0
0→1	Toggle	1
1→0	Toggle	1
1→1	Hold	0

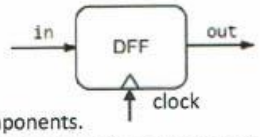
Q→Q⁺	Commands	S R
0→0	Hold Reset	0X
0→1	Set	10
1→0	Reset	01
1→1	Hold Set	X0

Q→Q⁺	Commands	J K
0→0	Hold Reset	0X
0→1	Set Toggle	1X
1→0	Reset Toggle	X1
1→1	Hold Set	X0

2. Design and Simulation of Sequential Components in Altera Quartus using VHDL

VIEW **LAB 3 EXPLAINED VIDEO** FOR MORE DETAILS, CODE AND DIAGRAMS

2.1 Data Flip Flop (DFF)



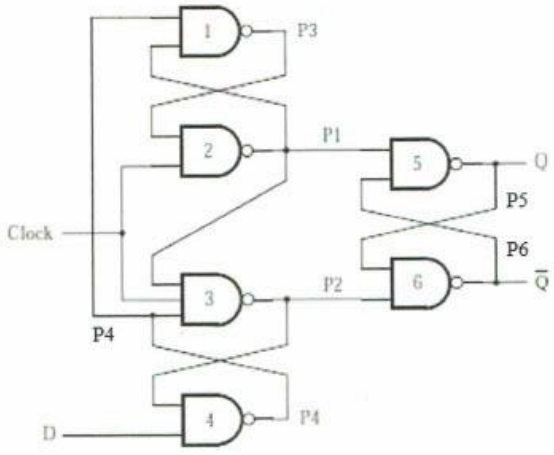
Below is the schematic for a Data Flip Flop, which part of the design of the other components.
Up to now we have used a *Structural* VHDL description of how to connect the hardware components that make up the circuit. To the right is the *Behavioral* VHDL description of the circuit, which looks more like a software program and describes how it behaves instead of how it is built. Use this code to Simulate the DFF

The VHDL statement **process** is used to execute the body of the process (enclosed between the **begin** and **end process**) each time a signal in the **sensitivity list** (in parenthesis) changes. You also see the conditional statement **if**, **then**, **end if** which works exactly as you experience in programming. In the condition, you see the **rising_edge** built-in VHDL clock function, which is true when a signal transitions from low to high. There is also a **falling_edge** function available in VHDL for negative edge triggered flip flops. Use the code at right and set the clock input to Value -> Clock In the Timing Diagram, and D values to mimic Ex. 1.1.

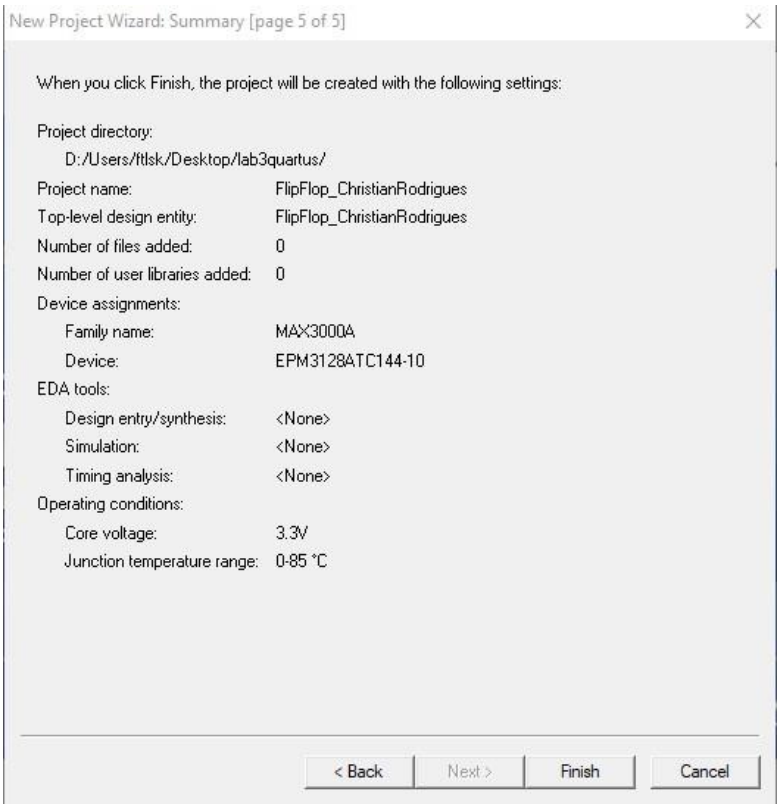
```
-- Data Flip Flop positive-edge triggered
-- Behavioral VHDL model
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;

ENTITY DFF_PetrieMaria IS
   PORT (D, clock: IN STD_LOGIC;
         Q       : INOUT STD_LOGIC );
END DFF_PetrieMaria;

ARCHITECTURE Behavior OF DFF_PetrieMaria IS
BEGIN
-- Update on the rising edge of the clock
   PROCESS (clock)
   BEGIN
      IF (RISING_EDGE(clock)) THEN
         Q <= D;
      END IF;
   END PROCESS;
END Behavior;
```

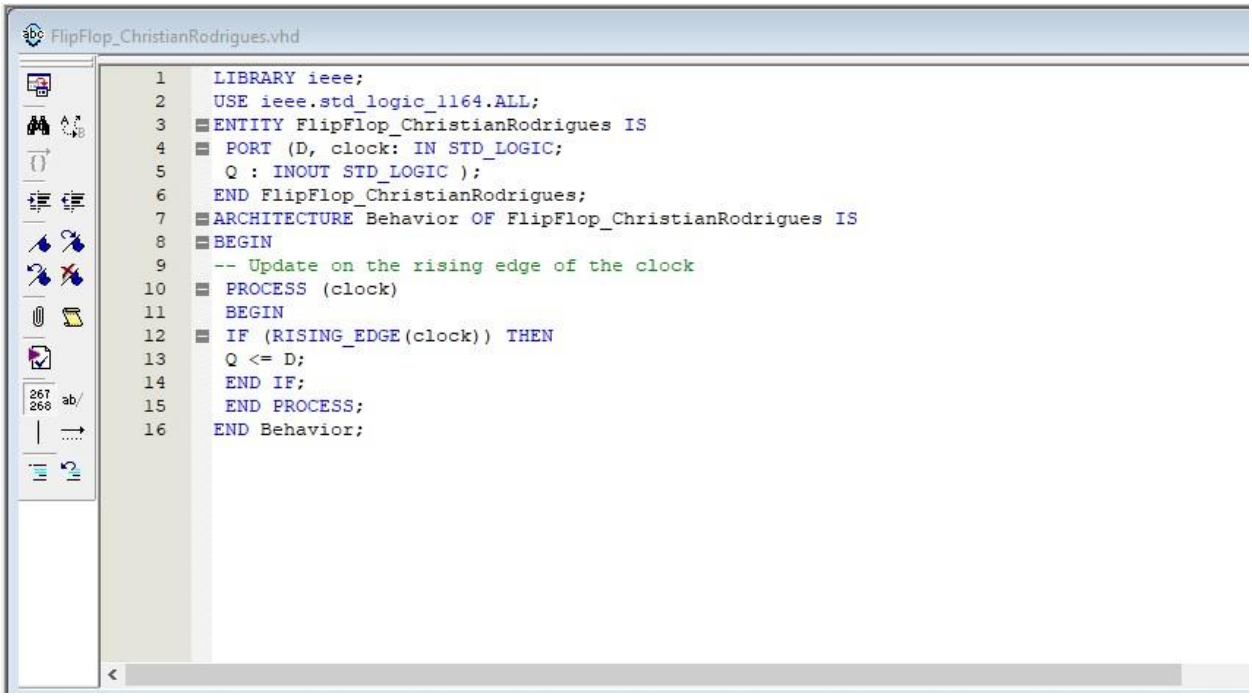
-- In .vwf Timing Diagram set values of inputs to mimic 1.1:
-- clock input to Value -> Clock
-- and adjust the parameters to set the Duty Cycle, length
-- of simulation, and Period; and
-- D input to same values as in Timing Diagram in 1.1

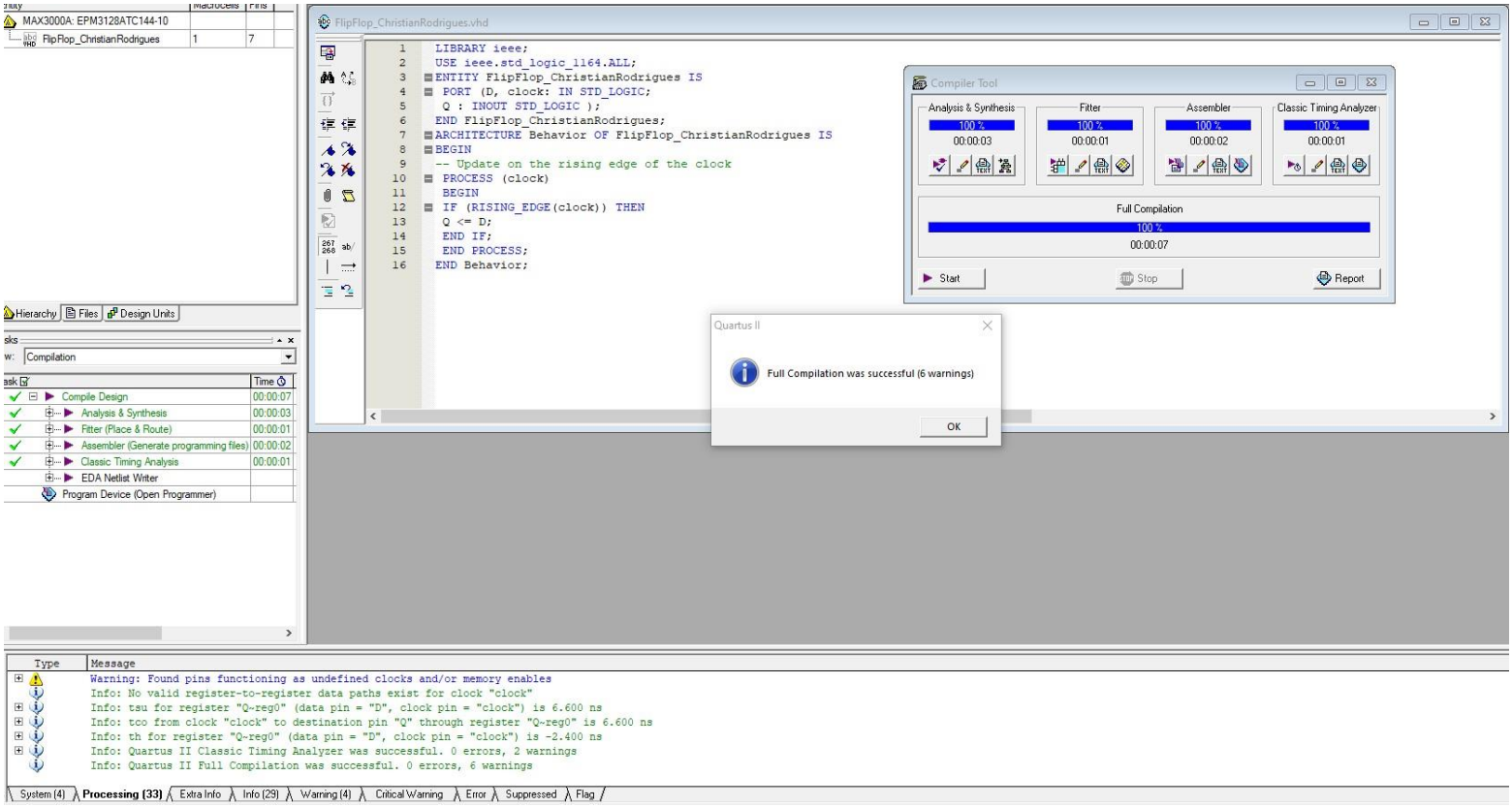
Turn in the snips of Project Setting, VHDL, Successful Compilation, and Timing Diagram in the portfolio

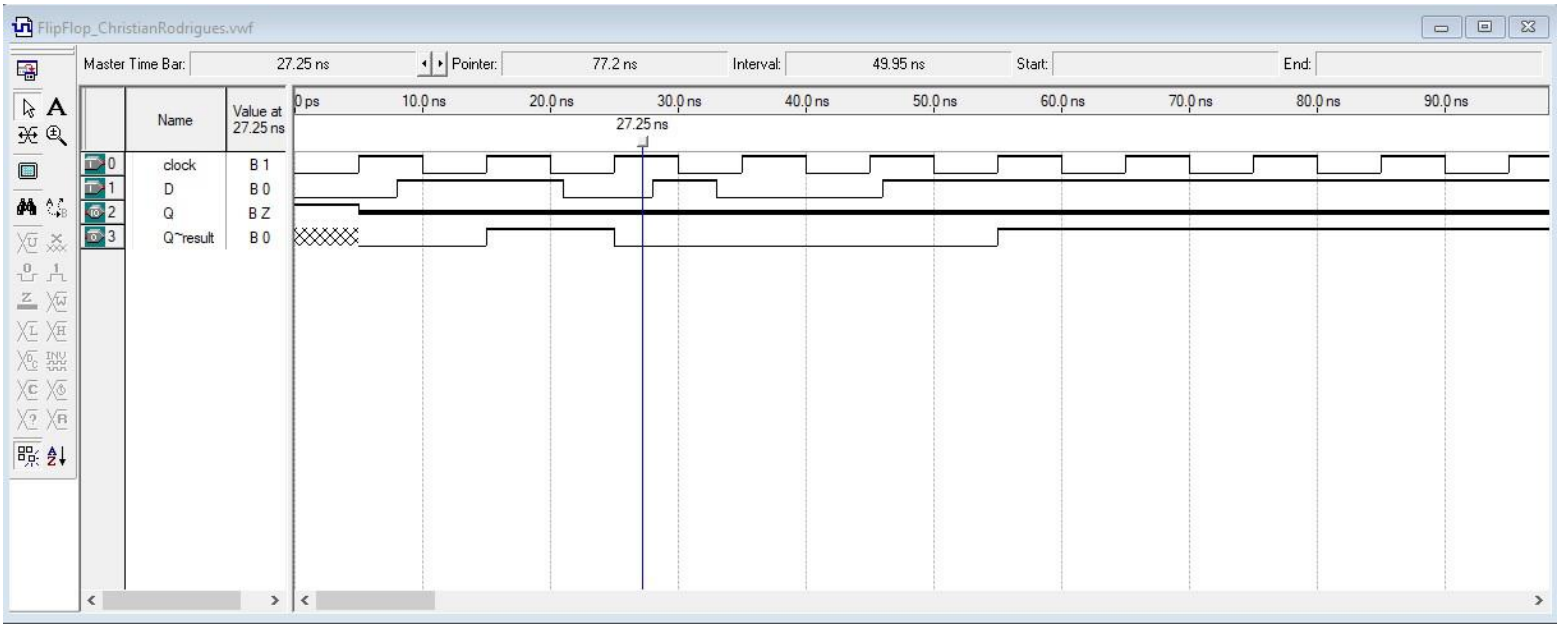


DFF Flip Flop





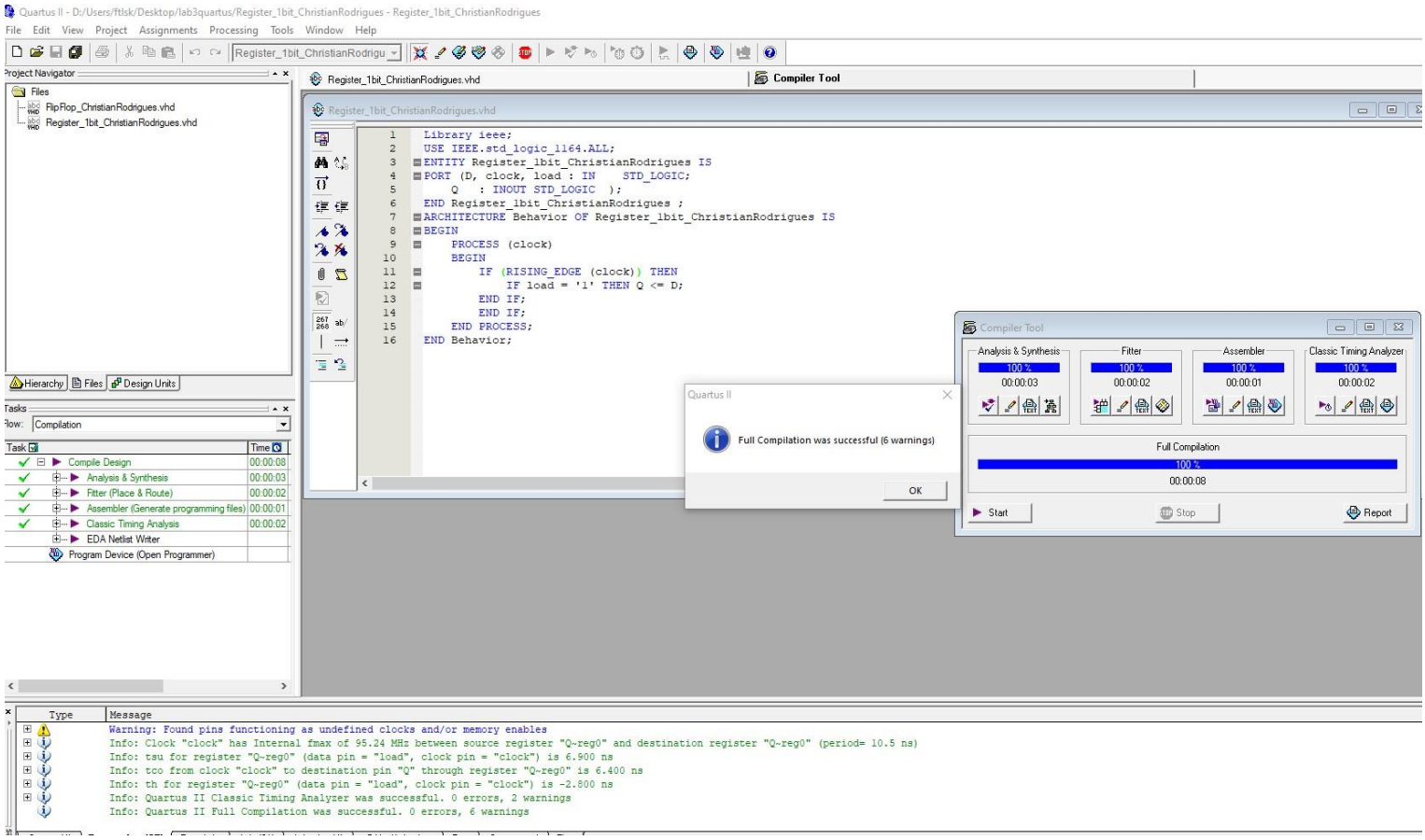

MAX3000A: EPM3128ATC144-10
FlipFlop_ChristianRodrigues
FlipFlop_ChristianRodrigues.vhd
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;
ENTITY FlipFlop_ChristianRodrigues IS
PORT (D, clock: IN STD_LOGIC;
Q : INOUT STD_LOGIC);
END FlipFlop_ChristianRodrigues;
ARCHITECTURE Behavior OF FlipFlop_ChristianRodrigues IS
BEGIN
-- Update on the rising edge of the clock
PROCESS (clock)
BEGIN
IF (RISING_EDGE(clock)) THEN
Q <= D;
END IF;
END PROCESS;
END Behavior;
Compiler Tool
Analysis & Synthesis
Fitter
Assembler
Classic Timing Analyzer
Full Compilation
Start
Stop
Report
Quartus II
Full Compilation was successful (6 warnings)
OK
Hierarchy
Files
Design Units
Compilation
Compile Design
Analysis & Synthesis (Place & Route)
Fitter (Place & Route)
Assembler (Generate programming files)
Classic Timing Analysis
EDA Netlist Writer
Program Device (Open Programmer)
Warning: Found pins functioning as undefined clocks and/or memory enables
Info: No valid register-to-register data paths exist for clock "clock"
Info: tsu for register "Q~reg0" (data pin = "D", clock pin = "clock") is 6.600 ns
Info: tco from clock "clock" to destination pin "Q" through register "Q~reg0" is 6.600 ns
Info: th for register "Q~reg0" (data pin = "D", clock pin = "clock") is -2.400 ns
Info: Quartus II Classic Timing Analyzer was successful. 0 errors, 2 warnings
Info: Quartus II Full Compilation was successful. 0 errors, 6 warnings
System (4)
Processing (33)
Extra Info
Info (29)
Warning (4)
Critical Warning
Error
Suppressed
Flag

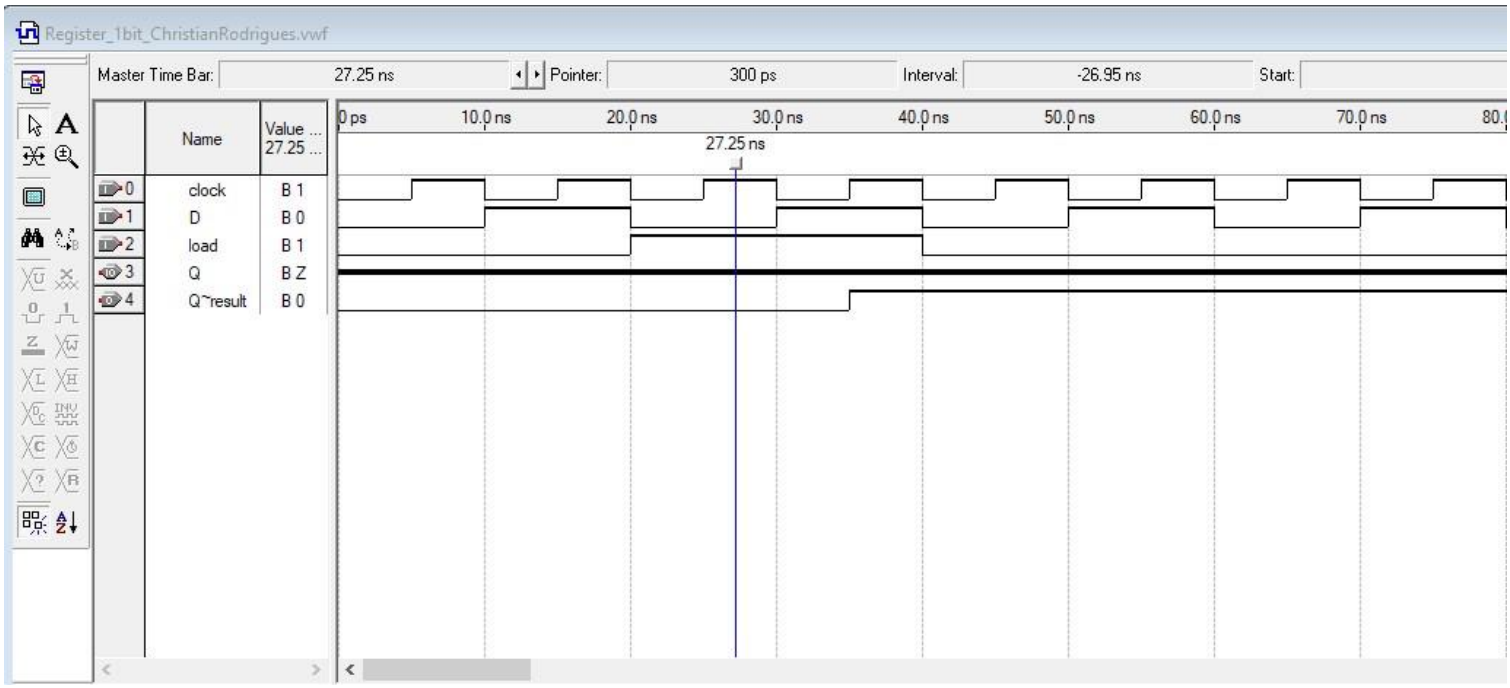

FlipFlop_ChristianRodrigues.vwf
Master Time Bar: 27.25 ns
Pointer: 77.2 ns
Interval: 49.95 ns
Start:
End:
Name
Value at 27.25 ns
0 clock B 1
1 D B 0
2 Q B Z
3 Q~result B 0
0 ps
10.0 ns
20.0 ns
30.0 ns
40.0 ns
50.0 ns
60.0 ns
70.0 ns
80.0 ns
90.0 ns
27.25 ns

1-Bit Register

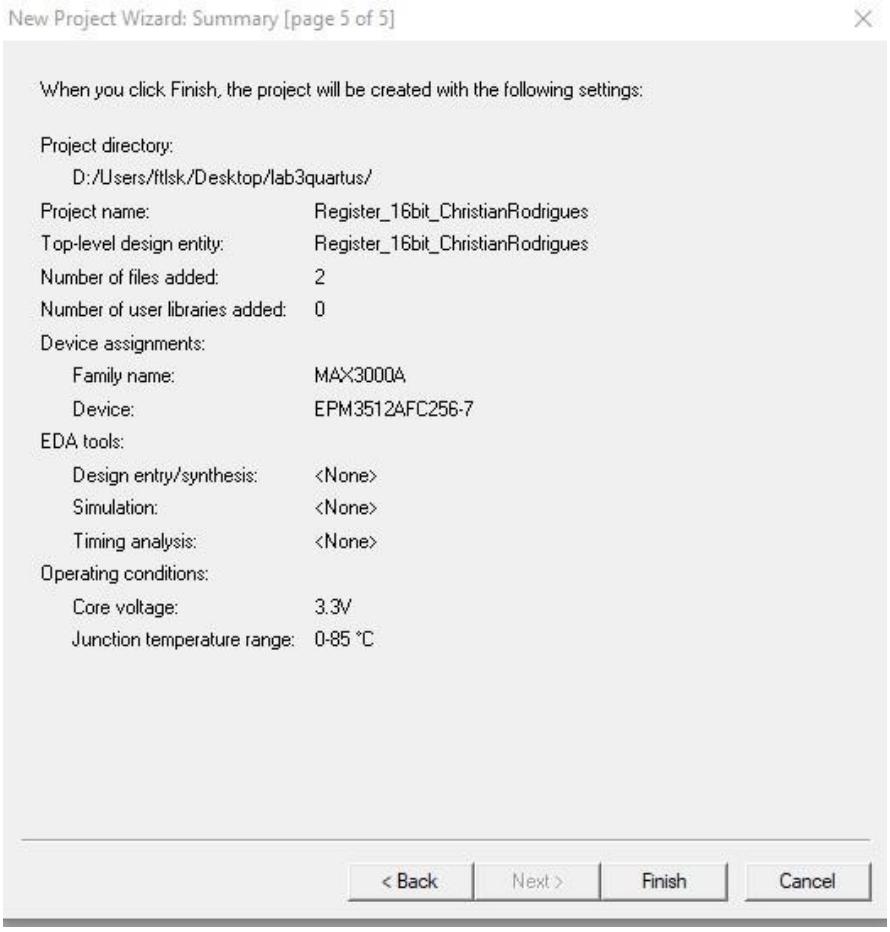
Register_1bit_ChristianRodrigues.vhd

```
1   Library ieee;
2   USE IEEE.std_logic_1164.ALL;
3   ENTITY Register_1bit_ChristianRodrigues IS
4   PORT (D, clock, load : IN    STD_LOGIC;
5         Q   : INOUT STD_LOGIC  );
6   END Register_1bit_ChristianRodrigues ;
7   ARCHITECTURE Behavior OF Register_1bit_ChristianRodrigues IS
8   BEGIN
9       PROCESS (clock)
10      BEGIN
11          IF (RISING_EDGE (clock)) THEN
12              IF load = '1' THEN Q <= D;
13          END IF;
14          END IF;
15      END PROCESS;
16  END Behavior;
```


Quartus II - D:/Users/ftlsk/Desktop/lab3quartus/Register_1bit_ChristianRodrigues - Register_1bit_ChristianRodrigues
File Edit View Project Assignments Processing Tools Window Help
Project Navigator
Files
FlipFlop_ChristianRodrigues.vhd
Register_1bit_ChristianRodrigues.vhd
Hierarchy Files Design Units
Tasks
Flow: Compilation
Task Time
Compile Design 00:00:08
Analysis & Synthesis 00:00:03
Fitter (Place & Route) 00:00:02
Assembler (Generate programming files) 00:00:01
Classic Timing Analysis 00:00:02
EDA Netlist Writer
Program Device (Open Programmer)
Register_1bit_ChristianRodrigues.vhd
Compiler Tool
1 Library ieee;
2 USE IEEE.std_logic_1164.ALL;
3 ENTITY Register_1bit_ChristianRodrigues IS
4 PORT (D, clock, load : IN STD_LOGIC;
5 Q : INOUT STD_LOGIC);
6 END Register_1bit_ChristianRodrigues ;
7 ARCHITECTURE Behavior OF Register_1bit_ChristianRodrigues IS
8 BEGIN
9 PROCESS (clock)
10 BEGIN
11 IF (RISING_EDGE (clock)) THEN
12 IF load = '1' THEN Q <= D;
13 END IF;
14 END IF;
15 END PROCESS;
16 END Behavior;
Quartus II
Full Compilation was successful (6 warnings)
OK
Compiler Tool
Analysis & Synthesis 100 % 00:00:03
Fitter 100 % 00:00:02
Assembler 100 % 00:00:01
Classic Timing Analyzer 100 % 00:00:02
Full Compilation 100 % 00:00:08
Start Stop Report
Type Message
Warning: Found pins functioning as undefined clocks and/or memory enables
Info: Clock "clock" has Internal fmax of 95.24 MHz between source register "Q~reg0" and destination register "Q~reg0" (period= 10.5 ns)
Info: tsu for register "Q~reg0" (data pin = "load", clock pin = "clock") is 6.900 ns
Info: tco from clock "clock" to destination pin "Q" through register "Q~reg0" is 6.400 ns
Info: th for register "Q~reg0" (data pin = "load", clock pin = "clock") is -2.800 ns
Info: Quartus II Classic Timing Analyzer was successful. 0 errors, 2 warnings
Info: Quartus II Full Compilation was successful. 0 errors, 6 warnings

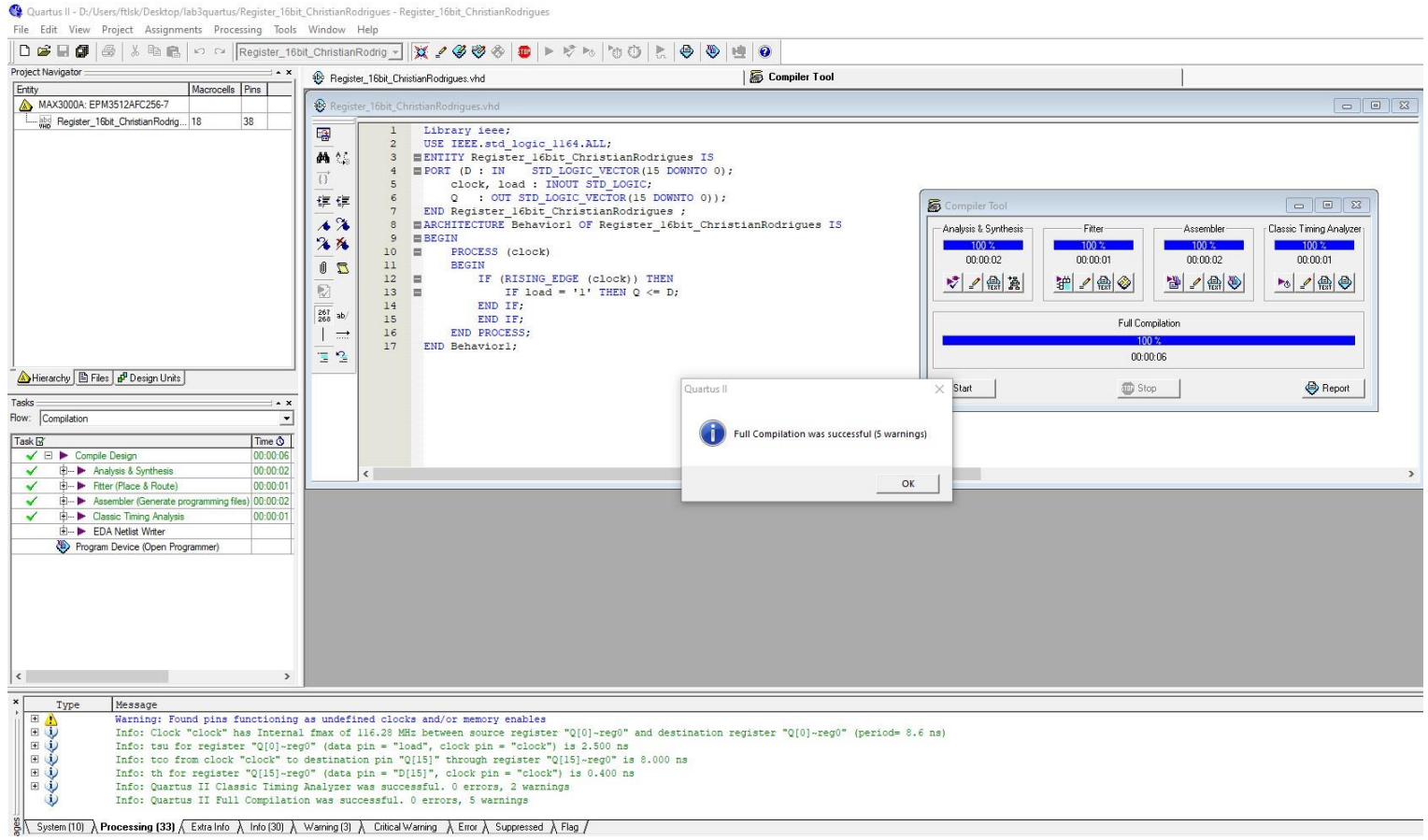

Register_1bit_ChristianRodrigues.vwf
Master Time Bar: 27.25 ns
Pointer: 300 ps
Interval: -26.95 ns
Start:
Name
Value ... 27.25 ...
0 clock B 1
1 D B 0
2 load B 1
3 Q B Z
4 Q~result B 0
0 ps
10.0 ns
20.0 ns
30.0 ns
40.0 ns
50.0 ns
60.0 ns
70.0 ns
27.25 ns

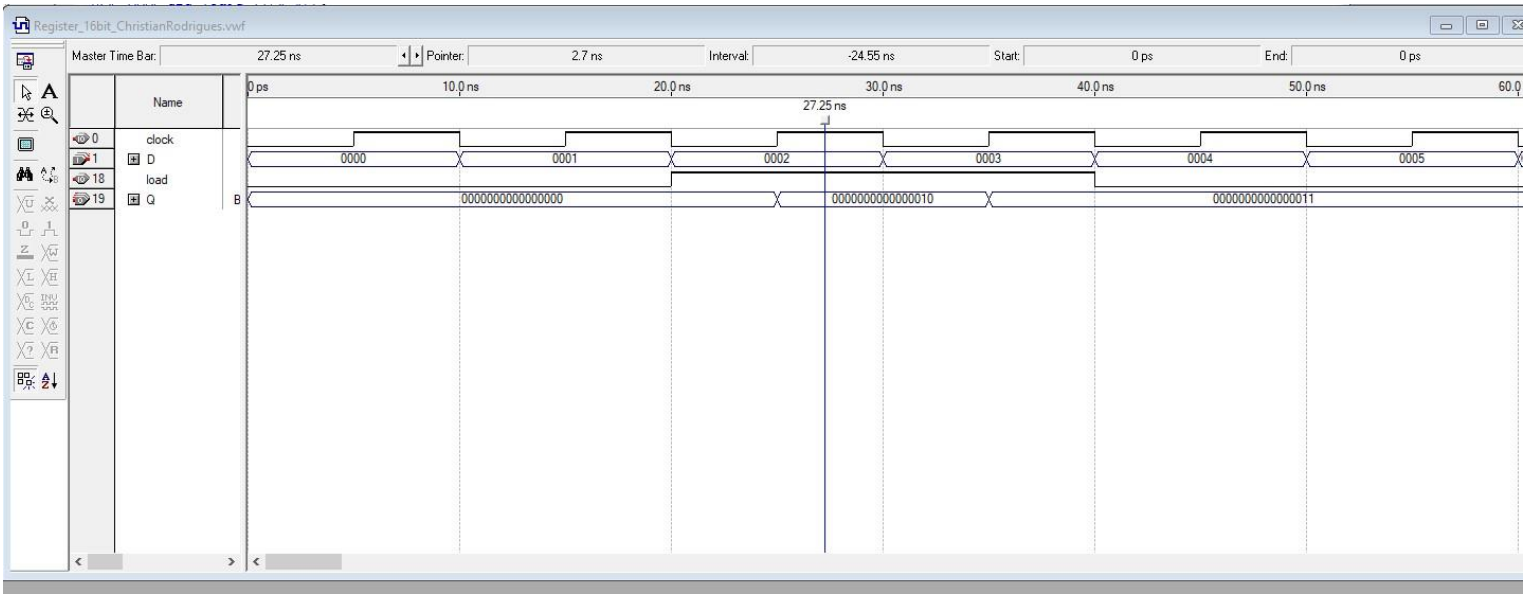
16-Bit Register



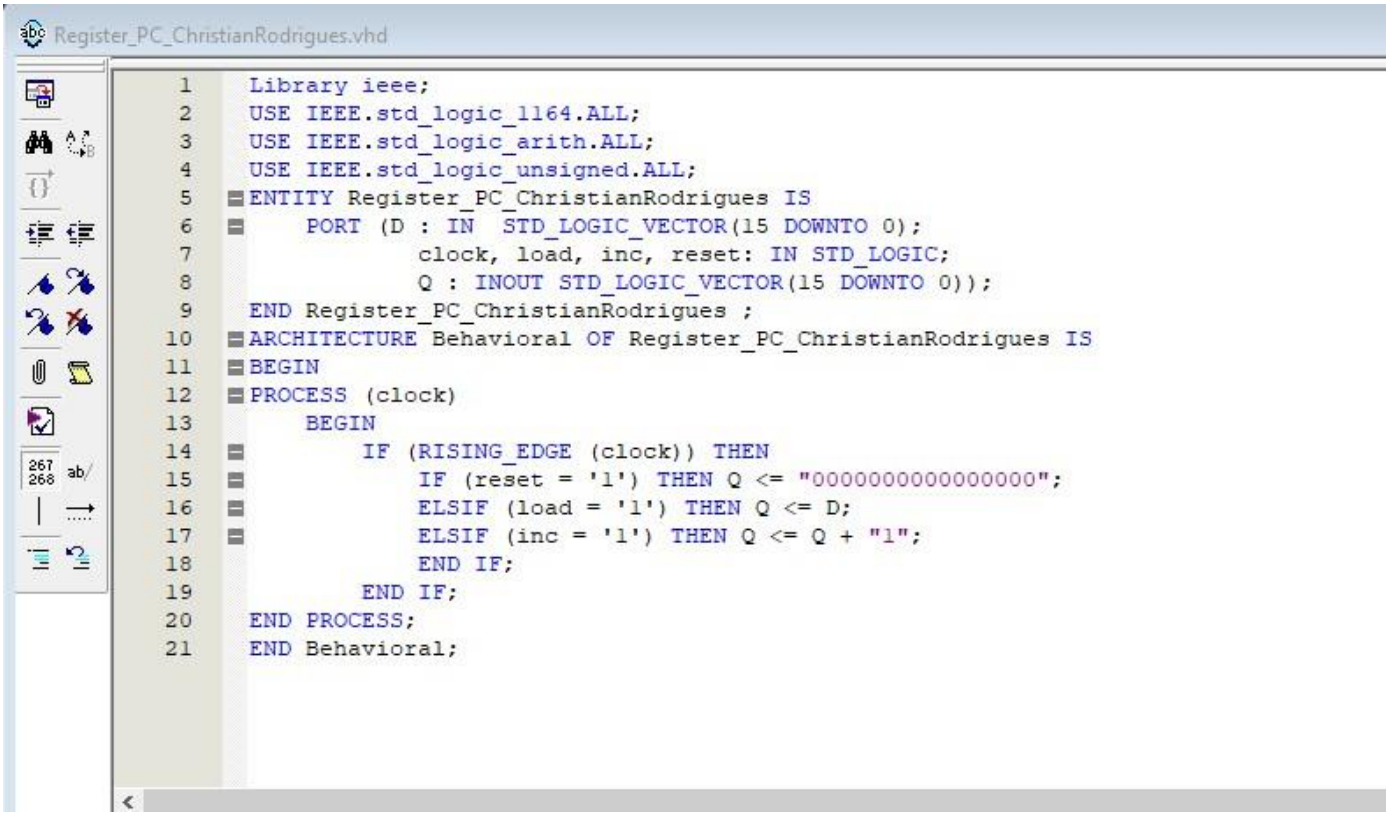
Register_16bit_ChristianRodrigues.vhd

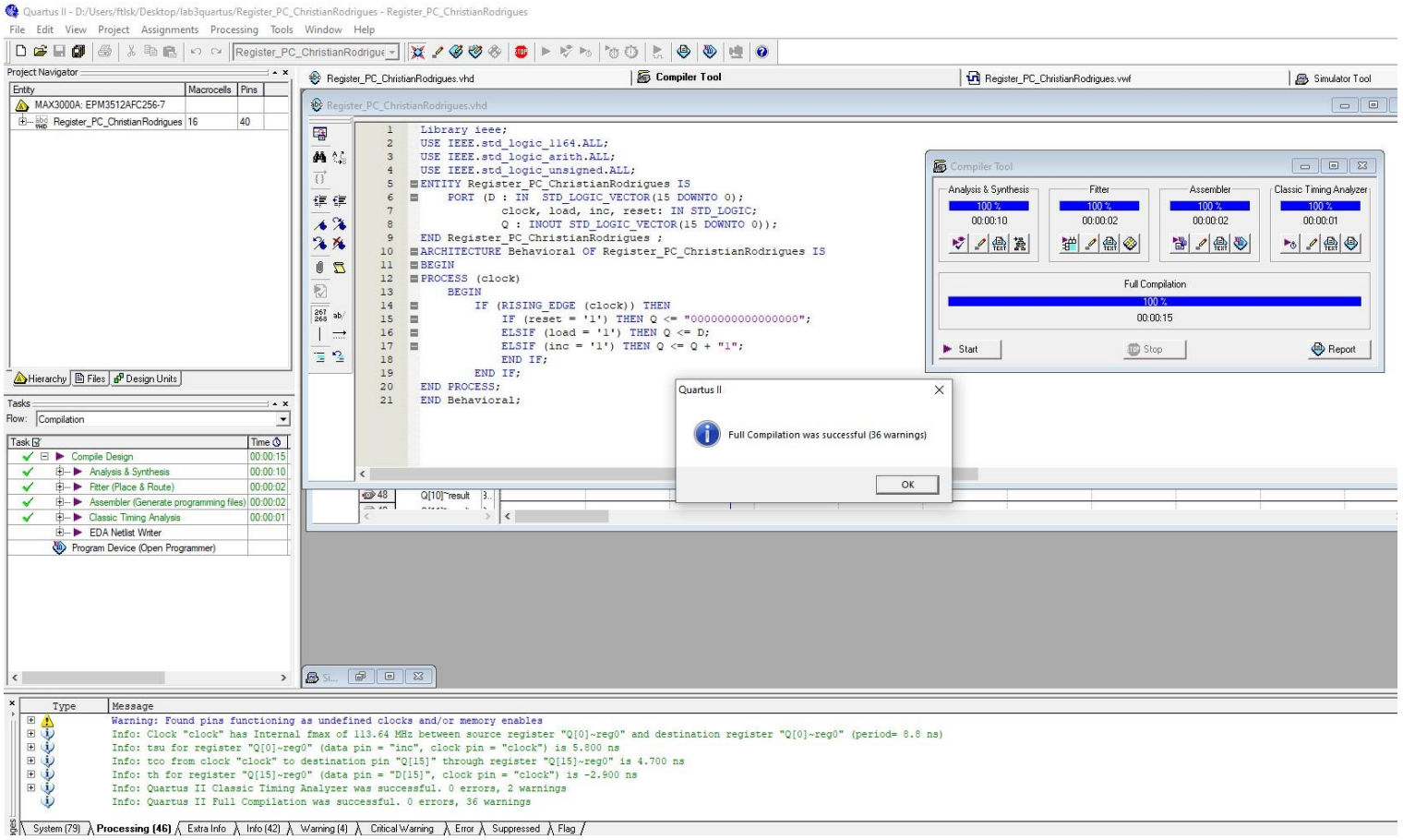
```
1   Library ieee;
2   USE IEEE.std_logic_1164.ALL;
3   ENTITY Register_16bit_ChristianRodrigues IS
4   PORT (D : IN    STD_LOGIC_VECTOR(15 DOWNTO 0);
5       clock, load : INOUT STD_LOGIC;
6       Q   : OUT STD_LOGIC_VECTOR(15 DOWNTO 0));
7   END Register_16bit_ChristianRodrigues ;
8   ARCHITECTURE Behaviorl OF Register_16bit_ChristianRodrigues IS
9   BEGIN
10      PROCESS (clock)
11      BEGIN
12          IF (RISING_EDGE (clock)) THEN
13              IF load = '1' THEN Q <= D;
14          END IF;
15          END IF;
16      END PROCESS;
17  END Behaviorl;
```

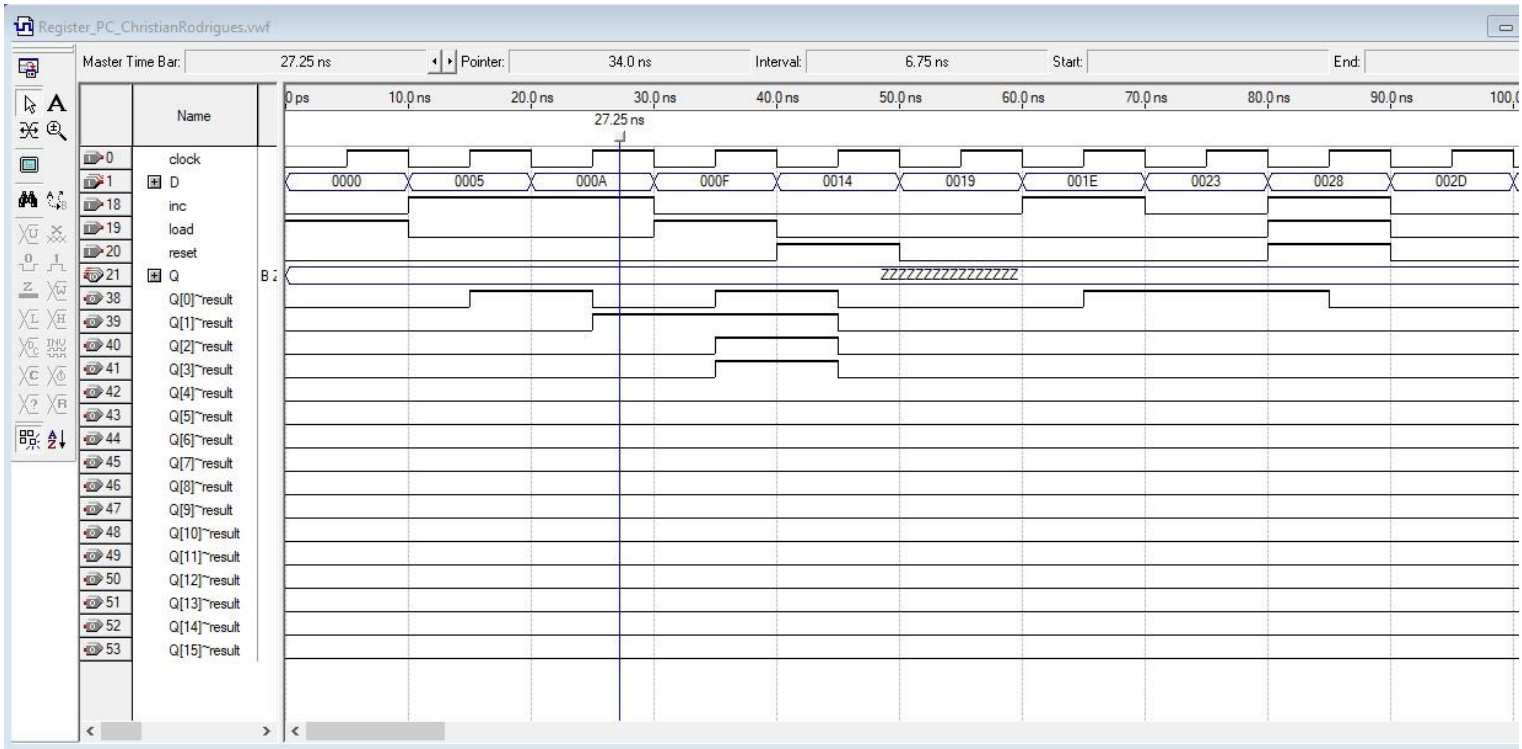

Quartus II - D:/Users/ftlsk/Desktop/lab3quartus/Register_16bit_ChristianRodrigues - Register_16bit_ChristianRodrigues
File Edit View Project Assignments Processing Tools Window Help
Project Navigator
Entity
Macrocells
Pins
MAX3000A: EPM3512AFC256-7
Register_16bit_ChristianRodrig...
18
38
Hierarchy
Files
Design Units
Tasks
Flow:
Compilation
Task
Time
Compile Design
Analysis & Synthesis
Fitter (Place & Route)
Assembler (Generate programming files)
Classic Timing Analysis
EDA Netlist Writer
Program Device (Open Programmer)
00:00:06
00:00:02
00:00:01
00:00:02
00:00:01
Register_16bit_ChristianRodrigues.vhd
Compiler Tool
1 Library ieee;
2 USE IEEE.std_logic_1164.ALL;
3 ENTITY Register_16bit_ChristianRodrigues IS
4 PORT (D : IN STD_LOGIC_VECTOR(15 DOWNTO 0);
5 clock, load : INOUT STD_LOGIC;
6 Q : OUT STD_LOGIC_VECTOR(15 DOWNTO 0));
7 END Register_16bit_ChristianRodrigues ;
8 ARCHITECTURE Behavior1 OF Register_16bit_ChristianRodrigues IS
9 BEGIN
10 PROCESS (clock)
11 BEGIN
12 IF (RISING_EDGE (clock)) THEN
13 IF load = '1' THEN Q <= D;
14 END IF;
15 END IF;
16 END PROCESS;
17 END Behavior1;
Analysis & Synthesis
Fitter
Assembler
Classic Timing Analyzer
100 %
00:00:02
00:00:01
00:00:02
00:00:01
Full Compilation
100 %
00:00:06
Start
Stop
Report
Quartus II
Full Compilation was successful (5 warnings)
OK
Type
Message
Warning: Found pins functioning as undefined clocks and/or memory enables
Info: Clock "clock" has Internal fmax of 116.28 MHz between source register "Q[0]~reg0" and destination register "Q[0]~reg0" (period= 8.6 ns)
Info: tsu for register "Q[0]~reg0" (data pin = "load", clock pin = "clock") is 2.500 ns
Info: tco from clock "clock" to destination pin "Q[15]" through register "Q[15]~reg0" is 8.000 ns
Info: th for register "Q[15]~reg0" (data pin = "D[15]", clock pin = "clock") is 0.400 ns
Info: Quartus II Classic Timing Analyzer was successful. 0 errors, 2 warnings
Info: Quartus II Full Compilation was successful. 0 errors, 5 warnings
System (10)
Processing (33)
Extra Info
Info (30)
Warning (3)
Critical Warning
Error
Suppressed
Flag


Register_16bit_ChristianRodrigues.vwf
Master Time Bar:
27.25 ns
Pointer:
2.7 ns
Interval:
-24.55 ns
Start:
0 ps
End:
0 ps
Name
0 clock
1 D
18 load
19 Q
0 ps
10.0 ns
20.0 ns
30.0 ns
40.0 ns
50.0 ns
60.0
27.25 ns
0000
0001
0002
0003
0004
0005
0000000000000000
0000000000000010
0000000000000011

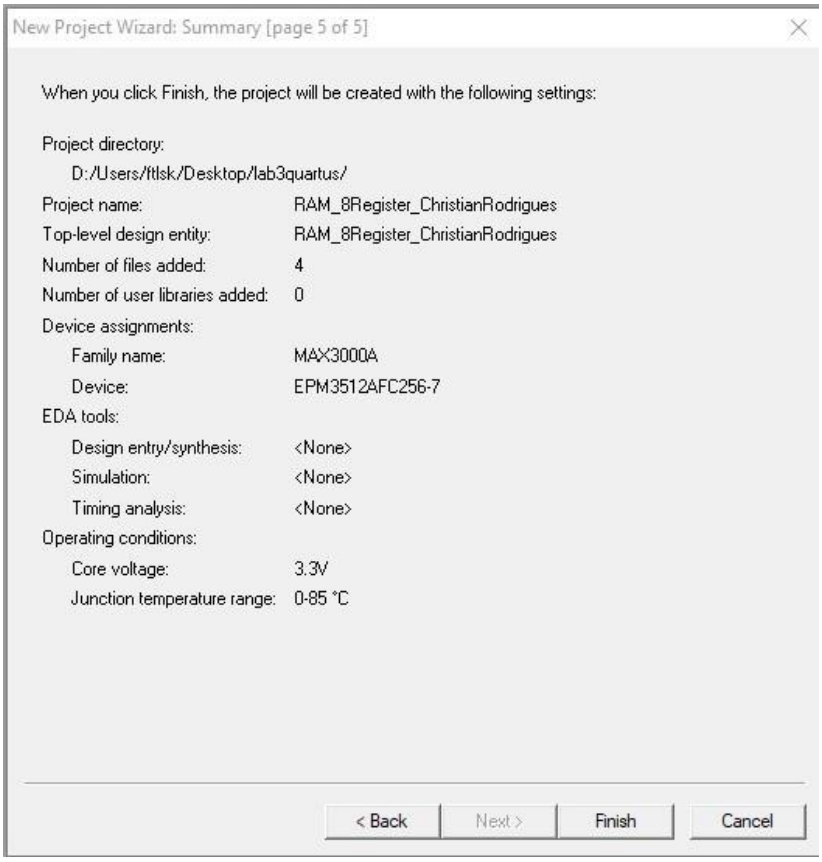
Program Counter




Quartus II - D:/Users/ftlsk/Desktop/lab3quartus/Register_PC_ChristianRodrigues - Register_PC_ChristianRodrigues
File Edit View Project Assignments Processing Tools Window Help
Project Navigator
Entity
MAX3000A: EPM3512AFC256-7
Register_PC_ChristianRodrigues
Hierarchy Files Design Units
Tasks
Flow: Compilation
Task
Time
Compile Design 00:00:15
Analysis & Synthesis 00:00:10
Fitter (Place & Route) 00:00:02
Assembler (Generate programming files) 00:00:02
Classic Timing Analysis 00:00:01
EDA Netlist Writer
Program Device (Open Programmer)
Register_PC_ChristianRodrigues.vhd
Compiler Tool
Register_PC_ChristianRodrigues.vwf
Simulator Tool
Library ieee;
USE IEEE.std_logic_1164.ALL;
USE IEEE.std_logic_arith.ALL;
USE IEEE.std_logic_unsigned.ALL;
ENTITY Register_PC_ChristianRodrigues IS
PORT (D : IN STD_LOGIC_VECTOR(15 DOWNTO 0);
clock, load, inc, reset: IN STD_LOGIC;
Q : INOUT STD_LOGIC_VECTOR(15 DOWNTO 0));
END Register_PC_ChristianRodrigues ;
ARCHITECTURE Behavioral OF Register_PC_ChristianRodrigues IS
BEGIN
PROCESS (clock)
BEGIN
IF (RISING_EDGE (clock)) THEN
IF (reset = '1') THEN Q <= "0000000000000000";
ELSIF (load = '1') THEN Q <= D;
ELSIF (inc = '1') THEN Q <= Q + "1";
END IF;
END IF;
END PROCESS;
END Behavioral;
Compiler Tool
Analysis & Synthesis
Fitter
Assembler
Classic Timing Analyzer
100 %
00:00:10
00:00:02
00:00:02
00:00:01
Full Compilation
00:00:15
Start
Stop
Report
Quartus II
Full Compilation was successful (36 warnings)
OK
Type
Message
Warning: Found pins functioning as undefined clocks and/or memory enables
Info: Clock "clock" has Internal fmax of 113.64 MHz between source register "Q[0]~reg0" and destination register "Q[0]~reg0" (period= 8.8 ns)
Info: tsu for register "Q[0]~reg0" (data pin = "inc", clock pin = "clock") is 5.800 ns
Info: tco from clock "clock" to destination pin "Q[15]" through register "Q[15]~reg0" is 4.700 ns
Info: th for register "Q[15]~reg0" (data pin = "D[15]", clock pin = "clock") is -2.900 ns
Info: Quartus II Classic Timing Analyzer was successful. 0 errors, 2 warnings
Info: Quartus II Full Compilation was successful. 0 errors, 36 warnings
System (79) Processing (46) Extra Info Info (42) Warning (4) Critical Warning Error Suppressed Flag

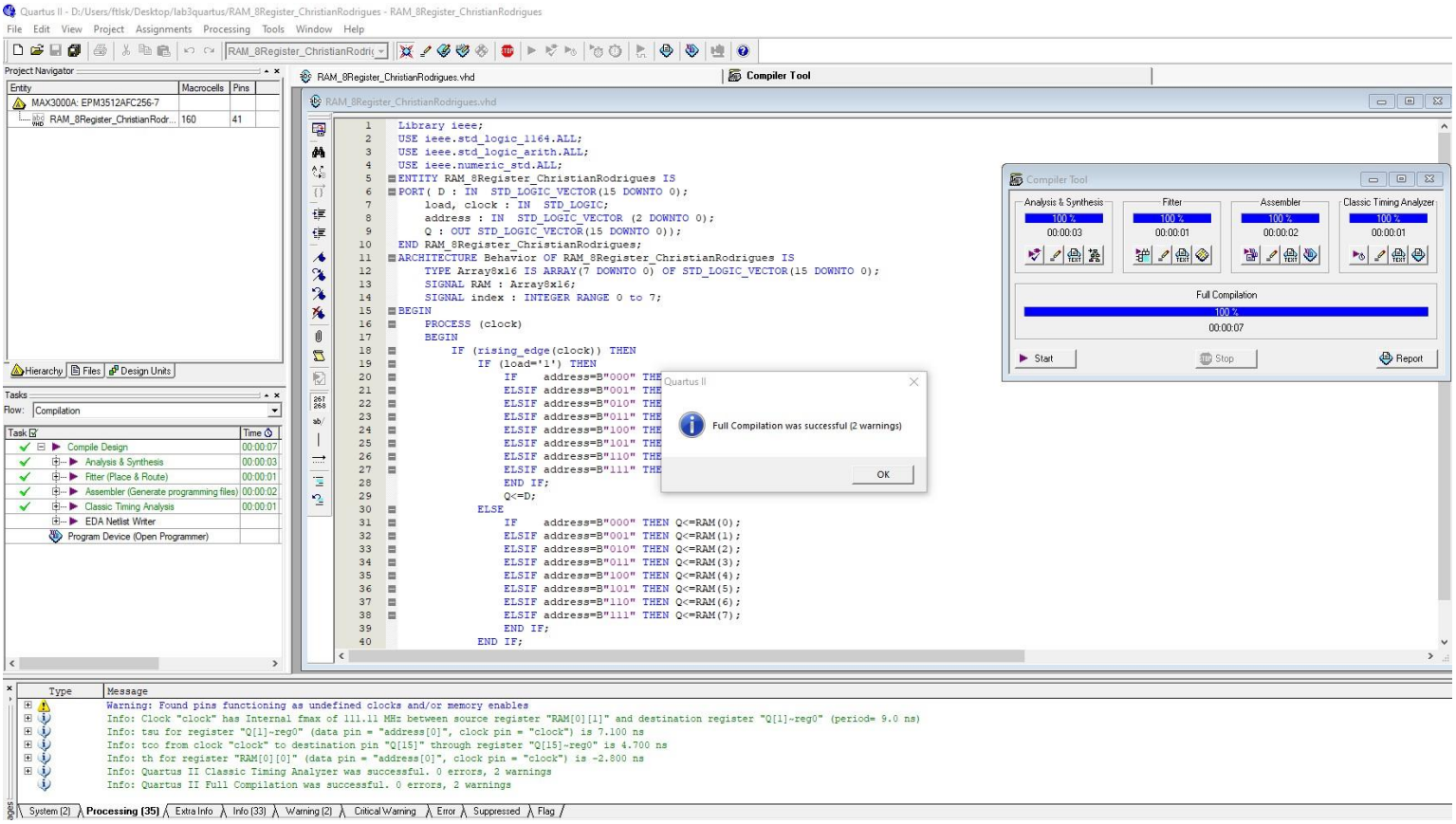

Register_PC_ChristianRodrigues.vwf
Master Time Bar: 27.25 ns
Pointer: 34.0 ns
Interval: 6.75 ns
Start:
End:
Name
0 clock
1 D
18 inc
19 load
20 reset
21 Q
38 Q[0]~result
39 Q[1]~result
40 Q[2]~result
41 Q[3]~result
42 Q[4]~result
43 Q[5]~result
44 Q[6]~result
45 Q[7]~result
46 Q[8]~result
47 Q[9]~result
48 Q[10]~result
49 Q[11]~result
50 Q[12]~result
51 Q[13]~result
52 Q[14]~result
53 Q[15]~result
0 ps
10.0 ns
20.0 ns
30.0 ns
40.0 ns
50.0 ns
60.0 ns
70.0 ns
80.0 ns
90.0 ns
27.25 ns
0000
0005
000A
000F
0014
0019
001E
0023
0028
002D
ZZZZZZZZZZZZZZZZ

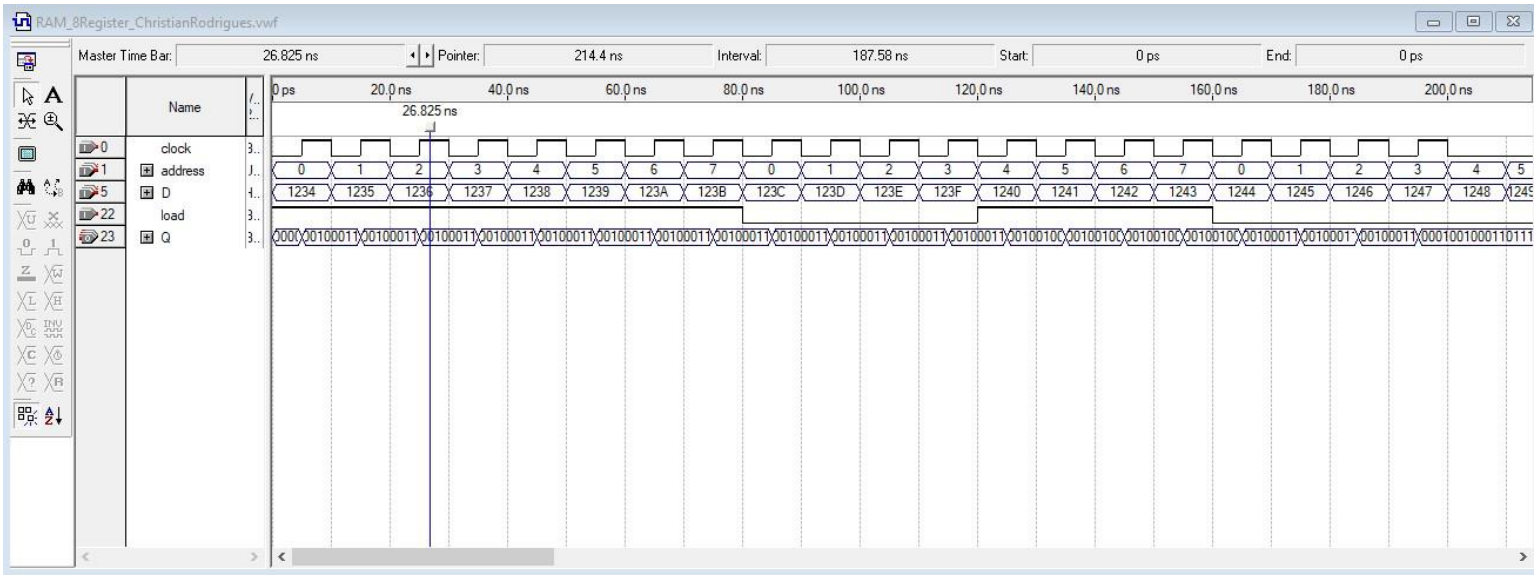
RAM with 8 Registers



RAM_8Register_ChristianRodrigues.vhd

```
 1  Library ieee;
 2  USE ieee.std_logic_1164.ALL;
 3  USE ieee.std_logic_arith.ALL;
 4  USE ieee.numeric_std.ALL;
 5  ENTITY RAM_8Register_ChristianRodrigues IS
 6  PORT( D : IN  STD_LOGIC_VECTOR(15 DOWNTO 0);
 7        load, clock : IN  STD_LOGIC;
 8        address : IN  STD_LOGIC_VECTOR (2 DOWNTO 0);
 9        Q : OUT STD_LOGIC_VECTOR(15 DOWNTO 0));
10  END RAM_8Register_ChristianRodrigues;
11  ARCHITECTURE Behavior OF RAM_8Register_ChristianRodrigues IS
12      TYPE Array8x16 IS ARRAY(7 DOWNTO 0) OF STD_LOGIC_VECTOR(15 DOWNTO 0);
13      SIGNAL RAM : Array8x16;
14      SIGNAL index : INTEGER RANGE 0 to 7;
15  BEGIN
16      PROCESS (clock)
17      BEGIN
18          IF (rising_edge(clock)) THEN
19              IF (load='1') THEN
20                  IF    address=B"000" THEN RAM(0)<=D;
21                  ELSIF address=B"001" THEN RAM(1)<=D;
22                  ELSIF address=B"010" THEN RAM(2)<=D;
23                  ELSIF address=B"011" THEN RAM(3)<=D;
24                  ELSIF address=B"100" THEN RAM(4)<=D;
25                  ELSIF address=B"101" THEN RAM(5)<=D;
26                  ELSIF address=B"110" THEN RAM(6)<=D;
27                  ELSIF address=B"111" THEN RAM(7)<=D;
28                  END IF;
29                  Q<=D;
30              ELSE
31                  IF    address=B"000" THEN Q<=RAM(0);
32                  ELSIF address=B"001" THEN Q<=RAM(1);
33                  ELSIF address=B"010" THEN Q<=RAM(2);
34                  ELSIF address=B"011" THEN Q<=RAM(3);
35                  ELSIF address=B"100" THEN Q<=RAM(4);
36                  ELSIF address=B"101" THEN Q<=RAM(5);
37                  ELSIF address=B"110" THEN Q<=RAM(6);
38                  ELSIF address=B"111" THEN Q<=RAM(7);
39                  END IF;
40              END IF;
41          END IF;
42      END PROCESS;
43  END Behavior;
```


Quartus II - D:/Users/ftlsk/Desktop/lab3quartus/RAM_8Register_ChristianRodrigues - RAM_8Register_ChristianRodrigues
File Edit View Project Assignments Processing Tools Window Help
Project Navigator
Entity
Macrocells
Pins
MAX3000A: EPM3512AFC256-7
RAM_8Register_ChristianRodr...
160
41
Hierarchy
Files
Design Units
Tasks
Flow:
Compilation
Task
Time
Compile Design 00:00:07
Analysis & Synthesis 00:00:03
Fitter (Place & Route) 00:00:01
Assembler (Generate programming files) 00:00:02
Classic Timing Analysis 00:00:01
EDA Netlist Writer
Program Device (Open Programmer)
RAM_8Register_ChristianRodrigues.vhd
Compiler Tool
Library ieee;
USE ieee.std_logic_1164.ALL;
USE ieee.std_logic_arith.ALL;
USE ieee.numeric_std.ALL;
ENTITY RAM_8Register_ChristianRodrigues IS
PORT(D : IN STD_LOGIC_VECTOR(15 DOWNTO 0);
load, clock : IN STD_LOGIC;
address : IN STD_LOGIC_VECTOR (2 DOWNTO 0);
Q : OUT STD_LOGIC_VECTOR(15 DOWNTO 0));
END RAM_8Register_ChristianRodrigues;
ARCHITECTURE Behavior OF RAM_8Register_ChristianRodrigues IS
TYPE Array8x16 IS ARRAY(7 DOWNTO 0) OF STD_LOGIC_VECTOR(15 DOWNTO 0);
SIGNAL RAM : Array8x16;
SIGNAL index : INTEGER RANGE 0 to 7;
BEGIN
PROCESS (clock)
BEGIN
IF (rising_edge(clock)) THEN
IF (load='1') THEN
IF address=B"000" THE
ELSIF address=B"001" THE
ELSIF address=B"010" THE
ELSIF address=B"011" THE
ELSIF address=B"100" THE
ELSIF address=B"101" THE
ELSIF address=B"110" THE
ELSIF address=B"111" THE
END IF;
Q<=D;
ELSE
IF address=B"000" THEN Q<=RAM(0);
ELSIF address=B"001" THEN Q<=RAM(1);
ELSIF address=B"010" THEN Q<=RAM(2);
ELSIF address=B"011" THEN Q<=RAM(3);
ELSIF address=B"100" THEN Q<=RAM(4);
ELSIF address=B"101" THEN Q<=RAM(5);
ELSIF address=B"110" THEN Q<=RAM(6);
ELSIF address=B"111" THEN Q<=RAM(7);
END IF;
END IF;
Quartus II
Full Compilation was successful (2 warnings)
OK
Compiler Tool
Analysis & Synthesis
Fitter
Assembler
Classic Timing Analyzer
100 %
00:00:03
00:00:01
00:00:02
00:00:01
Full Compilation
00:00:07
Start
Stop
Report
Type
Message
Warning: Found pins functioning as undefined clocks and/or memory enables
Info: Clock "clock" has Internal fmax of 111.11 MHz between source register "RAM[0][1]" and destination register "Q[1]~reg0" (period= 9.0 ns)
Info: tsu for register "Q[1]~reg0" (data pin = "address[0]", clock pin = "clock") is 7.100 ns
Info: tco from clock "clock" to destination pin "Q[15]" through register "Q[15]~reg0" is 4.700 ns
Info: th for register "RAM[0][0]" (data pin = "address[0]", clock pin = "clock") is -2.800 ns
Info: Quartus II Classic Timing Analyzer was successful. 0 errors, 2 warnings
Info: Quartus II Full Compilation was successful. 0 errors, 2 warnings
System (2)
Processing (35)
Extra Info
Info (33)
Warning (2)
Critical Warning
Error
Suppressed
Flag


RAM_8Register_ChristianRodrigues.vwf
Master Time Bar: 26.825 ns
Pointer: 214.4 ns
Interval: 187.58 ns
Start: 0 ps
End: 0 ps
Name
0 clock
1 address
5 D
22 load
23 Q
0 ps
20.0 ns
40.0 ns
60.0 ns
80.0 ns
100.0 ns
120.0 ns
140.0 ns
160.0 ns
180.0 ns
200.0 ns
26.825 ns
0 1 2 3 4 5 6 7 0 1 2 3 4 5 6 7 0 1 2 3 4 5
1234 1235 1236 1237 1238 1239 123A 123B 123C 123D 123E 123F 1240 1241 1242 1243 1244 1245 1246 1247 1248