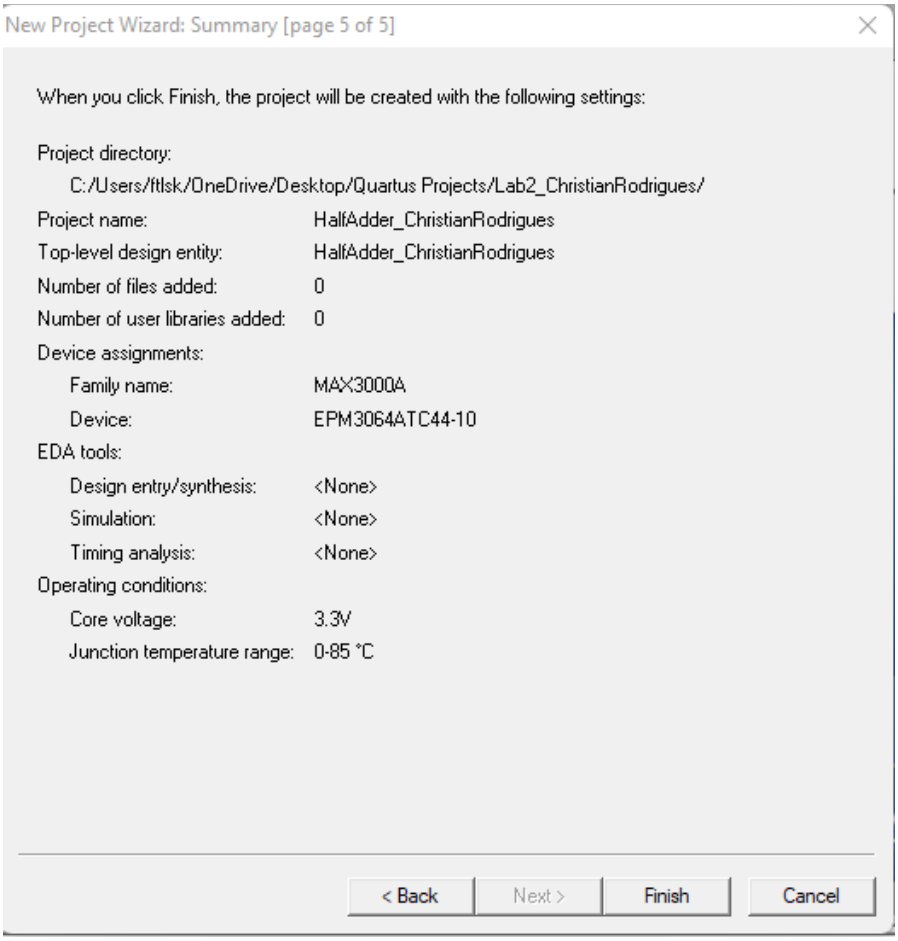
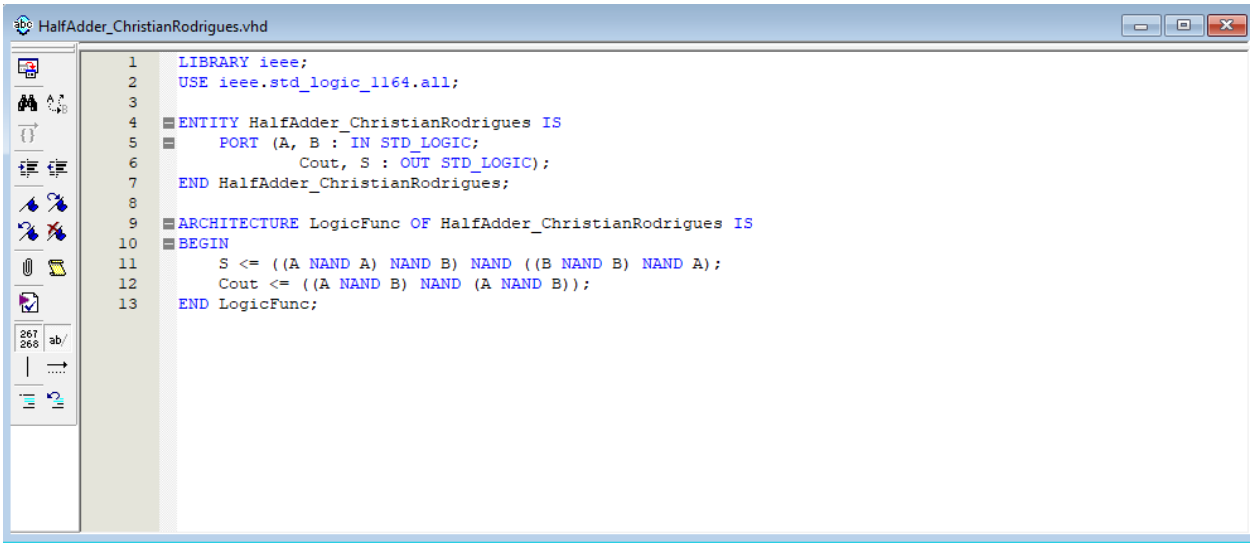
LAB2

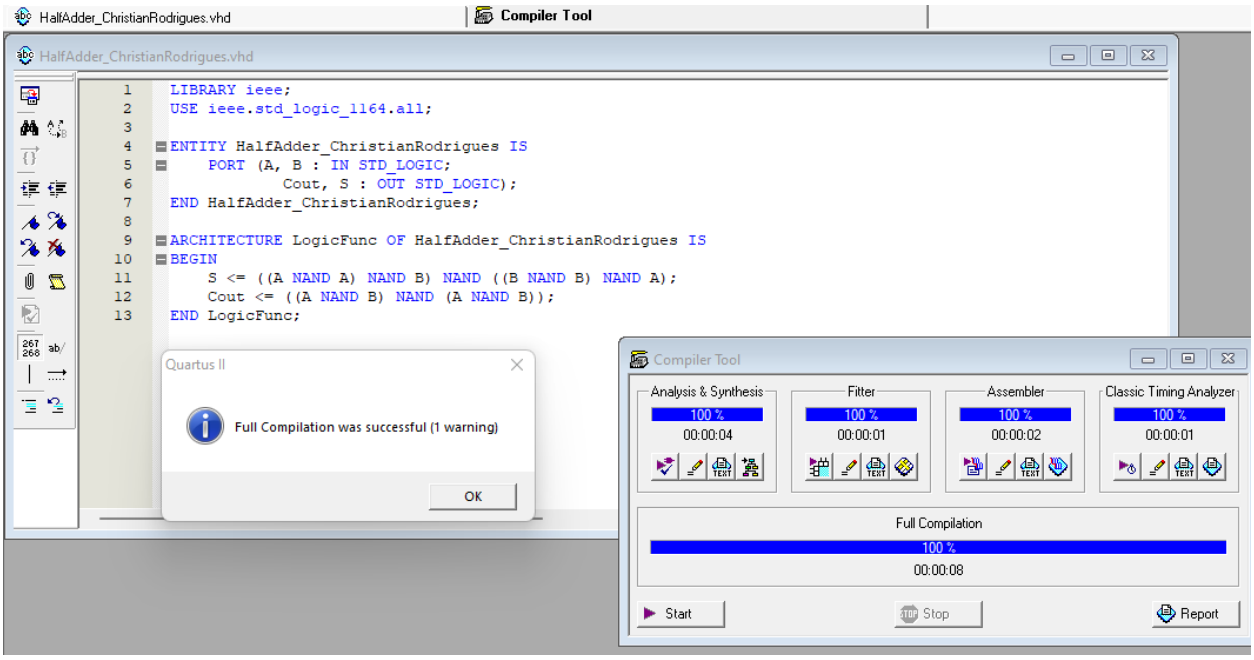
Christian Rodrigues –
Petrie CDA3203 –
11/3/2022

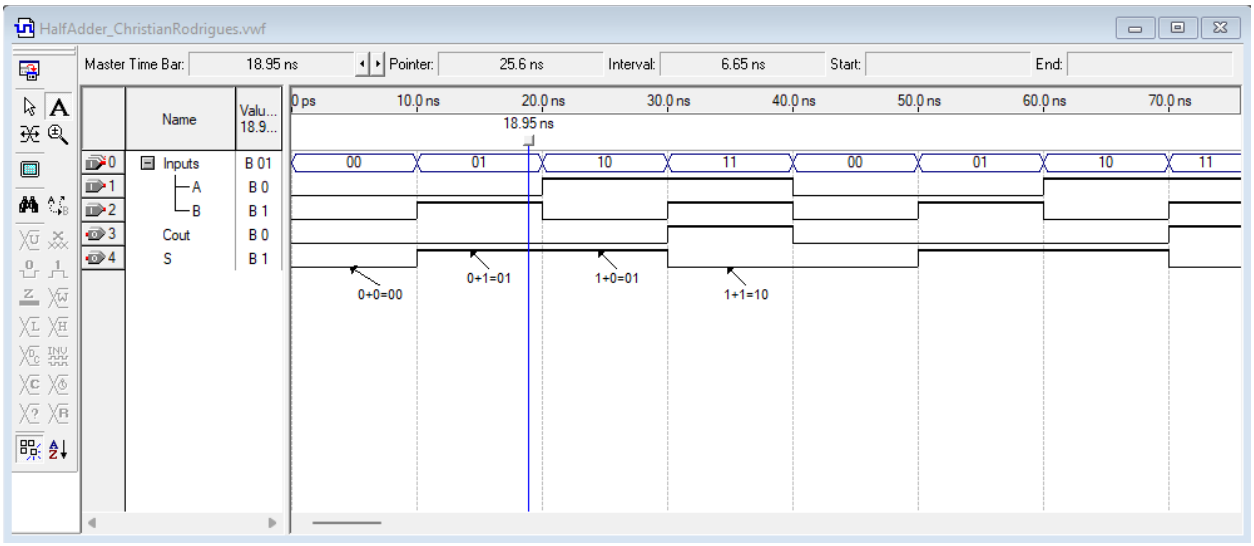
The purpose of this lab is to create a half adder and full adder to perform arithmetic on binary numbers. They will then be utilized as components to create a 4-bit, 8-bit, and 16-bit adder.

Half Adder


New Project Wizard: Summary [page 5 of 5]
When you click Finish, the project will be created with the following settings:
Project directory:
C:/Users/ftlsk/OneDrive/Desktop/Quartus Projects/Lab2_ChristianRodrigues/
Project name: HalfAdder_ChristianRodrigues
Top-level design entity: HalfAdder_ChristianRodrigues
Number of files added: 0
Number of user libraries added: 0
Device assignments:
Family name: MAX3000A
Device: EPM3064ATC44-10
EDA tools:
Design entry/synthesis: <None>
Simulation: <None>
Timing analysis: <None>
Operating conditions:
Core voltage: 3.3V
Junction temperature range: 0-85 °C
< Back
Next >
Finish
Cancel


HalfAdder_ChristianRodrigues.vhd
1 LIBRARY ieee;
2 USE ieee.std_logic_1164.all;
3
4 ENTITY HalfAdder_ChristianRodrigues IS
5 PORT (A, B : IN STD_LOGIC;
6 Cout, S : OUT STD_LOGIC);
7 END HalfAdder_ChristianRodrigues;
8
9 ARCHITECTURE LogicFunc OF HalfAdder_ChristianRodrigues IS
10 BEGIN
11 S <= ((A NAND A) NAND B) NAND ((B NAND B) NAND A);
12 Cout <= ((A NAND B) NAND (A NAND B));
13 END LogicFunc;


HalfAdder_ChristianRodrigues.vhd
Compiler Tool
HalfAdder_ChristianRodrigues.vhd
1 LIBRARY ieee;
2 USE ieee.std_logic_1164.all;
3
4 ENTITY HalfAdder_ChristianRodrigues IS
5 PORT (A, B : IN STD_LOGIC;
6 Cout, S : OUT STD_LOGIC);
7 END HalfAdder_ChristianRodrigues;
8
9 ARCHITECTURE LogicFunc OF HalfAdder_ChristianRodrigues IS
10 BEGIN
11 S <= ((A NAND A) NAND B) NAND ((B NAND B) NAND A);
12 Cout <= ((A NAND B) NAND (A NAND B));
13 END LogicFunc;
Quartus II
Full Compilation was successful (1 warning)
OK
Compiler Tool
Analysis & Synthesis
100 %
00:00:04
Fitter
100 %
00:00:01
Assembler
100 %
00:00:02
Classic Timing Analyzer
100 %
00:00:01
Full Compilation
100 %
00:00:08
Start
Stop
Report


HalfAdder_ChristianRodrigues.vwf
Master Time Bar: 18.95 ns
Pointer: 25.6 ns
Interval: 6.65 ns
Start:
End:
Name
Valu... 18.9...
Inputs
A
B
Cout
S
B 01
B 0
B 1
B 0
B 1
0 ps
10.0 ns
20.0 ns
30.0 ns
40.0 ns
50.0 ns
60.0 ns
70.0 ns
18.95 ns
00
01
10
11
00
01
10
11
0+0=00
0+1=01
1+0=01
1+1=10

Christian Rodrigues

Lab 2

Half Adder

Truth Table

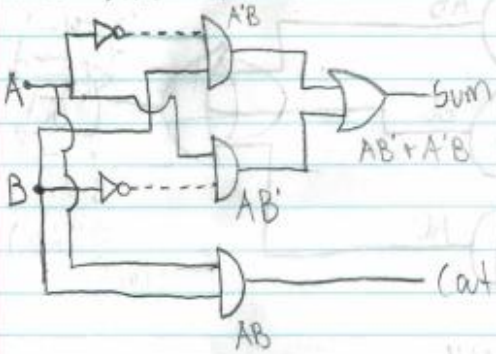
A	B	Cout	Sum
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

Kmap

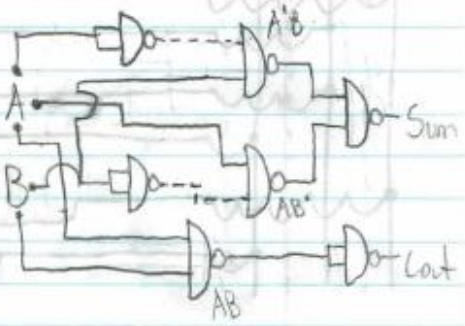
Sum SOP = $AB' + A'B$

Cout SOP = AB

NOT-AND-OR Circuit:



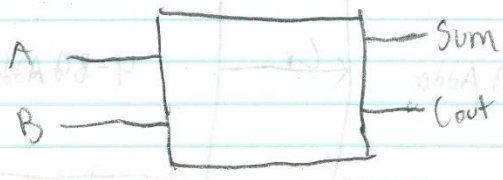
NAND Circuit



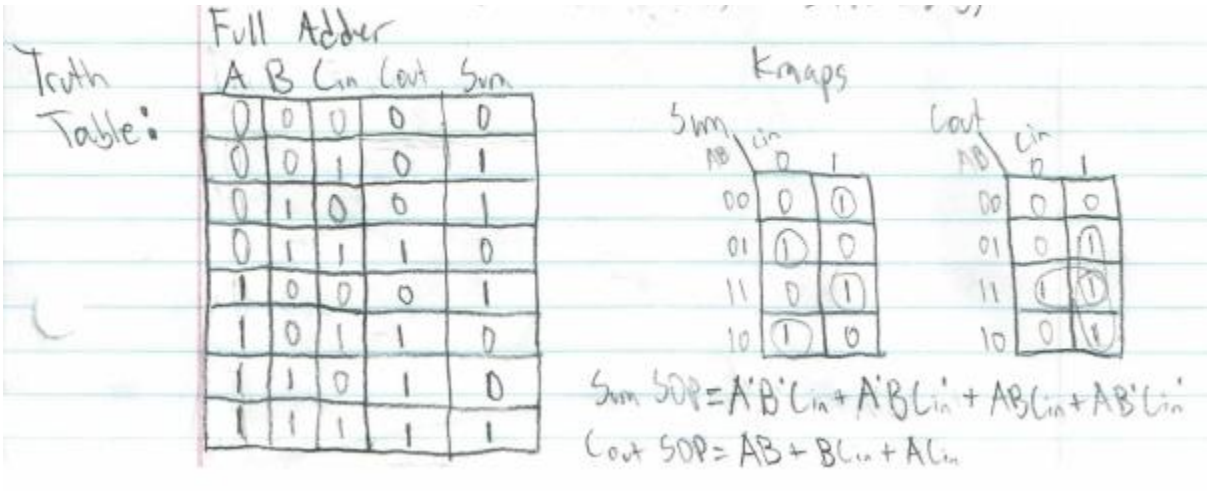
Sum = ((A NAND A) NAND B) NAND ((B NAND B) NAND A)

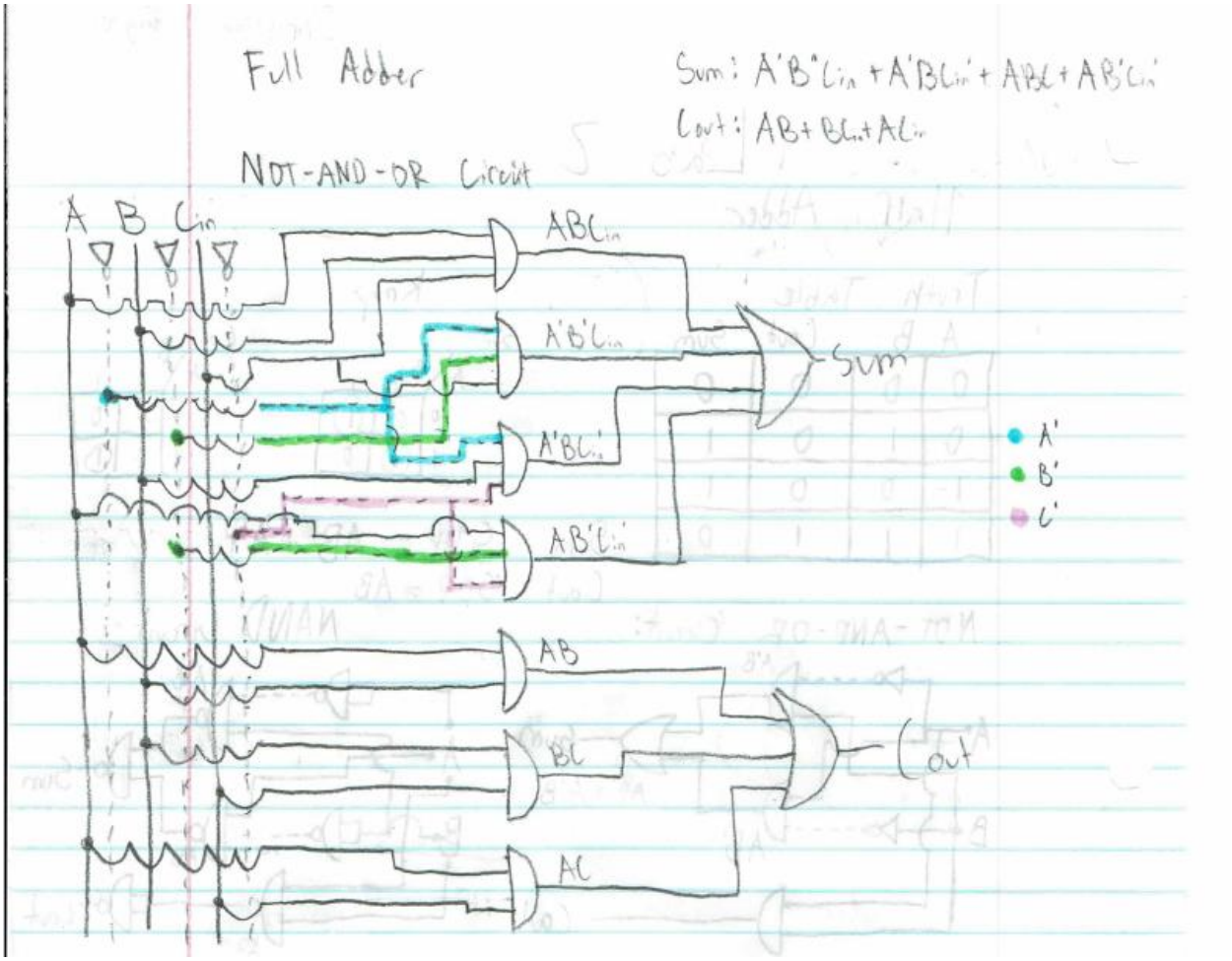
Cout = (A NAND B) NAND (A NAND B)

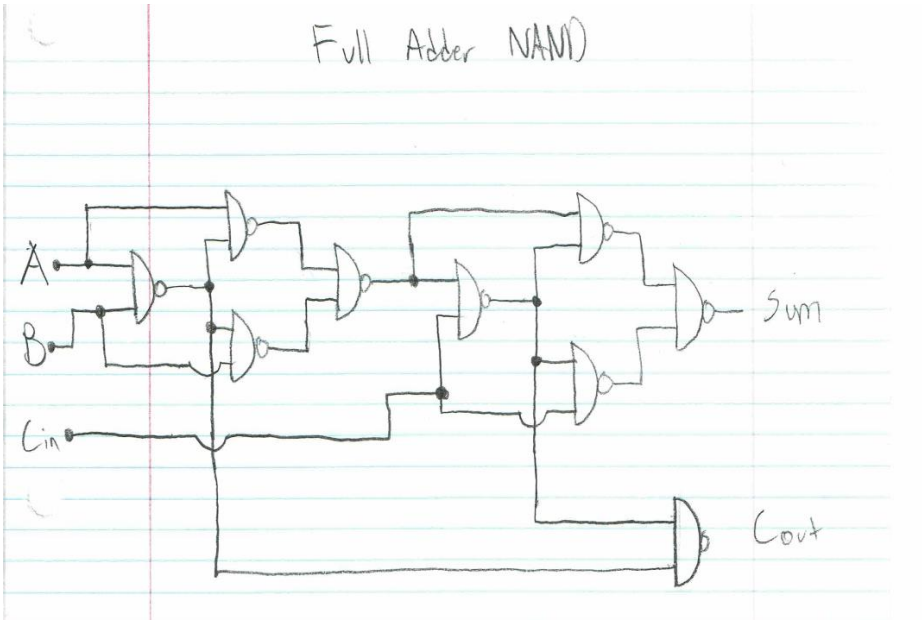
Half Adder



Full Adder


Full Adder
Truth Table:
A B Cin Cout Sum
Karnaps
Sum
AB \ Cin
Cout
AB \ Cin
Sum SOP = A'B'Cin + A'BCin' + ABCin + AB'Cin'
Cout SOP = AB + BCin + ACin


Full Adder
NOT-AND-OR Circuit
Sum: A'B'Cin + A'BCin' + ABCin + AB'Cin'
Cout: AB + BCin + ACin
A B Cin
ABCin
A'B'Cin
A'BCin'
AB'Cin'
Sum
AB
BC
AC
Cout
A'
B'
C'



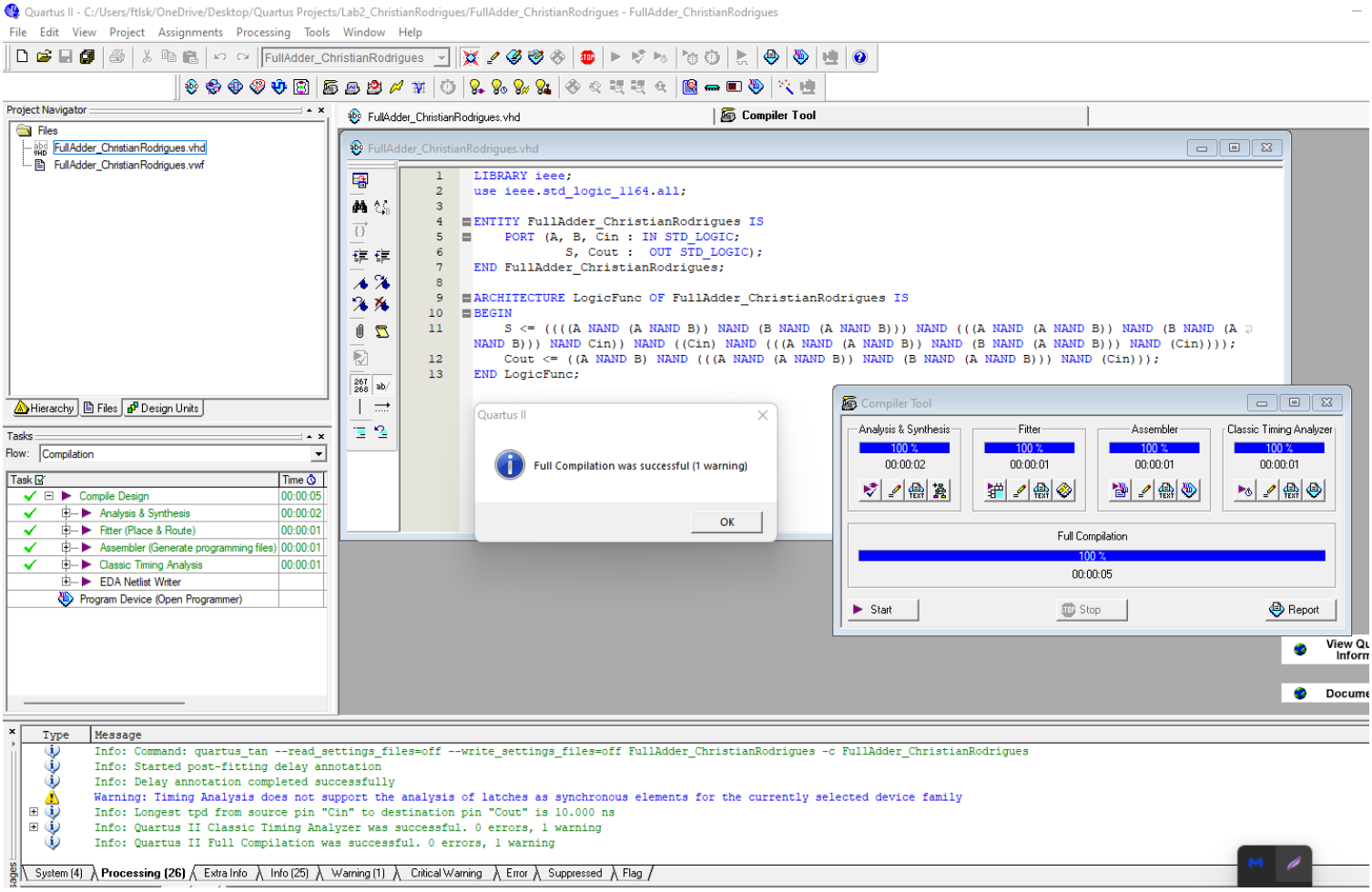
New Project Wizard: Summary [page 5 of 5]

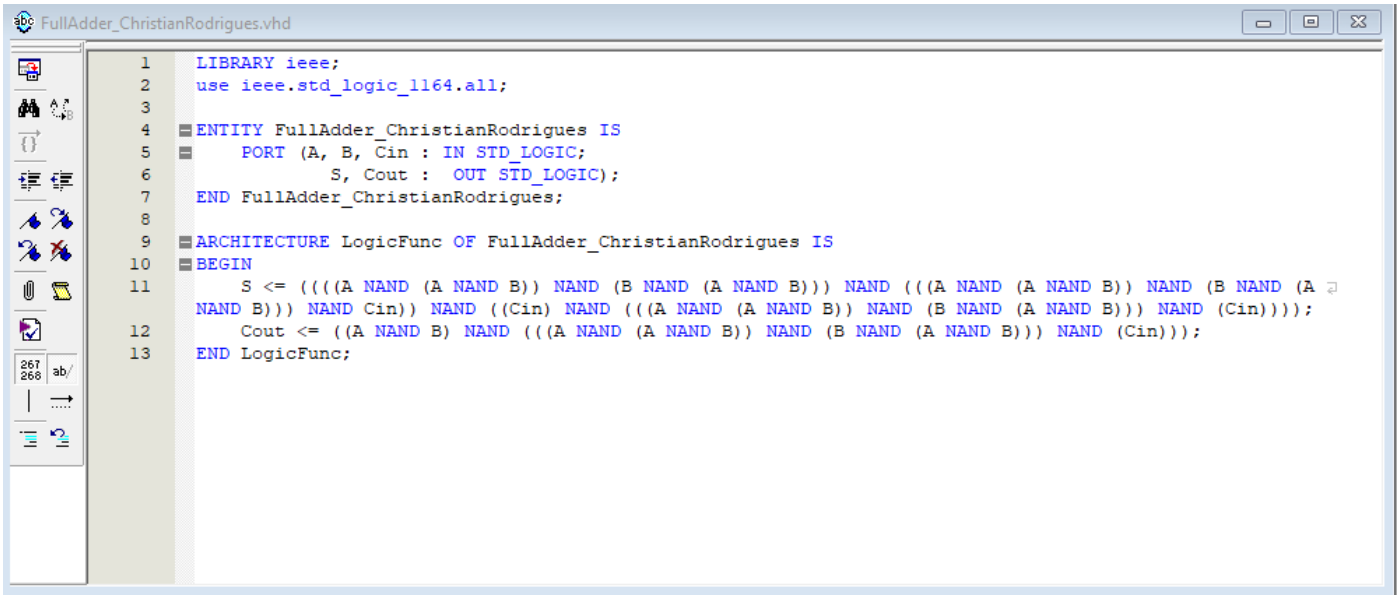
When you click Finish, the project will be created with the following settings:

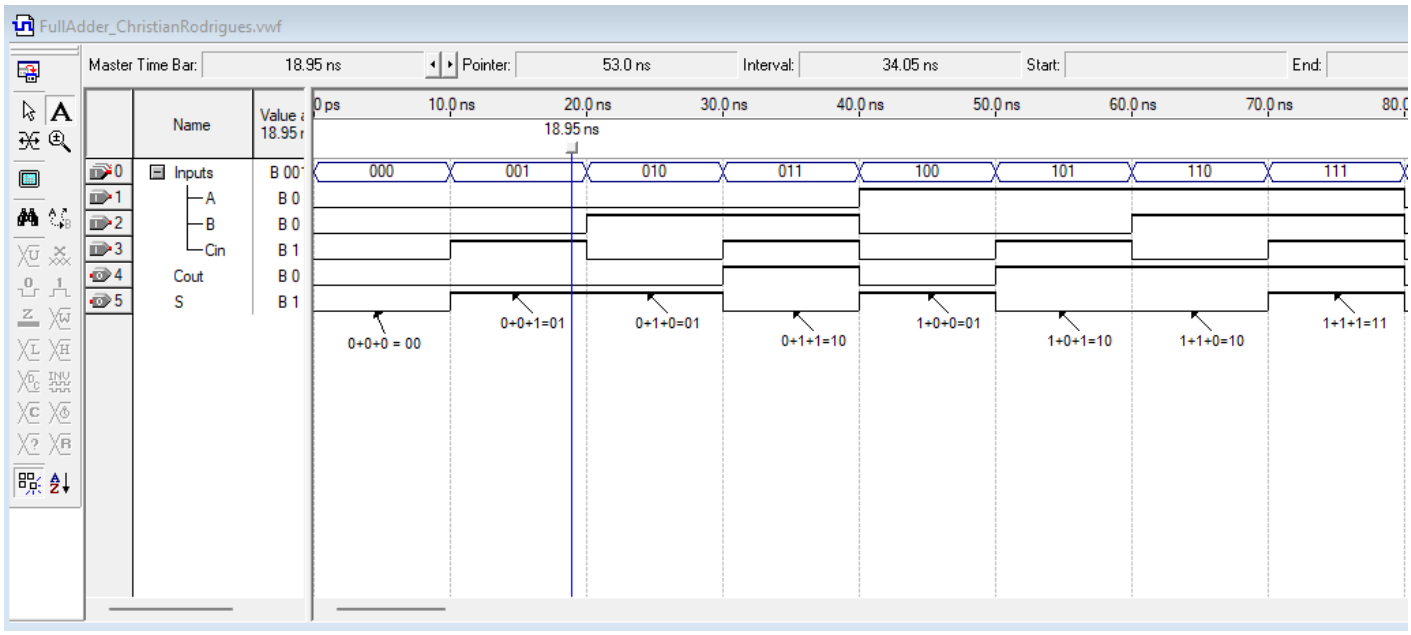
Project directory:
C:/Users/ftlsk/OneDrive/Desktop/Quartus Projects/Lab2_ChristianRodrigues/

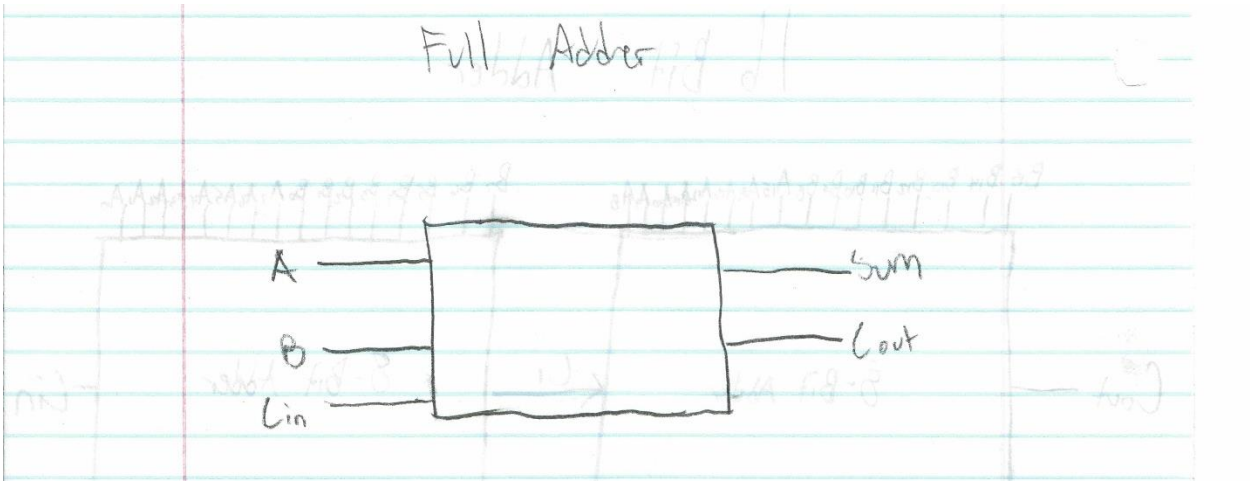
Project name:	FullAdder_ChristianRodrigues
Top-level design entity:	FullAdder_ChristianRodrigues
Number of files added:	0
Number of user libraries added:	0
Device assignments:	
Family name:	MAX3000A
Device:	EPM3064ATC44-10
EDA tools:	
Design entry/synthesis:	<None>
Simulation:	<None>
Timing analysis:	<None>
Operating conditions:	
Core voltage:	3.3V
Junction temperature range:	0-85 °C

< Back | Next > | Finish | Cancel

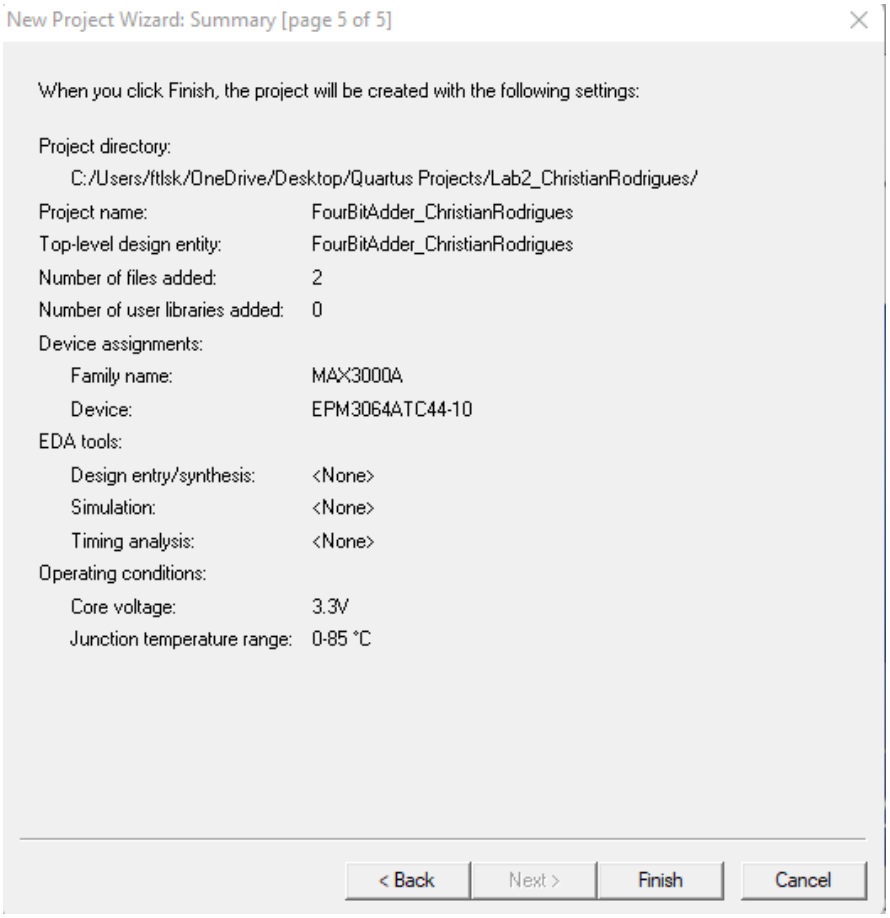

Quartus II - C:/Users/ftlsk/OneDrive/Desktop/Quartus Projects/Lab2_ChristianRodrigues/FullAdder_ChristianRodrigues - FullAdder_ChristianRodrigues
File Edit View Project Assignments Processing Tools Window Help
Project Navigator
Files
FullAdder_ChristianRodrigues.vhd
FullAdder_ChristianRodrigues.vwf
Hierarchy Files Design Units
Tasks
Flow: Compilation
Task Time
Compile Design 00:00:05
Analysis & Synthesis 00:00:02
Fitter (Place & Route) 00:00:01
Assembler (Generate programming files) 00:00:01
Classic Timing Analysis 00:00:01
EDA Netlist Writer
Program Device (Open Programmer)
FullAdder_ChristianRodrigues.vhd
Compiler Tool
1 LIBRARY ieee;
2 use ieee.std_logic_1164.all;
3
4 ENTITY FullAdder_ChristianRodrigues IS
5 PORT (A, B, Cin : IN STD_LOGIC;
6 S, Cout : OUT STD_LOGIC);
7 END FullAdder_ChristianRodrigues;
8
9 ARCHITECTURE LogicFunc OF FullAdder_ChristianRodrigues IS
10 BEGIN
11 S <= ((((A NAND (A NAND B)) NAND (B NAND (A NAND B))) NAND (((A NAND (A NAND B)) NAND (B NAND (A NAND B))) NAND Cin)) NAND ((Cin) NAND (((A NAND (A NAND B)) NAND (B NAND (A NAND B))) NAND (Cin))));
12 Cout <= ((A NAND B) NAND (((A NAND (A NAND B)) NAND (B NAND (A NAND B))) NAND (Cin)));
13 END LogicFunc;
Quartus II
Full Compilation was successful (1 warning)
OK
Compiler Tool
Analysis & Synthesis 100 % 00:00:02
Fitter 100 % 00:00:01
Assembler 100 % 00:00:01
Classic Timing Analyzer 100 % 00:00:01
Full Compilation 100 % 00:00:05
Start Stop Report
Type Message
Info: Command: quartus_tan --read_settings_files=off --write_settings_files=off FullAdder_ChristianRodrigues -c FullAdder_ChristianRodrigues
Info: Started post-fitting delay annotation
Info: Delay annotation completed successfully
Warning: Timing Analysis does not support the analysis of latches as synchronous elements for the currently selected device family
Info: Longest tpd from source pin "Cin" to destination pin "Cout" is 10.000 ns
Info: Quartus II Classic Timing Analyzer was successful. 0 errors, 1 warning
Info: Quartus II Full Compilation was successful. 0 errors, 1 warning
System (4) Processing (26) Extra Info Info (25) Warning (1) Critical Warning Error Suppressed Flag

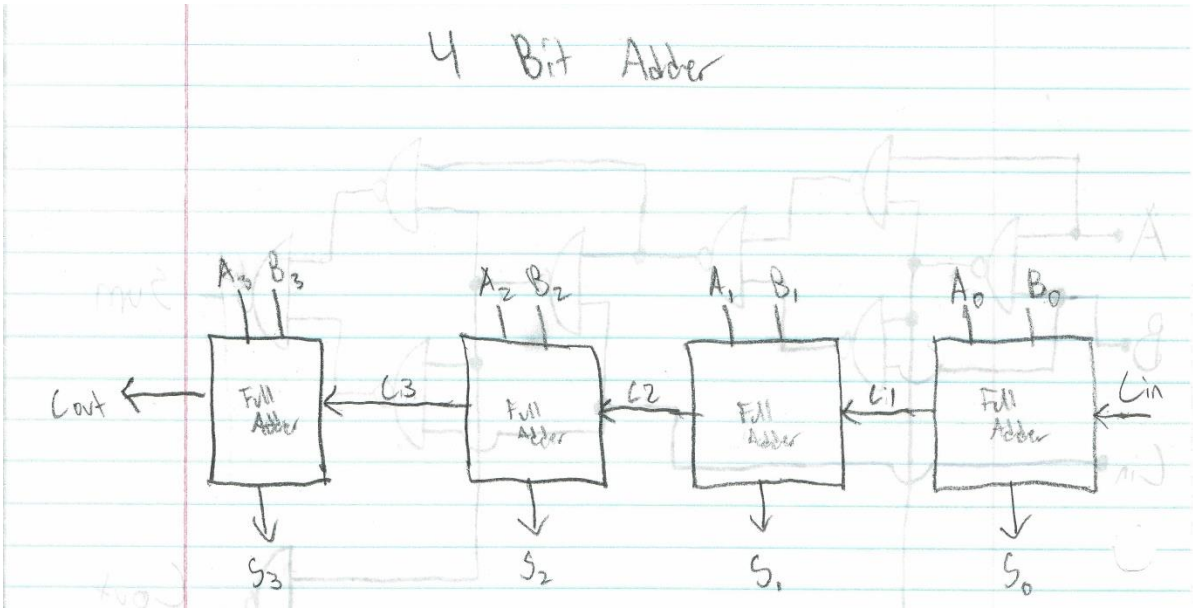

FullAdder_ChristianRodrigues.vhd
1 LIBRARY ieee;
2 use ieee.std_logic_1164.all;
3
4 ENTITY FullAdder_ChristianRodrigues IS
5 PORT (A, B, Cin : IN STD_LOGIC;
6 S, Cout : OUT STD_LOGIC);
7 END FullAdder_ChristianRodrigues;
8
9 ARCHITECTURE LogicFunc OF FullAdder_ChristianRodrigues IS
10 BEGIN
11 S <= ((((A NAND (A NAND B)) NAND (B NAND (A NAND B))) NAND (((A NAND (A NAND B)) NAND (B NAND (A NAND B))) NAND Cin)) NAND ((Cin) NAND (((A NAND (A NAND B)) NAND (B NAND (A NAND B))) NAND (Cin))));
12 Cout <= ((A NAND B) NAND (((A NAND (A NAND B)) NAND (B NAND (A NAND B))) NAND (Cin)));
13 END LogicFunc;


FullAdder_ChristianRodrigues.vwf
Master Time Bar: 18.95 ns
Pointer: 53.0 ns
Interval: 34.05 ns
Start:
End:
Name
Value
Inputs
A
B
Cin
Cout
S
000
001
010
011
100
101
110
111
0+0+0 = 00
0+0+1=01
0+1+0=01
0+1+1=10
1+0+0=01
1+0+1=10
1+1+0=10
1+1+1=11


Full Adder
A
B
Cin
Sum
Cout

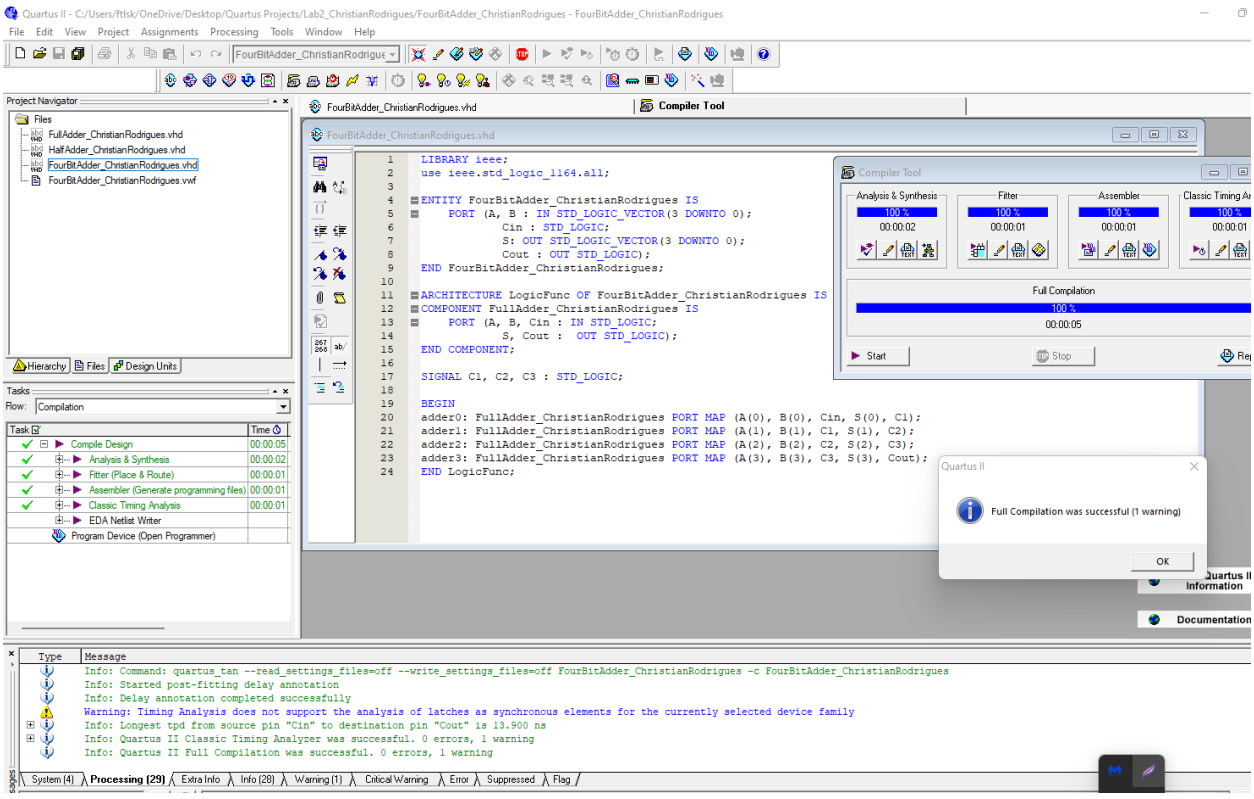
4-bit Adder

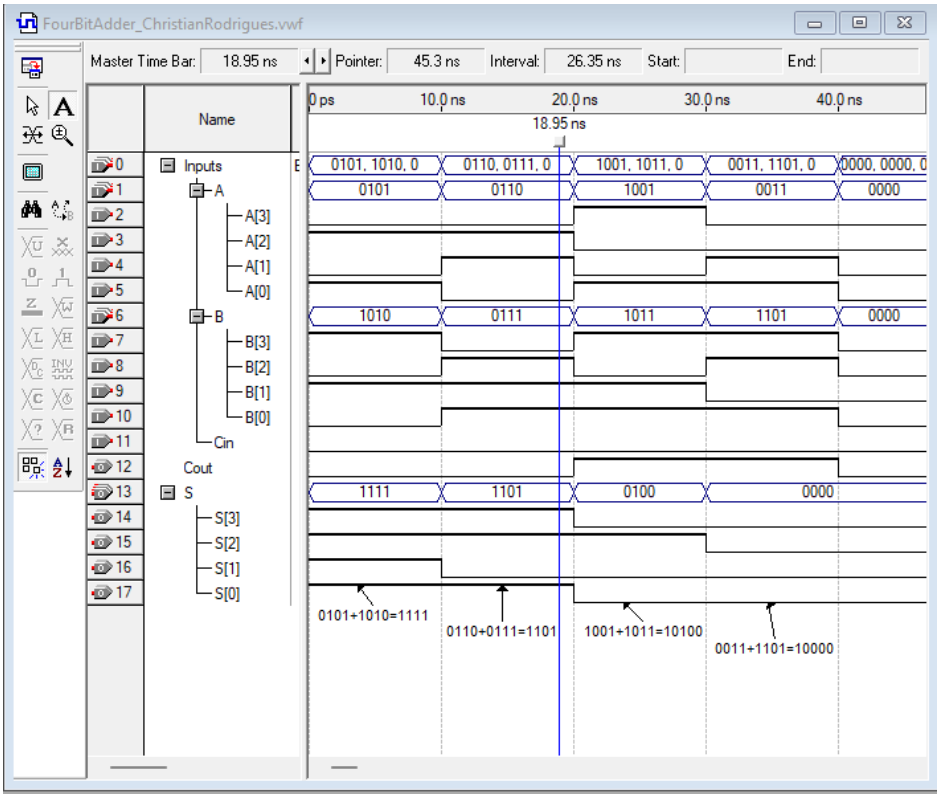

New Project Wizard: Summary [page 5 of 5]
When you click Finish, the project will be created with the following settings:
Project directory:
C:/Users/ftlsk/OneDrive/Desktop/Quartus Projects/Lab2_ChristianRodrigues/
Project name: FourBitAdder_ChristianRodrigues
Top-level design entity: FourBitAdder_ChristianRodrigues
Number of files added: 2
Number of user libraries added: 0
Device assignments:
Family name: MAX3000A
Device: EPM3064ATC44-10
EDA tools:
Design entry/synthesis: <None>
Simulation: <None>
Timing analysis: <None>
Operating conditions:
Core voltage: 3.3V
Junction temperature range: 0-85 °C
< Back
Next >
Finish
Cancel


4 Bit Adder
A3 B3
A2 B2
A1 B1
A0 B0
Cout
Full Adder
C3
C2
C1
Cin
S3
S2
S1
S0

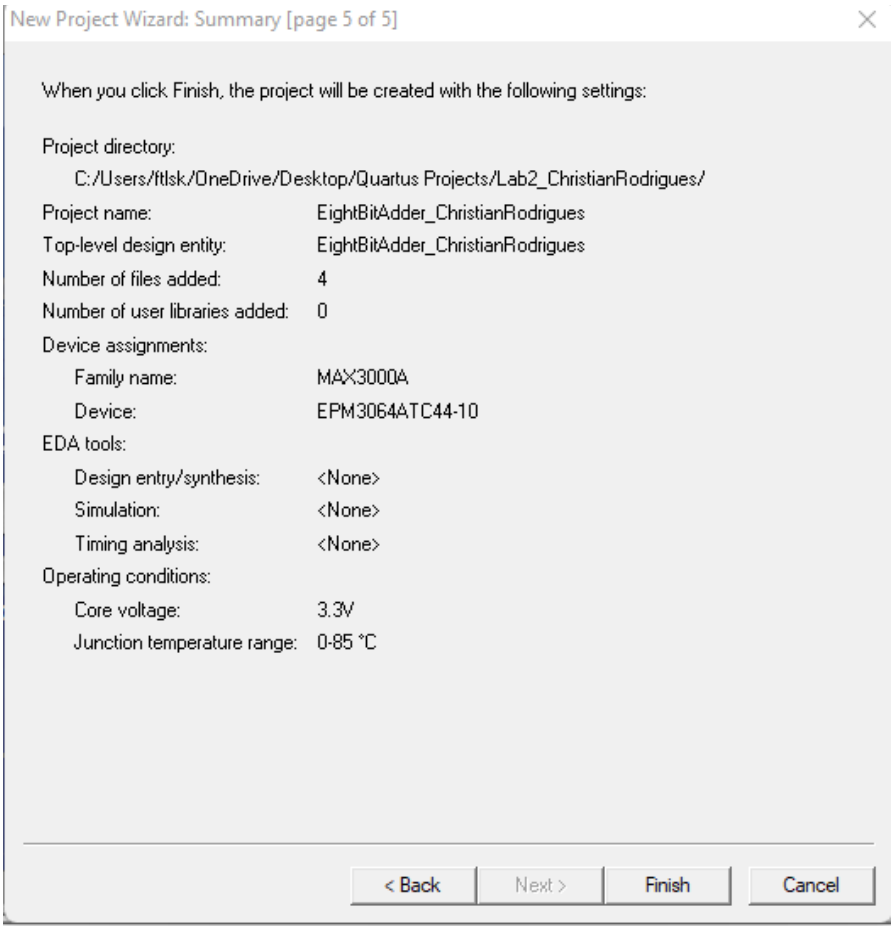
FourBitAdder_ChristianRodrigues.vhd

```
1   LIBRARY ieee;
2   use ieee.std_logic_1164.all;
3
4   ENTITY FourBitAdder_ChristianRodrigues IS
5       PORT (A, B : IN STD_LOGIC_VECTOR(3 DOWNTO 0);
6             Cin : STD_LOGIC;
7             S: OUT STD_LOGIC_VECTOR(3 DOWNTO 0);
8             Cout : OUT STD_LOGIC);
9   END FourBitAdder_ChristianRodrigues;
10
11  ARCHITECTURE LogicFunc OF FourBitAdder_ChristianRodrigues IS
12  COMPONENT FullAdder_ChristianRodrigues IS
13      PORT (A, B, Cin : IN STD_LOGIC;
14            S, Cout :  OUT STD_LOGIC);
15  END COMPONENT;
16
17  SIGNAL C1, C2, C3 : STD_LOGIC;
18
19  BEGIN
20  adder0: FullAdder_ChristianRodrigues PORT MAP (A(0), B(0), Cin, S(0), C1);
21  adder1: FullAdder_ChristianRodrigues PORT MAP (A(1), B(1), C1, S(1), C2);
22  adder2: FullAdder_ChristianRodrigues PORT MAP (A(2), B(2), C2, S(2), C3);
23  adder3: FullAdder_ChristianRodrigues PORT MAP (A(3), B(3), C3, S(3), Cout);
24  END LogicFunc;
```

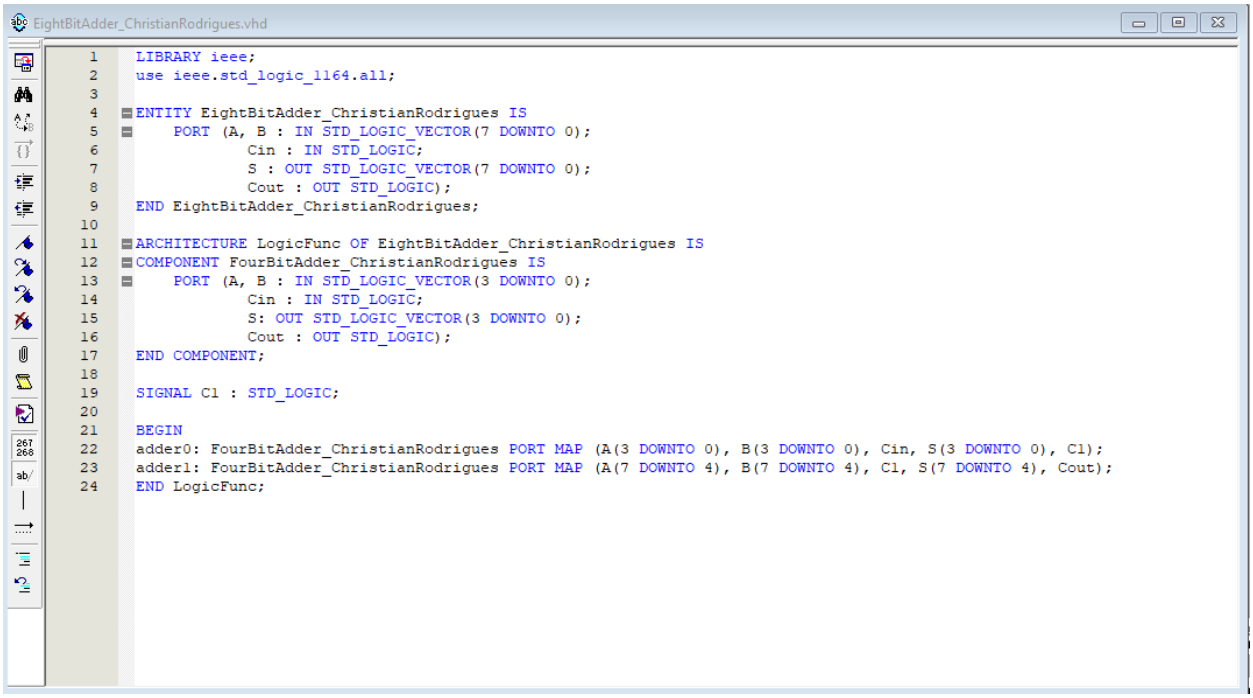


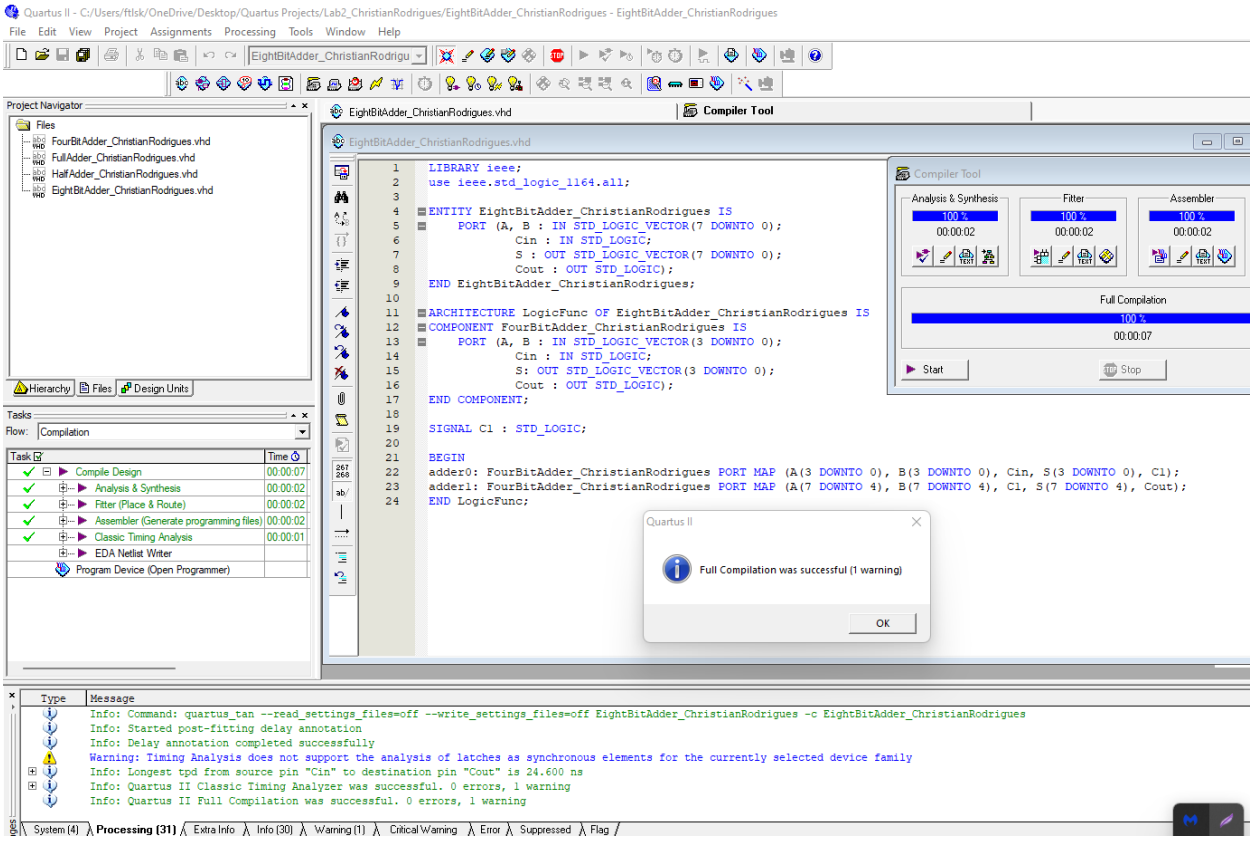

FourBitAdder_ChristianRodrigues.vwf
Master Time Bar: 18.95 ns
Pointer: 45.3 ns
Interval: 26.35 ns
Start:
End:
Name
0 ps
10.0 ns
20.0 ns
30.0 ns
40.0 ns
18.95 ns
Inputs
A
A[3]
A[2]
A[1]
A[0]
B
B[3]
B[2]
B[1]
B[0]
Cin
Cout
S
S[3]
S[2]
S[1]
S[0]
0101, 1010, 0
0110, 0111, 0
1001, 1011, 0
0011, 1101, 0
0000, 0000, 0
0101
0110
1001
0011
0000
1010
0111
1011
1101
0000
1111
1101
0100
0000
0101+1010=1111
0110+0111=1101
1001+1011=10100
0011+1101=10000

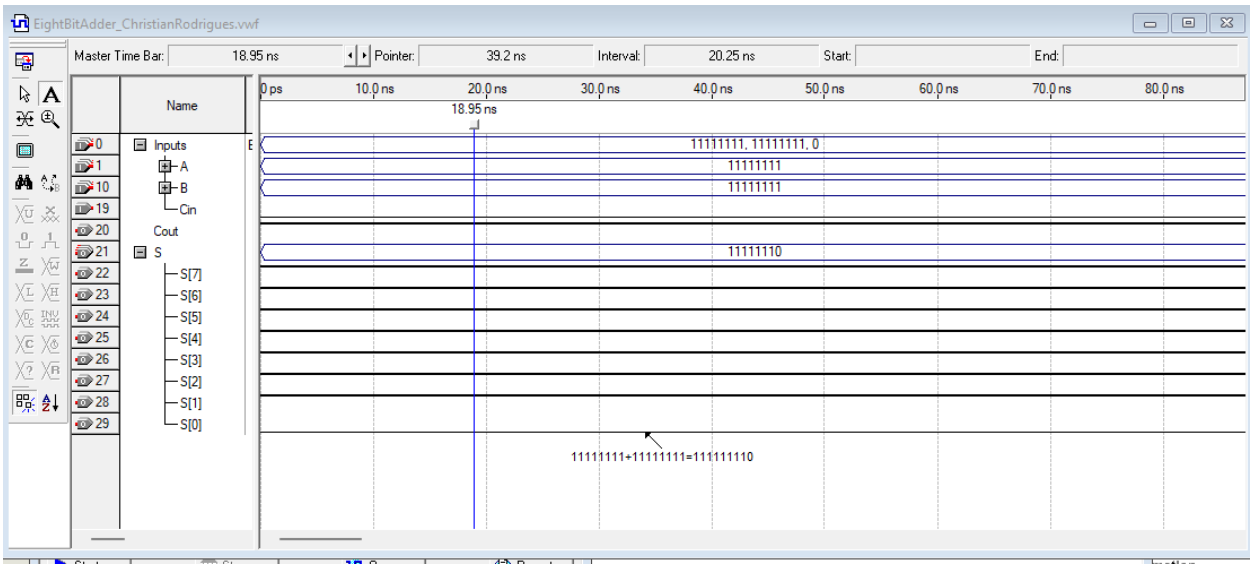
8-bit Adder


New Project Wizard: Summary [page 5 of 5]
When you click Finish, the project will be created with the following settings:
Project directory:
C:/Users/ftlsk/OneDrive/Desktop/Quartus Projects/Lab2_ChristianRodrigues/
Project name: EightBitAdder_ChristianRodrigues
Top-level design entity: EightBitAdder_ChristianRodrigues
Number of files added: 4
Number of user libraries added: 0
Device assignments:
Family name: MAX3000A
Device: EPM3064ATC44-10
EDA tools:
Design entry/synthesis: <None>
Simulation: <None>
Timing analysis: <None>
Operating conditions:
Core voltage: 3.3V
Junction temperature range: 0-85 °C
< Back
Next >
Finish
Cancel

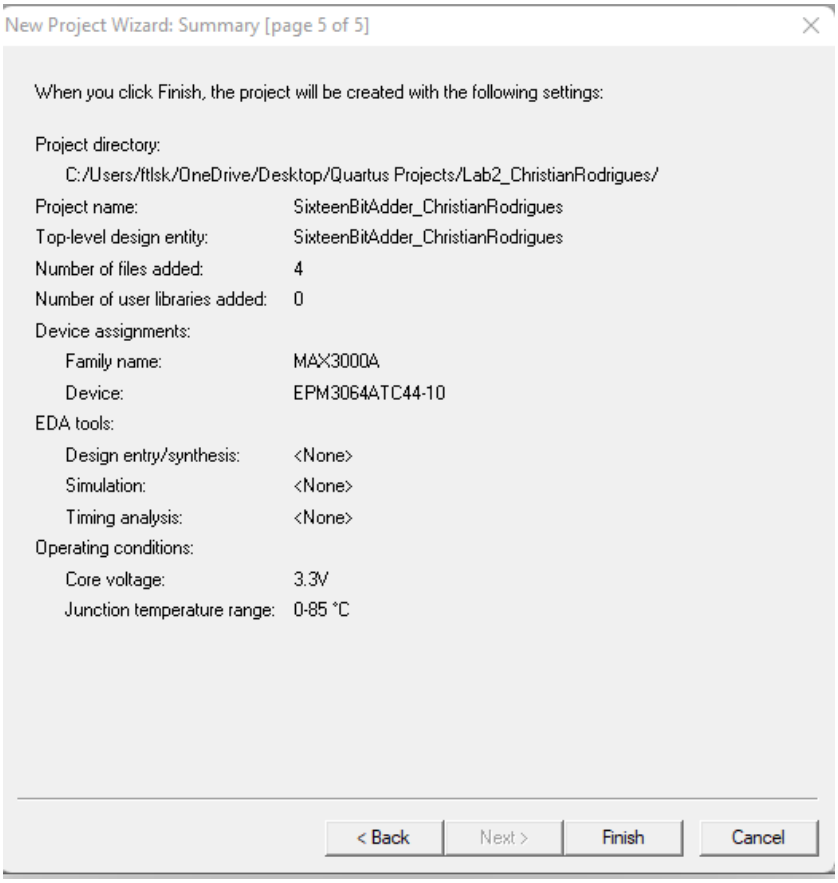

8-Bit Adder
4-Bit Adder
4-Bit Adder
Cout
Cin

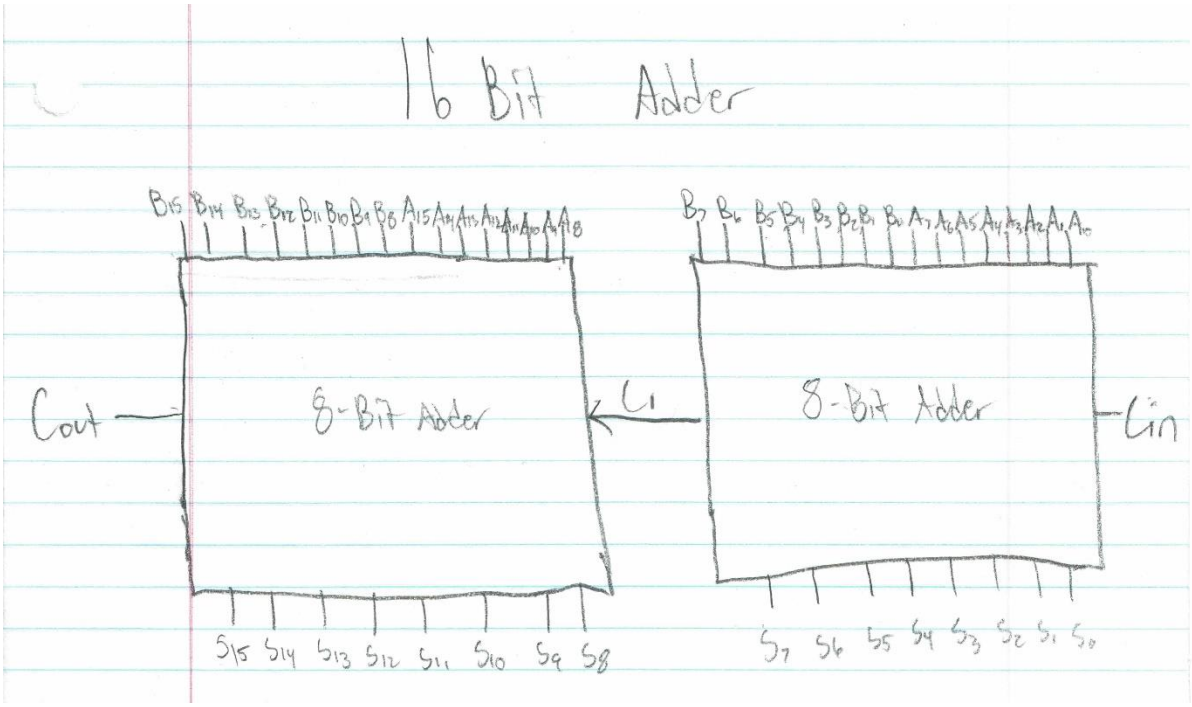

EightBitAdder_ChristianRodrigues.vhd
1 LIBRARY ieee;
2 use ieee.std_logic_1164.all;
3
4 ENTITY EightBitAdder_ChristianRodrigues IS
5 PORT (A, B : IN STD_LOGIC_VECTOR(7 DOWNTO 0);
6 Cin : IN STD_LOGIC;
7 S : OUT STD_LOGIC_VECTOR(7 DOWNTO 0);
8 Cout : OUT STD_LOGIC);
9 END EightBitAdder_ChristianRodrigues;
10
11 ARCHITECTURE LogicFunc OF EightBitAdder_ChristianRodrigues IS
12 COMPONENT FourBitAdder_ChristianRodrigues IS
13 PORT (A, B : IN STD_LOGIC_VECTOR(3 DOWNTO 0);
14 Cin : IN STD_LOGIC;
15 S: OUT STD_LOGIC_VECTOR(3 DOWNTO 0);
16 Cout : OUT STD_LOGIC);
17 END COMPONENT;
18
19 SIGNAL C1 : STD_LOGIC;
20
21 BEGIN
22 adder0: FourBitAdder_ChristianRodrigues PORT MAP (A(3 DOWNTO 0), B(3 DOWNTO 0), Cin, S(3 DOWNTO 0), C1);
23 adder1: FourBitAdder_ChristianRodrigues PORT MAP (A(7 DOWNTO 4), B(7 DOWNTO 4), C1, S(7 DOWNTO 4), Cout);
24 END LogicFunc;


Quartus II - C:/Users/ftlsk/OneDrive/Desktop/Quartus Projects/Lab2_ChristianRodrigues/EightBitAdder_ChristianRodrigues - EightBitAdder_ChristianRodrigues
File Edit View Project Assignments Processing Tools Window Help
Project Navigator
Files
FourBitAdder_ChristianRodrigues.vhd
FullAdder_ChristianRodrigues.vhd
HalfAdder_ChristianRodrigues.vhd
EightBitAdder_ChristianRodrigues.vhd
Hierarchy Files Design Units
Tasks
Flow: Compilation
Task Time
Compile Design 00:00:07
Analysis & Synthesis 00:00:02
Fitter (Place & Route) 00:00:02
Assembler (Generate programming files) 00:00:02
Classic Timing Analysis 00:00:01
EDA Netlist Writer
Program Device (Open Programmer)
EightBitAdder_ChristianRodrigues.vhd
Compiler Tool
Compiler Tool
Analysis & Synthesis
Fitter
Assembler
100 %
00:00:02
Full Compilation
00:00:07
Start
Stop
Quartus II
Full Compilation was successful (1 warning)
OK
Type Message
Info: Command: quartus_tan --read_settings_files=off --write_settings_files=off EightBitAdder_ChristianRodrigues -c EightBitAdder_ChristianRodrigues
Info: Started post-fitting delay annotation
Info: Delay annotation completed successfully
Warning: Timing Analysis does not support the analysis of latches as synchronous elements for the currently selected device family
Info: Longest tpd from source pin "Cin" to destination pin "Cout" is 24.600 ns
Info: Quartus II Classic Timing Analyzer was successful. 0 errors, 1 warning
Info: Quartus II Full Compilation was successful. 0 errors, 1 warning
System (4) Processing (31) Extra Info Info (30) Warning (1) Critical Warning Error Suppressed Flag


EightBitAdder_ChristianRodrigues.vwf
Master Time Bar: 18.95 ns
Pointer: 39.2 ns
Interval: 20.25 ns
Start:
End:
Name
0 ps
10.0 ns
20.0 ns
30.0 ns
40.0 ns
50.0 ns
60.0 ns
70.0 ns
80.0 ns
18.95 ns
Inputs
A
B
Cin
Cout
S
S[7]
S[6]
S[5]
S[4]
S[3]
S[2]
S[1]
S[0]
11111111, 11111111, 0
11111111
11111111
11111110
11111111+11111111=111111110

16-bit Adder


New Project Wizard: Summary [page 5 of 5]
When you click Finish, the project will be created with the following settings:
Project directory:
C:/Users/ttlsk/OneDrive/Desktop/Quartus Projects/Lab2_ChristianRodrigues/
Project name: SixteenBitAdder_ChristianRodrigues
Top-level design entity: SixteenBitAdder_ChristianRodrigues
Number of files added: 4
Number of user libraries added: 0
Device assignments:
Family name: MAX3000A
Device: EPM3064ATC44-10
EDA tools:
Design entry/synthesis: <None>
Simulation: <None>
Timing analysis: <None>
Operating conditions:
Core voltage: 3.3V
Junction temperature range: 0-85 °C
< Back
Next >
Finish
Cancel


16 Bit Adder
8-Bit Adder
8-Bit Adder
Cout
Cin
C1

SixteenBitAdder_ChristianRodrigues.vhd

```
1  LIBRARY ieee;
2  use ieee.std_logic_1164.all;
3
4  ENTITY SixteenBitAdder_ChristianRodrigues IS
5          PORT (A, B : IN STD_LOGIC_VECTOR(15 DOWNTO 0);
6                Cin : IN STD_LOGIC;
7                S : OUT STD_LOGIC_VECTOR(15 DOWNTO 0);
8                Cout : OUT STD_LOGIC);
9  END SixteenBitAdder_ChristianRodrigues;
10
11 ARCHITECTURE LogicFunc OF SixteenBitAdder_ChristianRodrigues IS
12 COMPONENT EightBitAdder_ChristianRodrigues IS
13     PORT (A, B : IN STD_LOGIC_VECTOR(7 DOWNTO 0);
14           Cin : IN STD_LOGIC;
15           S : OUT STD_LOGIC_VECTOR(7 DOWNTO 0);
16           Cout : OUT STD_LOGIC);
17 END COMPONENT;
18
19 SIGNAL C1 : STD_LOGIC;
20
21 BEGIN
22 adder0: EightBitAdder_ChristianRodrigues PORT MAP (A(7 DOWNTO 0), B(7 DOWNTO 0), Cin, S(7 DOWNTO 0), C1);
23 adder1: EightBitAdder_ChristianRodrigues PORT MAP (A(15 DOWNTO 8), B(15 DOWNTO 8), C1, S(15 DOWNTO 8), Cout);
24 END LogicFunc;
```

Quartus II - C:/Users/ftlsk/OneDrive/Desktop/Quartus Projects/Lab2_ChristianRodrigues/SixteenBitAdder_ChristianRodrigues - SixteenBitAdder_ChristianRodrigues

File Edit View Project Assignments Processing Tools Window Help

Project Navigator

Entity	Macrocells	Pins
MAX3000A: EPM3064ATC100-4		
SixteenBitAdder_ChristianRodri...	57	54

Hierarchy | Files | Design Units

Tasks

Flow: Compilation

Task	Time
Compile Design	00:00:07
Analysis & Synthesis	00:00:03
Fitter (Place & Route)	00:00:01
Assembler (Generate programming files)	00:00:02
Classic Timing Analysis	00:00:01
EDA Netlist Writer	
Program Device (Open Programmer)	

SixteenBitAdder_ChristianRodrigues.vhd | Compiler Tool


```
1  LIBRARY ieee;
2  use ieee.std_logic_1164.all;
3
4  ENTITY SixteenBitAdder_ChristianRodrigues IS
5          PORT (A, B : IN STD_LOGIC_VECTOR(15 DOWNTO 0);
6                Cin : IN STD_LOGIC;
7                S : OUT STD_LOGIC_VECTOR(15 DOWNTO 0);
8                Cout : OUT STD_LOGIC);
9  END SixteenBitAdder_ChristianRodrigues;
10
11 ARCHITECTURE LogicFunc OF SixteenBitAdder_ChristianRodrigues IS
12 COMPONENT EightBitAdder_ChristianRodrigues IS
13     PORT (A, B : IN STD_LOGIC_VECTOR(7 DOWNTO 0);
14           Cin : IN STD_LOGIC;
15           S : OUT STD_LOGIC_VECTOR(7 DOWNTO 0);
16           Cout : OUT STD_LOGIC);
17 END COMPONENT;
18
19 SIGNAL C1 : STD_LOGIC;
20
21 BEGIN
22 adder0: EightBitAdder_ChristianRodrigues PORT MAP (A(7 DOWNTO 0), B(7 DOWNTO 0), Cin, S(7 DOWNTO 0), C1);
23 adder1: EightBitAdder_ChristianRodrigues PORT MAP (A(15 DOWNTO 8), B(15 DOWNTO 8), C1, S(15 DOWNTO 8), Cout);
24 END LogicFunc;
```


Compiler Tool

Analysis & Synthesis 100 % 00:00:03 | Fitter 100 % 00:00:01 | Assembler 100 % 00:00:02

Full Compilation 100 % 00:00:07

Start | Stop

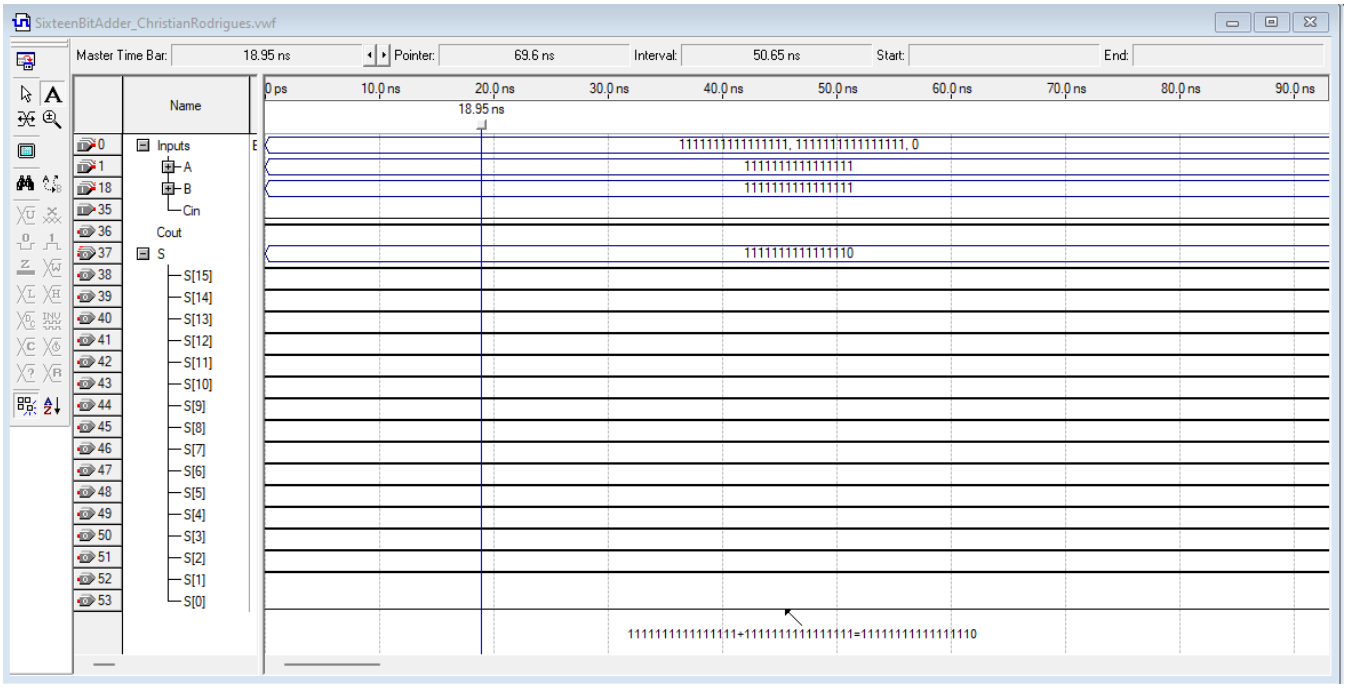
Quartus II

Full Compilation was successful (1 warning)

OK

Type	Message
	Info: Started post-fitting delay annotation
	Info: Delay annotation completed successfully
	Warning: Timing Analysis does not support the analysis of latches as synchronous elements for the currently selected device family
	Info: Longest tpd from source pin "Cin" to destination pin "S[10]" is 11.000 ns
	Info: Quartus II Classic Timing Analyzer was successful. 0 errors, 1 warning
	Info: Quartus II Full Compilation was successful. 0 errors, 1 warning

System (4) | Processing (33) | Extra Info | Info (32) | Warning (1) | Critical Warning | Error | Suppressed | Flag


SixteenBitAdder_ChristianRodrigues.vwf
Master Time Bar: 18.95 ns
Pointer: 69.6 ns
Interval: 50.65 ns
Start:
End:
Name
0 ps
10.0 ns
20.0 ns
30.0 ns
40.0 ns
50.0 ns
60.0 ns
70.0 ns
80.0 ns
90.0 ns
18.95 ns
Inputs
A
B
Cin
Cout
S
S[15]
S[14]
S[13]
S[12]
S[11]
S[10]
S[9]
S[8]
S[7]
S[6]
S[5]
S[4]
S[3]
S[2]
S[1]
S[0]
1111111111111111, 1111111111111111, 0
1111111111111111
1111111111111111
1111111111111110
1111111111111111+1111111111111111=1111111111111110