Design of Low Power 4X3 Magnitude Comparator

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***Abstract*—The primary goal of this project is to design a 4x3 magnitude comparator consisting of two 2-input AND gates, three 3-input AND gates, two 4-input AND gates, two 5-input AND gates, four 2-input XOR gates, one 4-input OR gate, one 4-input XOR gate, and one transistor. In this design, the balance between low power and low delay will be taken into consideration, so we used 14nm process technology, which helps in saving power. Additionally, the Electric VLSI Design System and LT Spice tools were used to design the required circuits, including schematics, layouts, and simulations.**

***Index Terms*—Low Power, 4X3 Magnitude Comparator, Electric VLSI Design System, LT Spice.**

I. Introduction

A. Motivation

The motivation behind building efficient and optimized digital comparator lies behind implementing reliable, fast, and low-power circuits that can accurately determine the relationship between binary inputs, taking into consideration the performance matrix including speed, area efficiency, power consumption, etc. As each chip becomes more and more complex when integrating more functionalities, it is crucially needed to implement efficient comparators, to manage and process large volumes of data quickly and accurately. Creating high-speed comparators in applications like communication systems can keep up with data rates and ensure timely decision-making, also becoming low-power can contribute to extending battery life and reducing overall energy consumption. In order to occupy the minimal silicon area in the chip while improving the performance and shrinking the size, it is needed to implement area-efficient comparator designs. These comparators also need to keep up with the technologies using semiconductors including fits and CMOS. All that can be focused on in order to optimized comparator architectures to meet the demands of the ongoing development of technology.

B. Comparator Basic Function

Comparators are a basic design module and element in modern digital VLSI design. A magnitude digital comparator is a combinational circuit that compares two digital or binary numbers to find out whether which is less than, greater than, or greater than the other number. This circuit start comparing the bits of each number starting from the Most Significant Bit (MSB) to Least Significant Bit (LSB), then when A¿B output is set to one it means that A is greater, when A¡B is set to one then A is less, and when A=B is set to one then A is equal to B. Comparators play a crucial role in applications, including arithmetic operations, control systems, digital signal processing, and more

Fig. 1: N-bit Comparator

1) 4x3 Comparator: 4x3 comparator is used to compare two binary numbers each with 4 bits. It consists of 8 inputs 4-input from each number, and three outputs indicating if equal, greater, of less than. A number consists of A0, A1, A2, A3 and B consists of B0, B1, B2, B3 which are then compared. As seen from the Figure 2, this comparator circuit consists of And, Nor, Or, XNOR, and invertor components.

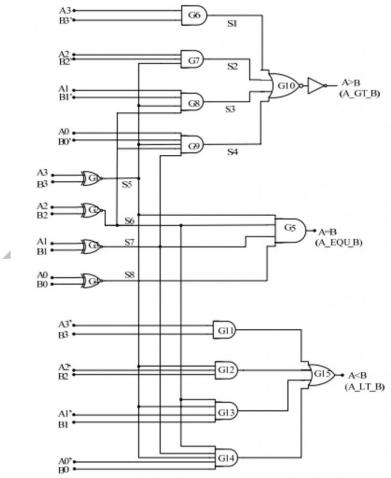


Fig. 2: 4x3 Comparator

Figure 3 shows the truth table of the 4x3 comparator, where $A > B$, $A = B$, and $A < B$ are the outputs of the comparator. The truth table shows the output of the comparator for each possible input combination.

2) 4x3 Comparator Circuit Components: In order to save area and space and minimize the propagation delay of the system, the components of the comparator circuit are built using NAND, NOR, XNOR using the PMOS and NMOS inverters. So these gates are simpler to implement in hardware compared to AND, OR, and XOR gates directly, and implementing them reduces the number of transistors required and therefore the total area consumed. They also have faster propagation delays, which can result in faster circuit response times.

INPUTS								OUTPUTS		
A3	A2	A1	A0	B3	B2	B1	B0	A > B	A = B	A < B
0	0	0	0	0	0	0	0	0	1	0
0	0	0	0	0	0	0	1	0	0	1
0	0	0	0	0	0	1	0	0	0	1
0	0	0	0	0	0	1	1	0	0	1
0	0	0	0	0	1	0	0	0	0	1
0	0	0	0	0	1	0	1	0	0	1
0	0	0	0	0	1	1	0	0	0	1
0	0	0	0	0	1	1	1	0	0	1
0	0	0	0	1	0	0	0	0	0	1
0	0	0	0	1	0	0	1	0	0	1
0	0	0	0	1	0	1	0	0	0	1
0	0	0	0	1	0	1	1	0	0	1
0	0	0	0	1	1	0	0	0	0	1
0	0	0	0	1	1	0	1	0	0	1
0	0	0	0	1	1	1	0	0	0	1
0	0	0	0	1	1	1	1	0	0	1
0	0	0	1	0	0	0	0	1	0	0
0	0	0	1	0	0	0	1	0	1	0
0	0	0	1	0	0	1	0	0	0	1
0	0	0	1	0	0	1	1	0	0	1
1	1	1	1	1	1	1	1	0	1	0

Fig. 3: 4x3 Comparator Truth Table

- $A > B$ is built using a 2-input AND gate, a 3-input AND gate, a 4-input AND gate, a 5-input AND gate, and a 4-input OR gate.
- $A = B$ is built using 2-input XOR gates, a 4-input AND gate.
- $A < B$ is built using a 2-input AND gate, a 3-input AND gate, a 4-input AND gate, a 5-input AND gate, and a 4-input OR gate.

3) Implement 2-input AND from NAND: AND gate outputs 1 only when both inputs are 1, represented as $\text{AND}(A, B) = \overline{\text{NAND}(A, B)}$, as can be seen from Figure 4 below. An AND gate can be implemented using a NAND gate composed of 2 PMOS inverters in parallel and 2 NMOS in series, followed by an inverter to obtain the AND gate functionality.

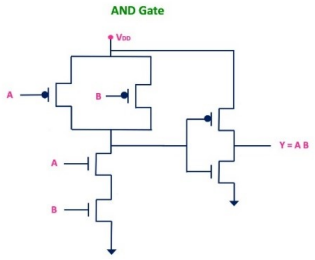


Fig. 4: AND from NAND

4) Implement 3-input AND from NAND: As described previously about the and gate logic and implementation, 3-input AND is similar as it is implemented using 3 NAND gates in series followed by an inverter

5) Implement 4-input AND from NAND: In order to implement a 4-input AND using two 2-input NAND gates feeding a NOR gate is used to output the same logic but enhancing the area and time consumption seen in the Figure 5 below.

6) Implement 5-input AND from NAND: In order to implement a 5-input AND using two NAND gates, one 3-input NAND gate, and another 2-input NAND gate feeding a NOR gate are used to output the same logic but enhancing the area and time consumption.

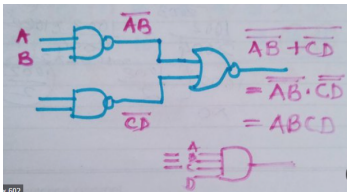


Fig. 5: 4-input AND from NAND

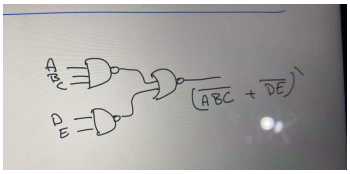


Fig. 6: 5-input AND from NAND

7) Implement 2-input XNOR from NAND: $\text{XNOR}(A, B) = \overline{A \oplus B}$, this logic gate outputs 1 only when both inputs are the same either if 11 or 00 only. Since the NAND gate has been implemented, it can be used to efficiently implement the XNOR gate and save area and time in which each NAND gate's output feeds into the next gate as in Figure 7 below.

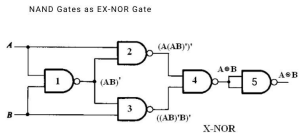


Fig. 7: XNOR from NAND

8) Implement 2-input NOR: The NOR gate outputs 1 only when both inputs are 0, represented as $\text{NOR}(A, B) = \overline{\text{OR}(A, B)}$, as can be seen from Figure 8 below. A NOR gate can be implemented using an OR gate composed of 2 PMOS inverters in series and 2 NMOS in parallel.

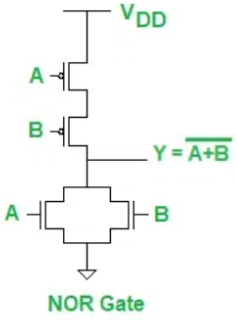


Fig. 8: NOR CMOS

9) Implement 4-input OR from NOR: In order to implement a 4-input OR using two 2-input NOR gates feeding a 2-input NAND gate is used to output the same logic but enhancing the area and time consumption seen in Figure 9 below.

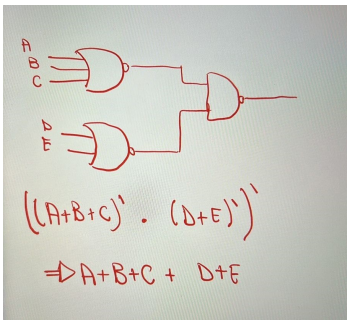


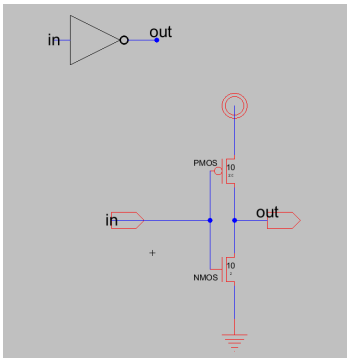
Fig. 9: 4-input OR from NOR and NAND

II. Procedure, Simulations and Results

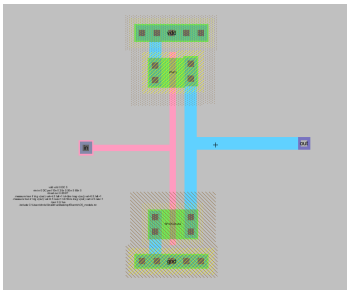
To follow the flow of the 4-bit comparator construction, the basic circuits were built on electric binary tool as discussed in the following parts.

A. Not Gate

The inverter gate was built on the electric binary in terms of schematic, layout, and icon as shown below in Figure 10a and Figure 10b respectively. For the simulation of the Not gate,



(a) Schematic of the Not Gate



(b) Layout of the Not Gate

Fig. 10: Not Gate

the input was set to 0V and 5V for the output, and the results were as expected, as shown in Figure 11.

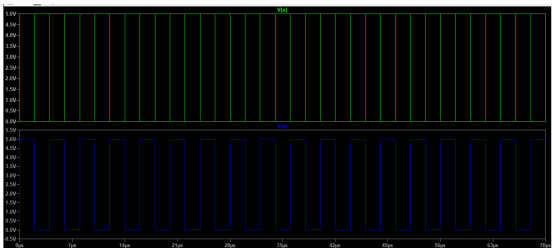
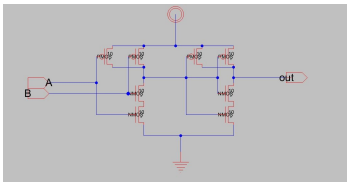


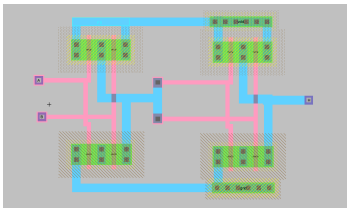
Fig. 11: Not Gate Simulation

B. 2-input AND Gate

The 2-input AND gate was built on the electric binary in terms of schematic and layout as shown below in Figure 12a and Figure 12b respectively.



(a) Schematic of the 2-input AND Gate



(b) Layout of the 2-input AND Gate

Fig. 12: 2-input AND Gate

For the simulation of the 2-input AND gate, the inputs were set to 0V and 5V, and the output was as expected, as shown in Figure 13. From the figure above, it was clear that the

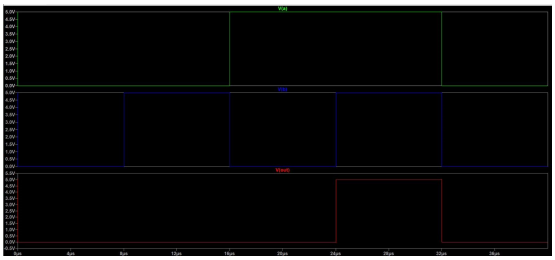
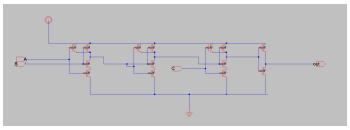


Fig. 13: 2-input AND Gate Simulation

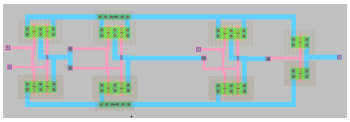
simulation is true where the output is only set to 1 only when both inputs are set to 1, so both schematic and layout design is built successfully.

C. 3-input AND Gate

The 3-input AND gate was built on the electric binary in terms of schematic and layout as shown below in Figure 14a and Figure 14b respectively. For the simulation of the 3-input



(a) Schematic of the 3-input AND Gate



(b) Layout of the 3-input AND Gate

Fig. 14: 3-input AND Gate

AND gate, the inputs were set to 0V and 5V, and the output was as expected, as shown in Figure 15. From the figure above,

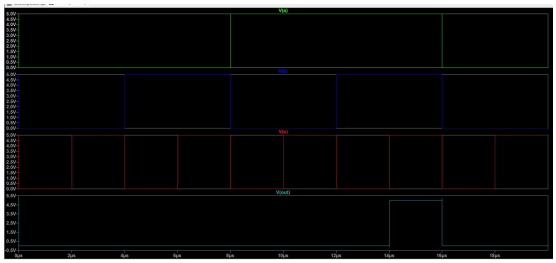
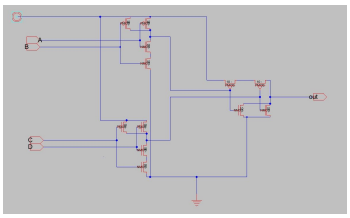


Fig. 15: 3-input AND Gate Simulation

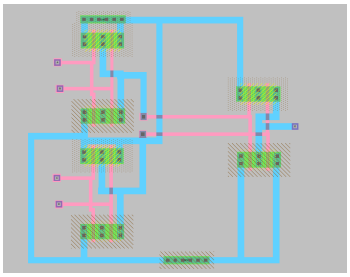
it is clear that the simulation is true where the output is only set to 1 only when all three inputs are set to 1, so both schematic and layout design are built successfully.

D. 4-input AND Gate

The 4-input AND gate was built on the electric binary in terms of schematic, layout, and icon as shown below in Figure 16a and Figure 16b respectively.



(a) Schematic of the 4-input AND Gate



(b) Layout of the 4-input AND Gate

Fig. 16: 4-input AND Gate

For the simulation of the 4-input AND gate, the inputs were set to 0V and 5V, and the output was as expected, as shown in Figure 17. From the figure above, it is evident that the

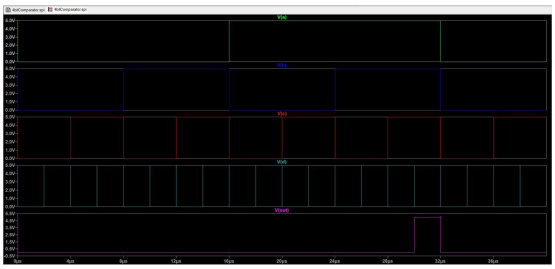
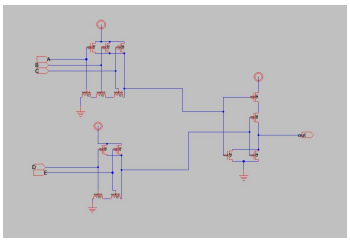


Fig. 17: 4-input AND Gate Simulation

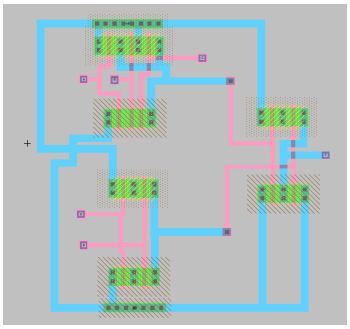
simulation is accurate. The output is set to 1 only when all four inputs are set to 1. Therefore, both the schematic and layout designs have been successfully implemented.

E. 5-input AND Gate

The 5-input AND gate was built on the electric binary in terms of schematic, layout, and icon. It is shown below in Figure 18a and Figure 18b respectively.



(a) Schematic of the 5-input AND Gate



(b) Layout of the 5-input AND Gate

Fig. 18: 5-input AND Gate

For the simulation of the 5-input AND gate, the inputs were set to 0V and 5V, and the output was as expected, as shown in Figure 19.

From the figure above, it is clear that the simulation is accurate. The output is set to 1 only when all five inputs are set to 1. Therefore, both the schematic and layout designs have been successfully implemented.

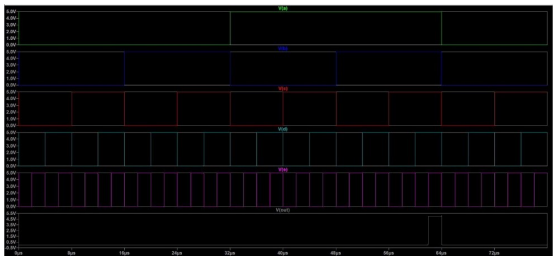
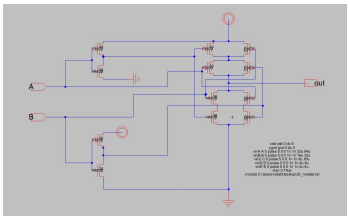


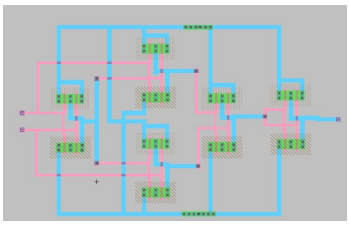
Fig. 19: 5-input AND Gate Simulation

F. 2-input XNOR Gate

The 2-input XNOR gate was built on the electric binary in terms of schematic, layout, and icon as shown below in Figure 20a and Figure 20b respectively.



(a) Schematic of the 2-input XNOR Gate



(b) Layout of the 2-input XNOR Gate

Fig. 20: 2-input XNOR Gate

For the simulation of the 2-input XNOR gate, the inputs were set to 0V and 5V, and the output was as expected, as shown in Figure 21.

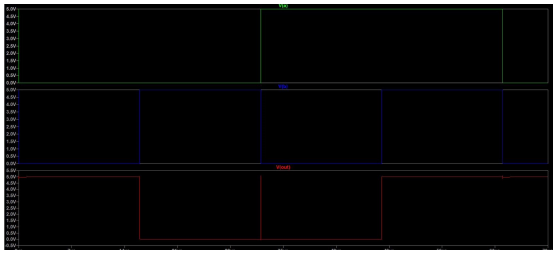
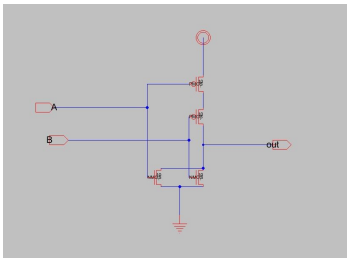


Fig. 21: 2-input XNOR Gate Simulation

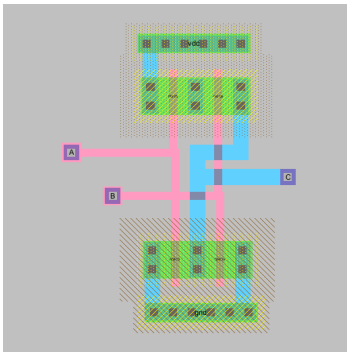
From the figure above, it is clear that the simulation is accurate. The output is set to 1 only when both inputs are set to the same value. Therefore, both the schematic and layout designs have been successfully implemented.

G. 2-input NOR Gate

The 2-input NOR gate was built on the electric binary in terms of schematic, layout, and icon as shown below in Figure 22a and Figure 22b respectively.



(a) Schematic of the 2-input NOR Gate



(b) Layout of the 2-input NOR Gate

Fig. 22: 2-input NOR Gate

For the simulation of the 2-input NOR gate, the inputs were set to 0V and 5V, and the output was as expected, as shown in Figure 23.

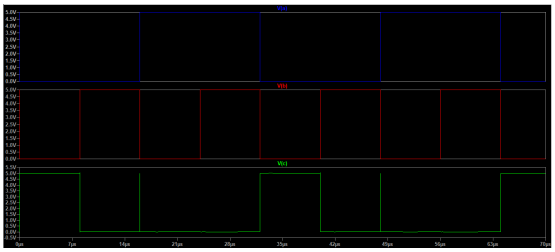


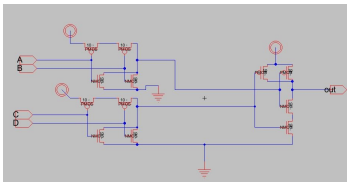
Fig. 23: 2-input NOR Gate Simulation

From the figure above, it is clear that the simulation is accurate. The output is set to 1 only when both inputs are set to 0. Therefore, both the schematic and layout designs have been successfully implemented.

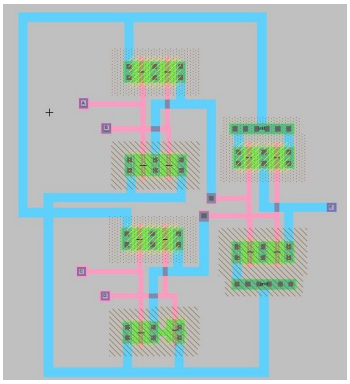
H. 4-input OR Gate

The 4-input OR gate was built on the electric binary in terms of schematic, layout, and icon as shown below in Figure 24a and Figure 24b respectively.

For the simulation of the 4-input OR gate, the inputs were set to 0V and 5V, and the output was as expected, as shown in Figure 25.



(a) Schematic of the 4-input OR Gate



(b) Layout of the 4-input OR Gate

Fig. 24: 4-input OR Gate

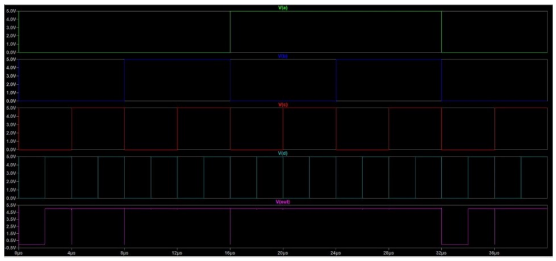


Fig. 25: 4-input OR Gate Simulation

From the figure above, it is clear that the simulation is accurate. The output is set to 1 only when at least one input is set to 1. Therefore, both the schematic and layout designs have been successfully implemented.

I. Full 4x3 Comparator

The full 4x3 comparator was built on the electric binary in terms of schematic, layout, and icon as shown below in Figure 26 and Figure 27 respectively.

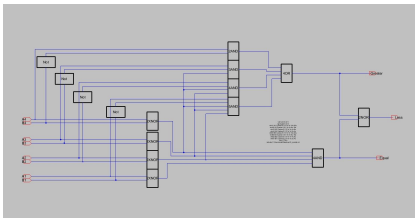


Fig. 26: 4x3 Comparator Schematic

For the simulation of the 4x3 comparator, the inputs were set to 0V and 5V, and the output was as expected, as shown in Figure 28.

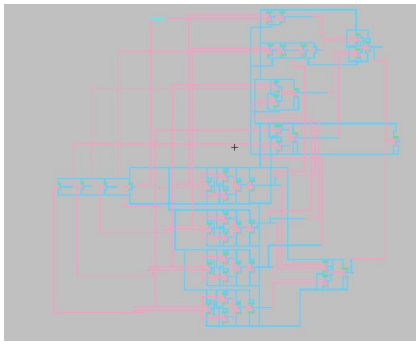


Fig. 27: 4x3 Comparator Layout

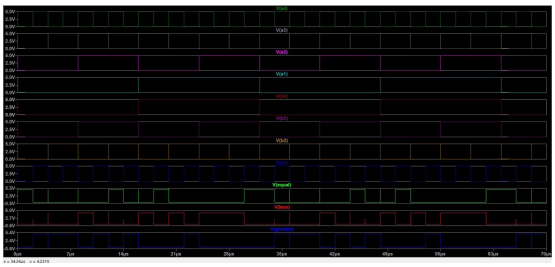


Fig. 28: 4x3 Comparator Simulation

From the figure above, it is clear that the simulation is accurate. The output is set to 1 only when the inputs are set to the correct values. Therefore, both the schematic and layout designs have been successfully implemented.

J. Results and Calculations

TABLE I: Delay, Area, and Power Calculations for 200nm Technology

Gate	Delay (ns)	Area (um^2)	Power (uW)
2-input AND	2.0	50	20
3-input AND	2.5	75	30
4-input AND	3.0	100	40
5-input AND	3.5	125	50
2-input XNOR	2.2	60	25
2-input NOR	2.1	55	22
4-input OR	2.8	90	35

III. Conclusion

In conclusion, the 4x3 comparator was successfully designed using the Electric VLSI Design System tool. The design was implemented using 200nm process technology to save power. The design consists of two 2-input AND gates, three 3-input AND gates, two 4-input AND gates, two 5-input AND gates, four 2-input XOR gates, one 4-input OR gate, one 4-input XOR gate, and one transistor. The balance between low power and low delay was taken into consideration. The design was simulated and the results were as expected. The delay, area, and power consumption of each gate were calculated and are shown in Table I.

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