CS3650 -- Homework #5 (20 points)

Problem 1 (5 points) Using graphical representation, show the pipeline execution of the following instructions on the 5-stage pipeline as given in the Lecture 7.

```
lw R20, 0x0100(R18)
or R24, R18, R16
sw R22, 0x0110(Ri6)
```

Instr	CC1	CC2	CC3	CC4	CC5	CC6	CC7				
lw	IM	REG	ALU	DM	REG						
or		IM	REG	ALU	DM	REG					
sw			IM	REG	ALU	DM	REG				

Also answer the following questions:

(1) How many cycles needed for the execution of these three instructions?
(2) What is ALU doing on cycle 3, 4, 5 respectively?
(3) What is the memory action in cycle 4, 5, 6 respectively?

Problem 2 (5 points) Using graphical representation, show the pipeline execution of the following instructions on the 5-stage pipeline with hazard detection and forwarding as implemented in Lecture 6. Clearly indicate the forwarding path(s) and stall(s).
Note: highlight the forwarding path and use bubbles (or O) for stalls.

```
Lw R20, 0x0100(R18)
Add R14, R20, R16
Sw R18, 0x0110(R16)
Or R12, R14, R20
Lw R18, 0x0100(R12)
```

instr	CC1	CC2	CC3	cc4	cc5	cc6	CC7	CC8	cc9	cc 10	CC 11			
lw	IM	REG	ALU	DM	REG									
		O	O	O	O	O								
add			IM	REG	ALU	DM	REG							
sw				IM	REG	ALU	DM	REG						
or					IM	REG	ALU	DM	REG					
						O	O	O	O	O				
lw							IM	REG	ALU	DM	REG			

Problem 3 (5 points) Consider a typical MIPS pipeline with branch penalty 1 cycle (i.e. 1 stall cycle if taken.) For the following MIPS instruction sequence, for two cases: (1) branch not taken; (2) branch taken.

```
    BEQ R14, R12, L
    AND R9, R9, R1
    OR R8, R12, R2
    SW R12, 0x0004 (R10)
L:  ADD R10, R14, R12
    LW R10, 0x0004(R12)
```

Answer sheet for Problem 3(a) branch is not taken.

instr	CC1	CC2	CC3	cc4	cc5	cc6	cc7	cc8	cc9	cc10									
beq	IM	REG	ALU	DM	REG														
AND		IM	REG	ALU	DM	REG													
OR			IM	REG	ALU	DM	REG												
SW				IM	REG	ALU	DM	REG											
L: ADD					IM	REG	ALU	DM	REG										
lW						IM	REG	ALU	DM	REG									

Answer sheet for Problem 3(b) branch is taken.

instr	CC1	CC2	CC3	cc4	cc5	cc6	cc7	cc8	cc9	cc10									
beq	IM	REG	ALU	DM	REG														
AND		0	0	0	0	0													
OR			0	0	0	0	0												
SW				0	0	0	0	0											
L: ADD					IM	REG	ALU	DM	REG										
LW						IM	REG	ALU	DM	REG									

Problem 4 (5 points) We implemented a new 5-stage pipeline with the following features: the delay by data and control hazards are as follows: 1 cycle stall for the load by immediate use, 2 cycle stalls for branch taken.

Assume we now run 10,000 instructions on the pipeline, among them:

(1) 35% are lw instructions. 10% of lw instructions are followed by instructions that use lw result immediately in ALU input;

(2)15% are branch instructions with 40% possibility of branch taken;

(3) the remaining 50% are sw and R-type instructions that don't cause any stalls.

How many cycles we need to execute the 10,000 instructions on the pipeline? You may ignore the pipeline overhead such as start-up cost.

HW #5

- Problem #1

1) Each stage is one clock cycle. Each instruction will need five cycles to complete. For pipeline execution, seven clock cycles will be needed.

2) For cycle 3, the ALU is adding the base and offset address.
For cycle 4, the ALU is performing logical OR
For cycle 5, the ALU is adding the base and offset address.

3) cycle 4, accessing data from memory to be written into a register.
cycle 5, no operation.
cycle 6, accessing data from register to be written into memory.

- Problem #4

1) stalls by LW immediate use : $10{,}000(0.35 \times 0.10 \times 1) = 350$ cycles
2) stalls by branch instructions : $10{,}000(0.15 \times 0.40 \times 2) = 1200$ cycles
3) NO stalls

cycles needed to execute instructions with NO stalls : 10,004

cycles needed to execute instructions with stalls:

$$10{,}004 + 350 + 1200 = \boxed{11{,}554}$$