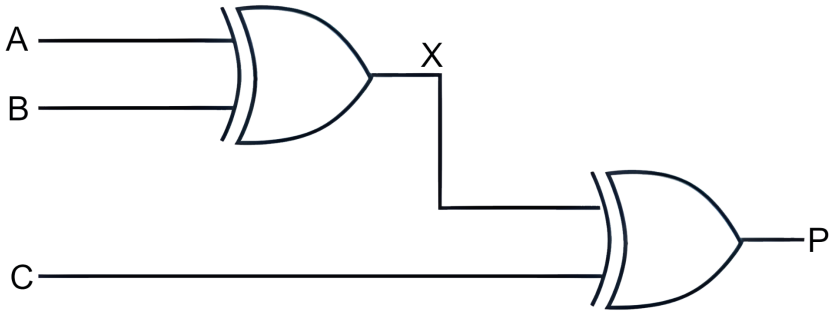
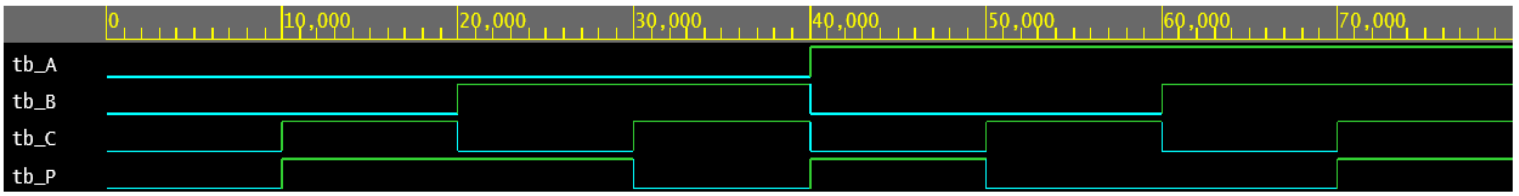
3 bit Even Parity Generator.

A	B	C	P
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1



Assume we have a 3-bit even parity generator. Suppose the three inputs A, B and C are applied to the circuit and the output bit is the parity bit P. The total number of 1's must be even to generate the even parity bit P. Based on the above circuit, we see that we need 2 gates XOR where X = A xor B and P = X xor C. X acts as the output of the first XOR and input of the second. In all 3 circuits the result of the simulation is as follows

Run Time: 80ns



> For instance:
At 0 ns A = 0, B = 0, C = 0 → **P = 0**
At 10 ns A = 0, B = 0, C = 1 → **P = 1**
At 40 ns A = 1, B = 0, C = 0 → **P = 1**
At 60 ns A = 1, B = 1, C = 0 → **P = 0**

By comparing the simulation results with the truth table we see that we have achieved the desired result

*The testbench remains the same for all three models.