

Analysis Report

d_gpu5(int, int, int, double*, double*, double*)

| | |
|-------------------------|---------------------------|
| Duration | 81.188 ms (81,188,375 ns) |
| Grid Size | [256,256,1] |
| Block Size | [16,16,1] |
| Registers/Thread | 28 |
| Shared Memory/Block | 4 KiB |
| Shared Memory Executed | 32 KiB |
| Shared Memory Bank Size | 4 B |

[1] Tesla V100-PCIE-16GB

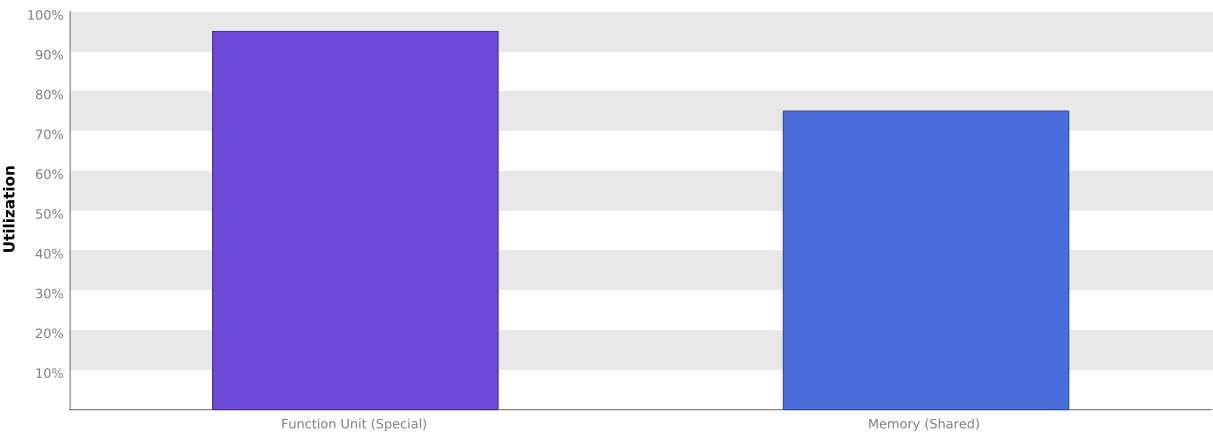
| | |
|---------------------------------------|--|
| GPU UUID | GPU-3c0567e0-df48-17c8-759b-baa355bbbcf3 |
| Compute Capability | 7.0 |
| Max. Threads per Block | 1024 |
| Max. Threads per Multiprocessor | 2048 |
| Max. Shared Memory per Block | 48 KiB |
| Max. Shared Memory per Multiprocessor | 96 KiB |
| Max. Registers per Block | 65536 |
| Max. Registers per Multiprocessor | 65536 |
| Max. Grid Dimensions | [2147483647, 65535, 65535] |
| Max. Block Dimensions | [1024, 1024, 64] |
| Max. Warps per Multiprocessor | 64 |
| Max. Blocks per Multiprocessor | 32 |
| Half Precision FLOP/s | 28.262 TeraFLOP/s |
| Single Precision FLOP/s | 14.131 TeraFLOP/s |
| Double Precision FLOP/s | 7.066 TeraFLOP/s |
| Number of Multiprocessors | 80 |
| Multiprocessor Clock Rate | 1.38 GHz |
| Concurrent Kernel | true |
| Max IPC | 4 |
| Threads per Warp | 32 |
| Global Memory Bandwidth | 898.048 GB/s |
| Global Memory Size | 15.752 GiB |
| Constant Memory Size | 64 KiB |
| L2 Cache Size | 6 MiB |
| Memcpy Engines | 7 |
| PCIe Generation | 3 |
| PCIe Link Rate | 8 Gbit/s |
| PCIe Link Width | 16 |

1. Compute, Bandwidth, or Latency Bound

The first step in analyzing an individual kernel is to determine if the performance of the kernel is bounded by computation, memory bandwidth, or instruction/memory latency. The results below indicate that the performance of kernel "d_gpu5" is most likely limited by compute. You should first examine the information in the "Compute Resources" section to determine how it is limiting performance.

1.1. Kernel Performance Is Bound By Compute

For device "Tesla V100-PCIE-16GB" the kernel's memory utilization is significantly lower than its compute utilization. These utilization levels indicate that the performance of the kernel is most likely being limited by computation on the SMs.



2. Compute Resources

GPU compute resources limit the performance of a kernel when those resources are insufficient or poorly utilized. Compute resources are used most efficiently when instructions do not overuse a function unit. The results below indicate that compute performance may be limited by overuse of a function unit.

2.1. Kernel Profile - Instruction Execution

The Kernel Profile - Instruction Execution shows the execution count, inactive threads, and predicated threads for each source and assembly line of the kernel. Using this information you can pinpoint portions of your kernel that are making inefficient use of compute resource due to divergence and predication.

Examine portions of the kernel that have high execution counts and inactive or predicated threads to identify optimization opportunities.

Cuda Functions :

d_gpu5(int, int, int, double*, double*, double*)

Maximum instruction execution count in assembly: 134217728

Average instruction execution count in assembly: 97080661

Instructions executed for the kernel: 12232163328

Thread instructions executed for the kernel: 391429226496

Non-predicated thread instructions executed for the kernel: 391378894848

Warp non-predicated execution efficiency of the kernel: 100.0%

Warp execution efficiency of the kernel: 100.0%

Source files :

/zhome/a8/6/114633/hpc/week3/ass3/hpc-gpu/mattmult/matmult_gpu5.cu

2.2. GPU Utilization Is Limited By Function Unit Usage

Different types of instructions are executed on different function units within each SM. Performance can be limited if a function unit is over-used by the instructions executed by the kernel. The following results show that the kernel's performance is potentially limited by overuse of the following function units: Special.

Load/Store - Load and store instructions for shared and constant memory.

Texture - Load and store instructions for local, global, and texture memory.

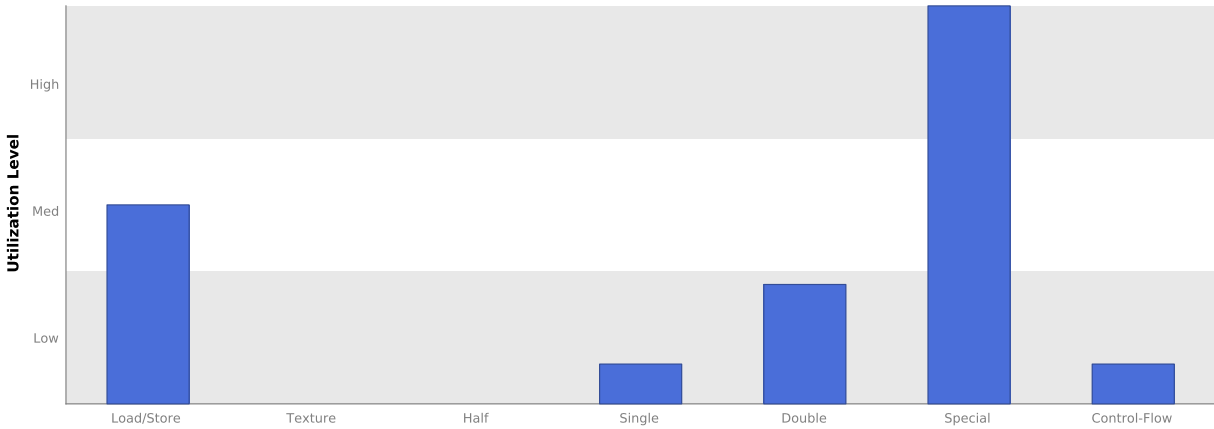
Half - Half-precision floating-point arithmetic instructions.

Single - Single-precision integer and floating-point arithmetic instructions.

Double - Double-precision floating-point arithmetic instructions.

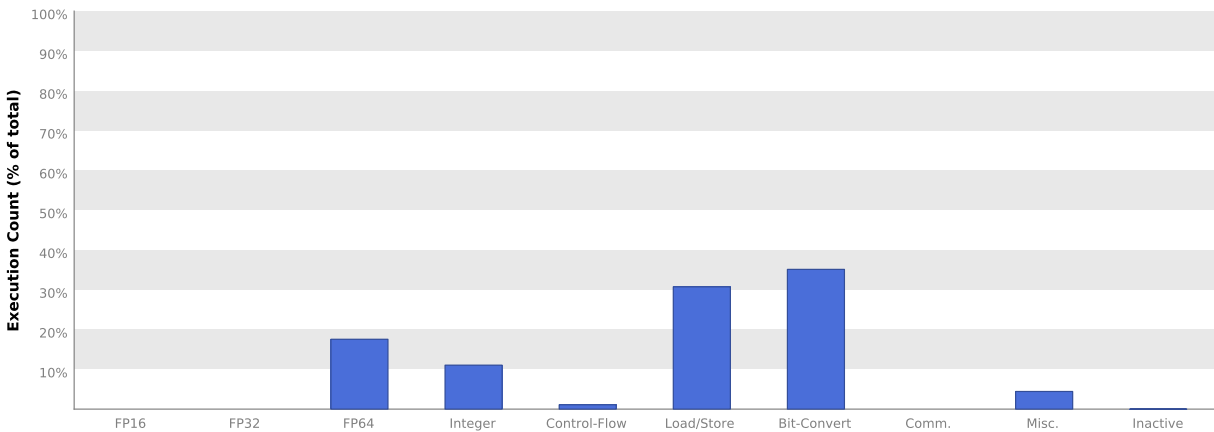
Special - Special arithmetic instructions such as sin, cos, popc, etc.

Control-Flow - Direct and indirect branches, jumps, and calls.



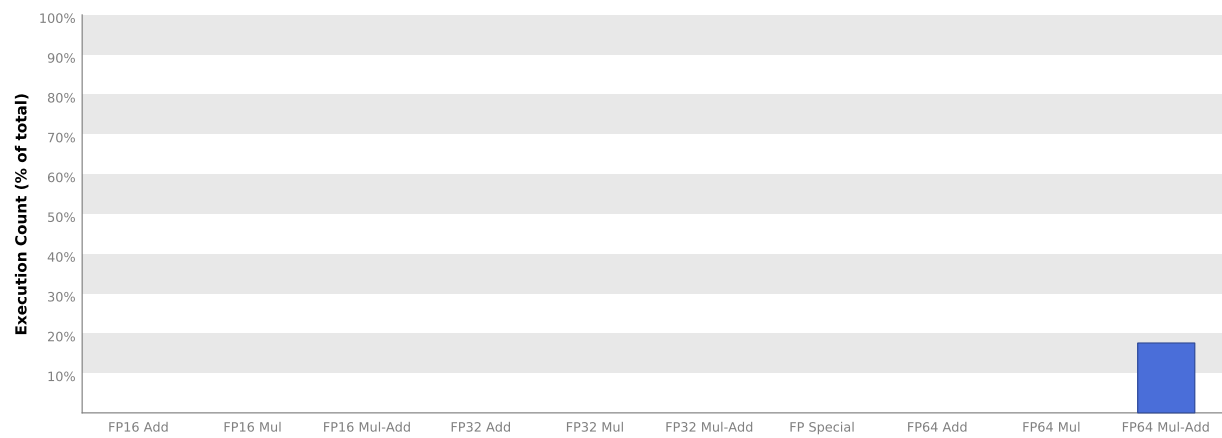
2.3. Instruction Execution Counts

The following chart shows the mix of instructions executed by the kernel. The instructions are grouped into classes and for each class the chart shows the percentage of thread execution cycles that were devoted to executing instructions in that class. The "Inactive" result shows the thread executions that did not execute any instruction because the thread was predicated or inactive due to divergence.



2.4. Floating-Point Operation Counts

The following chart shows the mix of floating-point operations executed by the kernel. The operations are grouped into classes and for each class the chart shows the percentage of thread execution cycles that were devoted to executing operations in that class. The results do not sum to 100% because non-floating-point operations executed by the kernel are not shown in this chart.



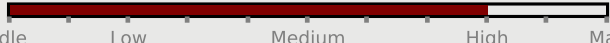





3. Memory Bandwidth

Memory bandwidth limits the performance of a kernel when one or more memories in the GPU cannot provide data at the rate requested by the kernel. The results below indicate that the kernel is limited by the bandwidth available to the shared memory.

3.1. Memory Bandwidth And Utilization

The following table shows the memory bandwidth used by this kernel for the various types of memory on the device. The table also shows the utilization of each memory type relative to the maximum throughput supported by the memory.

| Transactions | Bandwidth | Utilization | |
|--|-------------------|------------------------|--|
| Shared Memory | | | |
| Shared Loads | 6444600178 | 10,159.462 GB/s | |
| Shared Stores | 567430435 | 894.514 GB/s | |
| Shared Total | 7012030613 | 11,053.977 GB/s |  |
| L2 Cache | | | |
| Reads | 2048238536 | 807.226 GB/s | |
| Writes | 4194338 | 1.653 GB/s | |
| Total | 2052432874 | 808.879 GB/s |  |
| Unified Cache | | | |
| Local Loads | 0 | 0 B/s | |
| Local Stores | 0 | 0 B/s | |
| Global Loads | 2147483648 | 846.34 GB/s | |
| Global Stores | 4194304 | 1.653 GB/s | |
| Texture Reads | 6980370432 | 11,004.067 GB/s | |
| Unified Total | 9132048384 | 11,852.059 GB/s |  |
| Device Memory | | | |
| Reads | 1082268545 | 426.53 GB/s | |
| Writes | 4297709 | 1.694 GB/s | |
| Total | 1086566254 | 428.224 GB/s |  |
| System Memory | | | |
| [PCIe configuration: Gen3 x16, 8 Gbit/s] | | | |
| Reads | 0 | 0 B/s |  |
| Writes | 5 | 1.97 kB/s |  |

3.2. Memory Statistics

The following chart shows a summary view of the memory hierarchy of the CUDA programming model. The green nodes in the diagram depict logical memory space whereas blue nodes depicts actual hardware unit on the chip. For the various caches the reported percentage number states the cache hit rate; that is the ratio of requests that could be served with data locally available to the cache over all requests made.

The links between the nodes in the diagram depict the data paths between the SMs to the memory spaces into the memory system. Different metrics are shown per data path. The data paths from the SMs to the memory spaces report the total number of memory instructions executed, it includes both read and write operations. The data path between memory spaces and "Unified Cache" or "Shared Memory" reports the total amount of memory requests made (read or write). All other data paths report the total amount of transferred memory in bytes.

4. Instruction and Memory Latency

Instruction and memory latency limit the performance of a kernel when the GPU does not have enough work to keep busy. The results below indicate that the GPU does not have enough work because instruction execution is stalling excessively.

4.1. Kernel Profile - PC Sampling

The Kernel Profile - PC Sampling gives the number of samples for each source and assembly line with various stall reasons. The samples are collected at a period of 2048 [2¹¹] cycles. You can change the period under Settings->Analysis tab. The allowed values are from 5 to 31. Increasing the period would reduce the number of samples collected.

Using this information you can pinpoint portions of your kernel that are introducing latencies and the reason for the latency. Samples are taken in round robin order for all active warps at a fixed number of cycles regardless of whether the warp is issuing an instruction or not.

Instruction Issued - Warp was issued

Instruction Fetch - The next assembly instruction has not yet been fetched.

Execution Dependency - An input required by the instruction is not yet available. Execution dependency stalls can potentially be reduced by increasing instruction-level parallelism.

Memory Dependency - A load/store cannot be made because the required resources are not available or are fully utilized, or too many requests of a given type are outstanding. Data request stalls can potentially be reduced by optimizing memory alignment and access patterns.

Texture - The texture sub-system is fully utilized or has too many outstanding requests.

Synchronization - The warp is blocked at a __syncthreads() call.

Constant - A constant load is blocked due to a miss in the constants cache.

Pipe Busy - The compute resource(s) required by the instruction is not yet available.

Memory Throttle - Large number of pending memory operations prevent further forward progress. These can be reduced by combining several memory transactions into one.

Not Selected - Warp was ready to issue, but some other warp issued instead. You may be able to sacrifice occupancy without impacting latency hiding and doing so may help improve cache hit rates.

Other - The warp is blocked for an uncommon reason.

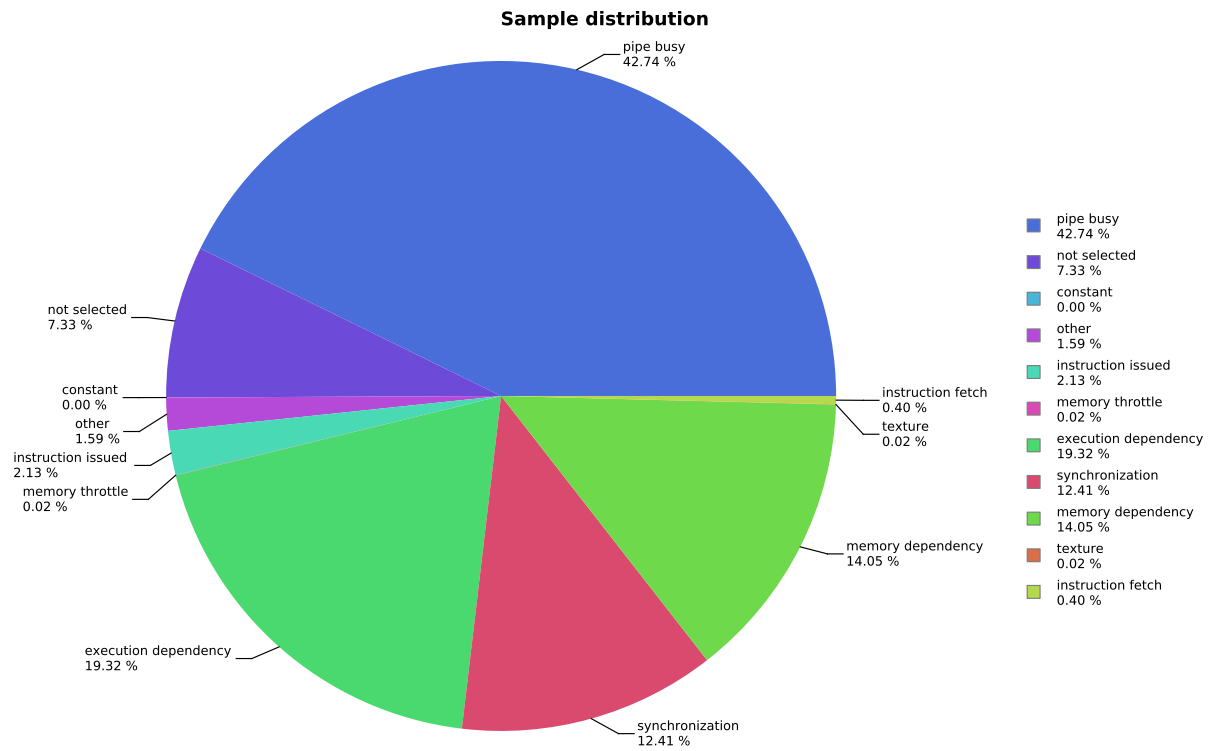
Sleeping -The warp is blocked, yielded or sleeping.

Examine portions of the kernel that have high number of samples to know where the maximum time was spent and observe the latency reasons for those samples to identify optimization opportunities.

| Cuda Functions | Sample Count | % of Kernel Samples |
|--|--------------|---------------------|
| d_gpu5(int, int, int, double*, double*, double*) | 4399941 | 100.0 |

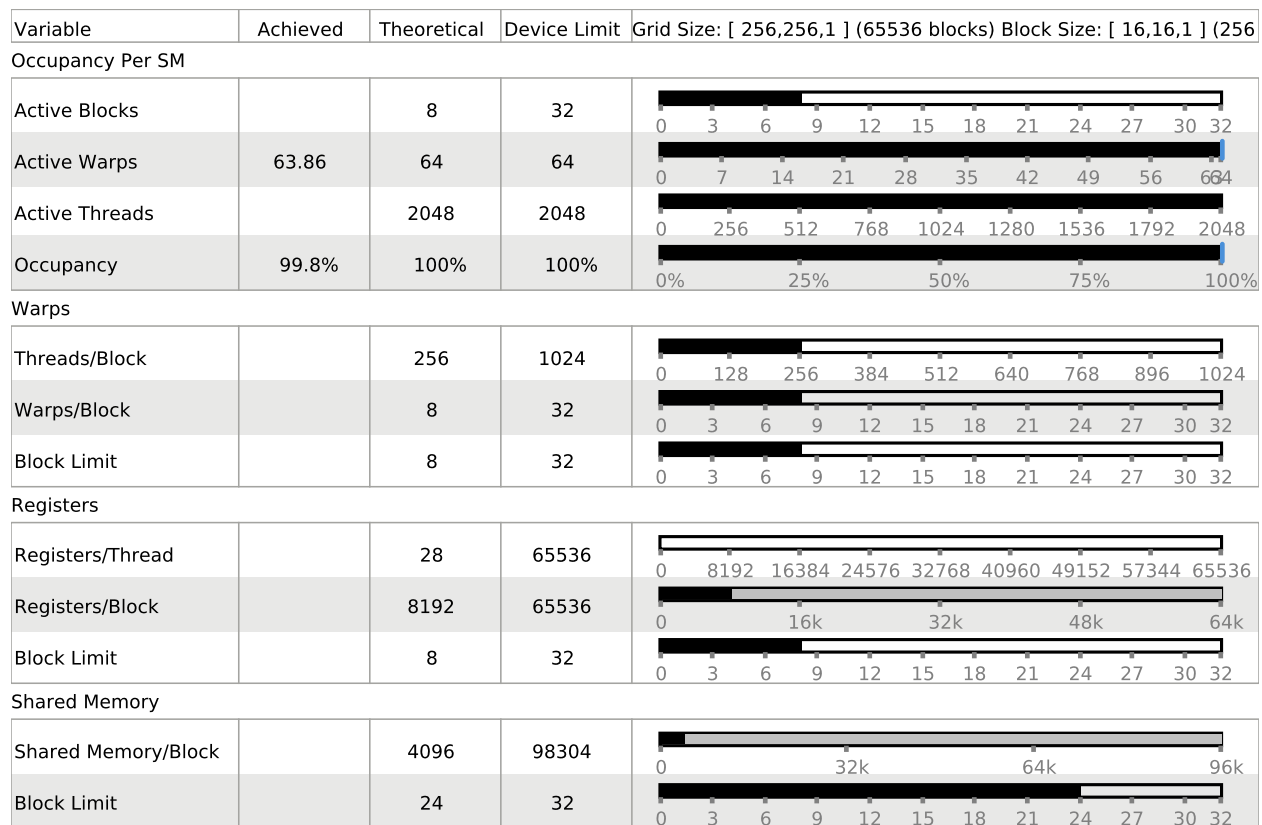
Source Files :

| |
|---|
| /zhome/a8/6/114633/hpc/week3/ass3/hpc-gpu/matmult/matmult_gpu5.cu |
|---|



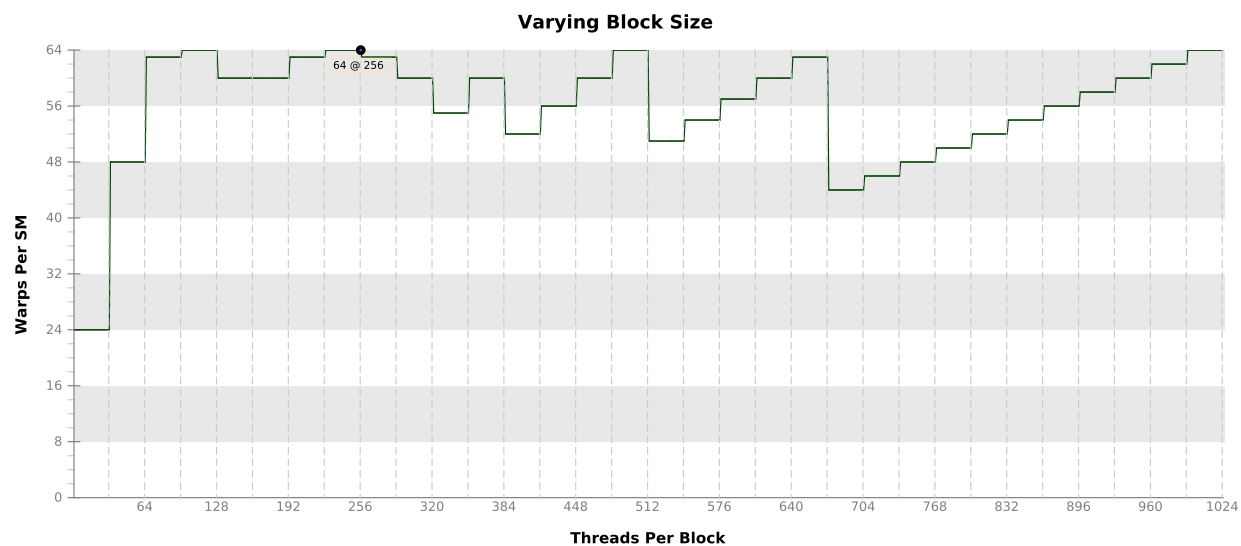
4.2. Occupancy Is Not Limiting Kernel Performance

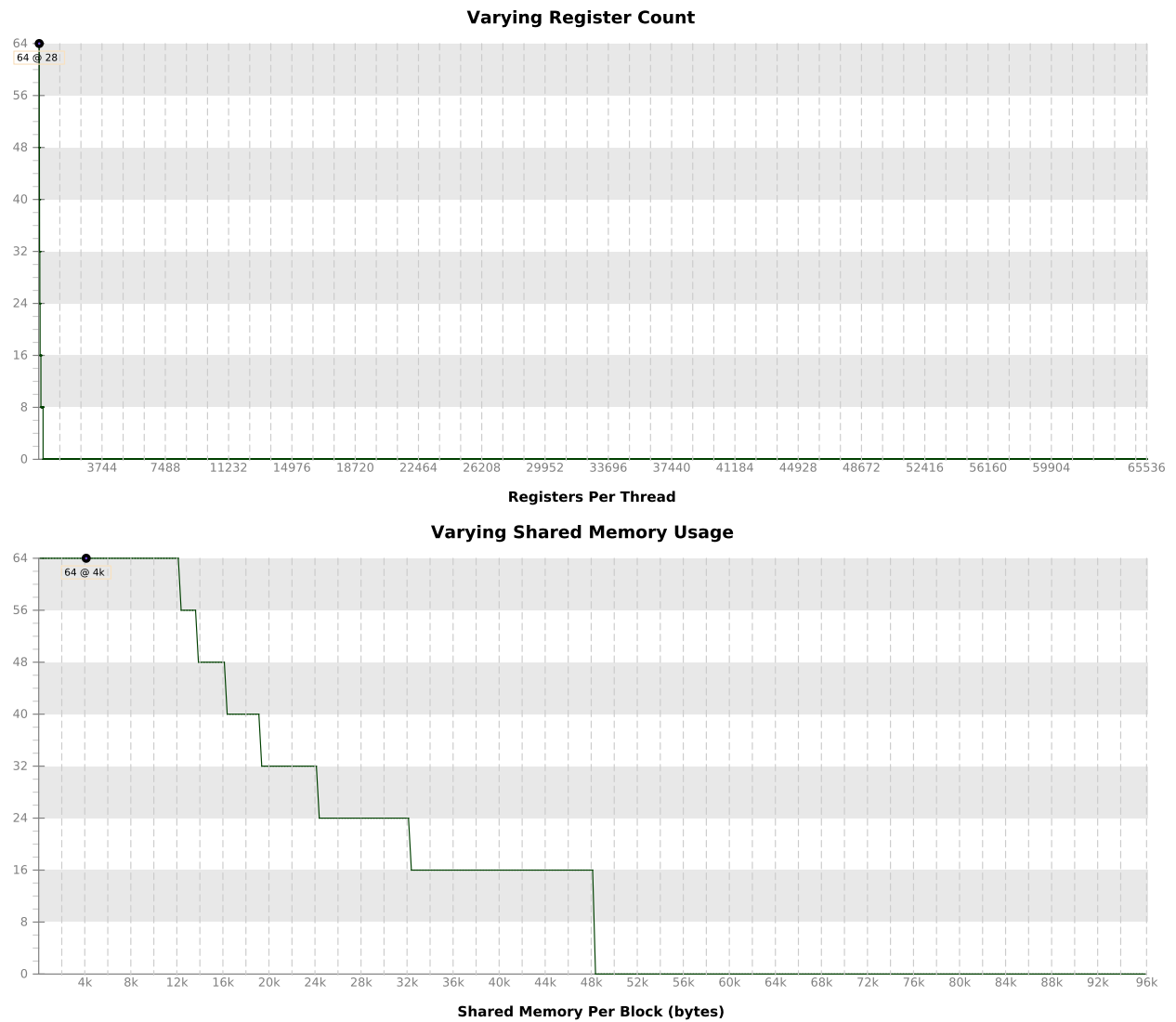
The kernel's block size, register usage, and shared memory usage allow it to fully utilize all warps on the GPU.



4.3. Occupancy Charts

The following charts show how varying different components of the kernel will impact theoretical occupancy.





4.4. Multiprocessor Utilization

The kernel's blocks are distributed across the GPU's multiprocessors for execution. Depending on the number of blocks and the execution duration of each block some multiprocessors may be more highly utilized than others during execution of the kernel. The following chart shows the utilization of each multiprocessor during execution of the kernel.

