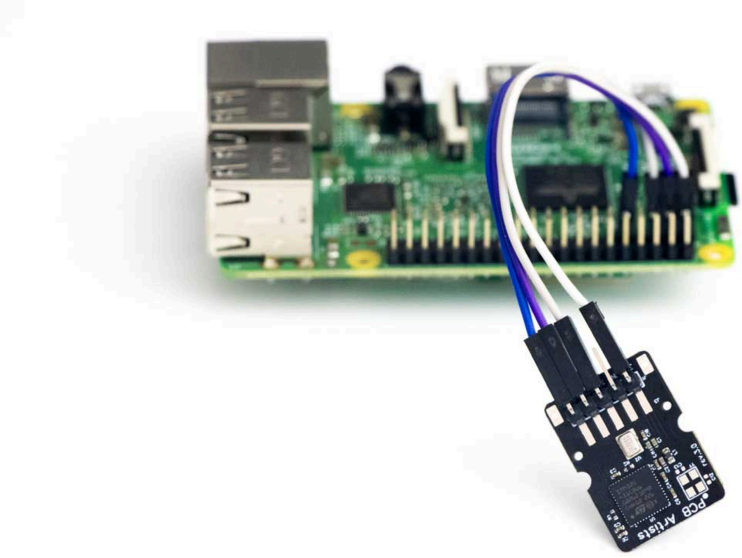
Product Documentation

I2C DECIBEL METER PROGRAMMING MANUAL

This decibel meter programming manual contains all the information that you will need to communicate with the decibel sensor module over I2C interface. All relevant registers and their bits have been described, along with their default states on power-up.

If you are new to the PCB Artists sound level module, this programming manual should be read along with the module interfacing reference.



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Decibel Meter Programming Basics

The I2C decibel meter uses an I2C interface for communication with a host. No particular initialization sequence is necessary and the module powers up with a commonly used combination of settings:

- A-weighting, suitable for general measurement
- 1000 ms averaging duration ("slow mode" on commercial sound meters)
- Interrupt function disabled
- Decibel history registers are updated every averaging duration (1000 ms) and min/max count is tracked

These settings can be changed and some other advanced settings can be configured using the I2C registers listed in this programming guide.

I2C Interface and Communication

Communicating with the Decibel Meter Module

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The PCB Artists sound level meter is ready for communication over I2C **within 5 ms of power-up**.
The host can communicate with the module by accessing the 7-bit **device I2C address** (**0x48 by default**, unless you ordered a custom module).

The host can then **read the DECIBEL register any time** for reading the latest sound intensity level in decibels (dB SPL). The decibel value usually takes about 1 second to stabilize after power-up.

Naming convention used for this section to describe I2C operations are:
DEV_ADDR – I2C device address
REG_ADDR – Device register address to read from or write to
R/W Read/write bit in the I2C device address frame
ACK – Acknowledge condition on the I2C bus
NACK – No-acknowledge condition on the I2C bus
START – Start condition on the I2C bus
STOP – Stop condition on the I2C bus
RESTART – Re-start or (stop + start) condition on the I2C bus

> To verify that I2C communication works, you can use the SCRATCH register to perform a write-read-verify sequence.

I2C Single Byte Write Sequence

- Generate a START condition
- Send DEV_ADDR with R/W bit set to ‘0’ (write)
- Send REG_ADDR
- Send the data byte to be written at REG_ADDR
- Generate a STOP condition

I2C Single Byte Read Sequence

- Generate a START condition
- Send DEV_ADDR with R/W bit set to ‘0’ (write)
- Send REG_ADDR
- Generate a RESTART condition
- Send DEV_ADDR with R/W bit set to ‘1’ (read)
- Read data from REG_ADDR
- Generate a STOP condition

I2C Multi-Byte Write Sequence

- Generate a START condition
- Send DEV_ADDR with R/W bit set to ‘0’ (write)
- Send REG_ADDR
- Send consecutive data bytes to be written starting at REG_ADDR
- Generate a STOP condition

I2C Multi-Byte Read Sequence

- Generate a START condition
- Send DEV_ADDR with R/W bit set to ‘0’ (write)
- Send REG_ADDR
- Generate a RESTART condition
- Send DEV_ADDR with R/W bit set to ‘1’ (read)
- Read consecutive data bytes starting at REG_ADDR

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SEND MESSAGE

- Generate a STOP condition

I2C Decibel Meter Module Register Map

The PCB Artists decibel meter contains the following registers. The host should not try to read from or write to undocumented locations as they are reserved for diagnostics and calibration.

VERSION register (0x00)

ADDRESS	DEFAULT VALUE	TYPE
0x00	See Notes	R/O

DESCRIPTION

- **BIT [7:4] – HW Version**
  Hardware version
- **BIT [3:0] – FW Version**
  Firmware version

ID3-ID0 registers (0x01-0x04)

ADDRESS	DEFAULT VALUE	TYPE
0x01 – 0x04	unique ID	R/O

DESCRIPTION

- **BIT [31:0] – Device ID**
  32-bit unique device ID (4 bytes)

SCRATCH register (0x05)

ADDRESS	DEFAULT VALUE	TYPE
0x05	0xAA	R/W

DESCRIPTION

- **BIT [7:0] – Scratch**
  Scratchpad register, host may write and read any value from this register at any time.
  Writing and reading back values from this register may be useful for I2C testing.

CONTROL register (0x06)

ADDRESS	DEFAULT VALUE	TYPE
0x06	0x02	R/W

DESCRIPTION

- **BIT [7:5] – Reserved**
  Do not write 1 to these bits
- **BIT [4] – Interrupt Type**
  Set to enable minimum/maximum level interrupts.
  – If 1, THR_MIN and THR_MAX registers are used as threshold values. When a decibel reading falls outside the range set by THR_MIN and THR_MAX, interrupt pin is activated.
  – If 0, INT pin goes low when 90 of the 100 DB_HISTORY registers are filled with readings.
- **BIT [3] – Interrupt Enable**
  Set to enable the interrupt pin operation. INT pin goes low to indicate a pending interrupt.
  A pending interrupt must be cleared by writing to the RESET register.
- **BIT [2:1] – Filter Selection**
  00 – None
  01 – A-weighting (default)
  10 – C- weighting
  11 – Reserved
- **BIT [0] – Power Down**
  Set this bit to power down the decibel sensor. Writing a 0 does nothing.
  NOTE: To power up the module, the host must set bit [3] of RESET register to cause a module reset. Failing to do so can put the module in an unknown state. After wake-up and reset, the module settings are restored to their power-up default state and application can use the module as usual.

TAVG high byte register (0x07)

ADDRESS	DEFAULT VALUE	TYPE
0x07	0x03	R/W

DESCRIPTION

- **BIT [7:0] – Tavg_high**
  Averaging time (high byte) in milliseconds for calculating sound intensity levels.
  Set [Tavg_high:Tavg_low] = 1,000 for slow mode intensity measurement.
  Set [Tavg_high:Tavg_low] = 125 for fast mode intensity measurement.

TAVG low byte register (0x08)

ADDRESS	DEFAULT VALUE	TYPE
0x08	0xE8	R/W

DESCRIPTION

- **BIT [7:0] – Tavg_low**
  Averaging time (low byte) in milliseconds for calculating sound intensity levels.
  Set [Tavg_high:Tavg_low] = 1,000 for slow mode intensity measurement.
  Set [Tavg_high:Tavg_low] = 125 for fast mode intensity measurement.
  NOTE: Writing to Tavg_low causes the combined value of Tavg_high:Tavg_low to take effect.
  Therefore, Tavg_high must be written first.

RESET register (0x09)

ADDRESS	DEFAULT VALUE	TYPE
0x09	0x00	W/O

DESCRIPTION

- **BIT [7:4] – Reserved**
- **BIT [3] – System Reset**
  Set this bit to perform a soft system reset and restore settings to defaults. This bit is automatically cleared.
  NOTE: This bit must be set to wake up the device from sleep mode.
- **BIT [2] – Clear History**
  Set this bit to clear the most recent 100 decibel values stored in history registers. This bit is self-clearing.
- **BIT [1] – Clear MIN/MAX**
  Set this bit to clear the maximum and minimum dB values stored in MAX and MIN registers. This bit is self-clearing.
- **BIT [0] – Clear Interrupt**
  Set this bit to clear interrupt signal and set INT pin to high-Z. This bit is self-clearing.

DECIBEL register (0x0A)

ADDRESS	DEFAULT VALUE	TYPE
0x0A	0x00	R/O

DESCRIPTION

- **BIT [7:0] – Decibel**
  Latest sound intensity value in decibels, averaged over the last Tavg time period.
  The decibel reading is only valid after about 1 second of module power-up.

MIN register (0x0B)

ADDRESS	DEFAULT VALUE	TYPE
0x0B	undefined	R/O

DESCRIPTION

- **BIT [7:0] – Minimum Reading**
  Minimum value of decibel reading captured since power-up or manual reset of MIN/MAX registers.

MAX register (0x0C)

ADDRESS	DEFAULT VALUE	TYPE
0x0C	undefined	R/O

DESCRIPTION

- **BIT [7:0] – Maximum Reading**
  Maximum value of decibel reading captured since power-up or manual reset of MIN/MAX registers.

THR_MIN register (0x0D)

ADDRESS	DEFAULT VALUE	TYPE
0x0D	45	R/W

DESCRIPTION

- **BIT [7:0] – Lower Threshold**
  Minimum decibel value (threshold) under which interrupt should be asserted.

THR_MAX register (0x0E)

ADDRESS	DEFAULT VALUE	TYPE
0x0E	85	R/W

DESCRIPTION

- **BIT [7:0] – Upper Threshold**
  Maximum decibel value (threshold) above which interrupt should be asserted.

DBHISTORY_0 to DBHISTORY_99 (0x14 to 0x77)

ADDRESS	DEFAULT VALUE	TYPE
0x14 to 0x77	0x00	R/O

DESCRIPTION

- **BIT [7:0] – History**
  Past decibel values arranged in a queue, captured every “Tavg” milliseconds.
  DBHISTORY_0 contains the latest value and DBHISTORY_99 contains the oldest value available.
  When the queue is full, the oldest value at DBHISTORY_99 is deleted to insert new value at DBHISTORY_00.

FREQ_64BINS_0 to FREQ_64BINS_63 (0x78 to 0xB7)

ADDRESS	DEFAULT VALUE	TYPE
0x78 to 0xB7	undefined	R/O

DESCRIPTION

- **BIT [7:0] – Frequency Component Values in dB SPL**
  Frequency components of the signal represented as 64 bands (8 kHz total band width). The number represents the magnitude of the frequency component in dB SPL.

No weighting filters are applied to frequency data. Exponential time averaging period is determined by “Tavg” value.
NOTE: This feature is only available in Spectrum Analyzer version of the module (VERSION = 0x32)

FREQ_16BINS_0 to FREQ_16BINS_15 (0xB8 to 0xC7)

ADDRESS	DEFAULT VALUE	TYPE
0xB8 to 0xC7	undefined	R/O

DESCRIPTION

- **BIT [7:0] – Frequency Component Values in dB SPL**
  Frequency components of the signal represented as 16 bands (8 kHz total band width). The number represents the magnitude of the frequency component in dB SPL.
  No weighting filters are applied to frequency data. Exponential time averaging period is determined by “Tavg” value.
  NOTE: This feature is only available in Spectrum Analyzer version of the module (VERSION = 0x32)

Firmware Version Notes

Several versions of the decibel sound level meter module are available for purchase. Here are some notes on the hardware/firmware versions available.

VERSION = 0x31 (MEMS mic version, long term support and available for sale)

Sensor module with Hardware v3 + Firmware v1 is currently available for sale on our store and will be supported for long term use. It contains a MEMS microphone and is easy to mount on an enclosure with a double sided tape.
Any future firmware updates will retain backward compatibility with firmware v1.

Hardware v3 + Firmware v1 notes:

- All registers and functions documented above are implemented
- Changing weight settings takes at least one Tavg period to take effect. Host should clear min/max and history records.

VERSION = 0x32 (version 0x31 features + audio spectrum analyzer)

Sensor module with Hardware v3 + Firmware v2 is currently available for sale on our store and supports audio spectrum analysis in addition to all the features listed for version = 0x31.
Firmware version = 0x32 is backward compatible with firmware version = 0x31.

Hardware v3 + Firmware v2 notes:

- Rolling average implementation for the frequency bins is not a real rolling average implementation. Instead, it uses a modified version of exponential moving average with low pass filtering to provide jitter-free averaging performance.
- Frequency bin registers from 0x78 to 0xC7 are only implemented on this version of the module.

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Change Log

- **11 January 2024**
  – Added FREQ BIN registers for spectrum analyzer version of the module
- **11 October 2023**
  – Added VERSION = 0x32 and audio spectrum analysis feature documentation
- **13 May 2023**
  – Update descriptions of Control and Reset registers
  – Change behavior of Int Type and Power Down bits in Control register
- **6 May 2023**
  – Initial release

DECIBEL METER SENSOR SOUND SENSOR

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