Experiment #1:

Introductory Experiment

Lab Report

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Lab Section:

1. **Introduction:**
   Lab 1: Introductory Experiment is to design a 2 to 1 MUX only using NAND gate COMS chips. The purpose of experiment 1 is to show there is a glitch between the gate level. The first part of the experiment is to design a 2 to 1 MUX by using the knowledge that we learned from ECE 120, and then we will observe a glitch on the scope. Then, we need to modify our design to glitch-free circuit by adding extra term to avoid a possibly of static-1 hazard.
2. **Written Description of the circuit**
   a. **Logic Pin Assignments**

Logic pins	Logic description
A	one of the logic inputs of the MUX
B	select signal of the MUX
C	one of the logic inputs of the MUX
Z	output of the MUX

   b. **Description of the design**

2 to 1 MUX allows you to select between 2 inputs. Logic pin B acts select signal to select between two inputs A and B respectively. Z serves as output and it contains the result of which input that B selects. MUX acts like a digital switch box between two signals.
In order to eliminate the possibly of static-1 hazard or glitches. We add another midterm that cover neighboring midterms, which it prevents glitch to happen. therefore, it adds one more NAND to our circuit design.

   c. **K-Maps, State diagrams, truth tables, Boolean expression**

Truth table is provided below.

A	B	C	Z
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

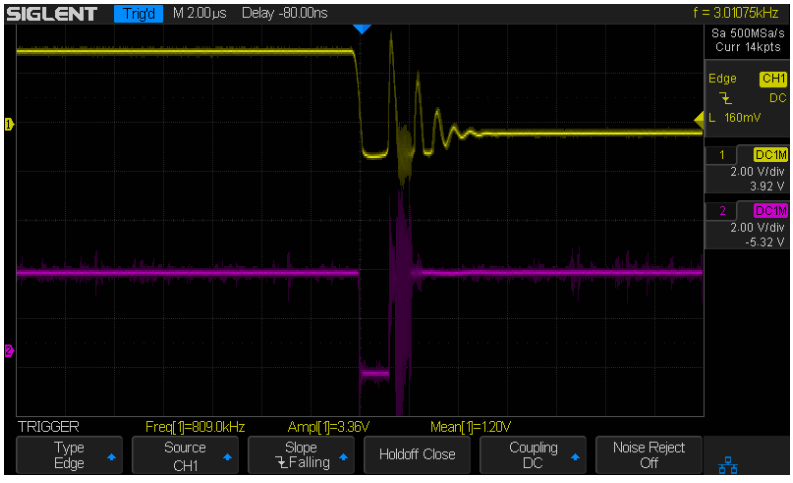
K-Mapping

	B'C'	B'C	BC	BC'
A	0	1	0	0
A'	0	1	1	1

the Boolean expression is Z = B'C + BC for the navie design. Since we want to a glitch free circuit, we need to add a mid-term that covers the neighboring k-mapping, and extra midterm is AC, therefore the Boolean expression of glitch-free design is Z = B'C + BC + AC

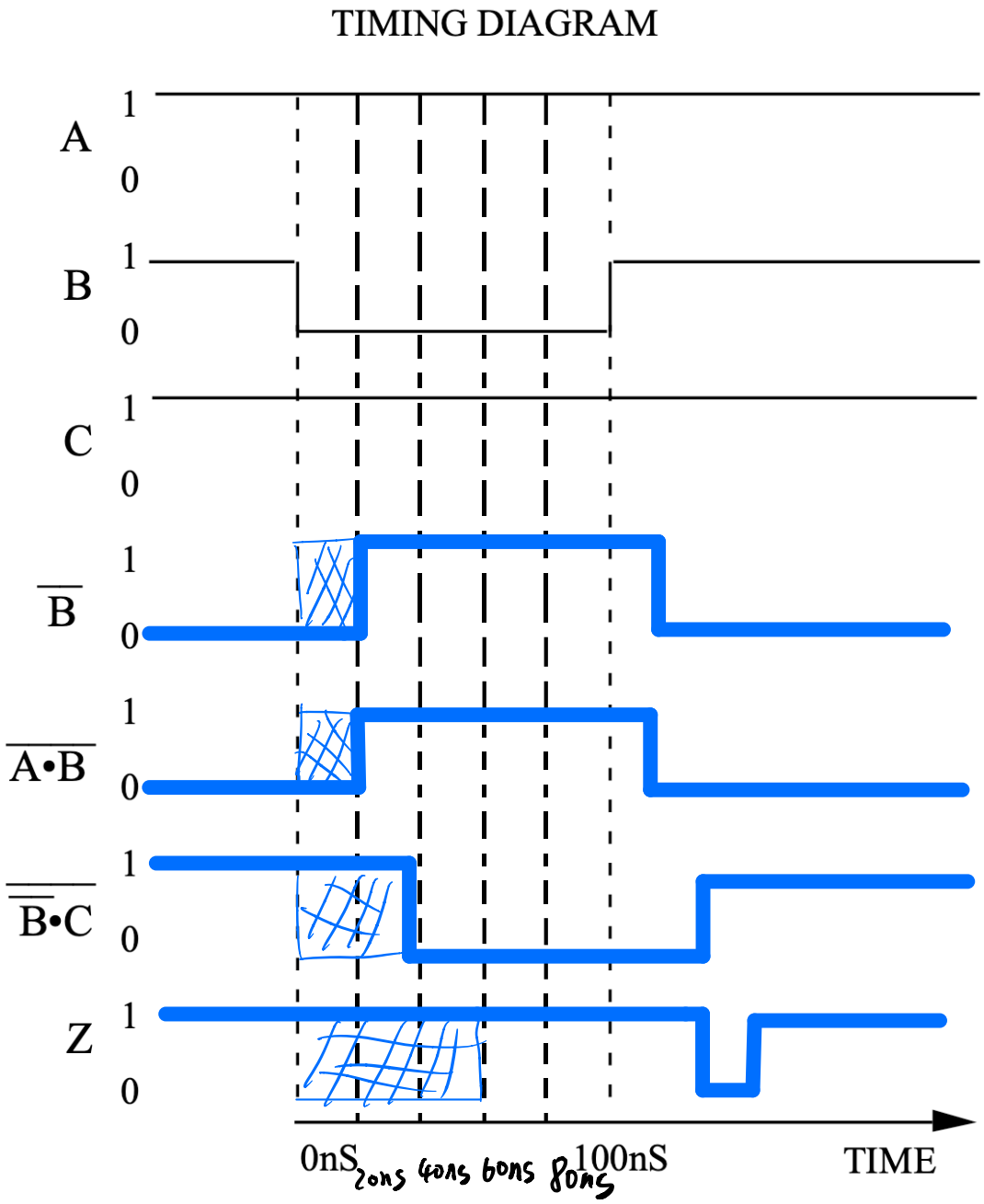
3. **High Level Block Diagram/Circuit Diagrams/Component layout**
   see the attachment at the end of the lab report
4. **Documentation**
   a. **Answer for Pre-Lab questions**
      i. I think not all groups may observe the static hazard due the gate delay is not significant big to have a static hazard. Also, it is the reason that professor Cheng in his video, he added 1uf capacity to increase the gate delay on the inverter in order to observe a glitch on the scope.
   b. **Answer for Lab questions**
      i. We redesigned the glitch free circuits and its result is the same thing that we had from part A. See the attachment for outputs image on the oscilloscope. The falling edge of the input B is more likely to observe a glitch at the output, because the input B because an extra gate level and due to the gate delay, therefore, the input B is more likely to observe a glitche.
      ii. Here is the truth table of the output. It responds like the circuit of part of A. We observed that at the falling edge of the input B is more likely to observe a glitch at the output. because the input B has an invert gate which is extra one gate delay, therefore it is more likely to observe a glitch at the output.

A	B	C	Z
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1



c. Answer for Post-Lab questions

i.



ii. De-bouncing circuit is built from an SPDT switch by using the pull-up resistor connect to double toggles, and a single throw is connected with GND. Toggles inputs will connect with NOT(S)-NOT(R) latch. The ill effect of the debouncing switch eliminates problem caused by switch contact bounce. It will give us a clean transition a logic zero to logic one, or vice versa.

5. General Guide Question Answers

i. The advantage of a larger noise immunity is the logic level will not change easily due to the effect of noise. The last inverter observed rather than the simply the first, because over many time sof the inverting, the logic one is losing its voltage on the gate level, therefore we can calculate the noise immunity. Then noise immunity for the inverter should be 3.5-1.35 = 2.2V.

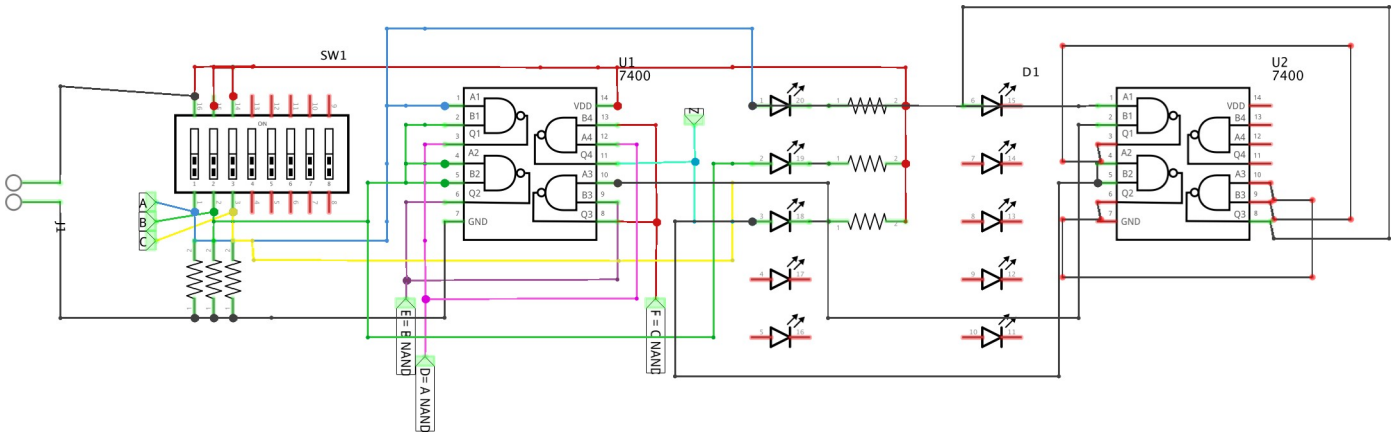
ii. The 1uF capacity is necessary near by the COMS chips, because it acts like a decoupling capacity, because it provides enough power to COMS IC to keep the voltage stable to void short circuit.

iii. The reason that we cannot share resistors between LEDS is to avoid burn or damage the LEDS driver IC. Each LED driver IC only can sink 16 mA maximum. If we shared the resistor between LEDS, the current cross is much higher than the limitation.

6. Conclusion

Experiment 1 taught us about glitch, and the way how we eliminate a possibility of static 1 or static 0 hazard. It gave us a fully understanding about glitches.

ATTACHMENT



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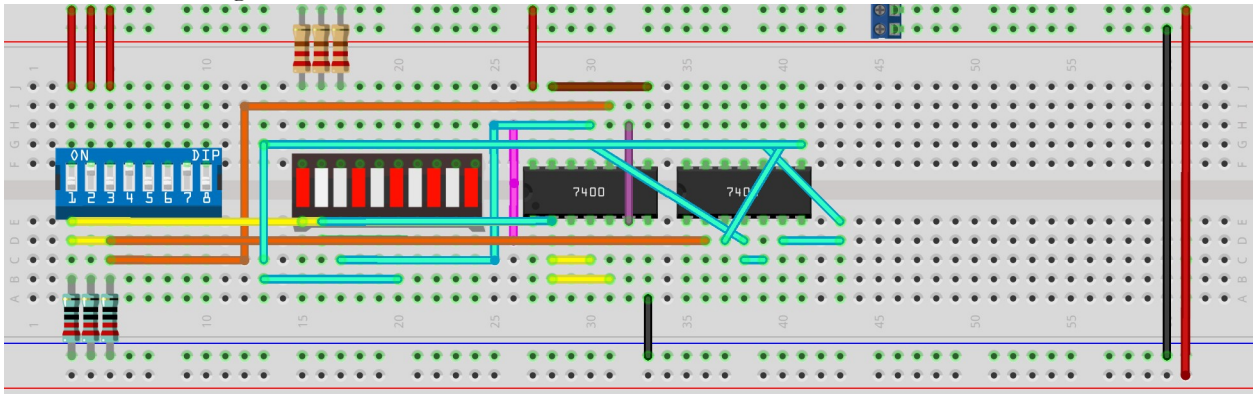

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