General Single-PORT SRAM
8192 WORDS X 32 BITS, MUX 16
SMIC 55nm LL Logic Process

Version 1.1.a

OVERVIEW

The General Single-PORT SRAM is designed for SMIC's 55nm CMOS Logic process. The memory is optimized for speed, power and area. It operates at a voltage range of 1.08V to 1.32V and a temperature range of -40°C to 125°C.

The write enable (WEN), chip enable (CEN), address (A) and data in (D) signals are latched on the rising-edge of the clock. When CEN is low and WEN is high, the memory will be in read operation. Data is read from the location specified by the address A[0:i], and is output on the output port Q[0:n].When CEN is low, WEN is low and BWEN[j] is high, the memory will be in read operation. Data D[j] is read from the location specified by the address A[0:i], and is output on the output port Q[j].When CEN is low, WEN is low and BWEN[j] is low the memory will be in write operation, the corresponding data on the data port D[j] will be written into the location specified by the address A[0:i] and the data will appear on the corresponding output port Q[j].When CEN is high the memory is in standby mode. Meanwhile, the data stored in memory is retained but cannot be read or written.

CONFIGURATION:

PARAMETER	VALUE
Mux	16
Words	8192
Bits	32
Width	569.26um
Height	307.045um
Area	174788.437um^2

PIN DEFINITION:

PIN	DIRECTION	DEFINITION
A[12:0]	Input	Address Inputs
D[31:0]	Input	Data Inputs
WEN	Input	Write Enable
CEN	Input	Chip Enable
CLK	Input	Clock Input
Q[31:0]	Output	Data Outputs

TIMING:

PARAMETER	DESCRIPTION	FF CORNER 1.32V, -40°C		FF CORNER 1.32V, 0°C		FF CORNER 1.32V, 125°C		SS CORNER 1.08V, -40°C		SS CORNER 1.08V, 125°C		TT CORNER 1.2V, 25°C	
(ns)		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
Tcyc	Cycle Time	0.565		0.595		0.675		3.046		2.987		1.510	
Ta	Access Time[1]	0.514		0.541		0.614			2.769		2.715		1.372
Tah	Address Hold	0.114		0.114		0.114		0.229		0.147		0.122	
Tas	Address Setup	0.404		0.404		0.428		0.697		0.681		0.424	
Tch	Cen Hold	0.042		0.039		0.033		0.032		0.000		0.019	
Tcs	Cen Setup	0.311		0.315		0.326		0.800		0.683		0.398	
Tdh	Data Hold	0.192		0.192		0.189		0.346		0.280		0.214	
Tds	Data Setup	0.289		0.321		0.347		0.781		0.781		0.294	
Twh	Wen Hold	0.092		0.088		0.073		0.196		0.086		0.084	
Tws	Wen Setup	0.300		0.299		0.348		0.467		0.443		0.295	
Tckh	Clock High	0.020		0.020		0.020		0.020		0.020		0.020	
Tckl	Clock Low	0.088		0.088		0.099		0.209		0.242		0.132	
Tckr	Clock Rise Skew	0.500		0.500		0.500		1.000		1.000		0.600	

Timing simulation conditions:

1. Access time = best case for fast corner and worst case for slow/typical corners

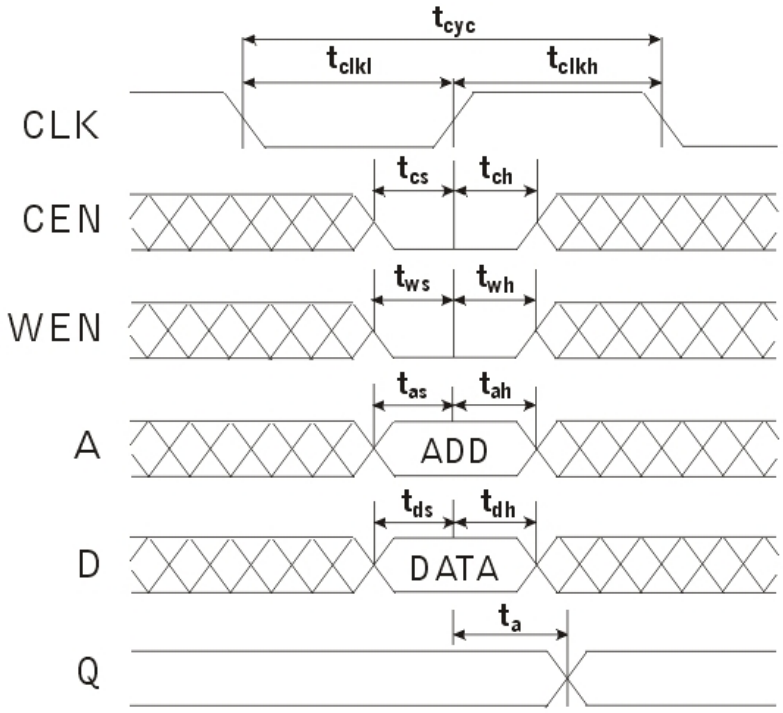
POWER:(UNITS=uA/Mhz)

PARAMETER	FF CORNER 1.32V, -40°C	FF CORNER 1.32V, 0°C	FF CORNER 1.32V, 125°C	SS CORNER 1.08V, -40°C	SS CORNER 1.08V, 125°C	TT CORNER 1.2V, 25°C
AC Current[2]	14.998	15.104	16.330	16.203	15.778	18.178
Read AC Current	14.240	14.345	15.400	15.397	15.010	17.443
Write AC Current	15.755	15.863	17.259	17.010	16.546	18.913
Standby Power (mW)	0.005067	0.025769	1.639130	0.000193	0.051999	0.005633
Deselect Power (mW)[3]	0.109744	0.114515	0.237071	0.063825	0.069225	0.085150

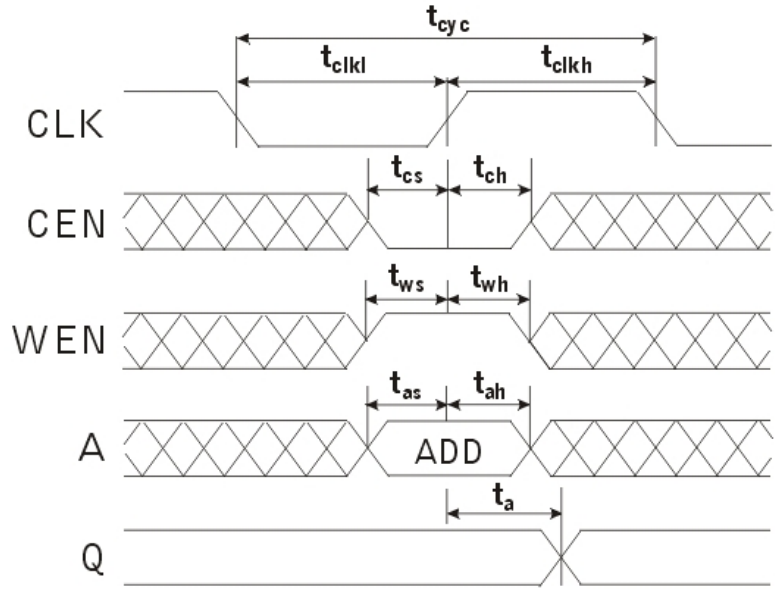
Power simulation conditions:

2. CEN is low, 50% read / 50% write operations, all addresses and 50% of input pins toggle at 1Mhz
3. CEN is high, 50% of input pins toggle at 1Mhz

WRITE CYCLE TIMING:



READ CYCLE TIMING:



Datasheet Revision History

Date	Version	Changes
	null	

Semiconductor Manufacturing International Corporation
No. 18 Zhangjiang Road
Pudong New Area
Shanghai 201203
The People Republic of China
URL: www.smics.com