Digital Design LU

Protocol

Lab Exercise I

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Structural modeling

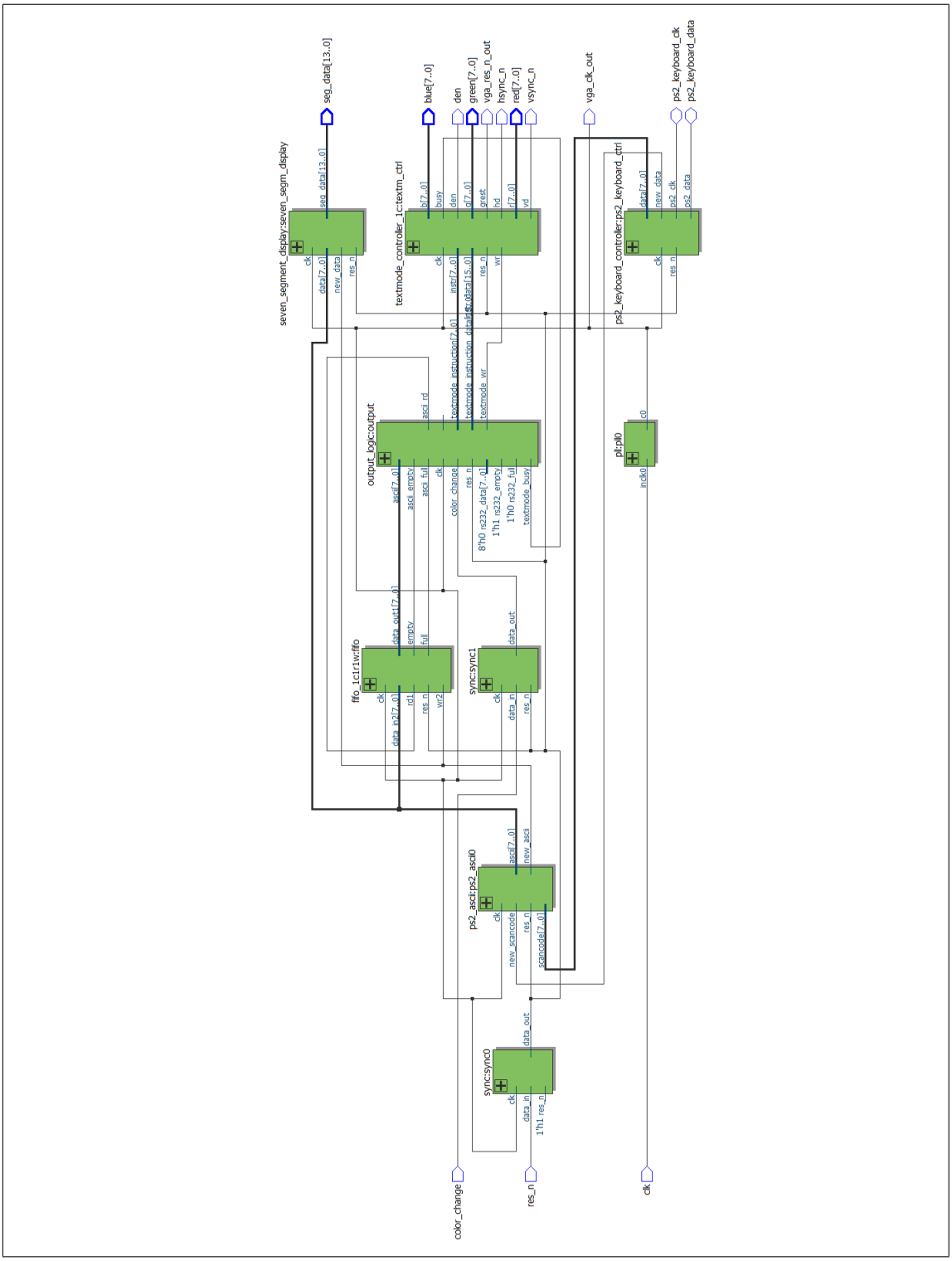

Figure 1: Screenshot showing the top level design in the RTL netlist viewer.

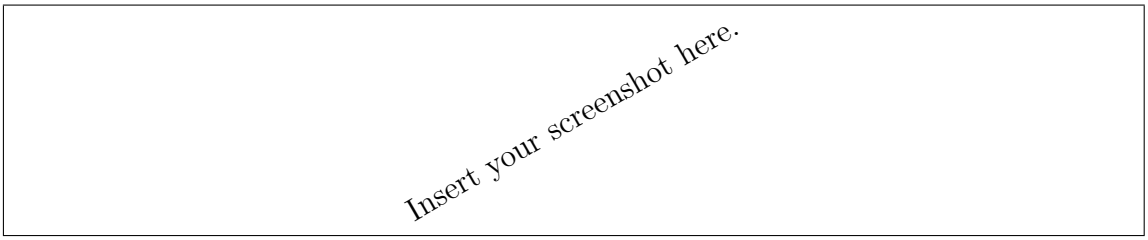

Figure 2: Screenshot of pin assignments.

Simulation

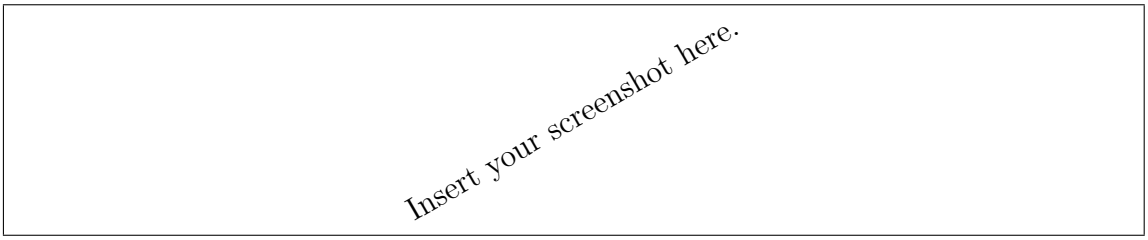

Figure 3: Three characters propagating from input to the displays

Table 1: Timing measurements

Time	Value
First transition of character input on PS2 to ASCII character output	? ns
ASCII character output to seven segment display update	? ns
ASCII character output to textmode instruction	? ns
1/Display frame rate (*vsync_n* period)	? ns

Question: Different propagation delays: How long is the transition time you measured when the seven segment display output bus changes its value and multiple signals toggle?

Answer: ...

Question: Describe how the bug in the *ps2_ascii* component affects the design.

Answer: ...

Behavioral Modeling

Question: Which baudrate did you use for the above simulation? How long should the transmission take for the whole frame (including start and stop bit)? What is the time you measured in the simulation (not including the stop bit)?

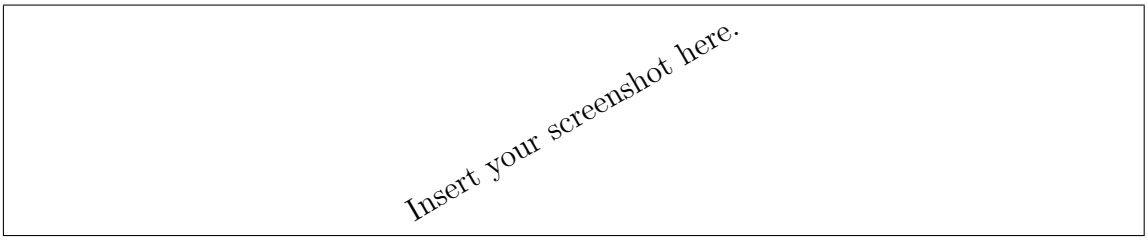

Figure 4: Different propagation delays on the seven segment display bus.

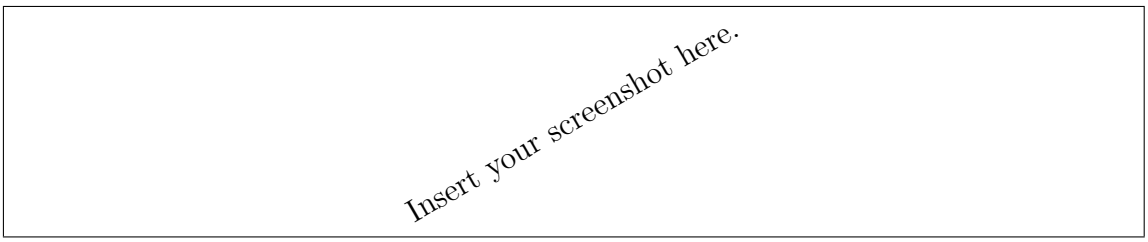

Figure 5: Screenshot of a simulation showing the reception of a whole UART frame.

Answer: ...

Table 2: Resouce usage of the serial module (including all submodules).

	LC Combinationals	LC Registers	Memory
Absolute number % of whole design % of whole FPGA resources			

Measurement

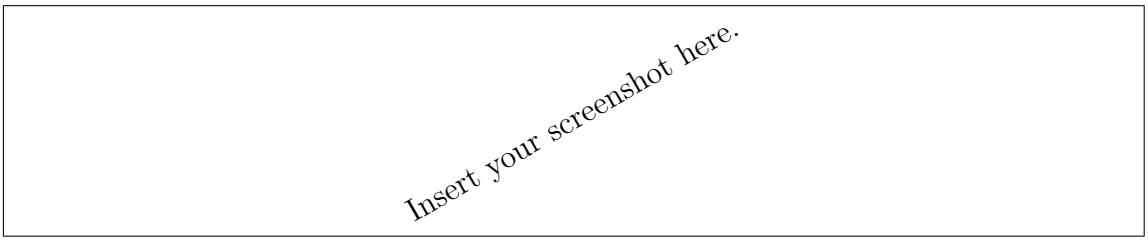

Figure 6: Screenshot of a measurement showing the duration of a whole UART frame sent from the FPGA to the computer.

Question: Which baudrate did you use for the hardware implementation? How long should the transmission take for the whole frame (including start and stop bit)? What is the time you measured (not including the stop bit)?

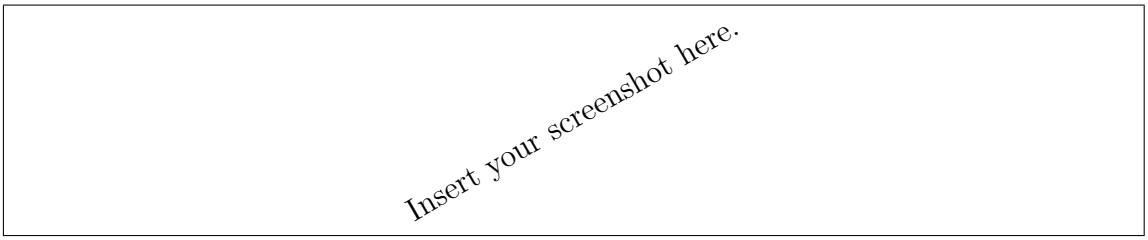

Figure 7: Screenshot of a display timing measurement showing the seventh visible pixel row.

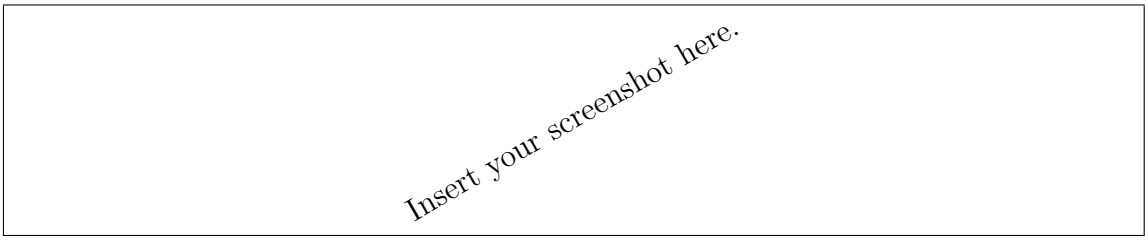

Figure 8: Screenshot of the trigger setting for finding the seventh row.

Answer: ...

Question: How long is the hsync-to-hsync interval you measured?

Answer: ...

Question: What is the sampling rate you used for this measurement?

Answer: ...

Question: What is the uncertainty you have to add to the measured time when sampling with this sample rate? ($\pm$? ns)

Answer: ...

Question: What is the maximum frequency that you could reliably display as a switching waveform at this sample rate (assuming a 50% duty cycle)?

Answer: ...

Feedback & Comments

By answering the optional questions below you can give us feedback and help us to further improve this lab course. Your answers will not influence your grading!

Question: How many hours did you need to solve this lab exercise? Please give us a rough estimate.

Answer:

Question: Were there any annoying problems you encountered (e.g. bugs in tools, flaws in the task description or documentation, etc.)?

Answer:

Question: Other remarks?

Answer: