Digital Design and Computer Architecture LU

Protocol

Lab Exercise II

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Simulation

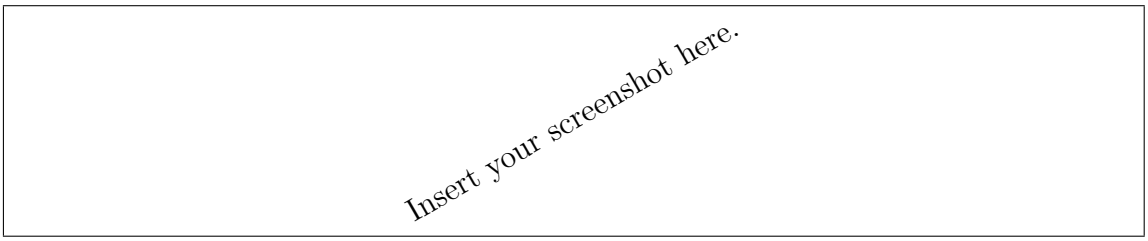

Figure 1: Screenshot of the simulation showing the operation of the LCD controller

Measurement

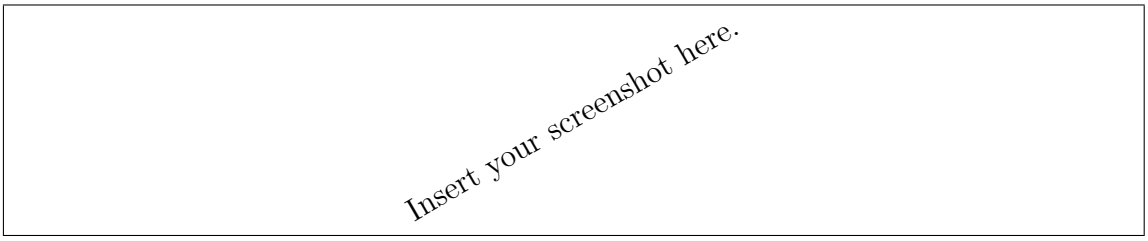

Figure 2: Screenshot of the SignalTap logic analyzer measurement

Question: How did you configure the trigger for the above measurement? If it is clear from a screenshot, you may answer with a figure.

Answer: ...

Question: Does the SignlTap LA provide corresponding acquisition modes for each acquisition mode of the Agilent LA in the lab? What are the differences?

Answer: ...

Question: What resources on the FPGA and board do you need to perform a measurement with the Agilent LA and what for the SignalTap LA?

Answer: ...

Question: (For SignalTap only.) Assuming you need a very low sampling frequency f_s to capture a long time window. How would you define a trigger that reliably stops acquisition when a glitch of length $f_s^{-1}/10$ occurs on a signal (Hint: You can assume the glitch is long enough to serve as a valid clock pulse for a flip flop. Also, you may ignore synchronization issues.)?

Answer: ...

Feedback & Comments

By answering the optional questions below you can give us feedback and help us to further improve this lab course. Your answers will not influence your grading!

Question: How many hours did you need to solve this lab exercise? Please give us a rough estimate.

Answer:

Question: Were there any annoying problems you encountered (e.g. bugs in tools, flaws in the task description or documentation, etc.)?

Answer:

Question: Other remarks?

Answer: