

## Lab: Add-Sub unit with Register file (3-ported RAM)

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## Table of contents

Objective.....	3
Specification.....	4
32-Bit Adder/Subtractor.....	5
2-Port RAM [32x32].....	6
3-Port RAM [32x32].....	8
Memory Initialization File [MIF].....	9
Instruction File.....	10
3-Port RAM Adder-Sub Unit .....	11
Simulations.....	12
3-Port RAM Adder-Sub Unit .....	12
Most Positive 32-bit Integer + 1.....	13
Most Positive 32-bit Integer – 1.....	14
Most Negative 32-bit Integer + 1.....	15
Most Negative 32-bit Integer – 1.....	16
Most Positive 32-bit Integer – Most Negative 32-bit integer.....	17
Most Positive 32-bit Integer + Most Negative 32-bit integer.....	18
Most Positive 32-bit Integer – Most positive 32-bit integer.....	19
Conclusion.....	20

## **Objective**

In this Laboratory Assignment, we will be Integrating an 32-bit Adder/Subtractor Unit into a 32 x 32 3-Port RAM with a Memory Instruction File(MIF). Furthermore, what will be included is a 32-bit MIPS like instruction that will be read and inputted into the 32-bit Adder/Subtractor unit.

## Specification

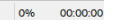
A 32-Bit MIPS like instruction is inputted in which is broken down in the **operation code [6 bits]**, **RS[5 bits]**, **RT[5 bits]**, **RD[5 bits]** with the remaining bits being 0's. **Operation code** is 6-bit long where if "000000", it will add and "000001" would be to subtract. Furthermore, **RS** and **RT** are the input values that we insert into the Adder/Subtractor unit and **RD** is where we are writing to. Next, we integrate an Adder/Subtractor Unit into the 3-Port Ram where the first 3 addresses of our MIF file are instantiated with the **Most Positive 32-Bit Integer**, **Most Negative 32-bit Integer** and **1**. The User will specify the address in the 32-bit instruction to obtain the 32-Bit Integer in which Addition or Subtraction can be performed on these values. After computation is completed, the value will be written into one of the 29 other addresses that were not instantiated in the MIF file. For example, we compute **Most Positive 32-Bit Integer + 1**, where once computations are finished, we can write the value into the 4<sup>th</sup> address in the MIF file which has not been instantiated.

```

1 library ieee;
2 use ieee.std_logic_1164.all;
3
4 entity ZHANG_SEPTMBER19_N_Bit_AddSub_Flag is
5     generic ( n : integer := 32); -- we can set this to whatever we want to test, for example 32
6     port ( ZHANG_SEPTMBER19_X, ZHANG_SEPTMBER19_Y : in std_logic_vector(n-1 downto 0);
7           ZHANG_SEPTMBER19_OP : in std_logic;
8           ZHANG_SEPTMBER19_S : out std_logic_vector(n-1 downto 0);
9           ZHANG_SEPTMBER19_Cout : out std_logic;
10          ZHANG_SEPTMBER19_Overflow, ZHANG_SEPTMBER19_Zero, ZHANG_SEPTMBER19_Negative: out std_logic);
11
12 end ZHANG_SEPTMBER19_N_Bit_AddSub_Flag;
13
14 architecture ZHANG_SEPTMBER19_behav of ZHANG_SEPTMBER19_N_Bit_AddSub_Flag is
15
16     signal ZHANG_SEPTMBER19_C, ZHANG_SEPTMBER19_SUM_BUFFER, ZHANG_SEPTMBER19_bxor, ZHANG_SEPTMBER19_zeroes : std_logic_vector(n-1 downto 0);
17
18     begin
19
20         ZHANG_SEPTMBER19_bxor_allocate: for i in 0 to n-1 generate -- OP xor Y, this to determine if we subtracting or not
21             ZHANG_SEPTMBER19_bxor(i) <= ZHANG_SEPTMBER19_OP xor ZHANG_SEPTMBER19_Y(i);
22         end generate;
23
24         ZHANG_SEPTMBER19_zero_allocate: for i in 0 to n-1 generate -- for zero flag, generates 'N' number of 0's
25             ZHANG_SEPTMBER19_zeroes(i) <= '0';
26         end generate;
27
28         process (ZHANG_SEPTMBER19_X, ZHANG_SEPTMBER19_bxor, ZHANG_SEPTMBER19_SUM_BUFFER, ZHANG_SEPTMBER19_OP, ZHANG_SEPTMBER19_C)
29         begin
30             ZHANG_SEPTMBER19_SUM_BUFFER(0) <= ZHANG_SEPTMBER19_X(0) xor ZHANG_SEPTMBER19_bxor(0) xor ZHANG_SEPTMBER19_OP;
31             ZHANG_SEPTMBER19_C(0) <= (ZHANG_SEPTMBER19_X(0) and ZHANG_SEPTMBER19_bxor(0)) or (( ZHANG_SEPTMBER19_X(0) xor ZHANG_SEPTMBER19_bxor(0)) and ZHANG_SEPTMBER19_OP);
32
33             for i in 1 to n-1 loop
34                 ZHANG_SEPTMBER19_SUM_BUFFER(i) <= ZHANG_SEPTMBER19_X(i) xor ZHANG_SEPTMBER19_bxor(i) xor ZHANG_SEPTMBER19_C(i-1);
35                 ZHANG_SEPTMBER19_C(i) <= (ZHANG_SEPTMBER19_X(i) and ZHANG_SEPTMBER19_bxor(i)) or ((ZHANG_SEPTMBER19_X(i) xor ZHANG_SEPTMBER19_bxor(i)) and ZHANG_SEPTMBER19_C(i-1));
36             end loop;
37
38         end process;
39
40         ZHANG_SEPTMBER19_Cout <= ZHANG_SEPTMBER19_C(n-1);
41         ZHANG_SEPTMBER19_S <= ZHANG_SEPTMBER19_SUM_BUFFER;
42         ZHANG_SEPTMBER19_Overflow <= ZHANG_SEPTMBER19_C(n-1) xor ZHANG_SEPTMBER19_C(n-2);
43         --ZHANG_SEPTMBER19_Zero <= '1' when ZHANG_SEPTMBER19_SUM_BUFFER = ZHANG_SEPTMBER19_zeroes else '0'; -- if sum == only zeroes, 1 else 0
44         ZHANG_SEPTMBER19_Zero <= '1';
45         ZHANG_SEPTMBER19_Negative <= ZHANG_SEPTMBER19_SUM_BUFFER(n-1); -- left most bit determines if it is negative or not
46
47     end ZHANG_SEPTMBER19_behav;
48

```

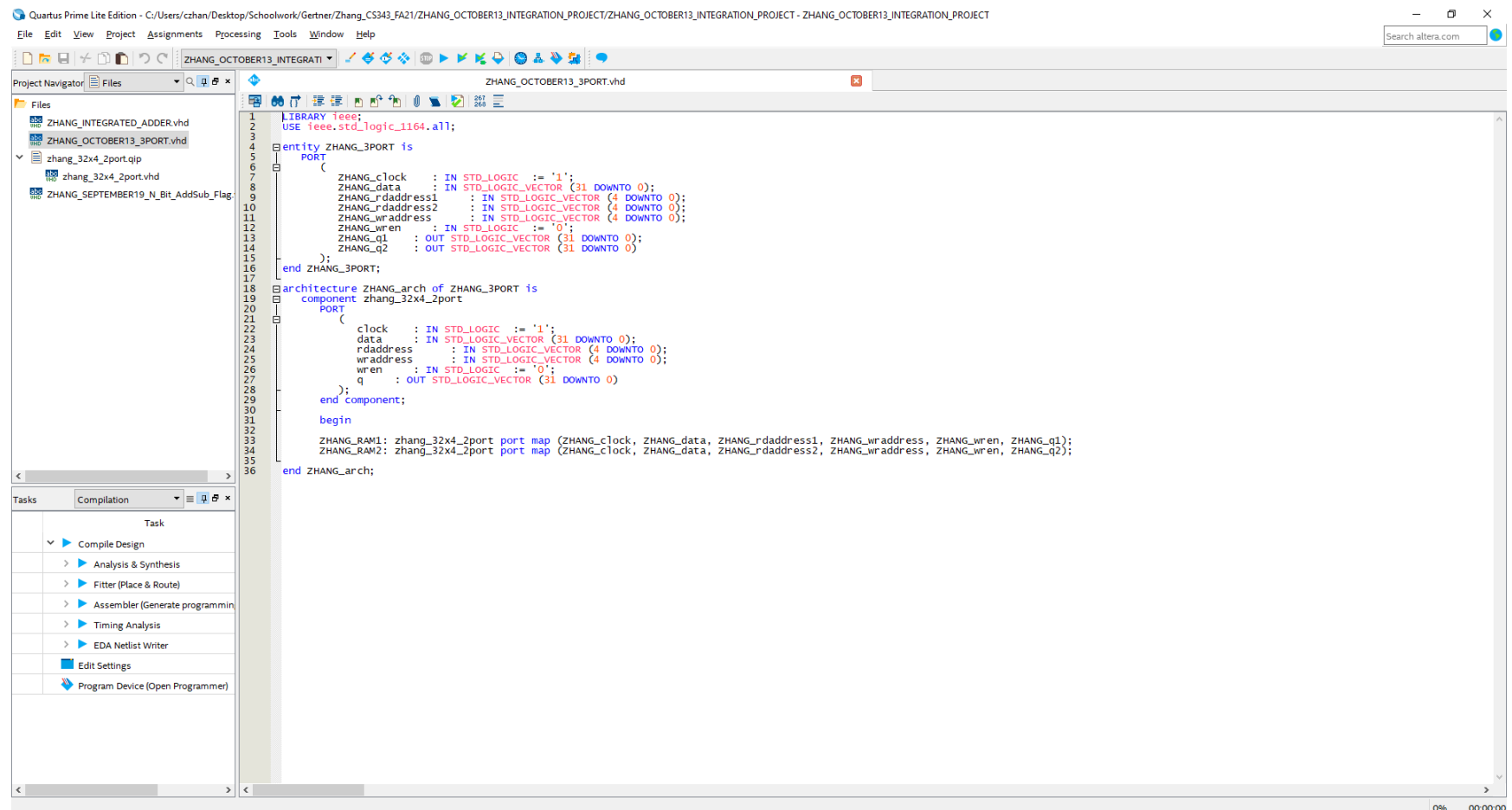
32-Bit Adder/subtractor unit that was created previously in the Adder Laboratory assignment. What is included is logic that detects for Overflow, Negative and Zero as well as an Operator Bit that determines whether or not a number should perform subtraction or addition.



```

66 address_reg_b => "CLOCK0",
67 clock_enable_input_a => "BYPASS",
68 clock_enable_input_b => "BYPASS",
69 clock_enable_output_b => "BYPASS",
70 init_file => "ram32x32.mif",
71 intended_device_family => "Cyclone V",
72 lpm_type => "altsyncram",
73 numwords_a => 32,
74 numwords_b => 32,
75 operation_mode => "DUAL_PORT",
76 outdata_aclr_b => "NONE",
77 outdata_reg_b => "UNREGISTERED",
78 power_up_uninitialized => "FALSE",
79 ram_block_type => "M10K",
80 read_during_write_mode_mixed_ports => "DONT_CARE",
81 widthad_a => 5,
82 widthad_b => 5,
83 width_a => 32,
84 width_b => 32,
85 width_byteena_a => 1
86 )
87 PORT MAP (
88   address_a => waddress,
89   address_b => raddress,
90   clock0 => clock,
91   data_a => data,
92   wren_a => wren,
93   q_b => sub_wire0
94 );
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100 END SYN;
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```



The code above showcases the usage of the previously generated 2-Port RAM in developing a 3-Port RAM. In a 3-port RAM, what is included is 2 read addresses and two q's which are the outputs after reading an address. Notice ZHANG\_raddress1, ZHANG\_raddress2, ZHANG\_q1 and ZHANG\_q2.

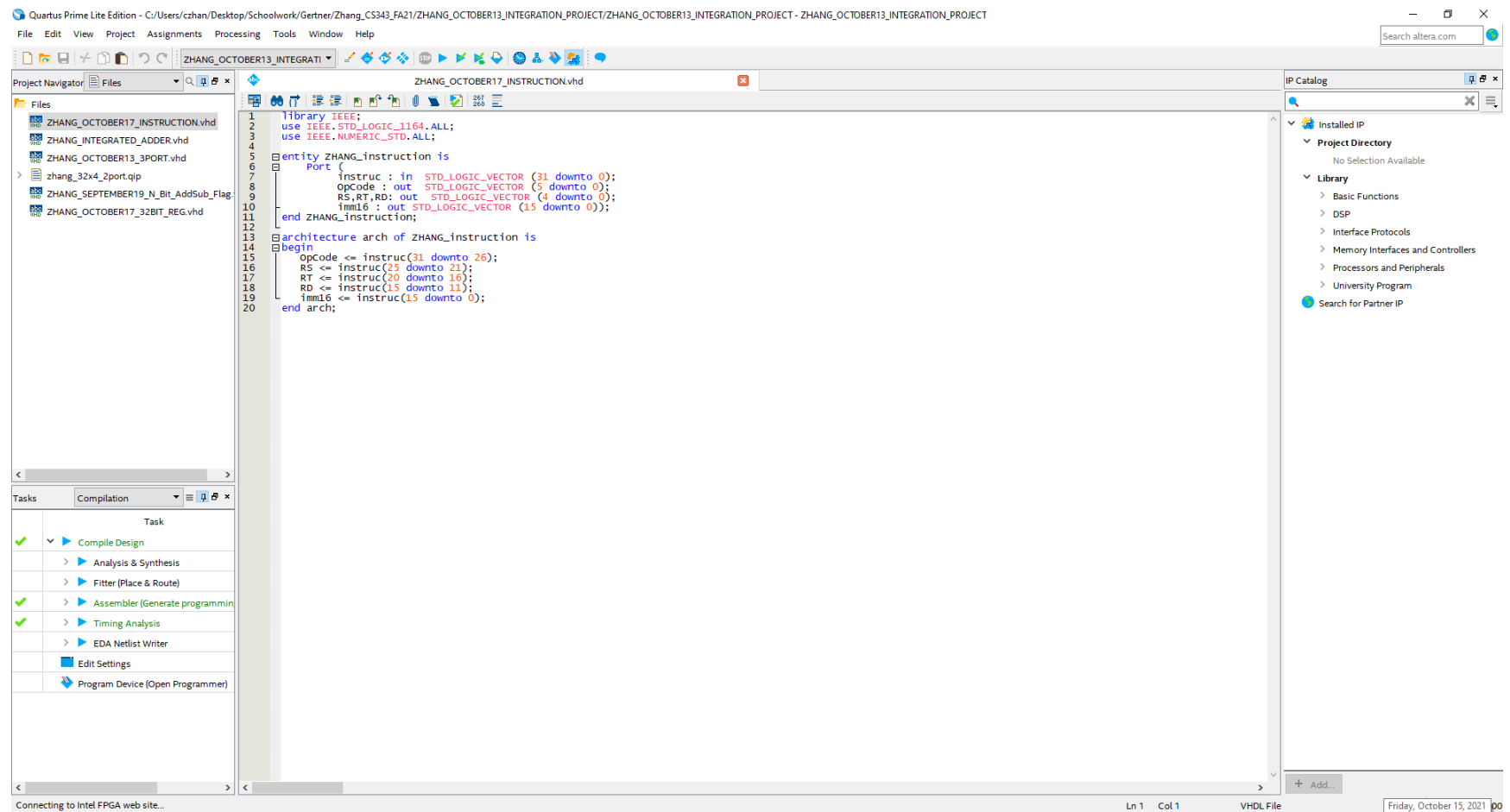


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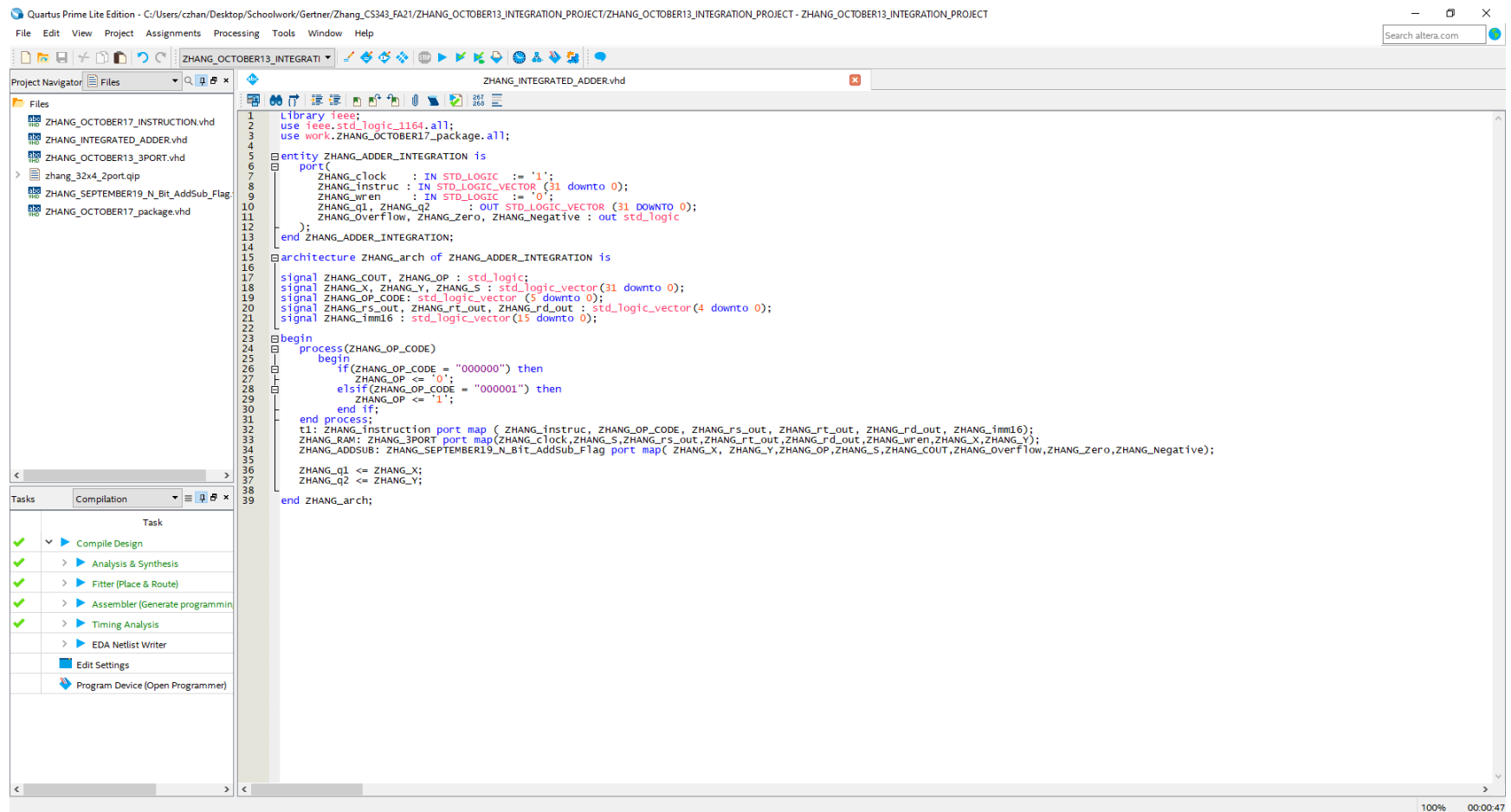
C:\Users\czhan\Desktop\Schoolwork\Gertner\Zhang_CS343_FA21\ZHANG_OCTOBER13_INTEGRATION_PROJECT\ram32x32.mif - Notepad++
File Edit Search View Encoding Language Settings Tools Macro Run Plugins Window ?
ram32x32.mif [x]
1 DEPTH = 32;           -- The size of memory in words
2 WIDTH = 32;          -- The size of data in bits
3 ADDRESS_RADIX = HEX; -- The radix for address values
4 DATA_RADIX = HEX;   -- The radix for data values
5 CONTENT              -- start of (address : data pairs)
6 BEGIN
7
8 0: 7FFFFFFF;
9 1: 80000000;
10 2: 00000001;
11 3: 00000000;
12 4: 00000000;
13 5: 00000000;
14 6: 00000000;
15 7: 00000000;
16 8: 00000000;
17 9: 00000000;
18 A: 00000000;
19 B: 00000000;
20 C: 00000000;
21 D: 00000000;
22 E: 00000000;
23 F: 00000000;
24 10: 00000000;
25 11: 00000000;
26 12: 00000000;
27 13: 00000000;
28 14: 00000000;
29 15: 00000000;
30 16: 00000000;
31 17: 00000000;
32 18: 00000000;
33 19: 00000000;
34 1A: 00000000;
35 1B: 00000000;
36 1C: 00000000;
37 1D: 00000000;
38 1E: 00000000;
39 1F: 00000000;
40
41 END;
42
43
Normal text file | length : 795 | lines : 43 | Ln : 43 | Col : 2 | Pos : 796 | Windows (CR LF) | UTF-8 | INS

```

Above is the MIF file that will be used for reading and writing to. Notice that the 1<sup>st</sup> address points towards the Largest Positive value, the 2<sup>nd</sup> address points to the Largest Negative value and the 3<sup>rd</sup> address points to 1. The rest of the address point to 0 as a placeholder where we will later be writing new values into.



In the screenshot above showcases how I process the 32-bit MIPS like instruction



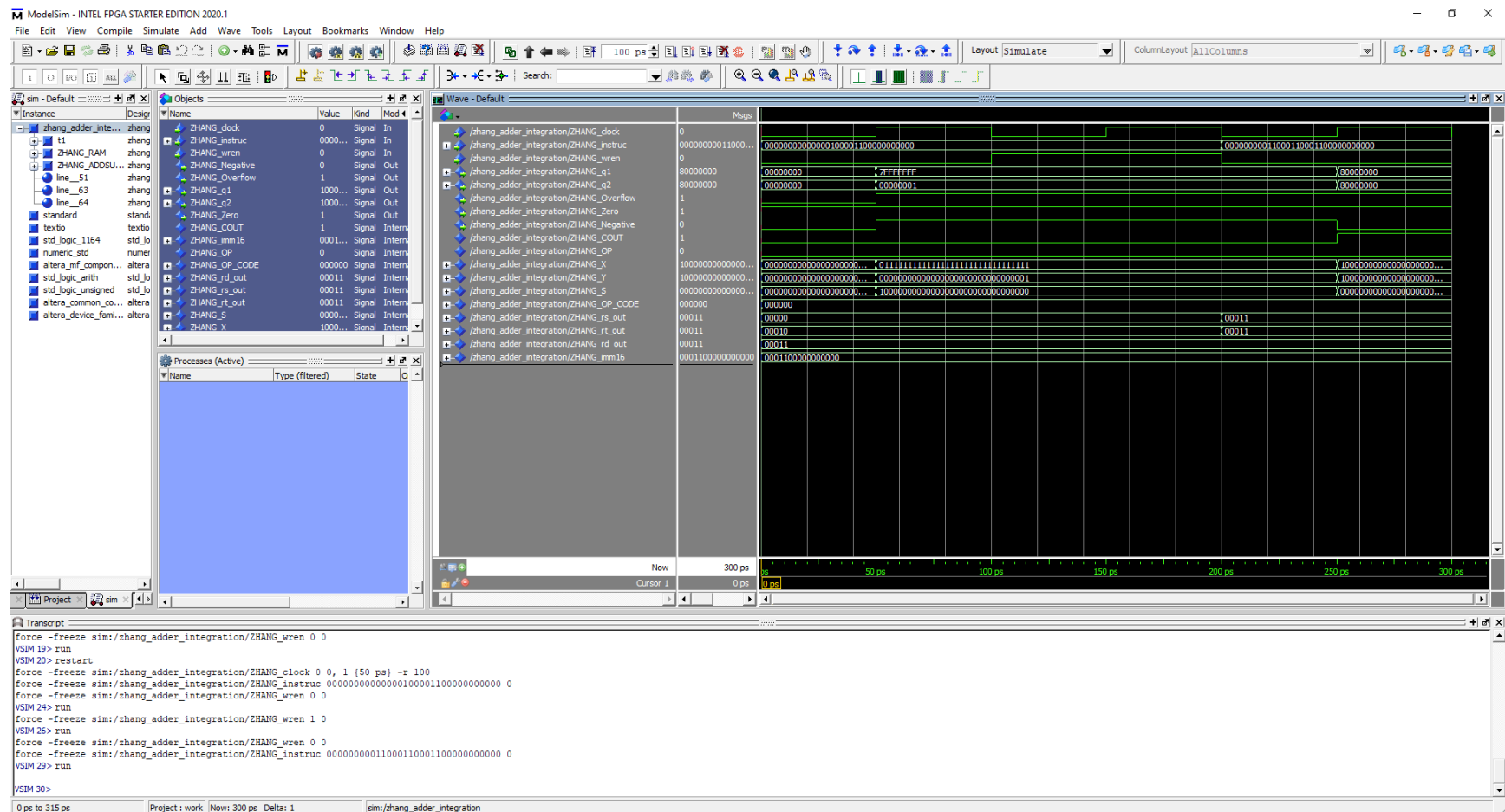
Above showcases the usage of the Instruction File, the 3-port ram and the 32-Bit Adder/Subtractor Unit

## **Simulations**

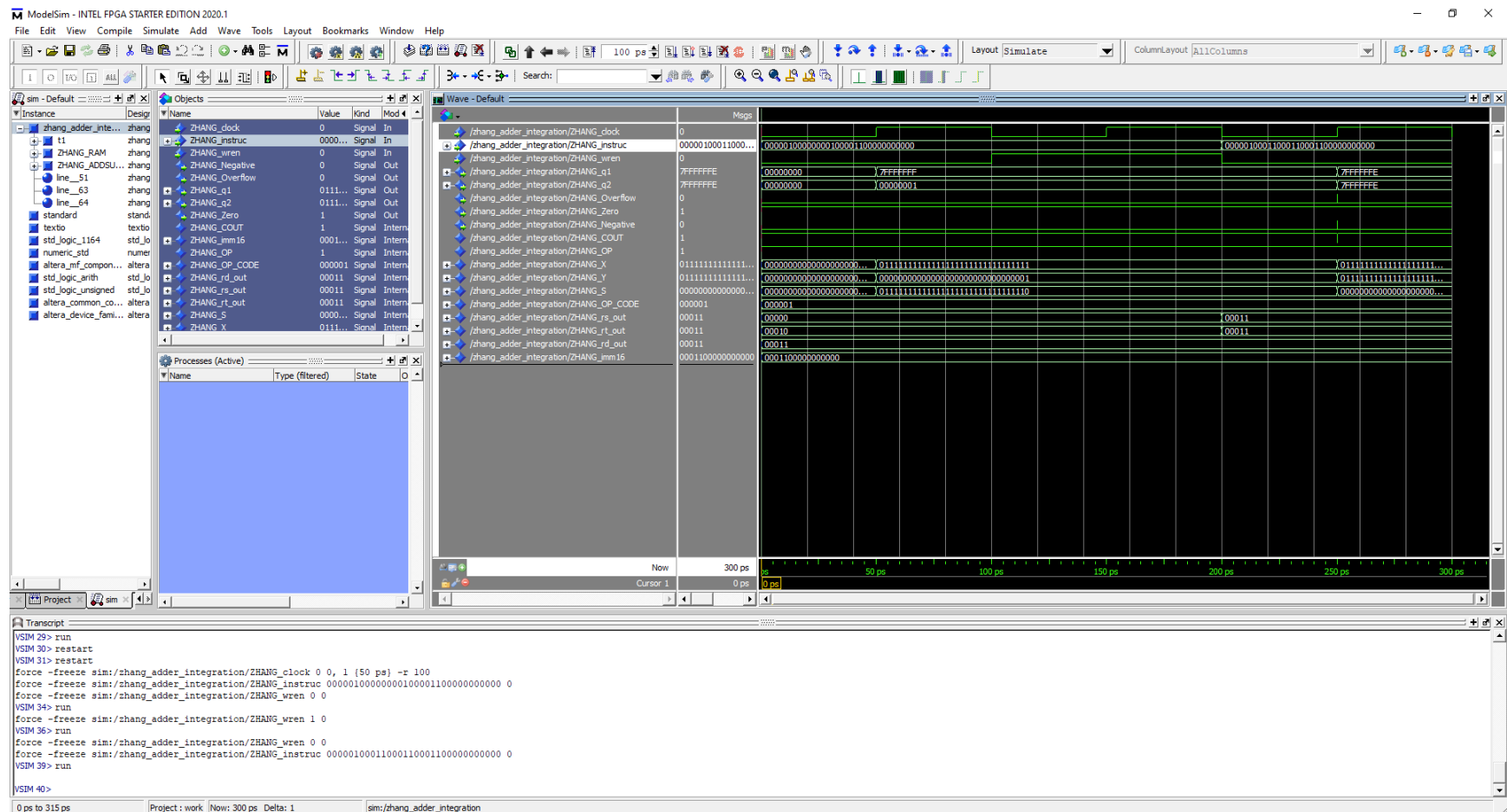
Simulations will be done to verify correctness of the 3-Port RAM Adder/Sub Unit and performed on Modelsim with waveform screenshots and explanations to further verify correctness.

What will be Tested is the following

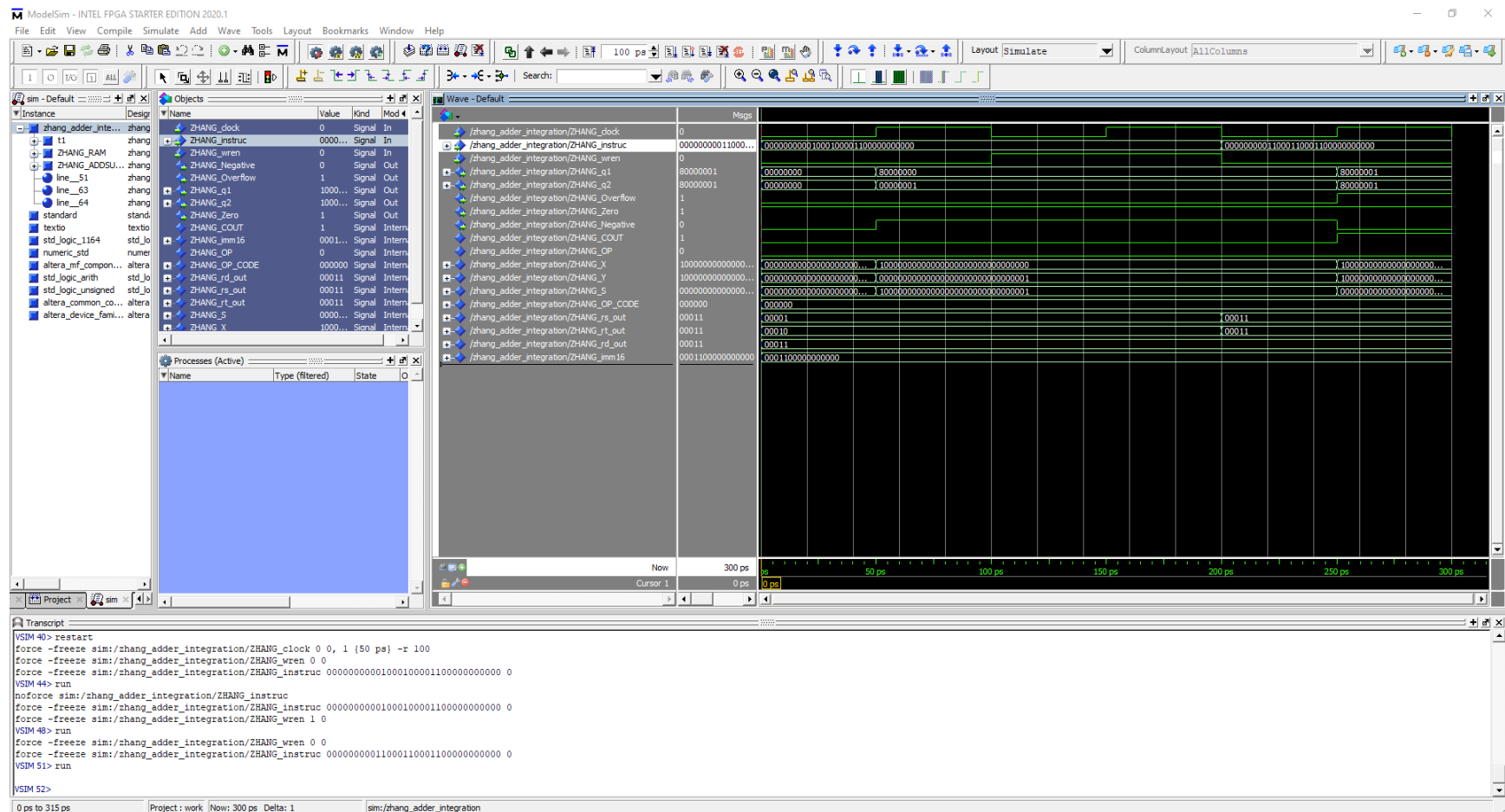
- 1. Most Positive 32-Bit Integer + 1**
- 2. Most Positive 32-Bit Integer – 1**
- 3. Most Negative 32-Bit Integer + 1**
- 4. Most Negative 32-Bit Integer – 1**
- 5. Most Positive 32-Bit Integer – Most Negative 32-Bit Integer**
- 6. Most Positive 32-Bit Integer + Most Positive 32-Bit Integer**
- 7. Most positive 32-Bit Integer – Most Positive 32-Bit Integer**



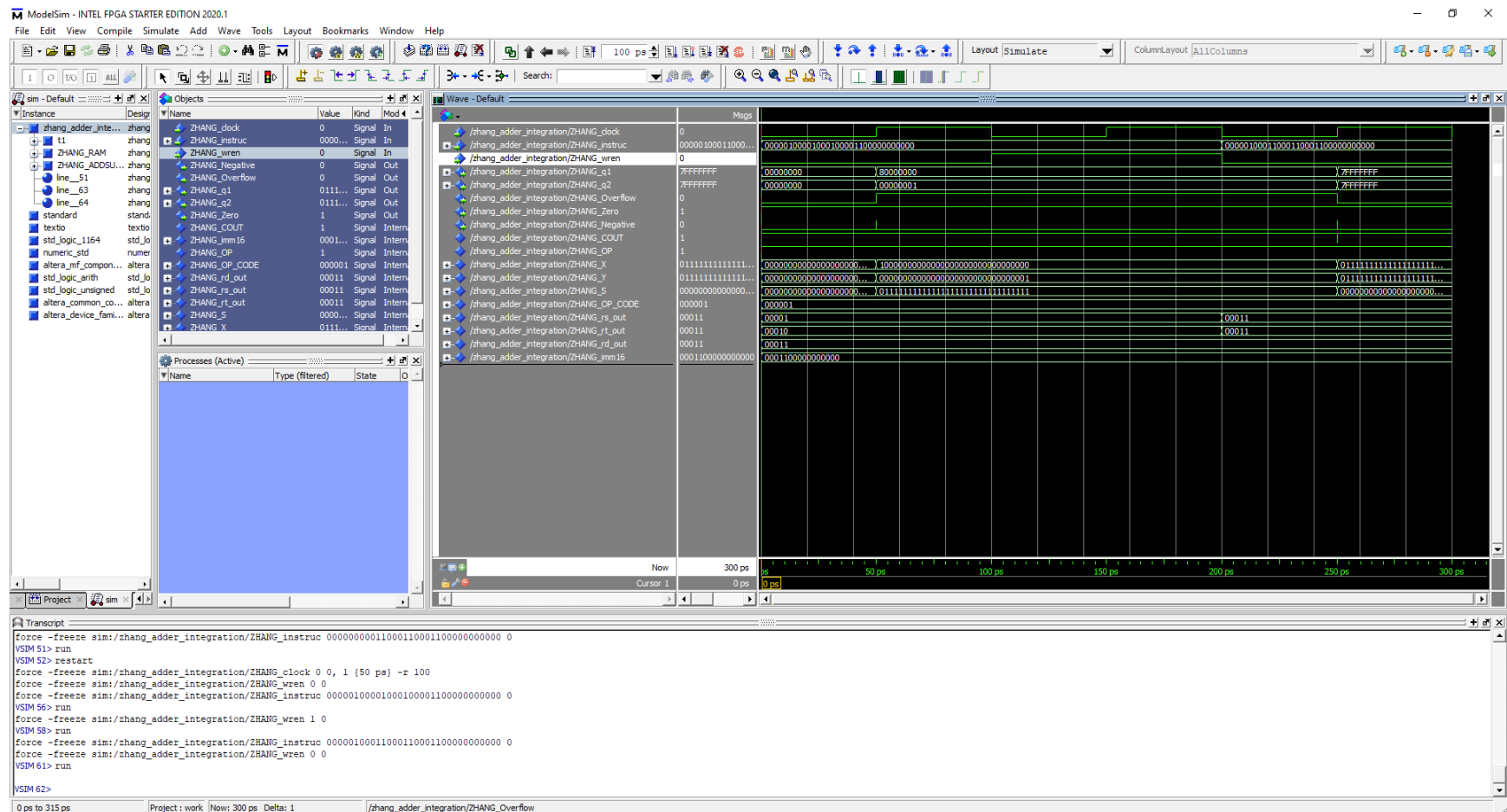
What is performed is the **Most Positive 32-Bit Integer + 1** where a 32-bit Instruction is read where once the instruction is broken down they will be inputted into the adder/subtractor where the 3-port ram calls the address from in the MIF File so that the Mathematical process can be performed then stored. Instruction bit is 000000 00000 00010 00011 000000000000, OP code, RS, RT, RD, Function respectively. Notice that the 1<sup>st</sup> Address and the 3<sup>rd</sup> Address is being called from the MIF, computed, then written into the 4<sup>th</sup> Address. Furthermore, Overflow flag and Negative flag has been triggered.



What is performed is the **Most Positive 32-Bit Integer - 1** where a 32-bit Instruction is read where once the instruction is broken down they will be inputted into the adder/subtractor where the 3-port ram calls the address from in the MIF File so that the Mathematical process can be performed then stored. Instruction bit is 000001 00000 00010 00011 00000000000, OP code, RS, RT, RD, Function respectively. Notice that the 1<sup>st</sup> Address and the 3<sup>rd</sup> Address is being called from the MIF, computed, then written into the 4<sup>th</sup> Address. Furthermore, zero flag has been triggered

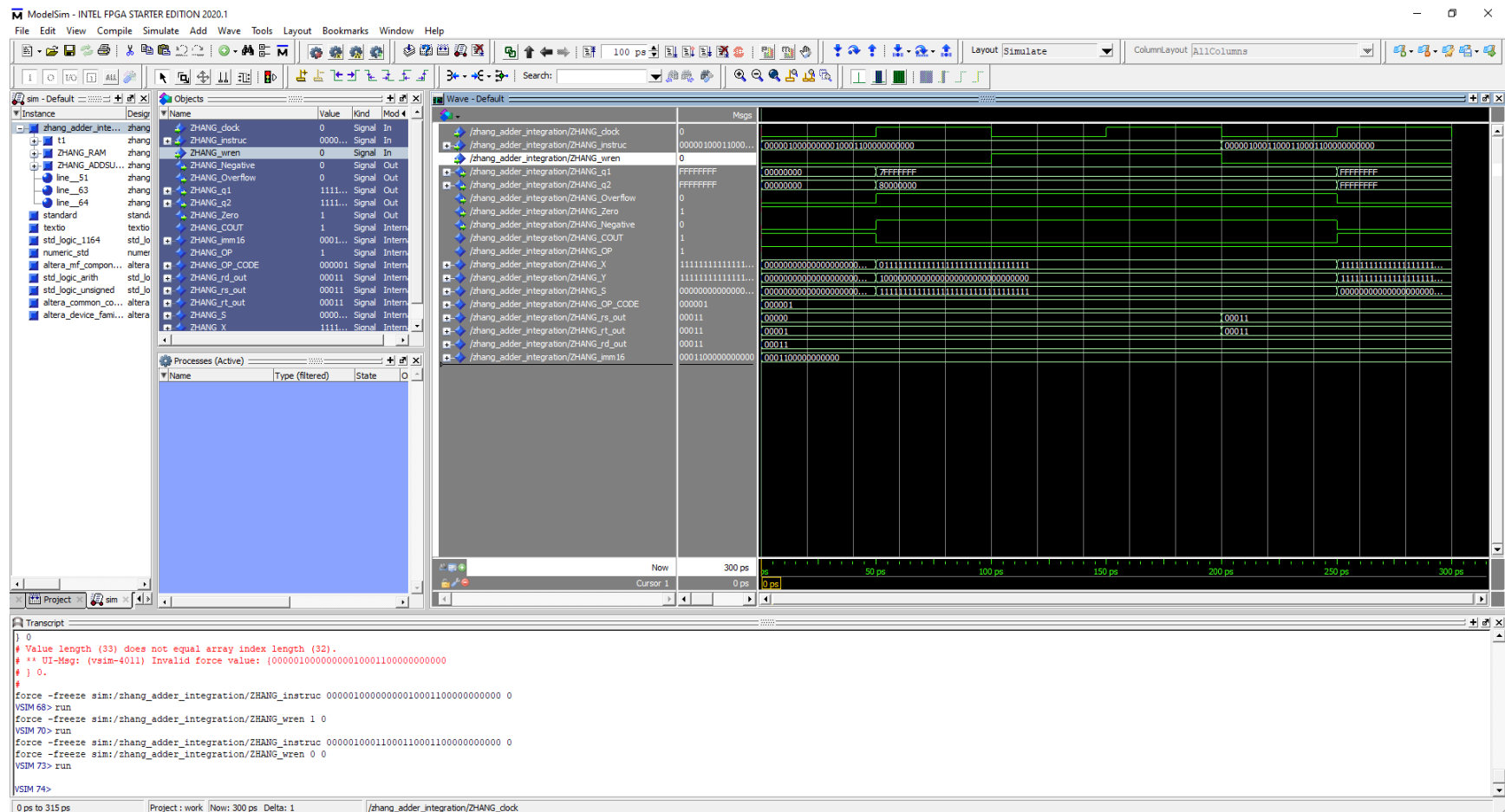


What is performed is the **Most Negative 32-Bit Integer + 1** where a 32-bit Instruction is read where once the instruction is broken down they will be inputted into the adder/subtractor where the 3-port ram calls the address from in the MIF File so that the Mathematical process can be performed then stored. Instruction bit is 000000 00001 00010 00011 000000000000, OP code, RS, RT, RD, Function respectively. Notice that the 2<sup>nd</sup> Address and the 3<sup>rd</sup> Address is being called from the MIF, computed, then written into the 4<sup>th</sup> Address. Furthermore, notice the Overflow Flag.

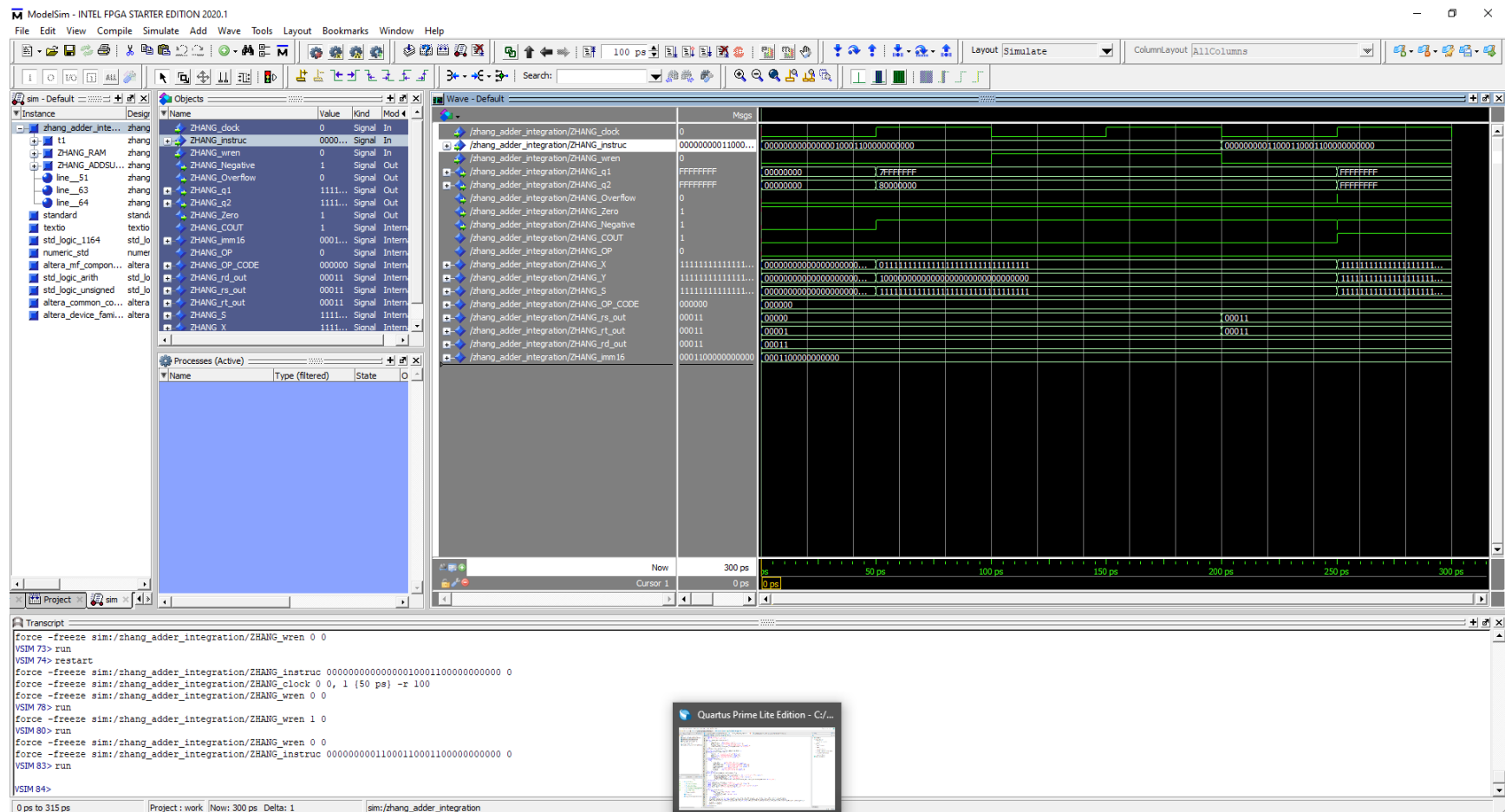


What is performed is the **Most Negative 32-Bit Integer - 1** where a 32-bit Instruction is read where once the instruction is broken down they will be inputted into the adder/subtractor where the 3-port ram calls the address from in the MIF File so that the Mathematical process can be performed then stored. Instruction bit is 000001 00001 00010 00011 000000000000, OP code, RS, RT, RD, Function respectively. Notice that the 2<sup>nd</sup> Address and the 3<sup>rd</sup> Address is being called from the MIF, computed, then written into the 4<sup>th</sup> Address.

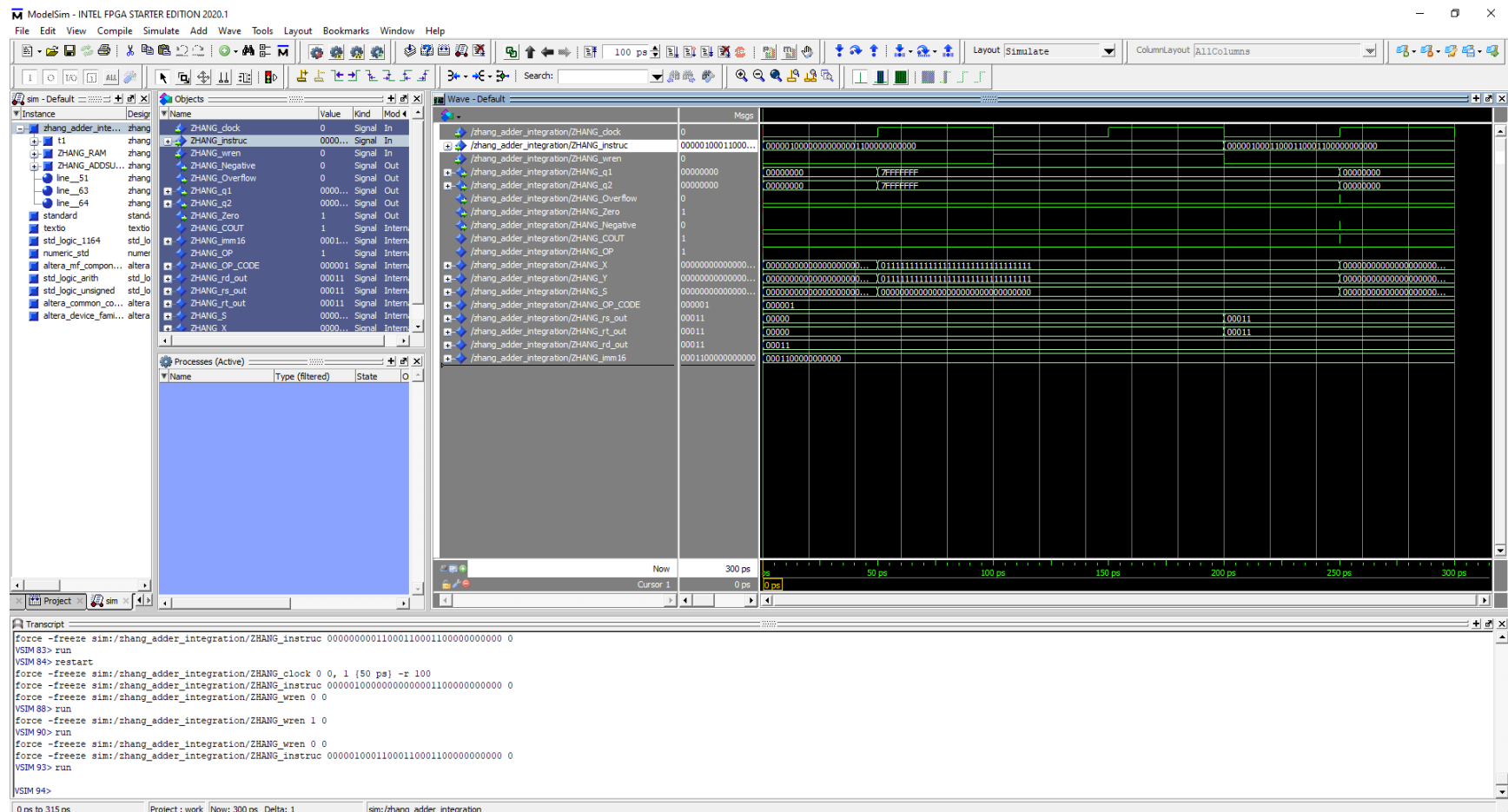




What is performed is the **Most Positive 32-Bit Integer - Most Negative 32-Bit Integer** where a 32-bit Instruction is read where once the instruction is broken down they will be inputted into the adder/subtractor where the 3-port ram calls the address from in the MIF File so that the Mathematical process can be performed then stored. Instruction bit is 000001 00000 00001 00011 00000000000, OP code, RS, RT, RD, Function respectively. Notice that the 1<sup>st</sup> Address and the 2<sup>nd</sup> Address is being called from the MIF, computed, then written into the 4<sup>th</sup> Address.



What is performed is the **Most Positive 32-Bit Integer + Most Negative 32-Bit Integer** where a 32-bit Instruction is read where once the instruction is broken down they will be inputted into the adder/subtractor where the 3-port ram calls the address from in the MIF File so that the Mathematical process can be performed then stored. Instruction bit is 000000 00000 00001 00011 00000000000, OP code, RS, RT, RD, Function respectively. Notice the 1<sup>st</sup> Address and the 2<sup>nd</sup> Address is being called from the MIF, computed, then written into the 4<sup>th</sup> address. Notice the negative flag being triggered.



What is performed is the **Most Positive 32-Bit Integer - Most Positive 32-Bit Integer** where a 32-bit Instruction is read where once the instruction is broken down they will be inputted into the adder/subtractor where the 3-port ram calls the address from in the MIF File so that the Mathematical process can be performed then stored. Instruction bit is 000001 00000 00000 00011 00000000000, OP code, RS, RT, RD, Function respectively. Notice the Zero flag being triggered.

## **Conclusion**

By doing this laboratory assignment, I was able to get familiar with the usage of the MIF file and how it works. I also learned more about how Register block works as well as how things are read and written. By the end of this lab, I have gained much knowledge on the importance of the usage of RAM as well as how to integrate units into it.