

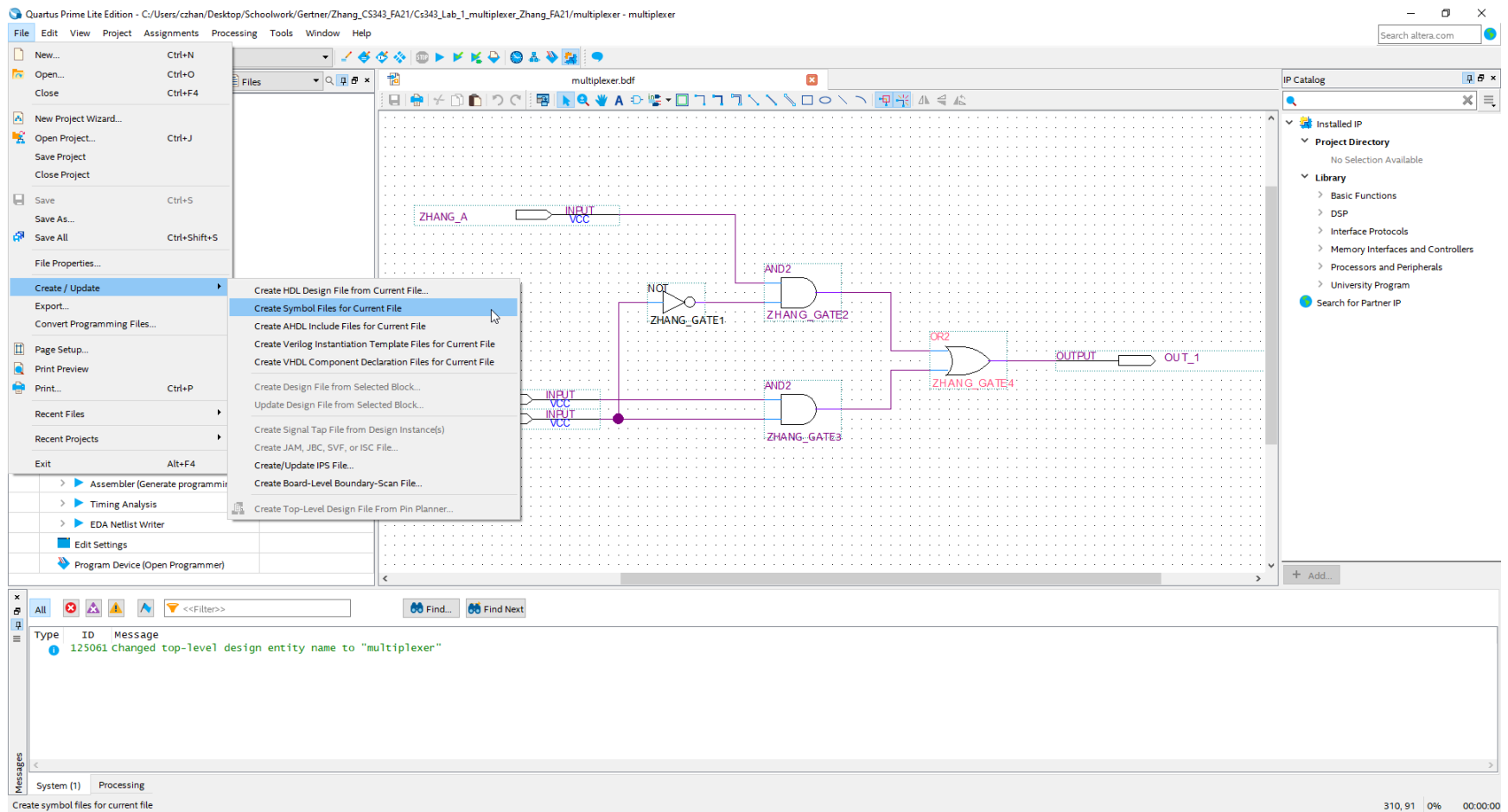
Lab Report : VHDL with LPM

Chue Zhang

Csc343 Fall 2021

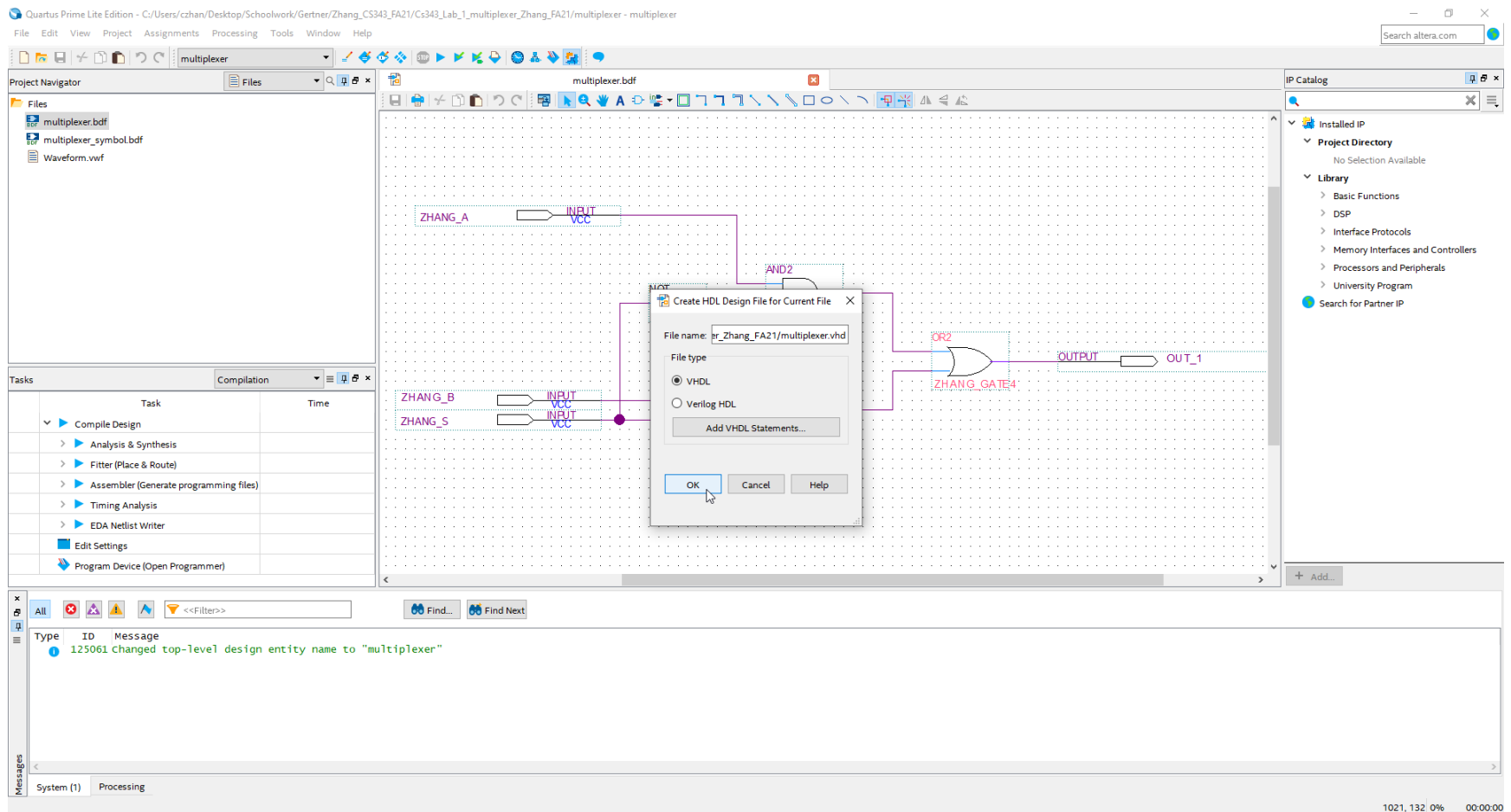
Professor Gertner

Task 1, Chue Zhang



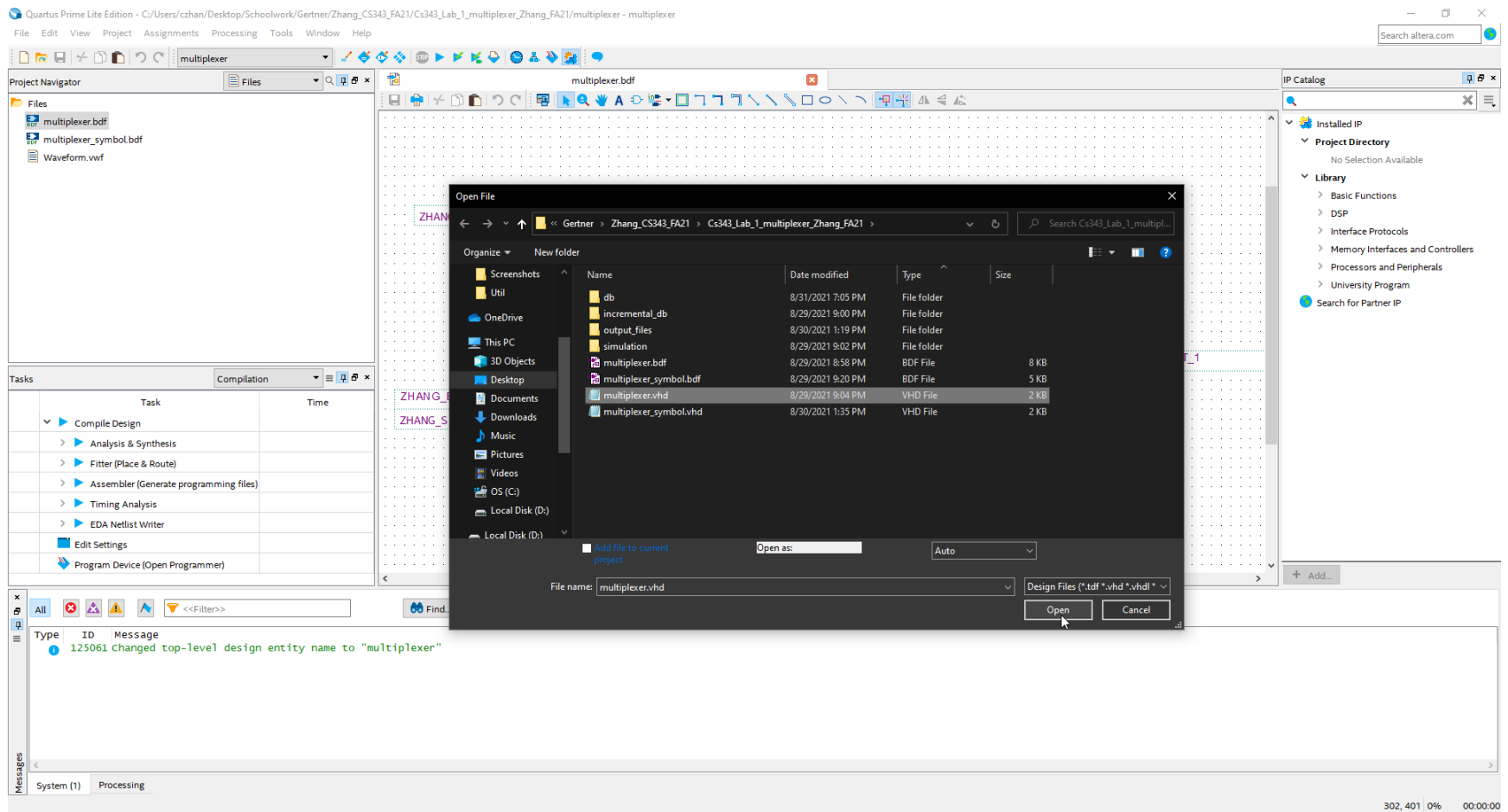
With the 2:1 Mux previously created, I go to the file → create HDL design File for Current File and a popup should show up

Task 1, Chue Zhang



Make sure that the file type is in VHDL not in Verilog and press OK

Task 1, Chue Zhang



I now add the VHDL file of the design into the files

Task 1, Chue Zhang

Quartus Prime Lite Edition - C:/Users/czhan/Desktop/Schoolwork/Gertner/Zhang_CS343_FA21/Cs343_Lab_1_multiplexer_Zhang_FA21/multiplexer - multiplexer

File Edit View Project Assignments Processing Tools Window Help

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Project Navigator

Files

- multiplexer.bdf
- multiplexer_symbol.bdf
- Waveform.vwf
- multiplexer.vhd

Tasks

Task	Time
Compile Design	
Analysis & Synthesis	
Fitter (Place & Route)	
Assembler (Generate programming files)	
Timing Analysis	
EDA Netlist Writer	
Edit Settings	
Program Device (Open Programmer)	

multiplexer.bdf

multiplexer.vhd

```
11 -- the sole purpose of programming logic devices manufactured by
12 -- Intel and sold by Intel or its authorized distributors. Please
13 -- refer to the applicable agreement for further details, at
14 -- https://fpgasoftware.intel.com/eula.
15
16 -- PROGRAM "Quartus Prime"
17 -- VERSION "Version 20.1.1 Build 720_11/11/2020 SJ Lite Edition"
18 -- CREATED "Sun Aug 29 21:04:23 2021"
19
20 LIBRARY ieee;
21 USE ieee.std_logic_1164.all;
22
23 LIBRARY work;
24
25 ENTITY multiplexer IS
26     PORT
27     (
28         ZHANG_A : IN STD_LOGIC;
29         ZHANG_B : IN STD_LOGIC;
30         ZHANG_S : IN STD_LOGIC;
31         OUT_1 : OUT STD_LOGIC
32     );
33 END multiplexer;
34
35 ARCHITECTURE bdf_type OF multiplexer IS
36
37     SIGNAL SYNTHESIZED_WIRE_0 : STD_LOGIC;
38     SIGNAL SYNTHESIZED_WIRE_1 : STD_LOGIC;
39     SIGNAL SYNTHESIZED_WIRE_2 : STD_LOGIC;
40
41
42 BEGIN
43
44     SYNTHESIZED_WIRE_0 <= NOT(ZHANG_S);
45
46
47
48
49     SYNTHESIZED_WIRE_2 <= ZHANG_A AND SYNTHESIZED_WIRE_0;
50
51
52     SYNTHESIZED_WIRE_1 <= ZHANG_B AND ZHANG_S;
53
54
55     OUT_1 <= SYNTHESIZED_WIRE_1 OR SYNTHESIZED_WIRE_2;
56
57
```

IP Catalog

- Installed IP
 - Project Directory
 - No Selection Available
 - Library
 - Basic Functions
 - DSP
 - Interface Protocols
 - Memory Interfaces and Controllers
 - Processors and Peripherals
 - University Program
 - Search for Partner IP

Find... Find Next

Type ID Message

- 125061 changed top-level design entity name to "multiplexer"

System (1) Processing

Ln 1 Col 1 VHDL File 0% 00:00:00

I now set the VHDL file to top level while showcasing some of the code

Task 1, Chue Zhang

Quartus Prime Lite Edition - C:/Users/czhan/Desktop/Schoolwork/Gertner/Zhang_CS343_FA21/Cs343_Lab_1_mux/multiplexer_Zhang_FA21/multiplexer - multiplexer

File Edit View Project Assignments Processing Tools Window Help

Search altera.com

Project Navigator

Files

- multiplexer.bdf
- multiplexer_symbol.bdf
- Waveform.vwf
- multiplexer.vhd

Table of Contents

- Flow Summary
- Flow Settings
- Flow Non-Default Global Settings
- Flow Elapsed Time
- Flow OS Summary
- Flow Log
- Analysis & Synthesis
 - Flow Messages
 - Flow Suppressed Messages

Flow Summary

<<Filter>>

Flow Status	Flow Failed - Tue Aug 31 19:17:48 2021
Quartus Prime Version	20.1.1 Build 720 11/11/2020 SJ Lite Edition
Revision Name	multiplexer
Top-level Entity Name	multiplexer
Family	Cyclone V
Device	5CGXFC7C7F23C8
Timing Models	Final
Logic utilization (in ALMs)	N/A until Partition Merge
Total registers	N/A until Partition Merge
Total pins	N/A until Partition Merge
Total virtual pins	N/A until Partition Merge
Total block memory bits	N/A until Partition Merge
Total PLLs	N/A until Partition Merge
Total DLLs	N/A until Partition Merge

Tasks

Compilation

Task	Time
Compile Design	00:00:08
Analysis & Synthesis	00:00:08
Fitter (Place & Route)	
Assembler (Generate programming files)	
Timing Analysis	
EDA Netlist Writer	
Edit Settings	
Program Device (Open Programmer)	

Messages

All

<<Filter>>

Find... Find Next

Type	ID	Message
Warning	18236	Number of processors has not been specified which may cause overloading on shared machines. set the global assignment NUM_PARALLEL_PROCESSORS in your QSF to an appropriate value for best performance.
Information	20030	Parallel compilation is enabled and will use 6 of the 6 processors detected
Information	12021	Found 1 design units, including 1 entities, in source file multiplexer.bdf
Information	12021	Found 1 design units, including 1 entities, in source file multiplexer_symbol.bdf
Error	12049	Can't compile duplicate declarations of entity "multiplexer" into library "work"
Information	12021	Found 2 design units, including 1 entities, in source file multiplexer.vhd
Error		Quartus Prime Analysis & Synthesis was unsuccessful. 3 errors, 1 warning
Error	293001	Quartus Prime Full Compilation was unsuccessful. 5 errors, 1 warning

System (1) Processing (11)

2% 00:00:08

I try to compile but come to an error

Task 1, Chue Zhang

Quartus Prime Lite Edition - C:/Users/czhan/Desktop/Schoolwork/Gertner/Zhang_CS343_FA21/Cs343_Lab_1/multiplexer_Zhang_FA21/multiplexer - multiplexer

File Edit View Project Assignments Processing Tools Window Help

Project Navigator

- Files
 - multiplexer.bdf
 - multiplexer_symbol.bdf
 - Waveform.vwf
 - multiplexer.vhd

Tasks

Task	Time
Compile Design	00:00:08
Analysis & Synthesis	00:00:08
Fitter (Place & Route)	
Assembler (Generate programming files)	
Timing Analysis	
EDA Netlist Writer	
Edit Settings	
Program Device (Open Programmer)	

multiplexer.bdf

```
-- the sole purpose of programming logic devices manufactured by
-- Intel and sold by Intel or its authorized distributors. Please
-- refer to the applicable agreement for further details, at
-- https://fpgasoftware.intel.com/eula.
-- PROGRAM "Quartus Prime"
-- VERSION "Version 20.1.1 Build 720 11/11/2020 S3 Lite Edition"
-- CREATED "Sun Aug 29 21:04:23 2021"

LIBRARY ieee;
USE ieee.std_logic_1164.all;

LIBRARY work;

ENTITY multiplexer IS
PORT
(
    ZHANG_A : IN STD_LOGIC;
    ZHANG_B : IN STD_LOGIC;
    ZHANG_S : IN STD_LOGIC;
    OUT_1 : OUT STD_LOGIC
);
END multiplexer;

ARCHITECTURE bdf_type OF multiplexer IS

SIGNAL SYNTHESIZED_WIRE_0 : STD_LOGIC;
SIGNAL SYNTHESIZED_WIRE_1 : STD_LOGIC;
SIGNAL SYNTHESIZED_WIRE_2 : STD_LOGIC;

BEGIN

    SYNTHESIZED_WIRE_0 <= NOT(ZHANG_S);

    SYNTHESIZED_WIRE_2 <= ZHANG_A AND SYNTHESIZED_WIRE_0;
```

multiplexer.vhd

Find what: multiplexer Replace with: multiplexer_VHDL Look in: Current File Search: Down Find Next Replace Replace All Mark All

Messages

Type	ID	Message
Warning	18236	Number of processors has not been specified which may cause overloading on shared machines. Set the global assignment NUM_PARALLEL_PROCESSORS in your QSF to an appropriate value for best performance.
Information	20030	Parallel compilation is enabled and will use 6 of the 6 processors detected
Information	12021	Found 1 design units, including 1 entities, in source file multiplexer.bdf
Information	12021	Found 1 design units, including 1 entities, in source file multiplexer_symbol.bdf
Error	12049	Can't compile duplicate declarations of entity "multiplexer" into library "work"
Information	12021	Found 2 design units, including 1 entities, in source file multiplexer.vhd
Error		quartus Prime Analysis & Synthesis was unsuccessful. 3 errors, 1 warning
Error	293001	quartus Prime Full Compilation was unsuccessful. 5 errors, 1 warning

System (1) Processing (11)

Ln 25 Col 19 VHDL File 2% 00:00:08

I change the highlighted multiplexer text to multiplexer_VHDL and save the VHDL file under the new corrected name

Task 1, Chue Zhang

Quartus Prime Lite Edition - C:/Users/czhan/Desktop/Schoolwork/Gertner/Zhang_CS343_FA21/Cs343_Lab_1_multiplexer_Zhang_FA21/multiplexer - multiplexer

File Edit View Project Assignments Processing Tools Window Help

Project Navigator

- Files
 - multiplexer.bdf
 - multiplexer_symbol.bdf
 - Waveform.vwf
 - multiplexer_VHDL.vhd
- Tasks
 - Task
 - Time
 - Compile Design
 - Analysis & Synthesis (00:00:08)
 - Fitter (Place & Route)
 - Assembler (Generate programming files)
 - Timing Analysis
 - EDA Netlist Writer
 - Edit Settings
 - Program Device (Open Programmer)

multplexer.bdf

```
1 -- Copyright (C) 2020 Intel Corporation. All rights reserved.
2 -- Your use of Intel Corporation's design tools, logic functions
3 -- and other software and tools, and any partner logic
4 -- functions, and any output files from any of the foregoing
5 -- (including device programming or simulation files), and any
6 -- associated documentation or information are expressly subject
7 -- to the terms and conditions of the Intel Program License
8 -- Subscription Agreement, the Intel Quartus Prime License Agreement,
9 -- the Intel FPGA IP License Agreement, or other applicable license
10 -- agreement, including, without limitation, that your use is for
11 -- the sole purpose of programming logic devices manufactured by
12 -- Intel and sold by Intel or its authorized distributors. Please
13 -- refer to the applicable agreement for further details, at
14 -- https://fpgasoftware.intel.com/eula.
15
16 -- PROGRAM "Quartus Prime"
17 -- VERSION "Version 20.1.1 Build 720_11/11/2020 SJ Lite Edition"
18 -- CREATED "Sun Aug 29 21:04:23 2021"
19
20 LIBRARY ieee;
21 USE ieee.std_logic_1164.all;
22
23 LIBRARY work;
24
25 ENTITY multiplexer_VHDL IS
26 PORT
27 (
28   ZHANG_A : IN STD_LOGIC;
29   ZHANG_B : IN STD_LOGIC;
30   ZHANG_S : IN STD_LOGIC;
31   OUT_1 : OUT STD_LOGIC
32 );
33 END multiplexer_VHDL;
34
35 ARCHITECTURE bdf_type OF multiplexer_VHDL IS
36
37   SIGNAL SYNTHESIZED_WIRE_0 : STD_LOGIC;
38   SIGNAL SYNTHESIZED_WIRE_1 : STD_LOGIC;
39   SIGNAL SYNTHESIZED_WIRE_2 : STD_LOGIC;
40
41 BEGIN
42
43   SYNTHESIZED_WIRE_0 <= NOT(ZHANG_S);
44
45
46
```

IP Catalog

- Installed IP
 - Project Directory
 - No Selection Available
 - Library
 - Basic Functions
 - DSP
 - Interface Protocols
 - Memory Interfaces and Controllers
 - Processors and Peripherals
 - University Program
 - Search for Partner IP

Messages

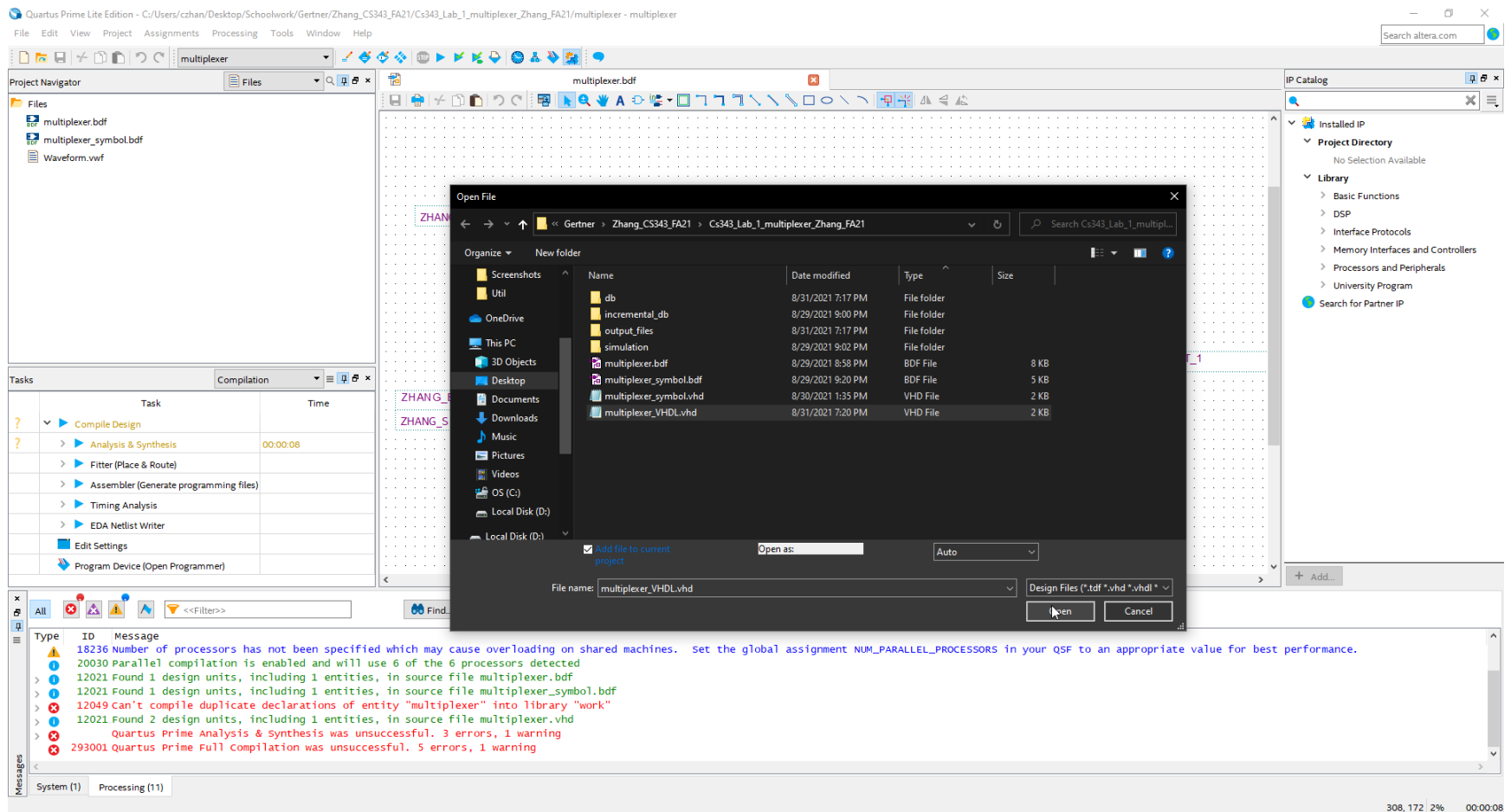
Type	ID	Message
Warning	18236	Number of processors has not been specified which may cause overloading on shared machines. set the global assignment NUM_PARALLEL_PROCESSORS in your QSF to an appropriate value for best performance.
Information	20030	Parallel compilation is enabled and will use 6 of the 6 processors detected
Information	12021	Found 1 design units, including 1 entities, in source file multiplexer.bdf
Information	12021	Found 1 design units, including 1 entities, in source file multiplexer_symbol.bdf
Error	12049	Can't compile duplicate declarations of entity "multiplexer" into library "work"
Information	12021	Found 2 design units, including 1 entities, in source file multiplexer.vhd
Warning		Quartus Prime Analysis & Synthesis was unsuccessful. 3 errors, 1 warning
Error	293001	Quartus Prime Full Compilation was unsuccessful. 5 errors, 1 warning

System (1) Processing (11)

Ln 1 Col 1 VHDL File 2% 00:00:08

Here is the corrected code that I will then save with a different name according to what I renamed the code to

Task 1, Chue Zhang



I re-add the vhd file

Task 1, Chue Zhang

Quartus Prime Lite Edition - C:/Users/czhan/Desktop/Schoolwork/Gertner/Zhang_CS343_FA21/Cs343_Lab_1_mux/multiplexer_Zhang_FA21/multiplexer - multiplexer

File Edit View Project Assignments Processing Tools Window Help

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Project Navigator multiplexer multiplexer.bdf multiplexer_VHDL.vhd Compilation Report - multiplexer IP Catalog

Files

- multiplexer.bdf
- multiplexer_symbol.bdf
- Waveform.vwf
- multiplexer_VHDL.vhd

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- Flow OS Summary
- Flow Log
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- Assembler
- Timing Analyzer

Flow Summary

<<Filter>>

Flow Status	Successful - Tue Aug 31 19:24:35 2021
Quartus Prime Version	20.1.1 Build 720 11/11/2020 SJ Lite Edition
Revision Name	multiplexer
Top-level Entity Name	multiplexer_VHDL
Family	Cyclone V
Device	5CGXFC7C7F23C8
Timing Models	Final
Logic utilization (in ALMs)	1 / 56,480 (< 1 %)
Total registers	0
Total pins	4 / 268 (1 %)
Total virtual pins	0
Total block memory bits	0 / 7,024,640 (0 %)
Total DSP Blocks	0 / 156 (0 %)
Total HSSI RX PCSs	0 / 6 (0 %)
Total HSSI PMA RX Deserializers	0 / 6 (0 %)
Total HSSI TX PCSs	0 / 6 (0 %)
Total HSSI PMA TX Serializers	0 / 6 (0 %)
Total PLLs	0 / 13 (0 %)
Total DLLs	0 / 4 (0 %)

Tasks

Compilation

Task	Time
Compile Design	00:00:48
Analysis & Synthesis	00:00:08
Fitter (Place & Route)	00:00:26
Assembler (Generate programming files)	00:00:09
Timing Analysis	00:00:05
EDA Netlist Writer	
Edit Settings	
Program Device (Open Programmer)	

Messages

All <<Filter>> Find... Find Next

Type	ID	Message
Warning	332140	No Hold paths to report
Warning	332140	No Recovery paths to report
Warning	332140	No Removal paths to report
Warning	332140	No Minimum Pulse Width paths to report
Warning	332102	Design is not fully constrained for setup requirements
Warning	332102	Design is not fully constrained for hold requirements
Information	293000	Quartus Prime Timing Analyzer was successful. 0 errors, 6 warnings
Information	293000	Quartus Prime Full Compilation was successful. 0 errors, 19 warnings

System (2) Processing (129)

100% 00:00:48

I compile with success

Task 2, Chue Zhang

The screenshot displays the Quartus Prime Lite Edition interface. The 'Utility Windows' menu is open, and the 'IP Catalog' option is selected. The 'IP Catalog' window is visible on the right side of the interface, showing the 'Project Directory' and 'Library' sections. The 'Library' section is expanded, showing various IP blocks such as 'Basic Functions', 'DSP', 'Interface Protocols', 'Memory Interfaces and Controllers', 'Processors and Peripherals', and 'University Program'. The 'Search for Partner IP' button is also visible.

The main window shows the 'Flow Summary' for the 'multiplexer_VHDL.vhd' project. The flow status is 'Successful - Tue Aug 31 19:24:35 2021'. The flow summary table is as follows:

Flow Status	Successful - Tue Aug 31 19:24:35 2021
Quartus Prime Version	20.1.1 Build 720 11/11/2020 SJ Lite Edition
Revision Name	multiplexer
Top-level Entity Name	multiplexer_VHDL
Family	Cyclone V
Device	5CGXFC7C7F23C8
Timing Models	Final
Logic utilization (in ALMs)	1 / 56,480 (< 1 %)
Total registers	0
Total pins	4 / 268 (1 %)
Total virtual pins	0
Total block memory bits	0 / 7,024,640 (0 %)
Total DSP Blocks	0 / 156 (0 %)
Total HSSI RX PCSs	0 / 6 (0 %)
Total HSSI PMA RX Deserializers	0 / 6 (0 %)
Total HSSI TX PCSs	0 / 6 (0 %)
Total HSSI PMA TX Serializers	0 / 6 (0 %)
Total PLLs	0 / 13 (0 %)
Total DLLs	0 / 4 (0 %)

The 'Tasks' window shows the compilation progress:

Task	Time
Compile Design	00:00:48
Analysis & Synthesis	00:00:08
Fitter (Place & Route)	00:00:26
Assembler (Generate programming files)	00:00:09
Timing Analysis	00:00:05
EDA Netlist Writer	
Edit Settings	
Program Device (Open Programmer)	

The 'Messages' window shows the following messages:

```
332140 No Hold paths to report
332140 No Recovery paths to report
332140 No Removal paths to report
332140 No Minimum Pulse Width paths to report
332102 Design is not fully constrained for setup requirements
332102 Design is not fully constrained for hold requirements
Quartus Prime Timing Analyzer was successful. 0 errors, 6 warnings
293000 Quartus Prime Full Compilation was successful. 0 errors, 19 warnings
```

Here I ensure that the IP catalog is checked out and is available for me to use

Task 2, Chue Zhang

The screenshot displays the Quartus Prime Lite Edition interface during a compilation process. The top menu bar includes File, Edit, View, Project, Assignments, Processing, Tools, Window, and Help. The main workspace is divided into several panes:

- Project Navigator:** Shows the project files: multiplexer.bdf, multiplexer_symbol.bdf, Waveform.vwf, and multiplexer_VHDL.vhd.
- Table of Contents:** Lists the compilation steps: Flow Summary, Flow Settings, Flow Non-Default Global Settings, Flow Elapsed Time, Flow OS Summary, Flow Log, Analysis & Synthesis, Fitter, Flow Messages, Flow Suppressed Messages, Assembler, and Timing Analyzer.
- Flow Summary:** Displays the compilation status: Successful - Tue Aug 31 19:24:35 2021. It lists details such as Quartus Prime Version (20.1.1 Build 720 11/11/2020 SJ Lite Edition), Revision Name (multiplexer), Top-level Entity Name (multiplexer_VHDL), Family (Cyclone V), Device (5CGXFC7C7F23C8), Timing Models (Final), Logic utilization (1 / 56,480 (< 1 %)), Total registers (0), Total pins (4 / 268 (1 %)), and Total virtual pins (0).
- Tasks:** A table showing the progress of various tasks:

Task	Time
Compile Design	00:00:48
Analysis & Synthesis	00:00:08
Fitter (Place & Route)	00:00:26
Assembler (Generate programming files)	00:00:09
Timing Analysis	00:00:05
EDA Netlist Writer	
Edit Settings	
Program Device (Open Programmer)	

A "Save IP Variation" dialog box is open, prompting for an IP variation file name and type. The file name is "43_Lab_1_multiplexer_Zhang_FA21/ZHANG_MUX_LPM" and the type is "VHDL". The "OK" button is highlighted.

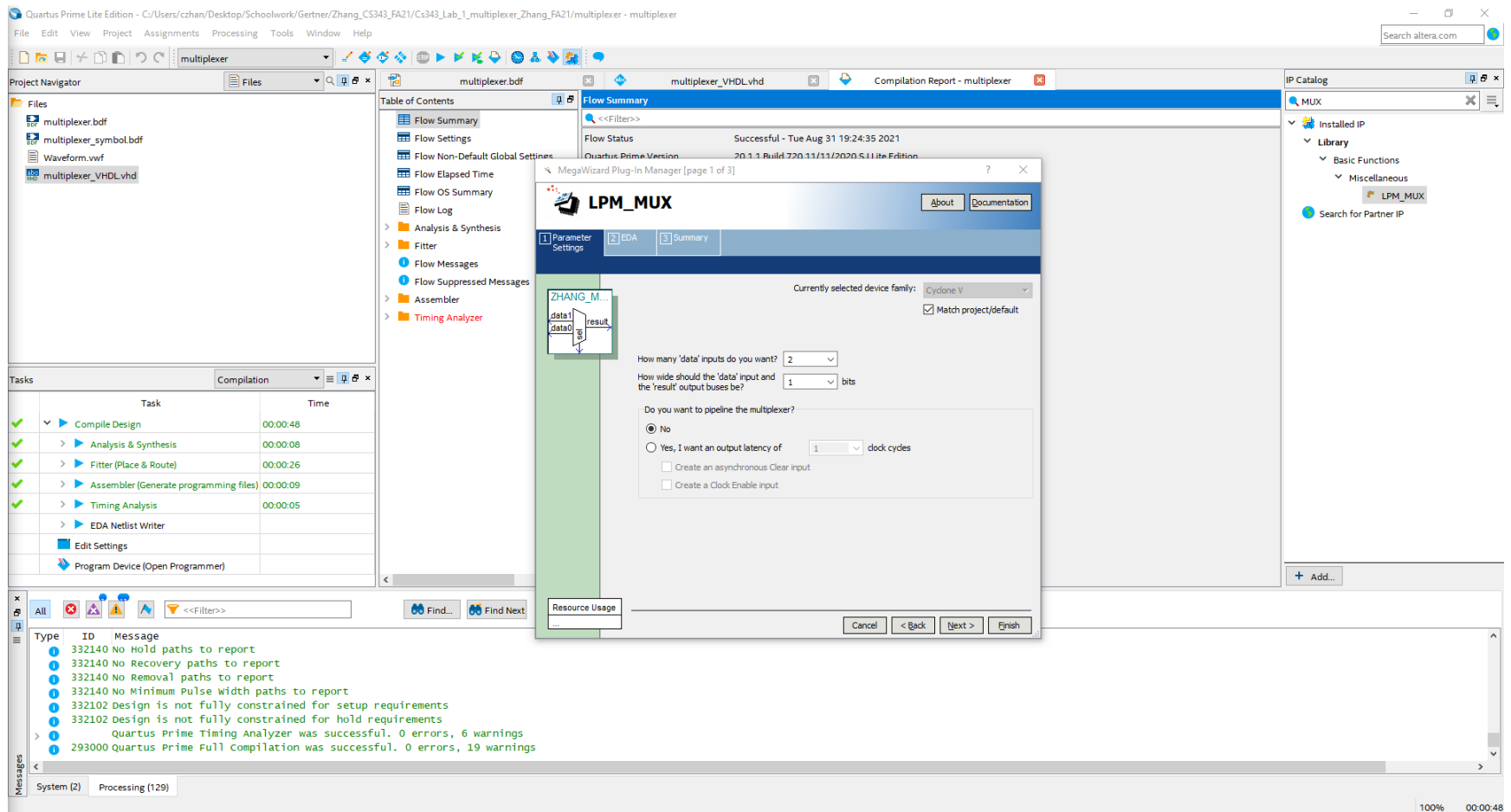
The IP Catalog on the right shows the "MUX" search results, with "LPM_MUX" selected under the "Library" > "Miscellaneous" category.

The Messages pane at the bottom shows the compilation results:

```
332140 No Hold paths to report
332140 No Recovery paths to report
332140 No Removal paths to report
332140 No Minimum Pulse Width paths to report
332102 Design is not fully constrained for setup requirements
332102 Design is not fully constrained for hold requirements
Quartus Prime Timing Analyzer was successful. 0 errors, 6 warnings
293000 Quartus Prime Full Compilation was successful. 0 errors, 19 warnings
```

In the right where the IP catalog is, I type in MUX and a drop down showing LPM_MUX shows up. I double click and press OK

Task 2, Chue Zhang



A pop up shows, I press next until I can no longer press next, then I press finish

Task 2, Chue Zhang

The screenshot displays the Quartus Prime Lite Edition interface. The top menu bar includes File, Edit, View, Project, Assignments, Processing, Tools, Window, and Help. The main workspace is divided into several panes:

- Project Navigator:** Shows the project files: multiplexer.bdf, multiplexer_symbol.bdf, Waveform.vwf, and multiplexer_VHDL.vhd.
- Table of Contents:** Lists the project's components, including Flow Summary, Flow Settings, Flow Non-Default Global Settings, Flow Elapsed Time, Flow OS Summary, Flow Log, Analysis & Synthesis, Fitter, Flow Messages, Flow Suppressed Messages, Assembler, and Timing Analyzer.
- Flow Summary:** Displays the compilation status: Successful - Tue Aug 31 19:24:35 2021. It lists the Quartus Prime Version (20.1.1 Build 720 11/11/2020 SJ Lite Edition), Revision Name (multiplexer), Top-level Entity Name (multiplexer_VHDL), Family (Cyclone V), Device (5CGXFC7C7F23C8), Timing Models (Final), Logic utilization (1 / 56,480 (< 1 %)), and Total registers (0).
- Tasks:** A table showing the compilation tasks and their durations:

Task	Time
Compile Design	00:00:48
Analysis & Synthesis	00:00:08
Fitter (Place & Route)	00:00:26
Assembler (Generate programming files)	00:00:09
Timing Analysis	00:00:05
EDA Netlist Writer	
Edit Settings	
Program Device (Open Programmer)	

A dialog box titled "Quartus Prime IP Files" is open, asking if the user wants to add the Quartus Prime IP File to the project. The file path is C:\Users\czhan\Desktop\Schoolwork\Gertner\Zhang_CS343_FA21\Cs3... The dialog also includes a checkbox for "Automatically add Quartus Prime IP Files to all projects" and a note that turning on this option permanently suppresses this dialog box. The "Yes" button is highlighted.

The bottom pane shows the Messages window with the following output:

```
System (2) Processing (129)
332140 No Hold paths to report
332140 No Recovery paths to report
332140 No Removal paths to report
332140 No Minimum Pulse Width paths to report
332102 Design is not fully constrained for setup requirements
332102 Design is not fully constrained for hold requirements
Quartus Prime Timing Analyzer was successful. 0 errors, 6 warnings
293000 Quartus Prime Full Compilation was successful. 0 errors, 19 warnings
```

A pop up shows up and I check the box that says “automatically add quartus prime IP files to all projects” and press Yes

Task 2, Chue Zhang

Quartus Prime Lite Edition - C:/Users/czhan/Desktop/Schoolwork/Gertner/Zhang_CS343_FA21/Cs343_Lab_1_muxplexer_Zhang_FA21/multiplexer - multiplexer

File Edit View Project Assignments Processing Tools Window Help

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Project Navigator

Files

- multiplexer.bdf
- multiplexer_symbol.bdf
- Waveform.vwf
- multiplexer_VHDL.vhd
- ZHANG_MUX_LPM.qip
- ZHANG_MUX_LPM.vhd**

Table of Contents

- Flow Summary
- Flow Settings
- Flow Non-Default Global Settings
- Flow Elapsed Time
- Flow OS Summary
- Flow Log
- Analysis & Synthesis
- Fitter
- Flow Messages
- Flow Suppressed Messages
- Assembler
- Timing Analyzer

Flow Summary

<<Filter>>

Flow Status	Successful - Tue Aug 31 19:24:35 2021
Quartus Prime Version	20.1.1 Build 720 11/11/2020 SJ Lite Edition
Revision Name	multiplexer
Top-level Entity Name	multiplexer_VHDL
Family	Cyclone V
Device	5CGXFC7C7F23C8
Timing Models	Final
Logic utilization (in ALMs)	1 / 56,480 (< 1 %)
Total registers	0
Total pins	4 / 268 (1 %)
Total virtual pins	0
Total block memory bits	0 / 7,024,640 (0 %)
Total DSP Blocks	0 / 156 (0 %)
Total HSSI RX PCSs	0 / 6 (0 %)
Total HSSI PMA RX Deserializers	0 / 6 (0 %)
Total HSSI TX PCSs	0 / 6 (0 %)
Total HSSI PMA TX Serializers	0 / 6 (0 %)
Total PLLs	0 / 13 (0 %)
Total DLLs	0 / 4 (0 %)

IP Catalog

Installed IP

- Project Directory
 - No Selection Available
- Library
 - Basic Functions
 - DSP
 - Interface Protocols
 - Memory Interfaces and Controllers
 - Processors and Peripherals
 - University Program
- Search for Partner IP

Tasks

Task	Time
Compile Design	
Analysis & Synthesis	00:00:08
Fitter (Place & Route)	00:00:26
Assembler (Generate programming files)	00:00:09
Timing Analysis	00:00:05
EDA Netlist Writer	
Edit Settings	
Program Device (Open Programmer)	

Messages

System (2) Processing (129)

Sets the current file entity as the top-level entity for the next compilation

100% 00:00:48

Open

- Remove File from Project
- Set as Top-Level Entity** Ctrl+Shift+V
- Create AHDL Include Files for Current File
- Create Symbol Files for Current File
- Create Verilog Instantiation Template Files for Current File
- Create VHDL Component Declaration Files for Current File
- Properties...

I set the new VHDL file as top level entity

Task 2, Chue Zhang

Quartus Prime Lite Edition - C:/Users/czhan/Desktop/Schoolwork/Gertner/Zhang_CS343_FA21/Cs343_Lab_1_mux/multiplexer_Zhang_FA21/multiplexer - multiplexer

File Edit View Project Assignments Processing Tools Window Help

Search altera.com

Project Navigator

Files

- multiplexer.bdf
- multiplexer_symbol.bdf
- Waveform.vwf
- multiplexer_VHDL.vhd
- ZHANG_MUX_LPM.qip
- ZHANG_MUX_LPM.vhd

Table of Contents

- Flow Summary
- Flow Settings
- Flow Non-Default Global Settings
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- Flow OS Summary
- Flow Log
- Analysis & Synthesis
- Fitter
- Messages
- Flow Suppressed Messages
- Assembler
- Timing Analyzer

Flow Summary

<<Filter>>

Flow Status	Successful - Tue Aug 31 19:31:21 2021
Quartus Prime Version	20.1.1 Build 720 11/11/2020 SJ Lite Edition
Revision Name	multiplexer
Top-level Entity Name	ZHANG_MUX_LPM
Family	Cyclone V
Device	5CGXFC7C7F23C8
Timing Models	Final
Logic utilization (in ALMs)	1 / 56,480 (< 1 %)
Total registers	0
Total pins	4 / 268 (1 %)
Total virtual pins	0
Total block memory bits	0 / 7,024,640 (0 %)
Total DSP Blocks	0 / 156 (0 %)
Total HSSI RX PCSs	0 / 6 (0 %)
Total HSSI PMA RX Deserializers	0 / 6 (0 %)
Total HSSI TX PCSs	0 / 6 (0 %)
Total HSSI PMA TX Serializers	0 / 6 (0 %)
Total PLLs	0 / 13 (0 %)
Total DLLs	0 / 4 (0 %)

Tasks

Compilation

Task	Time
Compile Design	00:00:43
Analysis & Synthesis	00:00:08
Fitter (Place & Route)	00:00:24
Assembler (Generate programming files)	00:00:06
Timing Analysis	00:00:05
EDA Netlist Writer	
Edit Settings	
Program Device (Open Programmer)	

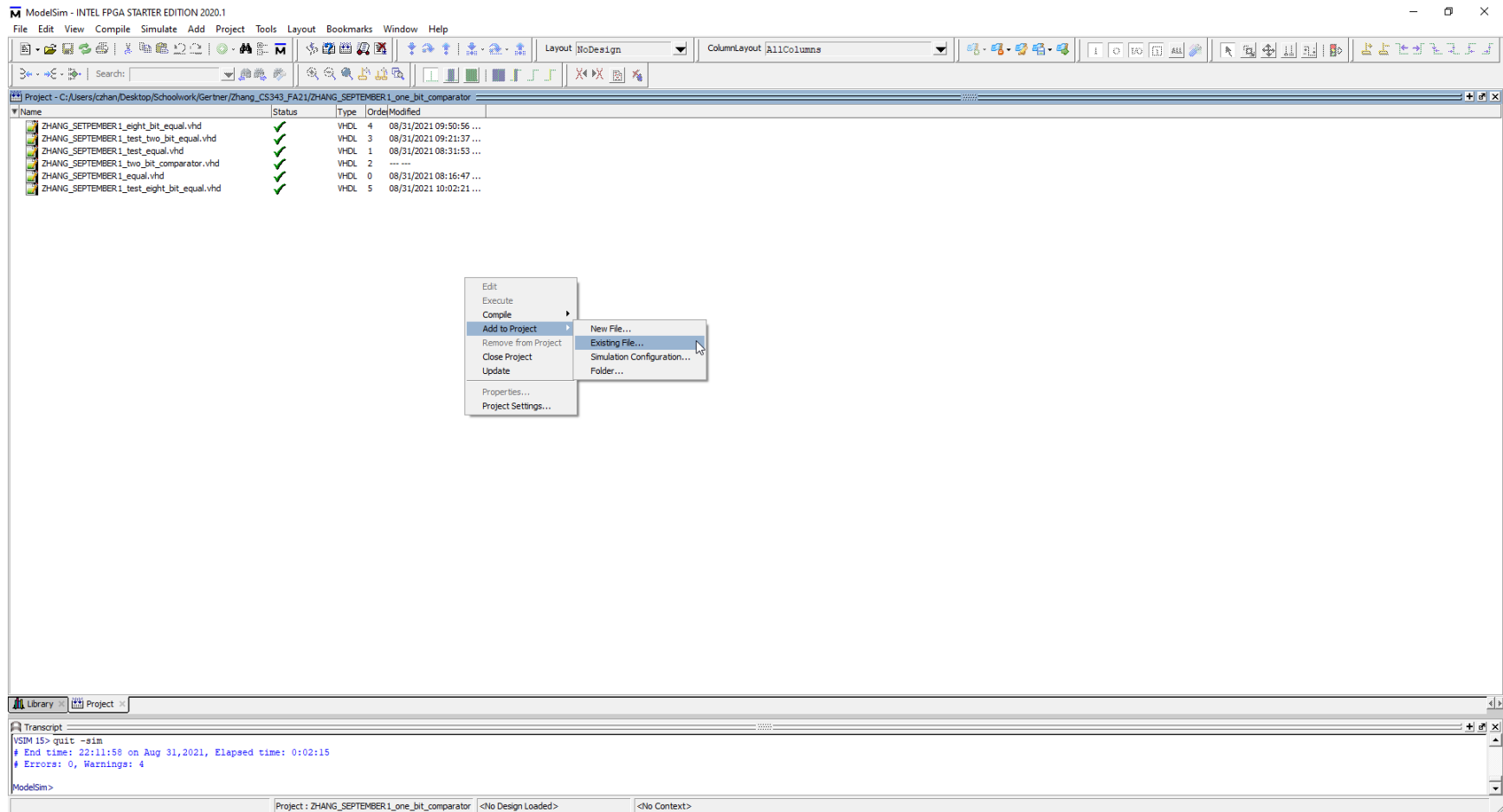
Messages

System (3) Processing (135)

100% 00:00:43

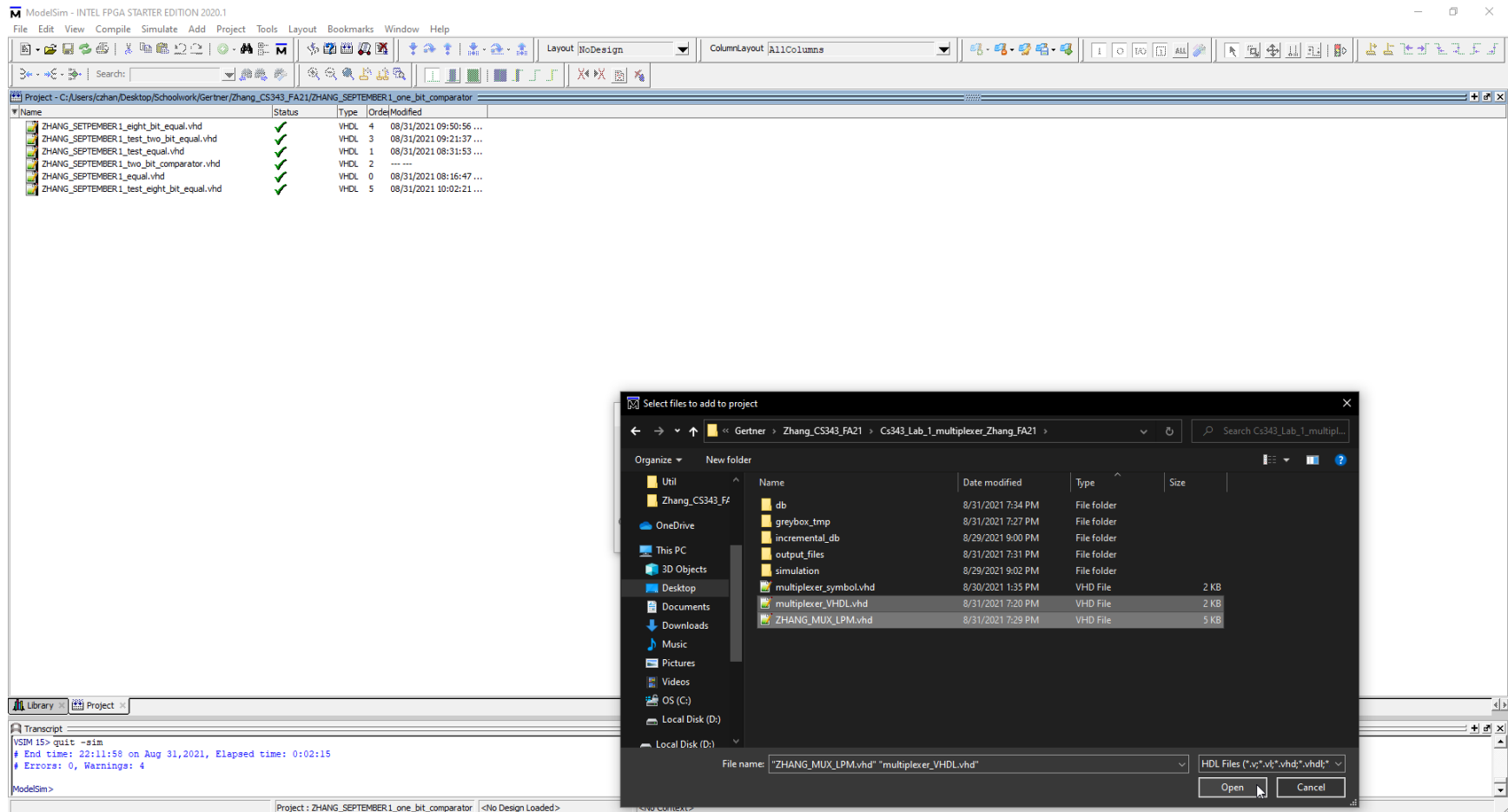
I compile with no error

Task 3, Chue Zhang



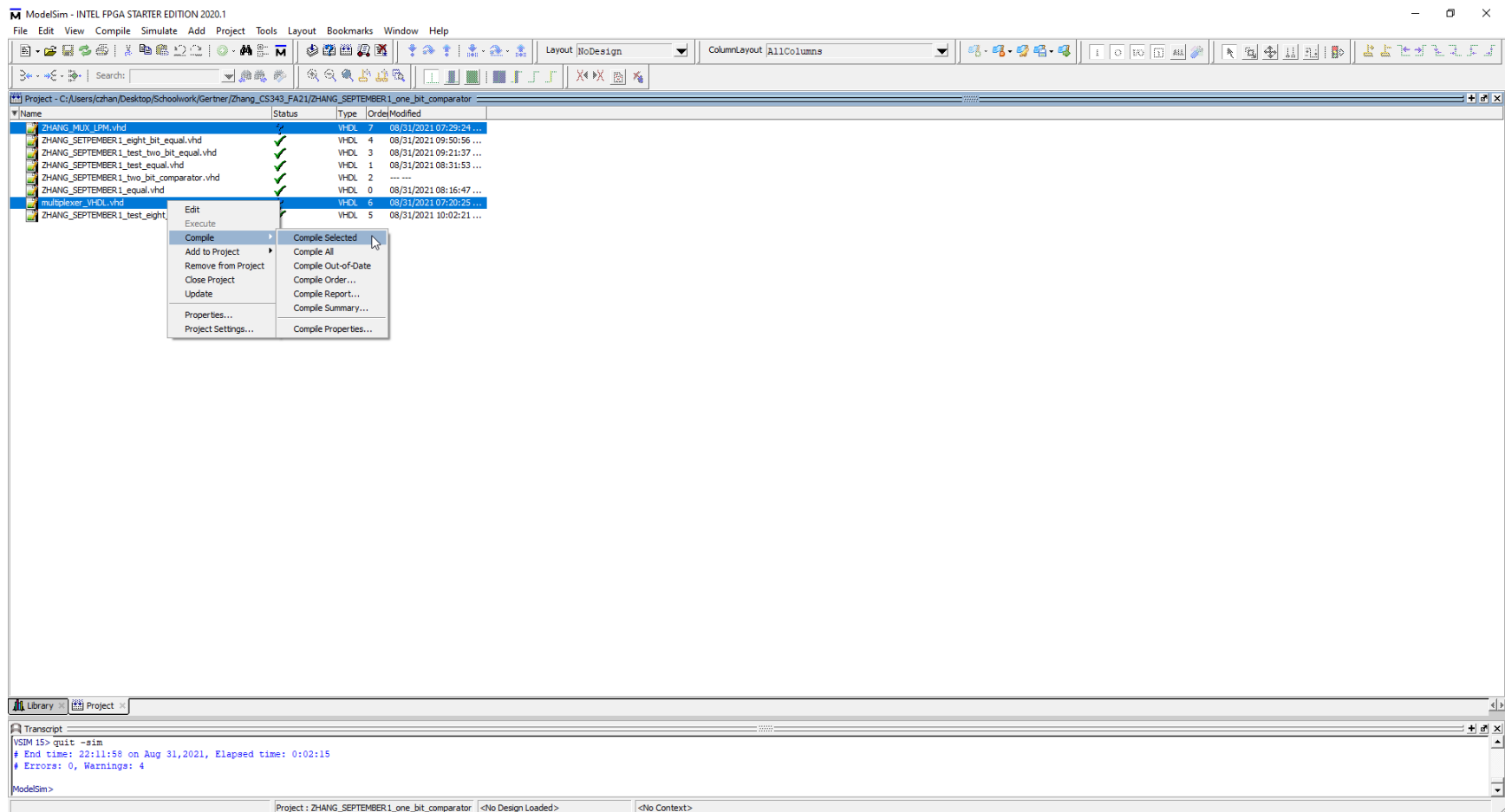
In ModelSim, I right click → Add to project → Existing file.. → and select the vhd files necessary

Task 3, Chue Zhang



Here I am selecting the LPM MUX vhd and the VHDL from my mux design

Task 3, Chue Zhang



To ensure that they are correct, I compile both files by selecting both files → right click → compile → compile selected

Task 3, Chue Zhang

ModelSim - INTEL FPGA STARTER EDITION 2020.1

File Edit View Compile Simulate Add Project Tools Layout Bookmarks Window Help

Layout: NoDesign ColumnLayout: AllColumns

Search:

Project: C:\Users\zhan\Desktop\Schoolwork\Gertner\Zhang_CS343_FA21\ZHANG_SEPTMBER1_one_bit_comparator

Name	Status	Type	Order	Modified
ZHANG_MUX_1PM.vhd	✓	VHDL	7	08/31/2021 07:29:24 ...
ZHANG_SEPTMBER1_eight_bit_equal.vhd	✓	VHDL	4	08/31/2021 09:50:56 ...
ZHANG_SEPTMBER1_test_two_bit_equal.vhd	✓	VHDL	3	08/31/2021 09:21:37 ...
ZHANG_SEPTMBER1_test_equal.vhd	✓	VHDL	1	08/31/2021 08:31:53 ...
ZHANG_SEPTMBER1_two_bit_comparator.vhd	✓	VHDL	2	---
ZHANG_SEPTMBER1_equal.vhd	✓	VHDL	0	08/31/2021 08:16:47 ...
multiplexer_VHDL.vhd	✓	VHDL	6	08/31/2021 07:20:25 ...
ZHANG_SEPTMBER1_test_eight_bit_equal.vhd	✓	VHDL	5	08/31/2021 10:02:21 ...

Library Project

Transcript

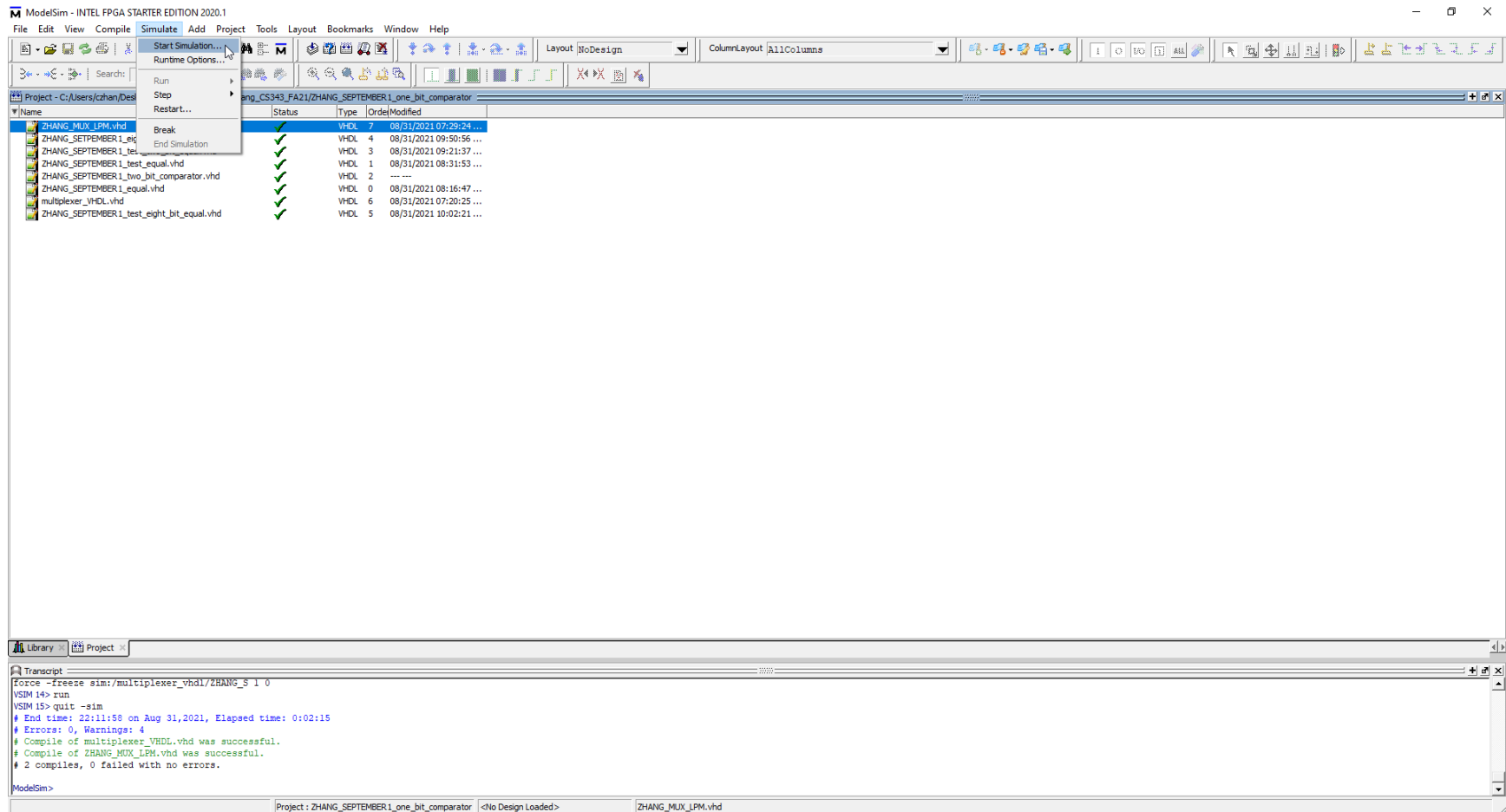
```
Force -freeze sim:/multiplexer_vhdl/ZHANG_S 1 0
V$IM 14> run
V$IM 15> quit -sim
# End time: 22:11:50 on Aug 31,2021, Elapsed time: 0:02:15
# Errors: 0, Warnings: 4
# Compile of multiplexer_VHDL.vhd was successful.
# Compile of ZHANG_MUX_1PM.vhd was successful.
# 2 compiles, 0 failed with no errors.
```

ModelSim>

Project: ZHANG_SEPTMBER1_one_bit_comparator <No Design Loaded> <No Context>

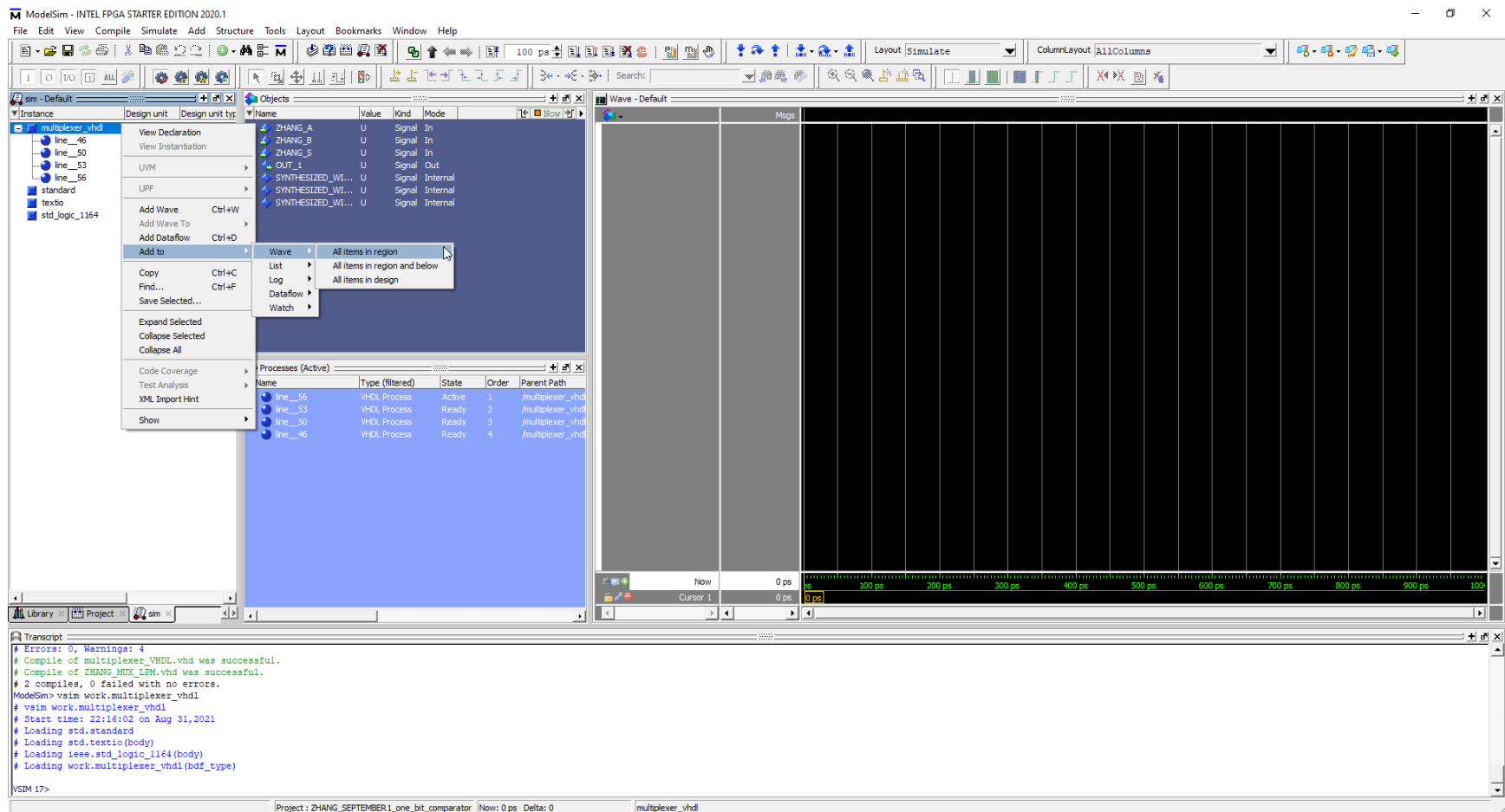
I have successfully compiled with no errors

Task 3, Chue Zhang



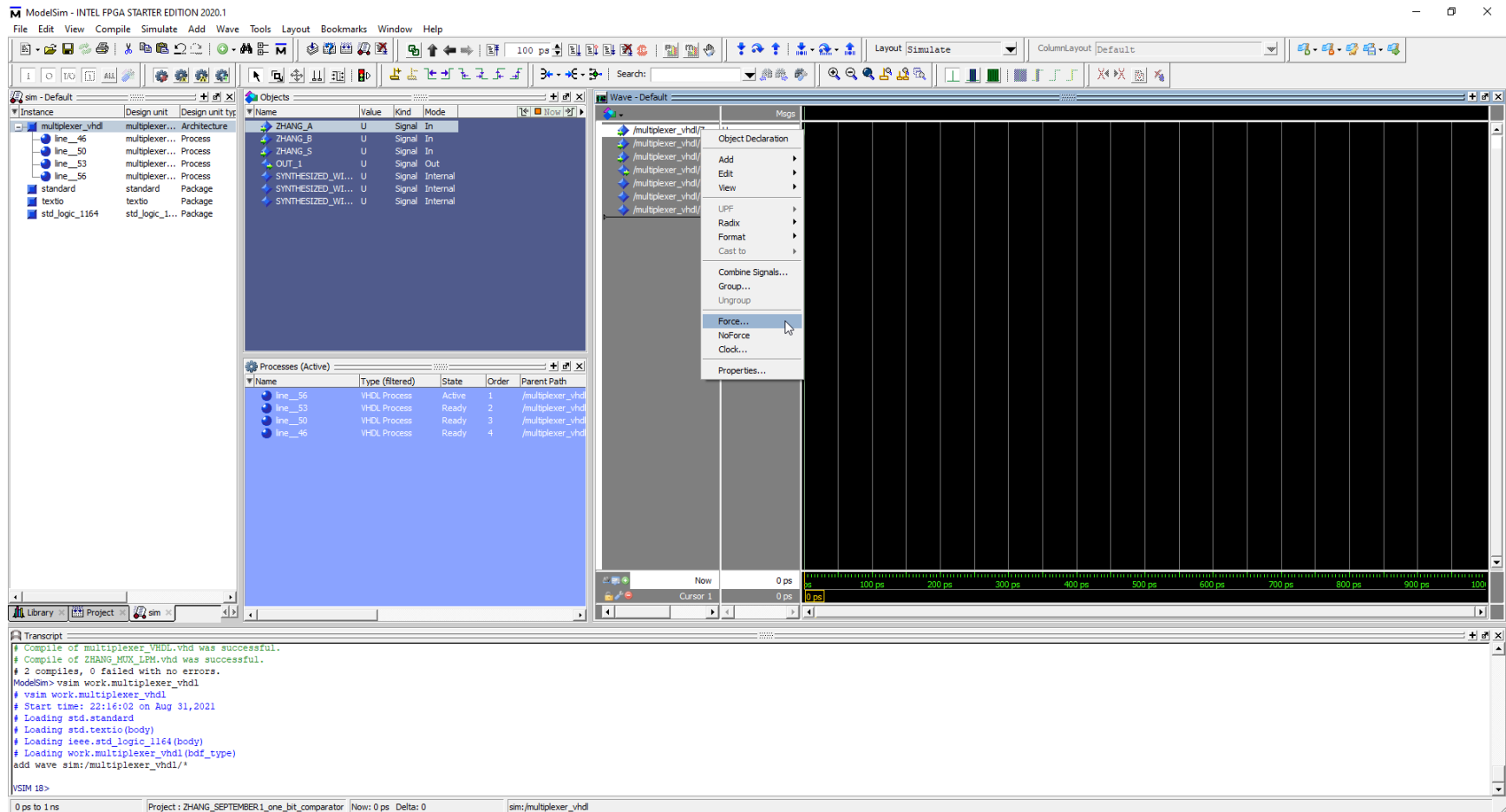
I will now proceed with simulations so on simulations → I press start simulation

Task 3, Chue Zhang



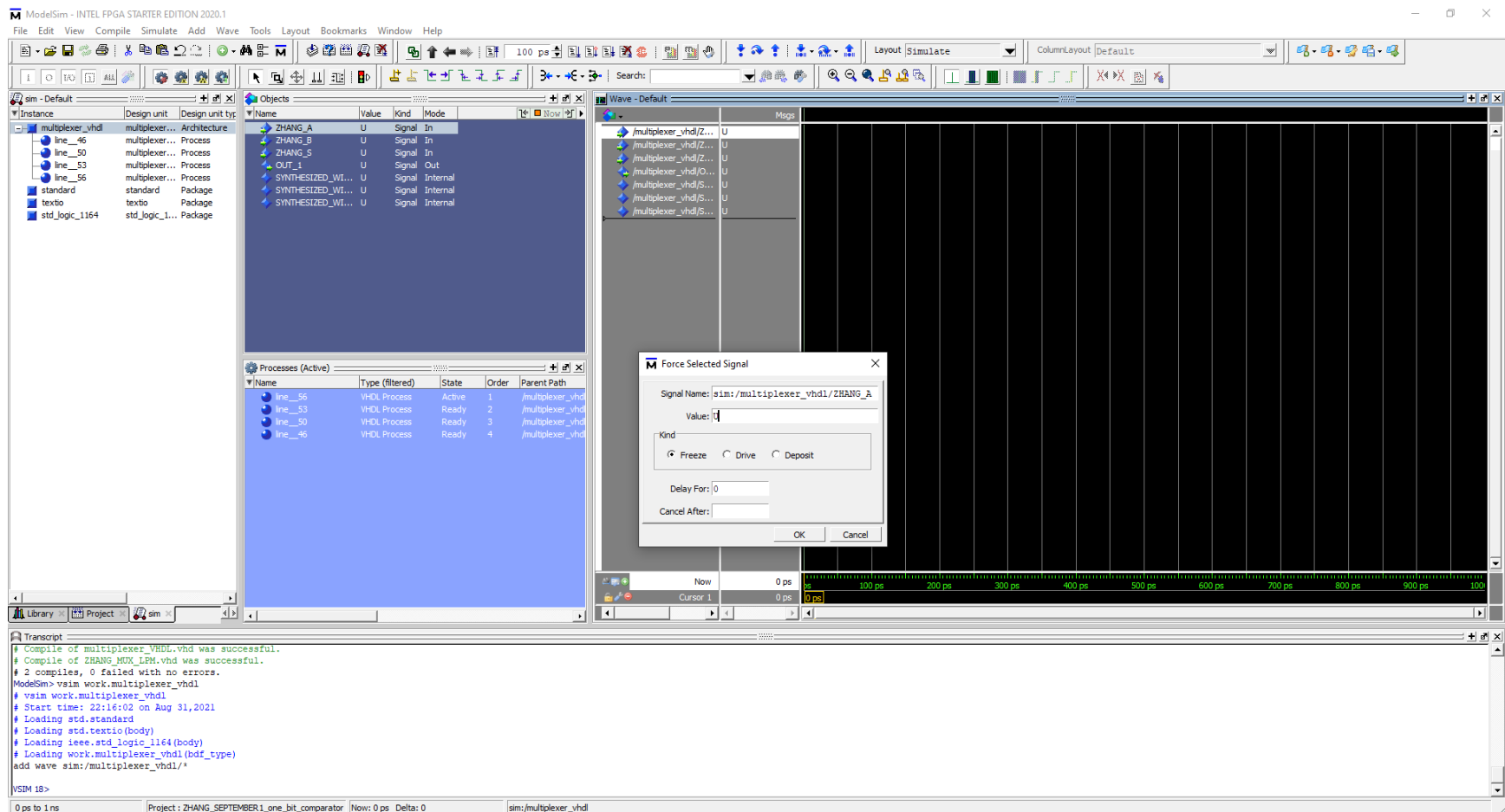
I right click the vhd1 with the items in it and right click → add to → wave → add items in region

Task 3, Chue Zhang



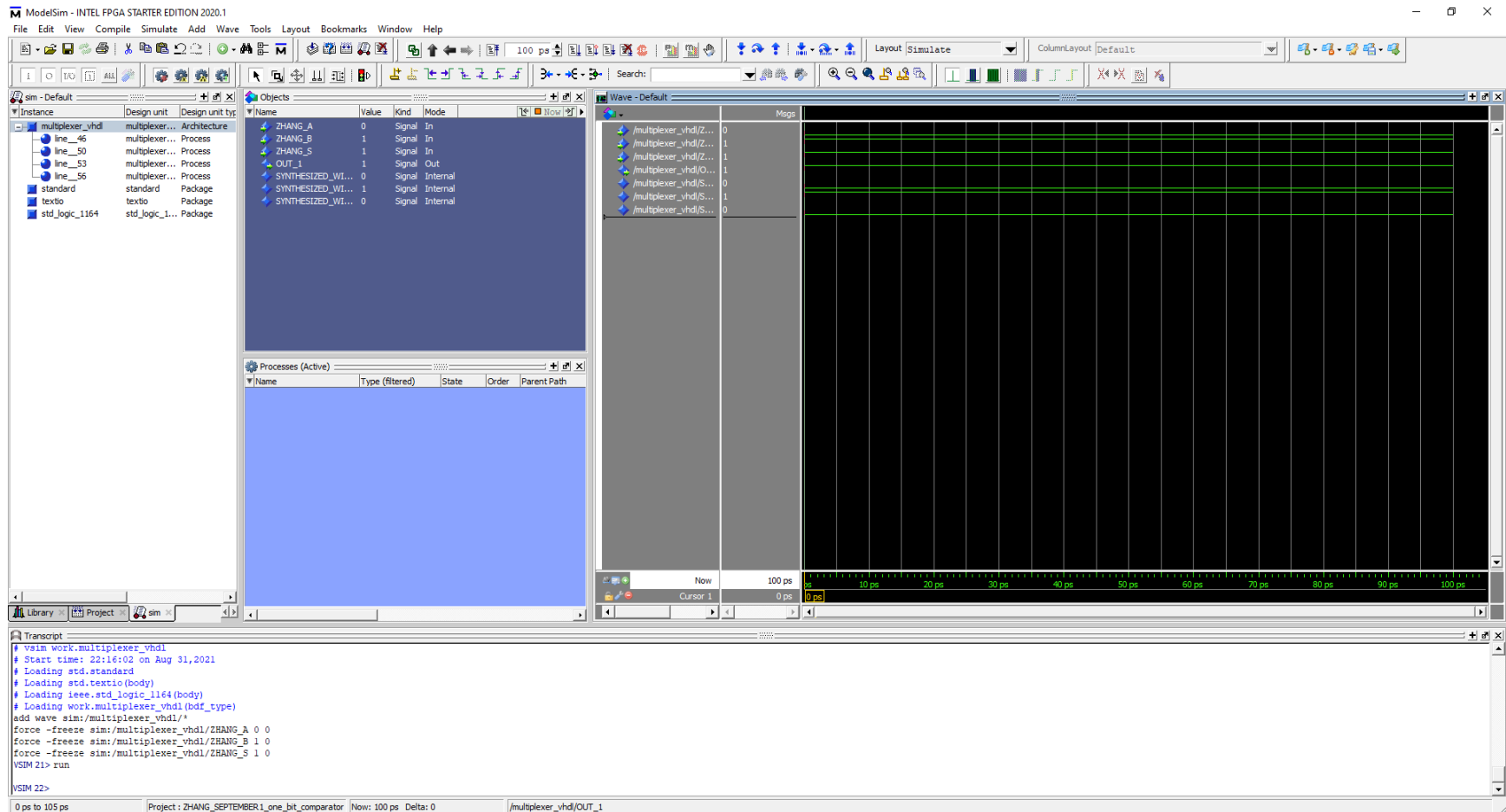
This adds all the files that I want to simulate in and then I right click ZHANG_A input and press force

Task 3, Chue Zhang



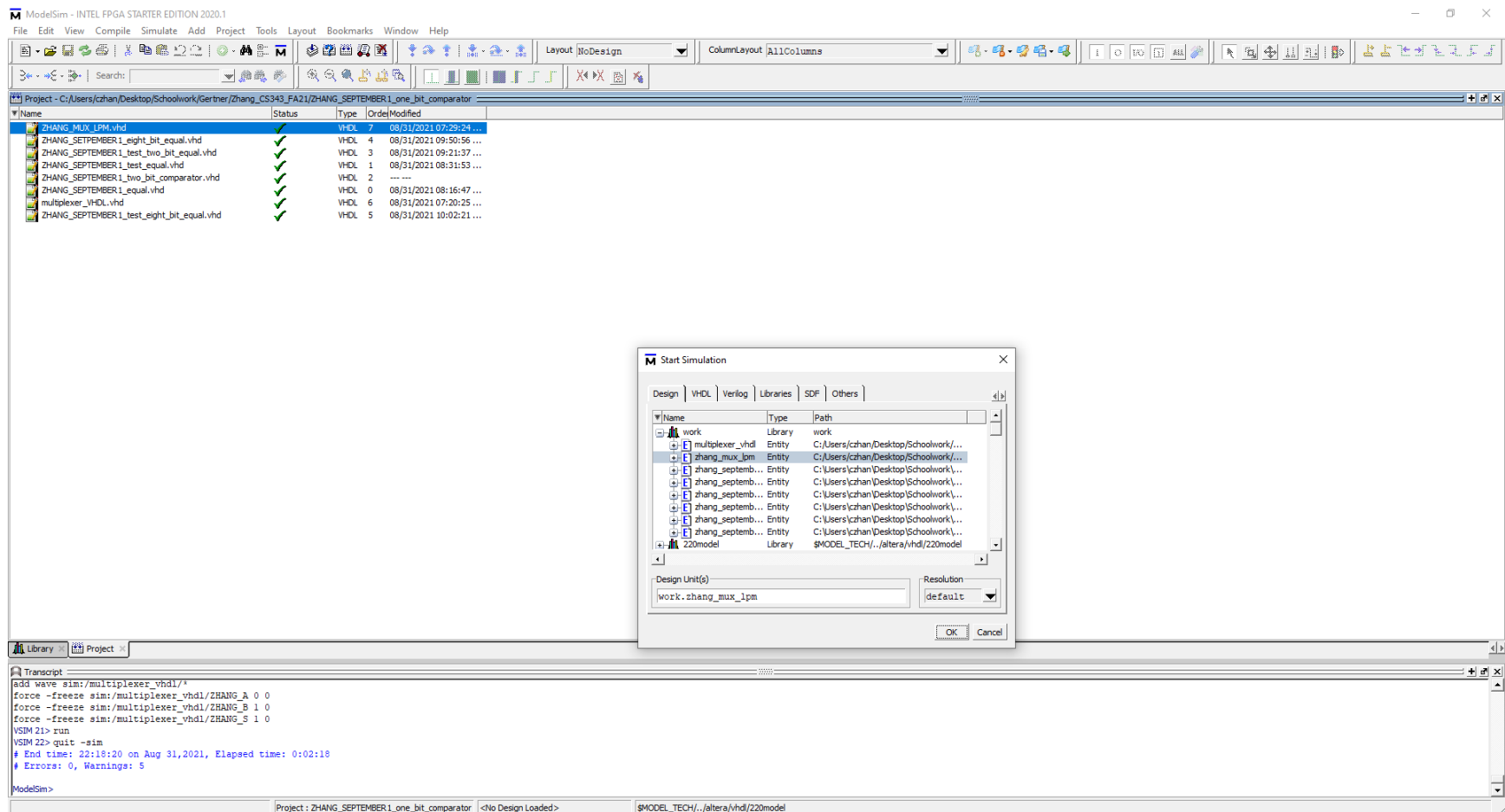
This gives me a popup menu where I can set values. For ZHANG_A I set values to 0 and for ZHANG_B and ZHANG_S I set values to 1

Task 3, Chue Zhang



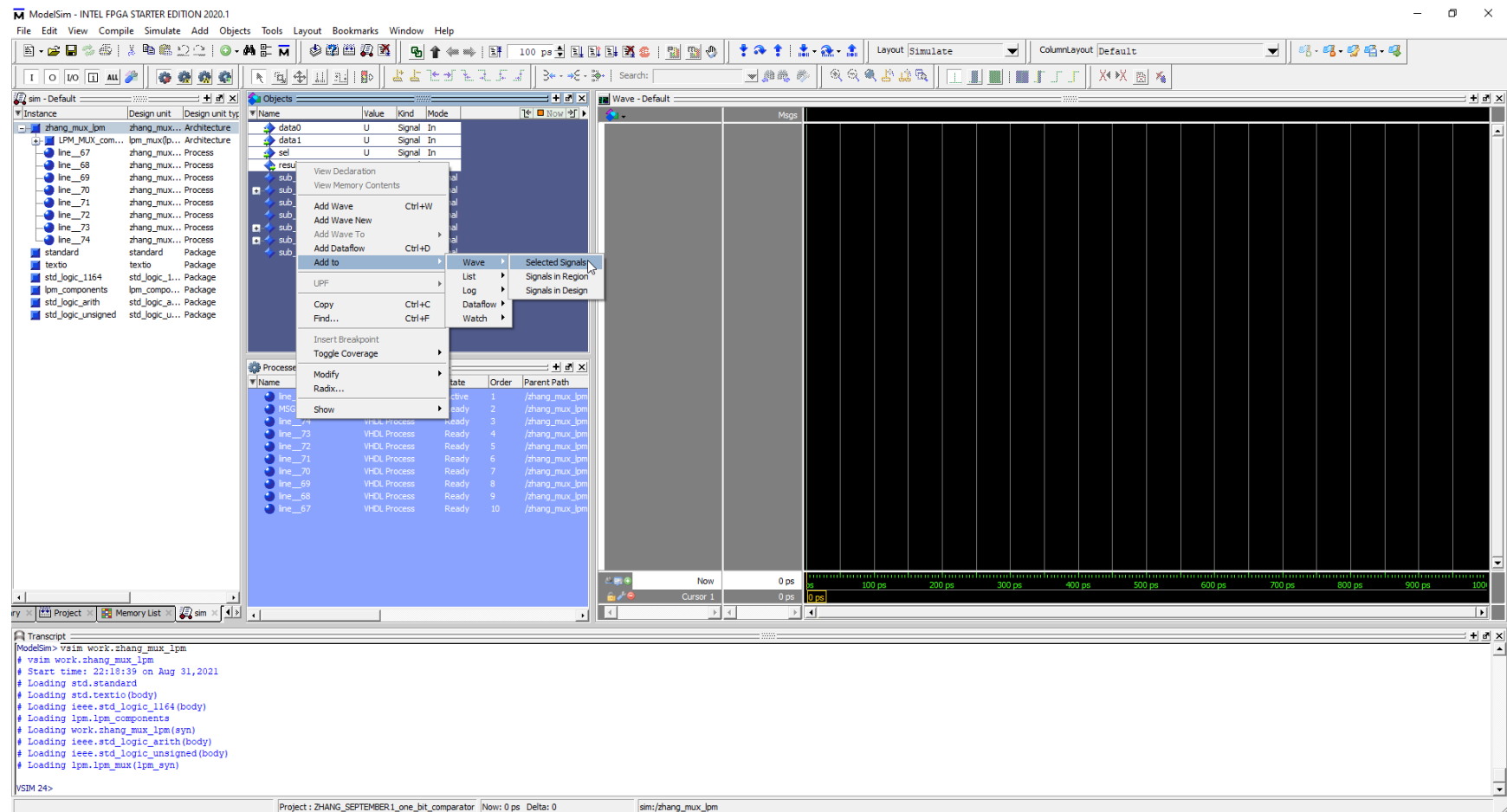
I then run the simulation and this is the output for my design's, VHDL file. No errors

Task 3, Chue Zhang



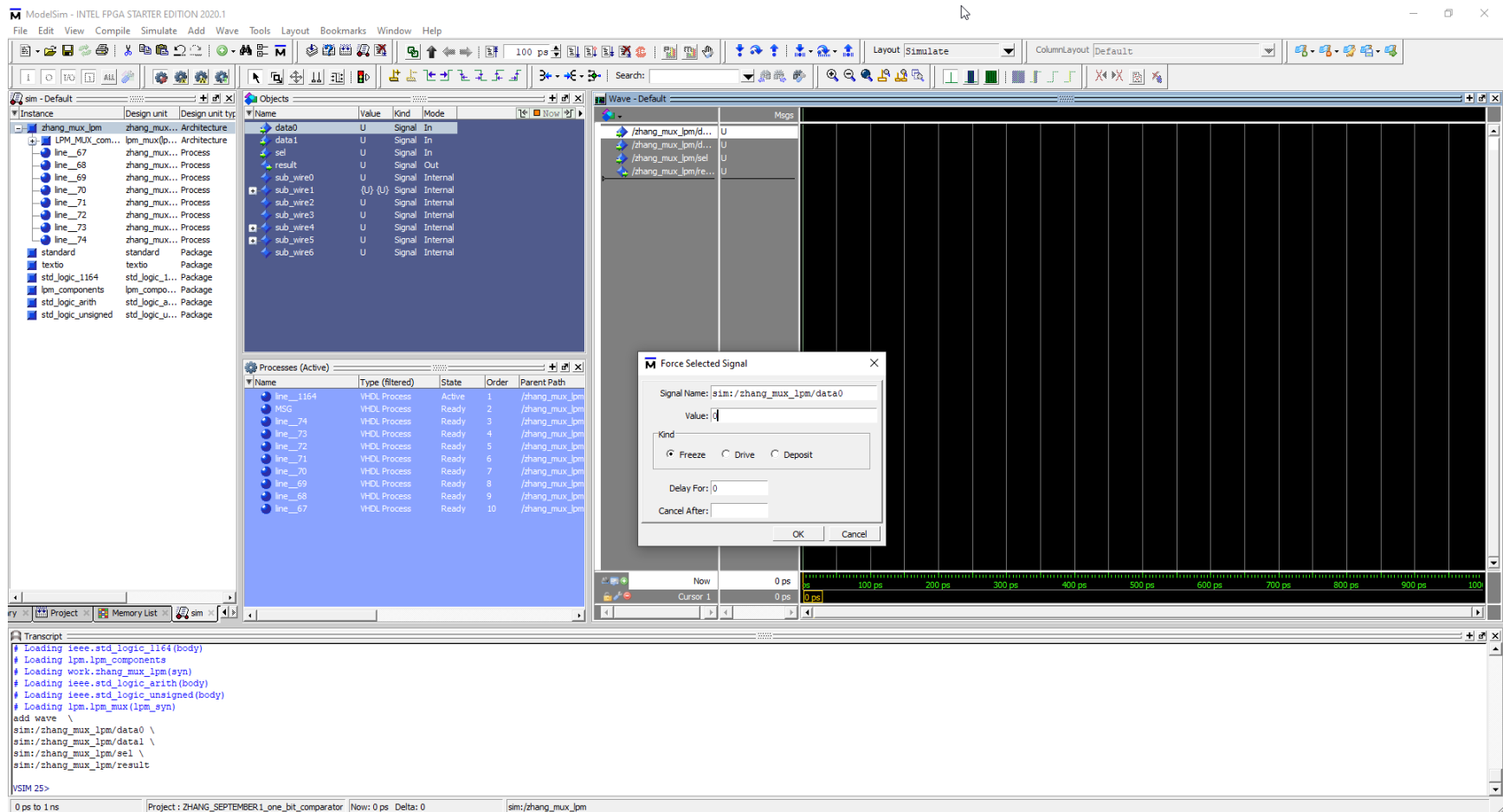
I follow the same steps as what I did for the previous VHDL file but instead, it is for the LPM MUX VHDL file

Task 3, Chue Zhang



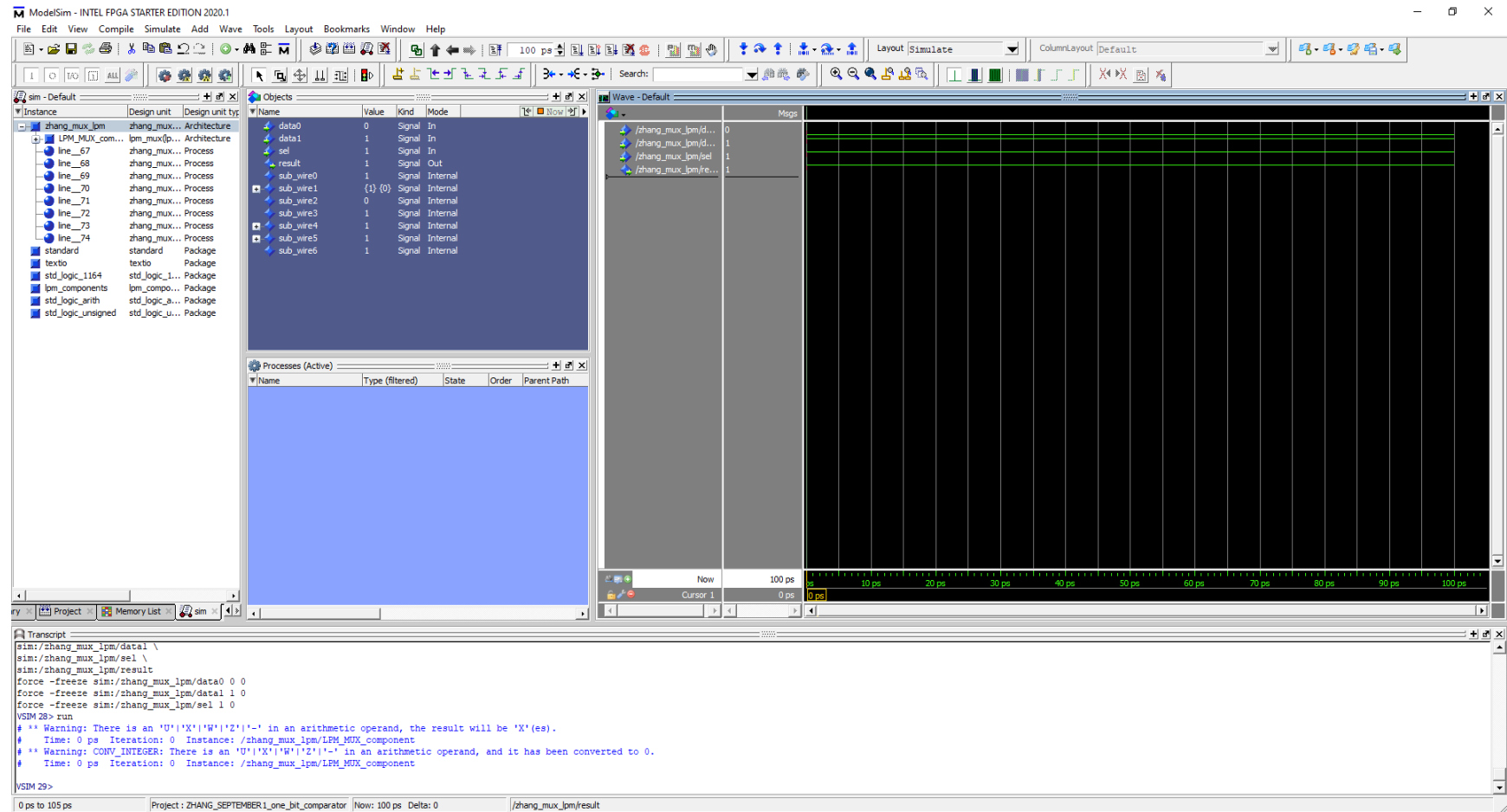
Like before, I add what I want to simulate however, I am only selecting the values necessary to be simulated with

Task 3, Chue Zhang



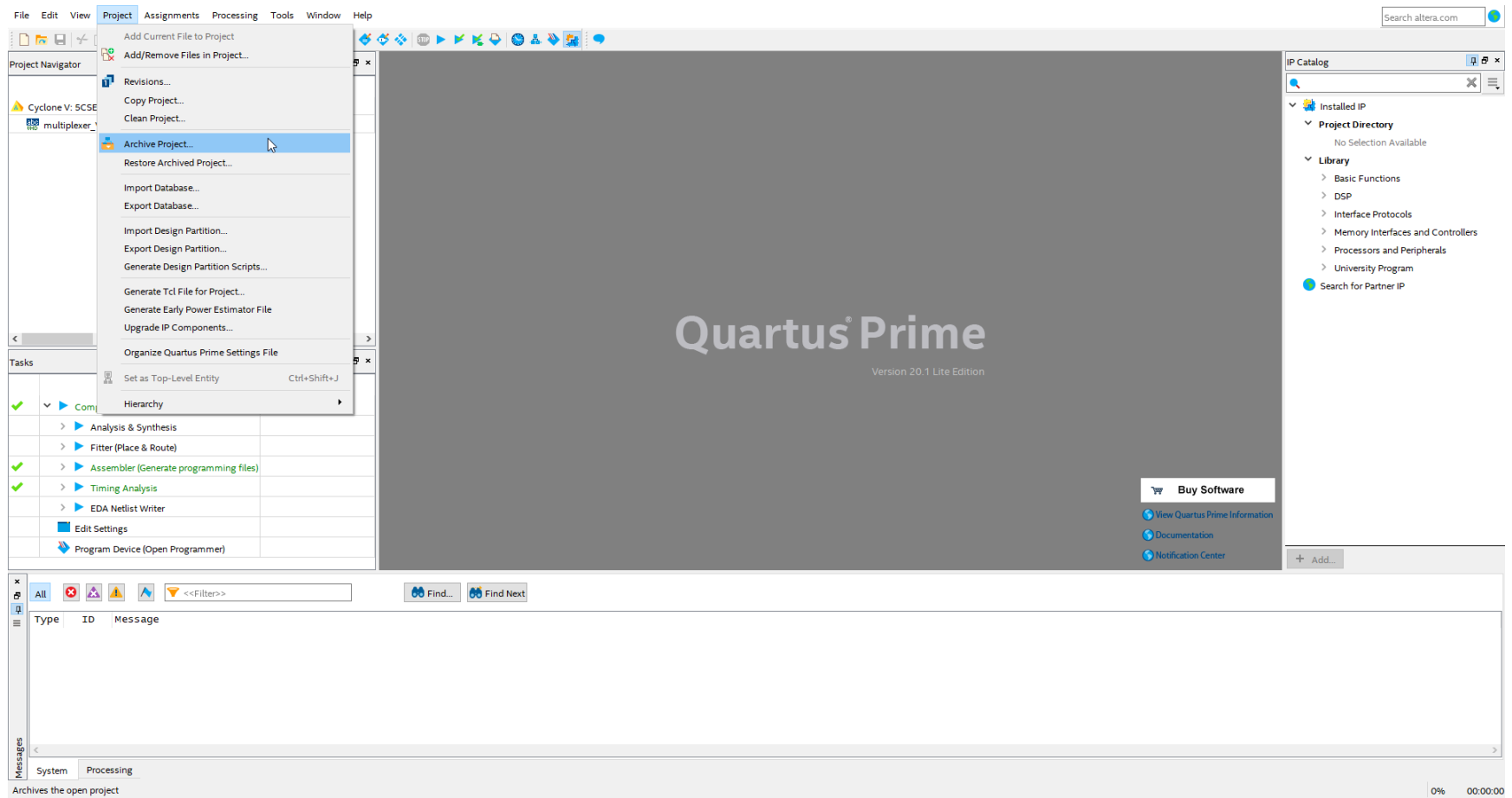
Like before, I right click on the inputs and I press force. Again will I set the values of data0 to "0" and data1 and sel to "1"

Task 3, Chue Zhang



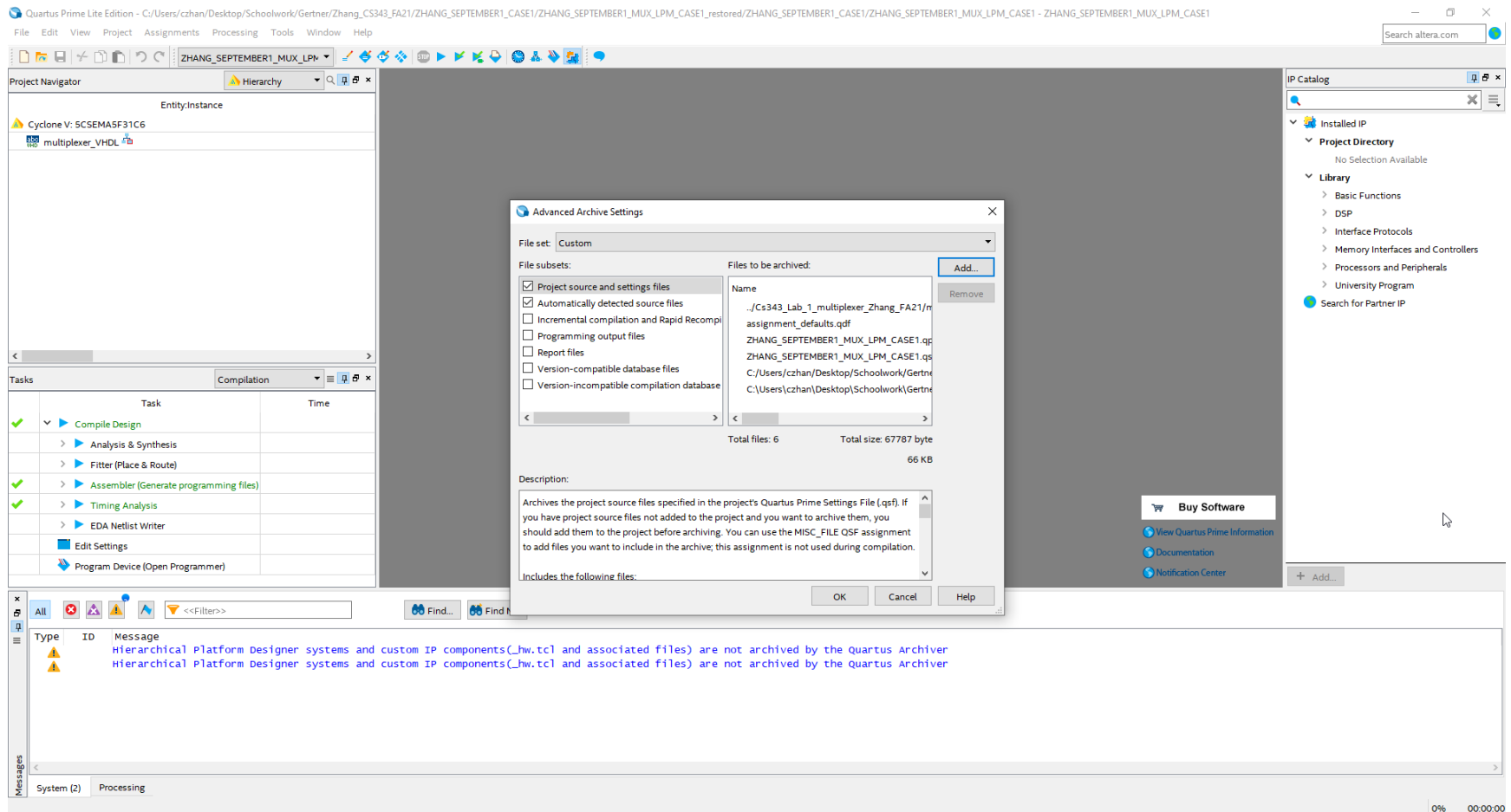
This is the output of the waveform. No errors

Task 4, Chue Zhang



To archive a project, click on project → archive project

Task 4, Chue Zhang



To add a README.TXT to the archive, press advanced → then the image above should show. Press add then add the respective file you wish to add in.

Task 4, Chue Zhang

HOW TO LOAD ARCHIVE AND RUN CONTENTS WITHIN

QUARTUS

1. Download the archive file
2. You can open the archive file directly from file --> open project --> open archive file
This should load up the contents of the archive file.
3. You should see a vhd file. Right click that vhd file and set it as the top level entity.
4. Go ahead and try to compile it doing
Processing --> Start compiling
This process should take a couple minutes, it depends on how strong your computer is.
5. You should have no errors compiling, you can even start using this in your own block file by right clicking the vhd file and pressing "Create symbol files for current file"
6. Make a new block file then press symbols tool and you can now use it
The symbol tool should look like this

```
> Project  
> c:/intelfpga_lite...
```

open project and it should show

MODELSIM

1. Open CMD
2. in the terminal, type in VSIM and modelsim should show up
3. Create a new project by going to file --> new --> project
4. Press add existing file, and within the directory of where you loaded the archive file,
load in the vhd file
5. Compile it to ensure correctness in the code, double click the vhd to view the code
6. Press Simulate at the top bar --> start simulation
7. press the project name you created and open up the vhd file
8. on the instances tab to the left, right click the vhd file instance and click add to wave
9. you should notice on the right that there are now waves to be inputted in, right click the inputs
ZHANG_A...
ZHANG_B...
ZHANG_S...
and press force and input values 0 or 1 to simulate the design.

This is the readme file that I will be including in, complete the archive by pressing ok

Task 4, Chue Zhang

Quartus Prime Lite Edition - C:/Users/czhan/Desktop/Schoolwork/Gertner/Zhang_CS343_FA21/ZHANG_SEPTMBER1_CASE1/ZHANG_SEPTMBER1_MUX_LPM_CASE1_restored/ZHANG_SEPTMBER1_CASE1/ZHANG_SEPTMBER1_MUX_LPM_CASE1 - ZHANG_SEPTMBER1_MUX_LPM_CASE1

File Edit View Project Assignments Processing Tools Window Help

Search altera.com

Project Navigator: Entity: Instance
Cyclone V: SC5EMA5F31C6
multiplexer_VHDL

Table of Contents: Flow Summary, Flow Settings, Flow Non-Default Global Settings, Flow Elapsed Time, Flow OS Summary, Flow Log, Analysis & Synthesis, Fitter, Assembler, Timing Analyzer, Archive Project, Flow Messages, Flow Suppressed Messages

Flow Summary: Flow Status: Successful - Wed Sep 01 17:49:03 2021
Quartus Prime Version: 20.1.1 Build 720 11/11/2020 SJ Lite Edition
Revision Name: ZHANG_SEPTMBER1_MUX_LPM_CASE1
Top-level Entity Name: multiplexer_VHDL
Family: Cyclone V
Device: SC5EMA5F31C6
Timing Models: Final
Logic utilization (in ALMs): 1 / 32,070 (< 1 %)
Total registers: 0
Total pins: 4 / 457 (< 1 %)
Total virtual pins: 0
Total block memory bits: 0 / 4,065,280 (0 %)
Total DSP Blocks: 0 / 4 (0 %)
Total HSSI RX PCSs: 0 / 4 (0 %)
Total HSSI PMA RX: 0 / 4 (0 %)
Total HSSI TX PCSs: 0 / 4 (0 %)
Total HSSI PMA TX: 0 / 4 (0 %)
Total PLLs: 0 / 4 (0 %)
Total DLLs: 0 / 4 (0 %)

Quartus Prime
Project successfully archived.
OK

Messages: System (2) Processing (20)
Type ID Message
Generated archive 'C:/Users/czhan/Desktop/Schoolwork/Gertner/Zhang_CS343_FA21/ZHANG_SEPTMBER1_CASE1/ZHANG_SEPTMBER1_MUX_LPM_CASE1_restored/ZHANG_SEPTMBER1_CASE1/ZHANG_SEPTMBER1_MUX_LPM_CASE1.qar'
Generated report 'ZHANG_SEPTMBER1_MUX_LPM_CASE1.archive.rpt'
23030 Evaluation of Tcl script c:/intelfpga_lite/20.1/quartus/common/tcl/apps/qpm/qar.tcl was successful
Quartus Prime shell was successful. 0 errors, 2 warnings

100% 00:00:02

Once the archived has been successfully created, a popup like this should show. Also refer to the green text below for success.