# ALU : Waveforms

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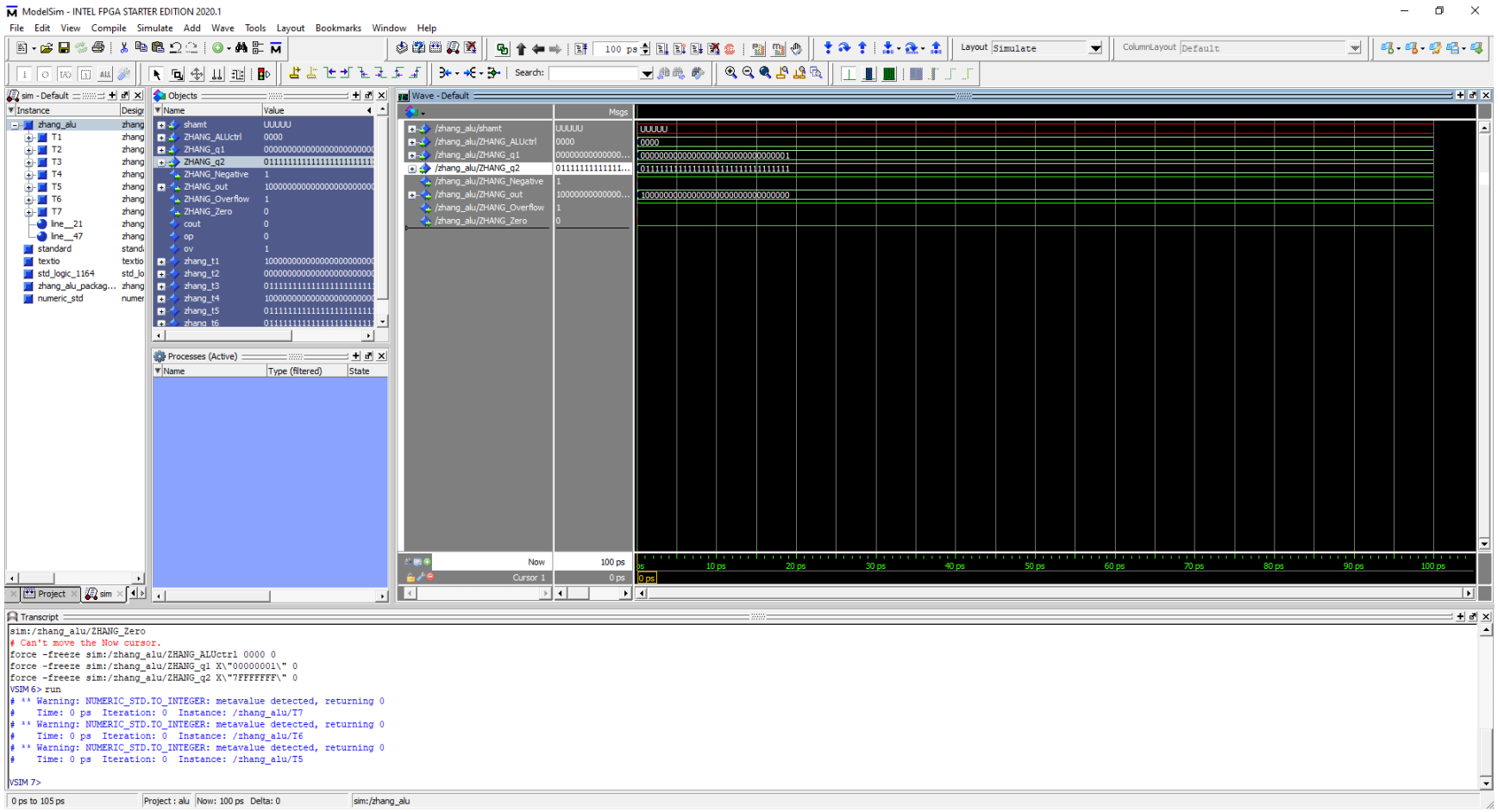
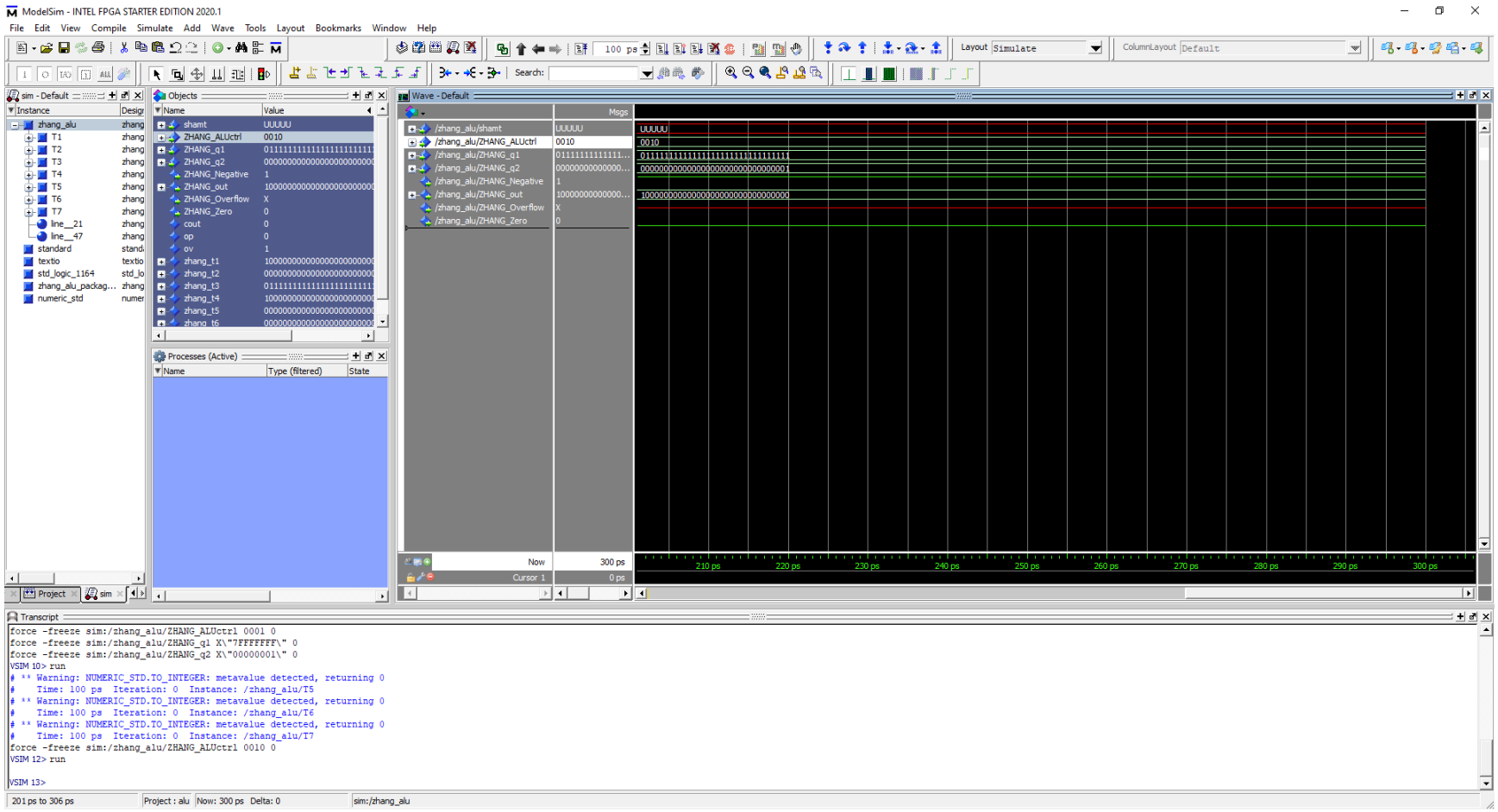
Csc343 Fall 2021

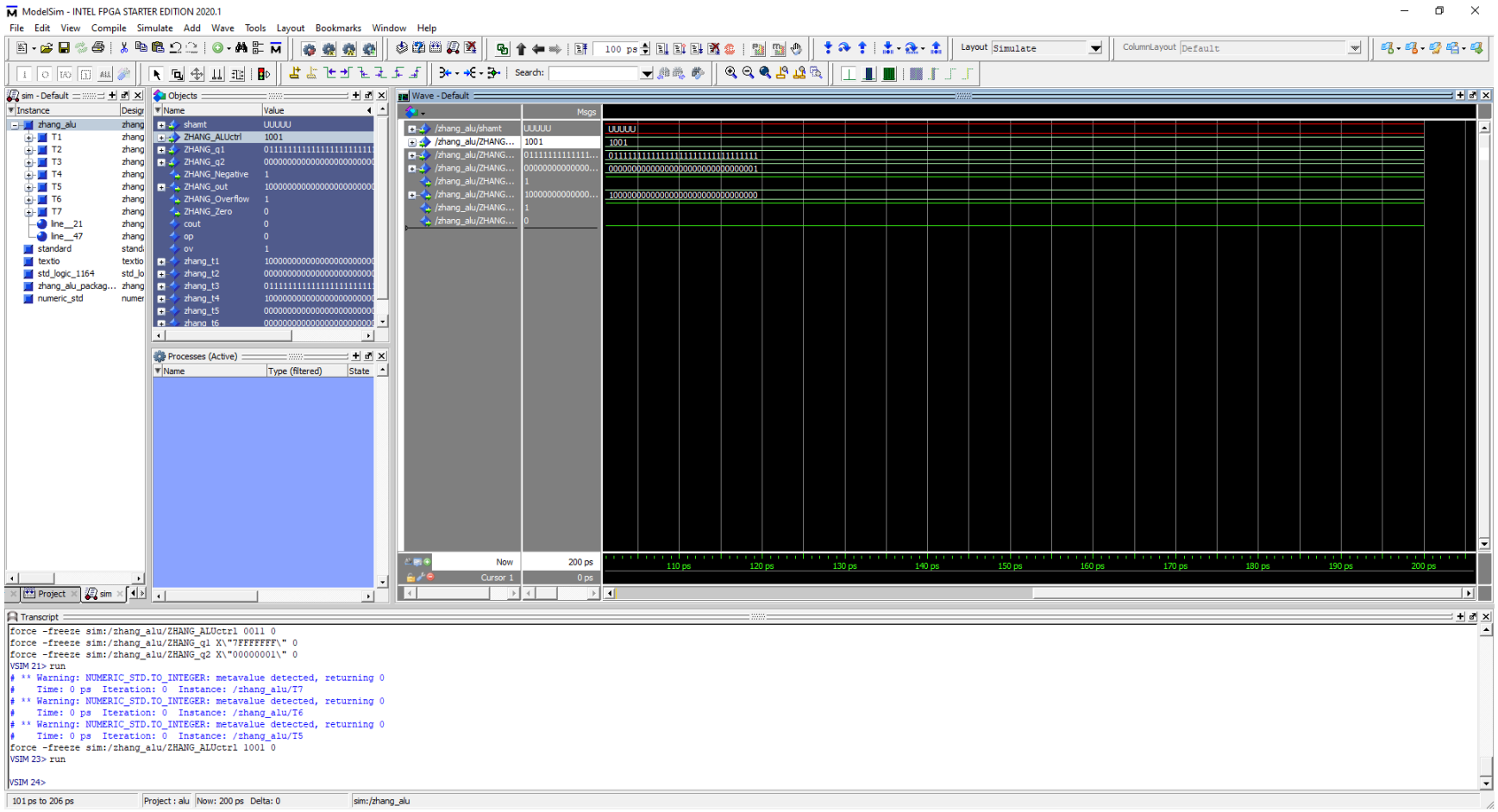
Professor Gertner



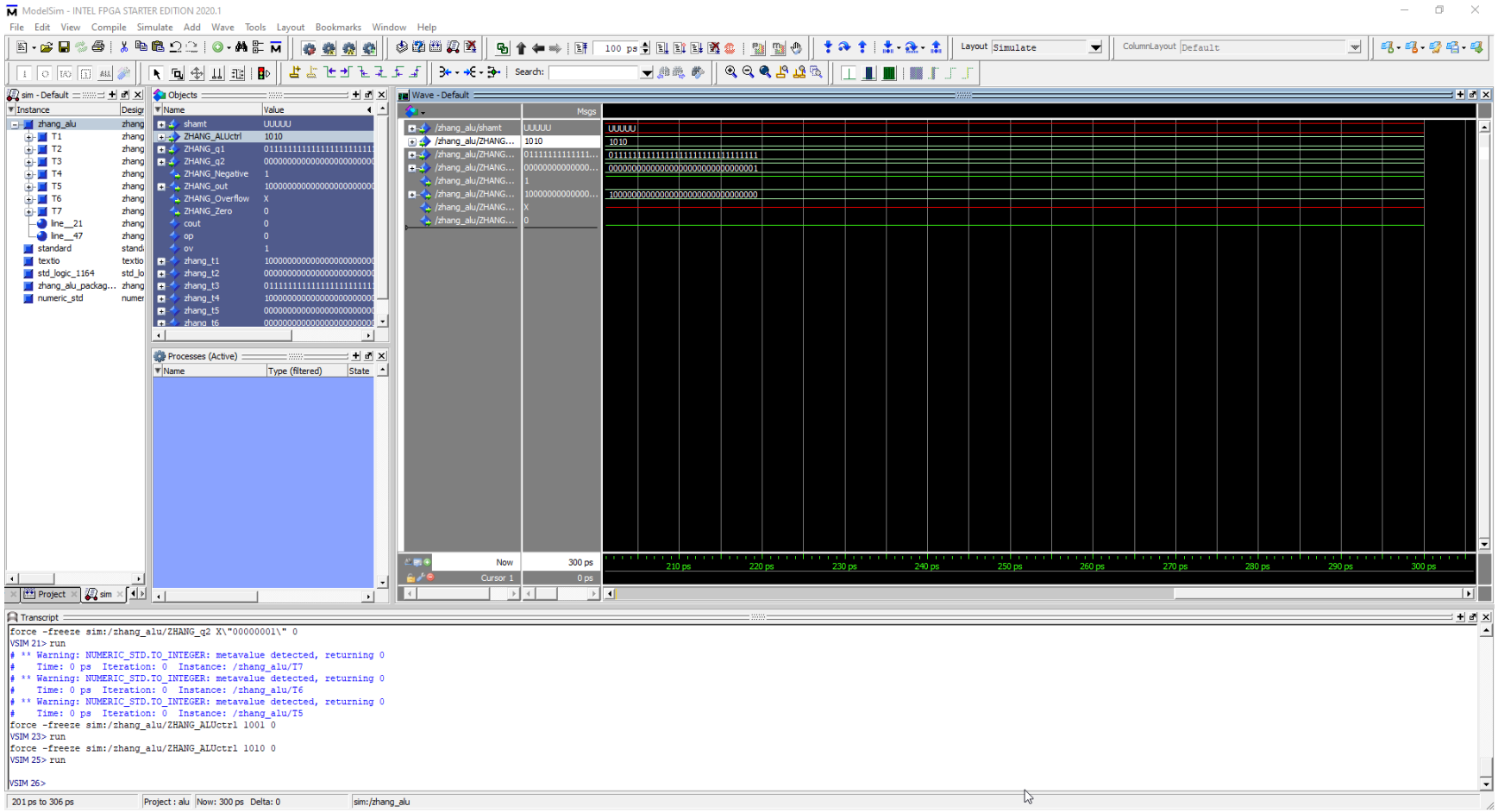

Op code = 0000, 7FFF FFFF add 0000 0001, Output = 8000 0000, All flags shown. Takes two operands and perform add operation onto them



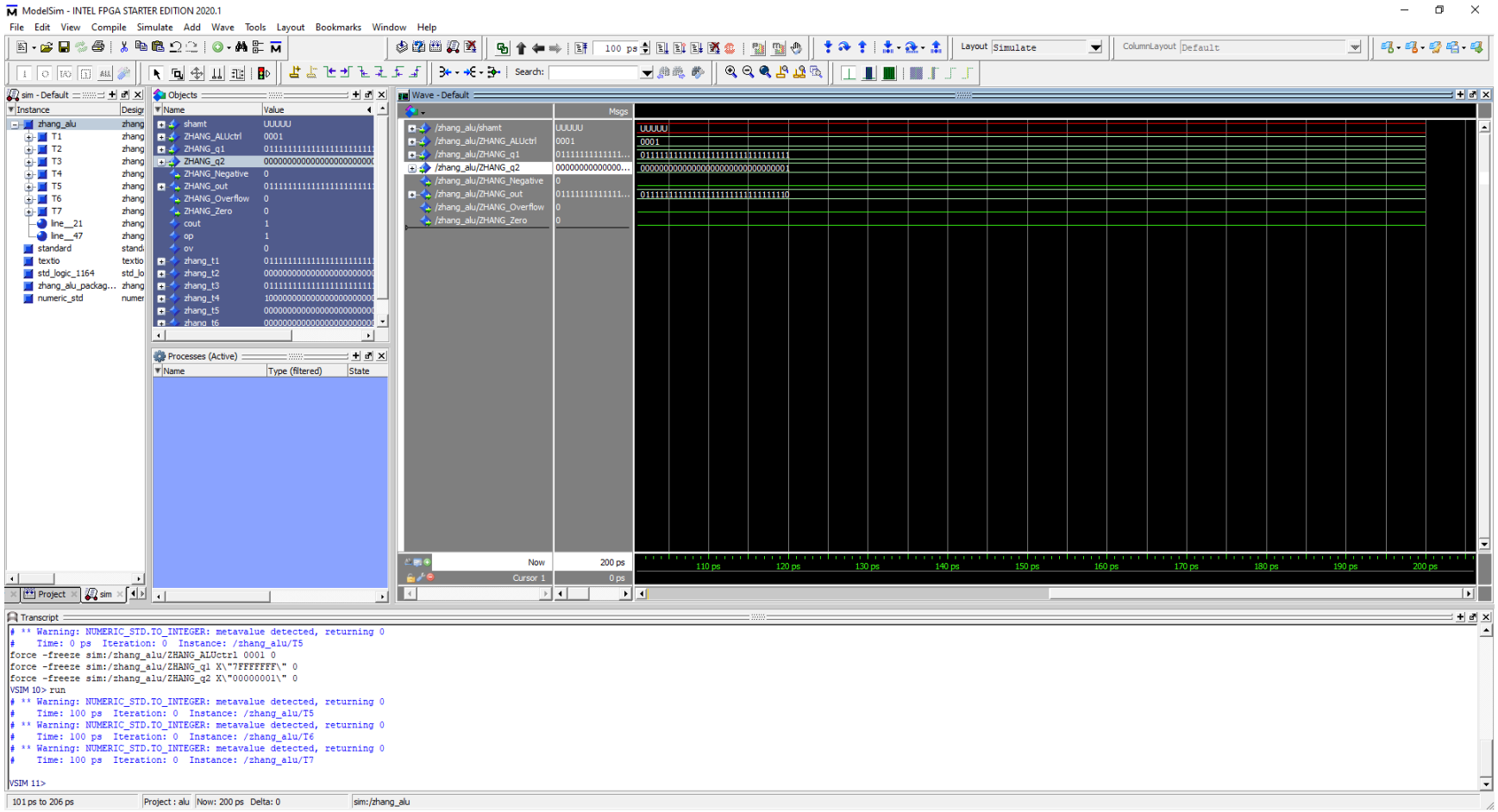

Opcode = 0010, 7FFF FFFF addu 0000 0001, Output = 8000 0000 with no overflow. Takes two operands and performs add operation on them and returns no overflow flag.



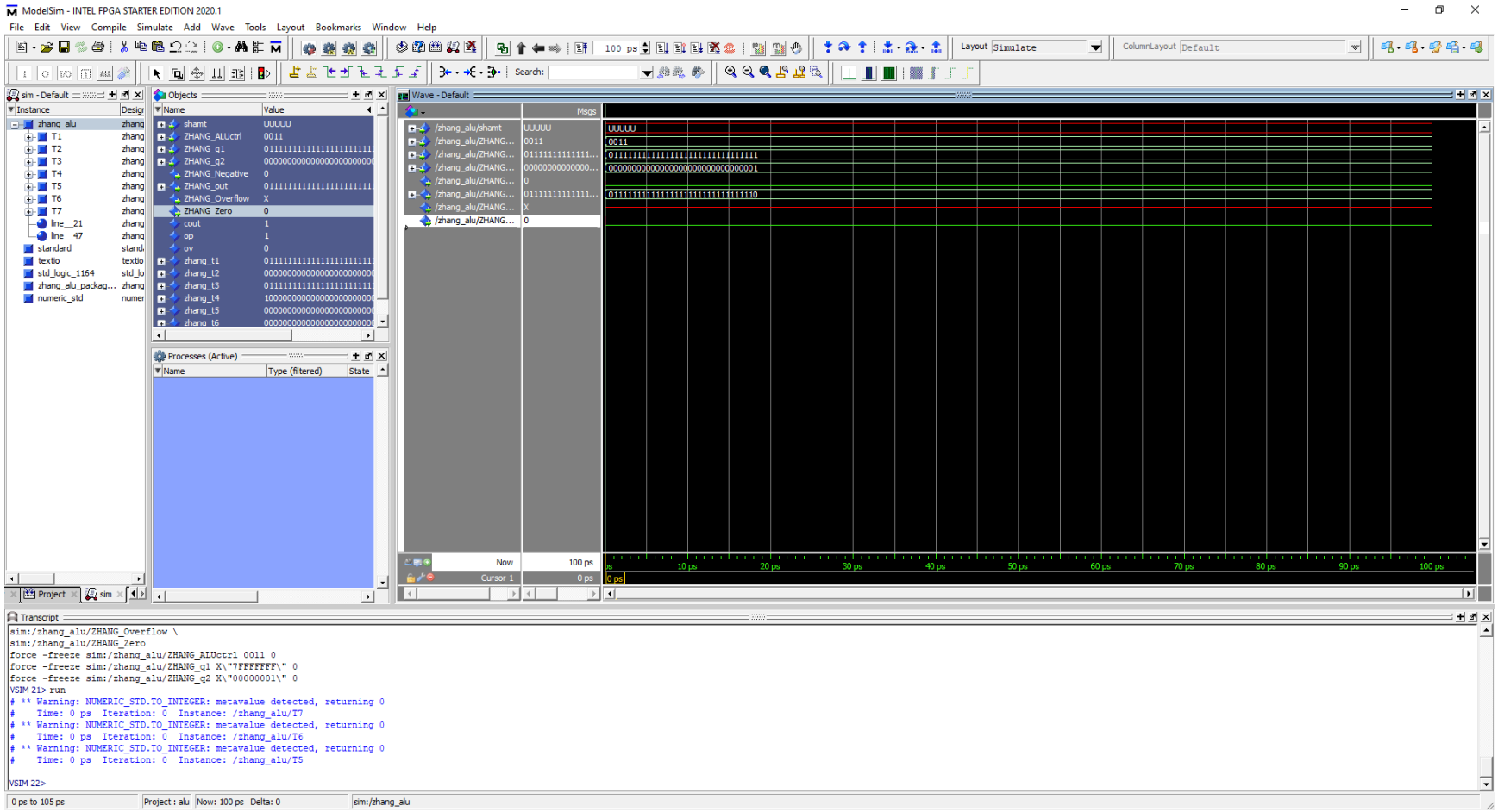

Opcode: 1001, 7FFF FFFF addi 0000 0001, Output = 8000 0000 with overflow flag. Performs Addi operation on operand 1 and imm16 with sign extension.



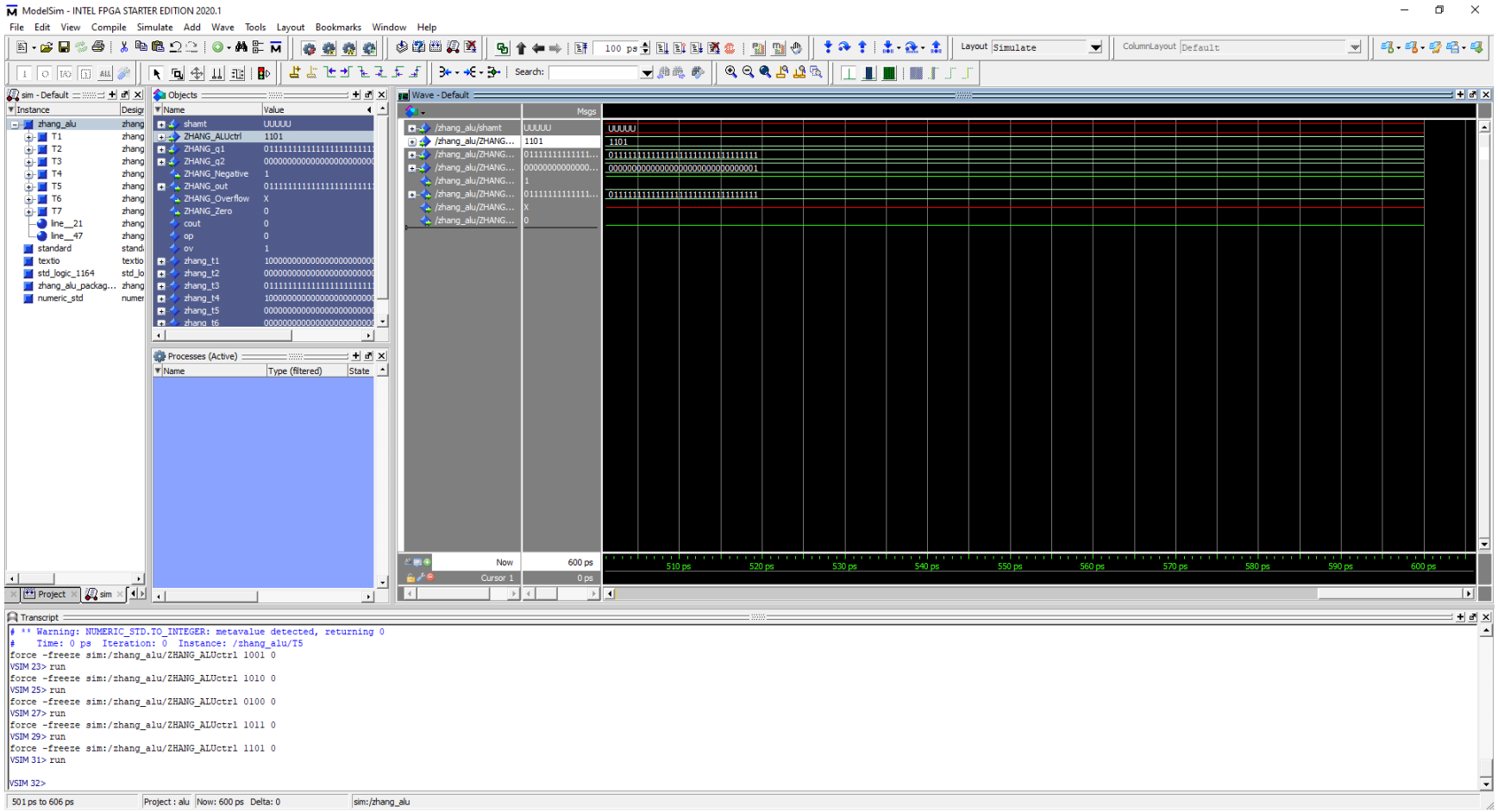

Opcode = 1010, 7FFF FFFF addiu 0000 0001, Output = 8000 0000 with no overflow. Addi performed on operand 1 and imm16 with sign extension without overflow flag.



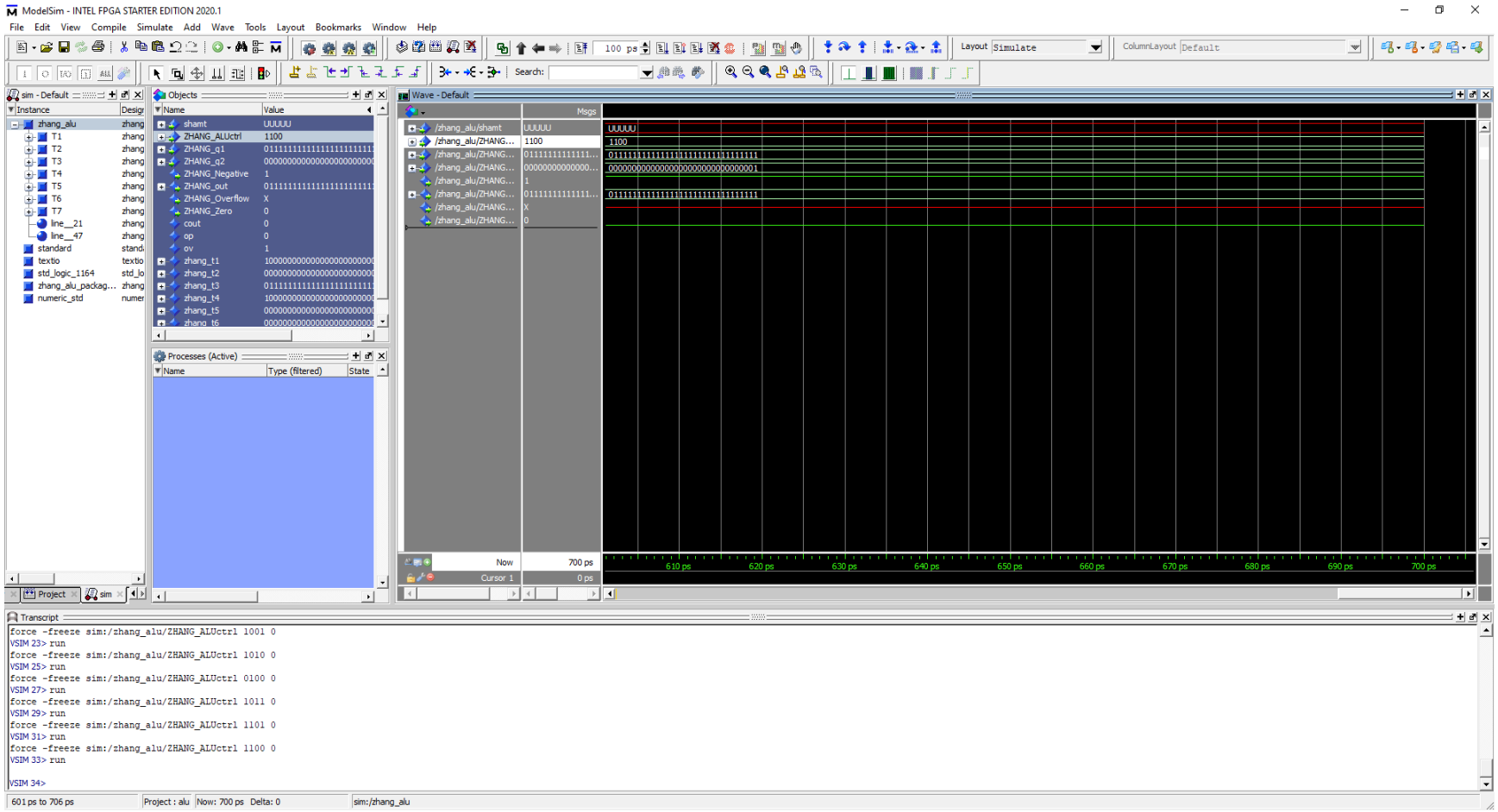

Opcode = 0001, 7FFF FFFF – 0000 0001 = 7FFF FFFE, All flags shown. Sub performed on operands with overflow flags.



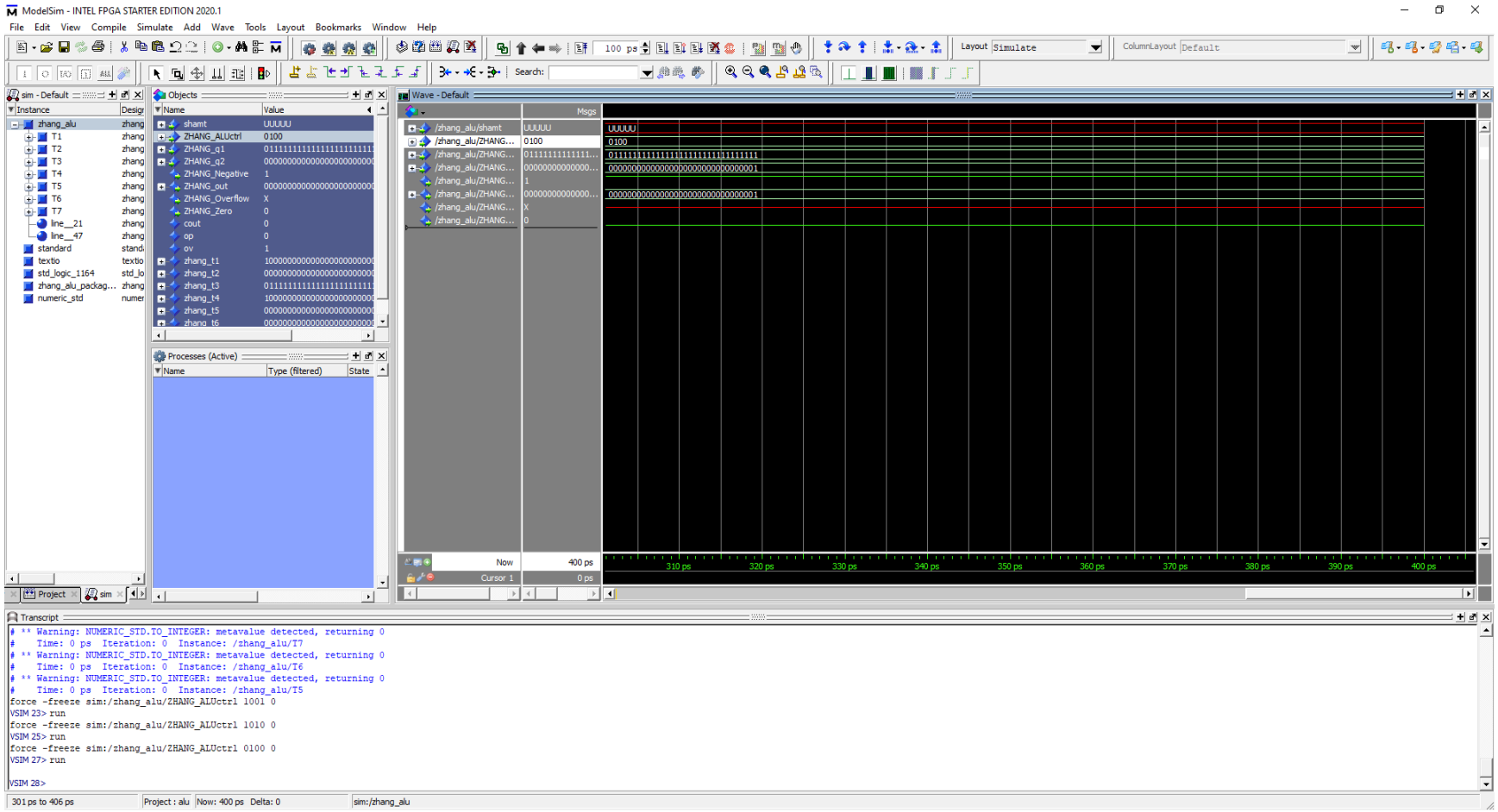

Opcode = 0001, 7FFF FFFF subu 0000 0001 = 7FFF FFFE, no overflow flag shown. Sub Operation performed on both operands without overflow flag



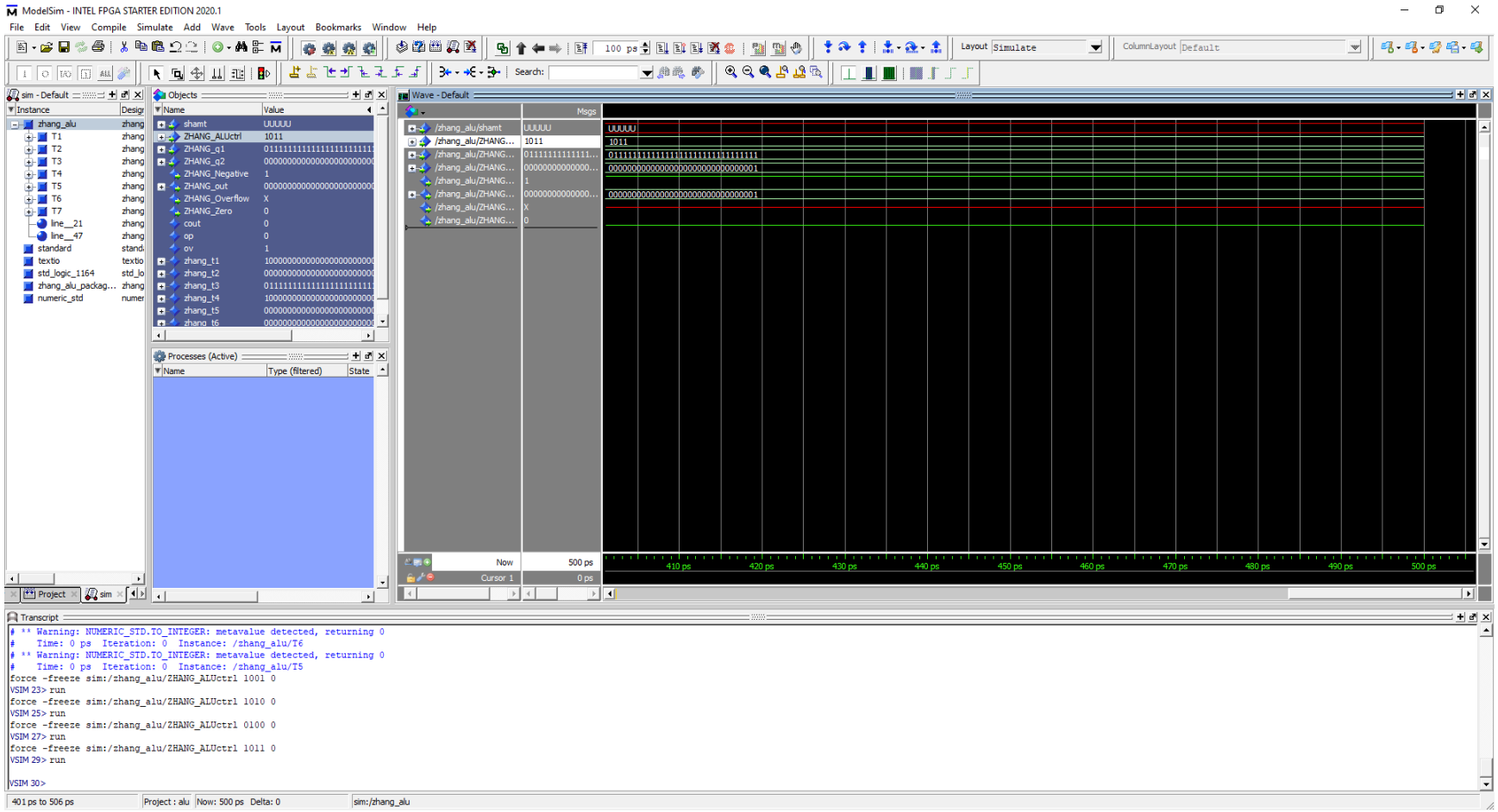

Opcode = 1101, 7FFF FFFF or 0000 0001 = 7FFF FFFF. Or operation performed on both operands.



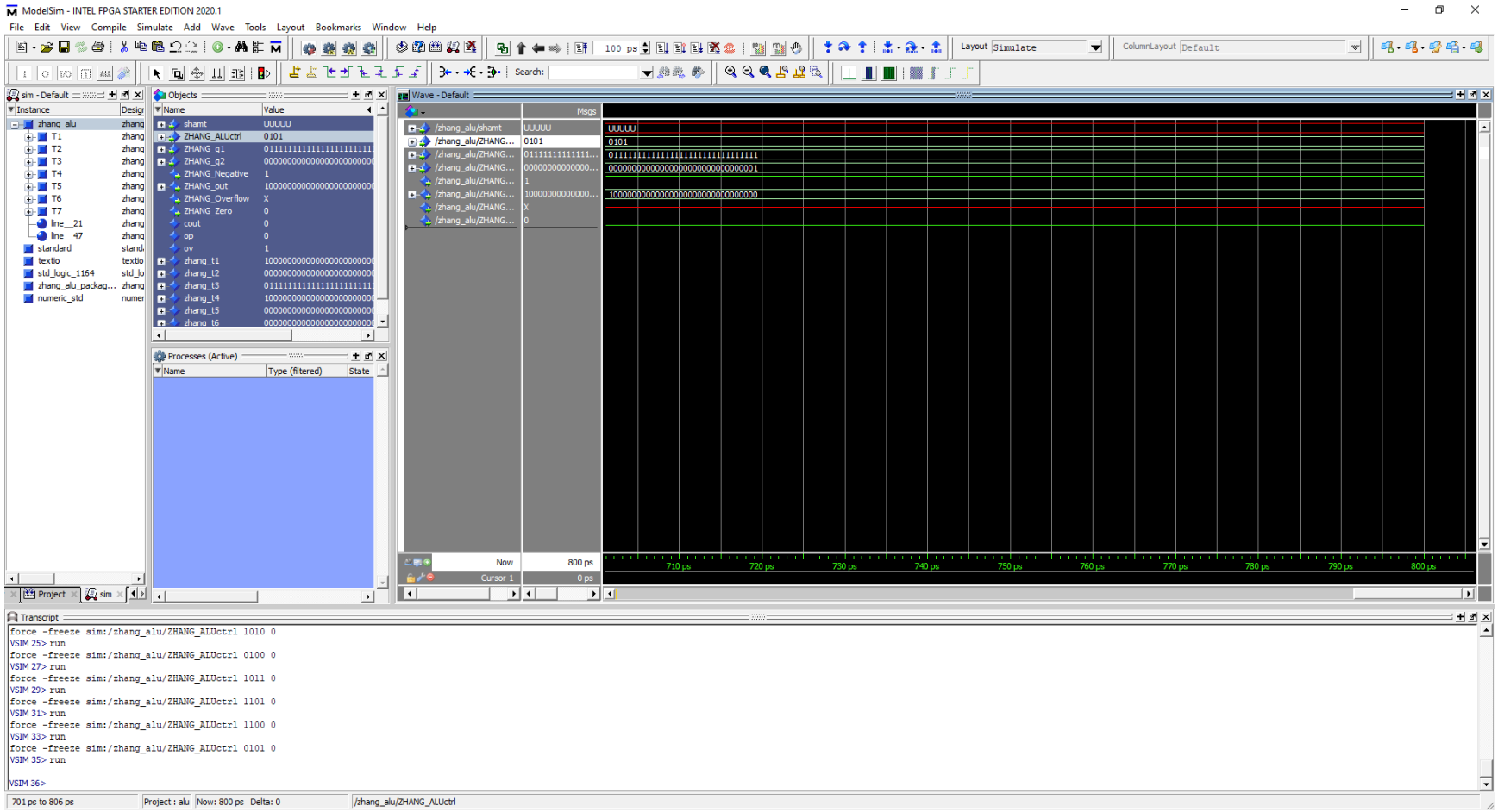

Opcode = 1100, 7FFF FFFF ori 0000 0001 = 7FFF FFFF. Or immediate operation performed on operand1 and imm16 bit with zero extension



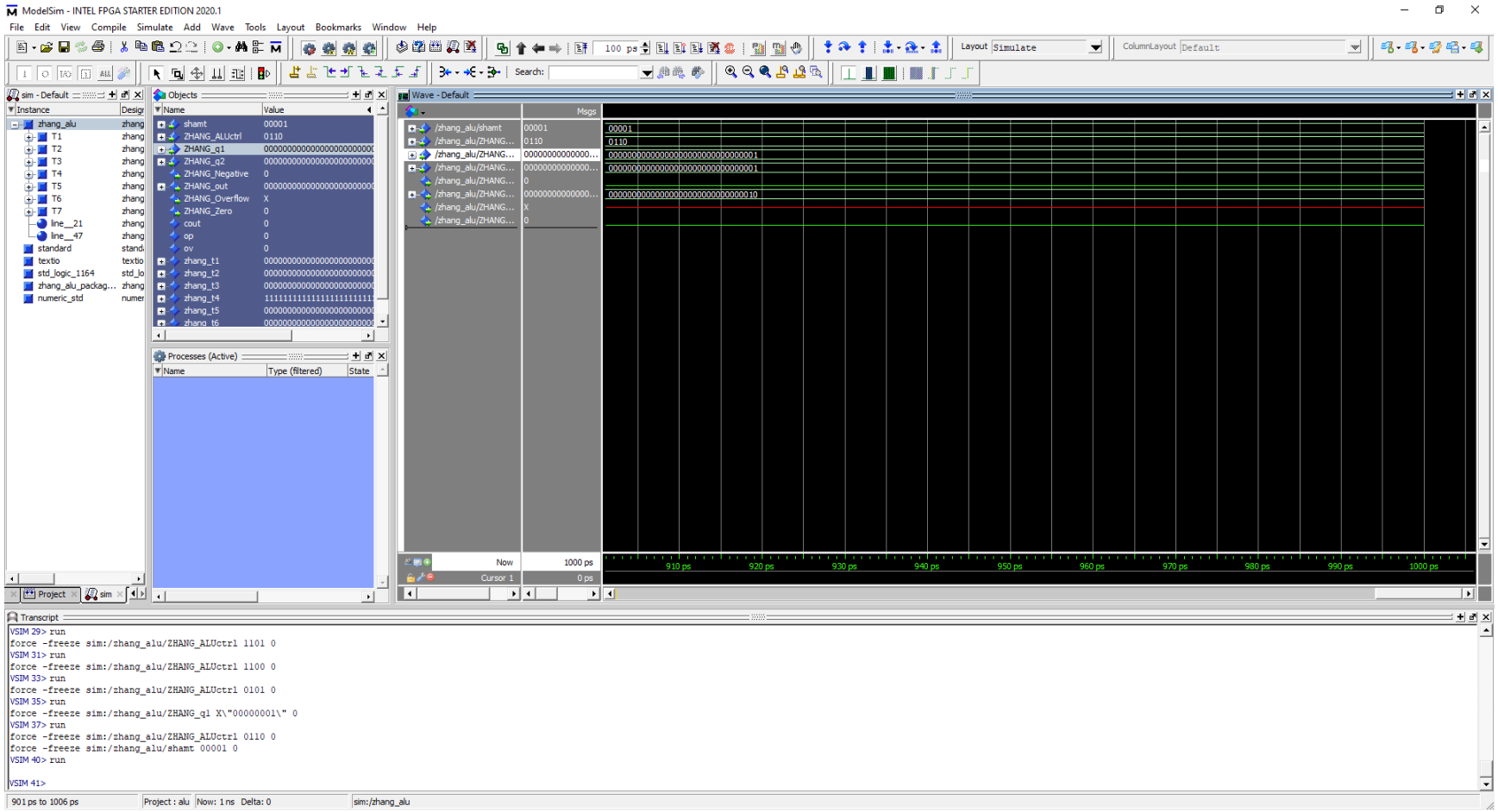

Opcode = 0100, 7FFF FFFF and 0000 0001 = 0000 0001 . And operation performed on both operands.



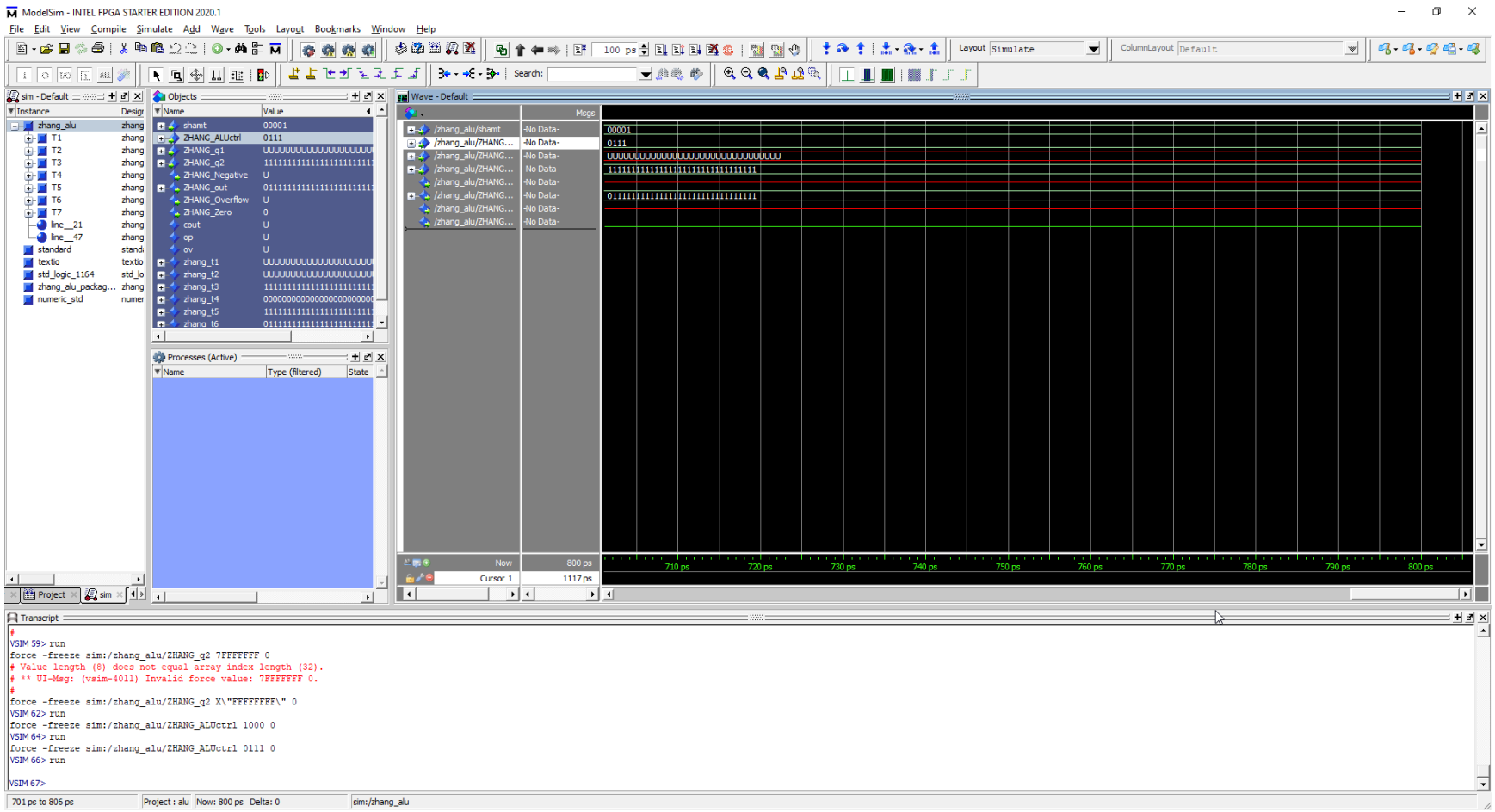

Opcode = 1011, 7FFF FFFF andi 0000 0001. And operation performed with operand 1 and imm16 with zero sign extension



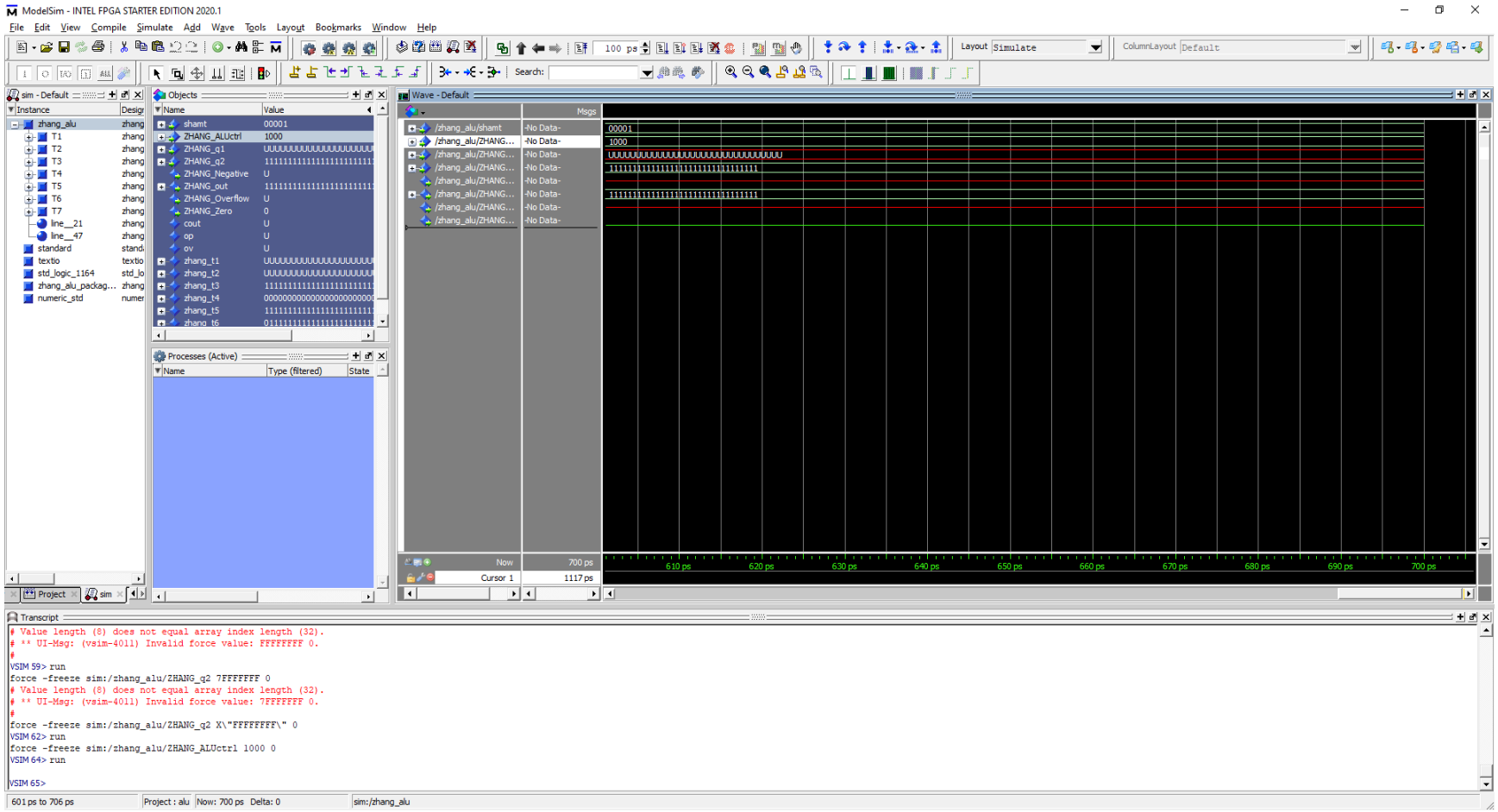

Opcode = 0101, 7FFF FFFF nor 0000 0001 = 8000 0000, NOR operation performed on operand 1 and operand 2




Opcode = 0110, Shamt = 00001, input = 0000 0001, Output = 0000 0010. Shift left operation performed on operand 2 with shift amount of 00001.




Opcode = 0111, shamt = 00001, Input = 1111 1111, Output = 0111 1111. Shift right operand performed on Operand 2 with shift amount of 1 giving us 0111 1111.




Opcode = 1000, shamt = 00001, input = 1111 1111, output = 1111 1111. Shift right Arithmetic performed on operand 2. Unlike Shift right, 0's don't replace right most bit.