Tutorial Lab : Memory Blocks

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Csc343 Fall 2021

Professor Gertner

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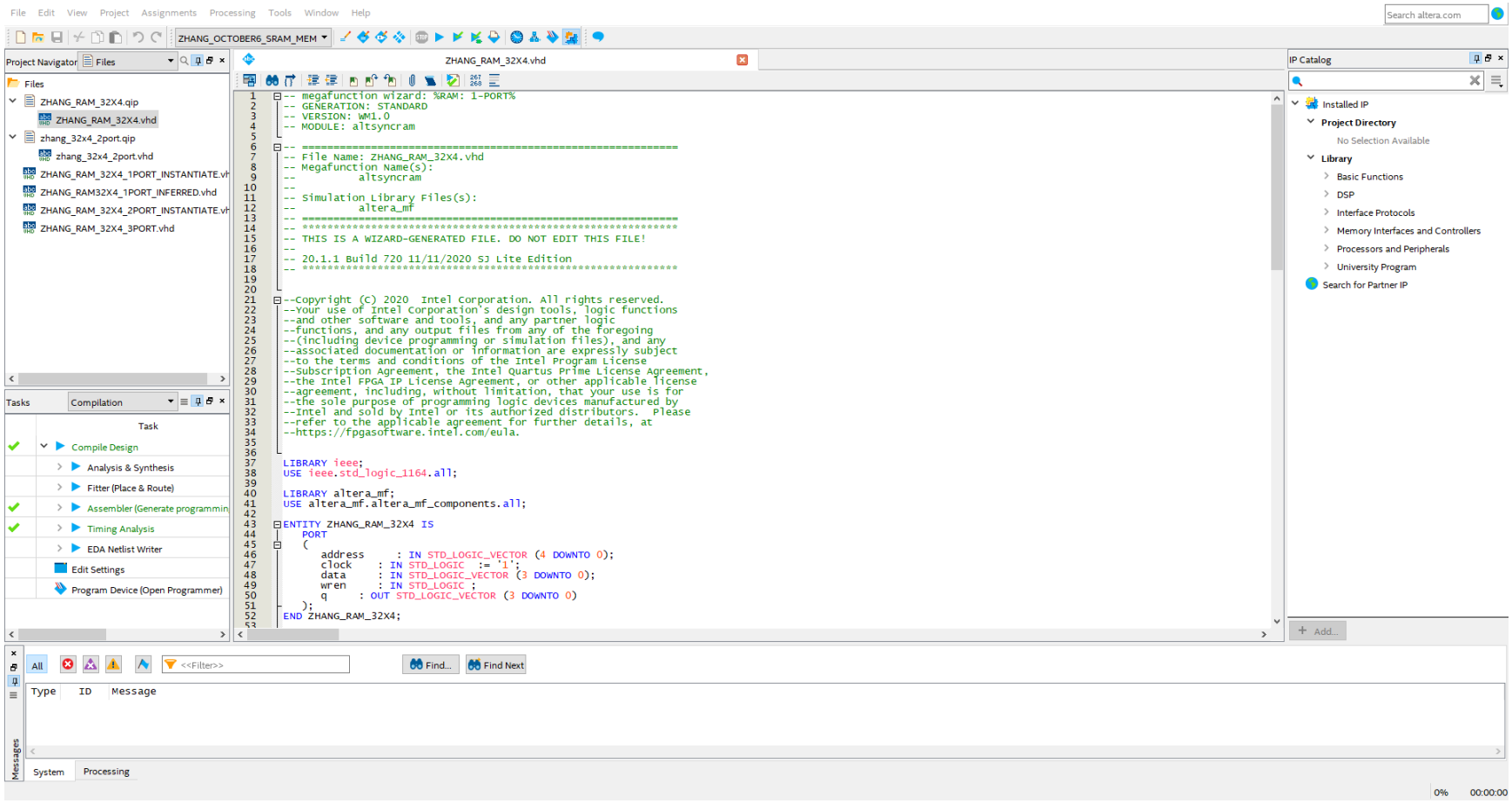
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-- megafunction wizard: %RAM: 1-PORT%
-- GENERATION: STANDARD
-- VERSION: WM1.0
-- MODULE: altsyncram
-- File Name: ZHANG_RAM_32X4.vhd
-- Megafunction Name(s):
-- altsyncram
-- Simulation Library Files(s):
-- altera_mf
-- THIS IS A WIZARD-GENERATED FILE. DO NOT EDIT THIS FILE!
-- 20.1.1 Build 720 11/11/2020 SJ Lite Edition
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--Your use of Intel Corporation's design tools, logic functions
--and other software and tools, and any partner logic
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--the sole purpose of programming logic devices manufactured by
--Intel and sold by Intel or its authorized distributors. Please
--refer to the applicable agreement for further details, at
--https://fpgasoftware.intel.com/eula.
LIBRARY ieee;
USE ieee.std_logic_1164.all;
LIBRARY altera_mf;
USE altera_mf.altera_mf_components.all;
ENTITY ZHANG_RAM_32X4 IS
PORT
(
address : IN STD_LOGIC_VECTOR (4 DOWNTO 0);
clock : IN STD_LOGIC := '1';
data : IN STD_LOGIC_VECTOR (3 DOWNTO 0);
wren : IN STD_LOGIC ;
q : OUT STD_LOGIC_VECTOR (3 DOWNTO 0)
);
END ZHANG_RAM_32X4;
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Search for Partner IP
Add...
All
<<Filter>>
Find...
Find Next
Type ID Message
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0%
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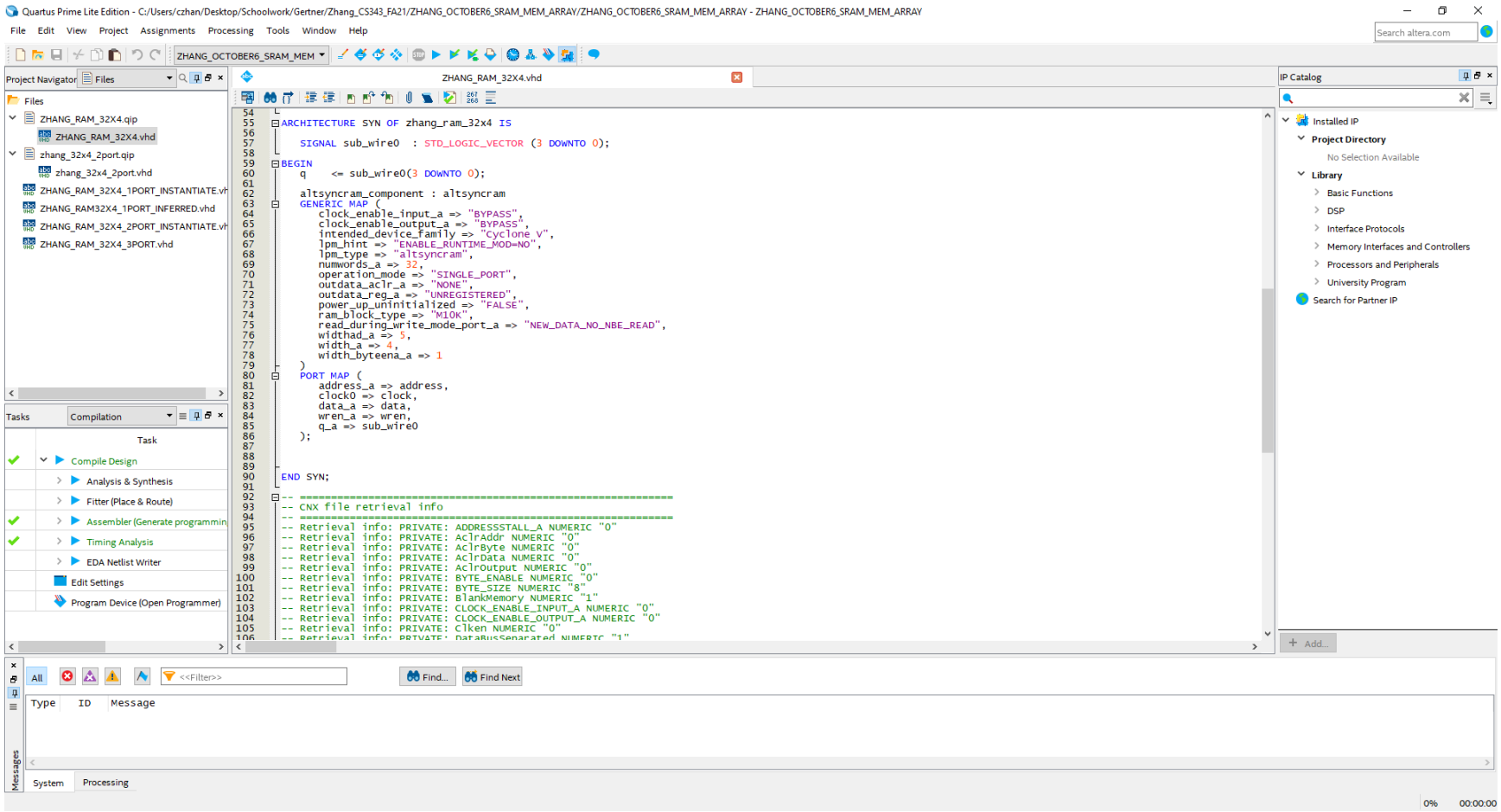
Quartus Prime Lite Edition - C:/Users/czhan/Desktop/Schoolwork/Gertner/Zhang_CS343_FA21/ZHANG_OCTOBER6_SRAM_MEM_ARRAY/ZHANG_OCTOBER6_SRAM_MEM_ARRAY - ZHANG_OCTOBER6_SRAM_MEM_ARRAY
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ZHANG_RAM_32X4.vhd
ARCHITECTURE SYN OF zhang_ram_32x4 IS
SIGNAL sub_wire0 : STD_LOGIC_VECTOR (3 DOWNTO 0);
BEGIN
q <= sub_wire0(3 DOWNTO 0);
altsyncram_component : altsyncram
GENERIC MAP (
clock_enable_input_a => "BYPASS",
clock_enable_output_a => "BYPASS",
intended_device_family => "Cyclone V",
lpm_hint => "ENABLE_RUNTIME_MOD=NO",
lpm_type => "altsyncram",
numwords_a => 32,
operation_mode => "SINGLE_PORT",
outdata_aclr_a => "NONE",
outdata_reg_a => "UNREGISTERED",
power_up_uninitialized => "FALSE",
ram_block_type => "M10K",
read_during_write_mode_port_a => "NEW_DATA_NO_NBE_READ",
widthad_a => 5,
width_a => 4,
width_byteena_a => 1
)
PORT MAP (
address_a => address,
clock0 => clock,
data_a => data,
wren_a => wren,
q_a => sub_wire0
);
END SYN;
-- CNX file retrieval info
-- Retrieval info: PRIVATE: ADDRESSSTALL_A NUMERIC "0"
-- Retrieval info: PRIVATE: AclrAddr NUMERIC "0"
-- Retrieval info: PRIVATE: AclrByte NUMERIC "0"
-- Retrieval info: PRIVATE: AclrData NUMERIC "0"
-- Retrieval info: PRIVATE: AclrOutput NUMERIC "0"
-- Retrieval info: PRIVATE: BYTE_ENABLE NUMERIC "0"
-- Retrieval info: PRIVATE: BYTE_SIZE NUMERIC "8"
-- Retrieval info: PRIVATE: BlankMemory NUMERIC "1"
-- Retrieval info: PRIVATE: CLOCK_ENABLE_INPUT_A NUMERIC "0"
-- Retrieval info: PRIVATE: CLOCK_ENABLE_OUTPUT_A NUMERIC "0"
-- Retrieval info: PRIVATE: Clken NUMERIC "0"
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Add...
All
<<Filter>>
Find...
Find Next
Type ID Message
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0%
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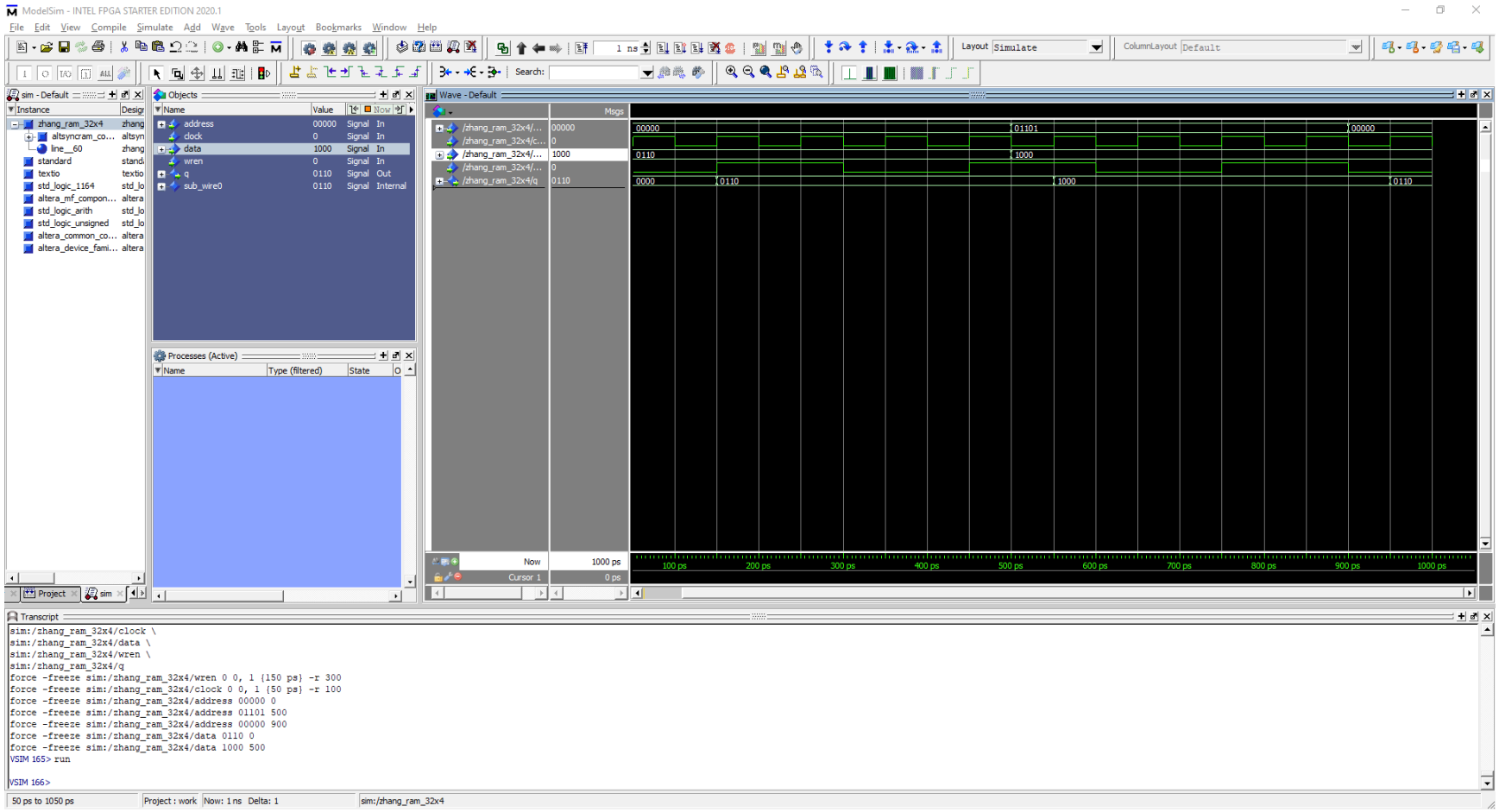
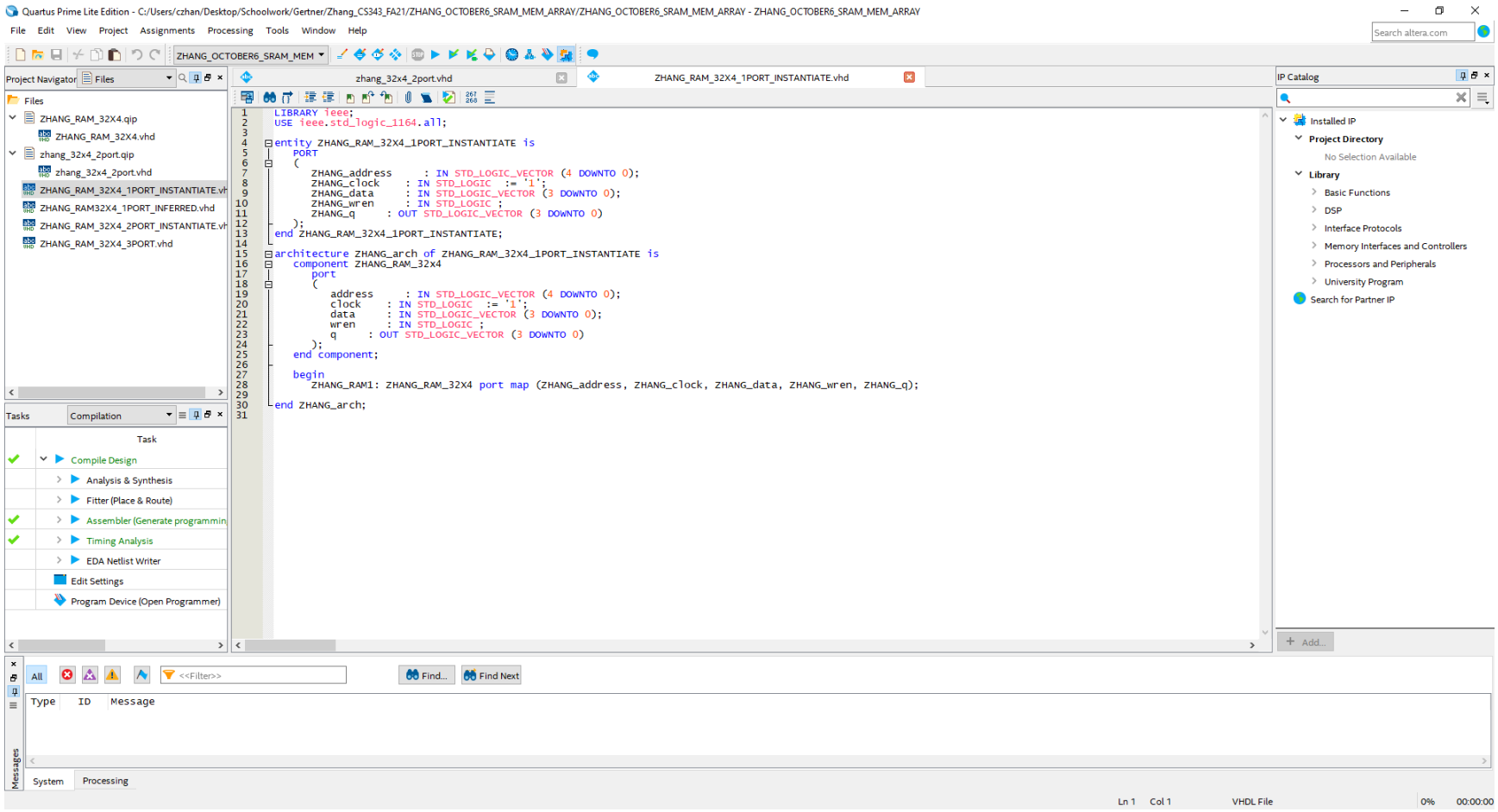


Modelsim testing outputs of the 1 port LPM generated with address of 00000 at 0ps, 01101 at 500ps, 00000 at 900ps.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ZHANG_RAM_32X4_3PORT.vhd
zhang_32x4_2port.vhd
ZHANG_RAM_32X4_1PORT_INSTANTIATE.vhd
1 LIBRARY ieee;
2 USE ieee.std_logic_1164.all;
3
4 entity ZHANG_RAM_32X4_1PORT_INSTANTIATE is
5 PORT
6 (
7 ZHANG_address : IN STD_LOGIC_VECTOR (4 DOWNTO 0);
8 ZHANG_clock : IN STD_LOGIC := '1';
9 ZHANG_data : IN STD_LOGIC_VECTOR (3 DOWNTO 0);
10 ZHANG_wren : IN STD_LOGIC ;
11 ZHANG_q : OUT STD_LOGIC_VECTOR (3 DOWNTO 0)
12);
13 end ZHANG_RAM_32X4_1PORT_INSTANTIATE;
14
15 architecture ZHANG_arch of ZHANG_RAM_32X4_1PORT_INSTANTIATE is
16 component ZHANG_RAM_32x4
17 port
18 (
19 address : IN STD_LOGIC_VECTOR (4 DOWNTO 0);
20 clock : IN STD_LOGIC := '1';
21 data : IN STD_LOGIC_VECTOR (3 DOWNTO 0);
22 wren : IN STD_LOGIC ;
23 q : OUT STD_LOGIC_VECTOR (3 DOWNTO 0)
24);
25 end component;
26
27 begin
28 ZHANG_RAM1: ZHANG_RAM_32X4 port map (ZHANG_address, ZHANG_clock, ZHANG_data, ZHANG_wren, ZHANG_q);
29
30 end ZHANG_arch;
31
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Find Next
Type ID Message
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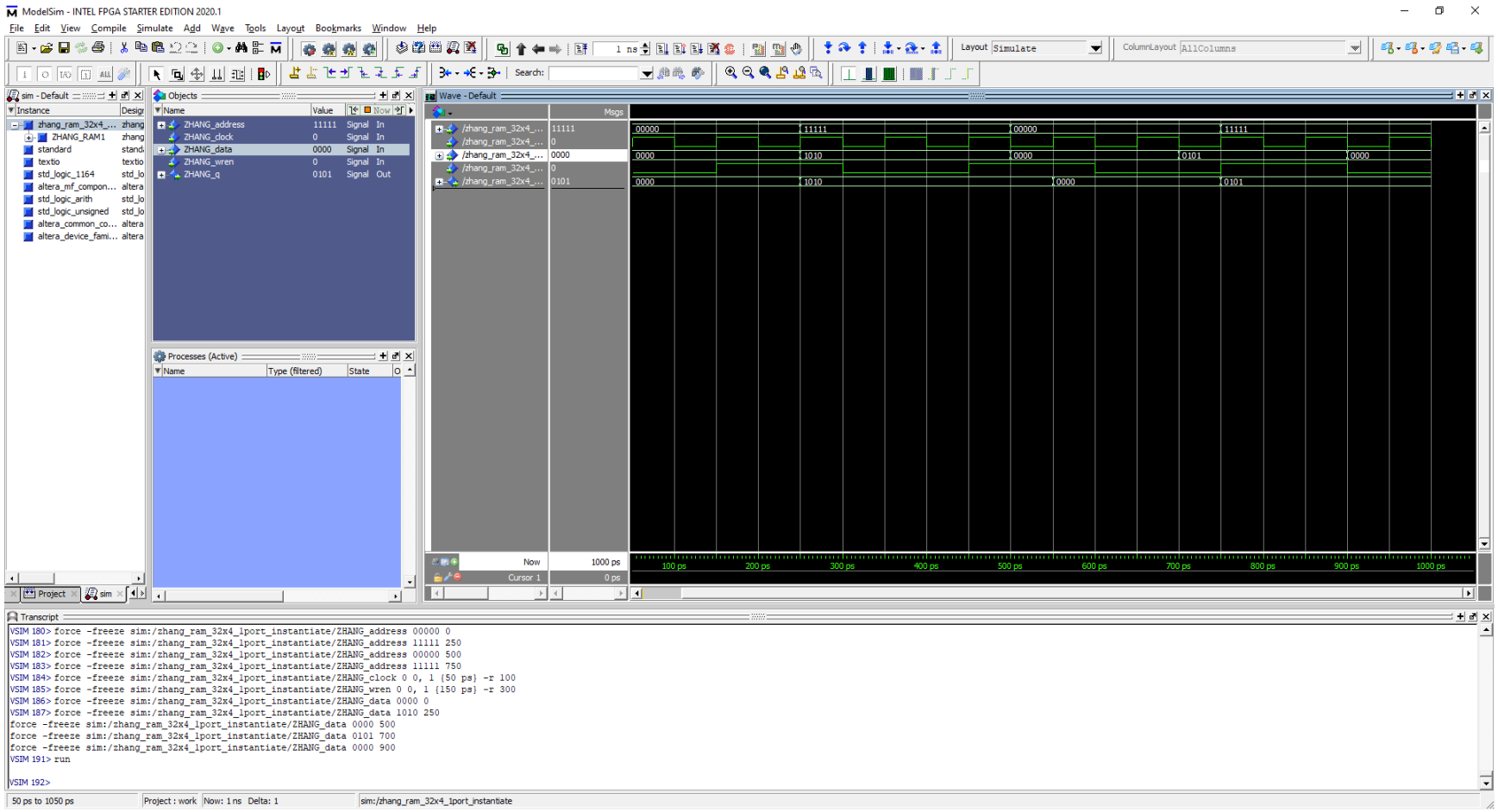
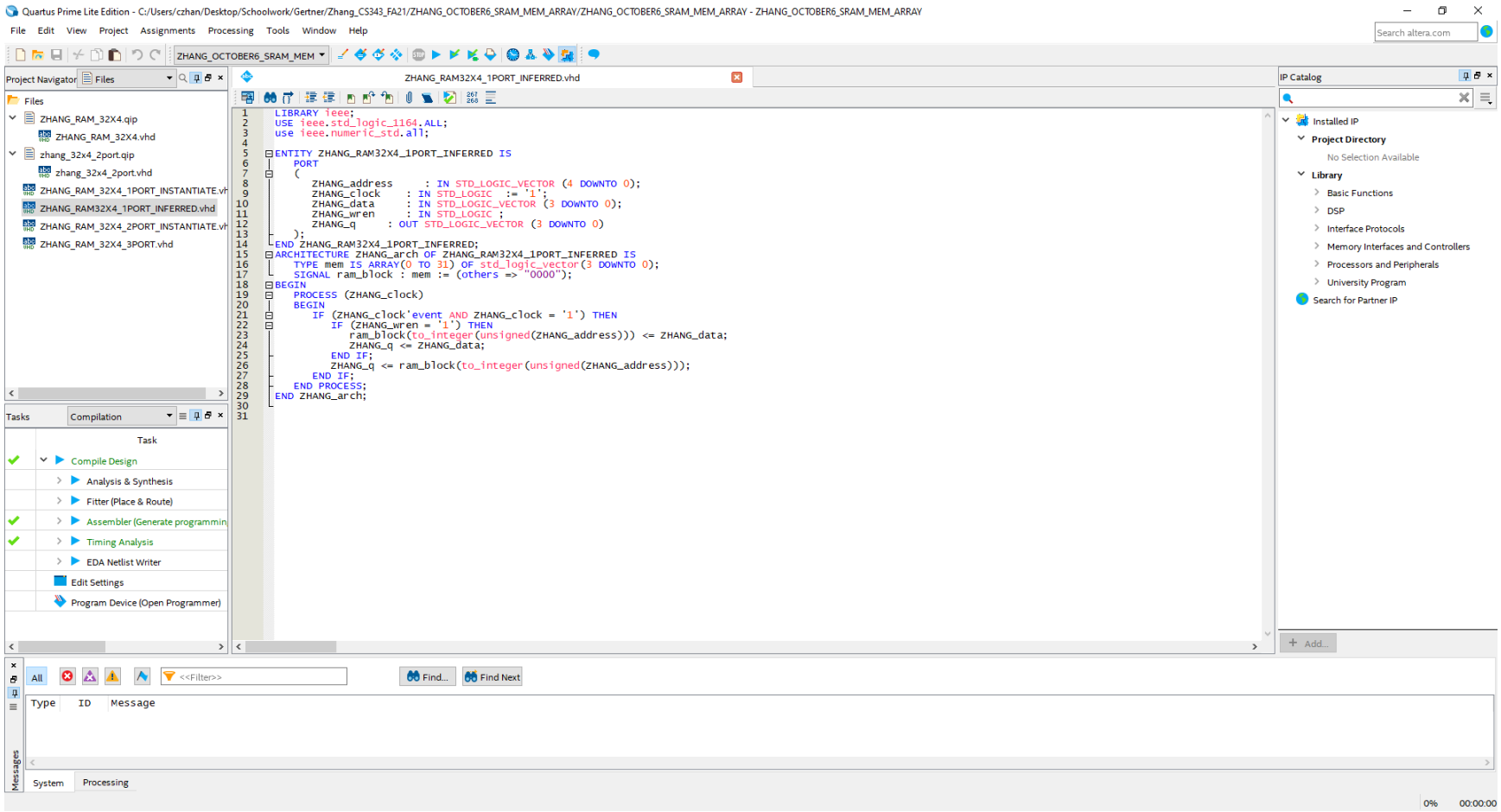
Ln 1 Col 1 VHDL File 0% 00:00:00



Testing with the same inputs as before and comparing, no differences and no errors.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ZHANG_RAM32X4_1PORT_INFERRED.vhd
1 LIBRARY ieee;
2 USE ieee.std_logic_1164.ALL;
3 use ieee.numeric_std.all;
4
5 ENTITY ZHANG_RAM32X4_1PORT_INFERRED IS
6 PORT
7 (
8 ZHANG_address : IN STD_LOGIC_VECTOR (4 DOWNTO 0);
9 ZHANG_clock : IN STD_LOGIC := '1';
10 ZHANG_data : IN STD_LOGIC_VECTOR (3 DOWNTO 0);
11 ZHANG_wren : IN STD_LOGIC ;
12 ZHANG_q : OUT STD_LOGIC_VECTOR (3 DOWNTO 0)
13);
14 END ZHANG_RAM32X4_1PORT_INFERRED;
15 ARCHITECTURE ZHANG_arch OF ZHANG_RAM32X4_1PORT_INFERRED IS
16 TYPE mem IS ARRAY(0 TO 31) OF std_logic_vector(3 DOWNTO 0);
17 SIGNAL ram_block : mem := (others => "0000");
18 BEGIN
19 PROCESS (ZHANG_clock)
20 BEGIN
21 IF (ZHANG_clock'event AND ZHANG_clock = '1') THEN
22 IF (ZHANG_wren = '1') THEN
23 ram_block(to_integer(unsigned(ZHANG_address))) <= ZHANG_data;
24 ZHANG_q <= ZHANG_data;
25 END IF;
26 ZHANG_q <= ram_block(to_integer(unsigned(ZHANG_address)));
27 END IF;
28 END PROCESS;
29 END ZHANG_arch;
30
31
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University Program
Search for Partner IP
Add...
All
<<Filter>>
Find...
Find Next
Type ID Message
Messages
System
Processing
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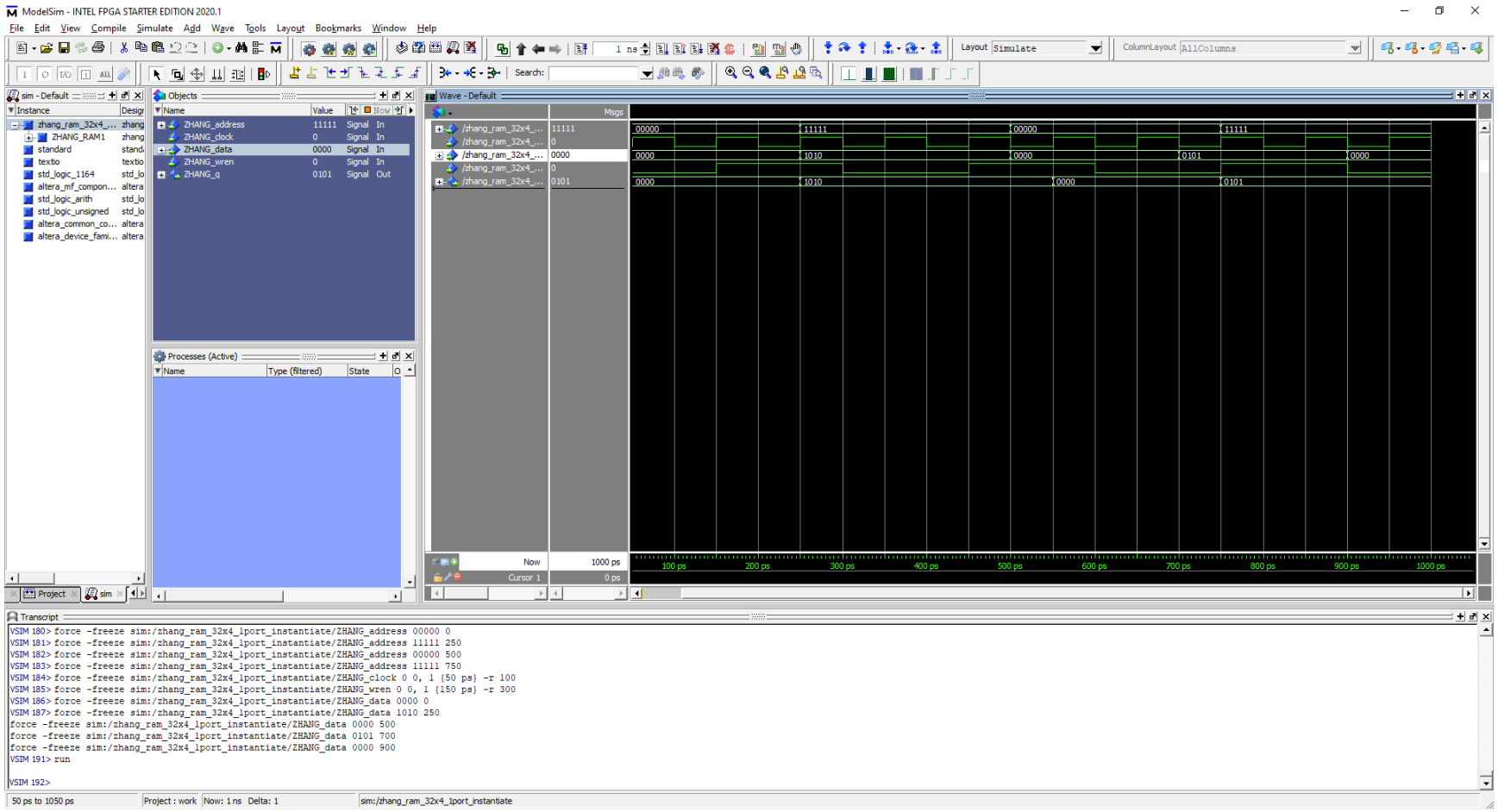
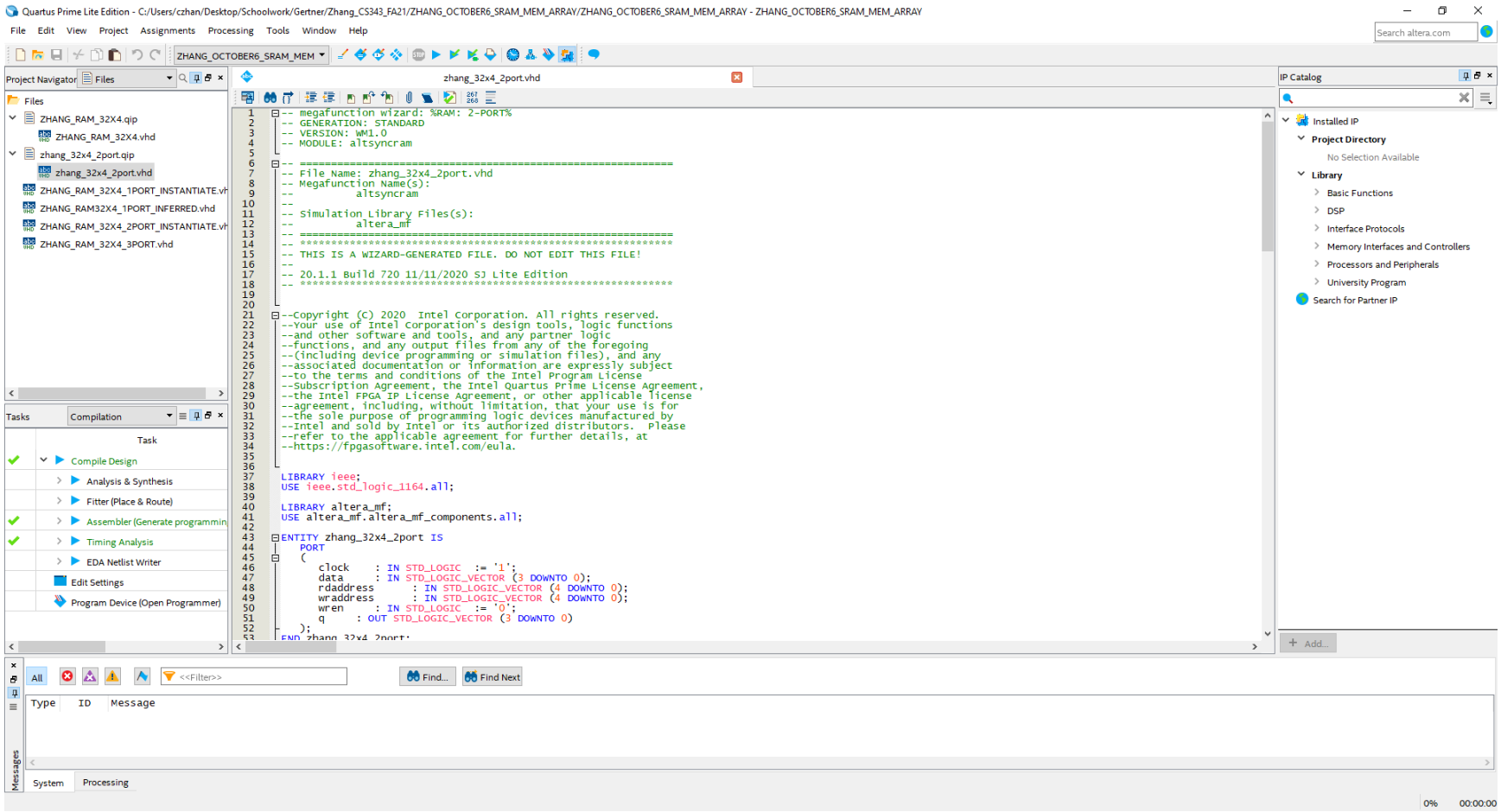


Testing with the same input as before when testing 1 port RAMS, no difference.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ZHANG_RAM32X4_1PORT_INFERRED.vhd
ZHANG_RAM_32X4_2PORT_INSTANTIATE.vh
ZHANG_RAM_32X4_3PORT.vhd
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Program Device (Open Programmer)
zhang_32x4_2port.vhd
-- megafunction wizard: %RAM: 2-PORT%
-- GENERATION: STANDARD
-- VERSION: WM1.0
-- MODULE: altsyncram
-- File Name: zhang_32x4_2port.vhd
-- Megafunction Name(s):
-- altsyncram
-- Simulation Library Files(s):
-- altera_mf
-- THIS IS A WIZARD-GENERATED FILE. DO NOT EDIT THIS FILE!
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--the sole purpose of programming logic devices manufactured by
--Intel and sold by Intel or its authorized distributors. Please
--refer to the applicable agreement for further details, at
--https://fpgasoftware.intel.com/eula.
LIBRARY ieee;
USE ieee.std_logic_1164.all;
LIBRARY altera_mf;
USE altera_mf.altera_mf_components.all;
ENTITY zhang_32x4_2port IS
PORT
(
clock : IN STD_LOGIC := '1';
data : IN STD_LOGIC_VECTOR (3 DOWNTO 0);
rdaddress : IN STD_LOGIC_VECTOR (4 DOWNTO 0);
wraddress : IN STD_LOGIC_VECTOR (4 DOWNTO 0);
wren : IN STD_LOGIC := '0';
q : OUT STD_LOGIC_VECTOR (3 DOWNTO 0)
);
END zhang_32x4_2port;
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Search for Partner IP
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Find...
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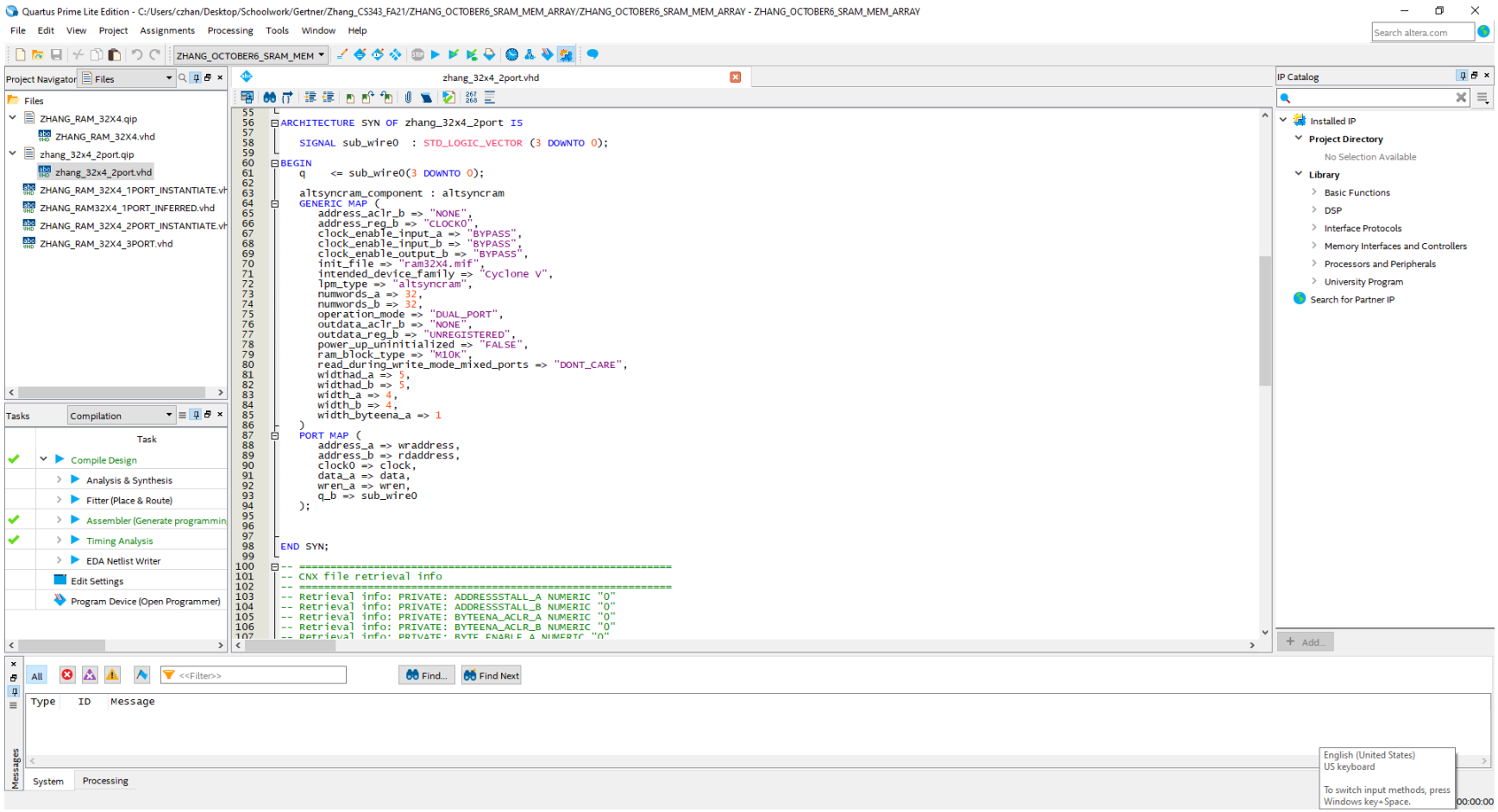
Quartus Prime Lite Edition - C:/Users/czhan/Desktop/Schoolwork/Gertner/Zhang_CS343_FA21/ZHANG_OCTOBER6_SRAM_MEM_ARRAY/ZHANG_OCTOBER6_SRAM_MEM_ARRAY - ZHANG_OCTOBER6_SRAM_MEM_ARRAY
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zhang_32x4_2port.vhd
ARCHITECTURE SYN OF zhang_32x4_2port IS
SIGNAL sub_wire0 : STD_LOGIC_VECTOR (3 DOWNTO 0);
BEGIN
q <= sub_wire0(3 DOWNTO 0);
altsyncram_component : altsyncram
GENERIC MAP (
address_aclr_b => "NONE",
address_reg_b => "CLOCK0",
clock_enable_input_a => "BYPASS",
clock_enable_input_b => "BYPASS",
clock_enable_output_b => "BYPASS",
init_file => "ram32X4.mif",
intended_device_family => "Cyclone V",
lpm_type => "altsyncram",
numwords_a => 32,
numwords_b => 32,
operation_mode => "DUAL_PORT",
outdata_aclr_b => "NONE",
outdata_reg_b => "UNREGISTERED",
power_up_uninitialized => "FALSE",
ram_block_type => "M10K",
read_during_write_mode_mixed_ports => "DONT_CARE",
widthad_a => 5,
widthad_b => 5,
width_a => 4,
width_b => 4,
width_byteena_a => 1
)
PORT MAP (
address_a => wraddress,
address_b => rdaddress,
clock0 => clock,
data_a => data,
wren_a => wren,
q_b => sub_wire0
);
END SYN;
-- ==
-- CNX file retrieval info
-- ==
-- Retrieval info: PRIVATE: ADDRESSSTALL_A NUMERIC "0"
-- Retrieval info: PRIVATE: ADDRESSSTALL_B NUMERIC "0"
-- Retrieval info: PRIVATE: BYTEENA_ACLR_A NUMERIC "0"
-- Retrieval info: PRIVATE: BYTEENA_ACLR_B NUMERIC "0"
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<<Filter>>
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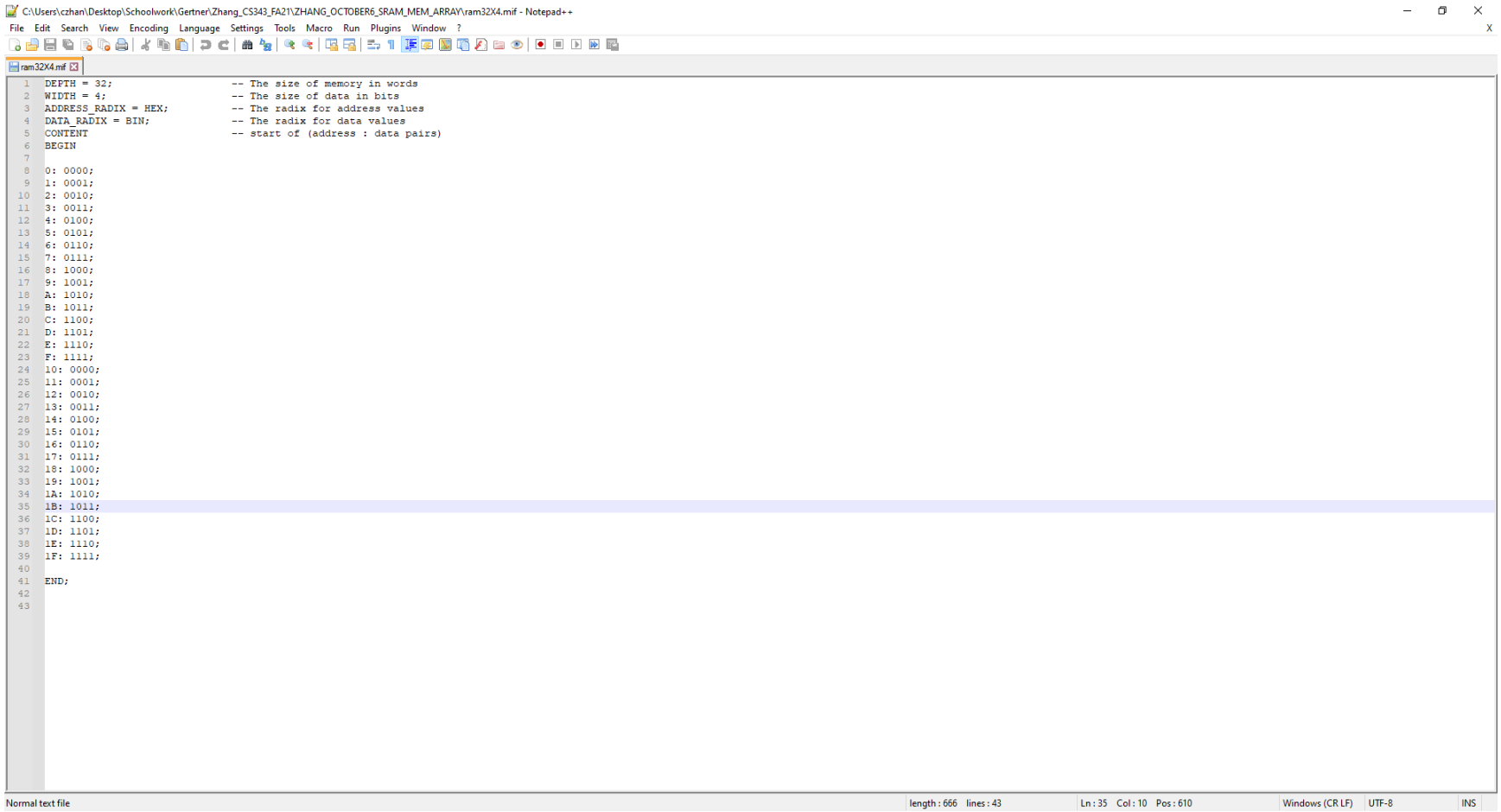
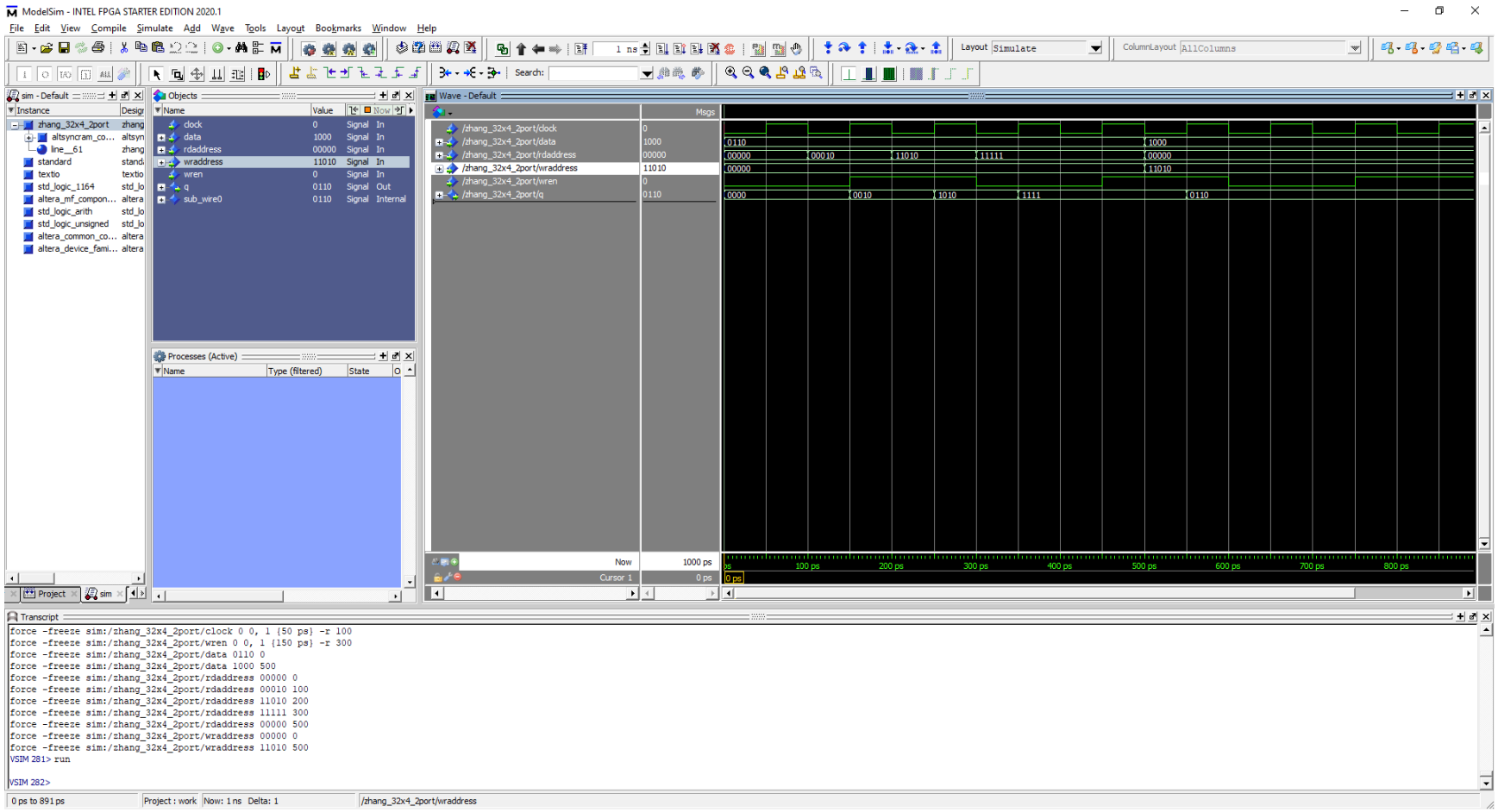
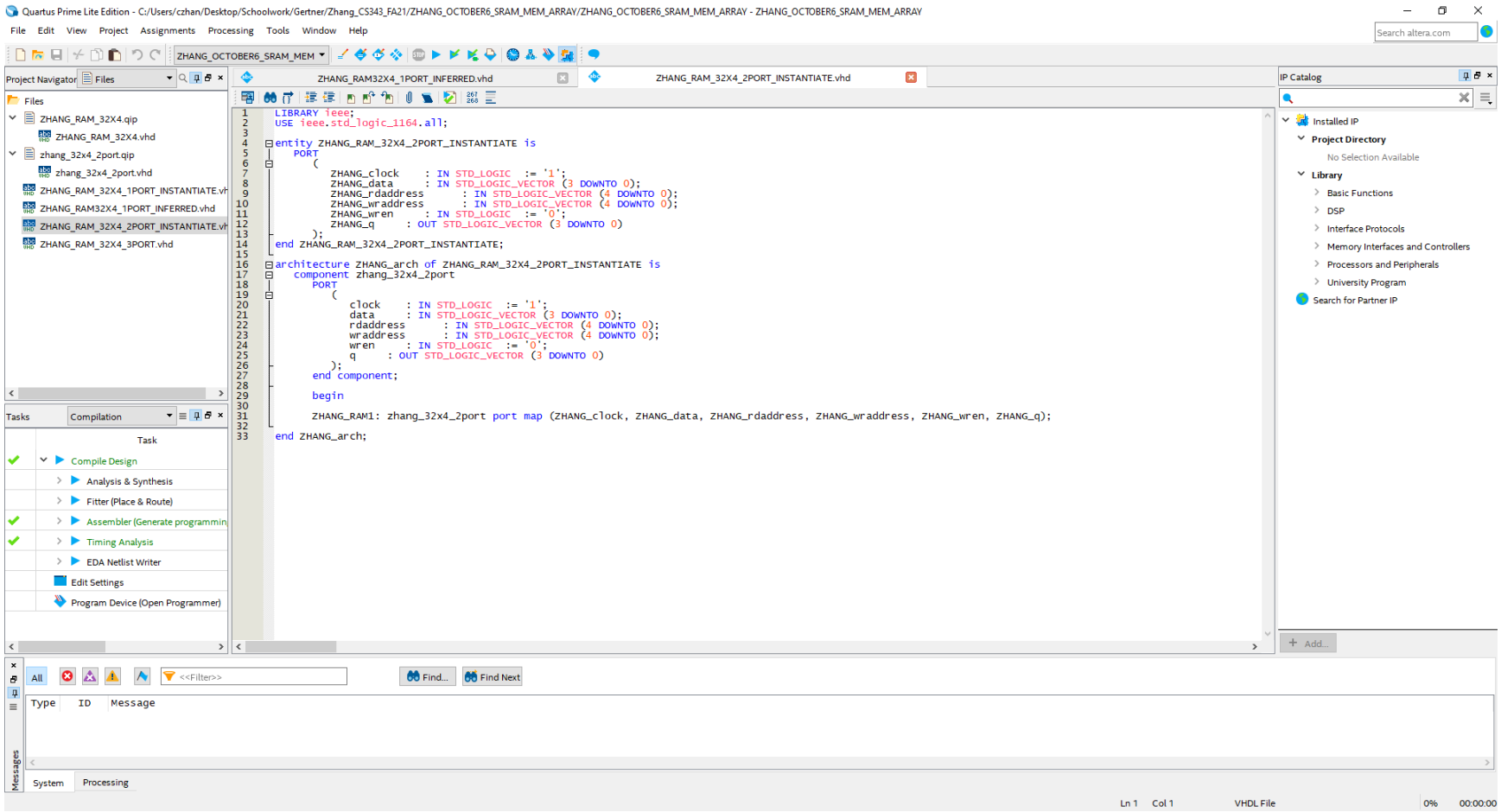
Find Next
Type ID Message
Messages
System
Processing
English (United States)
US keyboard
To switch input methods, press Windows key+Space.
00:00:00


C:\Users\czhan\Desktop\Schoolwork\Gertner\Zhang_CS343_FA21\ZHANG_OCTOBER6_SRAM_MEM_ARRAY\ram32X4.mif - Notepad++
File Edit Search View Encoding Language Settings Tools Macro Run Plugins Window ?
ram32X4.mif
DEPTH = 32; -- The size of memory in words
WIDTH = 4; -- The size of data in bits
ADDRESS_RADIX = HEX; -- The radix for address values
DATA_RADIX = BIN; -- The radix for data values
CONTENT -- start of (address : data pairs)
BEGIN
0: 0000;
1: 0001;
2: 0010;
3: 0011;
4: 0100;
5: 0101;
6: 0110;
7: 0111;
8: 1000;
9: 1001;
A: 1010;
B: 1011;
C: 1100;
D: 1101;
E: 1110;
F: 1111;
10: 0000;
11: 0001;
12: 0010;
13: 0011;
14: 0100;
15: 0101;
16: 0110;
17: 0111;
18: 1000;
19: 1001;
1A: 1010;
1B: 1011;
1C: 1100;
1D: 1101;
1E: 1110;
1F: 1111;
END;
Normal text file
length : 666 lines : 43
Ln : 35 Col : 10 Pos : 610
Windows (CR LF)
UTF-8
INS



2 port LPM generated file and testing with a clock on block wren and clock. No errors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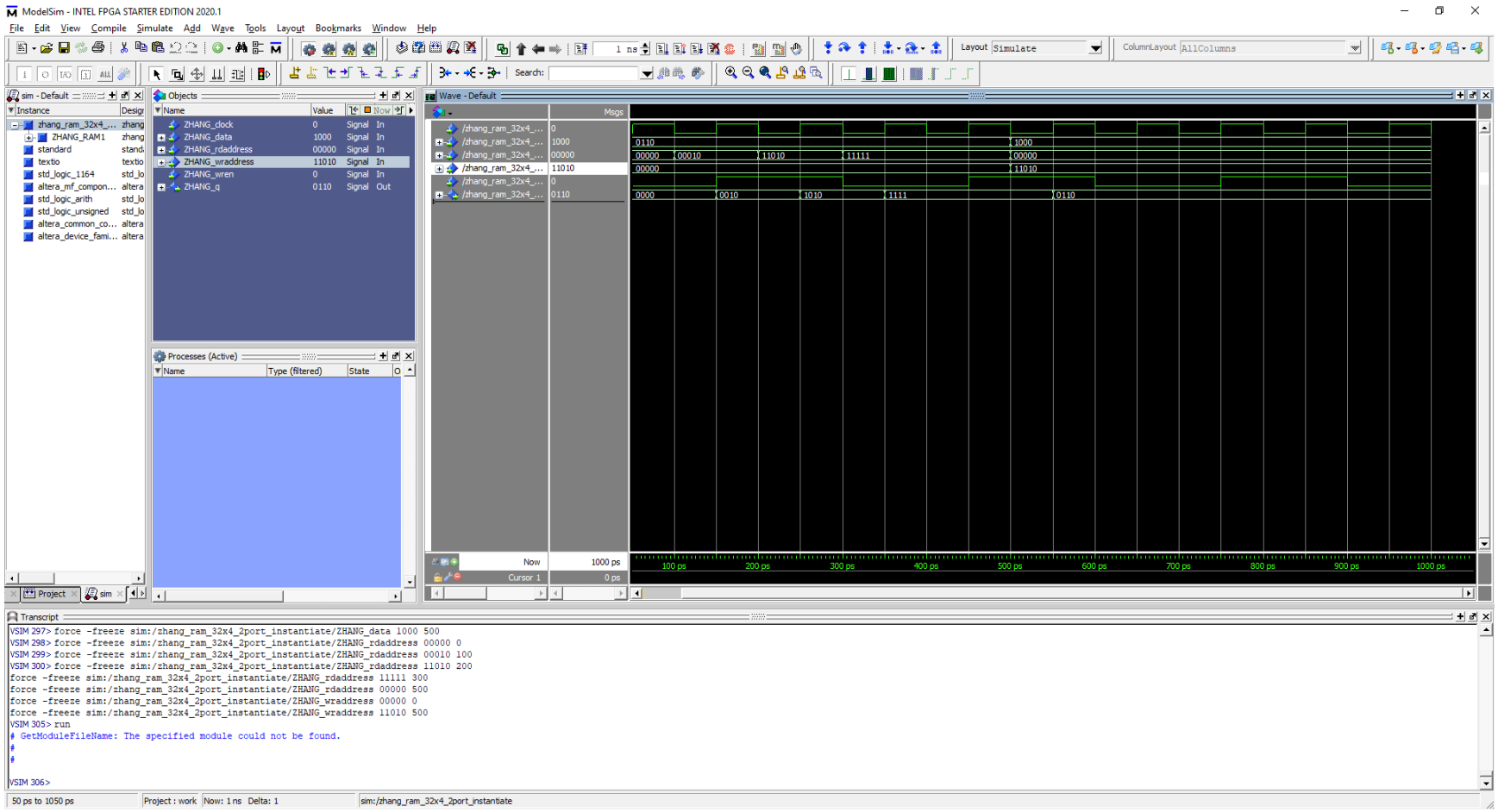
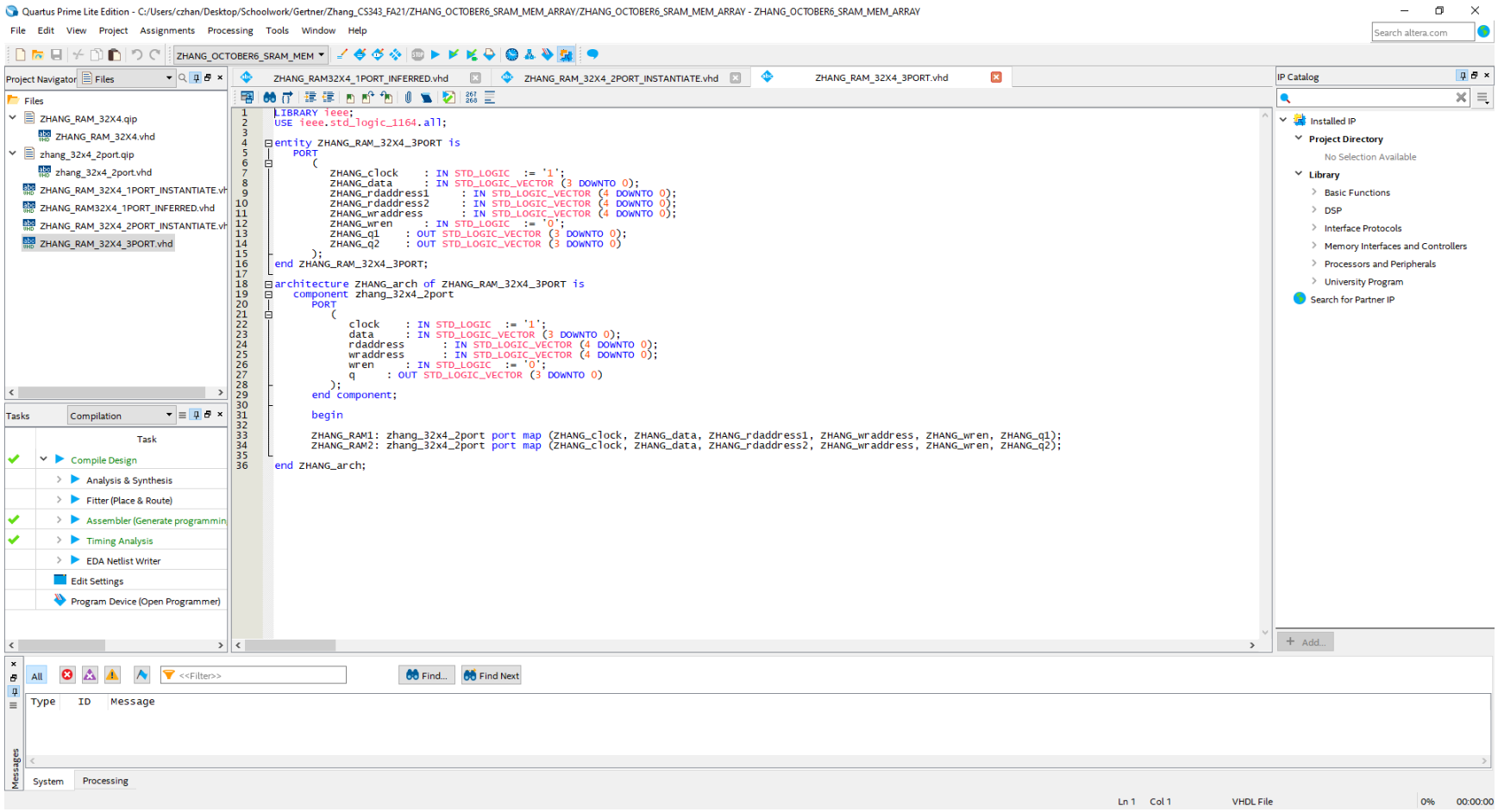
ZHANG_RAM32X4_1PORT_INFERRED.vhd
ZHANG_RAM_32X4_2PORT_INSTANTIATE.vhd
1 LIBRARY ieee;
2 USE ieee.std_logic_1164.all;
3
4 entity ZHANG_RAM_32X4_2PORT_INSTANTIATE is
5 PORT
6 (
7 ZHANG_clock : IN STD_LOGIC := '1';
8 ZHANG_data : IN STD_LOGIC_VECTOR (3 DOWNTO 0);
9 ZHANG_rdaddress : IN STD_LOGIC_VECTOR (4 DOWNTO 0);
10 ZHANG_wraddress : IN STD_LOGIC_VECTOR (4 DOWNTO 0);
11 ZHANG_wren : IN STD_LOGIC := '0';
12 ZHANG_q : OUT STD_LOGIC_VECTOR (3 DOWNTO 0)
13);
14 end ZHANG_RAM_32X4_2PORT_INSTANTIATE;
15
16 architecture ZHANG_arch of ZHANG_RAM_32X4_2PORT_INSTANTIATE is
17 component zhang_32x4_2port
18 PORT
19 (
20 clock : IN STD_LOGIC := '1';
21 data : IN STD_LOGIC_VECTOR (3 DOWNTO 0);
22 rdaddress : IN STD_LOGIC_VECTOR (4 DOWNTO 0);
23 wraddress : IN STD_LOGIC_VECTOR (4 DOWNTO 0);
24 wren : IN STD_LOGIC := '0';
25 q : OUT STD_LOGIC_VECTOR (3 DOWNTO 0)
26);
27 end component;
28
29 begin
30
31 ZHANG_RAM1: zhang_32x4_2port port map (ZHANG_clock, ZHANG_data, ZHANG_rdaddress, ZHANG_wraddress, ZHANG_wren, ZHANG_q);
32
33 end ZHANG_arch;
IP Catalog
Installed IP
Project Directory
No Selection Available
Library
Basic Functions
DSP
Interface Protocols
Memory Interfaces and Controllers
Processors and Peripherals
University Program
Search for Partner IP
Tasks
Compilation
Task
Compile Design
Analysis & Synthesis
Fitter (Place & Route)
Assembler (Generate programmin
Timing Analysis
EDA Netlist Writer
Edit Settings
Program Device (Open Programmer)
Type ID Message
System Processing
Ln 1 Col 1 VHDL File 0% 00:00:00



Testing using instantiated 2 port Ram with the same test inputs with no errors and no differences.


Quartus Prime Lite Edition - C:/Users/czhan/Desktop/Schoolwork/Gertner/Zhang_CS343_FA21/ZHANG_OCTOBER6_SRAM_MEM_ARRAY/ZHANG_OCTOBER6_SRAM_MEM_ARRAY - ZHANG_OCTOBER6_SRAM_MEM_ARRAY
File Edit View Project Assignments Processing Tools Window Help
ZHANG_OCTOBER6_SRAM_MEM
Project Navigator
Files
ZHANG_RAM_32X4.qip
ZHANG_RAM_32X4.vhd
zhang_32x4_2port.qip
zhang_32x4_2port.vhd
ZHANG_RAM_32X4_1PORT_INSTANTIATE.vh
ZHANG_RAM32X4_1PORT_INFERRED.vhd
ZHANG_RAM_32X4_2PORT_INSTANTIATE.vh
ZHANG_RAM_32X4_3PORT.vhd
ZHANG_RAM32X4_1PORT_INFERRED.vhd
ZHANG_RAM_32X4_2PORT_INSTANTIATE.vhd
ZHANG_RAM_32X4_3PORT.vhd
1 LIBRARY ieee;
2 USE ieee.std_logic_1164.all;
3
4 entity ZHANG_RAM_32X4_3PORT is
5 PORT
6 (
7 ZHANG_clock : IN STD_LOGIC := '1';
8 ZHANG_data : IN STD_LOGIC_VECTOR (3 DOWNTO 0);
9 ZHANG_rdaddress1 : IN STD_LOGIC_VECTOR (4 DOWNTO 0);
10 ZHANG_rdaddress2 : IN STD_LOGIC_VECTOR (4 DOWNTO 0);
11 ZHANG_wraddress : IN STD_LOGIC_VECTOR (4 DOWNTO 0);
12 ZHANG_wren : IN STD_LOGIC := '0';
13 ZHANG_q1 : OUT STD_LOGIC_VECTOR (3 DOWNTO 0);
14 ZHANG_q2 : OUT STD_LOGIC_VECTOR (3 DOWNTO 0)
15);
16 end ZHANG_RAM_32X4_3PORT;
17
18 architecture ZHANG_arch of ZHANG_RAM_32X4_3PORT is
19 component zhang_32x4_2port
20 PORT
21 (
22 clock : IN STD_LOGIC := '1';
23 data : IN STD_LOGIC_VECTOR (3 DOWNTO 0);
24 rdaddress : IN STD_LOGIC_VECTOR (4 DOWNTO 0);
25 wraddress : IN STD_LOGIC_VECTOR (4 DOWNTO 0);
26 wren : IN STD_LOGIC := '0';
27 q : OUT STD_LOGIC_VECTOR (3 DOWNTO 0)
28);
29 end component;
30
31 begin
32
33 ZHANG_RAM1: zhang_32x4_2port port map (ZHANG_clock, ZHANG_data, ZHANG_rdaddress1, ZHANG_wraddress, ZHANG_wren, ZHANG_q1);
34 ZHANG_RAM2: zhang_32x4_2port port map (ZHANG_clock, ZHANG_data, ZHANG_rdaddress2, ZHANG_wraddress, ZHANG_wren, ZHANG_q2);
35
36 end ZHANG_arch;
IP Catalog
Installed IP
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No Selection Available
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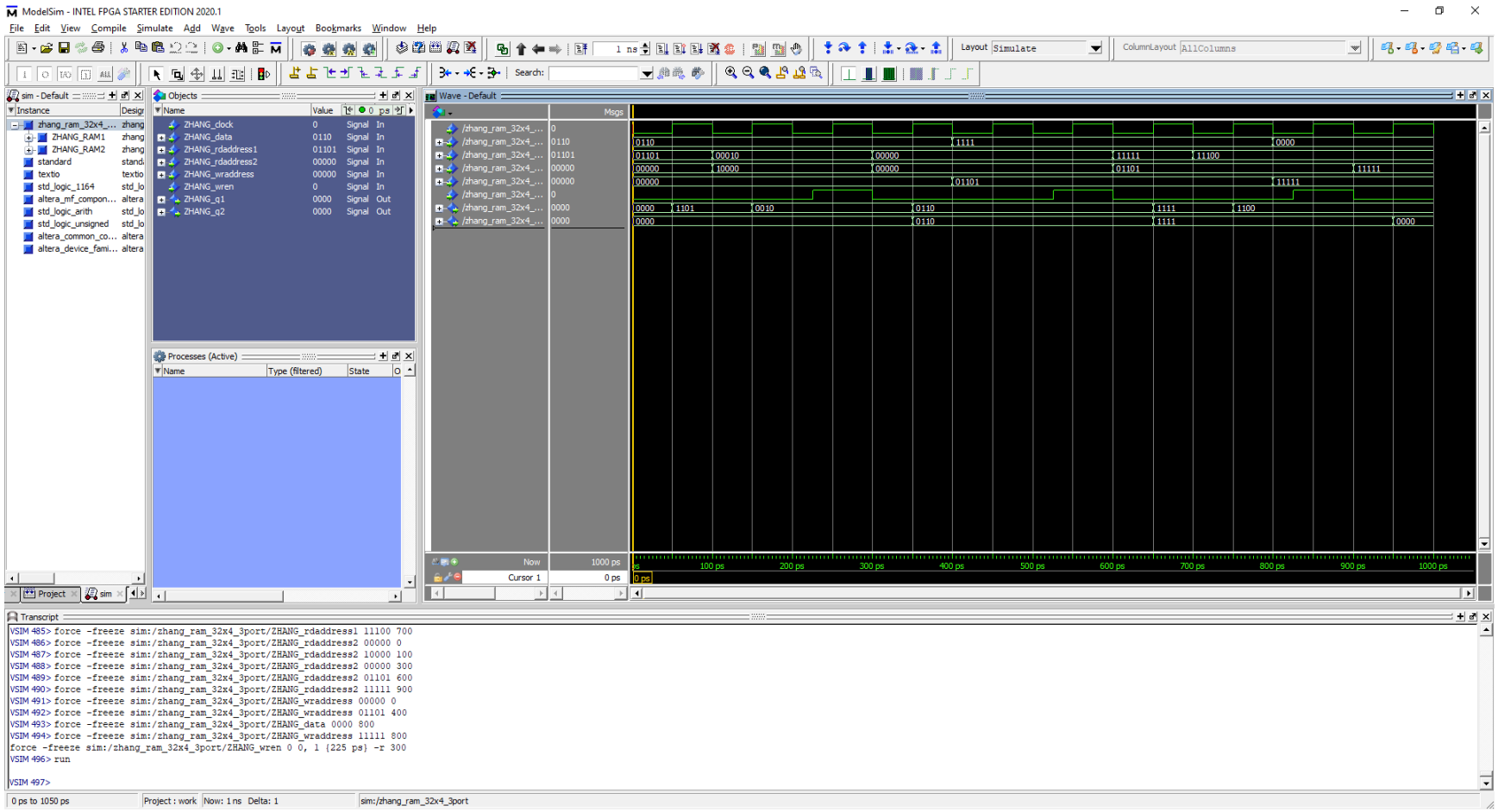
Basic Functions
DSP
Interface Protocols
Memory Interfaces and Controllers
Processors and Peripherals
University Program
Search for Partner IP
Tasks
Compilation
Task
Compile Design
Analysis & Synthesis
Fitter (Place & Route)
Assembler (Generate programmin
Timing Analysis
EDA Netlist Writer
Edit Settings
Program Device (Open Programmer)
Find...
Find Next
Type ID Message
Messages
System
Processing
Ln 1 Col 1 VHDL File 0% 00:00:00



Testing inputs with a 3 port ram which uses 2, 2 port rams. Above showcases two address inputs that needs to be read and one write.