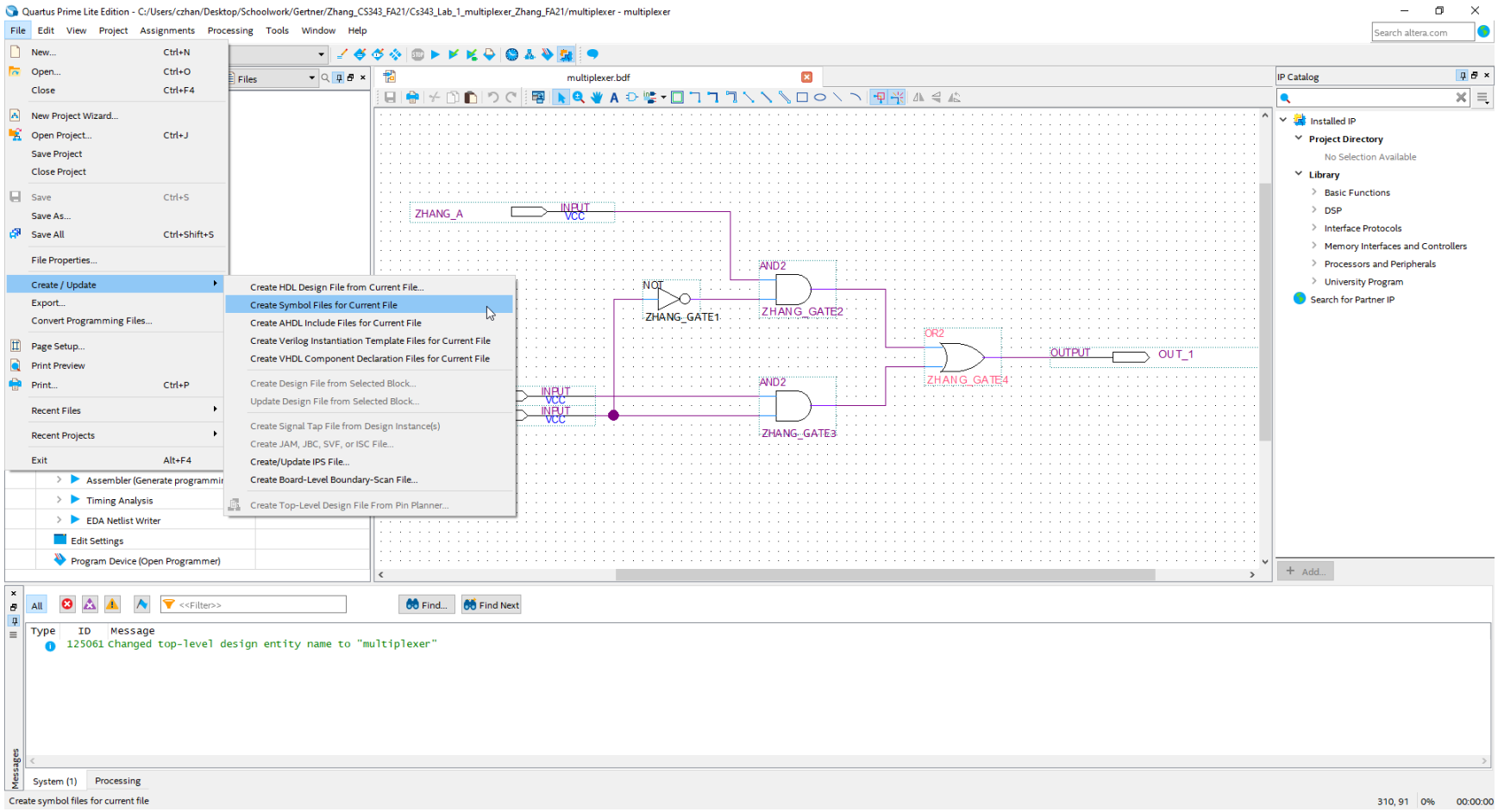
Lab Report : VHDL with LPM

Chue Zhang

Csc343 Fall 2021

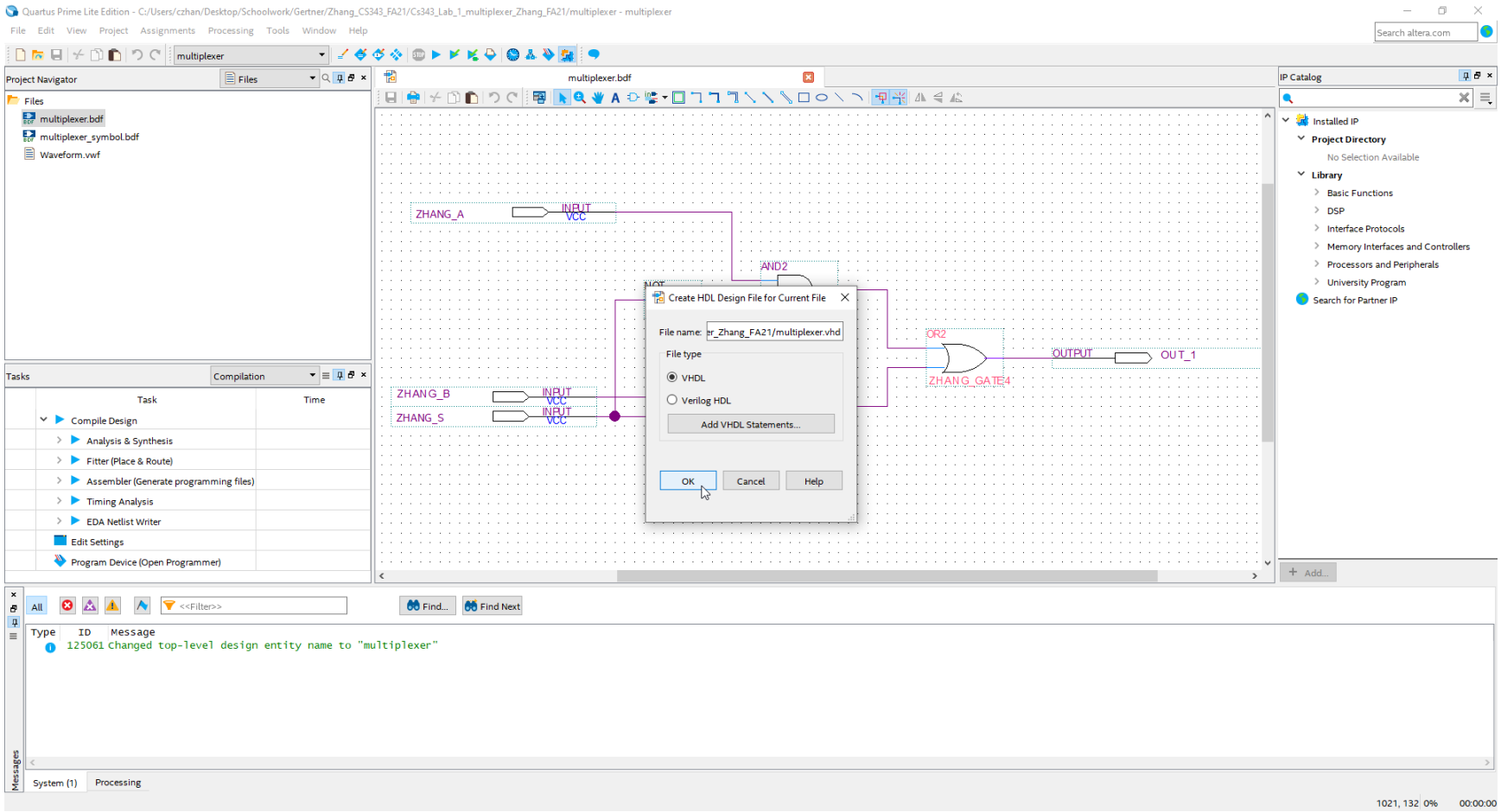
Professor Gertner

Task 1, Chue Zhang



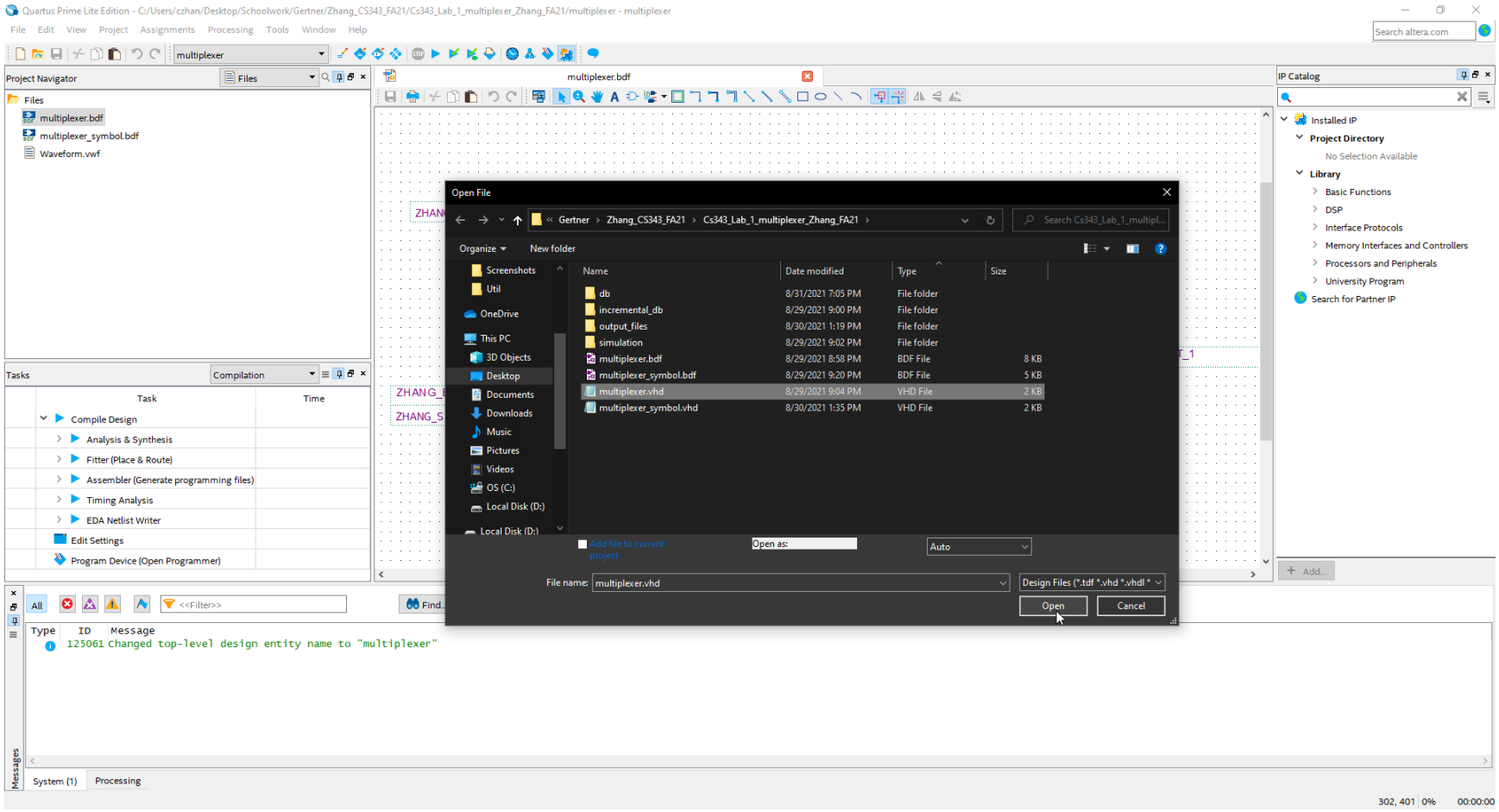
With the 2:1 Mux previously created, I go to the file → create HDL design File for Current File and a popup should show up

Task 1, Chue Zhang



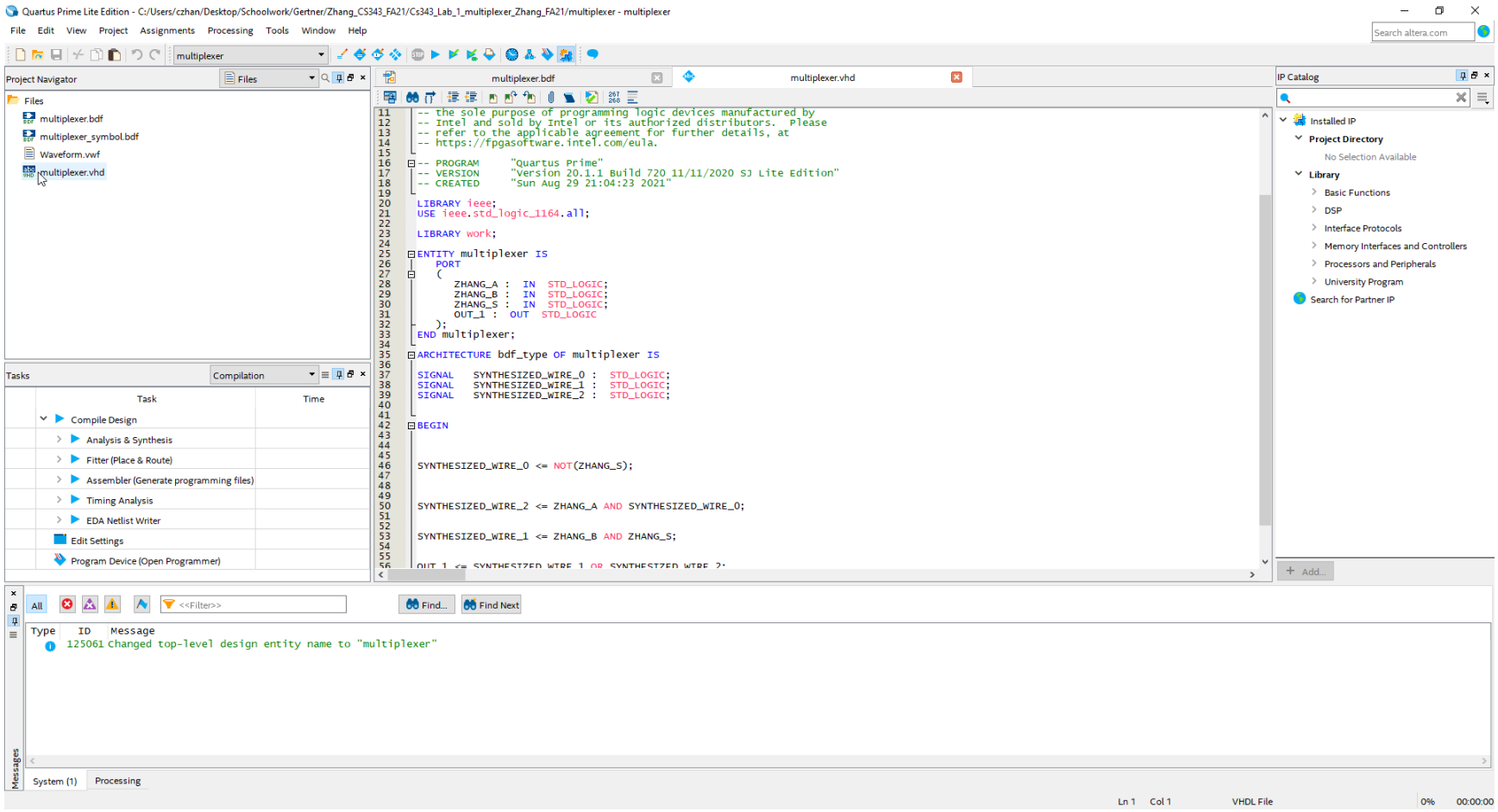
Make sure that the file type is in VHDL not in Verilog and press OK

Task 1, Chue Zhang



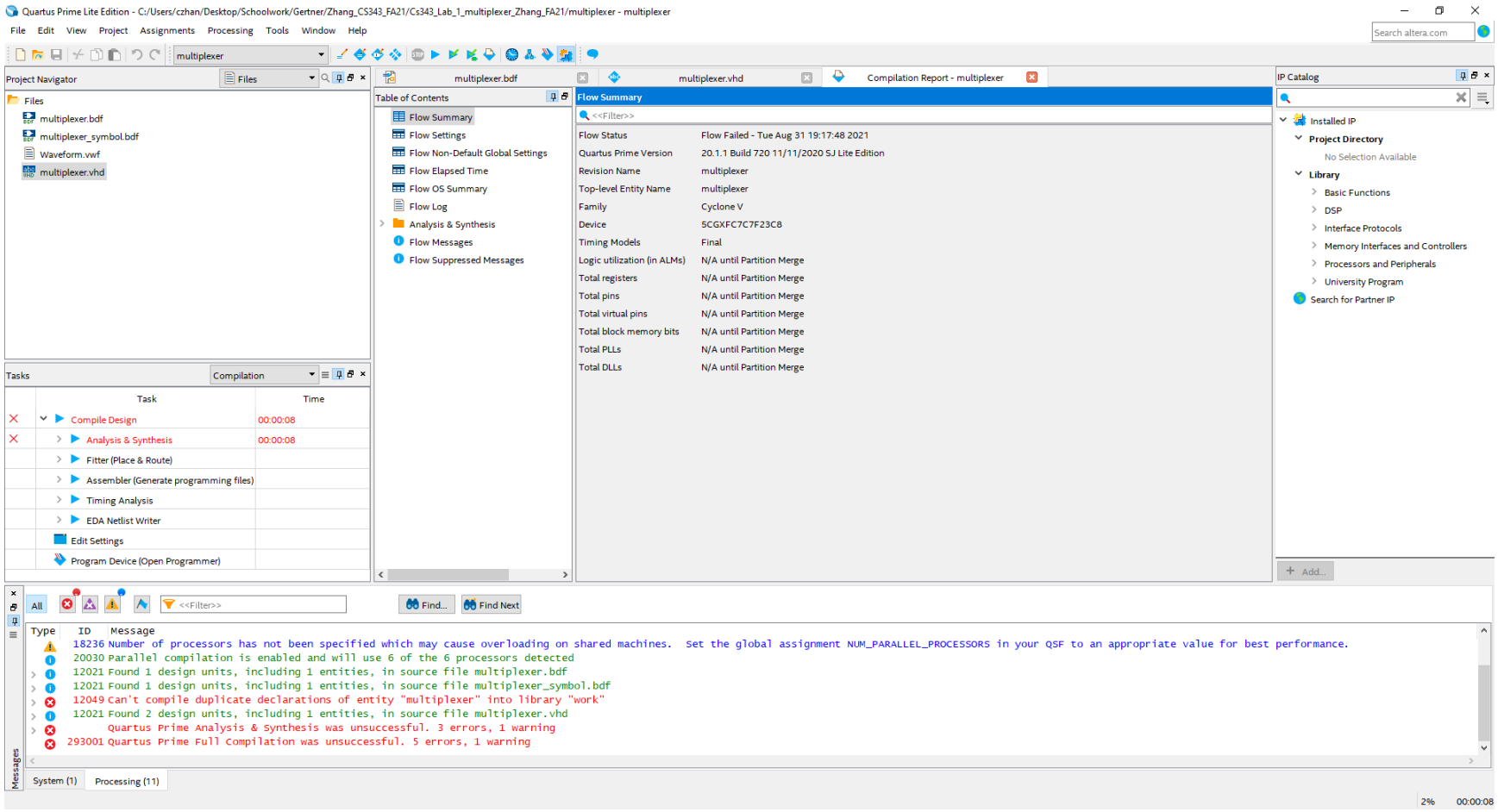
I now add the VHDL file of the design into the files

Task 1, Chue Zhang



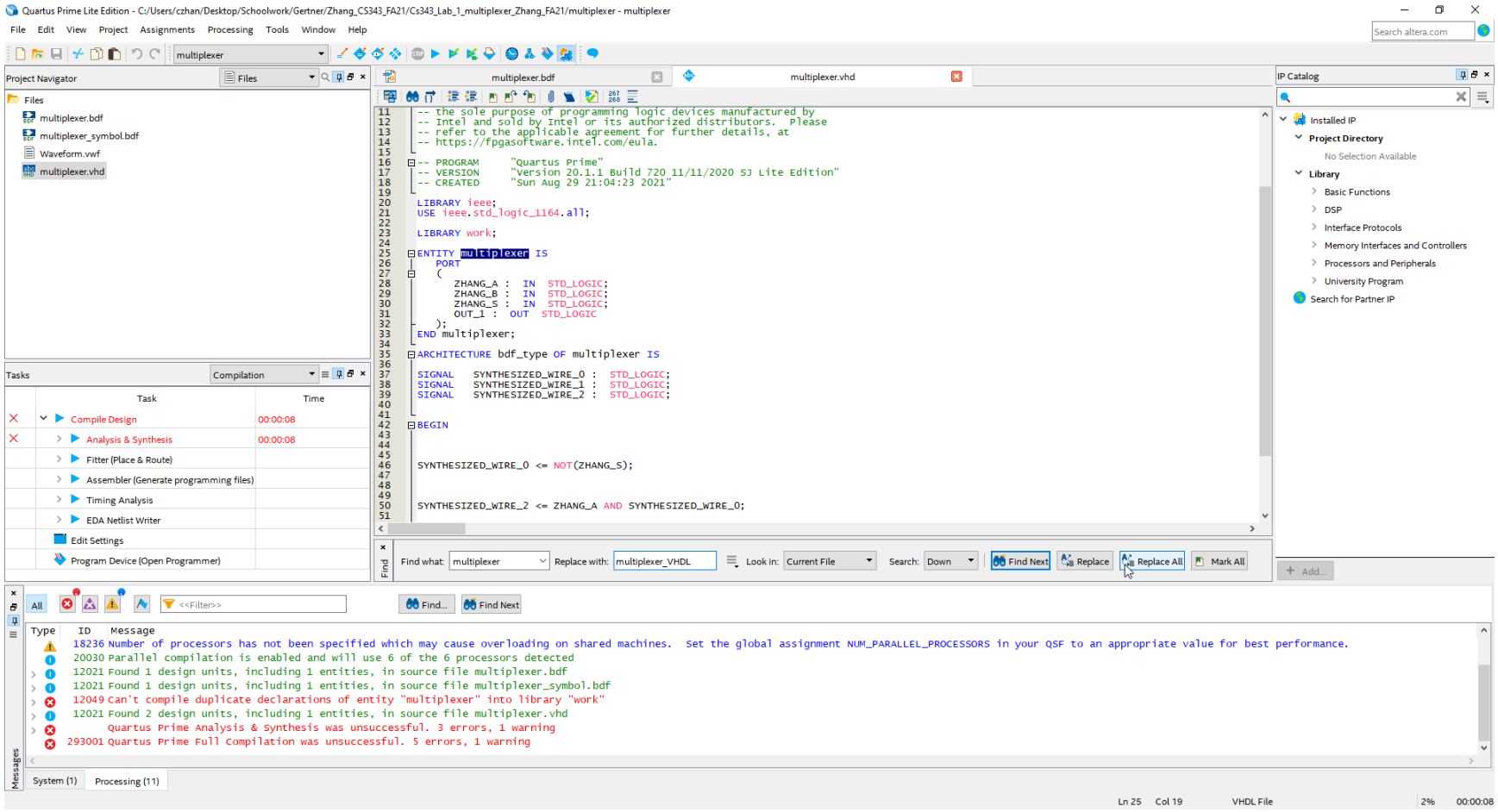
I now set the VHDL file to top level while showcasing some of the code

Task 1, Chue Zhang



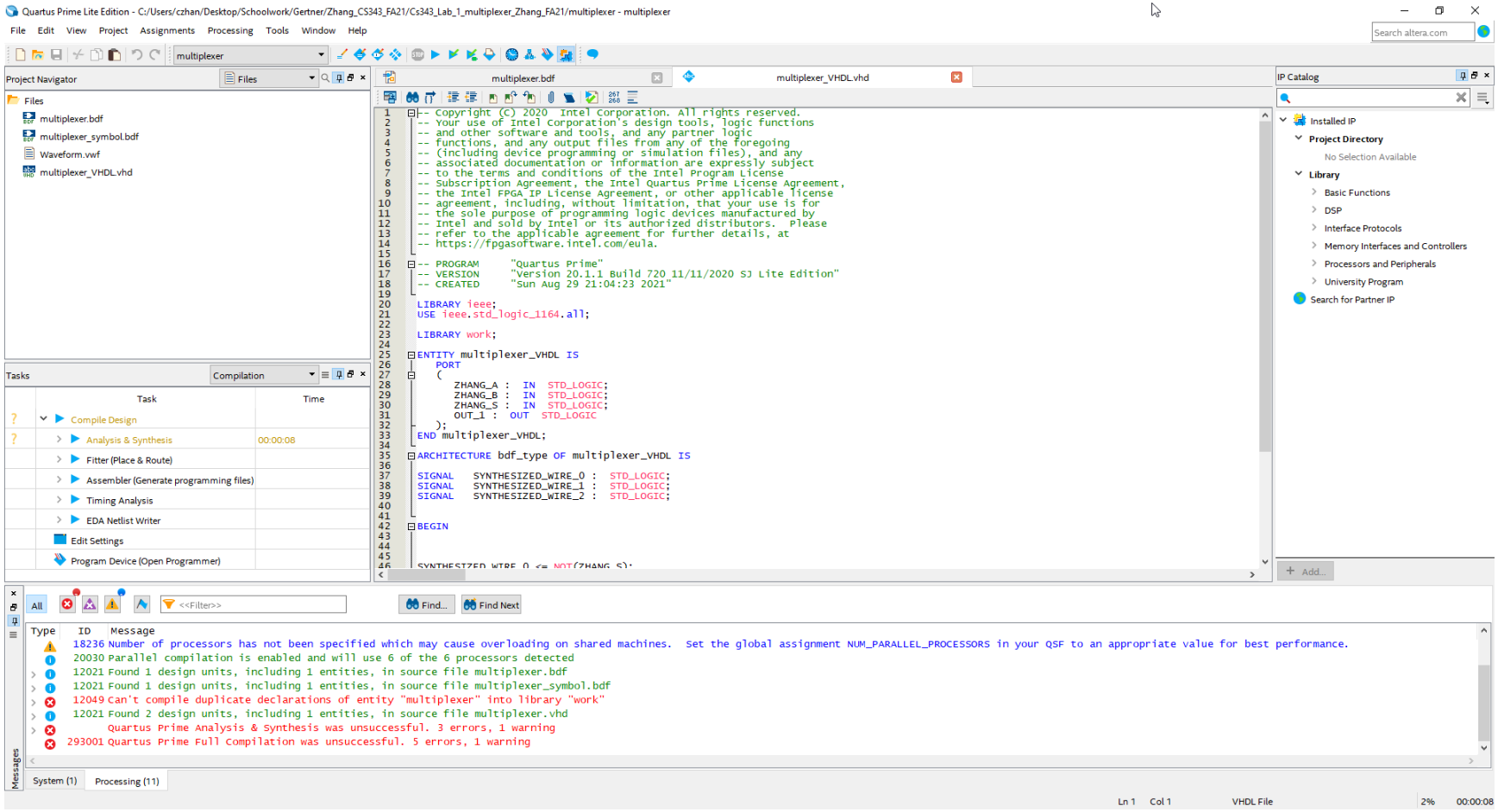
I try to compile but come to an error

Task 1, Chue Zhang



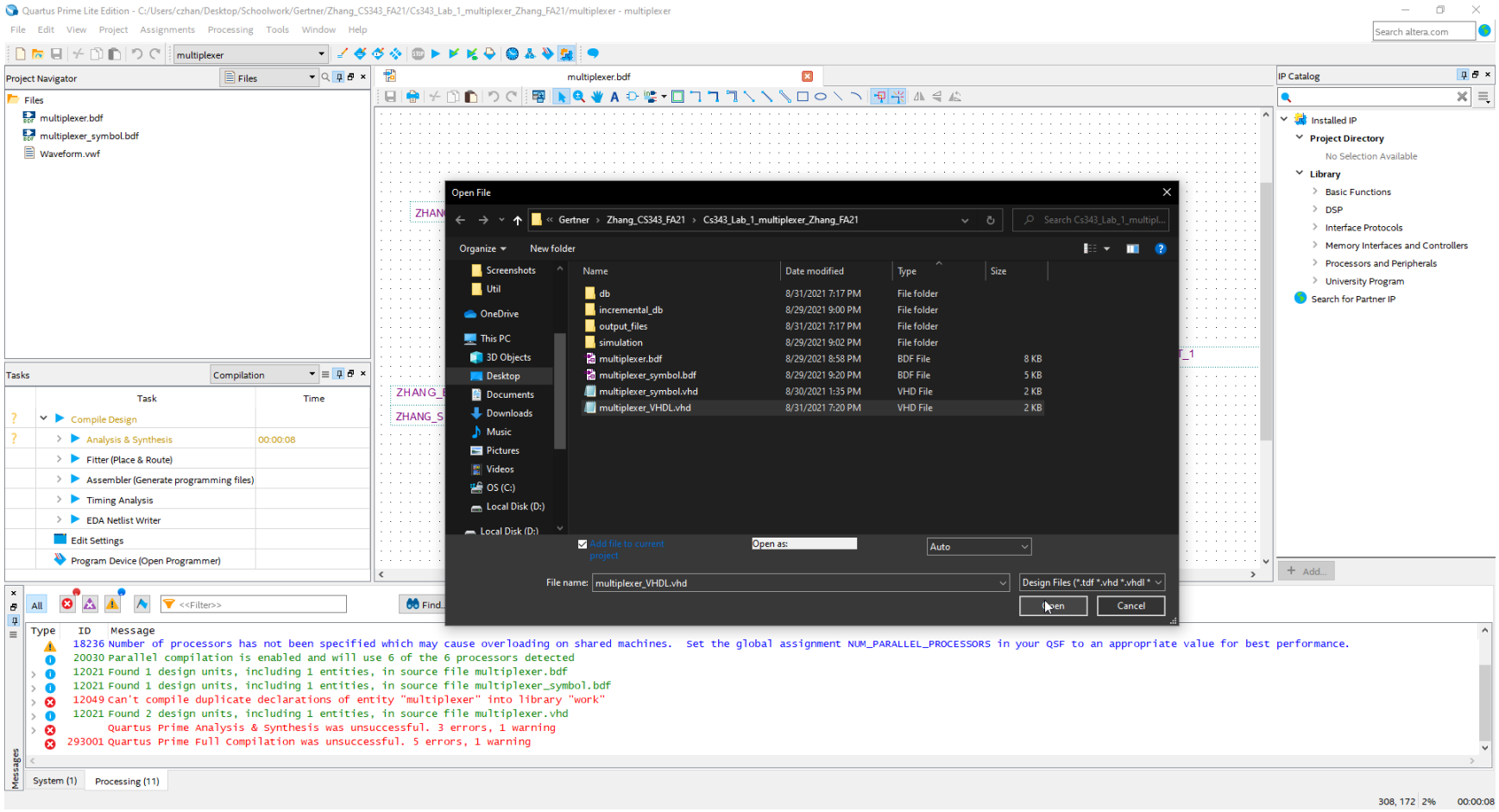
I change the highlighted multiplexer text to multiplexer_VHDL and save the VHDL file under the new corrected name

Task 1, Chue Zhang



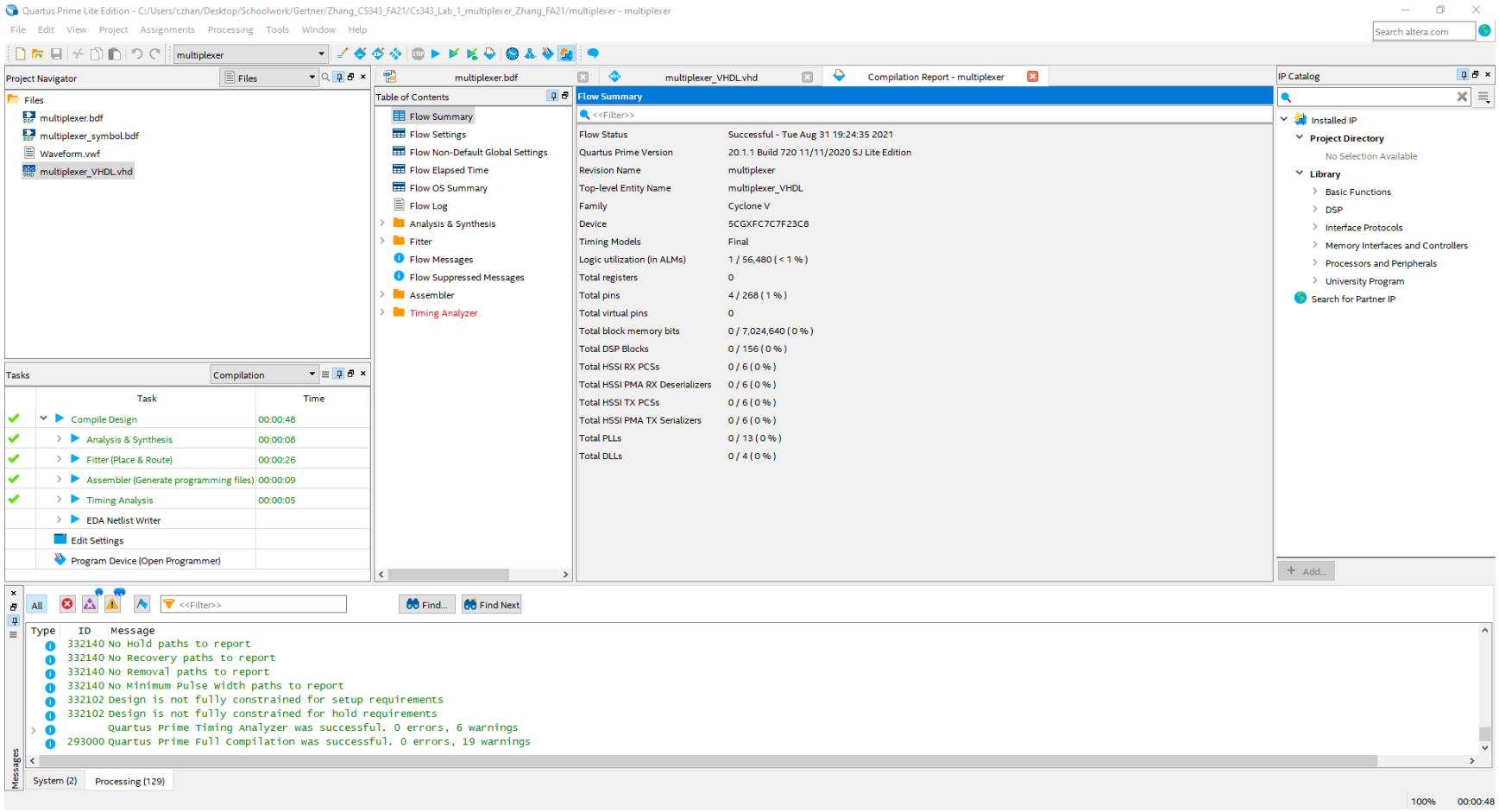
Here is the corrected code that I will then save with a different name according to what I renamed the code to

Task 1, Chue Zhang



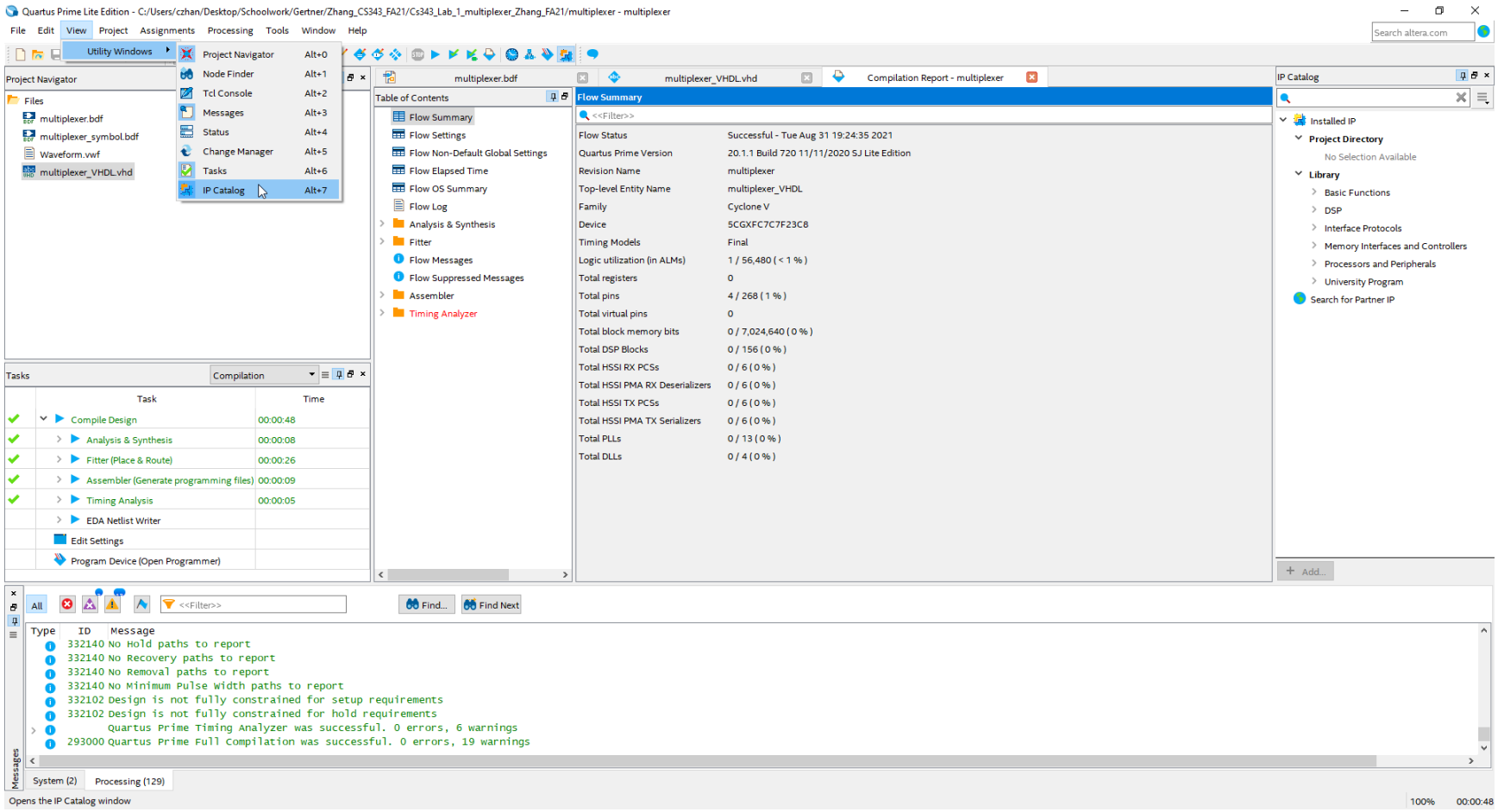
I re-add the vhdl file

Task 1, Chue Zhang



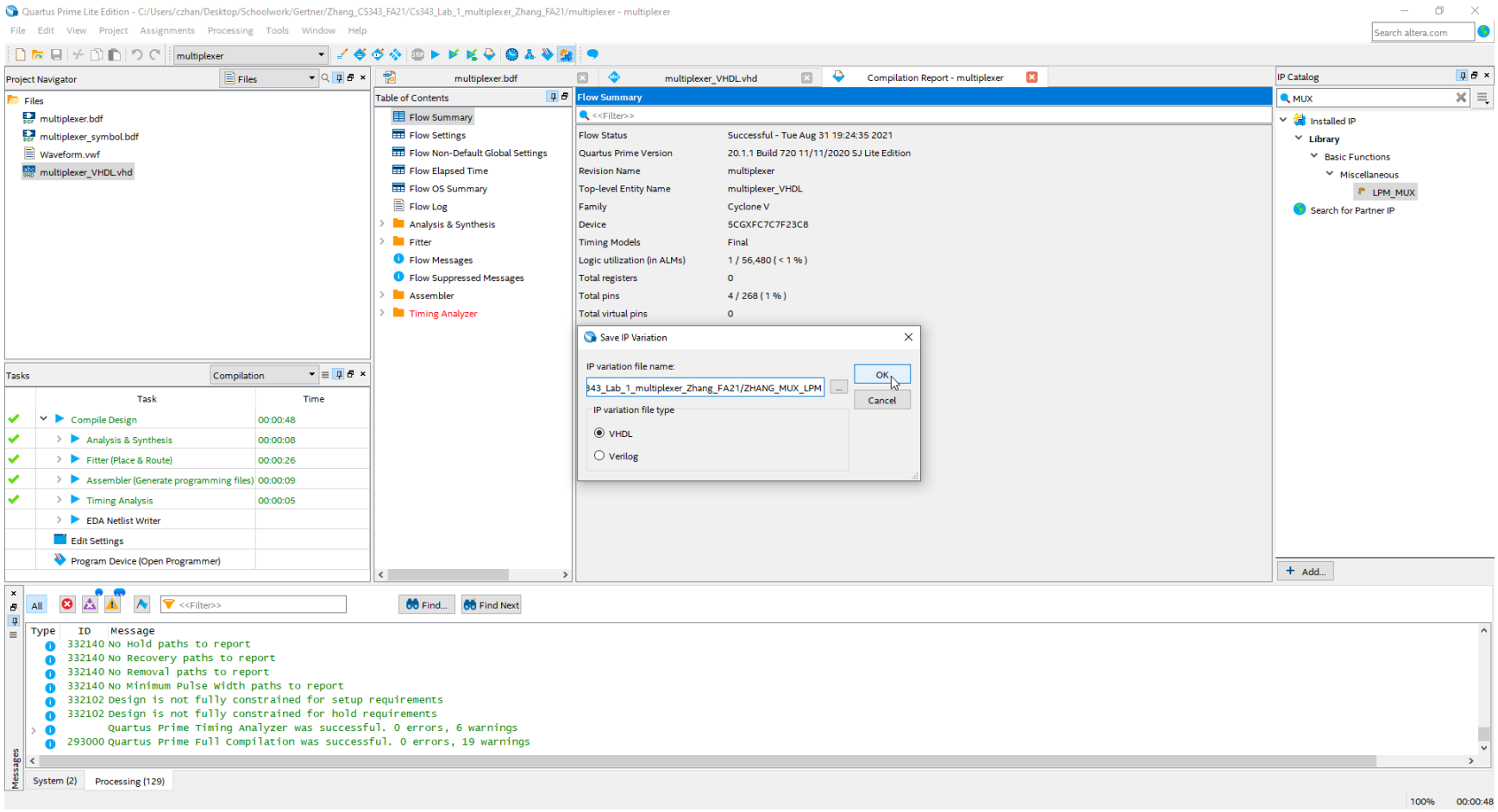
I compile with success

Task 2, Chue Zhang



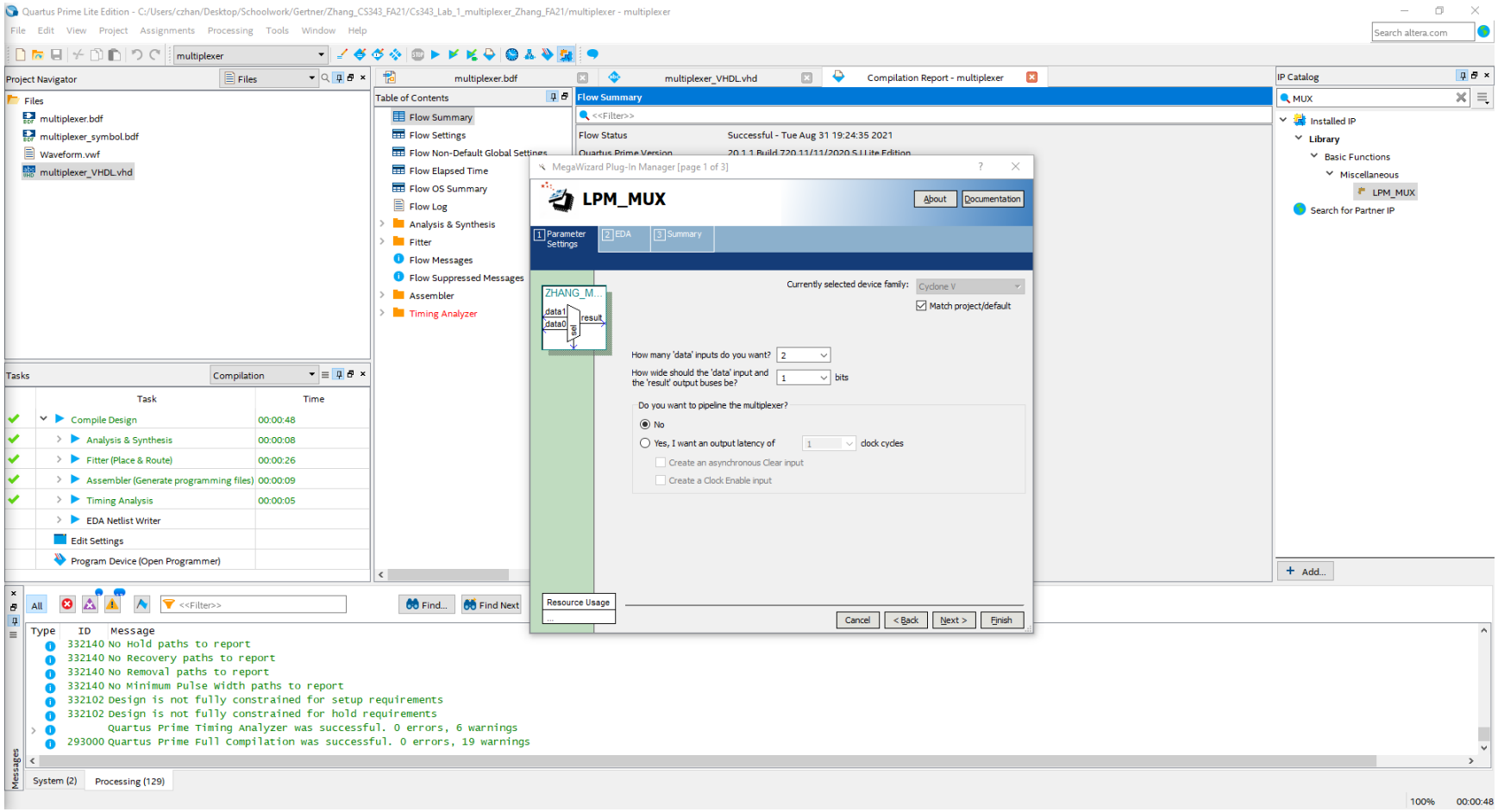
Here I ensure that the IP catalog is checked out and is available for me to use

Task 2, Chue Zhang



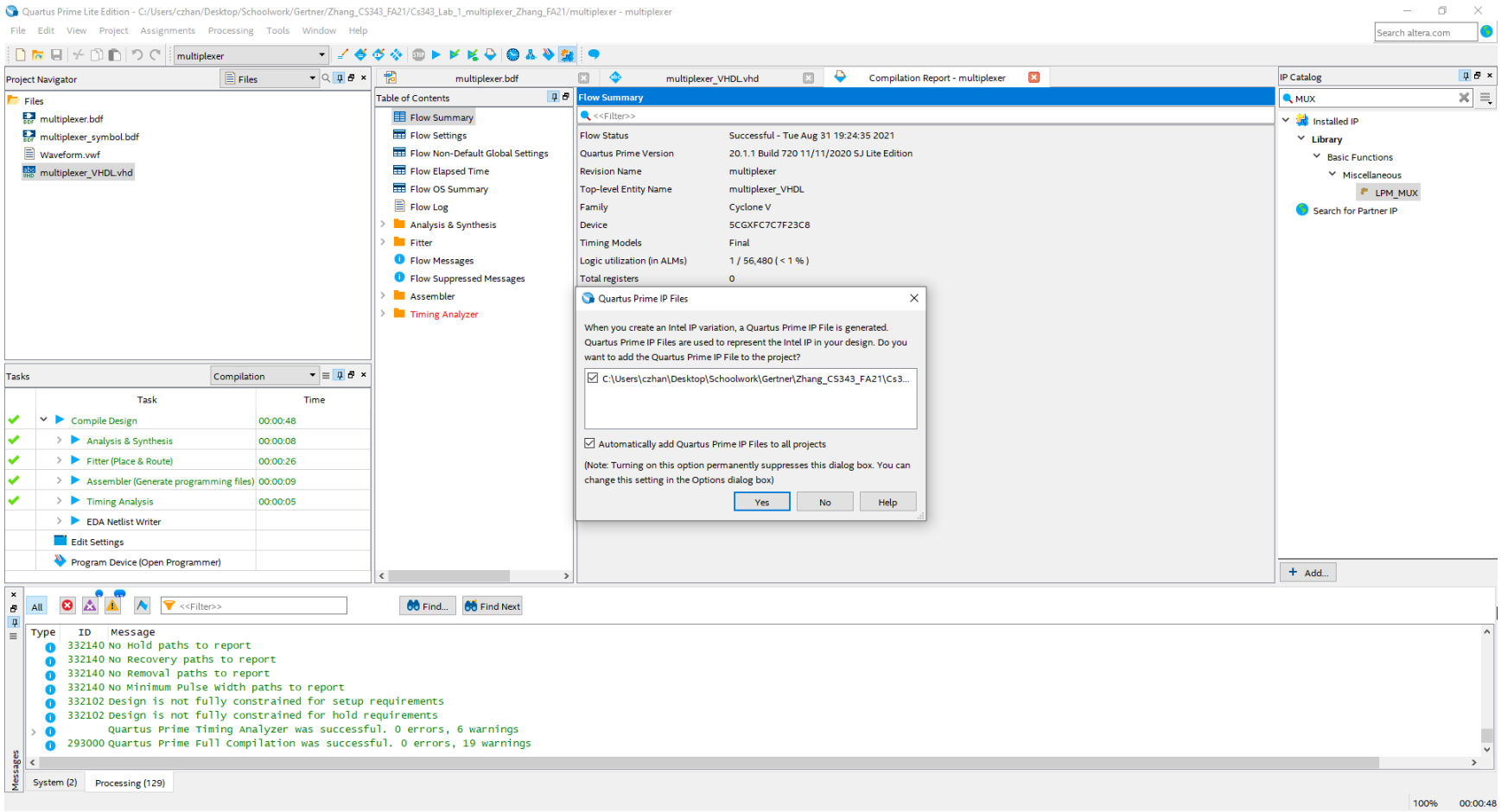
In the right where the IP catalog is, I type in MUX and a drop down showing LPM_MUX shows up. I double click and press OK

Task 2, Chue Zhang



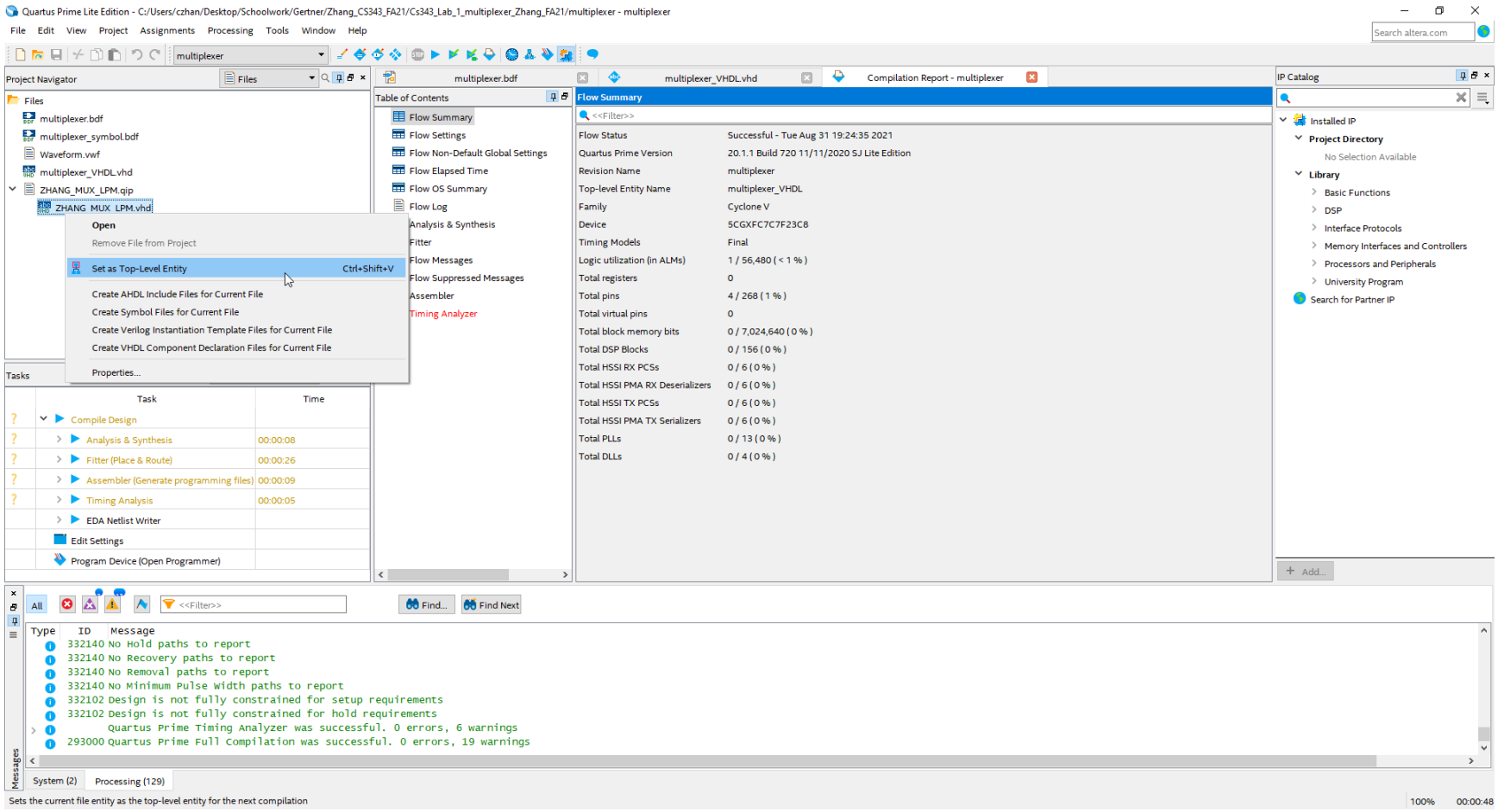
A pop up shows, I press next until I can no longer press next, then I press finish

Task 2, Chue Zhang



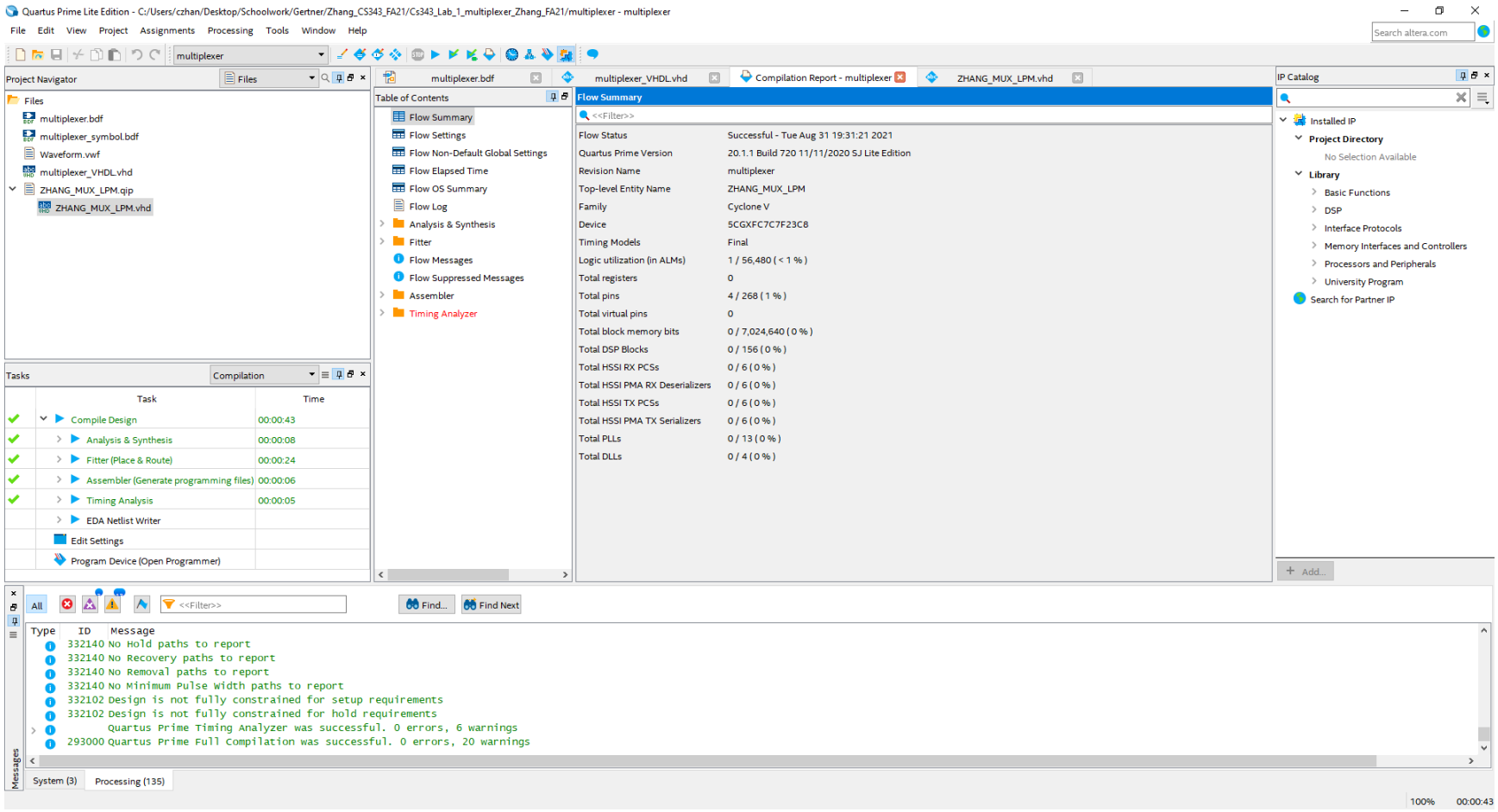
A pop up shows up and I check the box that says “automatically add quartus prime IP files to all projects” and press Yes

Task 2, Chue Zhang



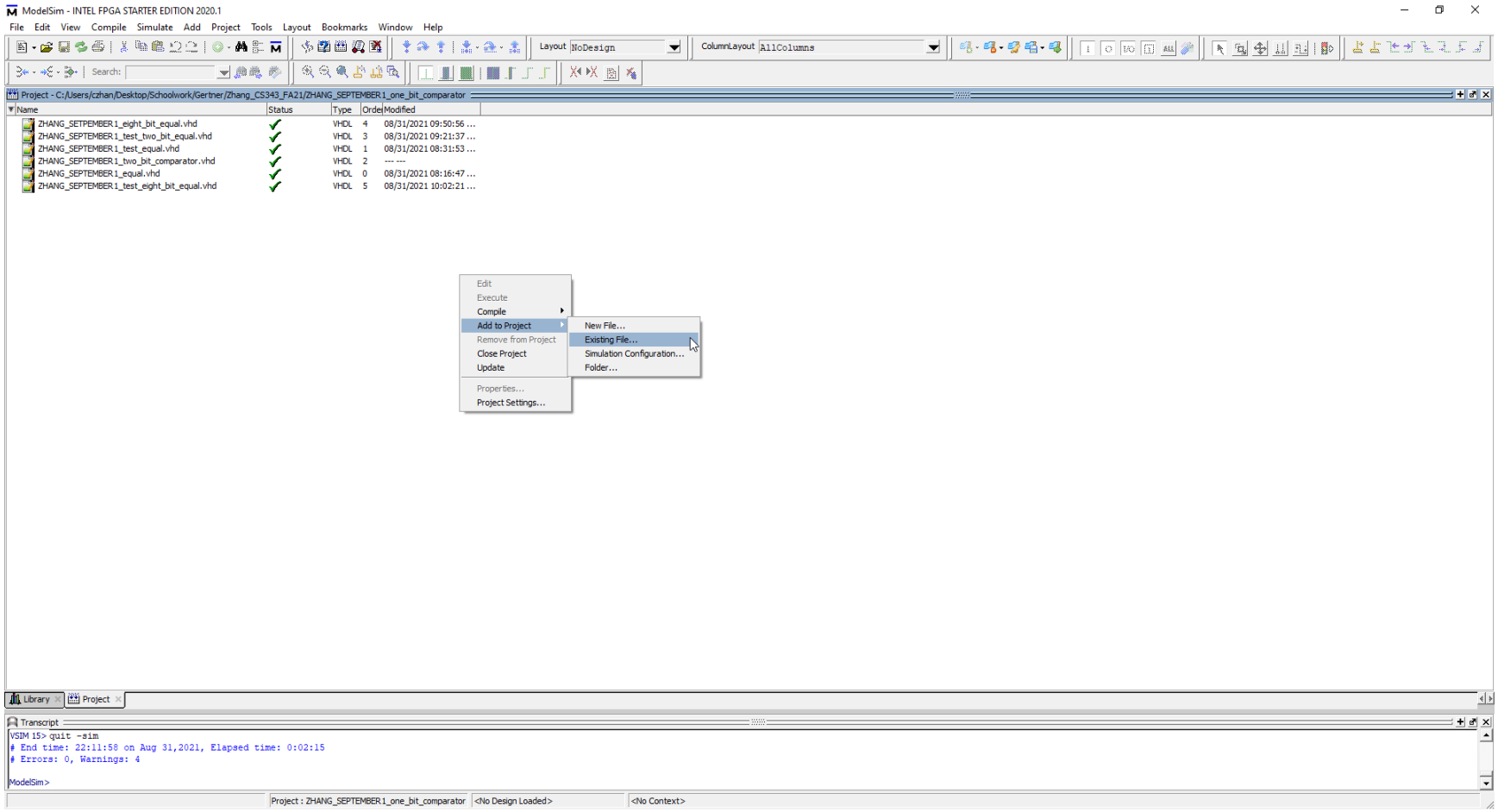
I set the new VHDL file as top level entity

Task 2, Chue Zhang



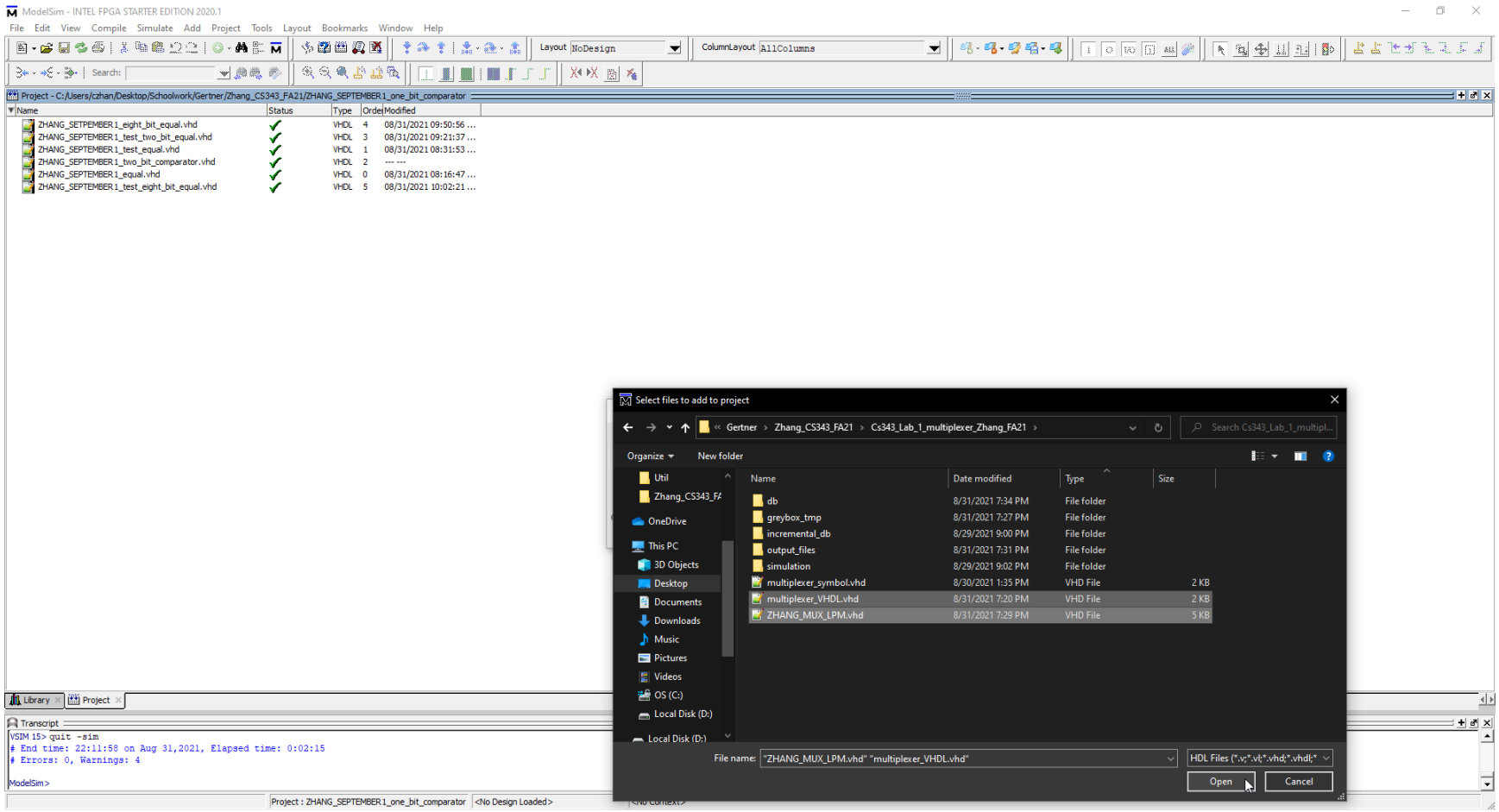
I compile with no erro

Task 3, Chue Zhang



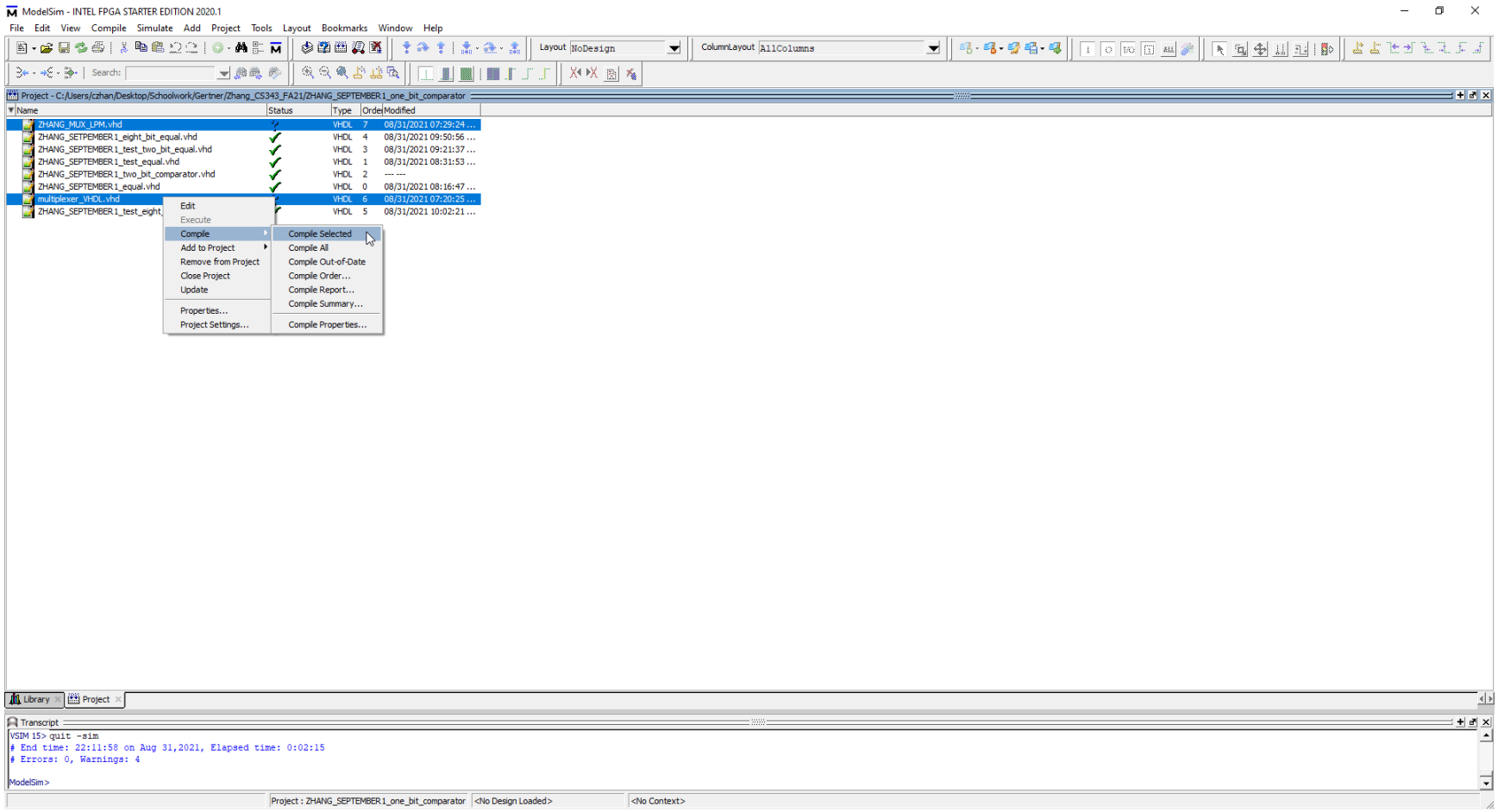
In ModelSim, I right click → Add to project → Existing file.. → and select the vhdl files necessary

Task 3, Chue Zhang



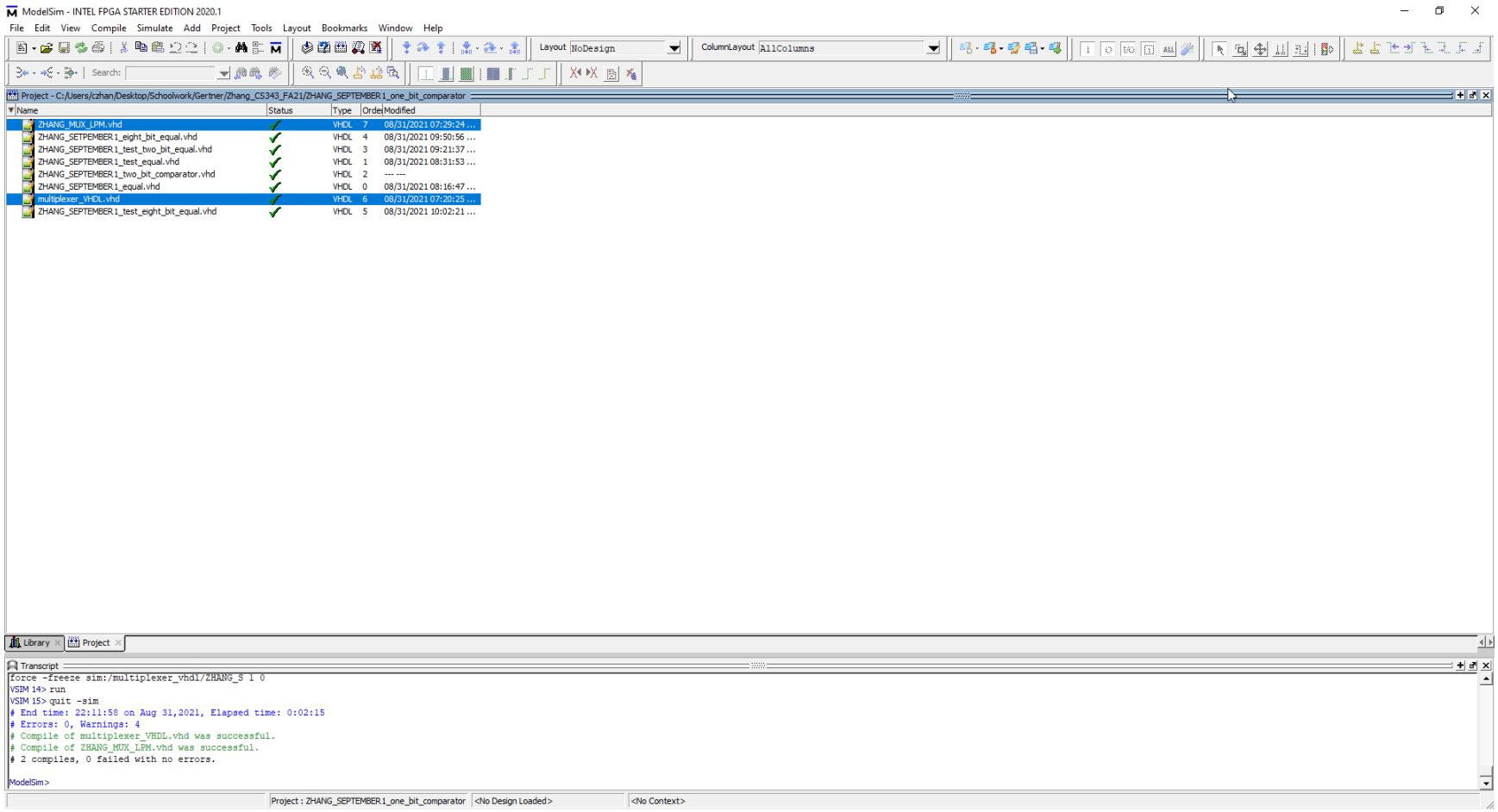
Here I am selecting the LPM MUX vhdl and the VHDL from my mux design

Task 3, Chue Zhang



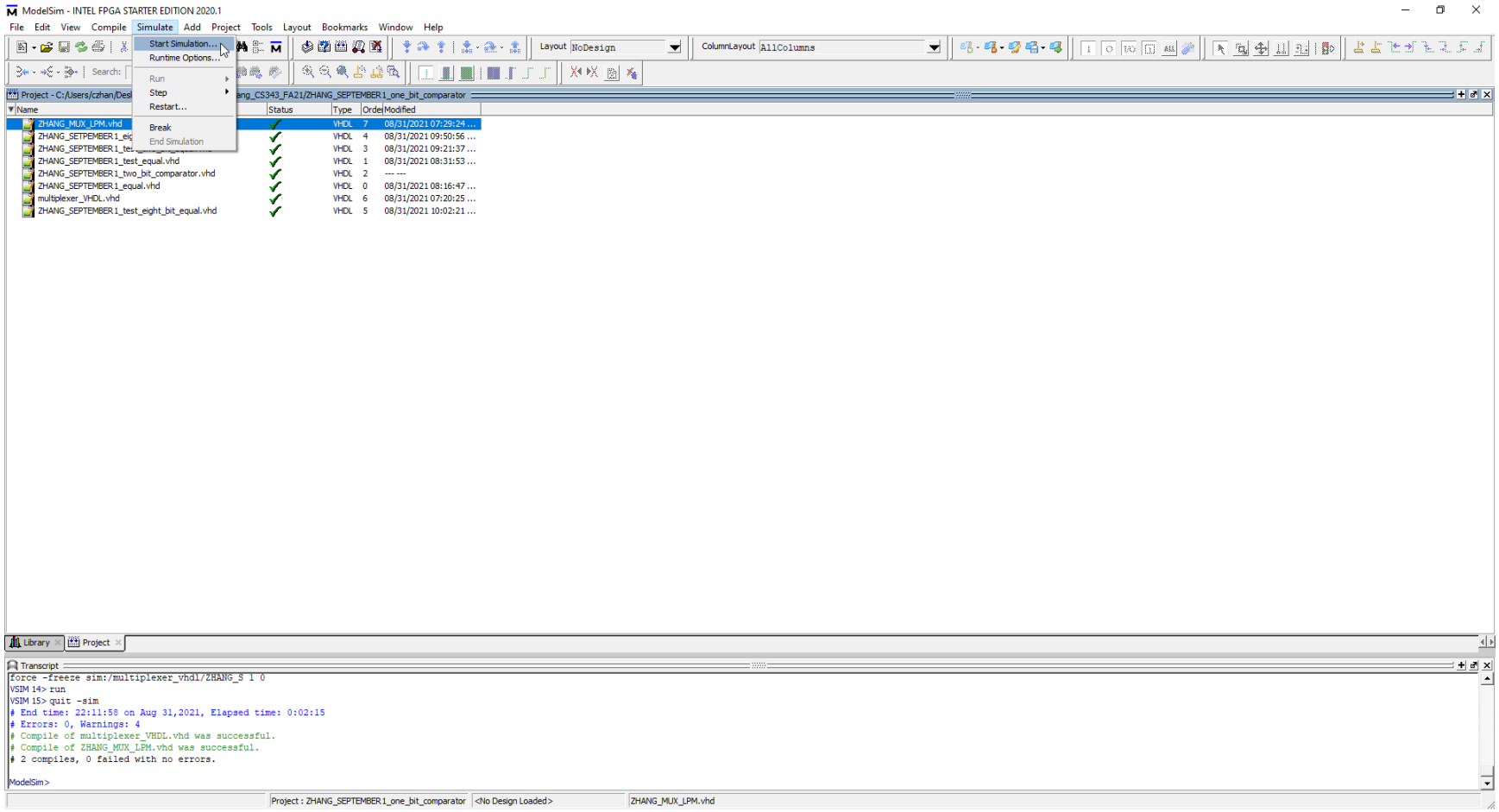
To ensure that they are correct, I compile both files by selecting both files → right click → compile → compile selected

Task 3, Chue Zhang



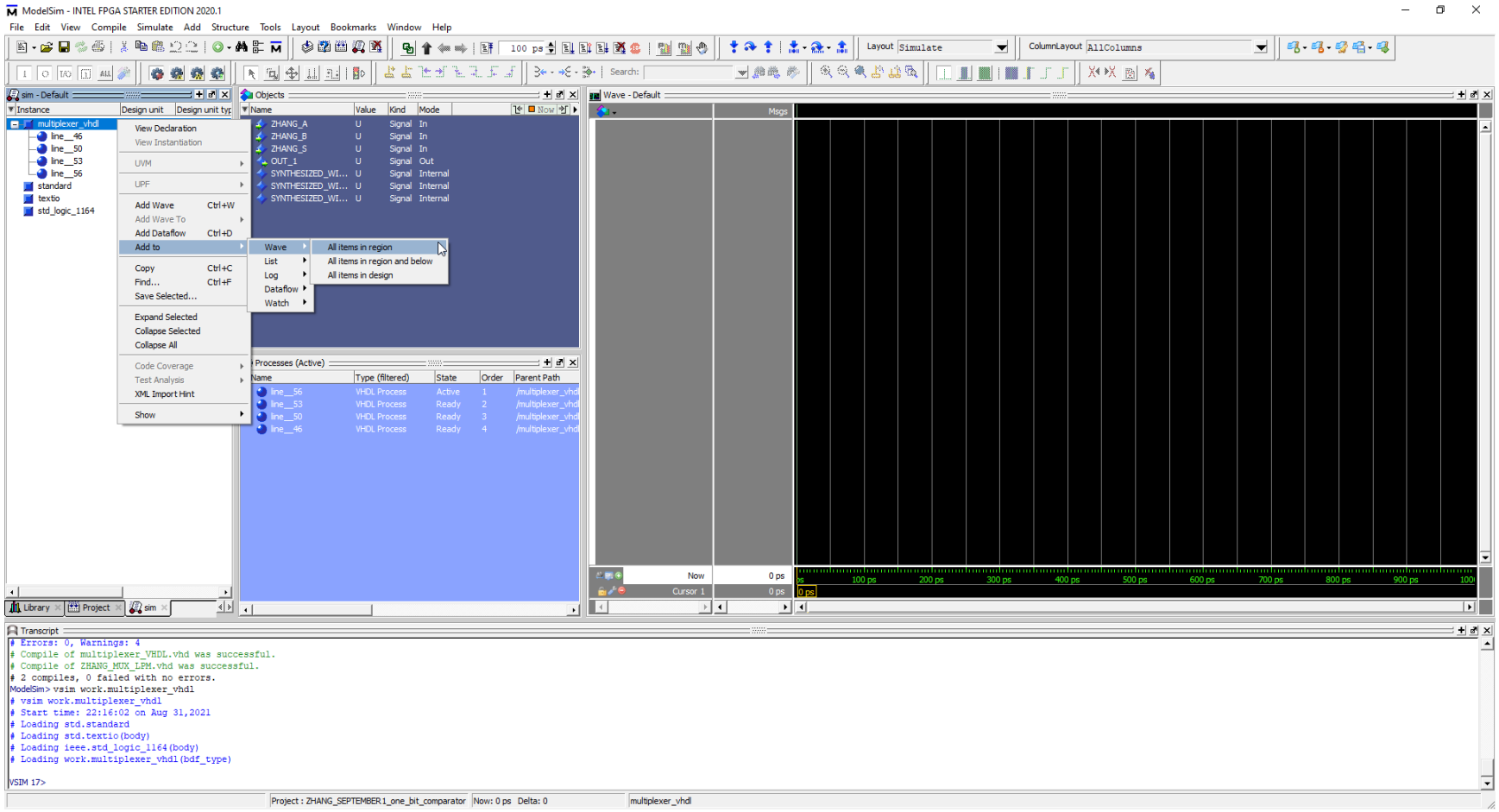
I have successfully compiled with no errors

Task 3, Chue Zhang



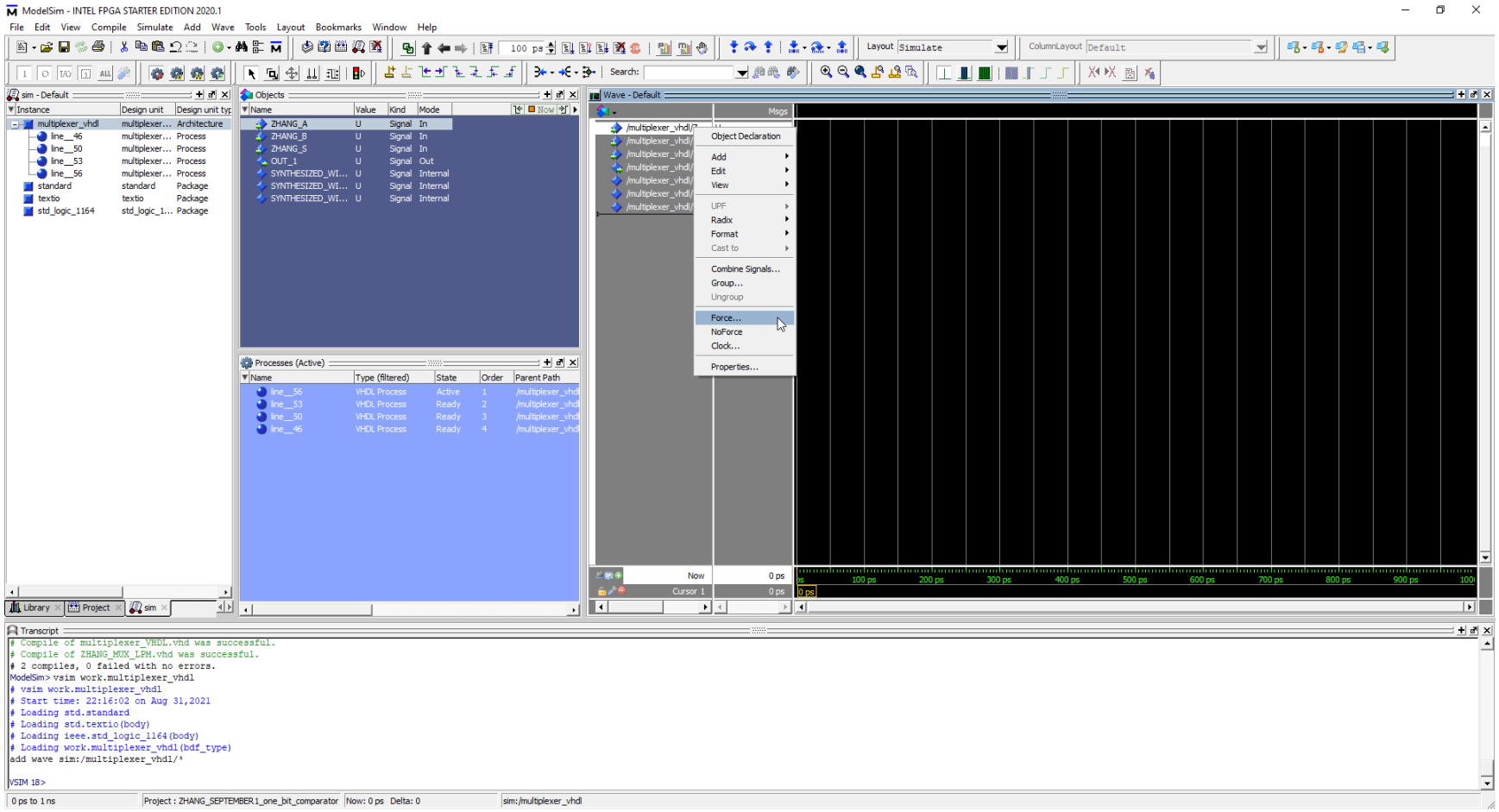
I will now proceed with simulations so on simulations → I press start simulation

Task 3, Chue Zhang



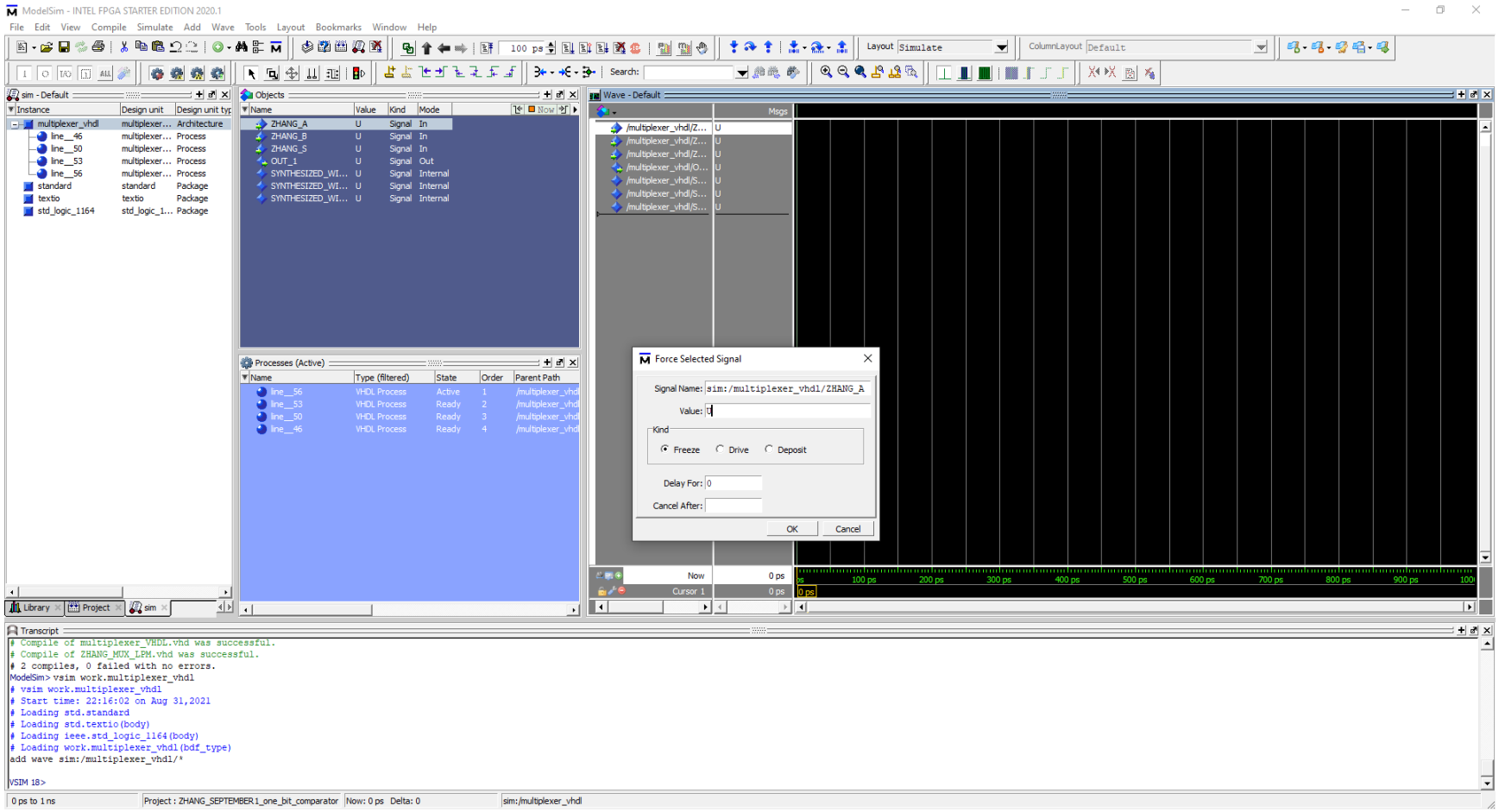
I right click the vhdl with the items in it and right click → add to → wave → add items in region

Task 3, Chue Zhang



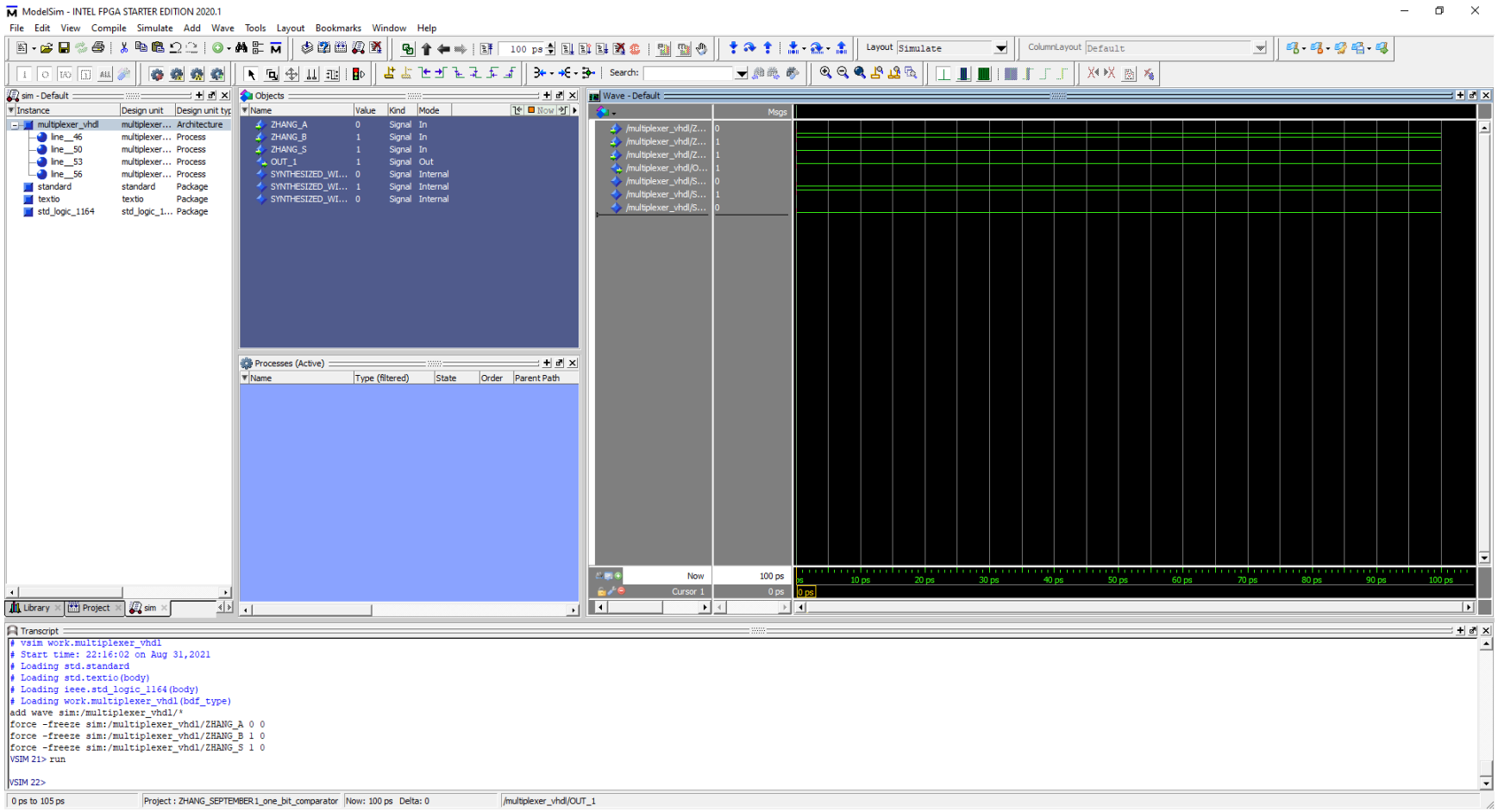
This adds all the files that I want to simulate in and then I right click ZHANG_A input and press force

Task 3, Chue Zhang



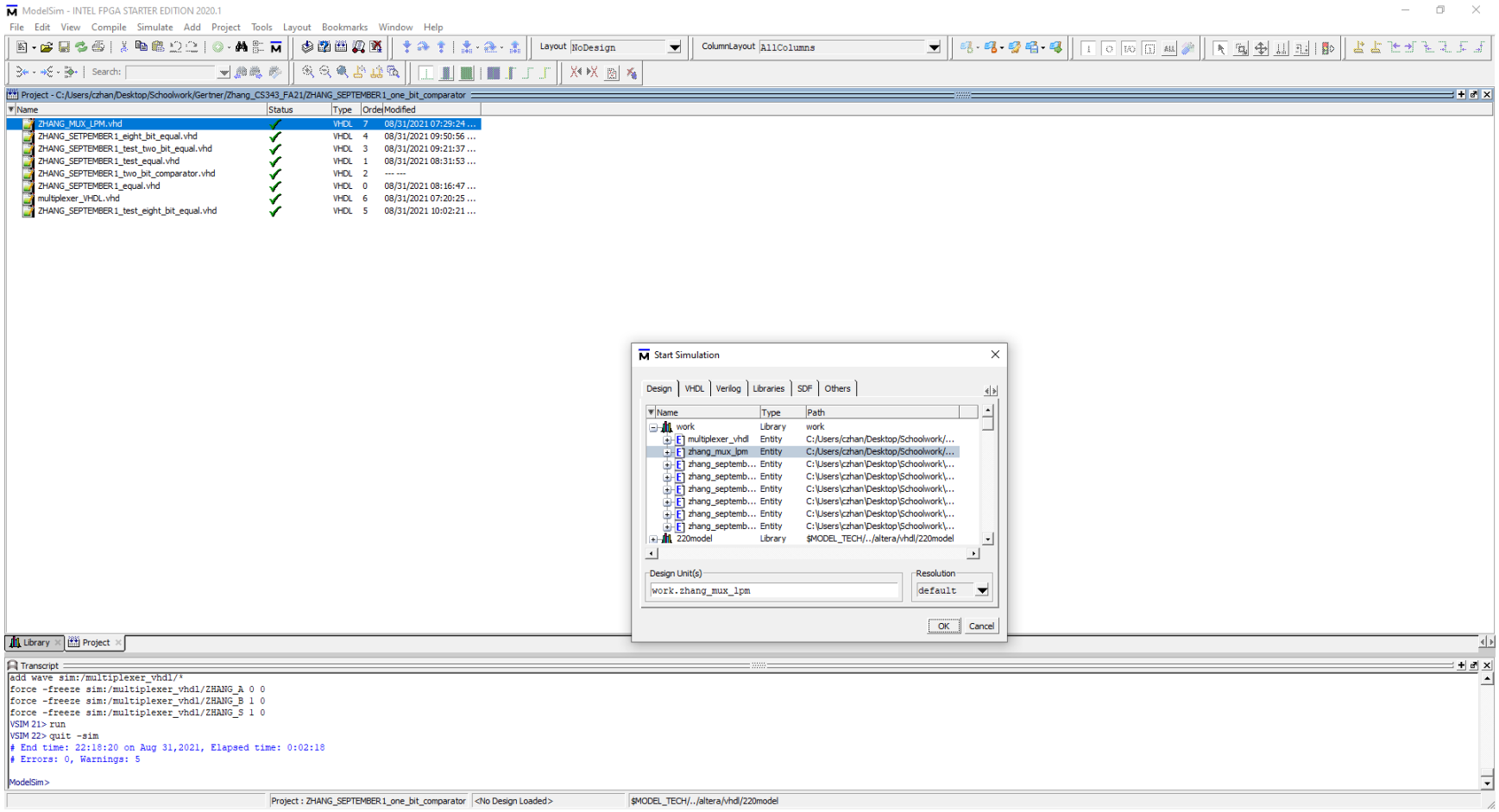
This gives me a popup menu where I can set values. For ZHANG_A I set values to 0 and for ZHANG_B and ZHANG_S I set values to 1

Task 3, Chue Zhang



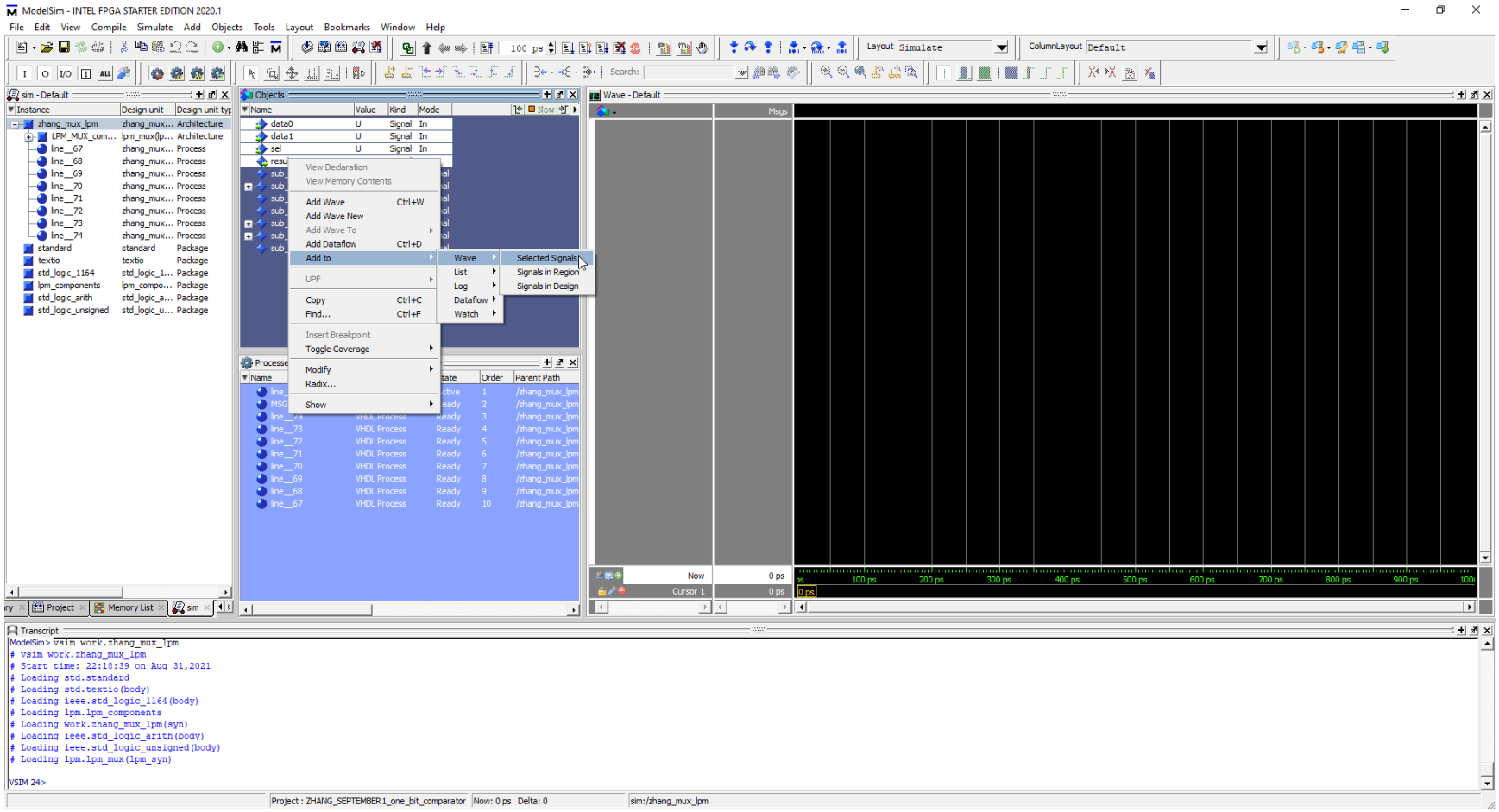
I then run the simulation and this is the output for my design's, VHDL file. No errors

Task 3, Chue Zhang



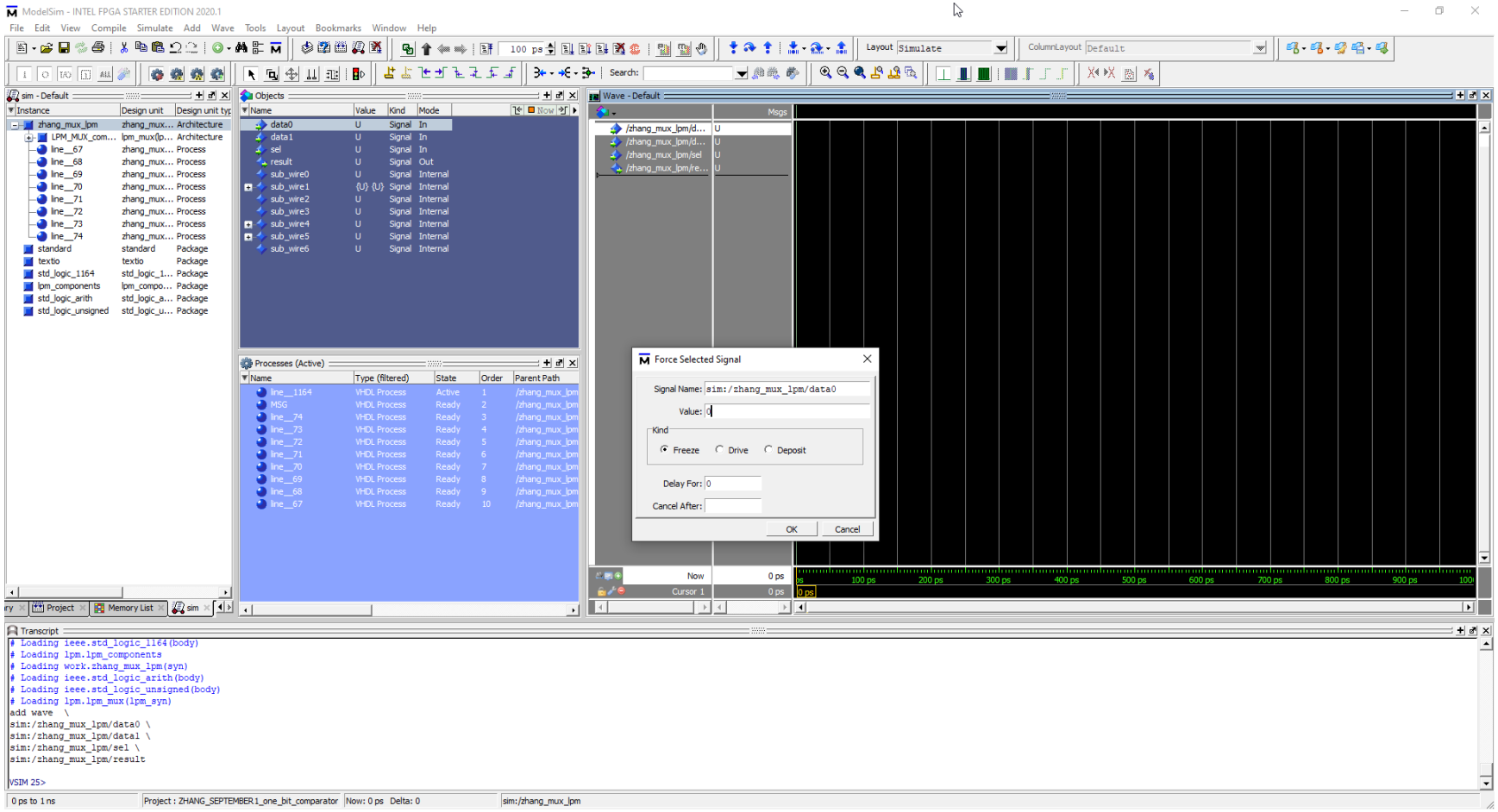
I follow the same steps as what I did for the previous VHDL file but instead, it is for the LPM MUX VHDL file

Task 3, Chue Zhang



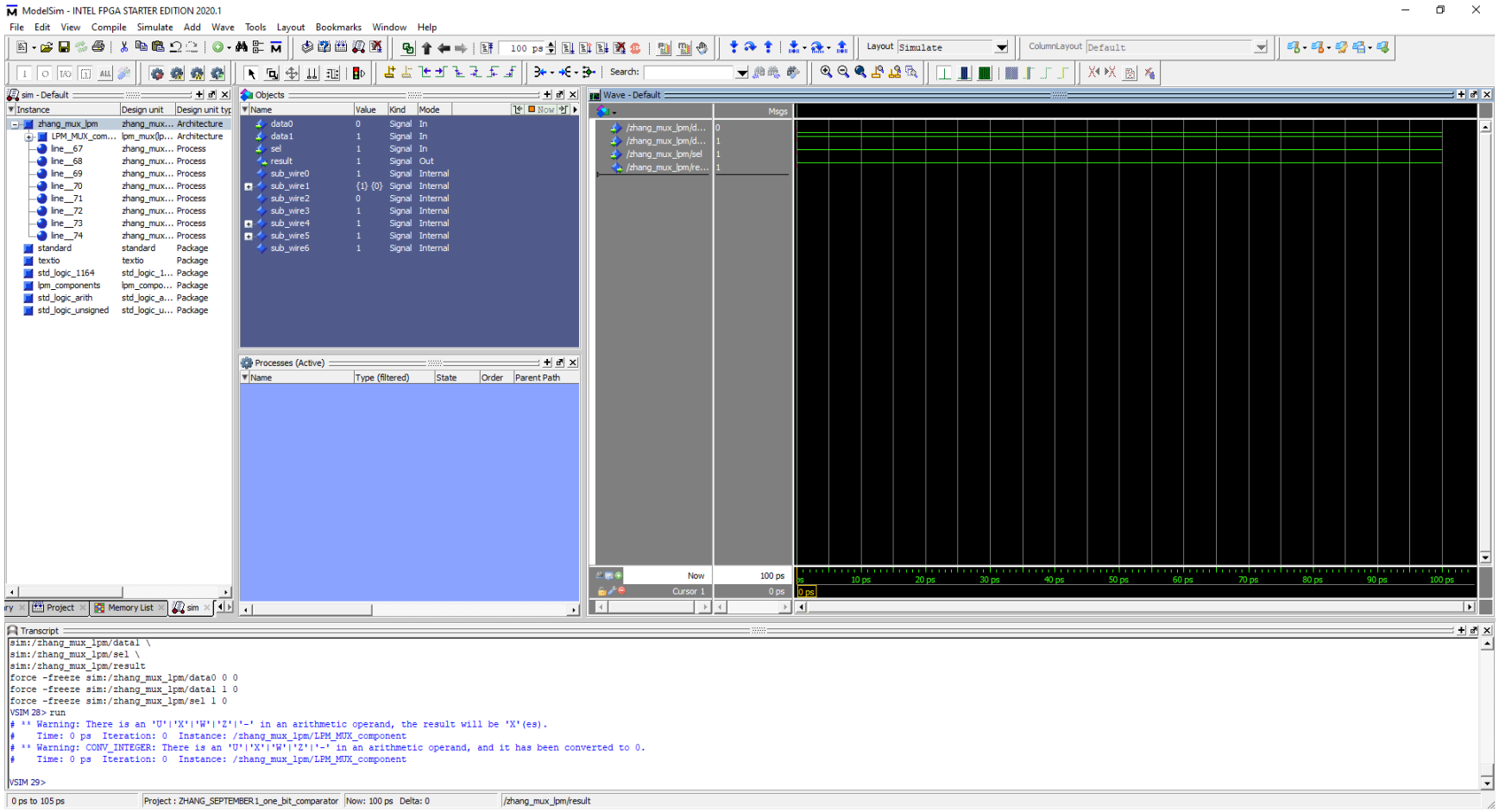
Like before, I add what I want to simulate however, I am only selecting the values necessary to be simulated with

Task 3, Chue Zhang



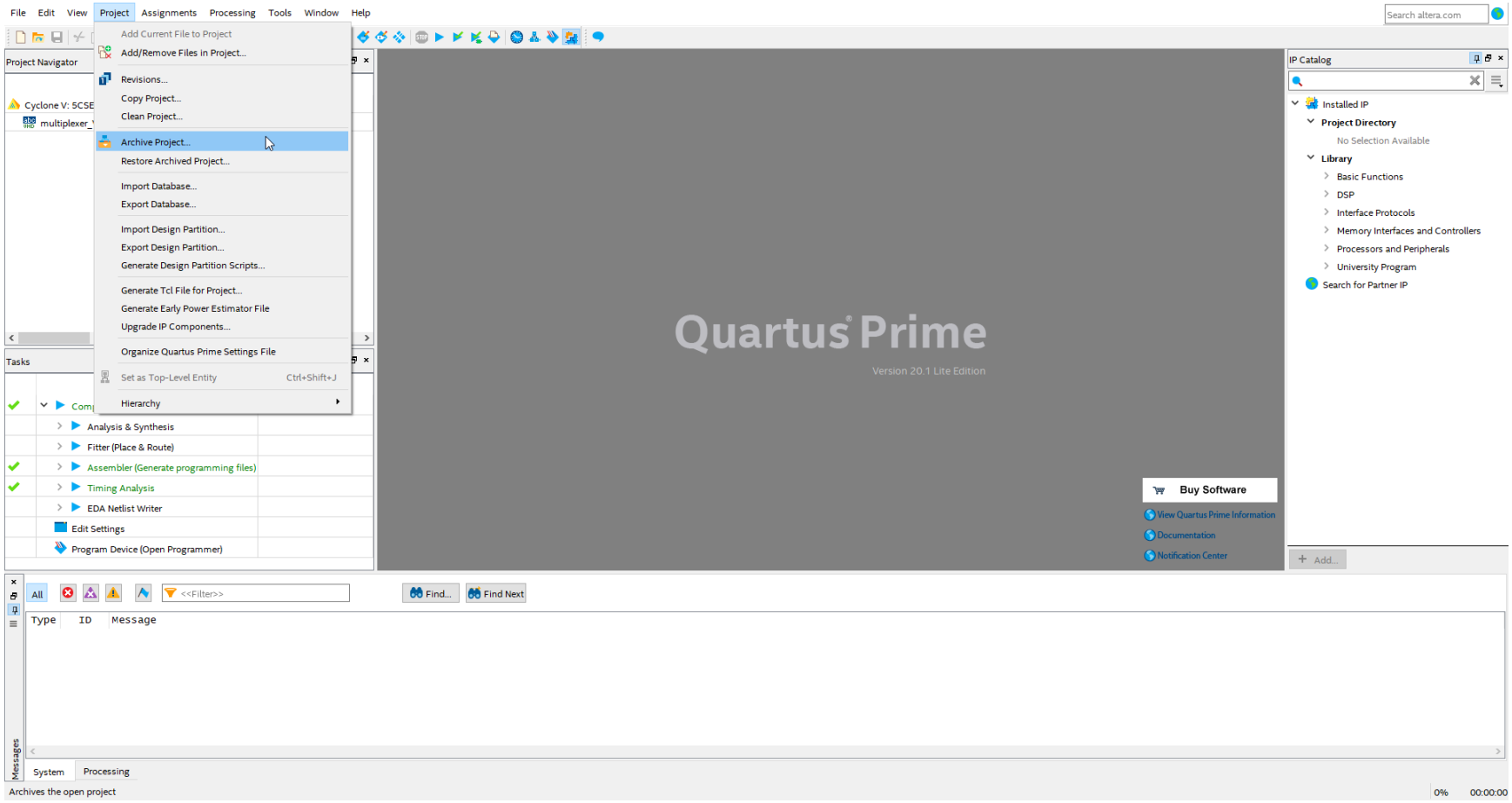
Like before, I right click on the inputs and I press force. Again will I set the values of data0 to “0” and data1 and sel to “1”

Task 3, Chue Zhang



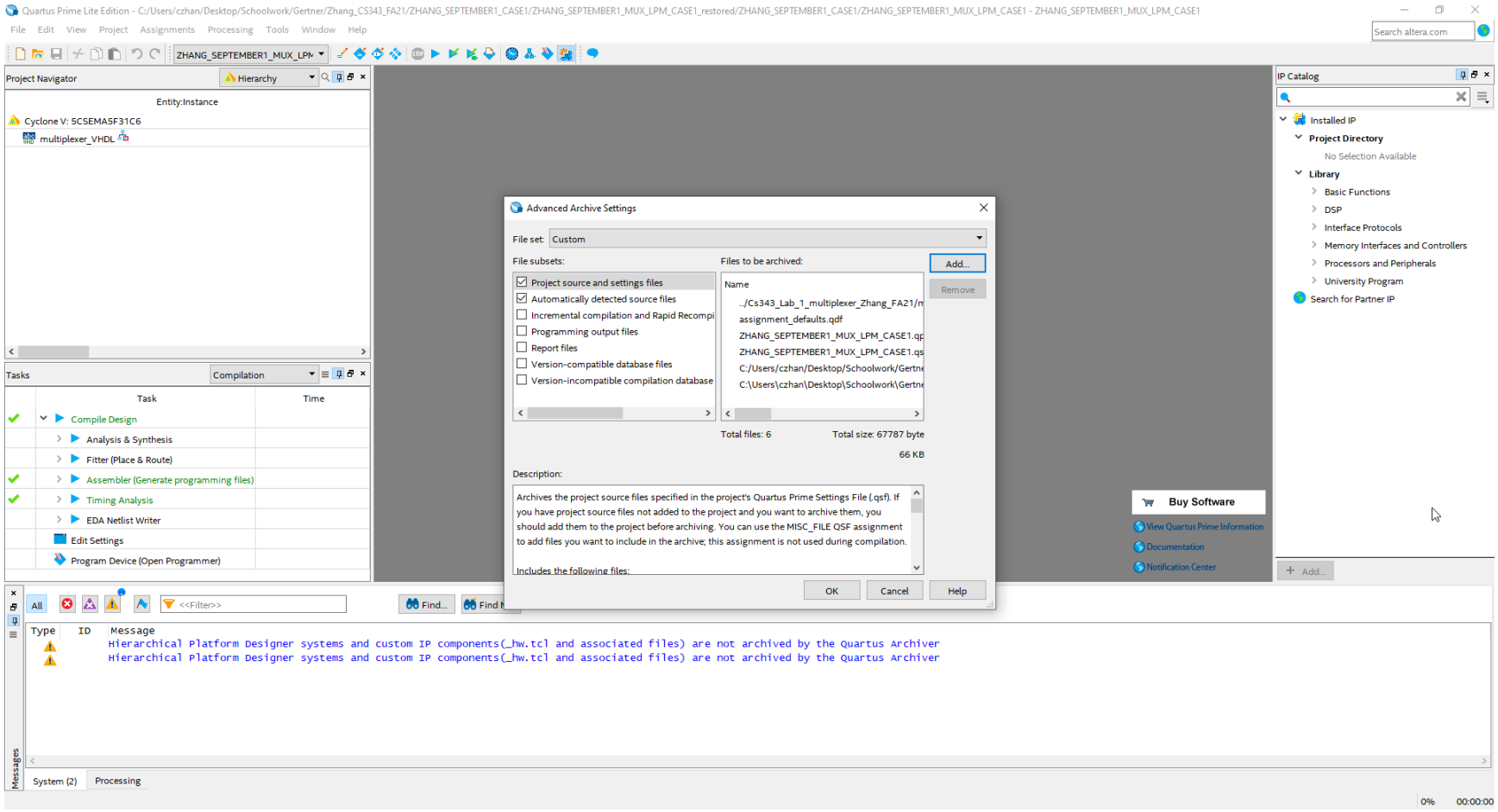
This is the output of the waveform. No errors

Task 4, Chue Zhang



To archive a project, click on project → archive project

Task 4, Chue Zhang



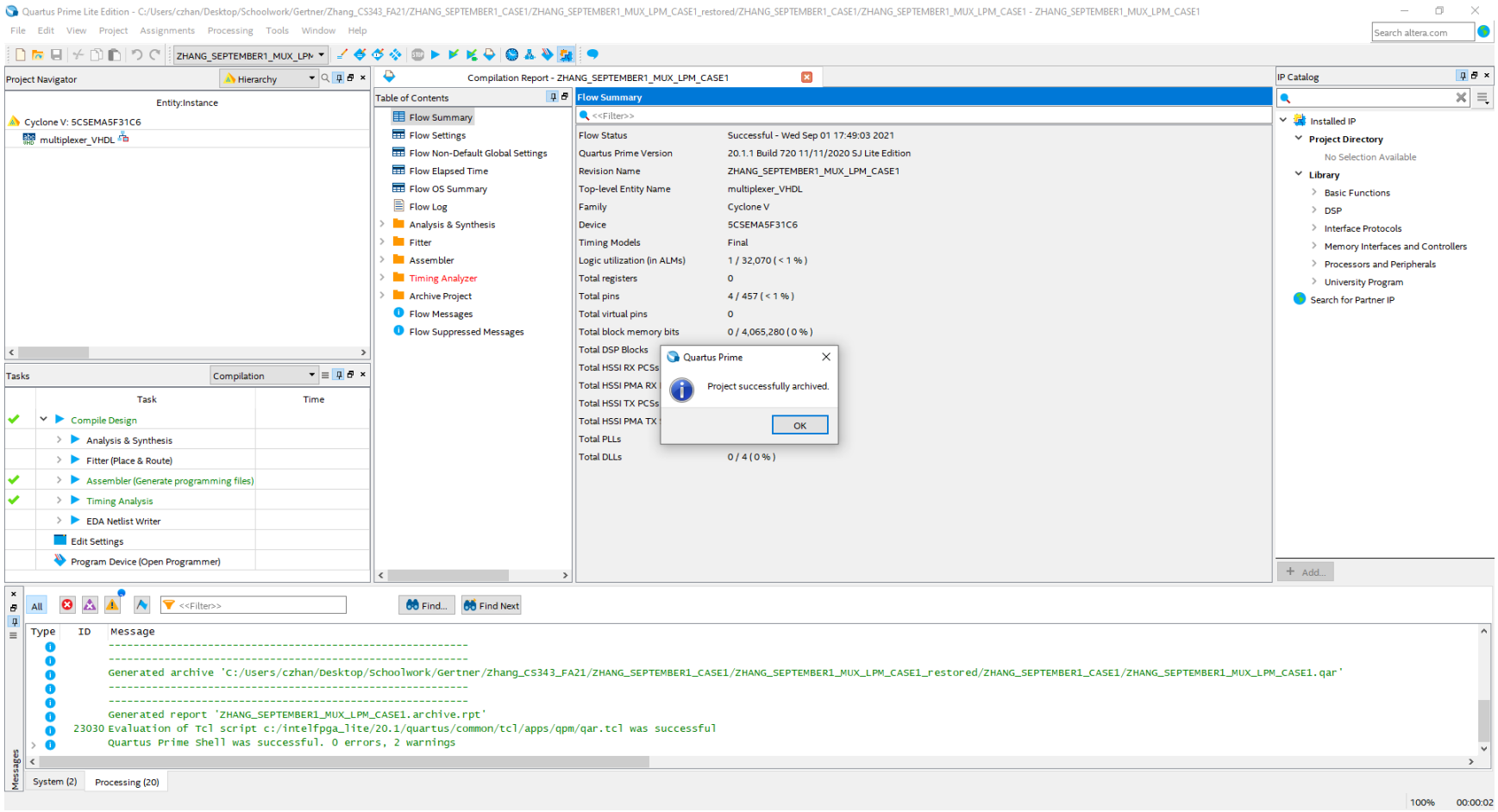
To add a README.TXT to the archive, press advanced → then the image above should show. Press add then add the respective file you wish to add in.

Task 4, Chue Zhang

```
HOW TO LOAD ARCHIVE AND RUN CONTENTS WITHIN
-------------------------------------------------

QUARTUS
=================================================
1. Download the archive file
2. You can open the archive file directly from file --> open project --> open archive file
   This should load up the contents of the archive file.
3. You should see a vhd file. Right click that vhd file and set it as the top level entity.
4. Go ahead and try to compile it doing
        Processing --> Start compiling
   This process should take a couple minutes, it depends on how strong your computer is.
5. You should have no errors compiling, you can even start using this in your own block file by
   right clicking the vhd file and pressing "Create symbol files for current file"
6. Make a new block file then press symbols tool and you can now use it
        The symbol tool should look like this

        > Project
        > c:/intelfpga_lite....

        open project and it should show

MODELSIM
=================================================
1. Open CMD
2. in the terminal, type in VSIM and modelsim should show up
3. Create a new project by going to file --> new --> project
4. Press add existing file, and within the directory of where you loaded the archive file,
   load in the vhd file
5. Compile it to ensure correctness in the code, double click the vhd to view the code
6. Press Simulate at the top bar --> start simulation
7. press the project name you created and open up the vhd file
8. on the instances tab to the left, right click the vhd file instance and click add to wave
9. you should notice on the right that there are now waves to be inputted in, right click the inputs
        ZHANG_A...
        ZHANG_B...
        ZHANG_S...
   and press force and input values 0 or 1 to simulate the design.
```

This is the readme file that I will be including in, complete the archive by pressing ok

Task 4, Chue Zhang



Once the archived has been successfully created, a popup like this should show. Also refer to the green text below for success.