

Laboratory Project 2: Comparators

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Cs343/Cs342, Professor Isidor Gertner

Task 0 : 1-bit comparator , Chue Zhang

```
C:\Users\czhan\Desktop\Schoolwork\Gertner\Zhang_CS343_FA21\ZHANG_SEPTMBER1_equal.vhd - Notepad++
File Edit Search View Encoding Language Settings Tools Macro Run Plugins Window ?
ZHANG_SEPTMBER1_equal.vhd [X]
1  library ieee;
2  use ieee.std_logic_1164.all;
3
4  entity ZHANG_SEPTMBER1_equal is
5      port ( ZHANG_SEPTMBER1_IO, ZHANG_SEPTMBER1_I1 : in std_logic;
6            ZHANG_SEPTMBER1_Eq : out std_logic);
7  end ZHANG_SEPTMBER1_equal;
8
9
10 architecture ZHANG_SEPTMBER1_arch of ZHANG_SEPTMBER1_equal is
11     signal ZHANG_SEPTMBER1_p0, ZHANG_SEPTMBER1_p1 : std_logic;
12     begin
13         ZHANG_SEPTMBER1_Eq <= ZHANG_SEPTMBER1_p0 or ZHANG_SEPTMBER1_p1;
14         ZHANG_SEPTMBER1_p0 <= (not ZHANG_SEPTMBER1_IO) and (not ZHANG_SEPTMBER1_I1);
15         ZHANG_SEPTMBER1_p1 <= ZHANG_SEPTMBER1_IO and ZHANG_SEPTMBER1_I1;
16     end ZHANG_SEPTMBER1_arch;

VHSIC Hardware Description Language file | length : 608 | lines : 16 | Ln : 14 | Col : 84 | Pos : 511 | Windows (CR.LF) | UTF-8 | INS
```

In here is the 1-bit comparator VHDL code that is unoptimized

Task 0 : 1-bit comparator , Chue Zhang

```
C:\Users\czhan\Desktop\Schoolwork\Gertner\Zhang_CS343_FA21\ZHANG_SEPTMBER1_test_equal.vhd - Notepad++
File Edit Search View Encoding Language Settings Tools Macro Run Plugins Window ?
ZHANG_SEPTMBER1_test_equal.vhd X
ZHANG_SEPTMBER1_test_equal.vhd X
1  library ieee;
2  use ieee.std_logic_1164.all;
3
4  entity ZHANG_SEPTMBER1_test_equal is
5  end ZHANG_SEPTMBER1_test_equal;
6
7  architecture ZHANG_SEPTMBER1_arch_test of ZHANG_SEPTMBER1_test_equal is
8  component ZHANG_SEPTMBER1_equal
9
10 port ( ZHANG_SEPTMBER1_I0, ZHANG_SEPTMBER1_I1 : in std_logic;
11        ZHANG_SEPTMBER1_Eq : out std_logic);
12 end component;
13
14 signal ZHANG_SEPTMBER1_p1, ZHANG_SEPTMBER1_p0, ZHANG_SEPTMBER1_pout : std_logic;
15 signal error : std_logic := '0';
16 begin
17 uut: ZHANG_SEPTMBER1_equal port map (ZHANG_SEPTMBER1_I0 => ZHANG_SEPTMBER1_p0, ZHANG_SEPTMBER1_I1 => ZHANG_SEPTMBER1_p1, ZHANG_SEPTMBER1_Eq => ZHANG_SEPTMBER1_pout);
18
19 process
20 begin
21 ZHANG_SEPTMBER1_p0 <= '1';
22 ZHANG_SEPTMBER1_p1 <= '0';
23 wait for 1 ns;
24 if (ZHANG_SEPTMBER1_pout = '1') then
25 error <= '1';
26 end if;
27 wait for 200 ns;
28 ZHANG_SEPTMBER1_p0 <= '1';
29 ZHANG_SEPTMBER1_p1 <= '1';
30 wait for 1 ns;
31 if (ZHANG_SEPTMBER1_pout = '0') then
32 error <= '1';
33 end if;
34 wait for 200 ns;
35 ZHANG_SEPTMBER1_p0 <= '0';
36 ZHANG_SEPTMBER1_p1 <= '1';
37 wait for 1 ns;
38 if (ZHANG_SEPTMBER1_pout = '1') then
39 error <= '1';
40 end if;
41 wait for 200 ns;
42 ZHANG_SEPTMBER1_p0 <= '0';
43 ZHANG_SEPTMBER1_p1 <= '0';
44 wait for 1 ns;
45 if (ZHANG_SEPTMBER1_pout = '0') then
46 error <= '1';
47 end if;
48 wait for 200 ns;
49 if (error = '0') then
50 report "No errors detected. Simulation successful" severity failure;
51 else
52 report "Error detected" severity failure;
53 end if;
54 end process;
55 end ZHANG_SEPTMBER1_arch_test;
56
VHSIC Hardware Description Language file length : 1,508 lines : 56 Ln:1 Col:1 Pos:1 Windows (CR.LF) UTF-8 INS
```

This here is the VHDL code for the test bench of the 1-bit comparator

Task 0 : 1-bit comparator , Chue Zhang

The screenshot displays the ModelSim interface for a 1-bit comparator test bench. The main window shows the VHDL code for the test bench, which is a process named `ut` that maps the `ZHANG_SEPTMBER1` entity to a test bench. The code includes initialization of signals, a loop of test cases, and error reporting.

```
17 ut: ZHANG_SEPTMBER1_equal port map (ZHANG_SEPTMBER1_I0 => ZHANG_SEPTMBER1_p0, ZHANG_SEPTMBER1_I1 => ZHANG_SEPTMBER1_p1, ZHANG_SEPTMBER1_Eq => ZHANG_
18 process
19 begin
20   ZHANG_SEPTMBER1_p0 <= '1';
21   ZHANG_SEPTMBER1_p1 <= '0';
22   wait for 1 ns;
23   if (ZHANG_SEPTMBER1_pout = '1') then
24     error <= '1';
25   end if;
26   wait for 200 ns;
27   ZHANG_SEPTMBER1_p0 <= '1';
28   ZHANG_SEPTMBER1_p1 <= '1';
29   wait for 1 ns;
30   if (ZHANG_SEPTMBER1_pout = '0') then
31     error <= '1';
32   end if;
33   wait for 200 ns;
34   ZHANG_SEPTMBER1_p0 <= '0';
35   ZHANG_SEPTMBER1_p1 <= '1';
36   wait for 1 ns;
37   if (ZHANG_SEPTMBER1_pout = '1') then
38     error <= '1';
39   end if;
40   wait for 200 ns;
41   ZHANG_SEPTMBER1_p0 <= '0';
42   ZHANG_SEPTMBER1_p1 <= '0';
43   wait for 1 ns;
44   if (ZHANG_SEPTMBER1_pout = '0') then
45     error <= '1';
46   end if;
47   wait for 200 ns;
48   if (error = '0') then
49     report "No errors detected. Simulation successful" severity failure;
50   else
51     report "Error detected" severity failure;
52   end if;
53 end process;
54 end ZHANG_SEPTMBER1_arch_test;
55
56
```

The left pane shows the design hierarchy with the test bench components. The bottom pane shows the simulation transcript, which confirms that no errors were detected during the simulation.

```

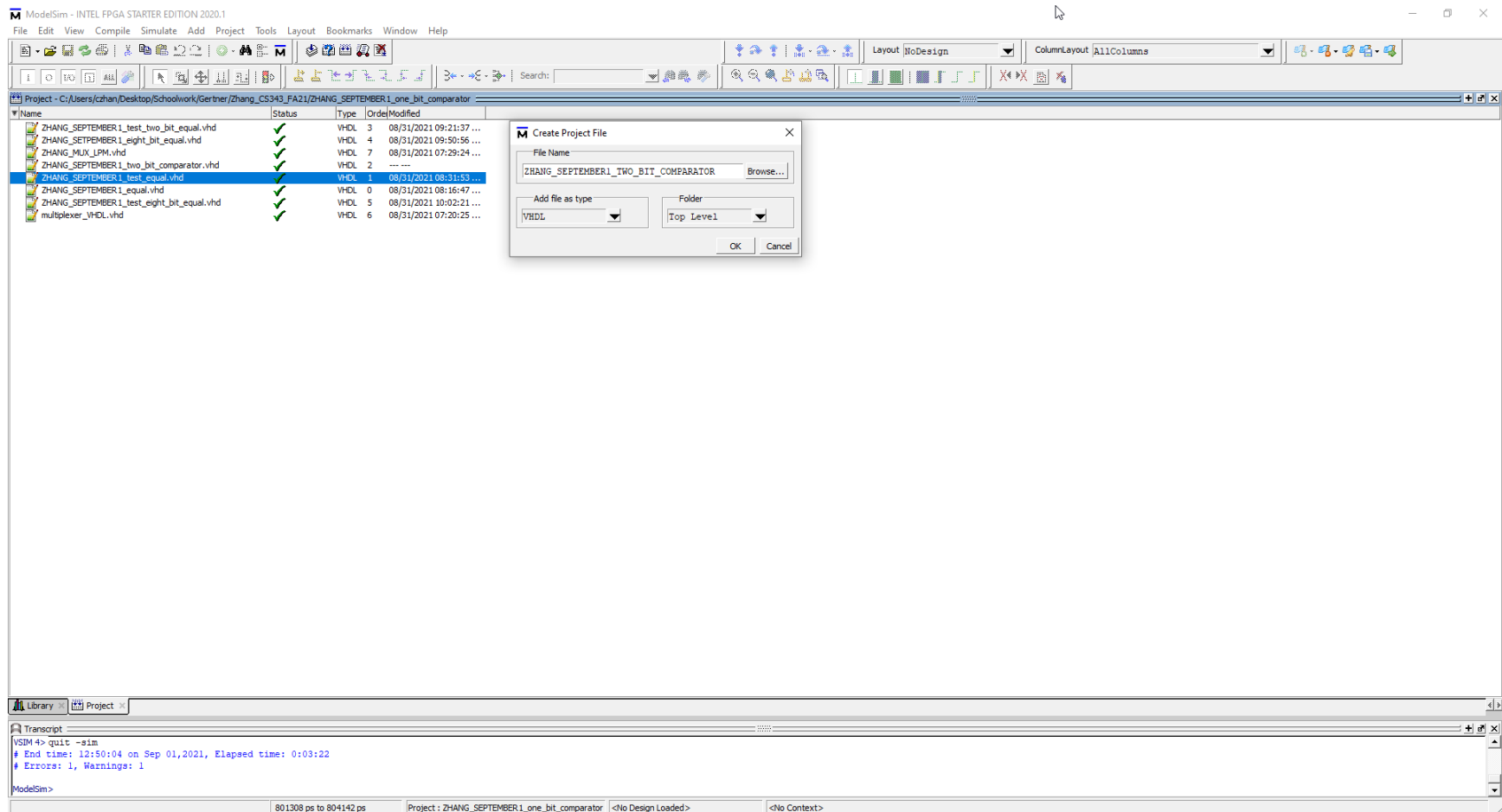
# Start time: 12:46:42 on Sep 01, 2021
# Loading std.standard
# Loading std.textio(body)
# Loading ieee.std_logic_1164(body)
# Loading work.zhang_september1_test_equal(zhang_september1_arch_test)
# Loading work.zhang_september1_equal(zhang_september1_arch)
add wave -position insertpoint sim:/zhang_september1_test_equal/*
VSI3M> run -all
# ** Failure: No errors detected. Simulation successful
# Time: 804 ns Iteration: 0 Process: /zhang_september1_test_equal/line_19 File: C:/Users/czhan/Desktop/Schoolwork/Gertner/Zhang_CS343_FA21/ZHANG_SEPTMBER1_test_equal.vhd
# Break in Process line_19 at C:/Users/czhan/Desktop/Schoolwork/Gertner/Zhang_CS343_FA21/ZHANG_SEPTMBER1_test_equal.vhd line 49
VSI3M>

```

The status bar at the bottom indicates the current position in the code: Ln: 49 Col: 0, READ, 801308 ps to 804142 ps, Project: ZHANG_SEPTMBER1_one_bit_comparator, Now: 804 ns Delta: 0, sim:/zhang_september1_test_equal/line_19.

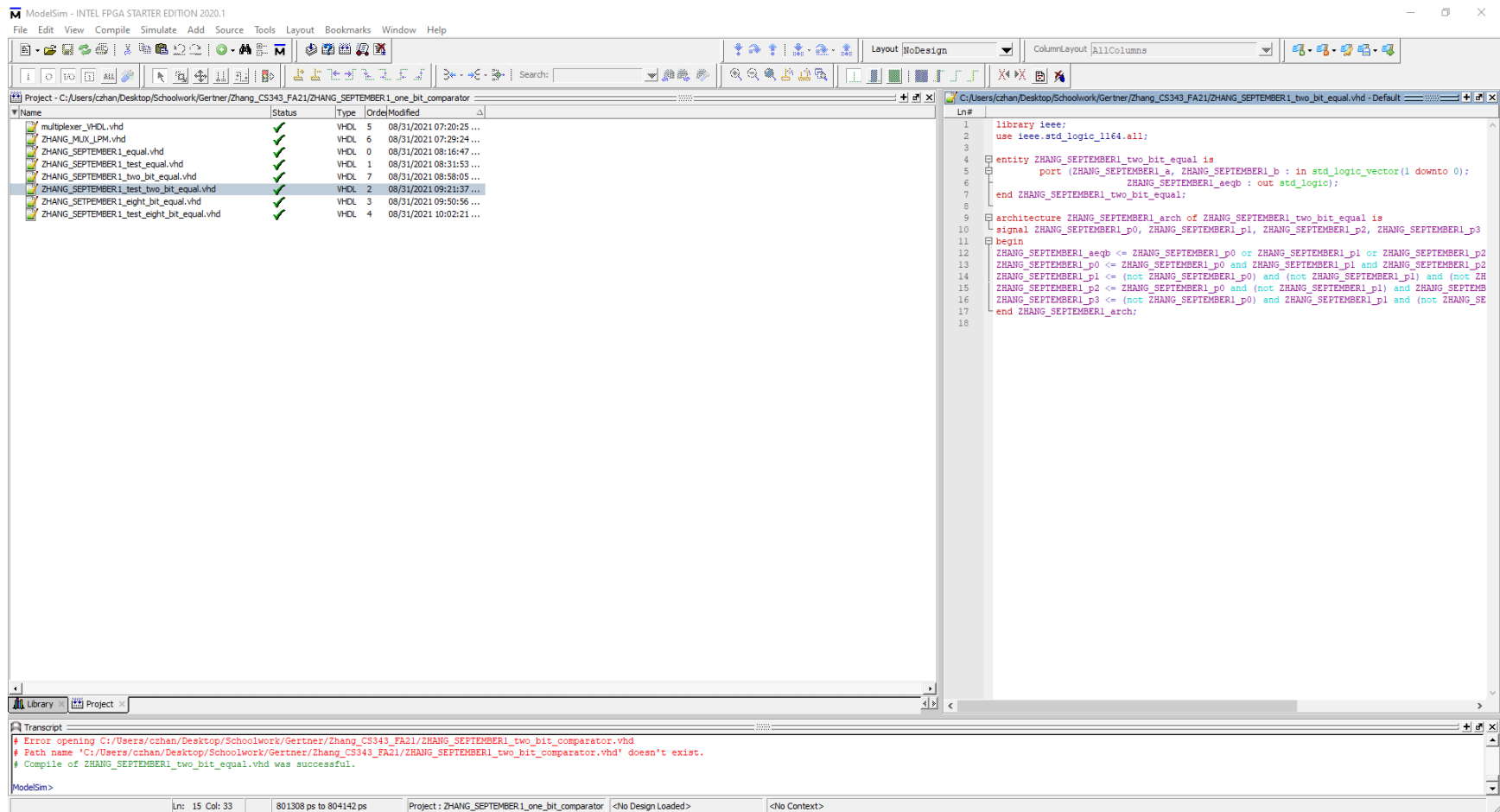
Verification of correctness through the use of test bench. In VHDL code, there is an arrow pointing to the line stating that there were no errors detected.

Task 1, Chue Zhang



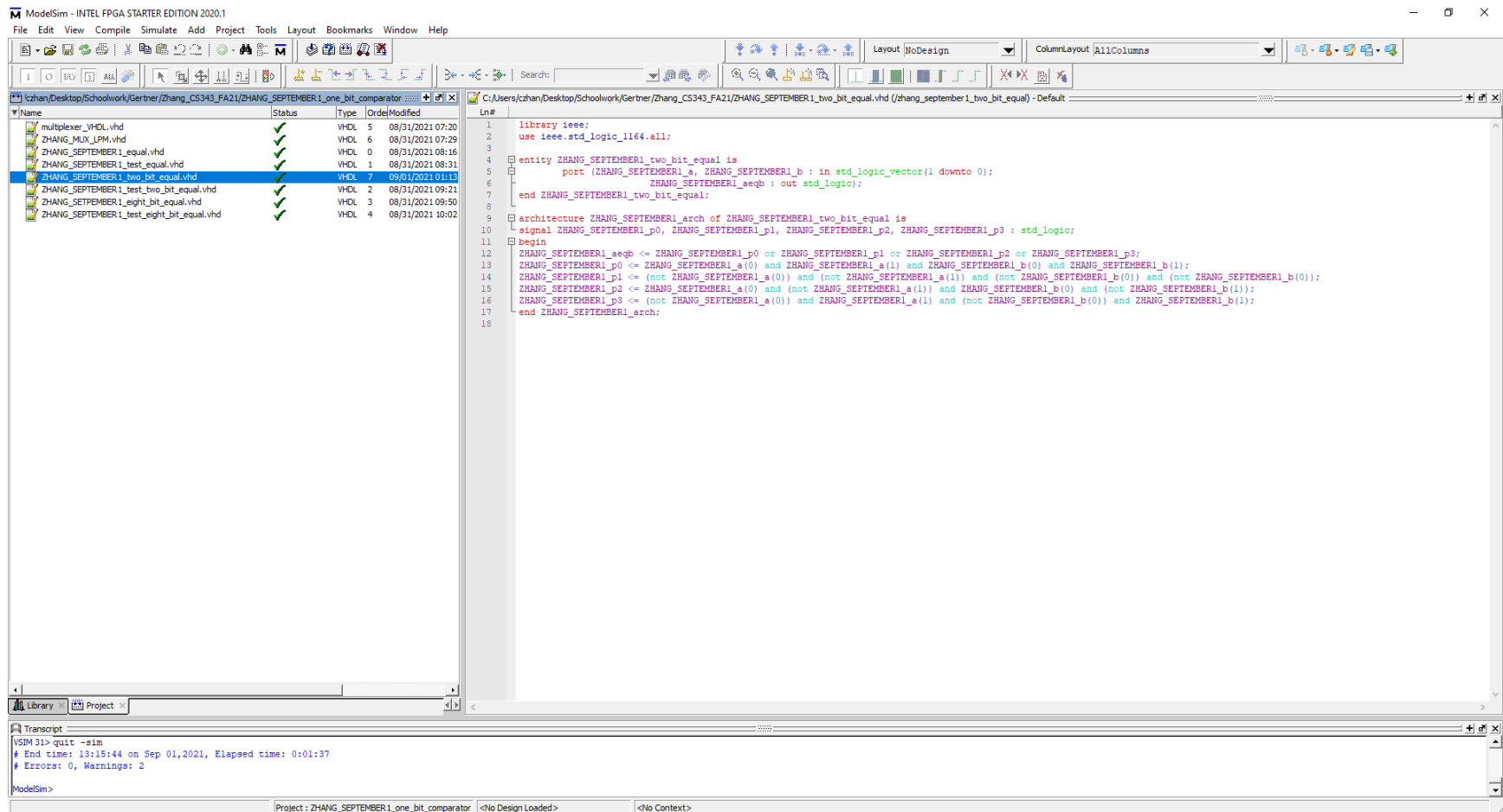
I first create a new file for the 2-bit comparator

Task 1 : 2-bit Comparator, Chue Zhang



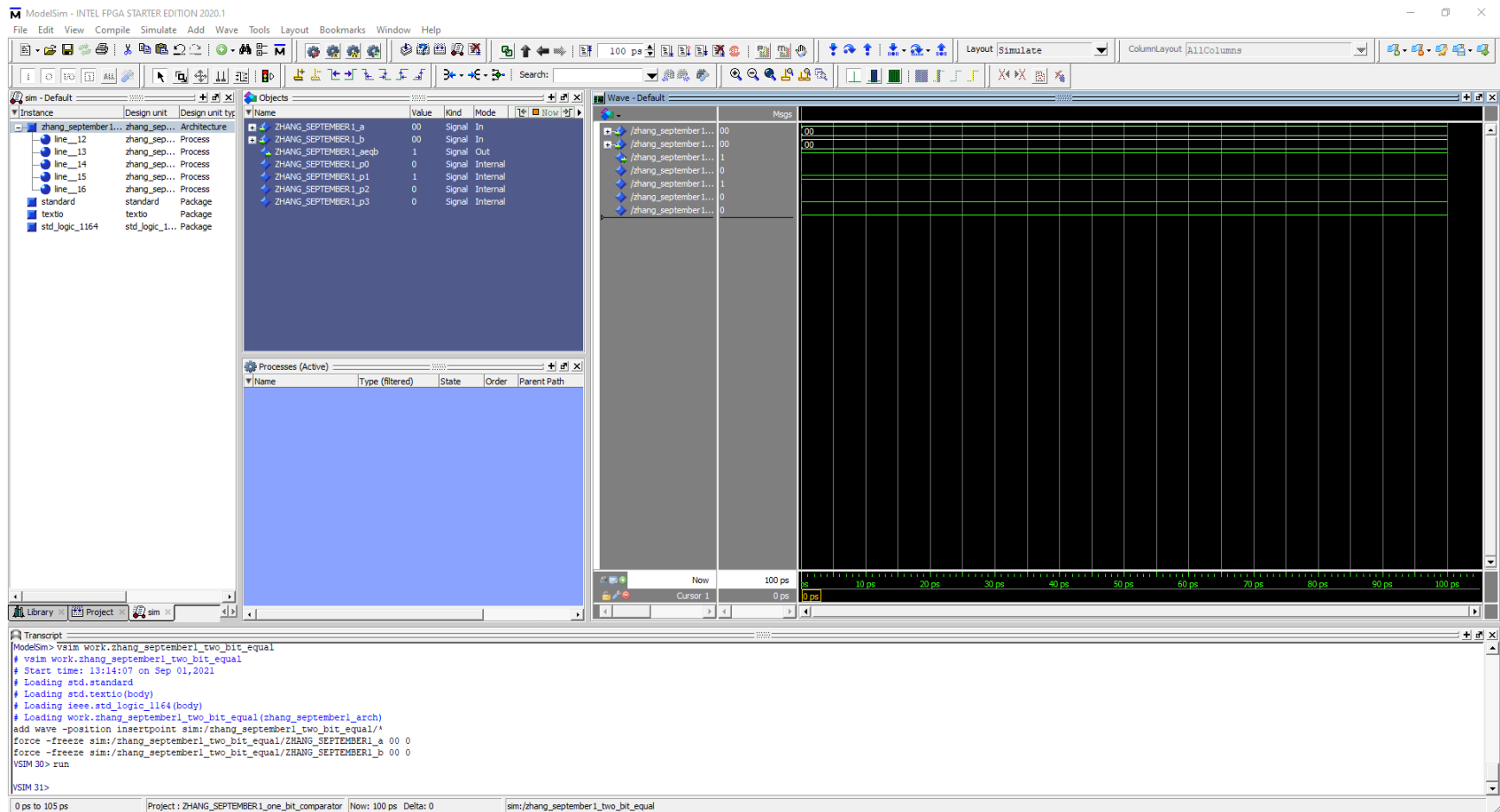
I double click the file and begin writing my VHDL code as seen on the right

Task 1 : 2-bit Comparator, Chue Zhang



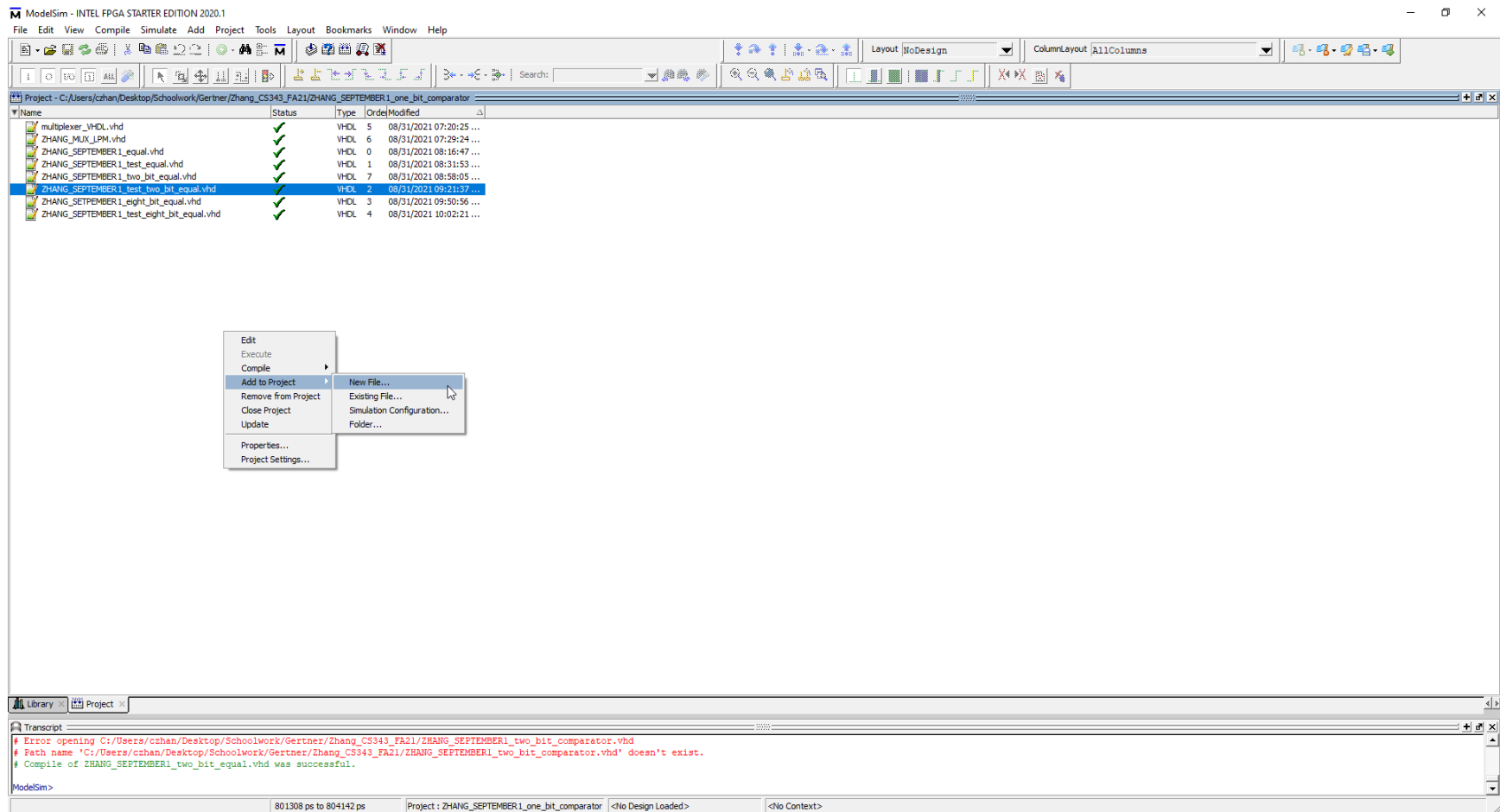
I select the two bit comparator VHDL file and right click → compile → compile selected. At the bottom it should show GREEN with no errors stating that the VHDL file was compiled successfully

Task 1 : 2-bit Comparator, Chue Zhang



In this figure, what is shown is the waveform model for testing the inputs 00,00 which shows the appropriate output

Task 1 : 2-bit Comparator, Chue Zhang



I am now going to create a new file for the test bench

Task 1 : 2-bit Comparator, Chue Zhang

ModelSim - INTEL FPGA STARTER EDITION 2020.1

File Edit View Compile Simulate Add Source Tools Layout Bookmarks Window Help

Layout NoDesign ColumnLayout AllColumns

Search:

File Name Status Type Order/Modified

File Name	Status	Type	Order/Modified
multiplexer_VHDL.vhd	✓	VHDL	5 08/31/2021 07:20
ZHANG_MUX_LPM.vhd	✓	VHDL	6 08/31/2021 07:29
ZHANG_SEPTMBER1_equal.vhd	✓	VHDL	0 08/31/2021 08:16
ZHANG_SEPTMBER1_test_equal.vhd	✓	VHDL	1 08/31/2021 08:31
ZHANG_SEPTMBER1_two_bit_equal.vhd	✓	VHDL	7 09/01/2021 01:13
ZHANG_SEPTMBER1_test_two_bit_equal.vhd	✓	VHDL	2 08/31/2021 09:21
ZHANG_SEPTMBER1_eight_bit_equal.vhd	✓	VHDL	3 08/31/2021 09:50
ZHANG_SEPTMBER1_test_eight_bit_equal.vhd	✓	VHDL	4 08/31/2021 10:02

C:\Users\zhan\Desktop\Schoolwork\Gertner\Zhang_CS343_FA21\ZHANG_SEPTMBER1_test_two_bit_equal.vhd - Default

```
Ln#
1 use ieee.std_logic_1164.all;
2
3 entity ZHANG_SEPTMBER1_test_two_bit_equal is
4   end ZHANG_SEPTMBER1_test_two_bit_equal;
5
6
7 architecture ZHANG_SEPTMBER1_arch_test of ZHANG_SEPTMBER1_test_two_bit_equal is
8   component ZHANG_SEPTMBER1_two_bit_equal
9     port (ZHANG_SEPTMBER1_a, ZHANG_SEPTMBER1_b : in std_logic_vector(1 downto 0);
10          ZHANG_SEPTMBER1_aeqb : out std_logic);
11
12   end component;
13
14 signal ZHANG_SEPTMBER1_p1, ZHANG_SEPTMBER1_p0 : std_logic_vector ( 1 downto 0 );
15 signal ZHANG_SEPTMBER1_pout : std_logic;
16 signal ZHANG_SEPTMBER1_error: std_logic := '0';
17 begin
18   uut: ZHANG_SEPTMBER1_two_bit_equal port map( ZHANG_SEPTMBER1_a => ZHANG_SEPTMBER1_p0,
19                                               ZHANG_SEPTMBER1_b => ZHANG_SEPTMBER1_p1,
20                                               ZHANG_SEPTMBER1_aeqb => ZHANG_SEPTMBER1_pout);
21
22   process
23   begin
24     ZHANG_SEPTMBER1_p0 <= "00";
25     ZHANG_SEPTMBER1_p1 <= "00";
26
27     wait for 1 ns;
28     if (ZHANG_SEPTMBER1_pout = '0') then
29       ZHANG_SEPTMBER1_error <= '1';
30     end if;
31     wait for 200 ns;
32
33     ZHANG_SEPTMBER1_p0 <= "01";
34     ZHANG_SEPTMBER1_p1 <= "00";
35
36     wait for 1 ns;
37     if (ZHANG_SEPTMBER1_pout = '1') then
38       ZHANG_SEPTMBER1_error <= '1';
39     end if;
40     wait for 200 ns;
41
42     ZHANG_SEPTMBER1_p0 <= "01";
43     ZHANG_SEPTMBER1_p1 <= "11";
44
45     wait for 1 ns;
46     if (ZHANG_SEPTMBER1_pout = '1') then
47       ZHANG_SEPTMBER1_error <= '1';
48     end if;
49     wait for 200 ns;
50
51   end process
```

Transcript

```
# Errors: 0, Warnings: 2
# Compile of ZHANG_SEPTMBER1_test_two_bit_equal.vhd was successful.
# Load canceled
```

ModelSim>

Ln: 1 Col: 0 Project: ZHANG_SEPTMBER1_one_bit_comparator <No Design Loaded> 08/31/2021 09:50:56 pm

Over here, I have the written test bench code and I will now proceed to compile to check for correctness in code.

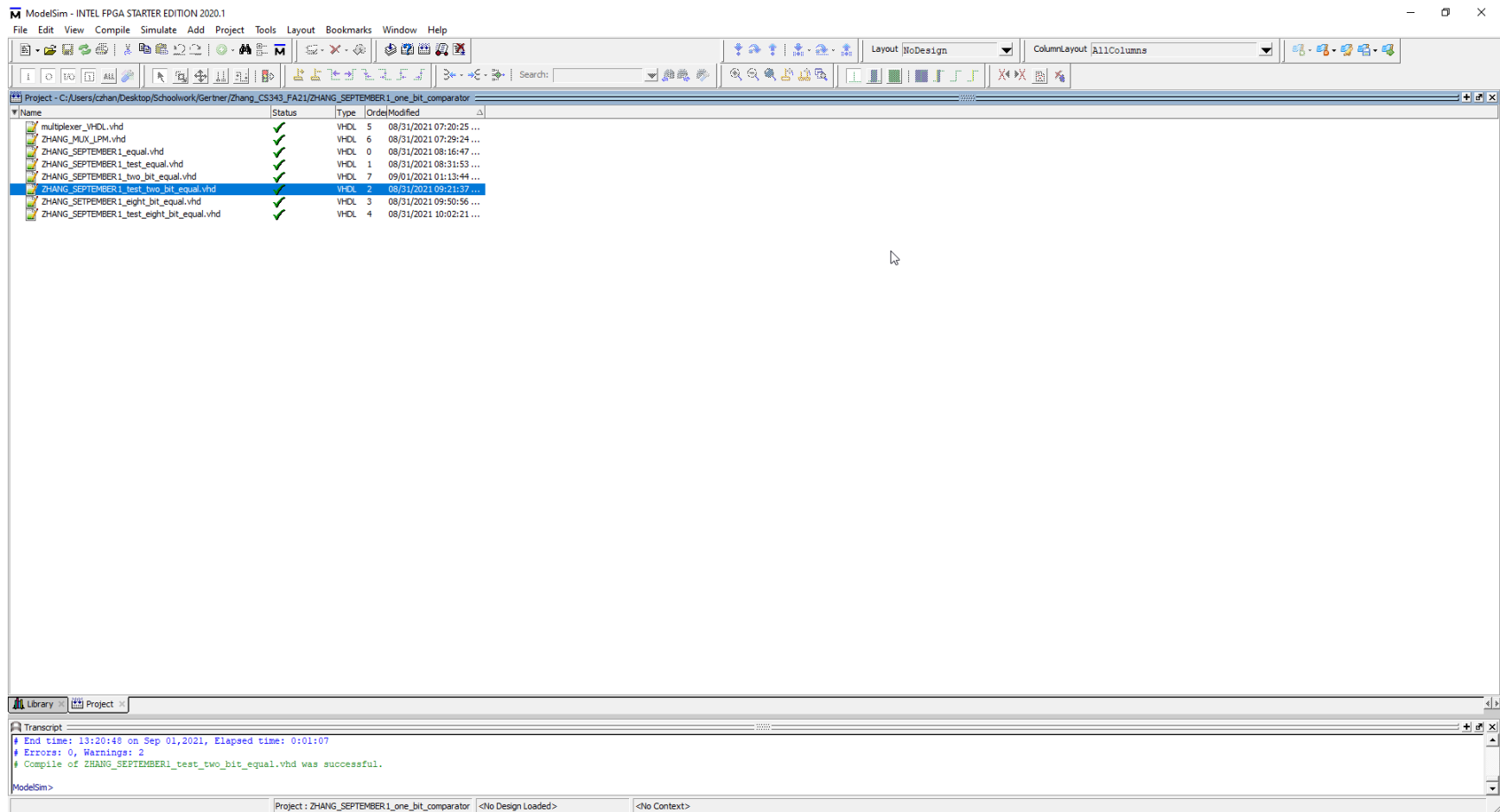
Task 1 : 2-bit Comparator, Chue Zhang

The image shows a screenshot of a VHDL code editor window. The title bar indicates the file path is C:\Users\zchen\Desktop\Schoolwork\Gertner\Zhang_CS343_FA21\ZHANG_SEPTMBER1_test_two_bit_equal.vhd. The editor displays the source code for a testbench named ZHANG_SEPTMBER1_test_two_bit_equal.vhd. The code is written in VHDL and includes several components and signals. The main logic involves comparing two 32-bit numbers, ZHANG_SEPTMBER1_test_two_bit_equal, and checking for equality. The code includes a series of test cases, each with a wait statement and a check for the equality signal. The code is organized into sections for component declarations, signal declarations, and test cases. The test cases are numbered 1 through 10, each with a wait statement and a check for the equality signal. The code is written in a standard VHDL syntax, with comments and indentation used to structure the code. The editor window also shows a status bar at the bottom with the text 'VHIC Hardware Description Language file', 'length: 2,480 lines: 103', and 'Ln: 1 Col: 1 Pos: 1'. The status bar also indicates the current window is 'Windows (CR LF)' and the encoding is 'UTF-8'.

```
1 library IEEE;
2 use IEEE.Std_Logic_1164.all;
3
4 component ZHANG_SEPTMBER1_test_two_bit_equal is
5     port (ZHANG_SEPTMBER1_test_two_bit_equal: out std_logic);
6 end component;
7
8 component ZHANG_SEPTMBER1_test_two_bit_equal is
9     port (ZHANG_SEPTMBER1_test_two_bit_equal: out std_logic);
10 end component;
11
12 component ZHANG_SEPTMBER1_test_two_bit_equal is
13     port (ZHANG_SEPTMBER1_test_two_bit_equal: out std_logic);
14 end component;
15
16 component ZHANG_SEPTMBER1_test_two_bit_equal is
17     port (ZHANG_SEPTMBER1_test_two_bit_equal: out std_logic);
18 end component;
19
20 component ZHANG_SEPTMBER1_test_two_bit_equal is
21     port (ZHANG_SEPTMBER1_test_two_bit_equal: out std_logic);
22 end component;
23
24 component ZHANG_SEPTMBER1_test_two_bit_equal is
25     port (ZHANG_SEPTMBER1_test_two_bit_equal: out std_logic);
26 end component;
27
28 component ZHANG_SEPTMBER1_test_two_bit_equal is
29     port (ZHANG_SEPTMBER1_test_two_bit_equal: out std_logic);
30 end component;
31
32 component ZHANG_SEPTMBER1_test_two_bit_equal is
33     port (ZHANG_SEPTMBER1_test_two_bit_equal: out std_logic);
34 end component;
35
36 component ZHANG_SEPTMBER1_test_two_bit_equal is
37     port (ZHANG_SEPTMBER1_test_two_bit_equal: out std_logic);
38 end component;
39
40 component ZHANG_SEPTMBER1_test_two_bit_equal is
41     port (ZHANG_SEPTMBER1_test_two_bit_equal: out std_logic);
42 end component;
43
44 component ZHANG_SEPTMBER1_test_two_bit_equal is
45     port (ZHANG_SEPTMBER1_test_two_bit_equal: out std_logic);
46 end component;
47
48 component ZHANG_SEPTMBER1_test_two_bit_equal is
49     port (ZHANG_SEPTMBER1_test_two_bit_equal: out std_logic);
50 end component;
51
52 component ZHANG_SEPTMBER1_test_two_bit_equal is
53     port (ZHANG_SEPTMBER1_test_two_bit_equal: out std_logic);
54 end component;
55
56 component ZHANG_SEPTMBER1_test_two_bit_equal is
57     port (ZHANG_SEPTMBER1_test_two_bit_equal: out std_logic);
58 end component;
59
60 component ZHANG_SEPTMBER1_test_two_bit_equal is
61     port (ZHANG_SEPTMBER1_test_two_bit_equal: out std_logic);
62 end component;
63
64 component ZHANG_SEPTMBER1_test_two_bit_equal is
65     port (ZHANG_SEPTMBER1_test_two_bit_equal: out std_logic);
66 end component;
67
68 component ZHANG_SEPTMBER1_test_two_bit_equal is
69     port (ZHANG_SEPTMBER1_test_two_bit_equal: out std_logic);
70 end component;
71
72 component ZHANG_SEPTMBER1_test_two_bit_equal is
73     port (ZHANG_SEPTMBER1_test_two_bit_equal: out std_logic);
74 end component;
75
76 component ZHANG_SEPTMBER1_test_two_bit_equal is
77     port (ZHANG_SEPTMBER1_test_two_bit_equal: out std_logic);
78 end component;
79
80 component ZHANG_SEPTMBER1_test_two_bit_equal is
81     port (ZHANG_SEPTMBER1_test_two_bit_equal: out std_logic);
82 end component;
83
84 component ZHANG_SEPTMBER1_test_two_bit_equal is
85     port (ZHANG_SEPTMBER1_test_two_bit_equal: out std_logic);
86 end component;
87
88 component ZHANG_SEPTMBER1_test_two_bit_equal is
89     port (ZHANG_SEPTMBER1_test_two_bit_equal: out std_logic);
90 end component;
91
92 component ZHANG_SEPTMBER1_test_two_bit_equal is
93     port (ZHANG_SEPTMBER1_test_two_bit_equal: out std_logic);
94 end component;
95
96 component ZHANG_SEPTMBER1_test_two_bit_equal is
97     port (ZHANG_SEPTMBER1_test_two_bit_equal: out std_logic);
98 end component;
99
100 component ZHANG_SEPTMBER1_test_two_bit_equal is
101     port (ZHANG_SEPTMBER1_test_two_bit_equal: out std_logic);
102 end component;
103
104 component ZHANG_SEPTMBER1_test_two_bit_equal is
105     port (ZHANG_SEPTMBER1_test_two_bit_equal: out std_logic);
106 end component;
107
108 component ZHANG_SEPTMBER1_test_two_bit_equal is
109     port (ZHANG_SEPTMBER1_test_two_bit_equal: out std_logic);
110 end component;
111
112 component ZHANG_SEPTMBER1_test_two_bit_equal is
113     port (ZHANG_SEPTMBER1_test_two_bit_equal: out std_logic);
114 end component;
115
116 component ZHANG_SEPTMBER1_test_two_bit_equal is
117     port (ZHANG_SEPTMBER1_test_two_bit_equal: out std_logic);
118 end component;
119
120 component ZHANG_SEPTMBER1_test_two_bit_equal is
121     port (ZHANG_SEPTMBER1_test_two_bit_equal: out std_logic);
122 end component;
123
124 component ZHANG_SEPTMBER1_test_two_bit_equal is
125     port (ZHANG_SEPTMBER1_test_two_bit_equal: out std_logic);
126 end component;
127
128 component ZHANG_SEPTMBER1_test_two_bit_equal is
129     port (ZHANG_SEPTMBER1_test_two_bit_equal: out std_logic);
130 end component;
131
132 component ZHANG_SEPTMBER1_test_two_bit_equal is
133     port (ZHANG_SEPTMBER1_test_two_bit_equal: out std_logic);
134 end component;
135
136 component ZHANG_SEPTMBER1_test_two_bit_equal is
137     port (ZHANG_SEPTMBER1_test_two_bit_equal: out std_logic);
138 end component;
139
140 component ZHANG_SEPTMBER1_test_two_bit_equal is
141     port (ZHANG_SEPTMBER1_test_two_bit_equal: out std_logic);
142 end component;
143
144 component ZHANG_SEPTMBER1_test_two_bit_equal is
145     port (ZHANG_SEPTMBER1_test_two_bit_equal: out std_logic);
146 end component;
147
148 component ZHANG_SEPTMBER1_test_two_bit_equal is
149     port (ZHANG_SEPTMBER1_test_two_bit_equal: out std_logic);
150 end component;
151
152 component ZHANG_SEPTMBER1_test_two_bit_equal is
153     port (ZHANG_SEPTMBER1_test_two_bit_equal: out std_logic);
154 end component;
155
156 component ZHANG_SEPTMBER1_test_two_bit_equal is
157     port (ZHANG_SEPTMBER1_test_two_bit_equal: out std_logic);
158 end component;
159
160 component ZHANG_SEPTMBER1_test_two_bit_equal is
161     port (ZHANG_SEPTMBER1_test_two_bit_equal: out std_logic);
162 end component;
163
164 component ZHANG_SEPTMBER1_test_two_bit_equal is
165     port (ZHANG_SEPTMBER1_test_two_bit_equal: out std_logic);
166 end component;
167
168 component ZHANG_SEPTMBER1_test_two_bit_equal is
169     port (ZHANG_SEPTMBER1_test_two_bit_equal: out std_logic);
170 end component;
171
172 component ZHANG_SEPTMBER1_test_two_bit_equal is
173     port (ZHANG_SEPTMBER1_test_two_bit_equal: out std_logic);
174 end component;
175
176 component ZHANG_SEPTMBER1_test_two_bit_equal is
177     port (ZHANG_SEPTMBER1_test_two_bit_equal: out std_logic);
178 end component;
179
180 component ZHANG_SEPTMBER1_test_two_bit_equal is
181     port (ZHANG_SEPTMBER1_test_two_bit_equal: out std_logic);
182 end component;
183
184 component ZHANG_SEPTMBER1_test_two_bit_equal is
185     port (ZHANG_SEPTMBER1_test_two_bit_equal: out std_logic);
186 end component;
187
188 component ZHANG_SEPTMBER1_test_two_bit_equal is
189     port (ZHANG_SEPTMBER1_test_two_bit_equal: out std_logic);
190 end component;
191
192 component ZHANG_SEPTMBER1_test_two_bit_equal is
193     port (ZHANG_SEPTMBER1_test_two_bit_equal: out std_logic);
194 end component;
195
196 component ZHANG_SEPTMBER1_test_two_bit_equal is
197     port (ZHANG_SEPTMBER1_test_two_bit_equal: out std_logic);
198 end component;
199
200 component ZHANG_SEPTMBER1_test_two_bit_equal is
201     port (ZHANG_SEPTMBER1_test_two_bit_equal: out std_logic);
202 end component;
203
204 component ZHANG_SEPTMBER1_test_two_bit_equal is
205     port (ZHANG_SEPTMBER1_test_two_bit_equal: out std_logic);
206 end component;
207
208 component ZHANG_SEPTMBER1_test_two_bit_equal is
209     port (ZHANG_SEPTMBER1_test_two_bit_equal: out std_logic);
210 end component;
211
212 component ZHANG_SEPTMBER1_test_two_bit_equal is
213     port (ZHANG_SEPTMBER1_test_two_bit_equal: out std_logic);
214 end component;
215
216 component ZHANG_SEPTMBER1_test_two_bit_equal is
217     port (ZHANG_SEPTMBER1_test_two_bit_equal: out std_logic);
218 end component;
219
220 component ZHANG_SEPTMBER1_test_two_bit_equal is
221     port (ZHANG_SEPTMBER1_test_two_bit_equal: out std_logic);
222 end component;
223
224 component ZHANG_SEPTMBER1_test_two_bit_equal is
225     port (ZHANG_SEPTMBER1_test_two_bit_equal: out std_logic);
226 end component;
227
228 component ZHANG_SEPTMBER1_test_two_bit_equal is
229     port (ZHANG_SEPTMBER1_test_two_bit_equal: out std_logic);
230 end component;
231
232 component ZHANG_SEPTMBER1_test_two_bit_equal is
233     port (ZHANG_SEPTMBER1_test_two_bit_equal: out std_logic);
234 end component;
235
236 component ZHANG_SEPTMBER1_test_two_bit_equal is
237     port (ZHANG_SEPTMBER1_test_two_bit_equal: out std_logic);
238 end component;
239
240 component ZHANG_SEPTMBER1_test_two_bit_equal is
241     port (ZHANG_SEPTMBER1_test_two_bit_equal: out std_logic);
242 end component;
243
244 component ZHANG_SEPTMBER1_test_two_bit_equal is
245     port (ZHANG_SEPTMBER1_test_two_bit_equal: out std_logic);
246 end component;
247
248 component ZHANG_SEPTMBER1_test_two_bit_equal is
249     port (ZHANG_SEPTMBER1_test_two_bit_equal: out std_logic);
250 end component;
251
252 component ZHANG_SEPTMBER1_test_two_bit_equal is
253     port (ZHANG_SEPTMBER1_test_two_bit_equal: out std_logic);
254 end component;
255
256 component ZHANG_SEPTMBER1_test_two_bit_equal is
257     port (ZHANG_SEPTMBER1_test_two_bit_equal: out std_logic);
258 end component;
259
260 component ZHANG_SEPTMBER1_test_two_bit_equal is
261     port (ZHANG_SEPTMBER1_test_two_bit_equal: out std_logic);
262 end component;
263
264 component ZHANG_SEPTMBER1_test_two_bit_equal is
265     port (ZHANG_SEPTMBER1_test_two_bit_equal: out std_logic);
266 end component;
267
268 component ZHANG_SEPTMBER1_test_two_bit_equal is
269     port (ZHANG_SEPTMBER1_test_two_bit_equal: out std_logic);
270 end component;
271
272 component ZHANG_SEPTMBER1_test_two_bit_equal is
273     port (ZHANG_SEPTMBER1_test_two_bit_equal: out std_logic);
274 end component;
275
276 component ZHANG_SEPTMBER1_test_two_bit_equal is
277     port (ZHANG_SEPTMBER1_test_two_bit_equal: out std_logic);
278 end component;
279
280 component ZHANG_SEPTMBER1_test_two_bit_equal is
281     port (ZHANG_SEPTMBER1_test_two_bit_equal: out std_logic);
282 end component;
283
284 component ZHANG_SEPTMBER1_test_two_bit_equal is
285     port (ZHANG_SEPTMBER1_test_two_bit_equal: out std_logic);
286 end component;
287
288 component ZHANG_SEPTMBER1_test_two_bit_equal is
289     port (ZHANG_SEPTMBER1_test_two_bit_equal: out std_logic);
290 end component;
291
292 component ZHANG_SEPTMBER1_test_two_bit_equal is
293     port (ZHANG_SEPTMBER1_test_two_bit_equal: out std_logic);
294 end component;
295
296 component ZHANG_SEPTMBER1_test_two_bit_equal is
297     port (ZHANG_SEPTMBER1_test_two_bit_equal: out std_logic);
298 end component;
299
300 component ZHANG_SEPTMBER1_test_two_bit_equal is
301     port (ZHANG_SEPTMBER1_test_two_bit_equal: out std_logic);
302 end component;
303
304 component ZHANG_SEPTMBER1_test_two_bit_equal is
305     port (ZHANG_SEPTMBER1_test_two_bit_equal: out std_logic);
306 end component;
307
308 component ZHANG_SEPTMBER1_test_two_bit
```

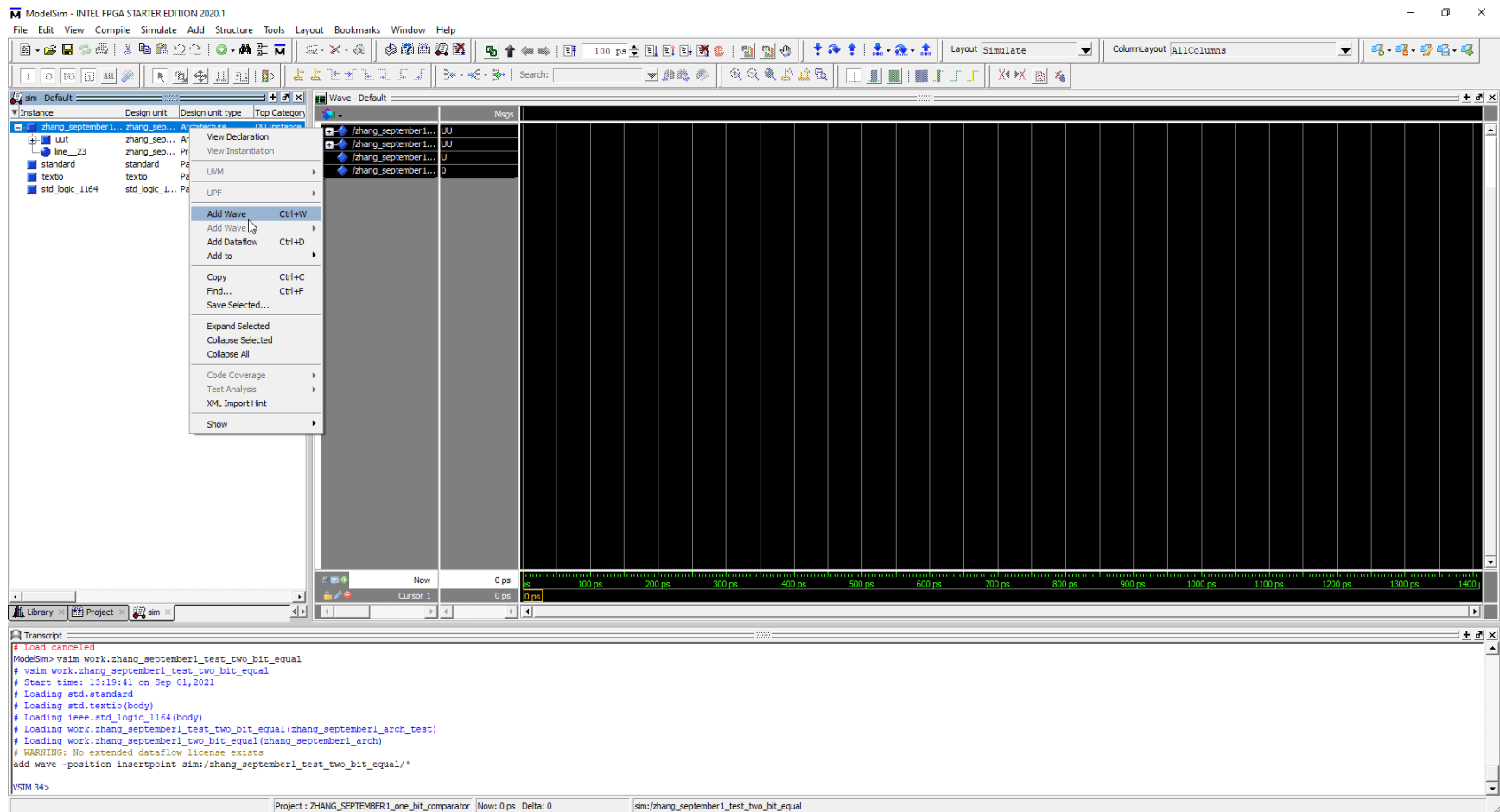
This is the entire code in a screen shot

Task 1 : 2-bit Comparator, Chue Zhang



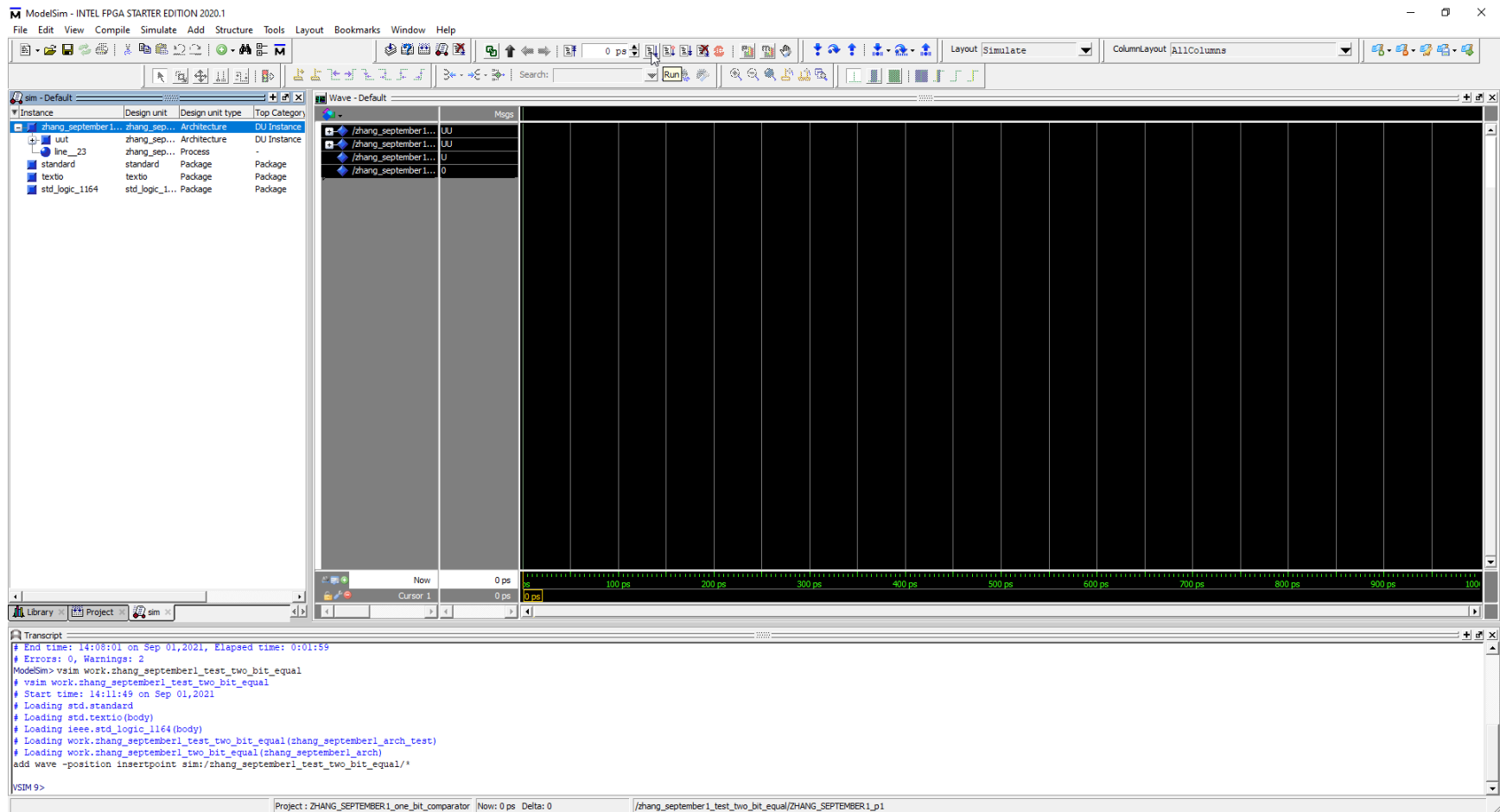
Compilation successful, will proceed to simulation on model sim

Task 1 : 2-bit Comparator, Chue Zhang



In modelsim I add the waves by pressing right click → add wave

Task 1 : 2-bit Comparator, Chue Zhang



Appropriate waves have been added and I proceed to run-all

Task 1 : 2-bit Comparator, Chue Zhang

The screenshot displays the ModelSim interface for a 2-bit comparator test bench. The left pane shows the project hierarchy with the test bench file selected. The main window shows the VHDL code for the test bench, which includes two test cases for the comparator. The bottom pane shows the simulation transcript, which confirms that the simulation was successful with no errors detected.

Simulation Transcript:

```
# Start time: 13:23:26 on Sep 01, 2021
# Loading std.standard
# Loading std.textio(body)
# Loading ieee.std_logic_1164(body)
# Loading work.zhang_september1_test_two_bit_equal(zhang_september1_arch_test)
# Loading work.zhang_september1_test_two_bit_equal(zhang_september1_arch)
add wave -position insertpoint sim:/zhang_september1_test_two_bit_equal/*
VSI3> run -all
# ** Failure: No errors detected. Simulation successful
# Time: 1608 ns Iteration: 0 Process: /zhang_september1_test_two_bit_equal/line_23 File: C:/Users/cchan/Desktop/Schoolwork/Gertner/Zhang_CS343_FA21/ZHANG_SEPTMBER1_test_two_bit_equal.vhd
# Break in Process line_23 at C:/Users/cchan/Desktop/Schoolwork/Gertner/Zhang_CS343_FA21/ZHANG_SEPTMBER1_test_two_bit_equal.vhd line 98
VSI4>
```

Project Hierarchy:

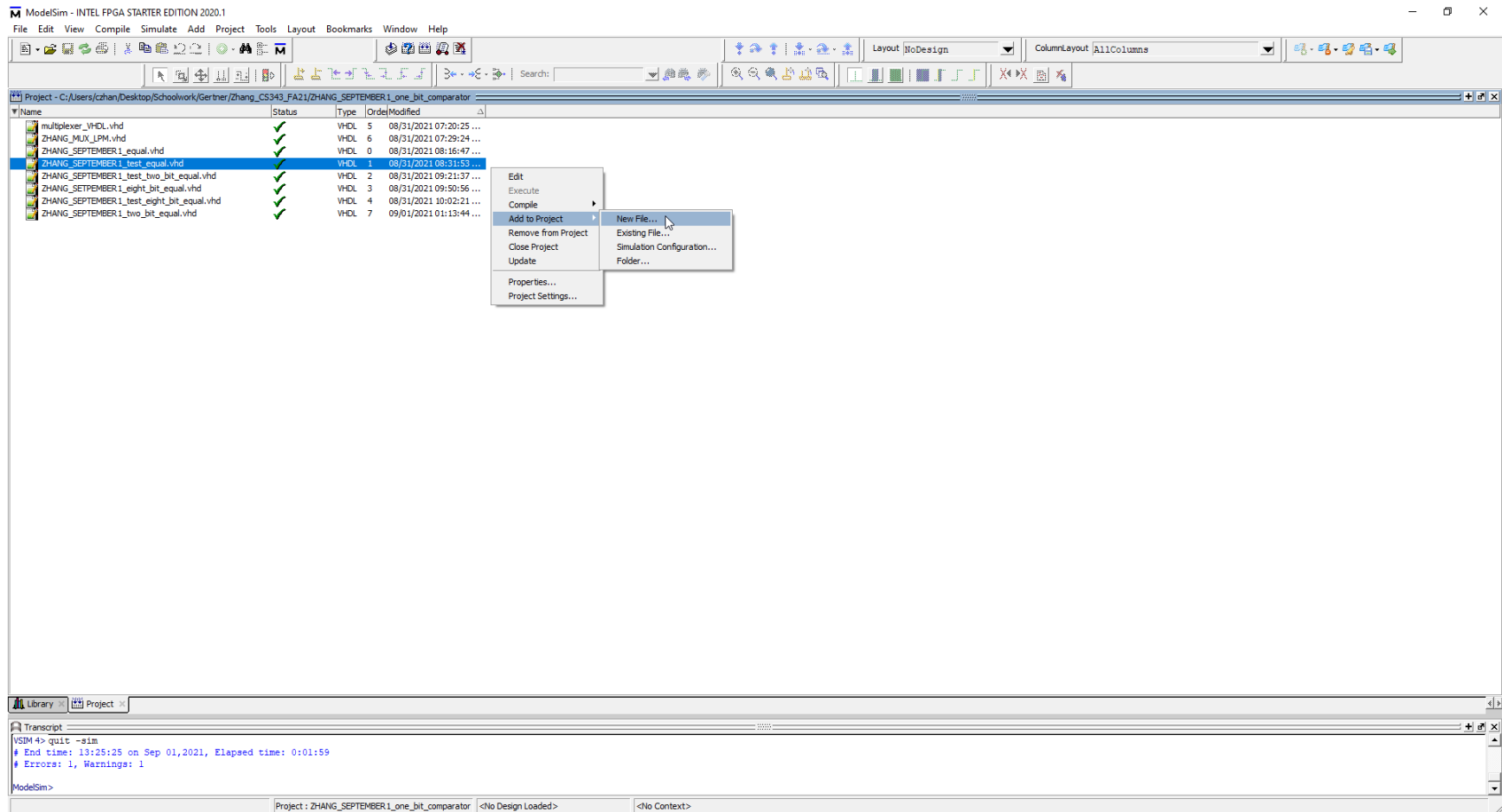
Instance	Design unit	Design unit type	Top Category
zhang_september1...	zhang_sep...	Architecture	DU Instance
uit	zhang_sep...	Architecture	DU Instance
line_23	zhang_sep...	Process	-
standard	standard	Package	Package
textio	textio	Package	Package
std_logic_1164	std_logic_1...	Package	Package

VHDL Code Snippets:

```
64 wait for 1 ns;
65 if (ZHANG_SEPTMBER1_pout = '0') then
66     ZHANG_SEPTMBER1_error <= '1';
67 end if;
68 wait for 200 ns;
69
70 ZHANG_SEPTMBER1_p0 <= "10";
71 ZHANG_SEPTMBER1_p1 <= "11";
72
73 wait for 1 ns;
74 if (ZHANG_SEPTMBER1_pout = '1') then
75     ZHANG_SEPTMBER1_error <= '1';
76 end if;
77 wait for 200 ns;
78
79 ZHANG_SEPTMBER1_p0 <= "10";
80 ZHANG_SEPTMBER1_p1 <= "10";
81
82 wait for 1 ns;
83 if (ZHANG_SEPTMBER1_pout = '0') then
84     ZHANG_SEPTMBER1_error <= '1';
85 end if;
86 wait for 200 ns;
87
88 ZHANG_SEPTMBER1_p0 <= "11";
89 ZHANG_SEPTMBER1_p1 <= "01";
90
91 wait for 1 ns;
92 if (ZHANG_SEPTMBER1_pout = '1') then
93     ZHANG_SEPTMBER1_error <= '1';
94 end if;
95 wait for 200 ns;
96
97 if (ZHANG_SEPTMBER1_error = '0') then
98     report "No errors detected. Simulation successful" severity failure;
99 else
100     report "Error detected" severity failure;
101 end if;
102 end process;
103 end ZHANG_SEPTMBER1_arch_test;
```

I press run all and there is no errors created so test bench is successful.

Task 2 : 8-bit Comparator , Chue Zhang



I am now going to create a new VHDL file for 8 bit comparator

Task 2 : 8-bit Comparator , Chue Zhang

ModelSim - INTEL FPGA STARTER EDITION 2020.1

File Edit View Compile Simulate Add Project Tools Layout Bookmarks Window Help

Layout: NoDesign ColumnLayout: AllColumns

Search:

File Name Status Type Order Modified

File Name	Status	Type	Order	Modified
multiplexer_VHDL.vhd	✓	VHDL	5	08/31/2021 07:20:25...
ZHANG_MUX_LPM.vhd	✓	VHDL	6	08/31/2021 07:29:24...
ZHANG_SEPTMBER1_equal.vhd	✓	VHDL	0	08/31/2021 08:16:47...
ZHANG_SEPTMBER1_test_equal.vhd	✓	VHDL	1	08/31/2021 08:31:53...
ZHANG_SEPTMBER1_test_two_bit_equal.vhd	✓	VHDL	2	08/31/2021 09:21:37...
ZHANG_SEPTMBER1_eight_bit_equal.vhd	✓	VHDL	3	08/31/2021 09:50:56...
ZHANG_SEPTMBER1_test_eight_bit_equal.vhd	✓	VHDL	4	08/31/2021 10:02:21...
ZHANG_SEPTMBER1_two_bit_equal.vhd	✓	VHDL	7	09/01/2021 01:13:44...

C:\Users\chan\Desktop\Schoolwork\Gertner\Zhang_CS343_FA21\ZHANG_SEPTMBER1_eight_bit_equal.vhd - Default

```
1 library ieee;
2 use ieee.std_logic_1164.all;
3
4 entity ZHANG_SEPTMBER1_eight_bit_equal is
5     port (
6         ZHANG_SEPTMBER1_a, ZHANG_SEPTMBER1_b : in std_logic_vector(7 downto 0);
7         ZHANG_SEPTMBER1_aeqb : out std_logic);
8
9 end ZHANG_SEPTMBER1_eight_bit_equal;
10
11 architecture ZHANG_SEPTMBER1_arch of ZHANG_SEPTMBER1_eight_bit_equal is
12
13     component ZHANG_SEPTMBER1_equal
14     port (
15         ZHANG_SEPTMBER1_I0, ZHANG_SEPTMBER1_I1 : in std_logic;
16         ZHANG_SEPTMBER1_Eq : out std_logic);
17     end component;
18
19 signal ZHANG_SEPTMBER1_p0, ZHANG_SEPTMBER1_p1, ZHANG_SEPTMBER1_p2, ZHANG_SEPTMBER1_p3, ZHANG_SEPTMBER1_p4, ZHANG_SEPTMBER1_p5, ZHANG_SEPTMBER1_p6, ZHANG_SEPTMBER1_p7, ZHANG_SEPTMBER1_p8, ZHANG_SEPTMBER1_p9, ZHANG_SEPTMBER1_p10, ZHANG_SEPTMBER1_p11, ZHANG_SEPTMBER1_p12, ZHANG_SEPTMBER1_p13, ZHANG_SEPTMBER1_p14, ZHANG_SEPTMBER1_p15, ZHANG_SEPTMBER1_p16, ZHANG_SEPTMBER1_p17, ZHANG_SEPTMBER1_p18, ZHANG_SEPTMBER1_p19, ZHANG_SEPTMBER1_p20, ZHANG_SEPTMBER1_p21, ZHANG_SEPTMBER1_p22, ZHANG_SEPTMBER1_p23, ZHANG_SEPTMBER1_p24, ZHANG_SEPTMBER1_p25, ZHANG_SEPTMBER1_p26, ZHANG_SEPTMBER1_p27, ZHANG_SEPTMBER1_p28, ZHANG_SEPTMBER1_p29, ZHANG_SEPTMBER1_p30, ZHANG_SEPTMBER1_p31, ZHANG_SEPTMBER1_p32, ZHANG_SEPTMBER1_p33, ZHANG_SEPTMBER1_p34, ZHANG_SEPTMBER1_p35, ZHANG_SEPTMBER1_p36, ZHANG_SEPTMBER1_p37, ZHANG_SEPTMBER1_p38, ZHANG_SEPTMBER1_p39, ZHANG_SEPTMBER1_p40, ZHANG_SEPTMBER1_p41, ZHANG_SEPTMBER1_p42, ZHANG_SEPTMBER1_p43, ZHANG_SEPTMBER1_p44, ZHANG_SEPTMBER1_p45, ZHANG_SEPTMBER1_p46, ZHANG_SEPTMBER1_p47, ZHANG_SEPTMBER1_p48, ZHANG_SEPTMBER1_p49, ZHANG_SEPTMBER1_p50, ZHANG_SEPTMBER1_p51, ZHANG_SEPTMBER1_p52, ZHANG_SEPTMBER1_p53, ZHANG_SEPTMBER1_p54, ZHANG_SEPTMBER1_p55, ZHANG_SEPTMBER1_p56, ZHANG_SEPTMBER1_p57, ZHANG_SEPTMBER1_p58, ZHANG_SEPTMBER1_p59, ZHANG_SEPTMBER1_p60, ZHANG_SEPTMBER1_p61, ZHANG_SEPTMBER1_p62, ZHANG_SEPTMBER1_p63, ZHANG_SEPTMBER1_p64, ZHANG_SEPTMBER1_p65, ZHANG_SEPTMBER1_p66, ZHANG_SEPTMBER1_p67, ZHANG_SEPTMBER1_p68, ZHANG_SEPTMBER1_p69, ZHANG_SEPTMBER1_p70, ZHANG_SEPTMBER1_p71, ZHANG_SEPTMBER1_p72, ZHANG_SEPTMBER1_p73, ZHANG_SEPTMBER1_p74, ZHANG_SEPTMBER1_p75, ZHANG_SEPTMBER1_p76, ZHANG_SEPTMBER1_p77, ZHANG_SEPTMBER1_p78, ZHANG_SEPTMBER1_p79, ZHANG_SEPTMBER1_p80, ZHANG_SEPTMBER1_p81, ZHANG_SEPTMBER1_p82, ZHANG_SEPTMBER1_p83, ZHANG_SEPTMBER1_p84, ZHANG_SEPTMBER1_p85, ZHANG_SEPTMBER1_p86, ZHANG_SEPTMBER1_p87, ZHANG_SEPTMBER1_p88, ZHANG_SEPTMBER1_p89, ZHANG_SEPTMBER1_p90, ZHANG_SEPTMBER1_p91, ZHANG_SEPTMBER1_p92, ZHANG_SEPTMBER1_p93, ZHANG_SEPTMBER1_p94, ZHANG_SEPTMBER1_p95, ZHANG_SEPTMBER1_p96, ZHANG_SEPTMBER1_p97, ZHANG_SEPTMBER1_p98, ZHANG_SEPTMBER1_p99;
20
21 begin
22
23     ZHANG_SEPTMBER1_H1: ZHANG_SEPTMBER1_equal port map(ZHANG_SEPTMBER1_I0 => ZHANG_SEPTMBER1_a(0), ZHANG_SEPTMBER1_I1 => ZHANG_SEPTMBER1_b(0), ZHANG_SEPTMBER1_Eq
24     ZHANG_SEPTMBER1_H2: ZHANG_SEPTMBER1_equal port map(ZHANG_SEPTMBER1_I0 => ZHANG_SEPTMBER1_a(1), ZHANG_SEPTMBER1_I1 => ZHANG_SEPTMBER1_b(1), ZHANG_SEPTMBER1_Eq
25     ZHANG_SEPTMBER1_H3: ZHANG_SEPTMBER1_equal port map(ZHANG_SEPTMBER1_I0 => ZHANG_SEPTMBER1_a(2), ZHANG_SEPTMBER1_I1 => ZHANG_SEPTMBER1_b(2), ZHANG_SEPTMBER1_Eq
26     ZHANG_SEPTMBER1_H4: ZHANG_SEPTMBER1_equal port map(ZHANG_SEPTMBER1_I0 => ZHANG_SEPTMBER1_a(3), ZHANG_SEPTMBER1_I1 => ZHANG_SEPTMBER1_b(3), ZHANG_SEPTMBER1_Eq
27     ZHANG_SEPTMBER1_H5: ZHANG_SEPTMBER1_equal port map(ZHANG_SEPTMBER1_I0 => ZHANG_SEPTMBER1_a(4), ZHANG_SEPTMBER1_I1 => ZHANG_SEPTMBER1_b(4), ZHANG_SEPTMBER1_Eq
28     ZHANG_SEPTMBER1_H6: ZHANG_SEPTMBER1_equal port map(ZHANG_SEPTMBER1_I0 => ZHANG_SEPTMBER1_a(5), ZHANG_SEPTMBER1_I1 => ZHANG_SEPTMBER1_b(5), ZHANG_SEPTMBER1_Eq
29     ZHANG_SEPTMBER1_H7: ZHANG_SEPTMBER1_equal port map(ZHANG_SEPTMBER1_I0 => ZHANG_SEPTMBER1_a(6), ZHANG_SEPTMBER1_I1 => ZHANG_SEPTMBER1_b(6), ZHANG_SEPTMBER1_Eq
30     ZHANG_SEPTMBER1_H8: ZHANG_SEPTMBER1_equal port map(ZHANG_SEPTMBER1_I0 => ZHANG_SEPTMBER1_a(7), ZHANG_SEPTMBER1_I1 => ZHANG_SEPTMBER1_b(7), ZHANG_SEPTMBER1_Eq
31
32     ZHANG_SEPTMBER1_aeqb <= ZHANG_SEPTMBER1_p0 and ZHANG_SEPTMBER1_p1 and ZHANG_SEPTMBER1_p2 and ZHANG_SEPTMBER1_p3 and ZHANG_SEPTMBER1_p4 and ZHANG_SEPTMBER1_p5
33 end ZHANG_SEPTMBER1_arch;
```

Transcript

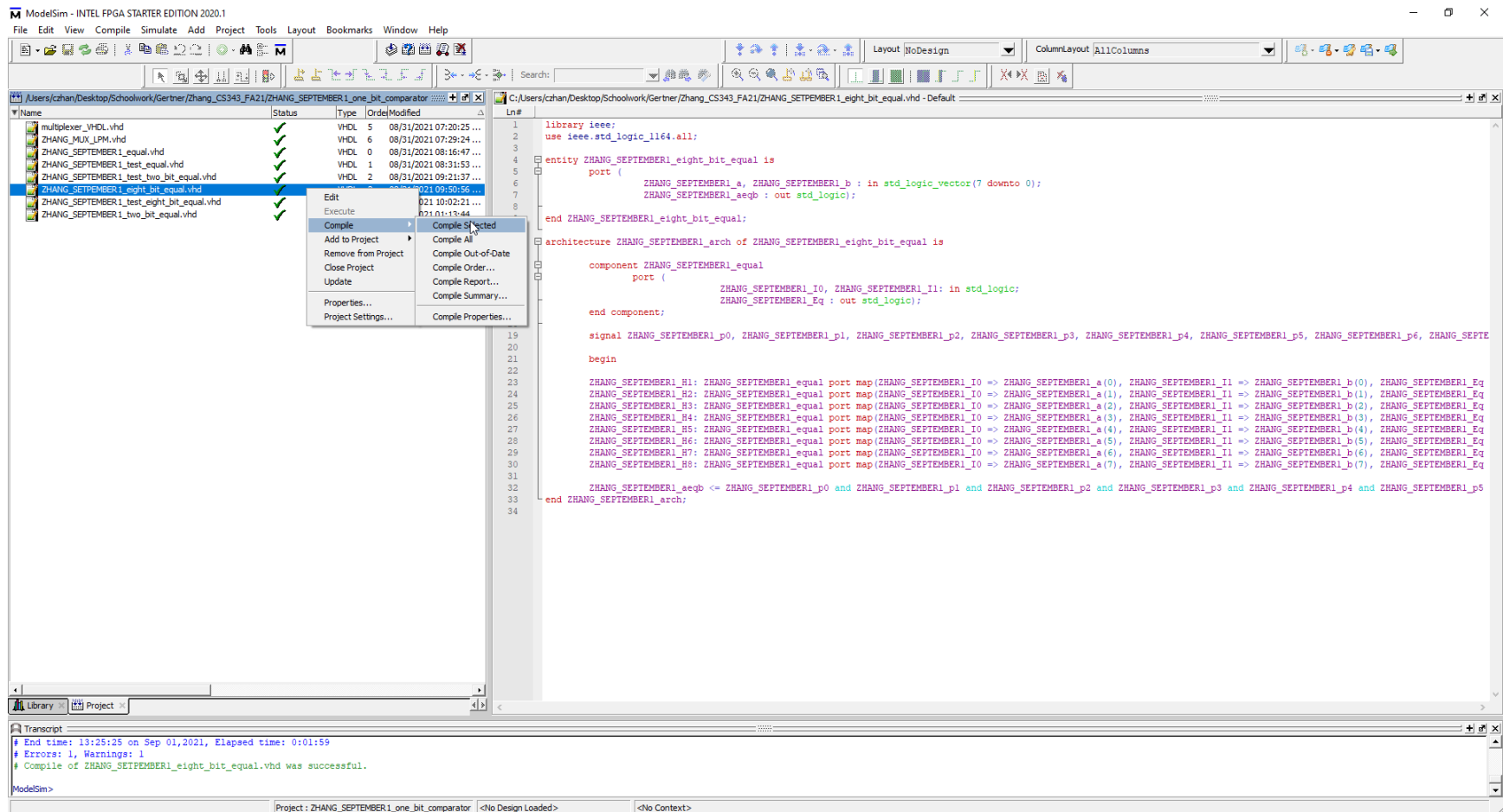
```
VSIM4> quit -sim
# End time: 13:25:25 on Sep 01,2021, Elapsed time: 0:01:59
# Errors: 1, Warnings: 1
```

ModelSim>

Project: ZHANG_SEPTMBER1_one_bit_comparator <No Design Loaded> <No Context>

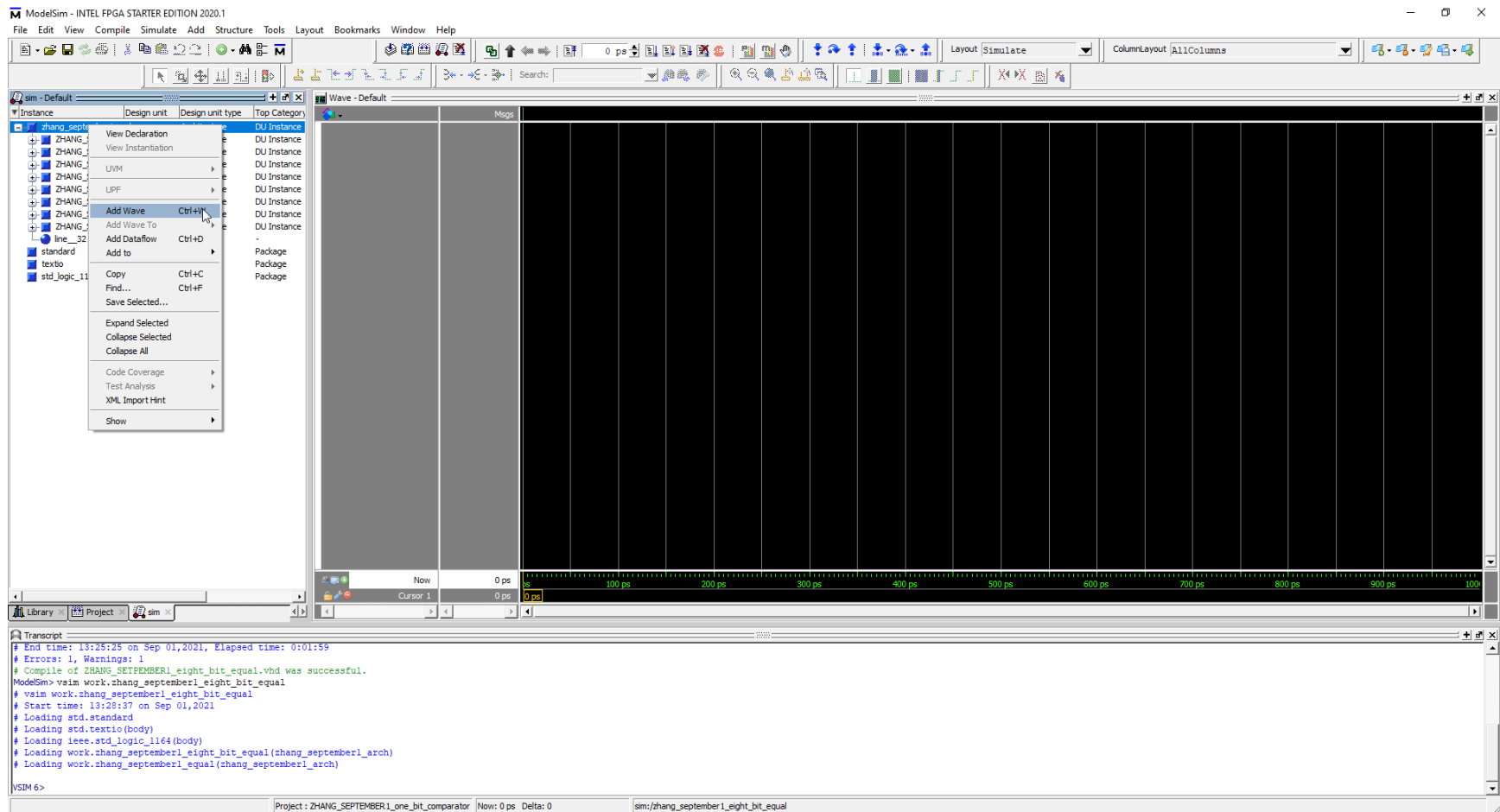
This is the vhdl code created for the eight bit comparator that I have written

Task 2 : 8-bit Comparator , Chue Zhang



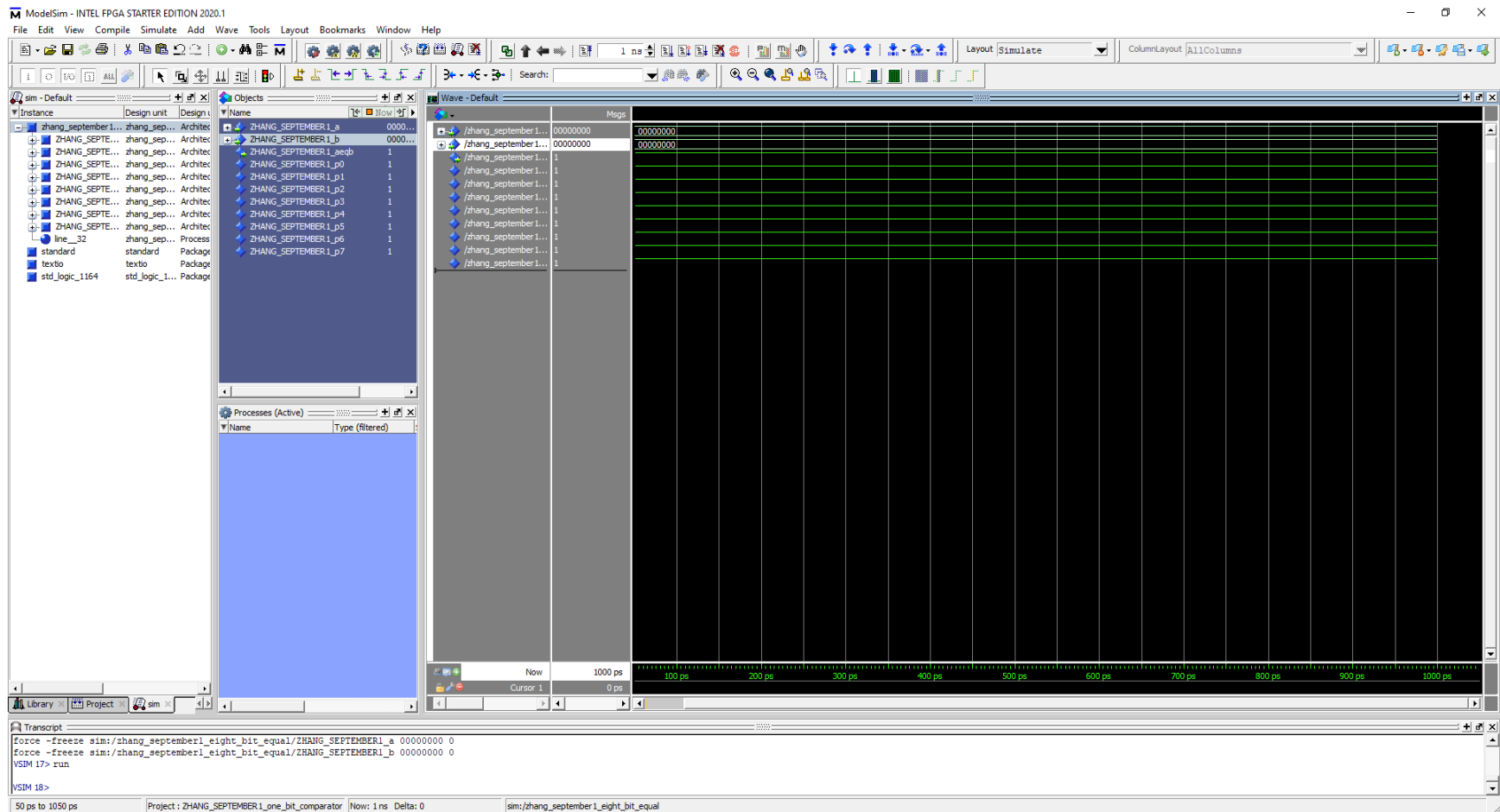
I compile with success as shown in the textbox at the bottom of the figure

Task 2 : 8-bit Comparator , Chue Zhang



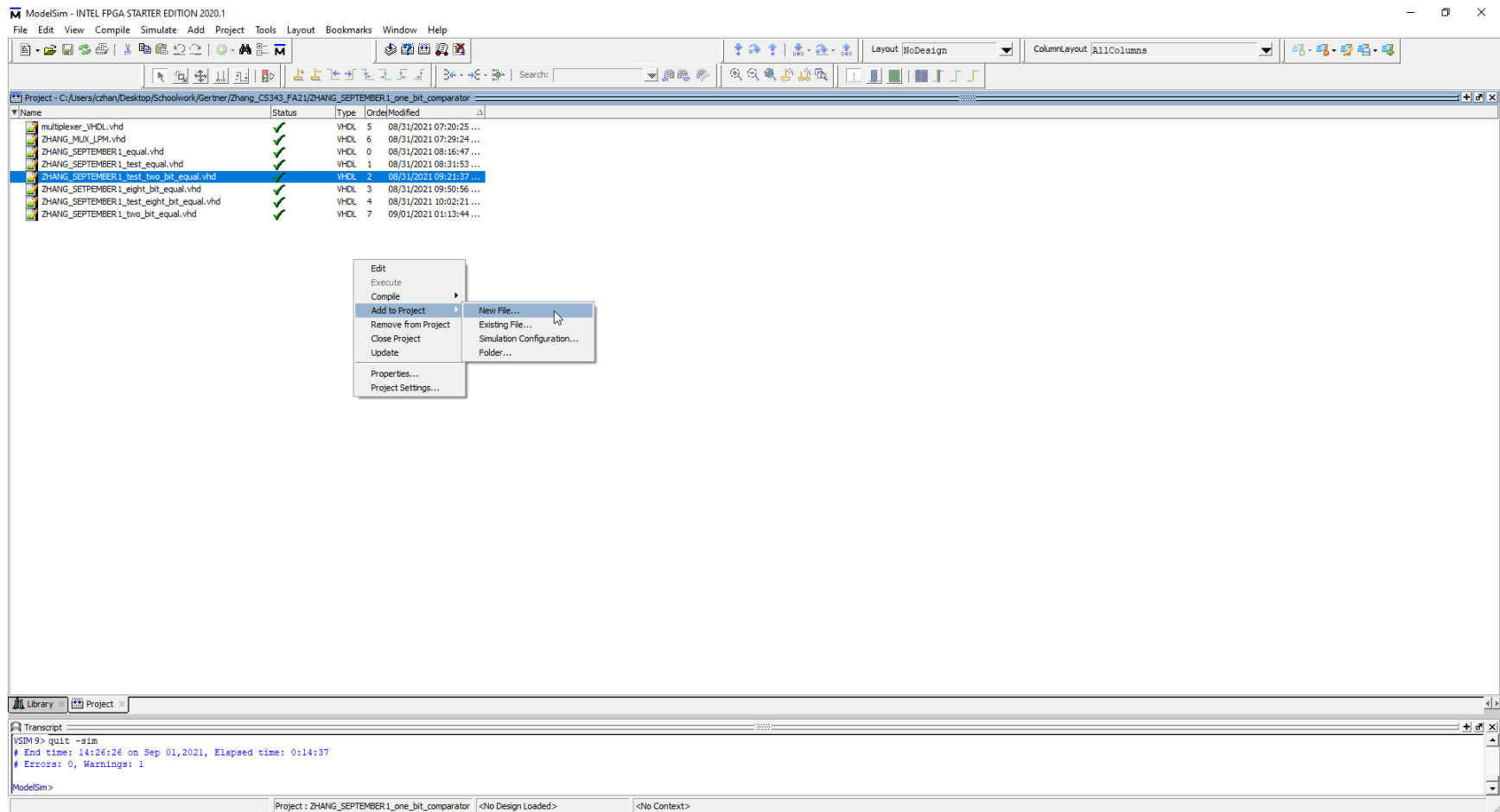
I begin simulating in modelsim by adding the waves to be simulated with

Task 2 : 8-bit Comparator , Chue Zhang



This was the modelsim Output, as you can see in it, output is 1 which is correct

Task 2 : 8-bit Comparator , Chue Zhang



Next I create another file for the test bench

Task 2 : 8-bit Comparator , Chue Zhang

The screenshot shows the ModelSim - INTEL FPGA STARTER EDITION 2020.1 interface. The left pane displays a project tree with the following files:

Name	Status	Type	Order	Modified
multiplexer_VHDL.vhd	✓	VHDL	5	08/31/2021 07:20:25 ...
ZHANG_MUX_LPM.vhd	✓	VHDL	6	08/31/2021 07:29:24 ...
ZHANG_SEPTMBER1_equal.vhd	✓	VHDL	0	08/31/2021 08:16:47 ...
ZHANG_SEPTMBER1_test_equal.vhd	✓	VHDL	1	08/31/2021 08:31:53 ...
ZHANG_SEPTMBER1_test_two_bit_equal.vhd	✓	VHDL	2	08/31/2021 09:21:37 ...
ZHANG_SEPTMBER1_eight_bit_equal.vhd	✓	VHDL	3	08/31/2021 09:50:56 ...
ZHANG_SEPTMBER1_test_eight_bit_equal.vhd	✓	VHDL	4	08/31/2021 10:02:21 ...
ZHANG_SEPTMBER1_two_bit_equal.vhd	✓	VHDL	7	09/01/2021 01:13:44 ...

The right pane shows the VHDL code for the file `C:/Users/czhan/Desktop/Schoolwork/Gertner/Zhang_CS343_FA21/ZHANG_SEPTMBER1_test_eight_bit_equal.vhd`. The code is as follows:

```
2 use ieee.std_logic_1164.all;
3
4 entity ZHANG_SEPTMBER1_test_eight_bit_equal_port_map is
5 end ZHANG_SEPTMBER1_test_eight_bit_equal_port_map;
6
7 architecture ZHANG_SEPTMBER1_arch_test of ZHANG_SEPTMBER1_test_eight_bit_equal_port_map is
8
9 component ZHANG_SEPTMBER1_eight_bit_equal
10 port ( ZHANG_SEPTMBER1_a, ZHANG_SEPTMBER1_b : in std_logic_vector(7 downto 0);
11       ZHANG_SEPTMBER1_aeqb : out std_logic);
12 end component;
13
14 signal ZHANG_SEPTMBER1_p1, ZHANG_SEPTMBER1_p0 : std_logic_vector(7 downto 0);
15 signal ZHANG_SEPTMBER1_pout : std_logic;
16 signal ZHANG_SEPTMBER1_error : std_logic := '0';
17
18 begin
19     uut : ZHANG_SEPTMBER1_eight_bit_equal port map (ZHANG_SEPTMBER1_a => ZHANG_SEPTMBER1_p0,
20                                                    ZHANG_SEPTMBER1_b => ZHANG_SEPTMBER1_p1,
21                                                    ZHANG_SEPTMBER1_aeqb => ZHANG_SEPTMBER1_pout);
22
23     process
24     begin
25         ZHANG_SEPTMBER1_p0 <= "00000000";
26         ZHANG_SEPTMBER1_p1 <= "00000000";
27         wait for 1 ns;
28         if (ZHANG_SEPTMBER1_pout = '0') then
29             ZHANG_SEPTMBER1_error <= '1';
30         end if;
31         wait for 200 ns;
32         ZHANG_SEPTMBER1_p0 <= "01010101";
33         ZHANG_SEPTMBER1_p1 <= "00010101";
34         wait for 1 ns;
35         if (ZHANG_SEPTMBER1_pout = '1') then
36             ZHANG_SEPTMBER1_error <= '1';
37         end if;
38         wait for 200 ns;
39         ZHANG_SEPTMBER1_p0 <= "01100101";
40         ZHANG_SEPTMBER1_p1 <= "11111001";
41         wait for 1 ns;
42         if (ZHANG_SEPTMBER1_pout = '1') then
43             ZHANG_SEPTMBER1_error <= '1';
44         end if;
45         wait for 200 ns;
46         ZHANG_SEPTMBER1_p0 <= "11110011";
47         ZHANG_SEPTMBER1_p1 <= "00010100";
48         wait for 1 ns;
49         if (ZHANG_SEPTMBER1_pout = '1') then
50             ZHANG_SEPTMBER1_error <= '1';
51         end if;
52         wait for 200 ns;
```

The bottom pane shows the transcript of the simulation:

```
VSDM9> quit -sim
# End time: 13:34:11 on Sep 01,2021, Elapsed time: 0:01:44
# Errors: 0, Warnings: 2
```

The status bar at the bottom indicates the project is `ZHANG_SEPTMBER1_one_bit_comparator` and the design is not loaded.

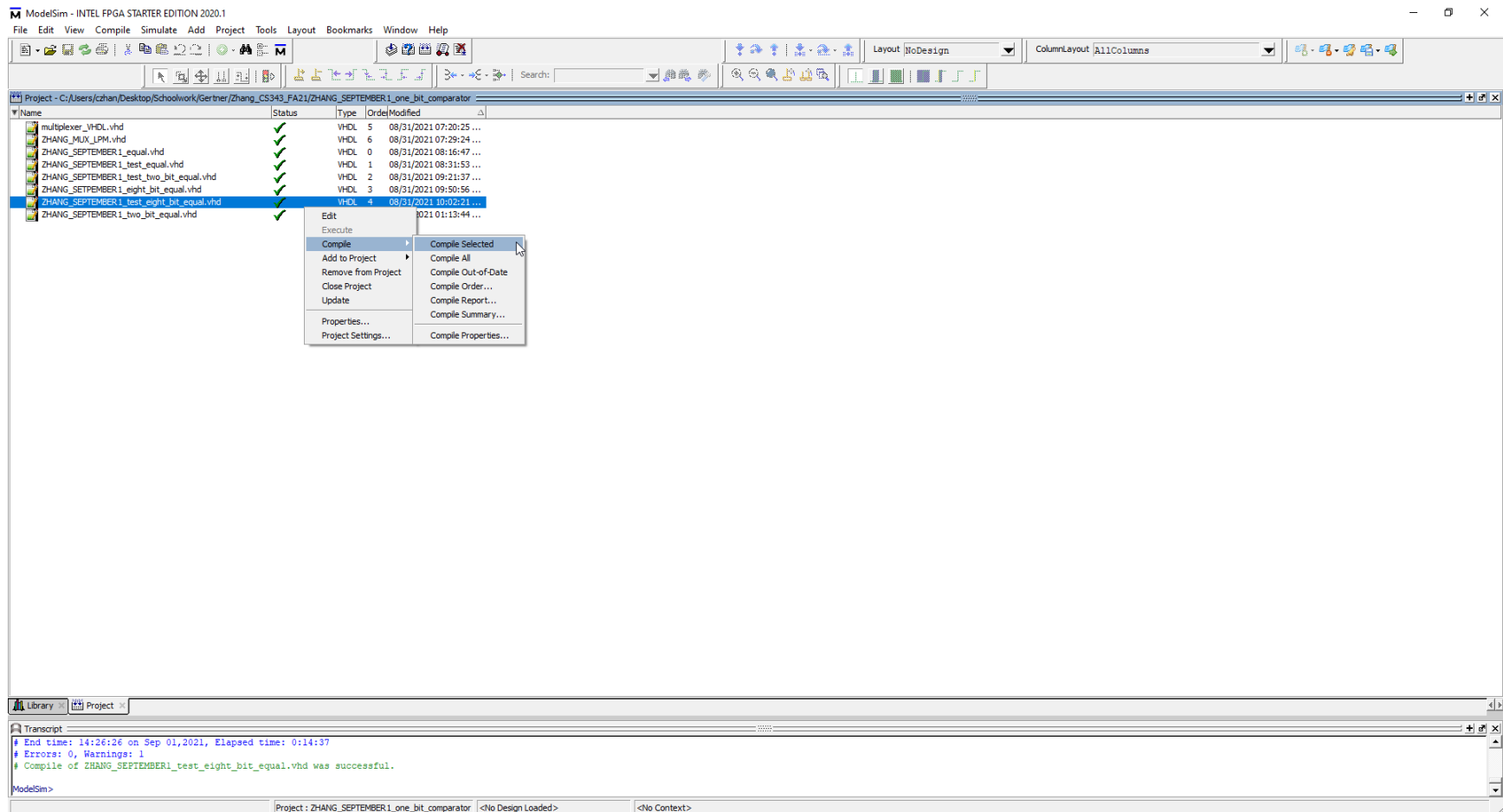
I begin writing VHDL code in the new file I have created

Task 2 : 8-bit Comparator , Chue Zhang

[illegible]

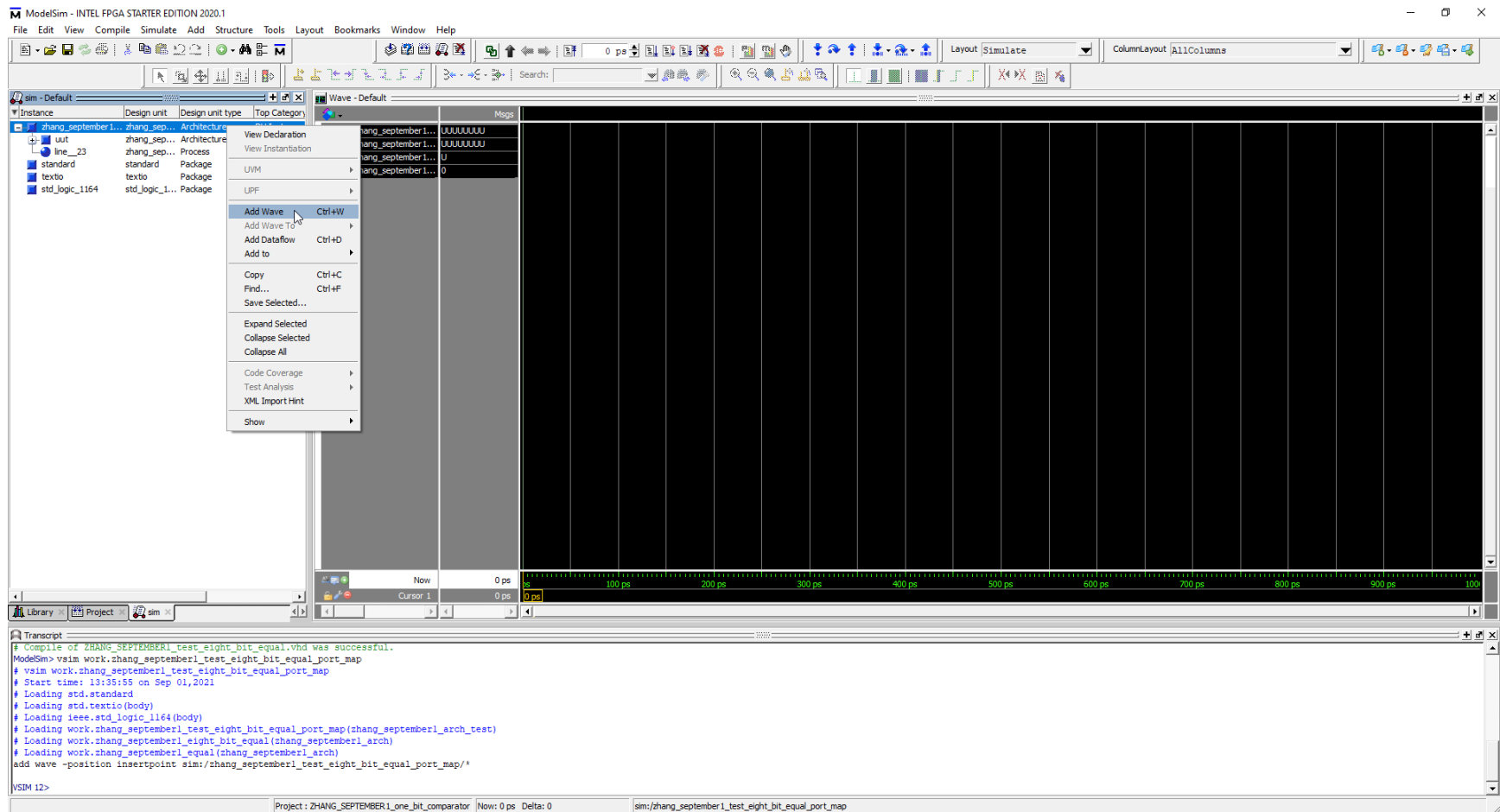
This is the entire code in a screenshot

Task 2 : 8-bit Comparator , Chue Zhang



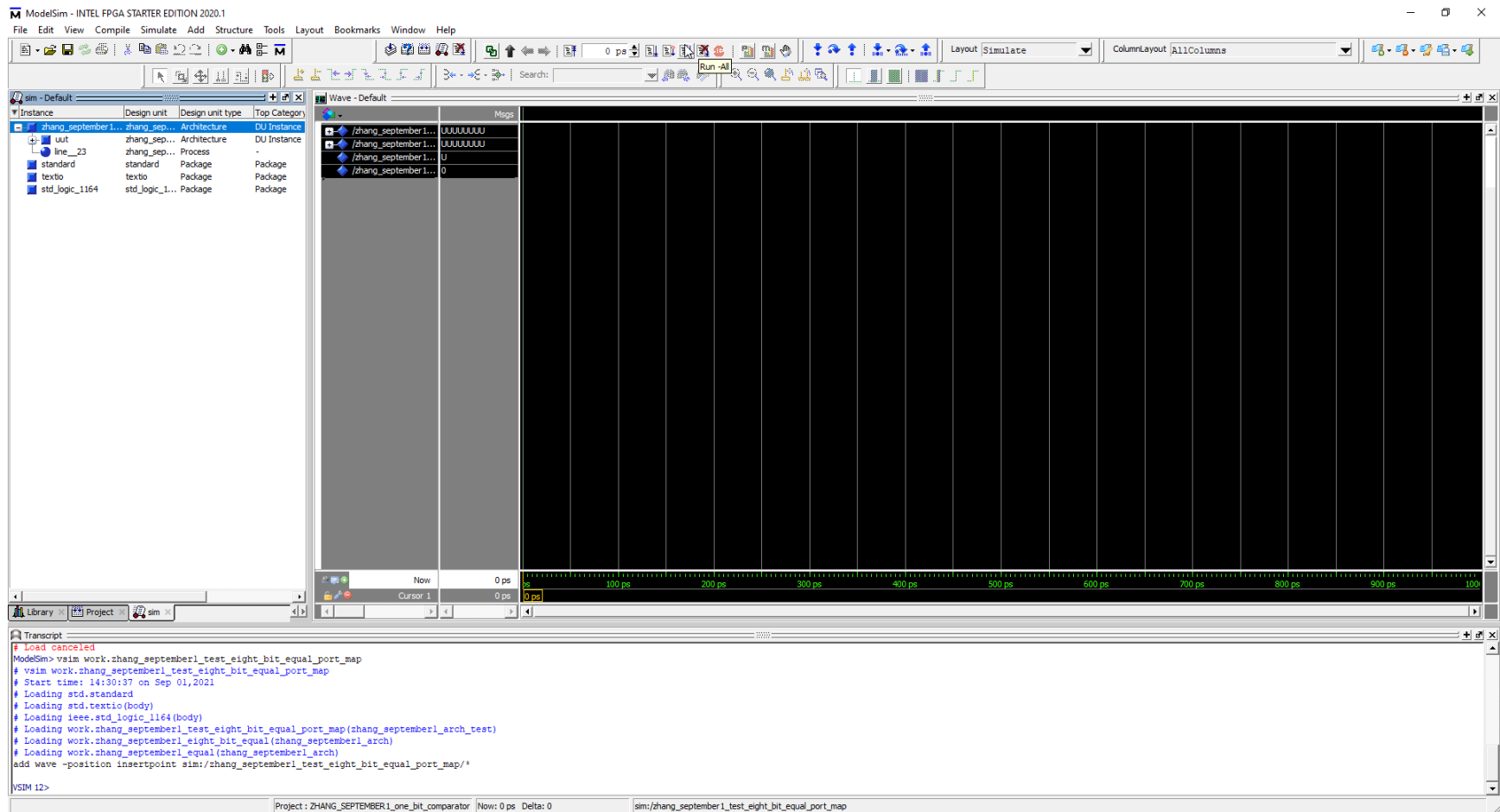
I compile the test bench VHDL file for the 8 bit comparator with no issues. Refer to green text on the bottom of image for verification of success

Task 2 : 8-bit Comparator , Chue Zhang



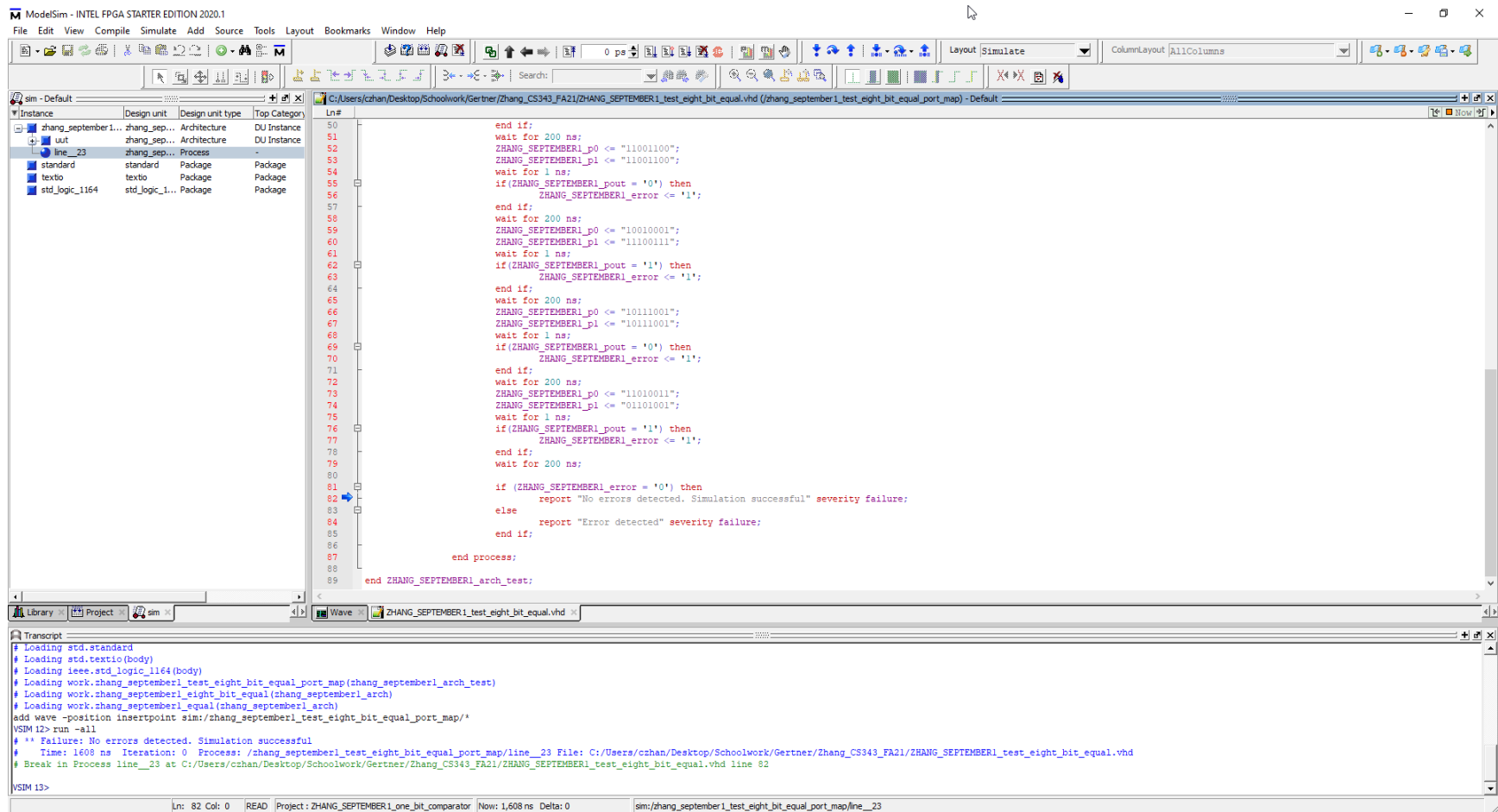
I add waves that are required to be simulated

Task 2 : 8-bit Comparator , Chue Zhang



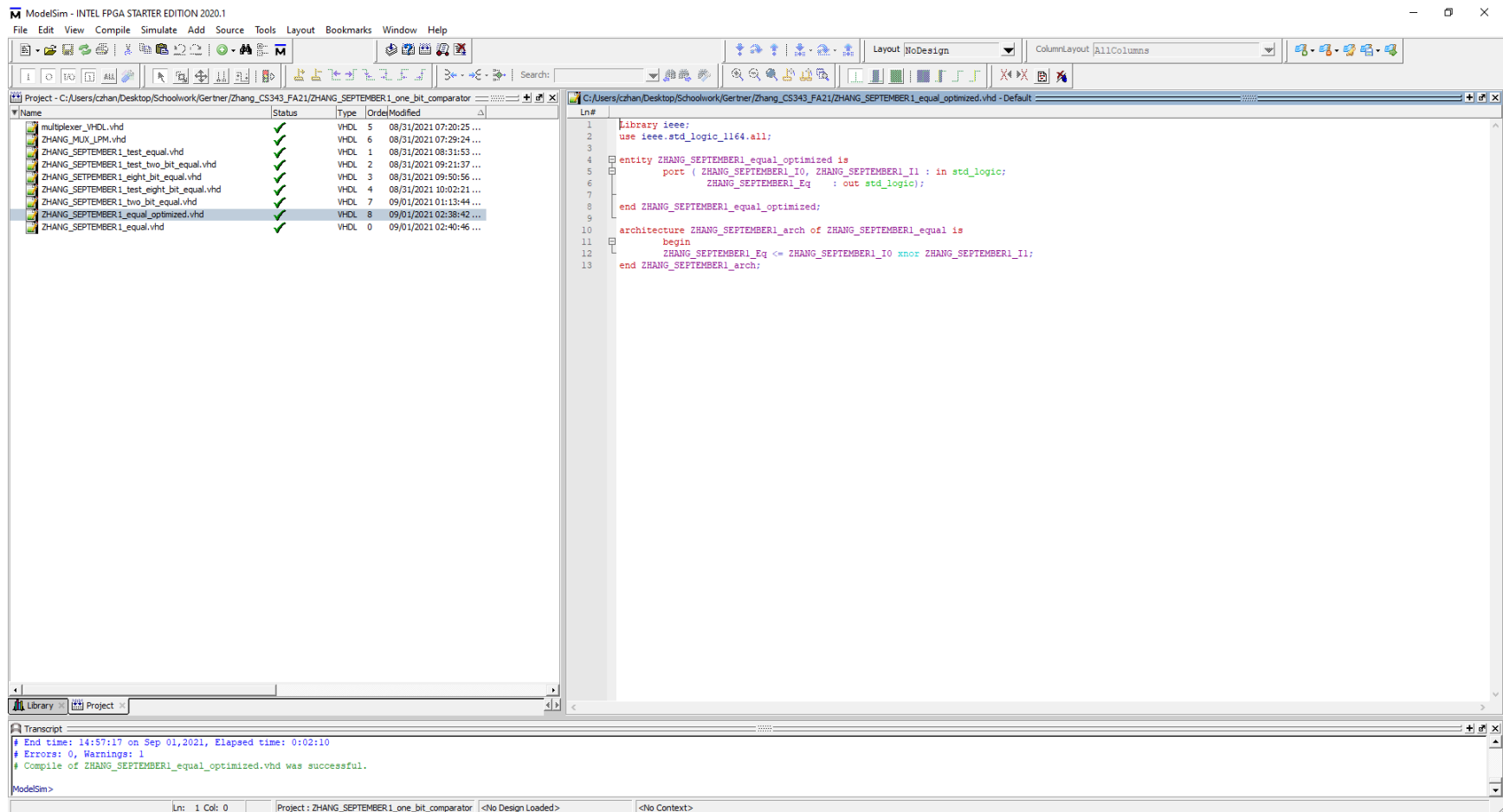
I press run all

Task 2 : 8-bit Comparator , Chue Zhang



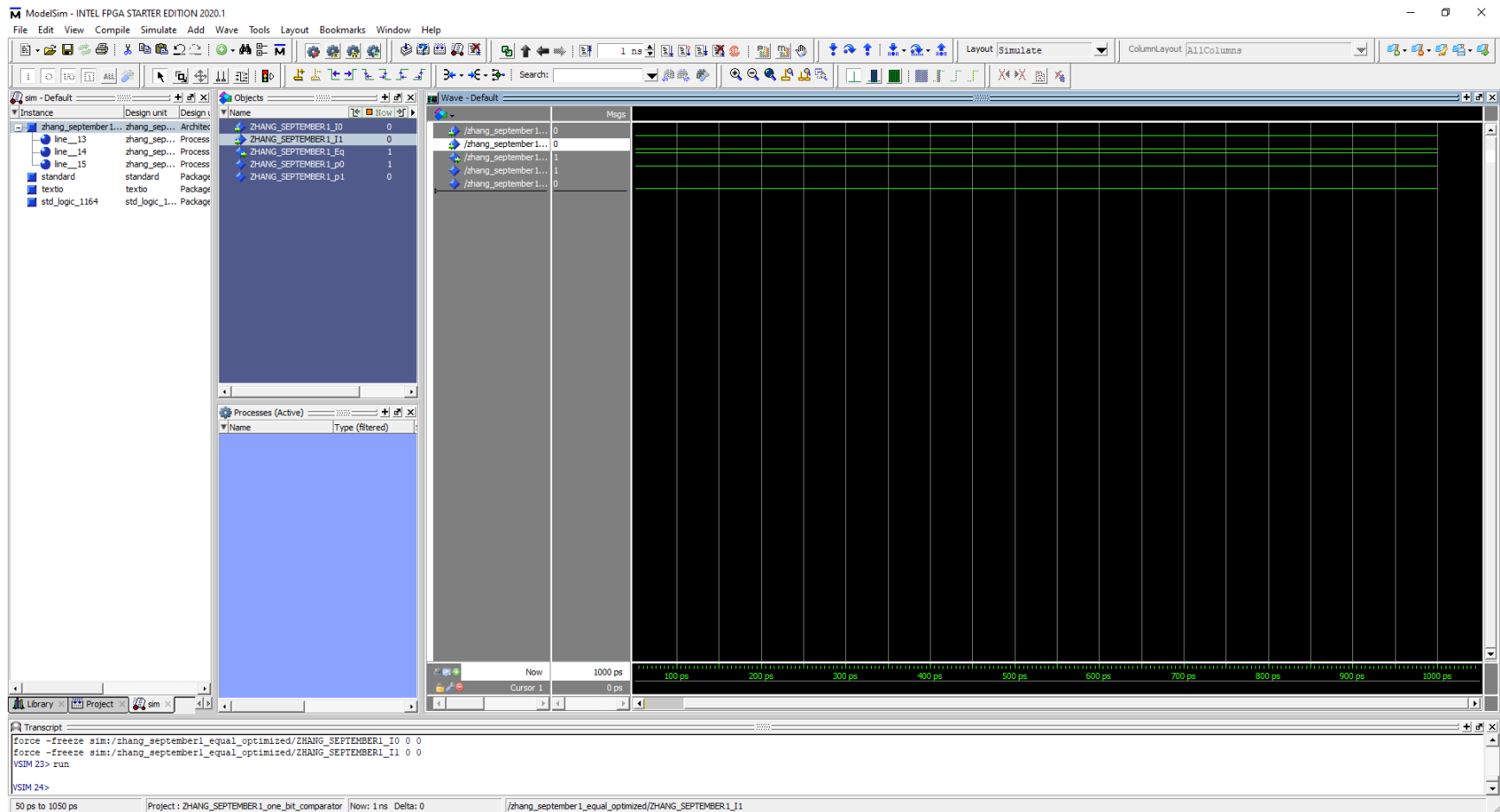
I press run all in modelsim and this page is prompted. There is an arrow at line 62 pointing that there were no errors with the simulation therefore correctness for the 8 bit comparator is verified

Task A1 : 1-bit Comparator optimized, Chue Zhang



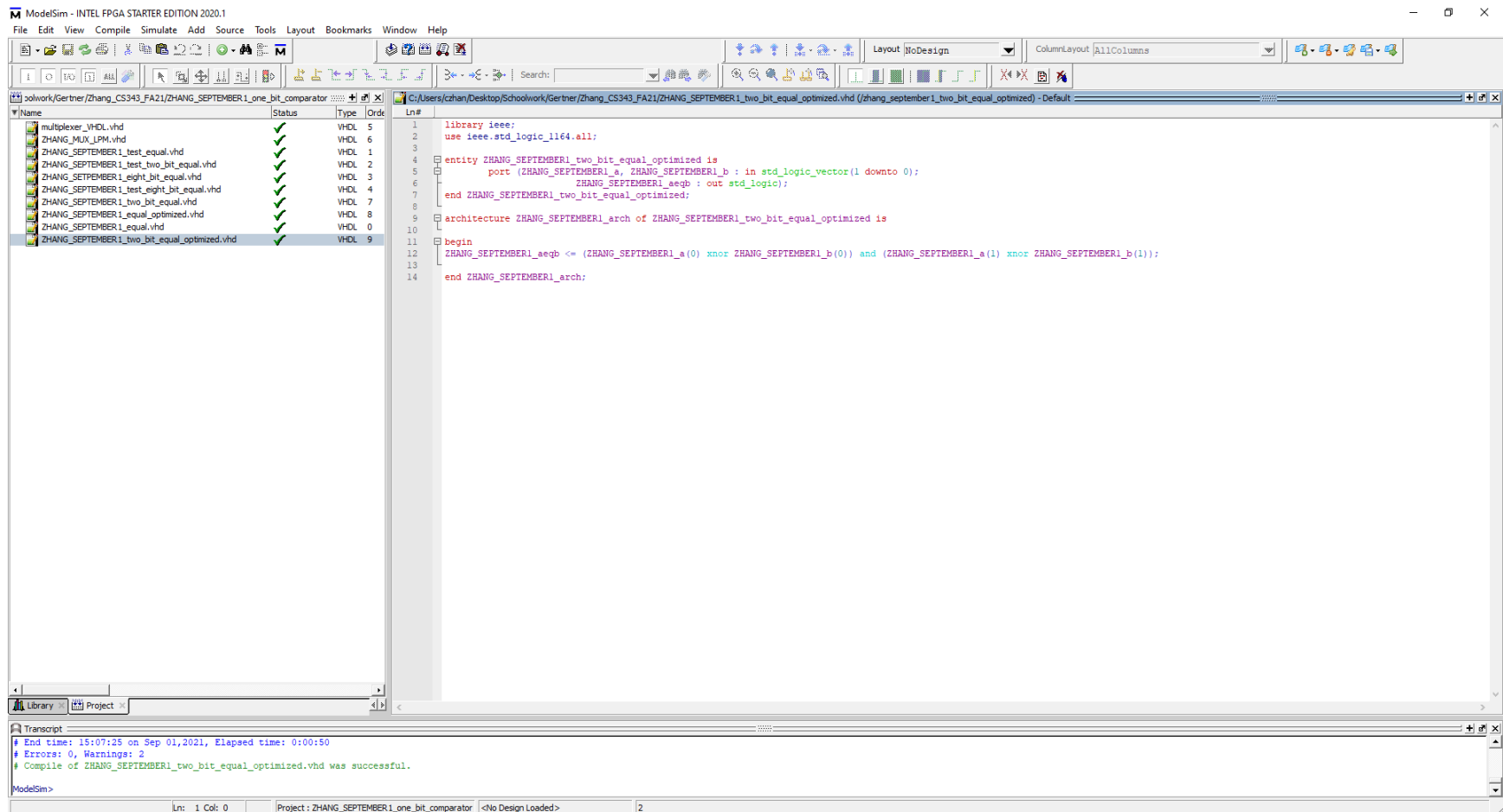
This is the 1 bit comparator that is optimized using XNOR. At the bottom of the image is also a successful compilation OF the optimized 1 bit comparator

Task A1 : 1-bit Comparator optimized, Chue Zhang



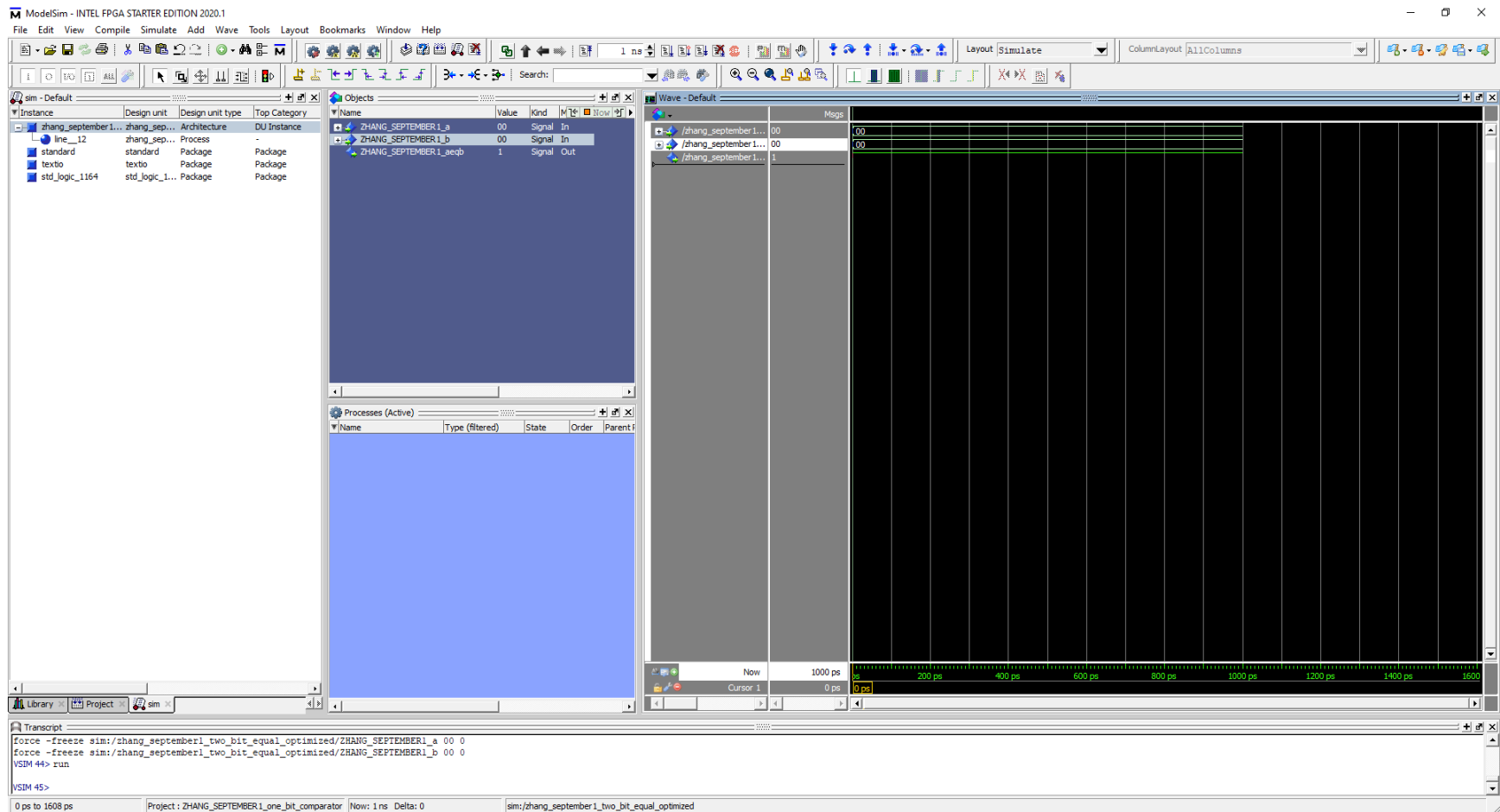
To test for correctness, in modelsim I used inputs 0 and 0 for inputs “a” and “b” respectively and received the output 1 which is correct according to xnor’s truth table.

Task A2 : 2-bit Comparator optimized, Chue Zhang



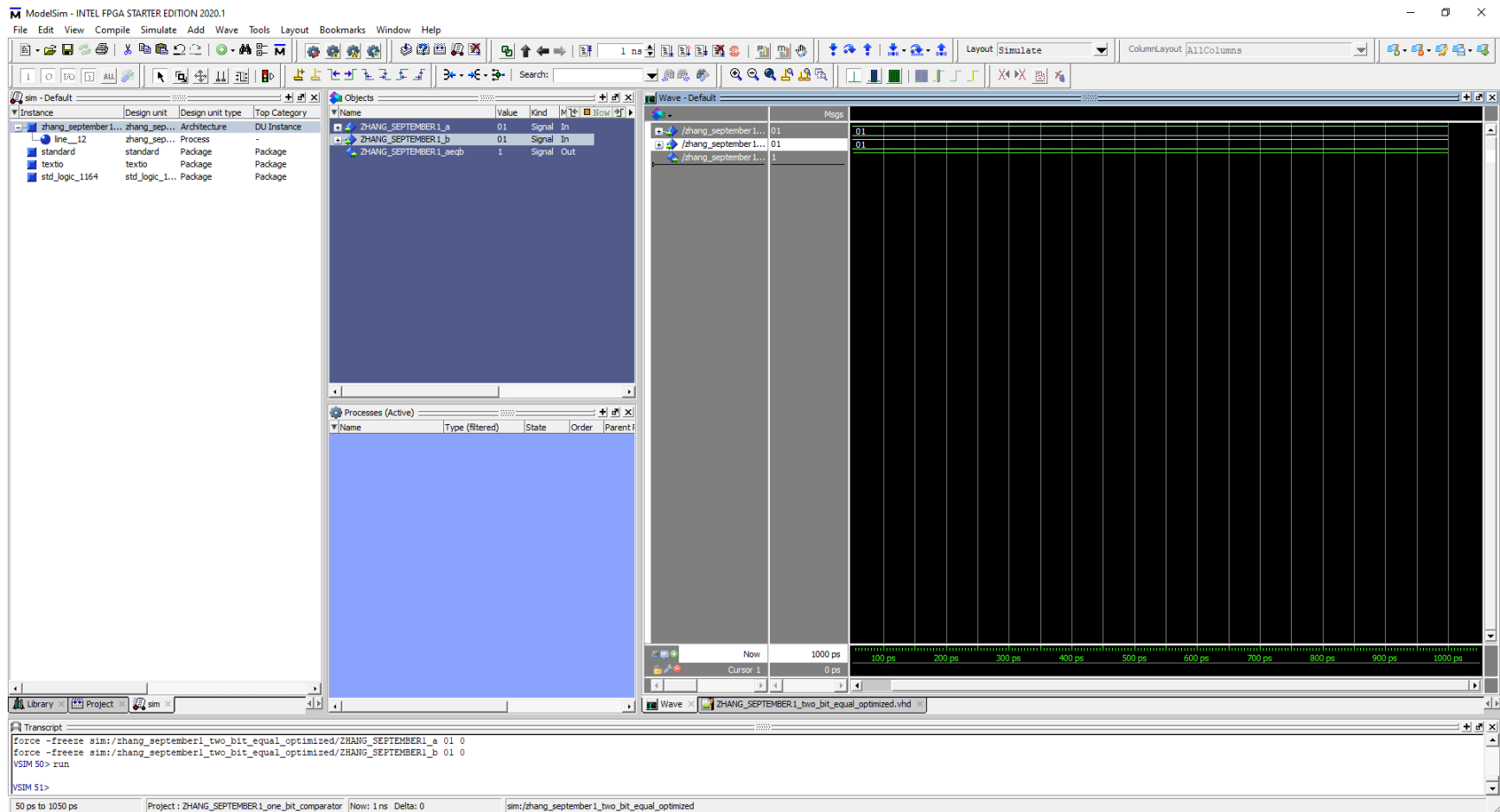
In this image, what is shown is the optimized code for a 2-bit comparator as well as a successful compilation to ensure that the code we will be simulating is correct

Task A2 : 2-bit Comparator optimized, Chue Zhang



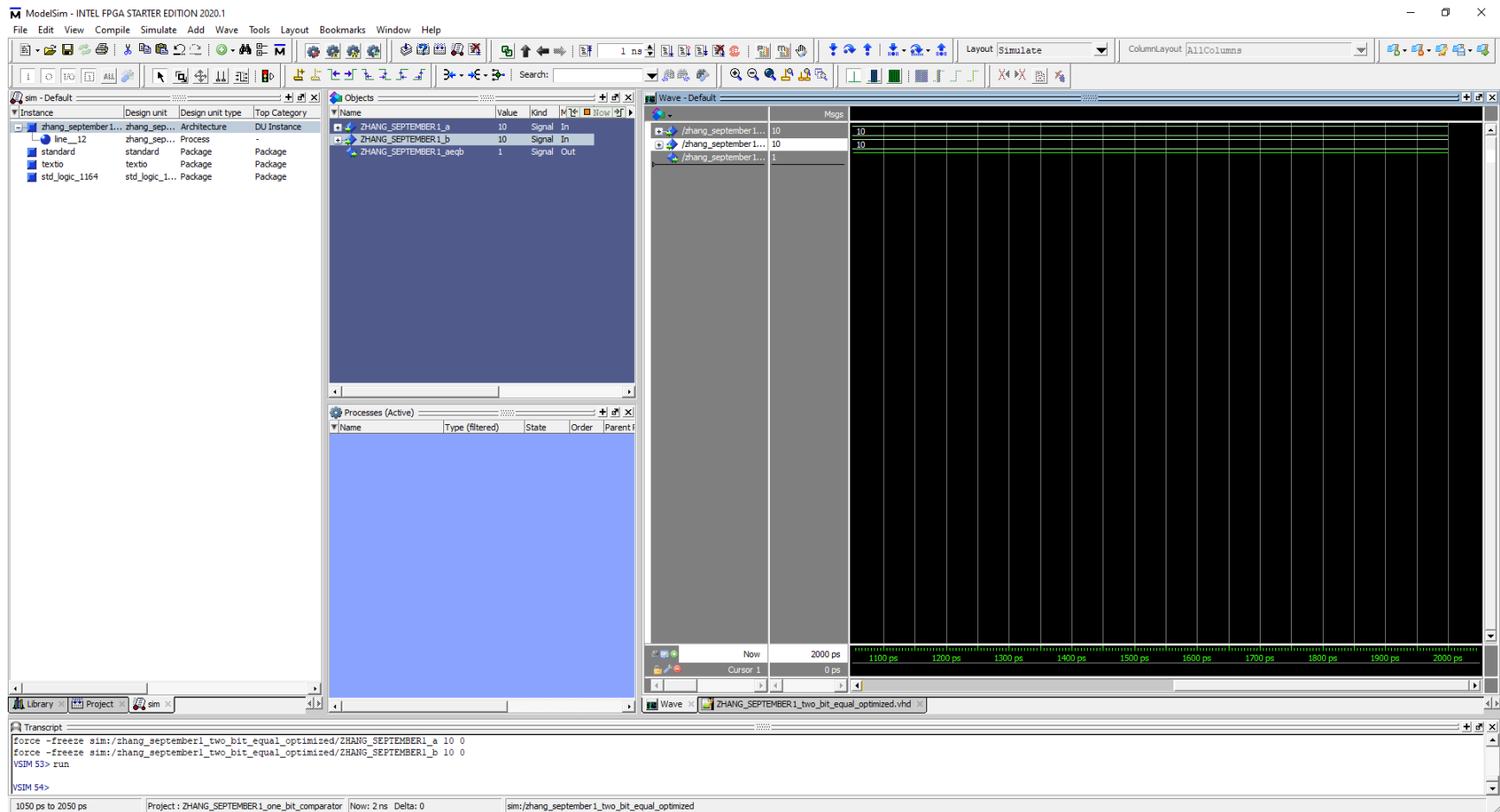
In the image above is the modelsim simulation of the optimized 2 bit comparator running with the inputs “0000” with the output of 1 which is correct.

Task A2 : 2-bit Comparator optimized, Chue Zhang



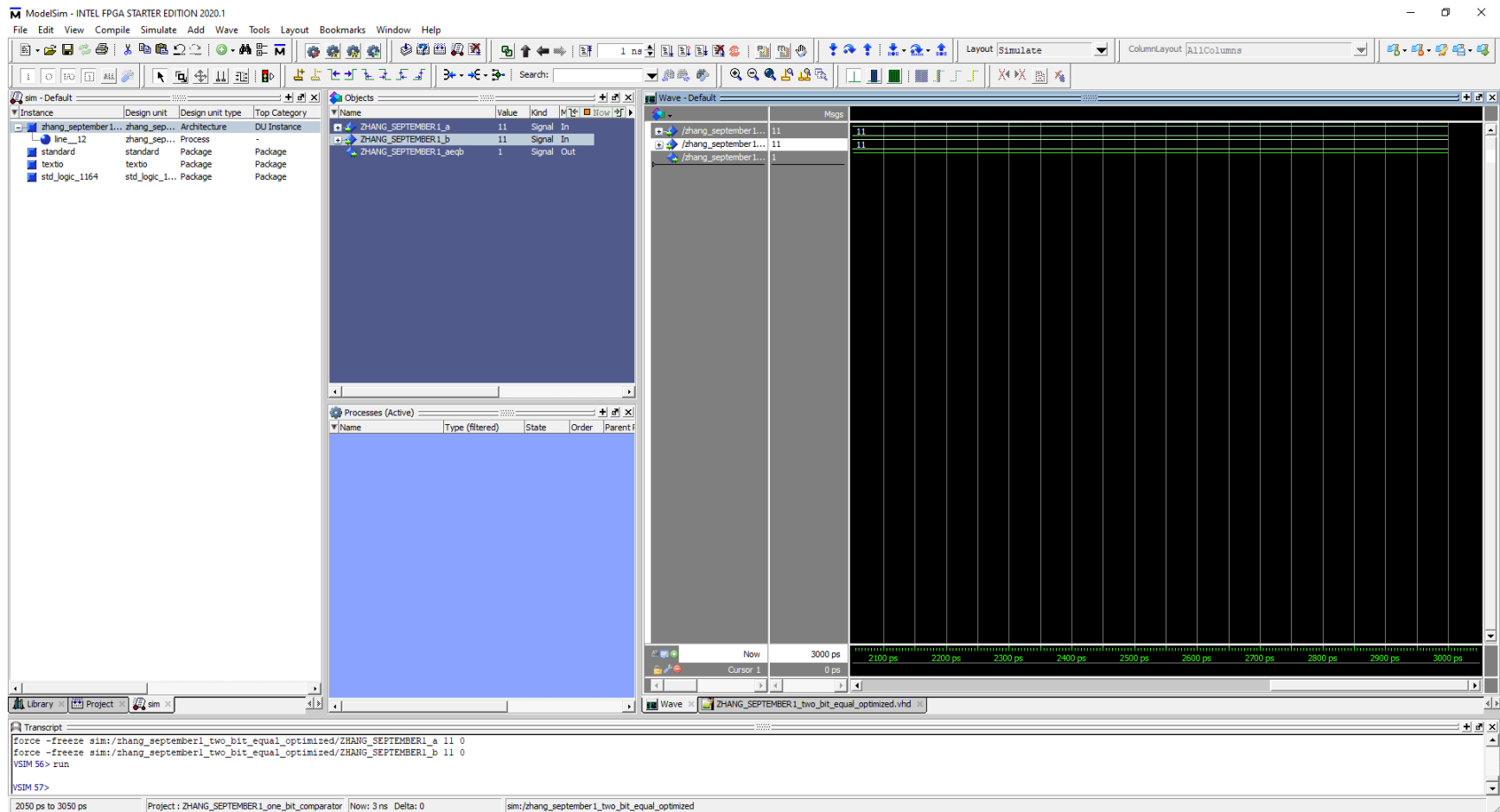
Input with 0101 returning 1

Task A2 : 2-bit Comparator optimized, Chue Zhang



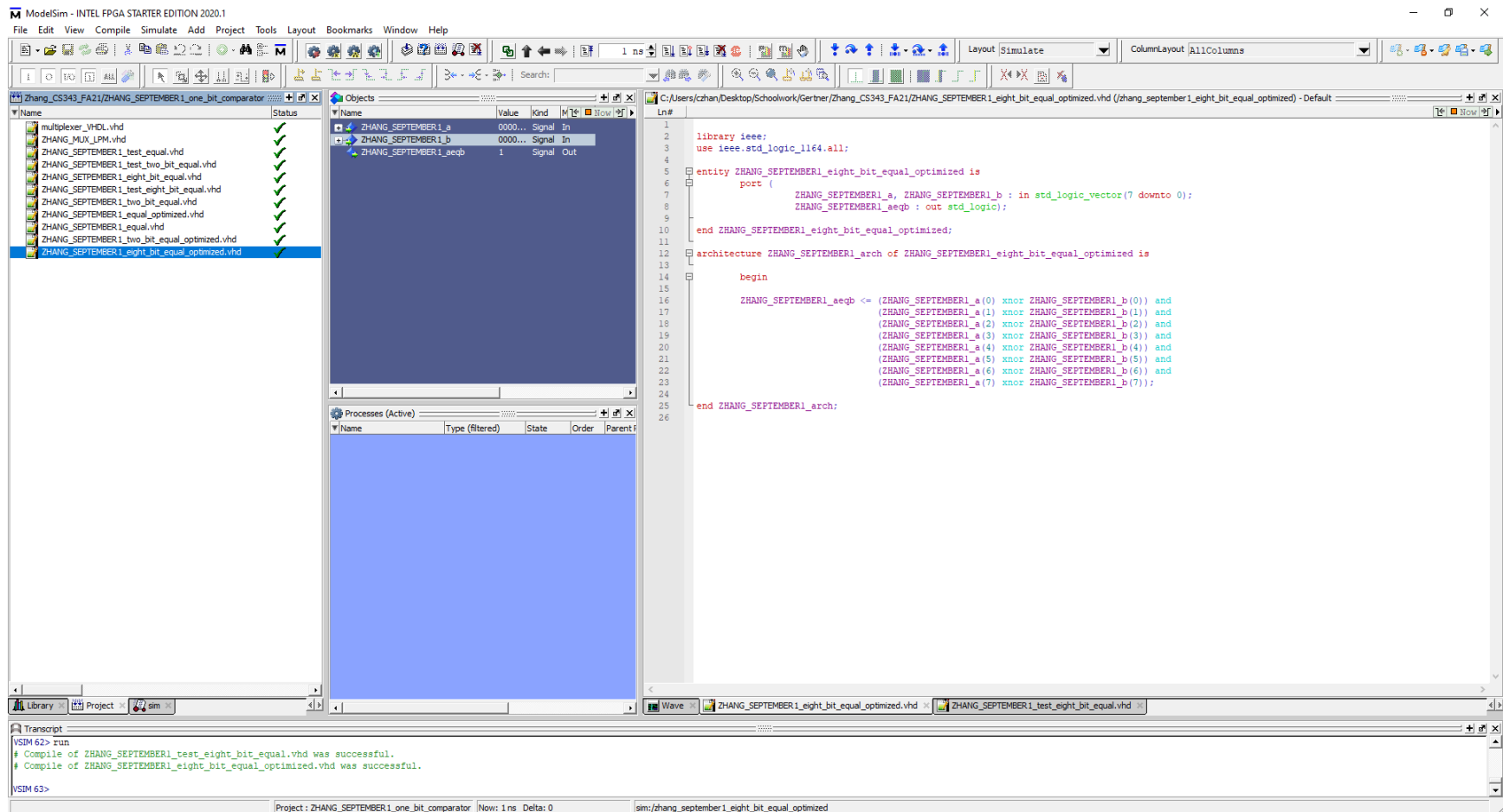
Input with 1010 returning 1

Task A2 : 2-bit Comparator optimized, Chue Zhang



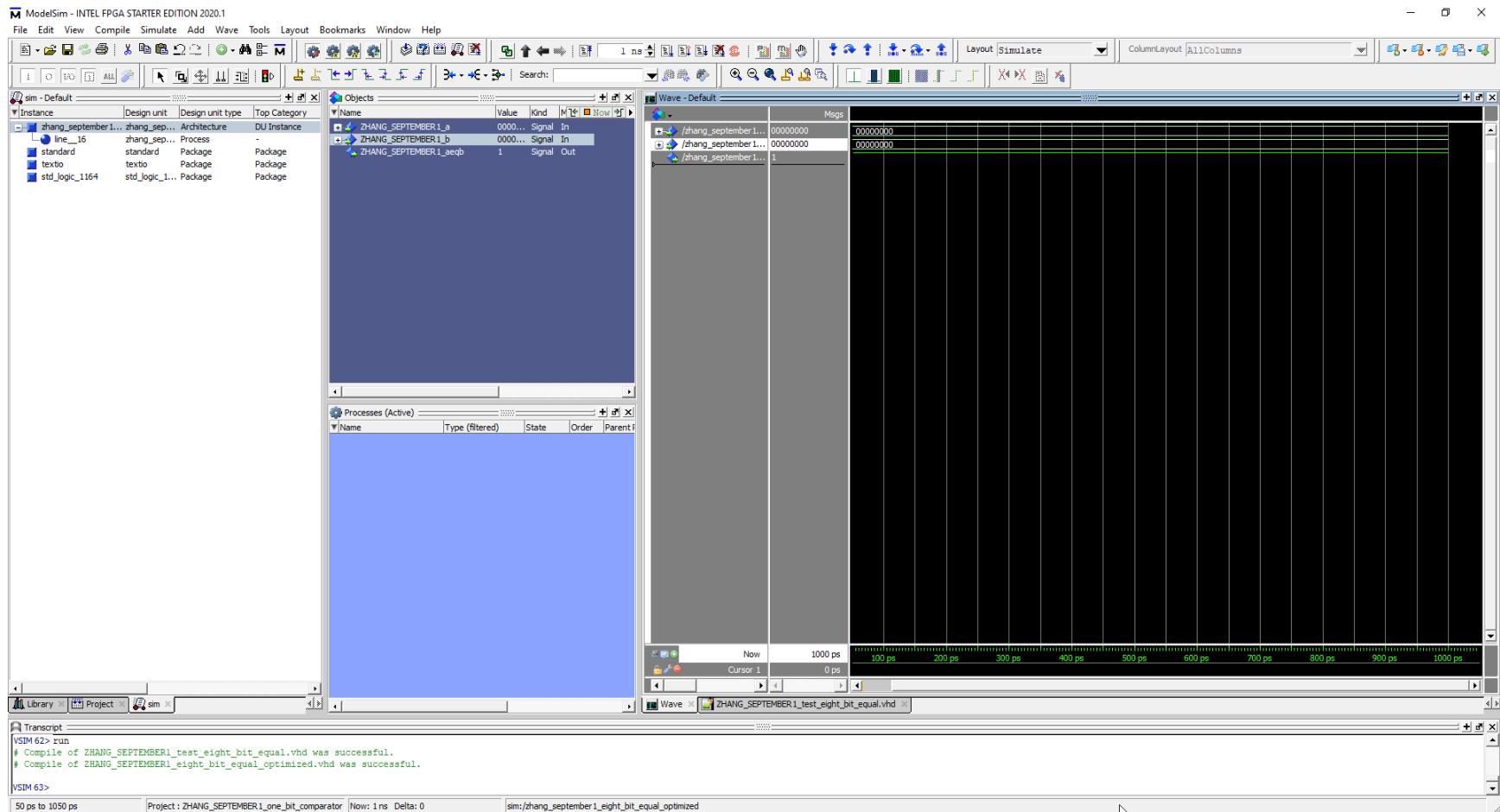
Input with 1111 returning 1

Task A3 : 8-bit Comparator optimized, Chue Zhang



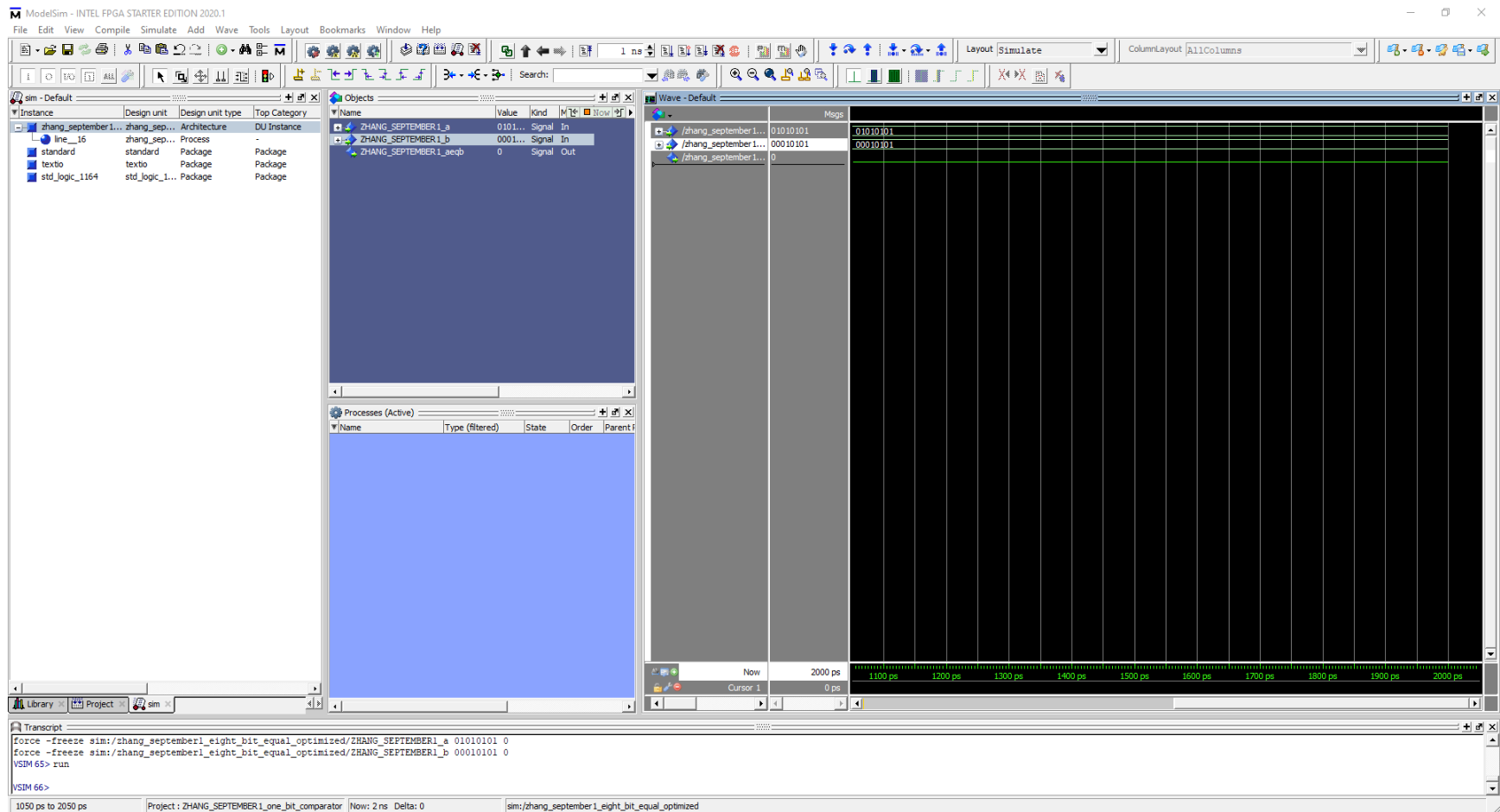
In the image above, it shows the 8 bit comparator with optimized code and successful compilation to verify correctness in the code

Task A3 : 8-bit Comparator optimized, Chue Zhang



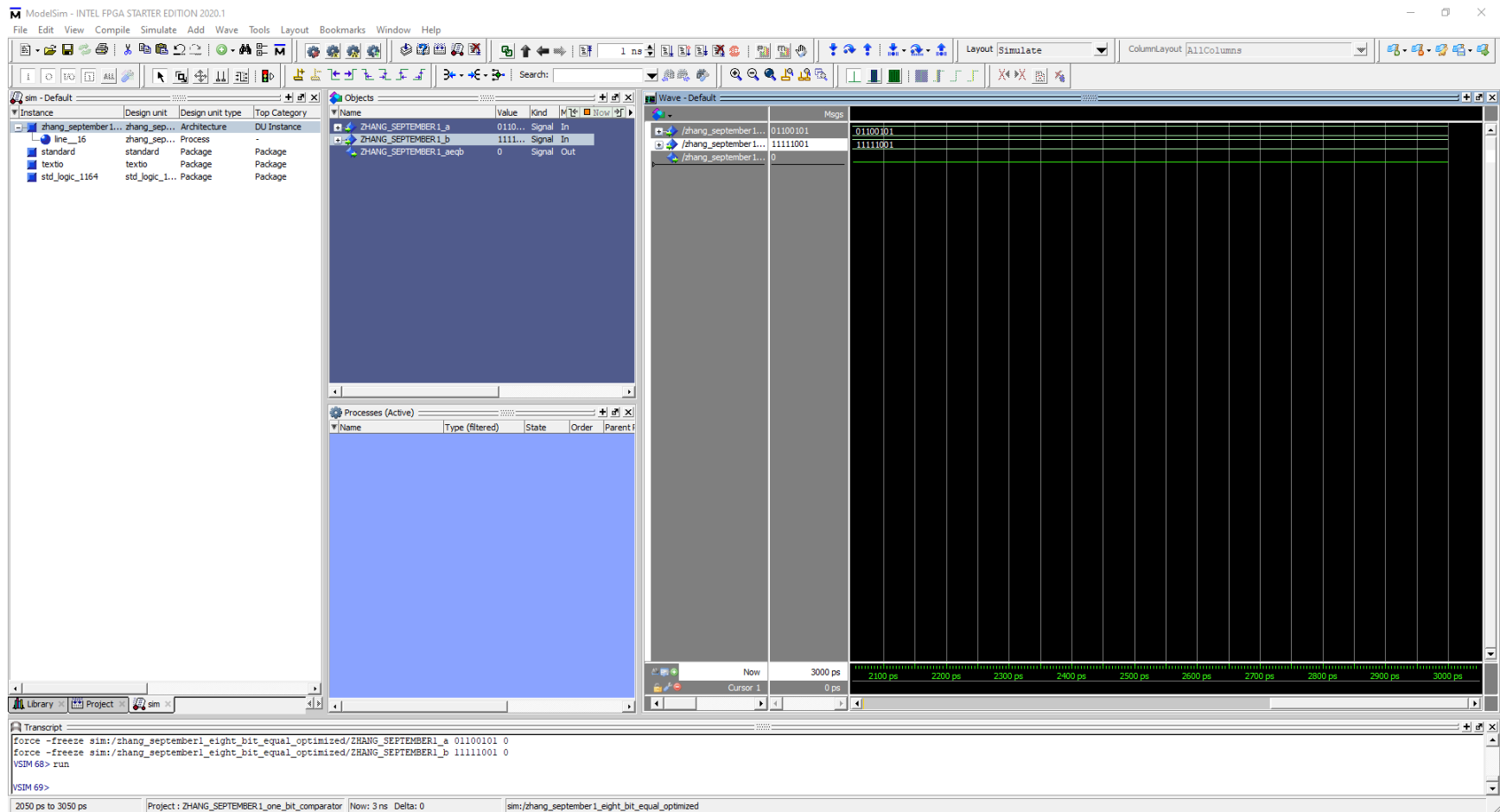
Input of 00000000, 00000000 for an output of 1

Task A3 : 8-bit Comparator optimized, Chue Zhang



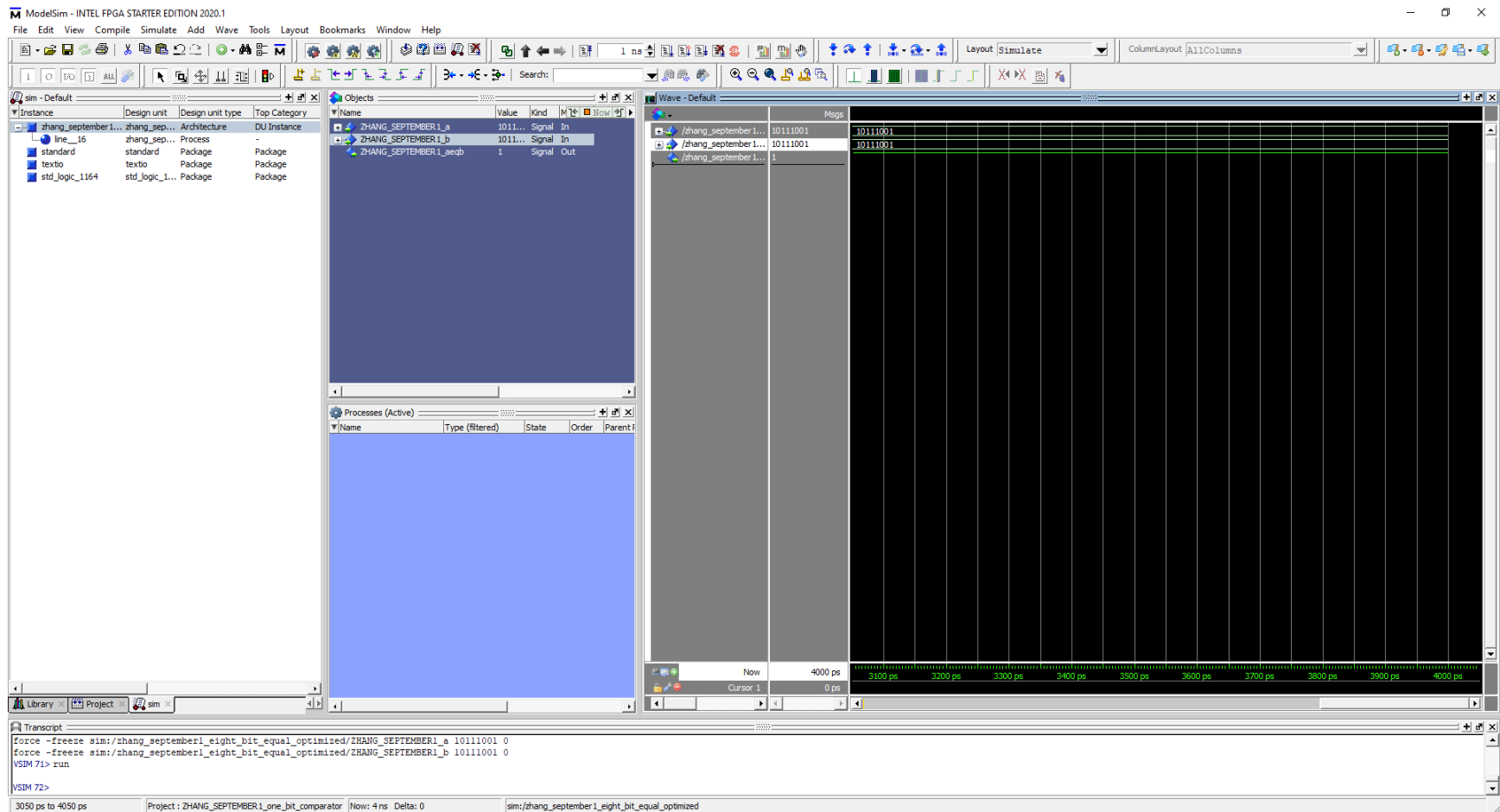
Inputted 01010101, 00010101 which outputted 0. Following the test bench logic, this should be the scenario therefore correct

Task A3 : 8-bit Comparator optimized, Chue Zhang



Inputted 01100101, 11111001 which outputted 0 which is correct according to the test bench.

Task A3 : 8-bit Comparator optimized, Chue Zhang



Input 10111001, 10111001 output 1. So in conclusion, so as long as both inputs share the same values, output 1 is guaranteed and this also helps to verify the correctness of the design of the 8 bit optimized comparator