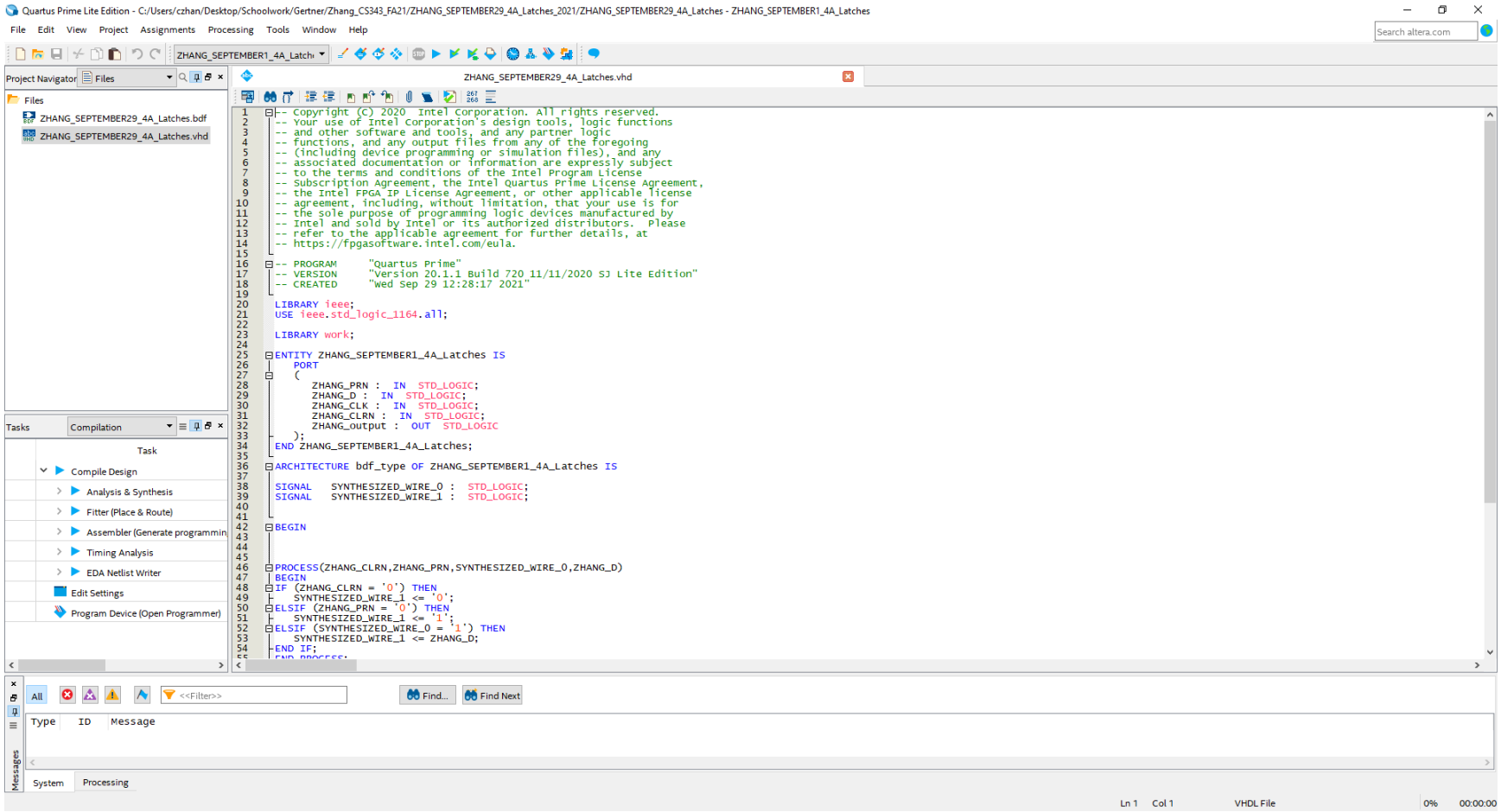
Review Lab : Master Slave

Chue Zhang

Csc343 Fall 2021

Professor Gertner


Quartus Prime Lite Edition - C:/Users/czhan/Desktop/Schoolwork/Gertner/Zhang_CS343_FA21/ZHANG_SEPTEMBER29_4A_Latches_2021/ZHANG_SEPTEMBER29_4A_Latches - ZHANG_SEPTEMBER1_4A_Latches
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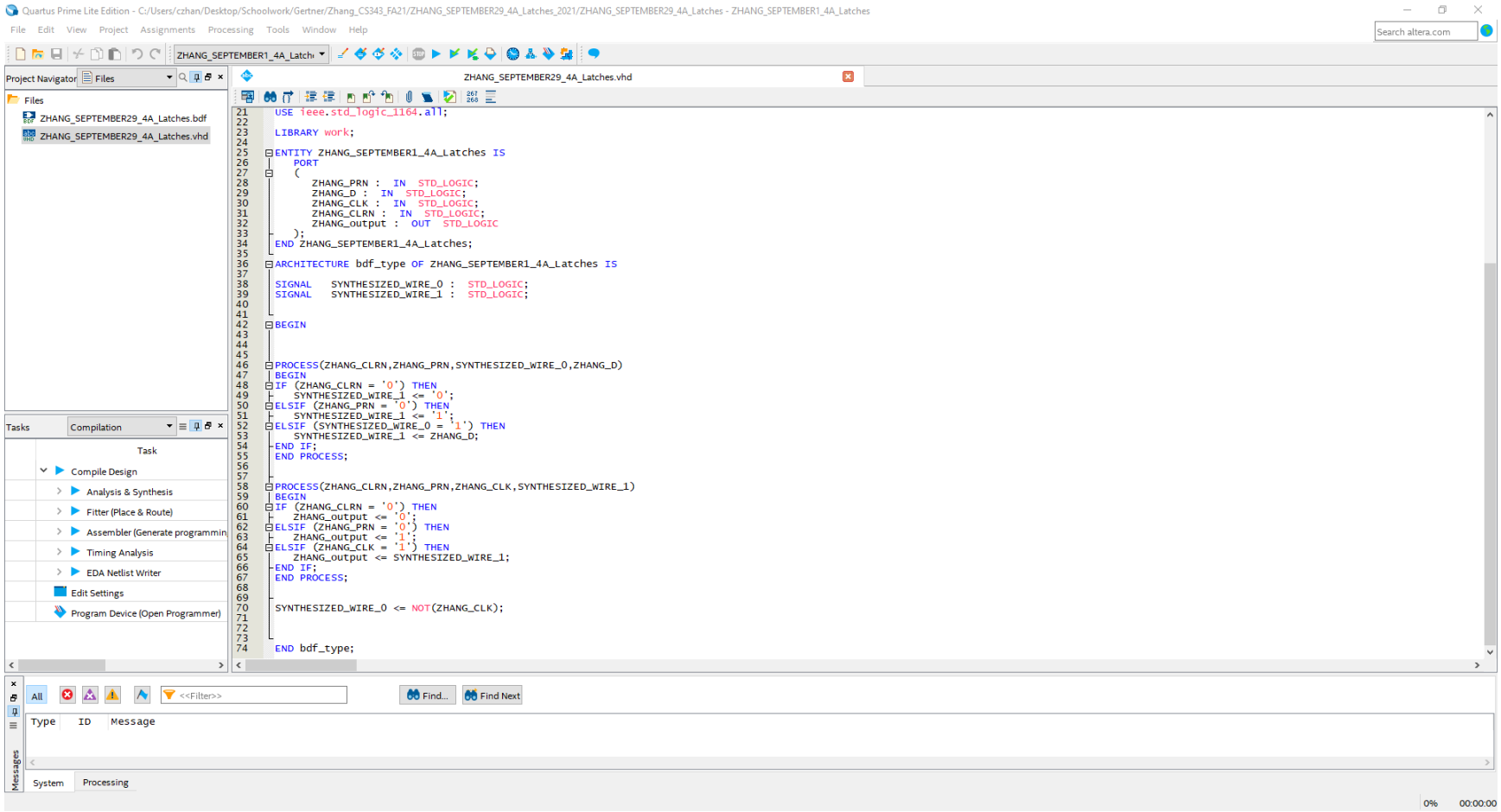
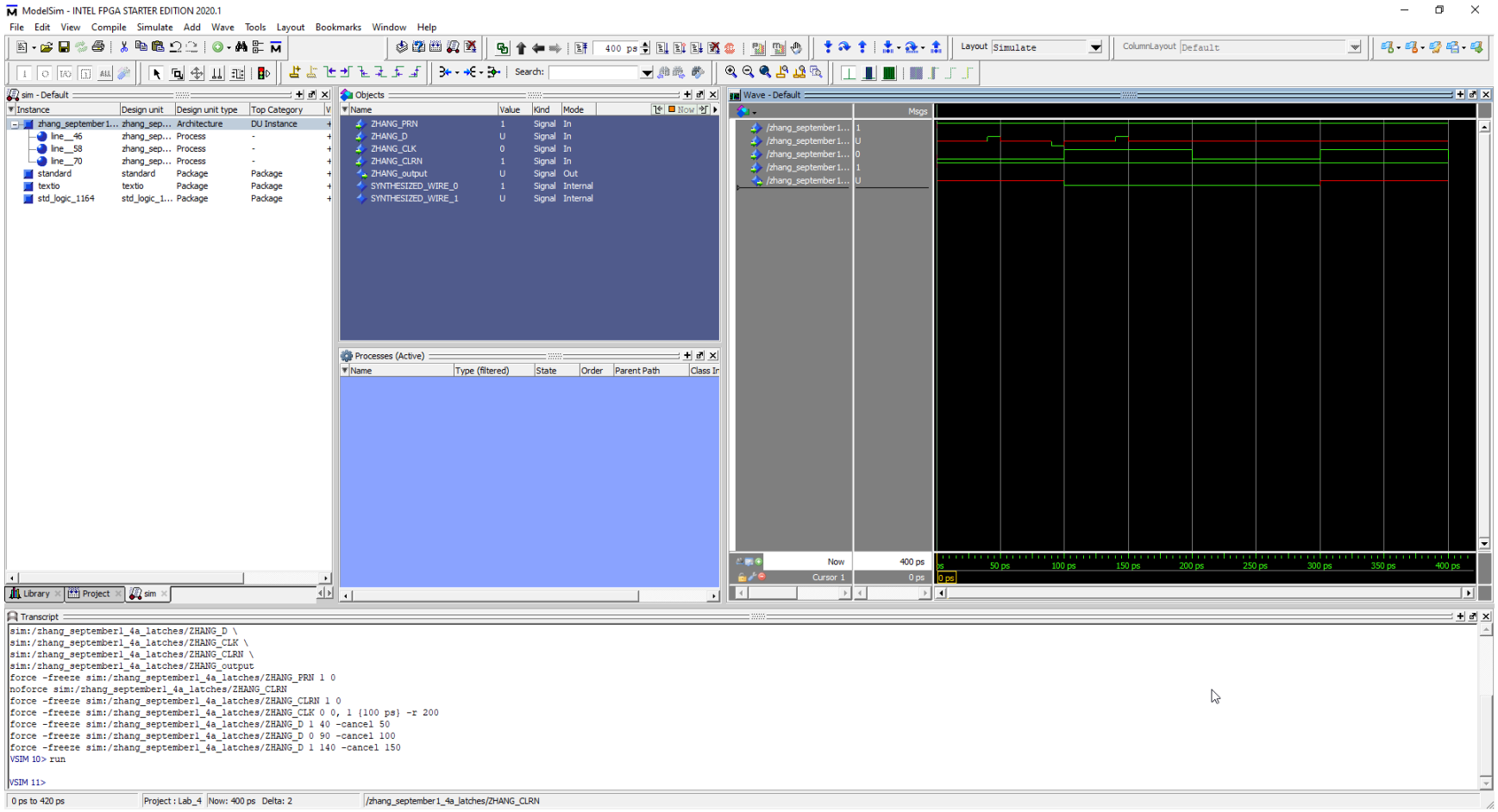
-- https://fpgasoftware.intel.com/eula.
-- PROGRAM "Quartus Prime"
-- VERSION "Version 20.1.1 Build 720 11/11/2020 SJ Lite Edition"
-- CREATED "Wed Sep 29 12:28:17 2021"
LIBRARY ieee;
USE ieee.std_logic_1164.all;
LIBRARY work;
ENTITY ZHANG_SEPTEMBER1_4A_Latches IS
PORT
(
ZHANG_PRN : IN STD_LOGIC;
ZHANG_D : IN STD_LOGIC;
ZHANG_CLK : IN STD_LOGIC;
ZHANG_CLRN : IN STD_LOGIC;
ZHANG_output : OUT STD_LOGIC
);
END ZHANG_SEPTEMBER1_4A_Latches;
ARCHITECTURE bdf_type OF ZHANG_SEPTEMBER1_4A_Latches IS
SIGNAL SYNTHESIZED_WIRE_0 : STD_LOGIC;
SIGNAL SYNTHESIZED_WIRE_1 : STD_LOGIC;
BEGIN
PROCESS(ZHANG_CLRN,ZHANG_PRN,SYNTHESIZED_WIRE_0,ZHANG_D)
BEGIN
IF (ZHANG_CLRN = '0') THEN
SYNTHESIZED_WIRE_1 <= '0';
ELSIF (ZHANG_PRN = '0') THEN
SYNTHESIZED_WIRE_1 <= '1';
ELSIF (SYNTHESIZED_WIRE_0 = '1') THEN
SYNTHESIZED_WIRE_1 <= ZHANG_D;
END IF;
Tasks
Compilation
Task
Compile Design
Analysis & Synthesis
Fitter (Place & Route)
Assembler (Generate programmin
Timing Analysis
EDA Netlist Writer
Edit Settings
Program Device (Open Programmer)
All
<<Filter>>
Find...
Find Next
Type ID Message
Messages
System
Processing
Ln 1 Col 1 VHDL File 0% 00:00:00



Lpm generated D latches which were used to create a master slave flip flop design.



Clock is at 200ps intervals with input data D at 40ps-50ps, 90ps-100ps, 140ps-150ps. First input nothing because not positive edge triggered, second input is positive edge triggered so you notice output result and third input is no changes.