Review Lab : Register
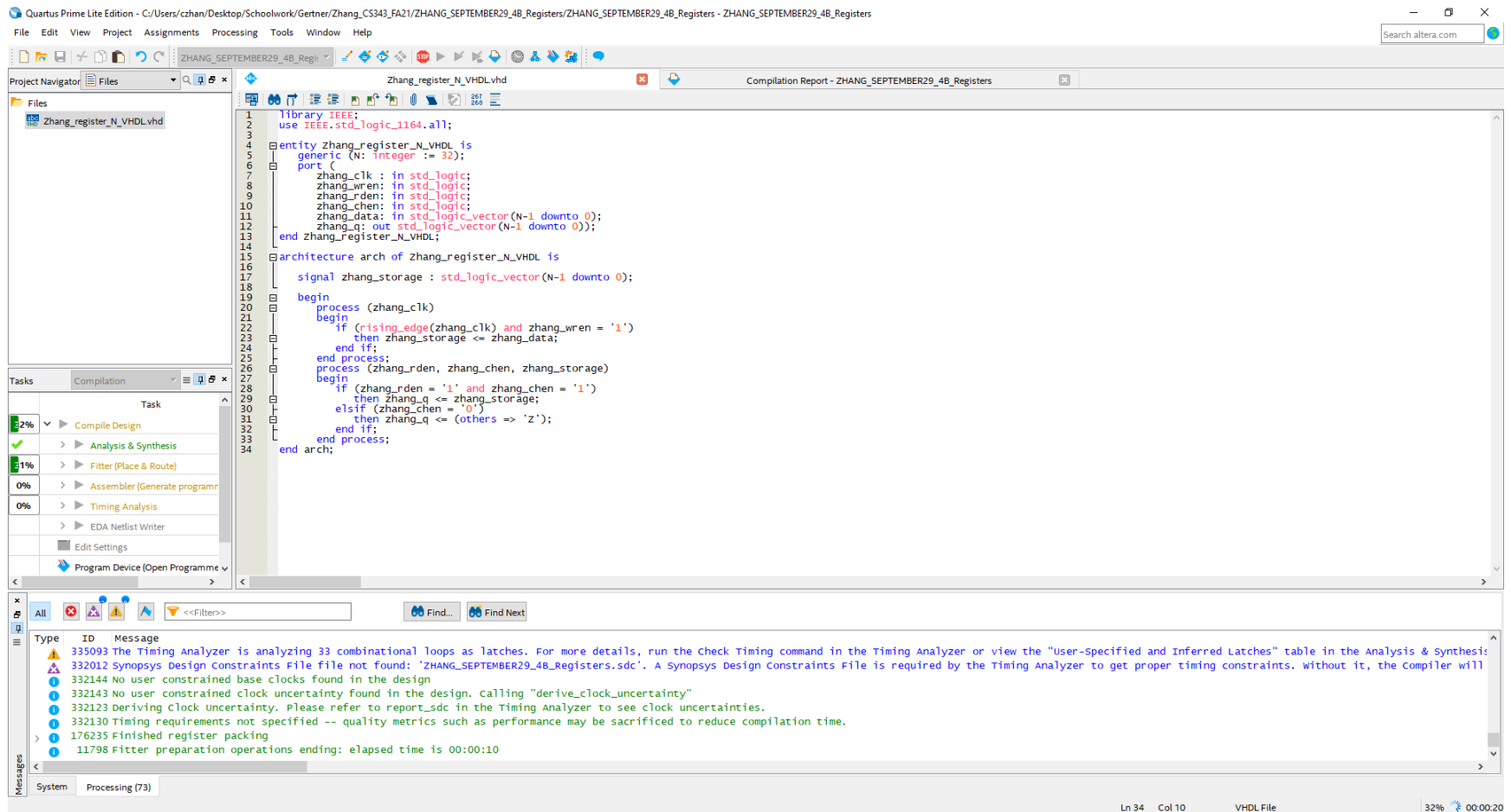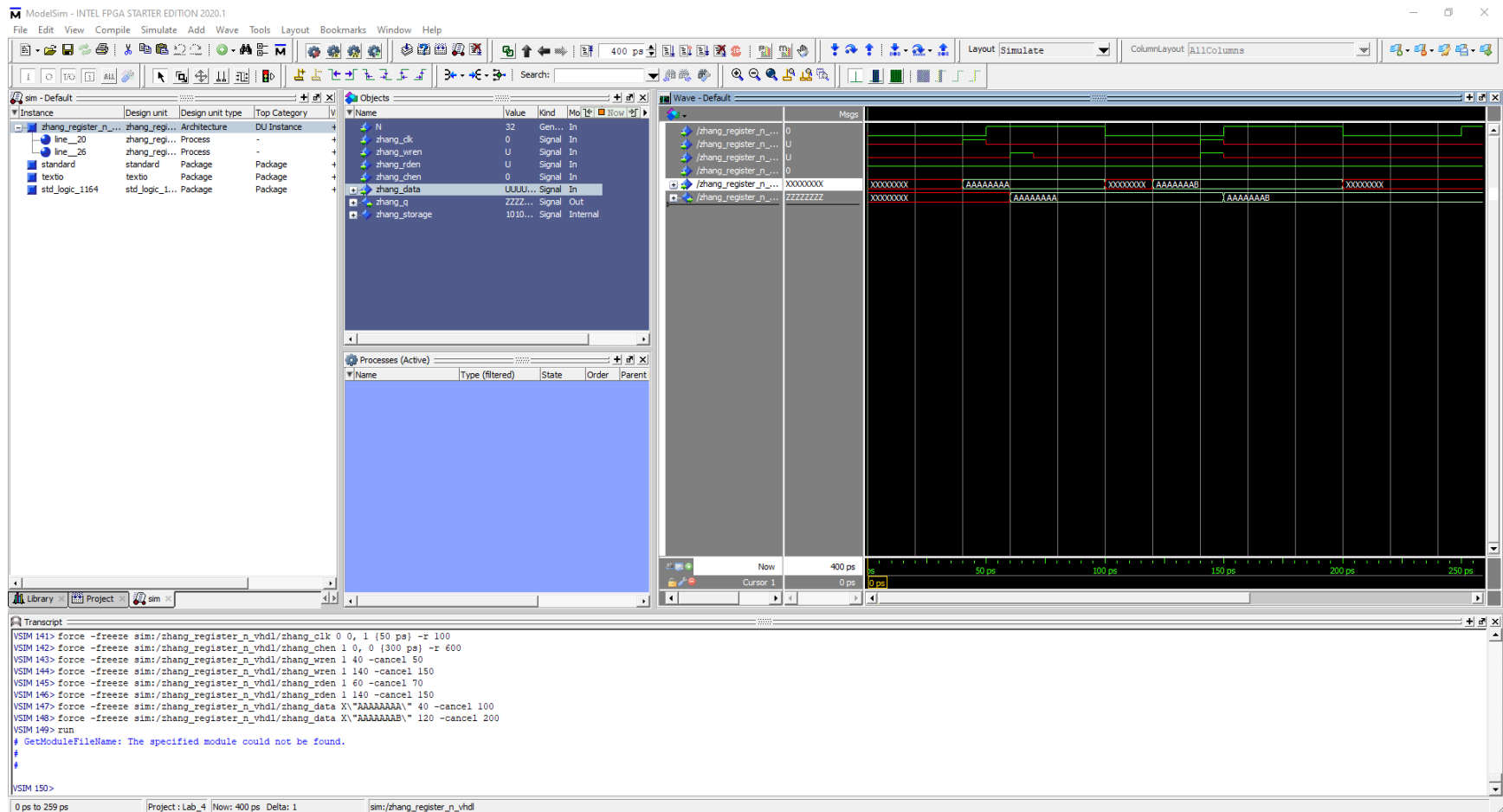
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Csc343 Fall 2021

Professor Gertner

VHDL code of the N bit register

Inputted in data values of AAAAAAAA and AAAAAAAB and as you can notice, both have been inputted into the storage register as shown in the result. Values written in 40 to 50 and inputted at 40 to 50 then read and outputted at 60~. Same thing applies for second input as you can see result at 140~