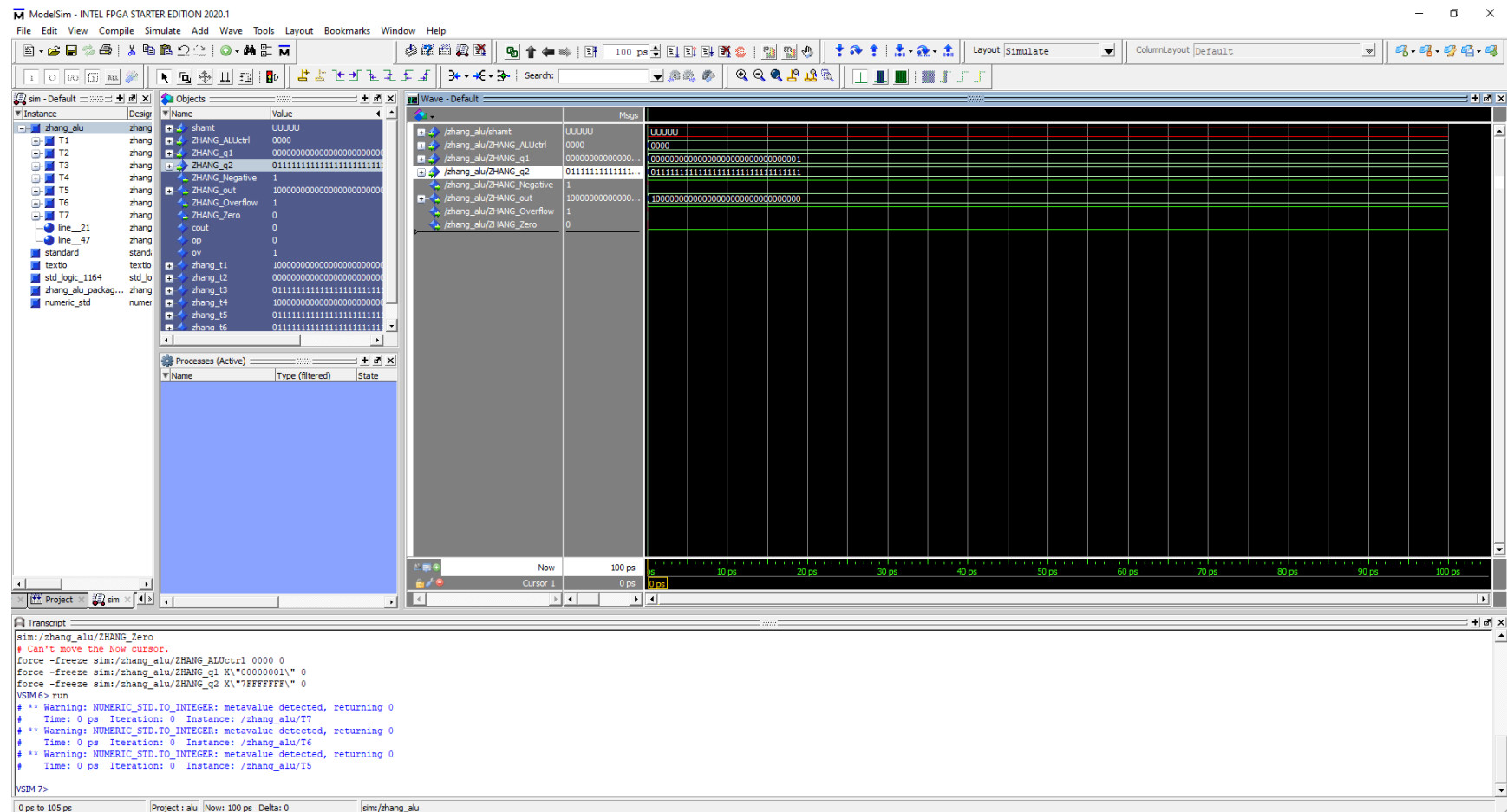


ALU : Waveforms

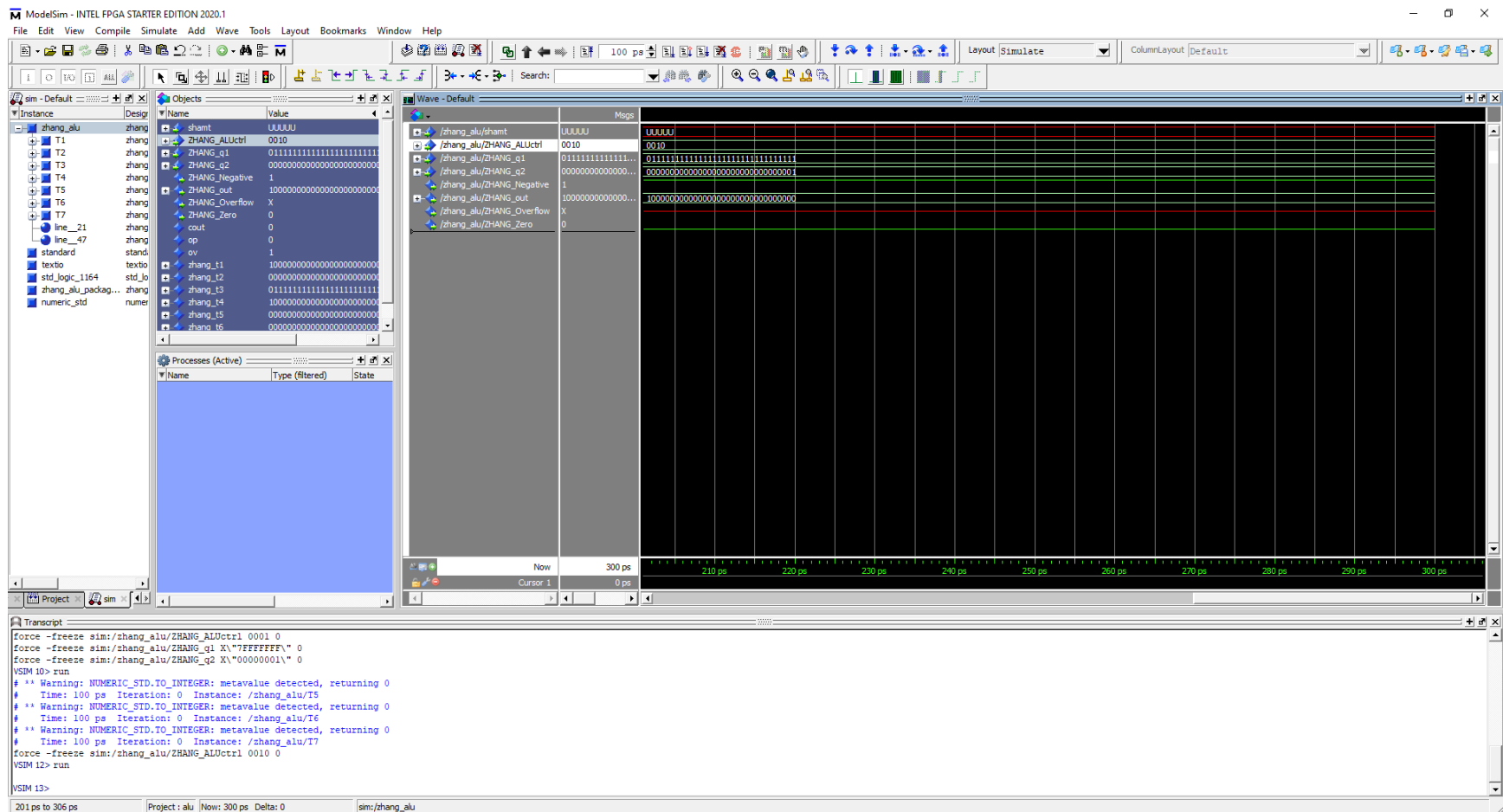
Chue Zhang

Csc343 Fall 2021

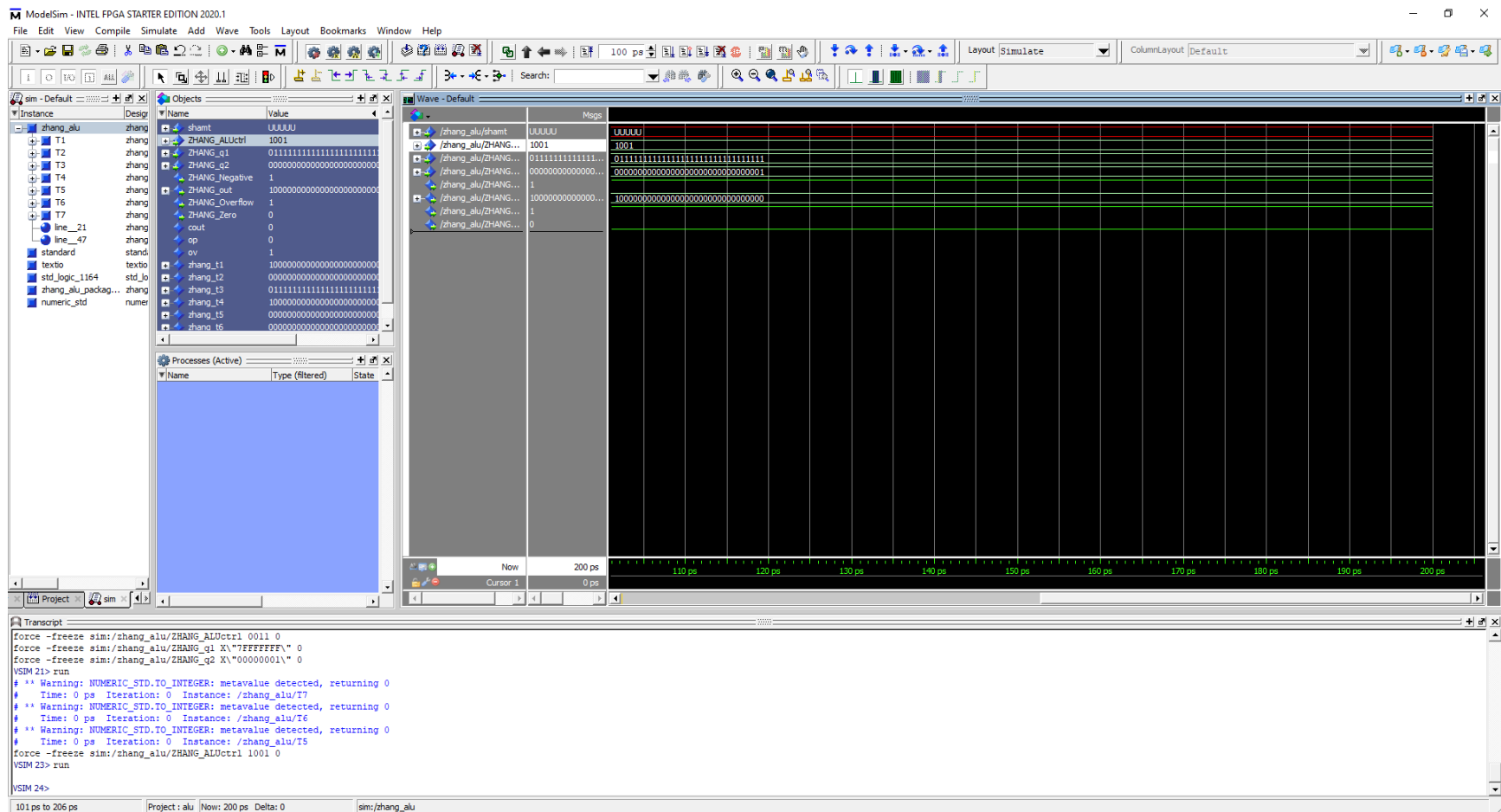
Professor Gertner



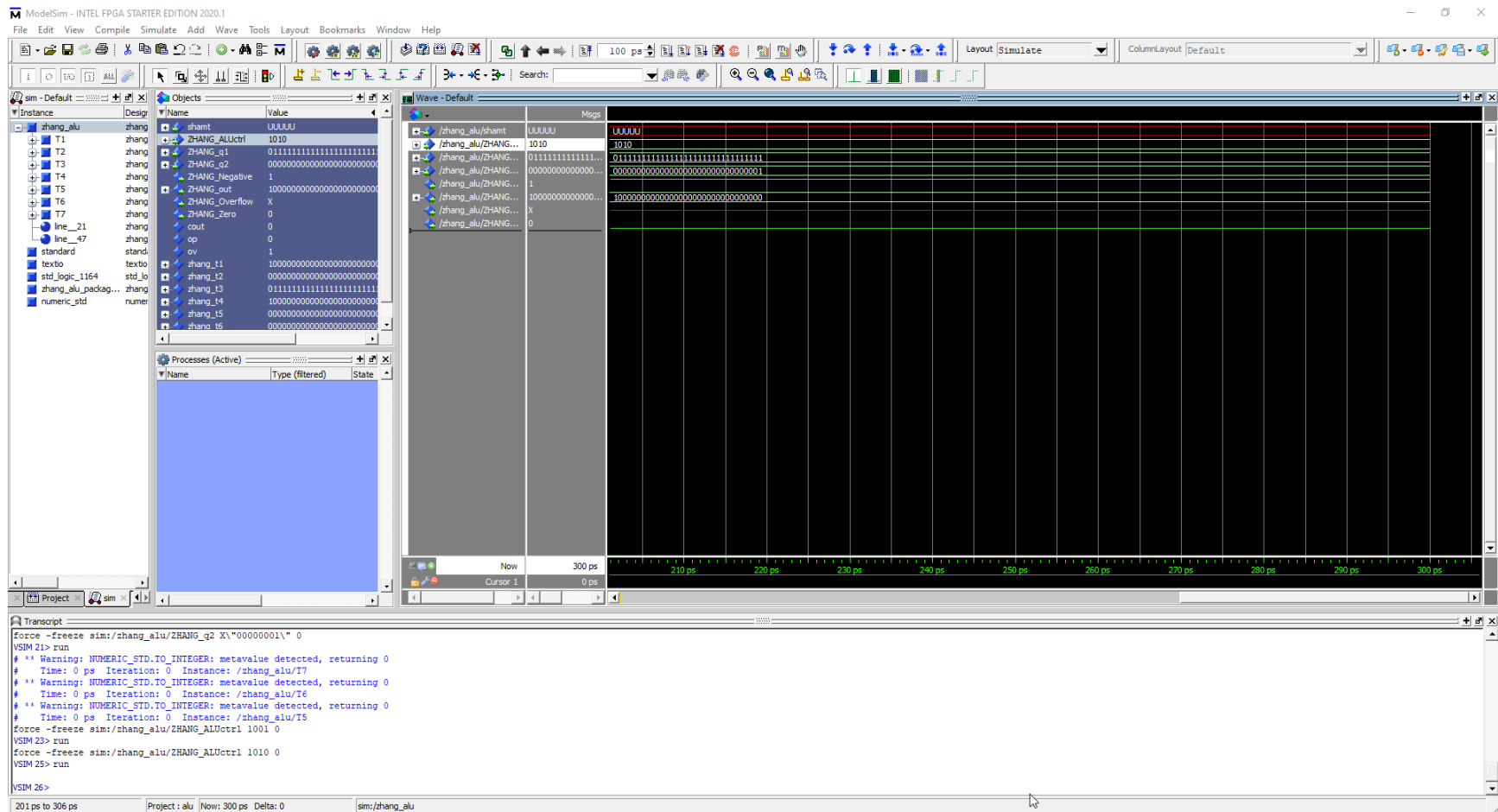
Op code = 0000, 7FFF FFFF add 0000 0001, Output = 8000 0000, All flags shown. Takes two operands and perform add operation onto them



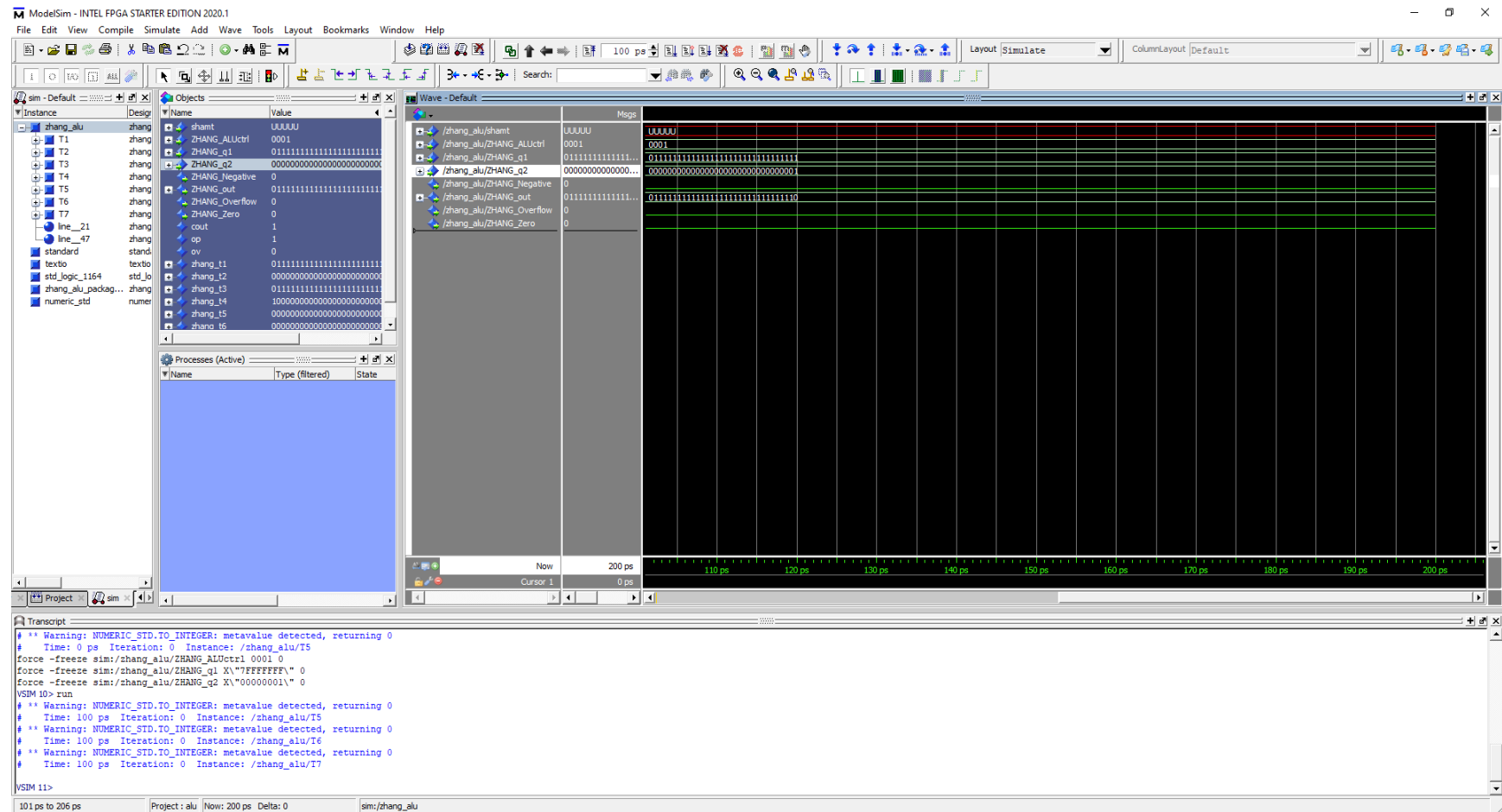
Opcode = 0010, 7FFF FFFF addu 0000 0001, Output = 8000 0000 with no overflow. Takes two operands and performs add operation on them and returns no overflow flag.



Opcode: 1001, 7FFF FFFF addi 0000 0001, Output = 8000 0000 with overflow flag. Performs Addi operation on operand 1 and imm16 with sign extension.



Opcode = 1010, 7FFF FFFF addiu 0000 0001, Output = 8000 0000 with no overflow. Addi performed on operand 1 and imm16 with sign extension without overflow flag.



Opcode = 0001, 7FFF FFFF – 0000 0001 = 7FFF FFFE, All flags shown. Sub performed on operands with overflow flags.

The screenshot shows the ModelSim interface for a simulation of a Subu operation. The Design Hierarchy on the left lists various components including T1 through T7, line_21, line_47, standard, textio, std_logic_1164, zhang_alu_package, and numeric_std. The Objects list in the center shows the internal components of the zhang_alu, including ZHANG_ALUctrl, ZHANG_q1, ZHANG_q2, ZHANG_Negative, ZHANG_out, ZHANG_Overflow, ZHANG_Zero, cout, op, ov, zhang_t1 through zhang_t5. The Wave window on the right displays the signals for these components over time, with a cursor at 100 ps. The Transcript window at the bottom shows the simulation commands and warnings.

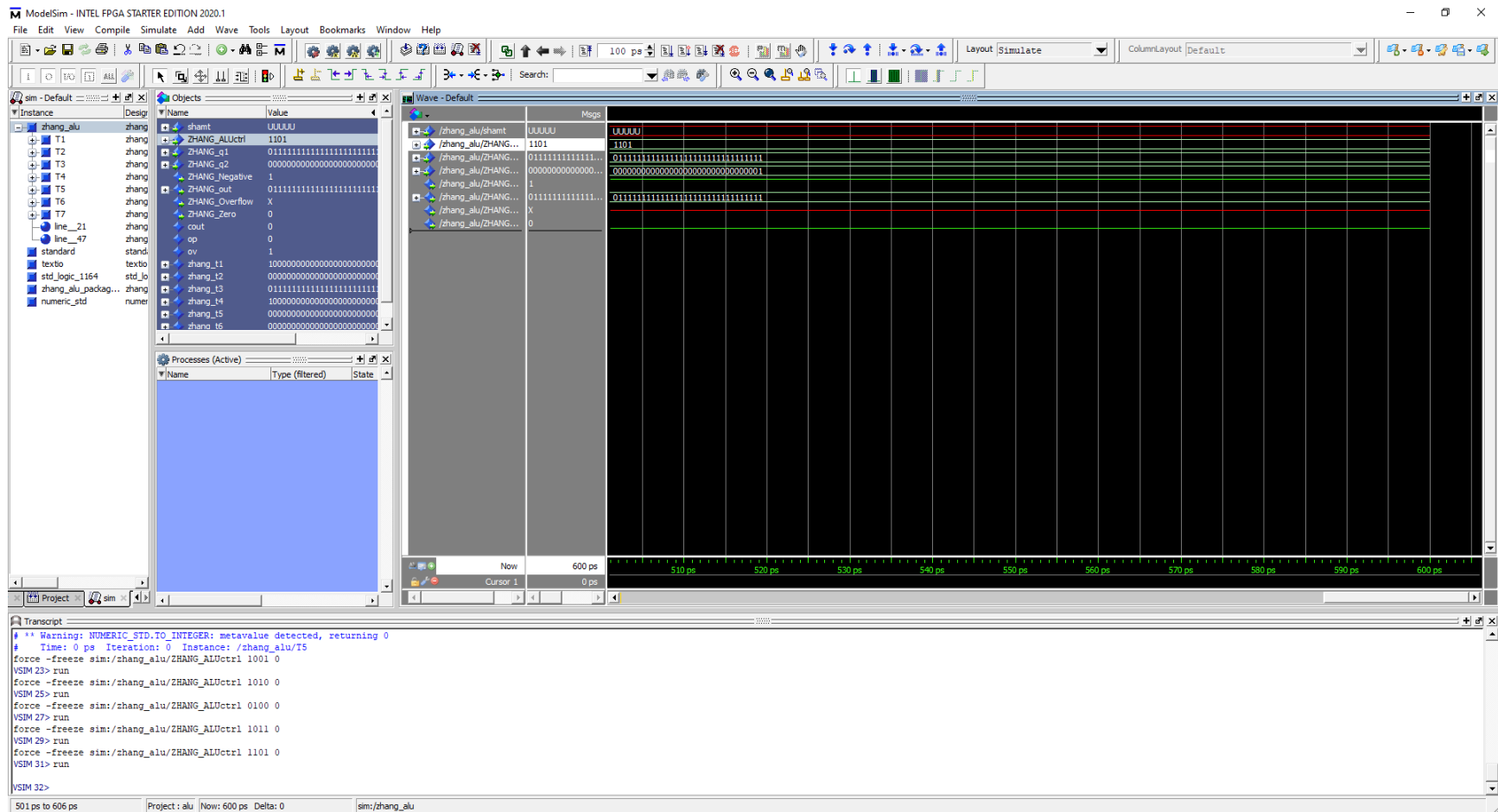
Transcript:

```

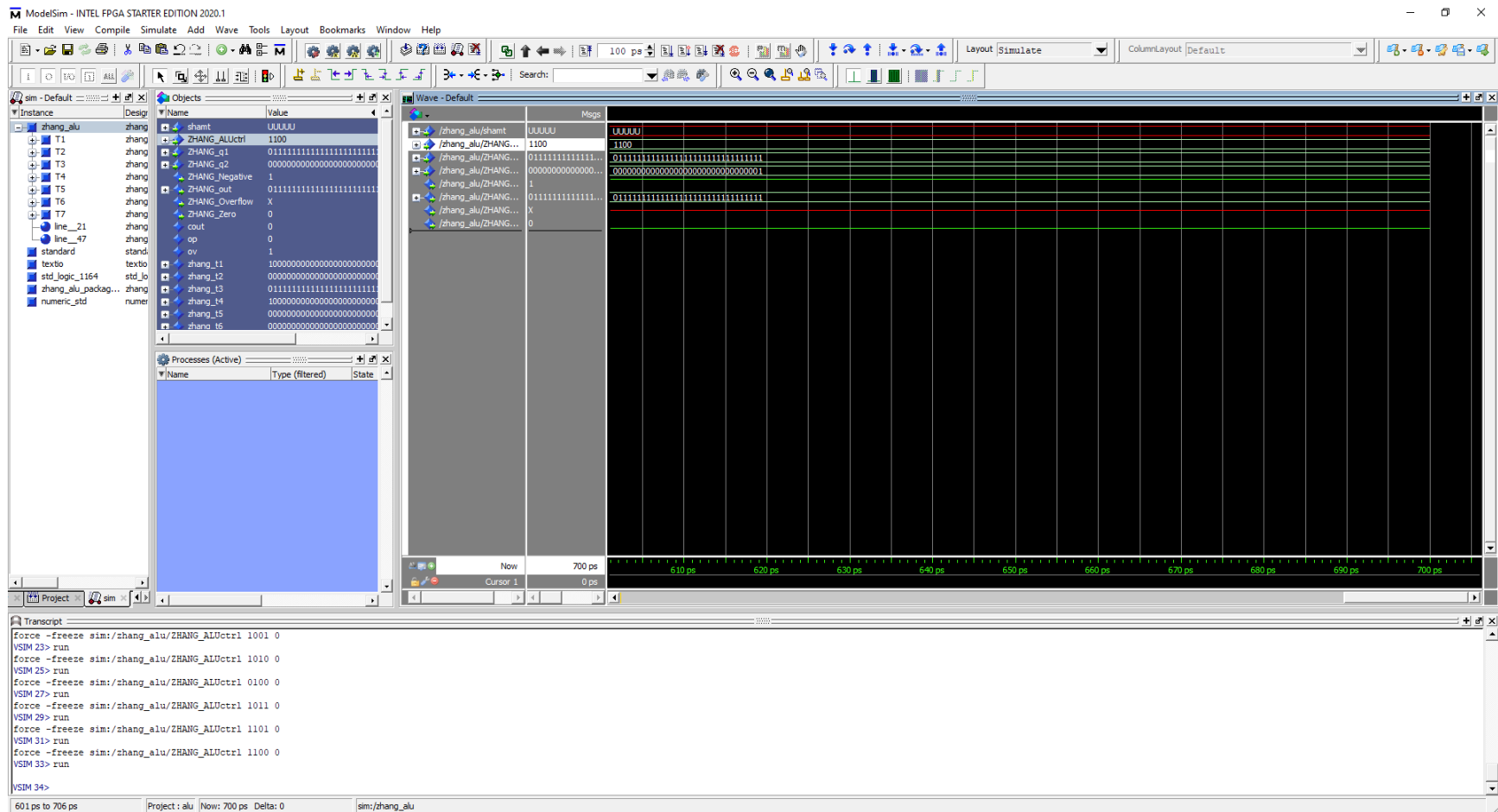
sim:/zhang_alu/ZHANG_Overflow \
sim:/zhang_alu/ZHANG_Zero
force -freeze sim:/zhang_alu/ZHANG_ALUctrl 0011 0
force -freeze sim:/zhang_alu/ZHANG_q1 X"7FFFFFFF" 0
force -freeze sim:/zhang_alu/ZHANG_q2 X"00000001" 0
VSIIM21> run
# ** Warning: NUMERIC_STD.TO_INTEGER: metavalue detected, returning 0
# Time: 0 ps Iteration: 0 Instance: /zhang_alu/T7
# ** Warning: NUMERIC_STD.TO_INTEGER: metavalue detected, returning 0
# Time: 0 ps Iteration: 0 Instance: /zhang_alu/T6
# ** Warning: NUMERIC_STD.TO_INTEGER: metavalue detected, returning 0
# Time: 0 ps Iteration: 0 Instance: /zhang_alu/T5
VSIIM22>
0 ps to 105 ps      Project: alu Now: 100 ps Delta: 0      sim:/zhang_alu

```

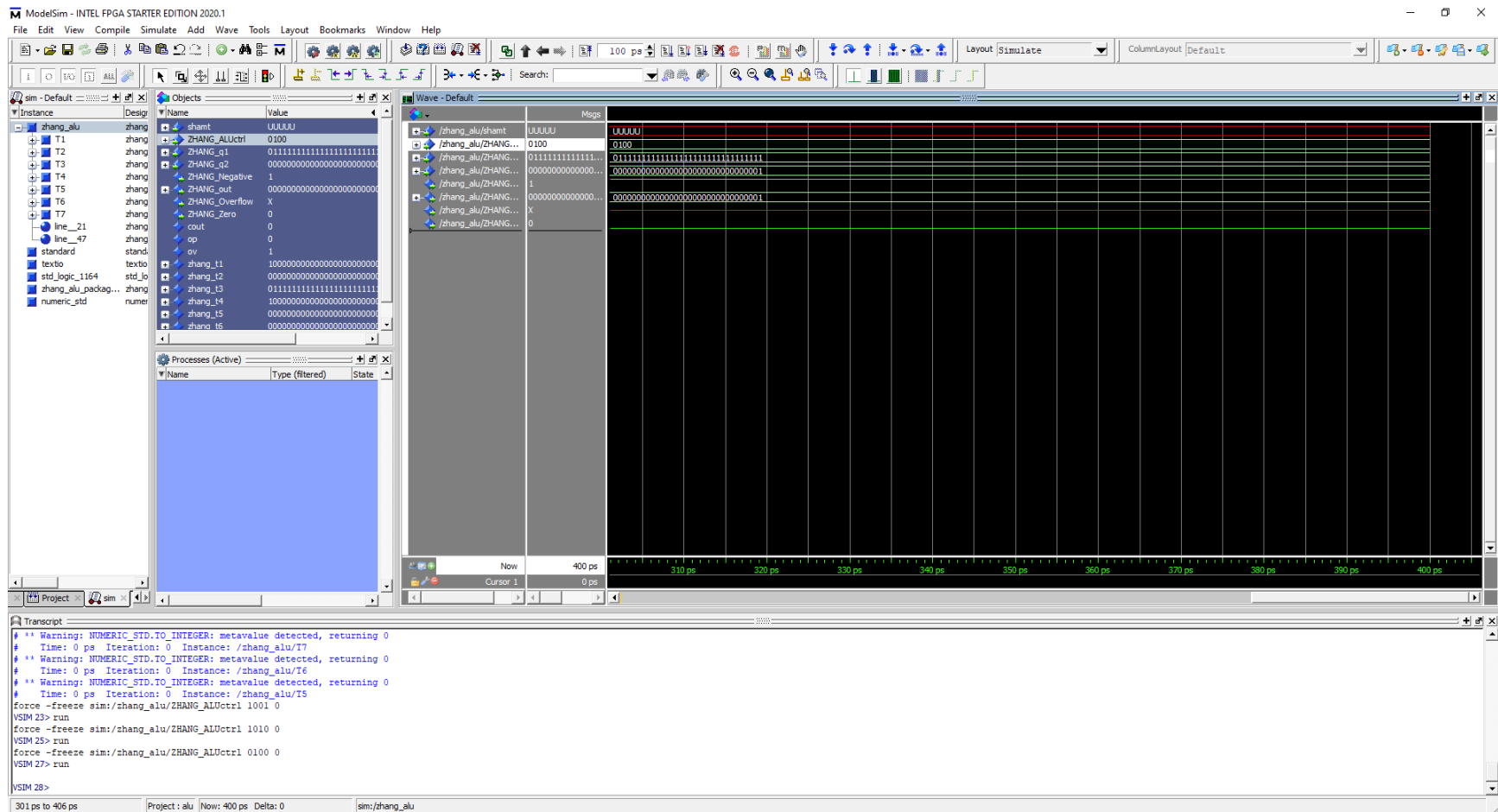
Opcode = 0001, 7FFF FFFF subu 0000 0001 = 7FFF FFFE, no overflow flag shown. Sub Operation performed on both operands without overflow flag



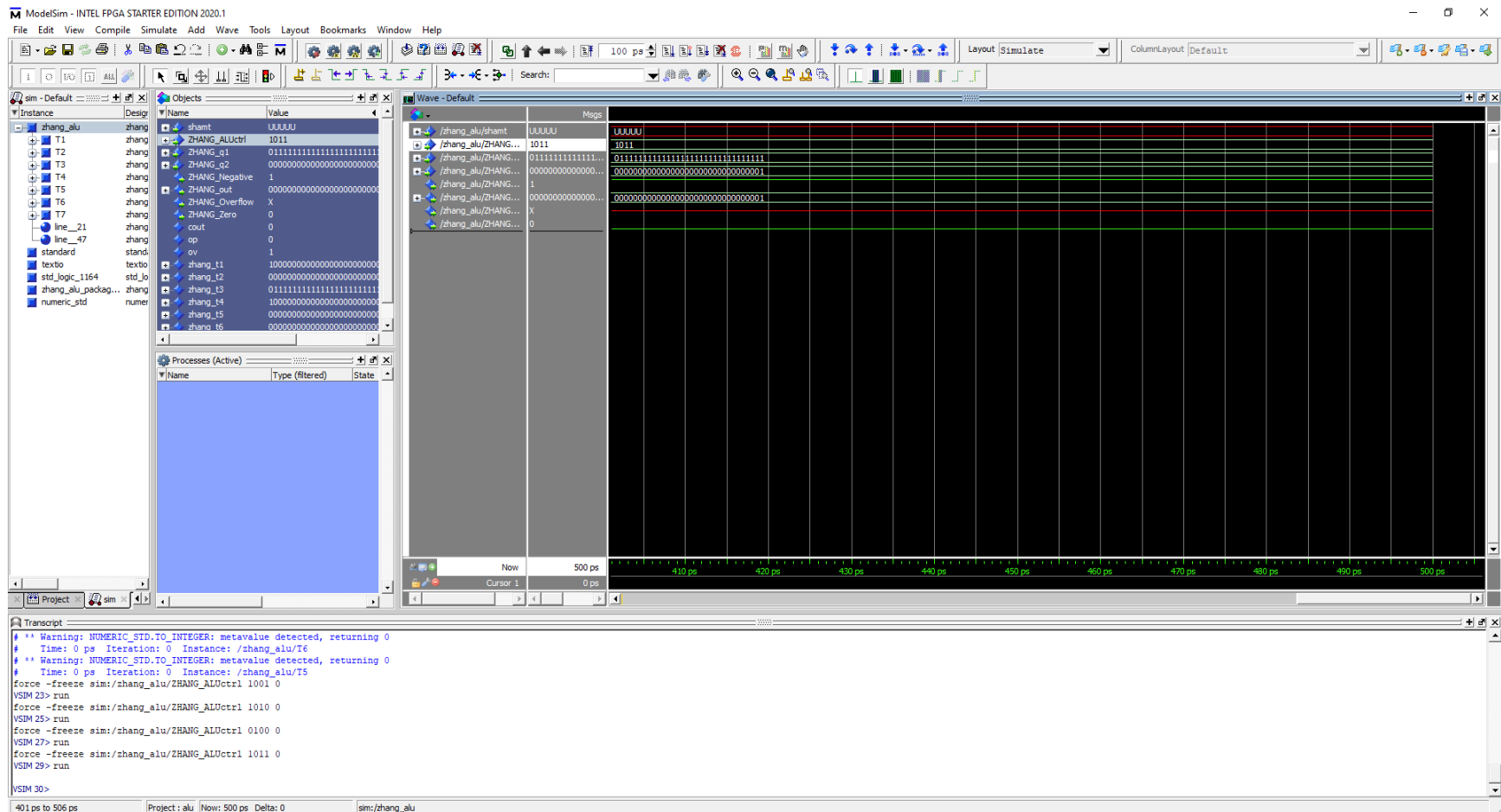
Opcode = 1101, 7FFF FFFF or 0000 0001 = 7FFF FFFF. Or operation performed on both operands.



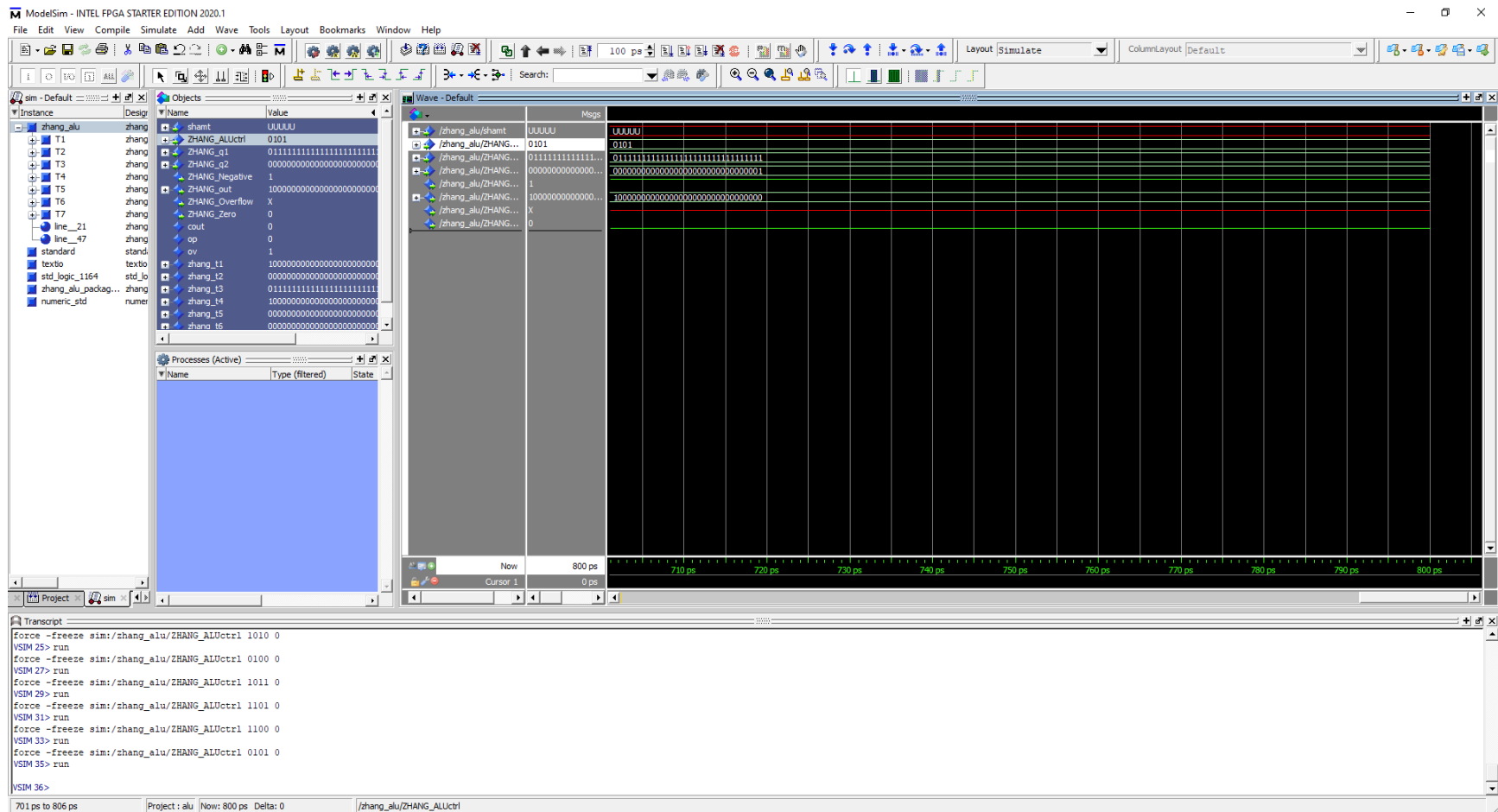
Opcode = 1100, 7FFF FFFF ori 0000 0001 = 7FFF FFFF. Or immediate operation performed on operand1 and imm16 bit with zero extension



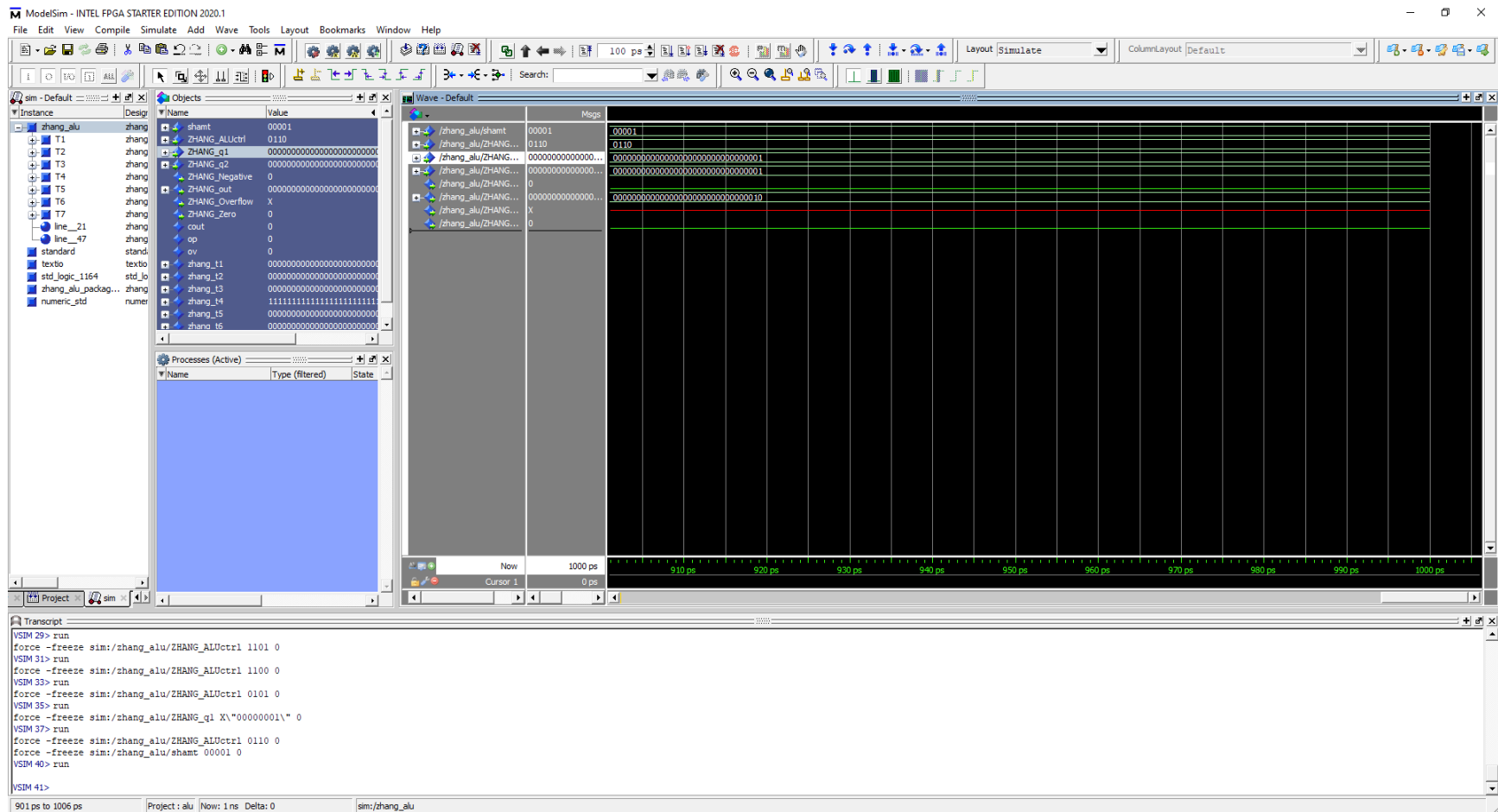
Opcode = 0100, 7FFF FFFF and 0000 0001 = 0000 0001 . And operation performed on both operands.



Opcode = 1011, 7FFF FFFF and 0000 0001. And operation performed with operand 1 and imm16 with zero sign extension



Opcode = 0101, 7FFF FFFF nor 0000 0001 = 8000 0000, NOR operation performed on operand 1 and operand 2



Opcode = 0110, Shamt = 00001, input = 0000 0001, Output = 0000 0010. Shift left operation performed on operand 2 with shift amount of 00001.

