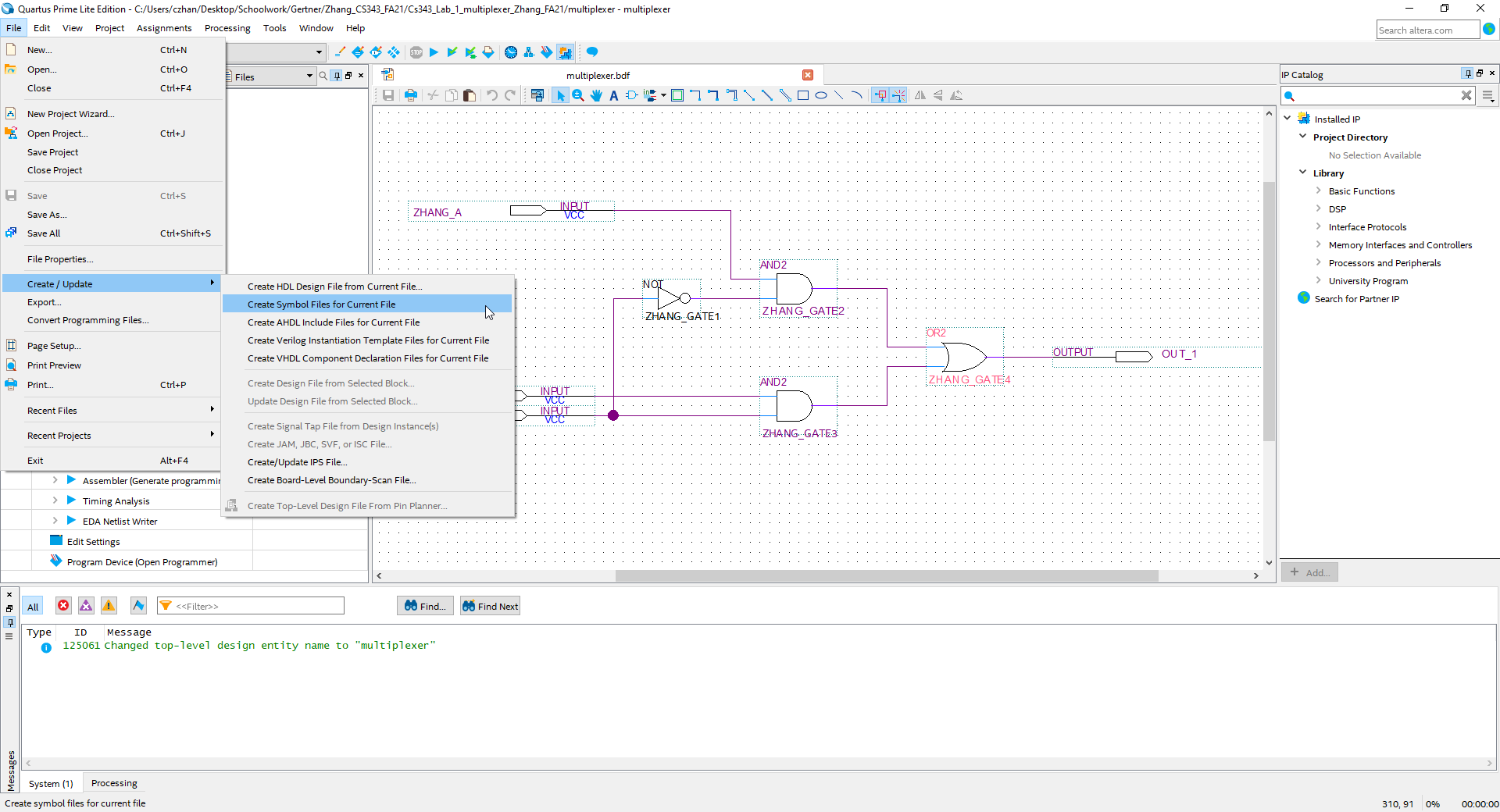
Lab Report : VHDL with LPM

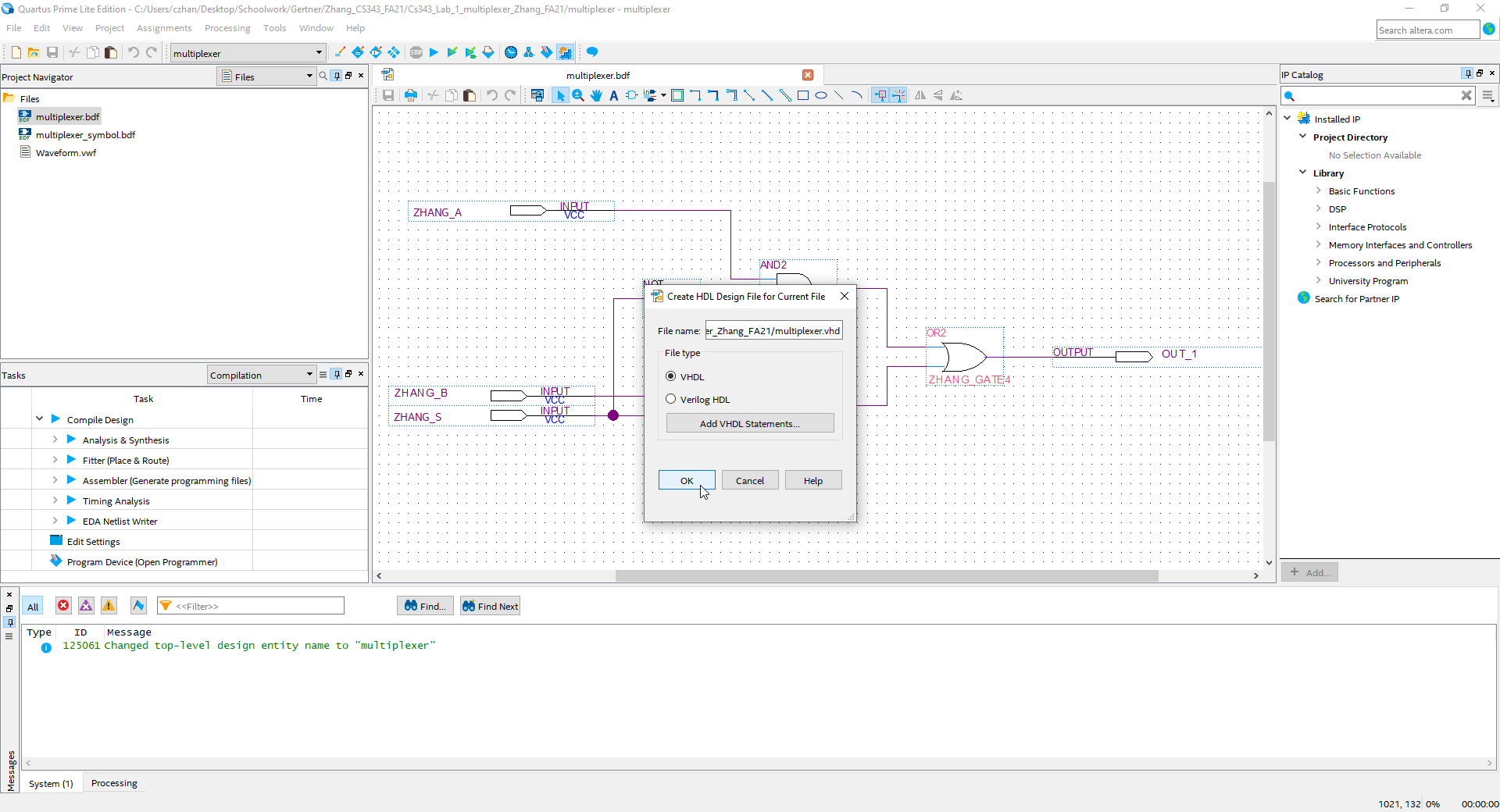
Chue Zhang

Csc343 Fall 2021

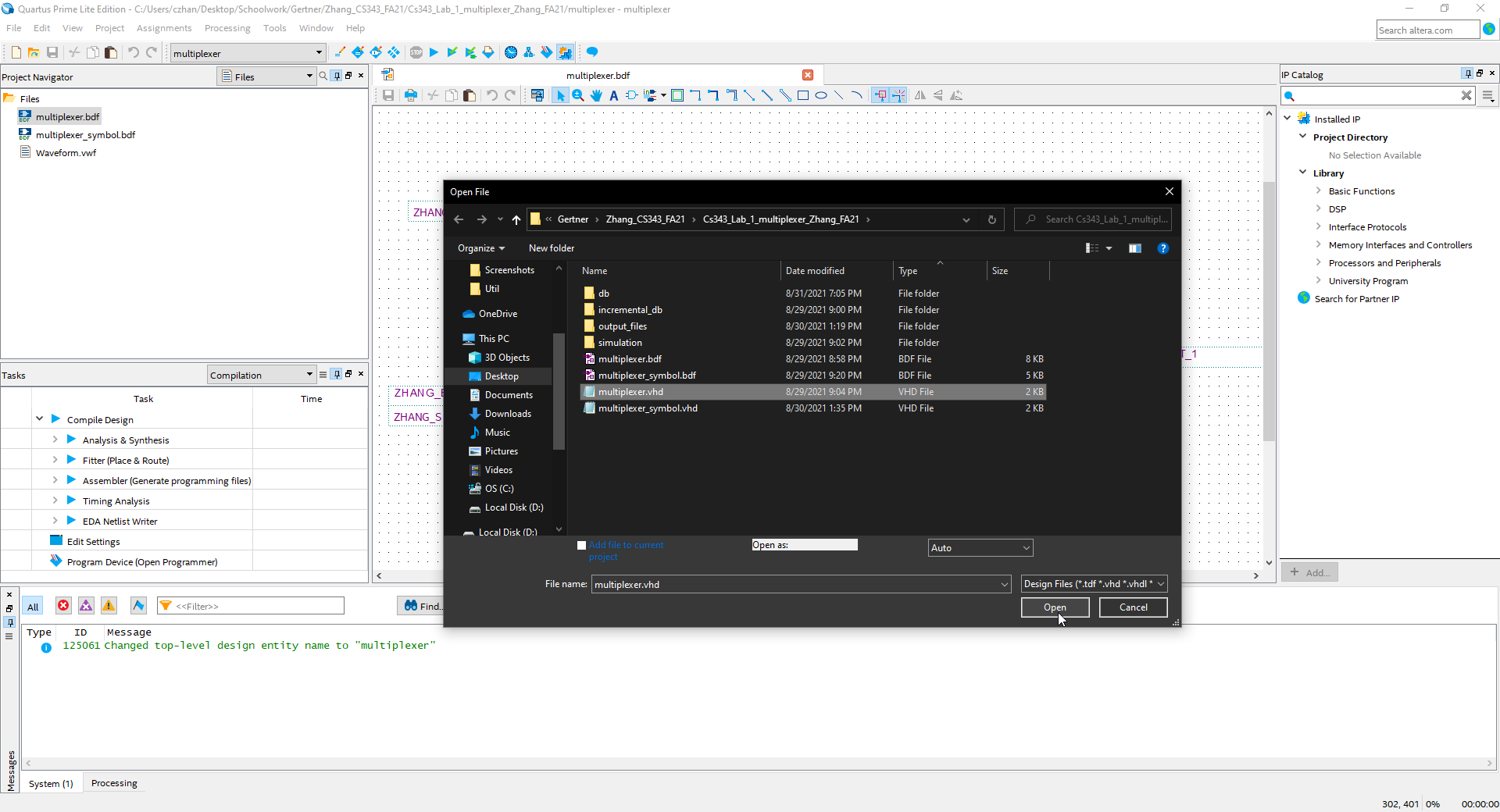
Professor Gertner



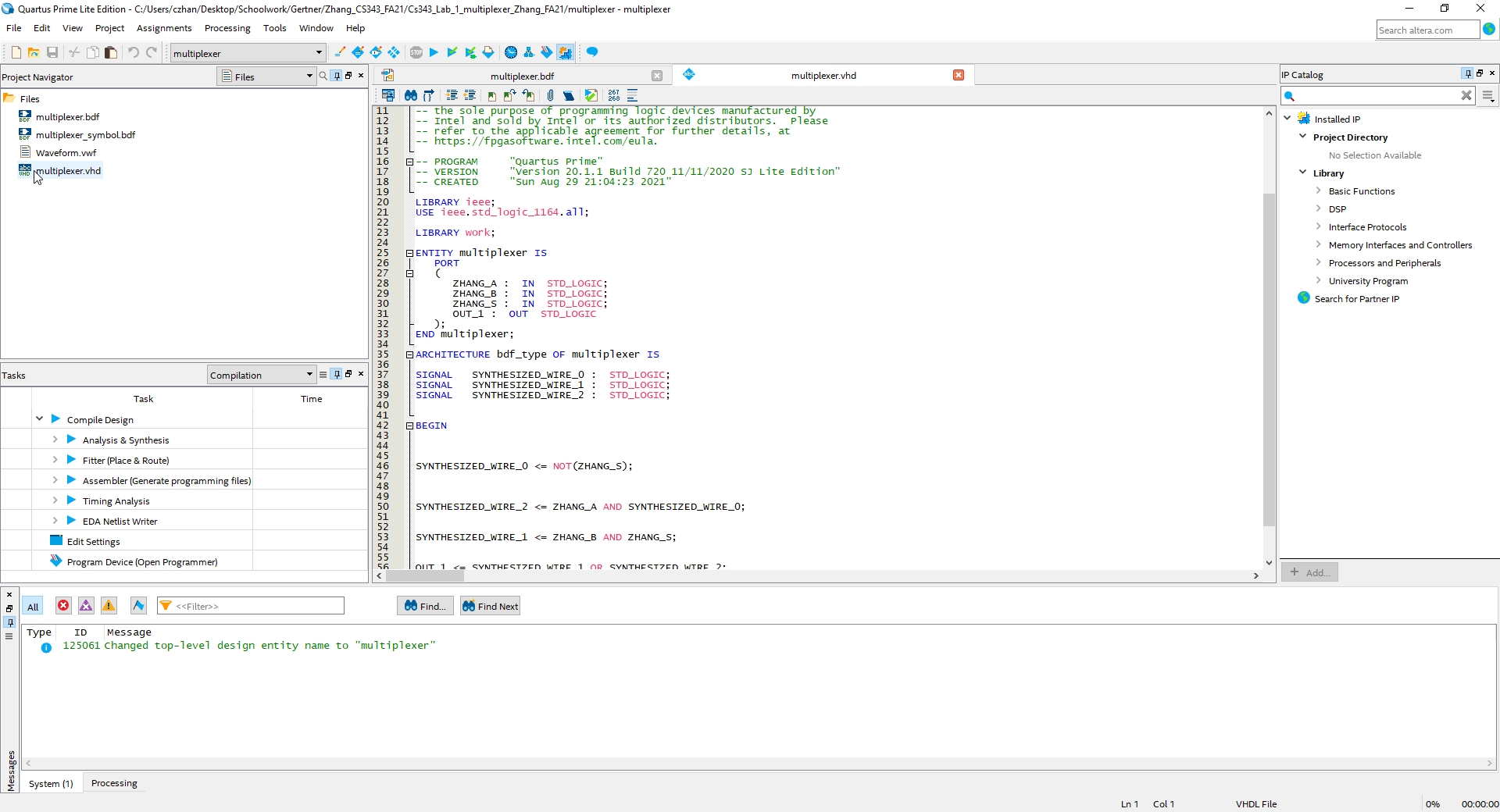
With the 2:1 Mux previously created, I go to the file 🡪 create HDL design File for Current File and a popup should show up



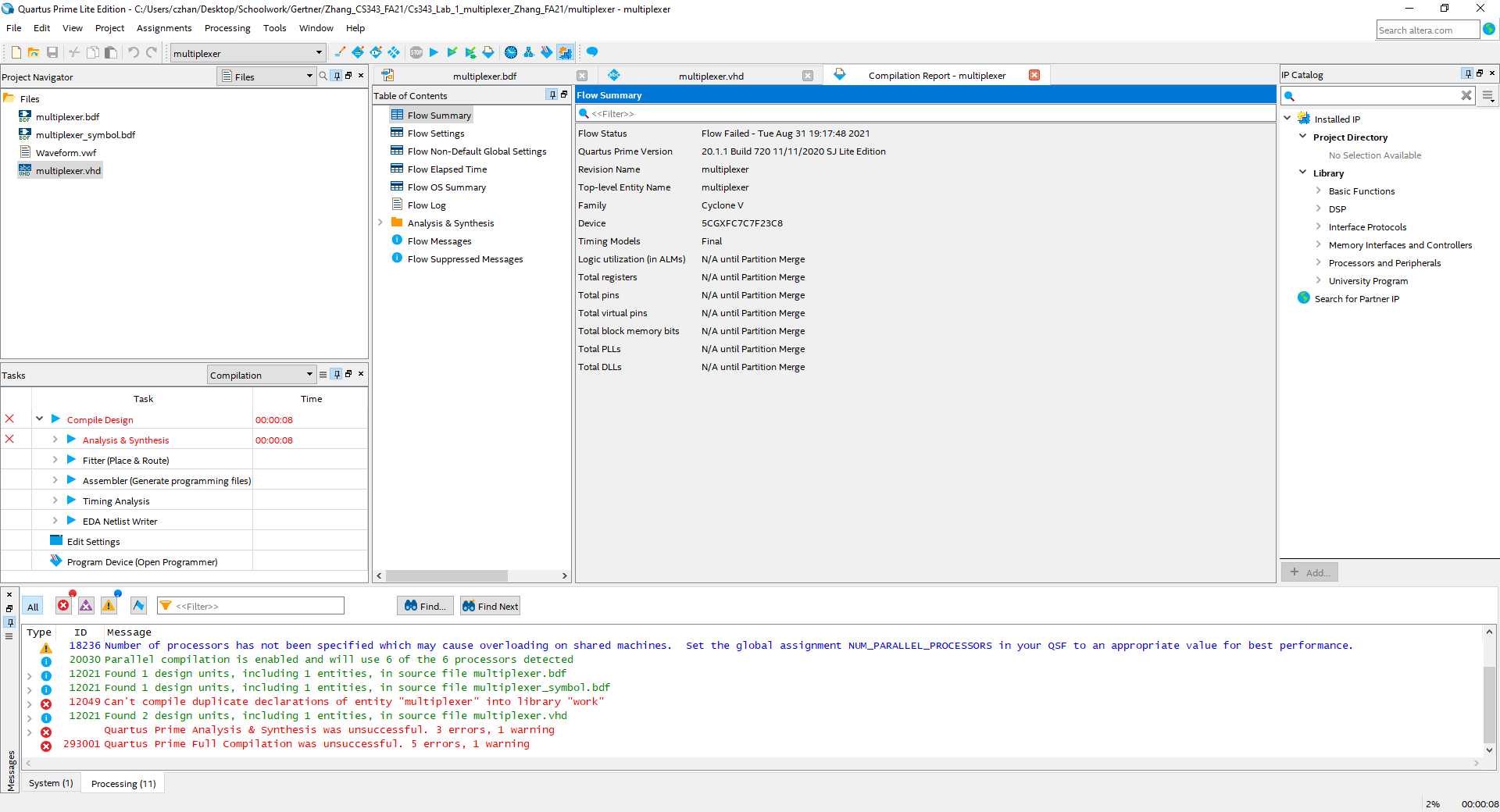
Make sure that the file type is in VHDL not in Verilog and press OK



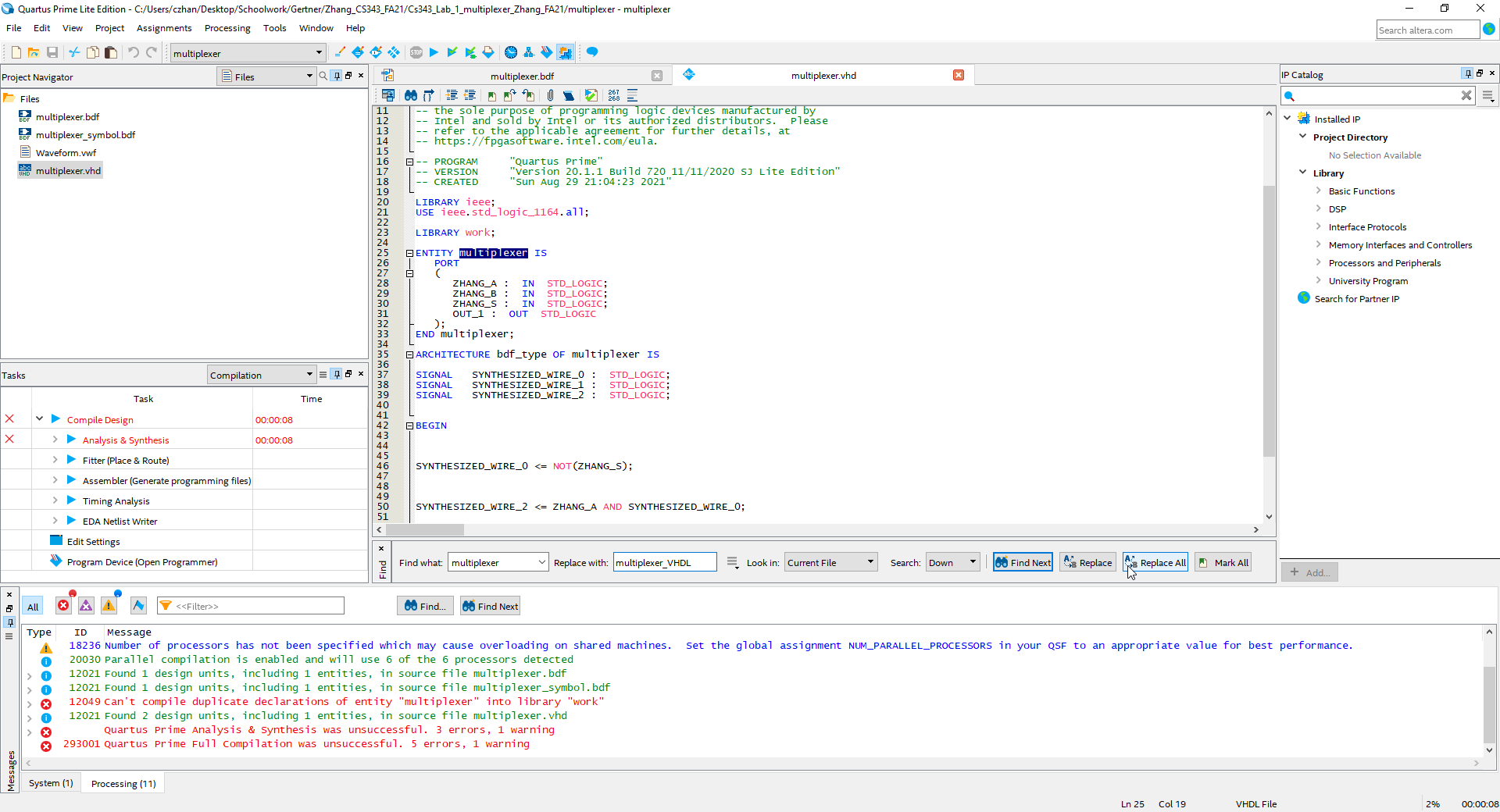
I now add the VHDL file of the design into the files



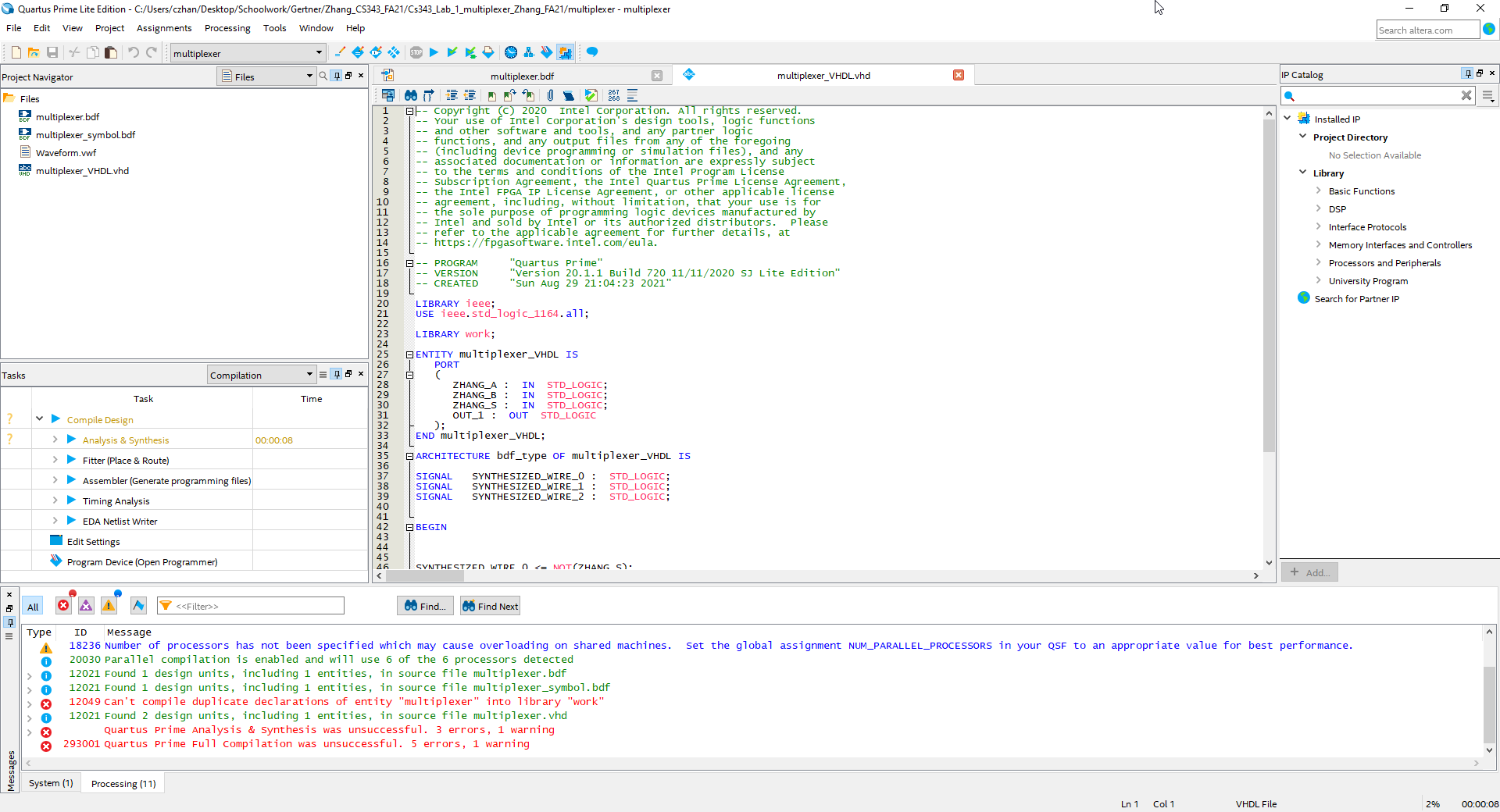
I now set the VHDL file to top level while showcasing some of the code



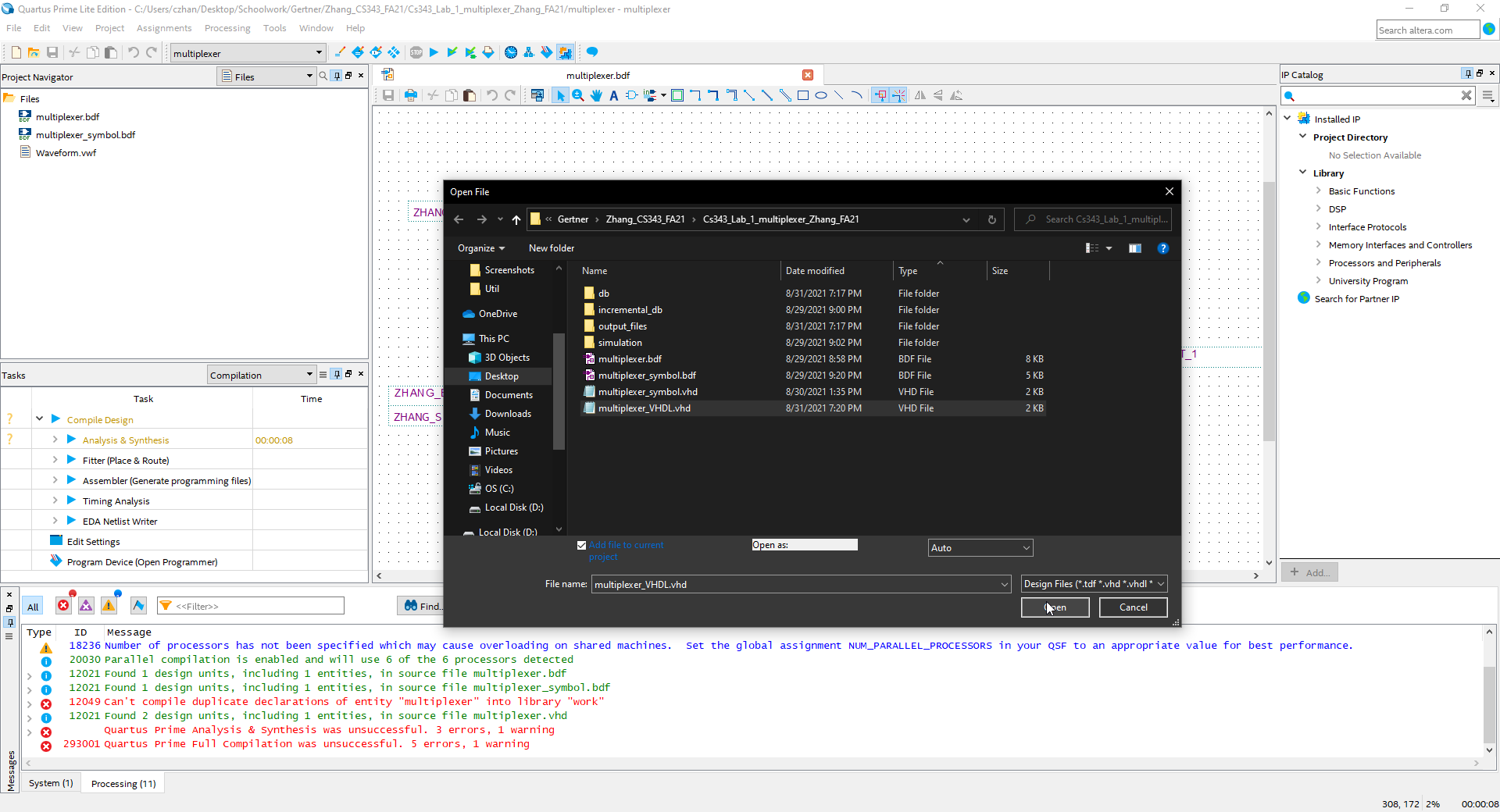
I try to compile but come to an error



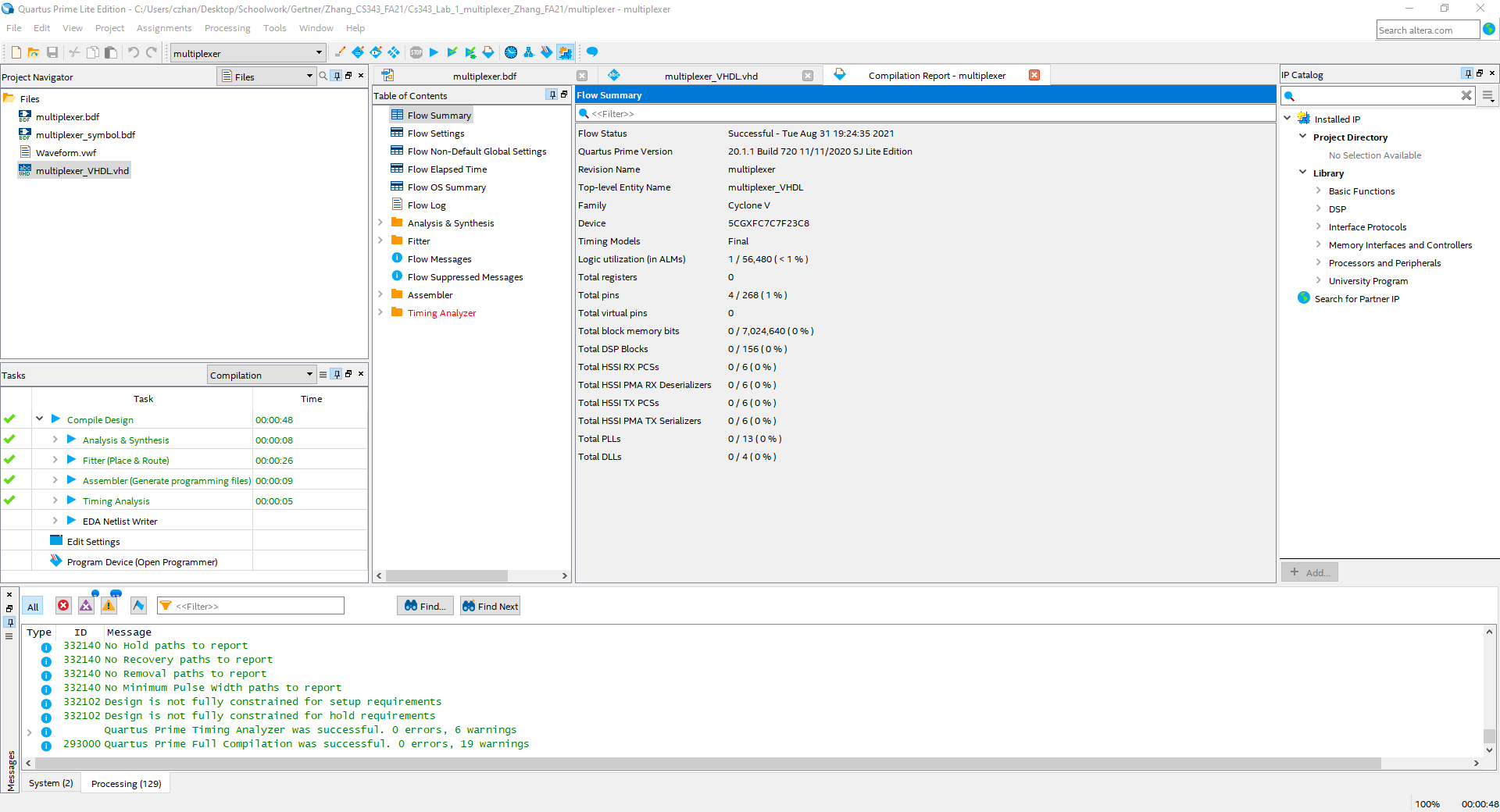
I change the highlighted multiplexer text to multiplexer\_VHDL and save the VHDL file under the new corrected name



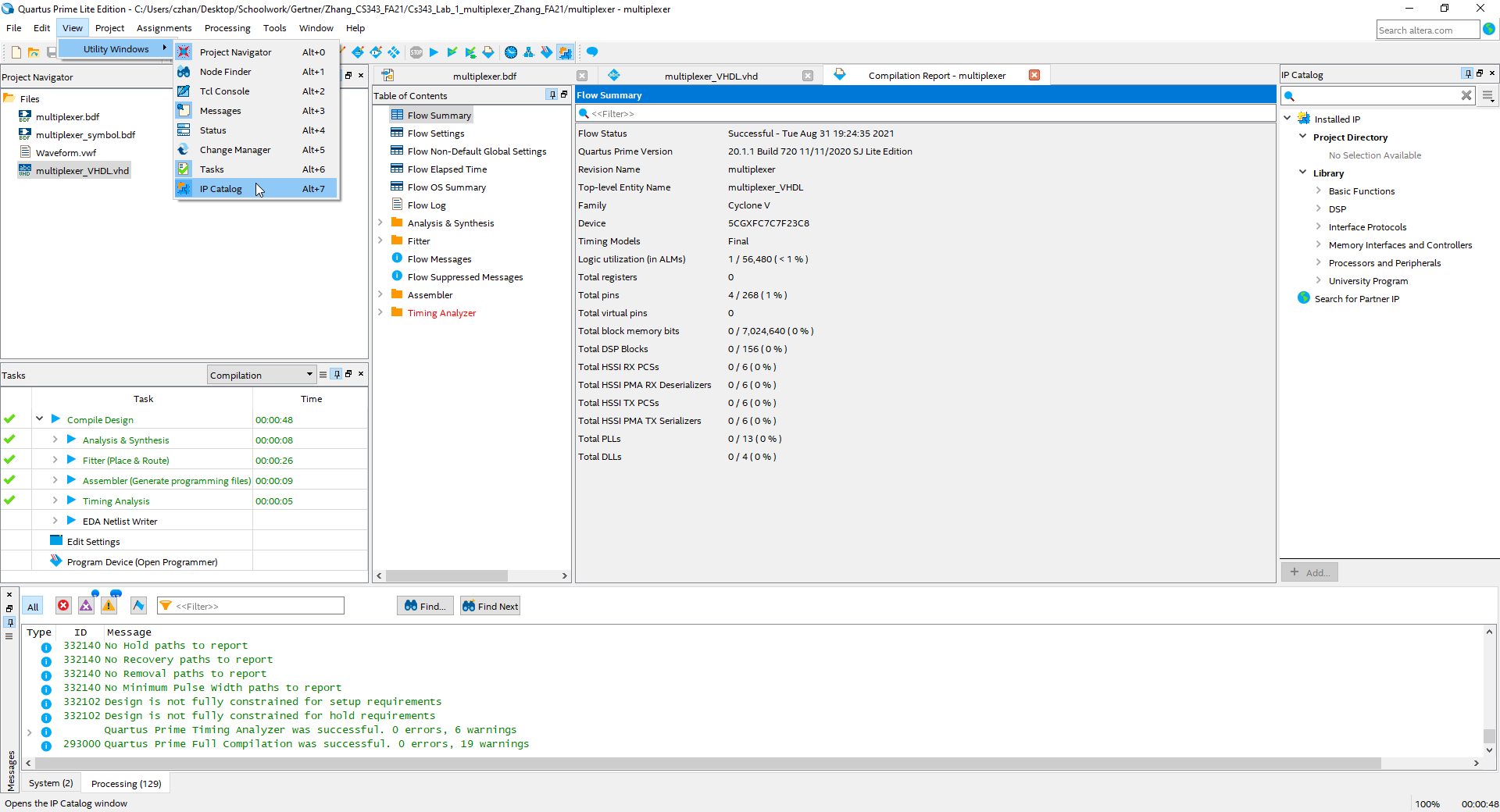
Here is the corrected code that I will then save with a different name according to what I renamed the code to



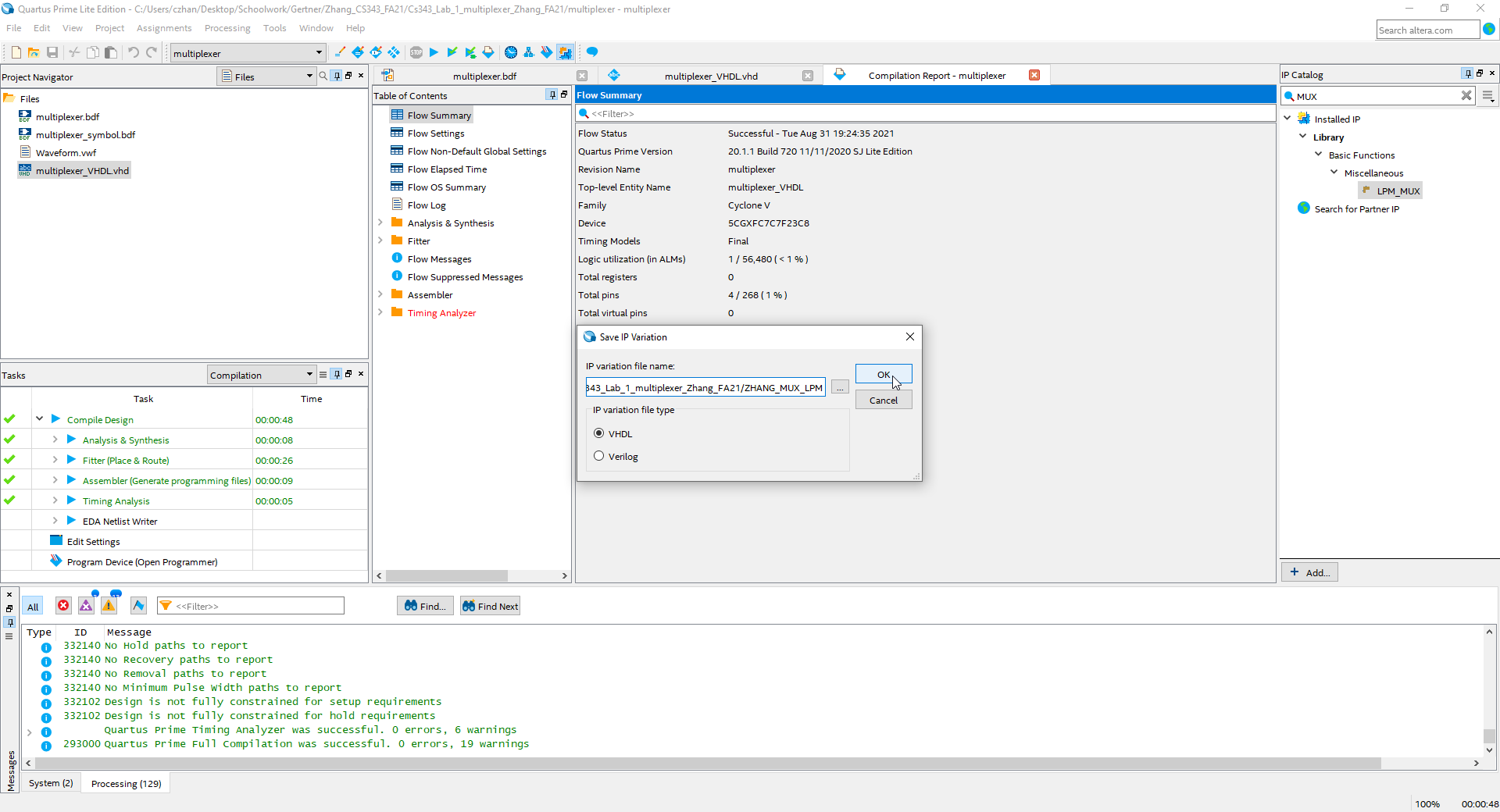
I re-add the vhdl file



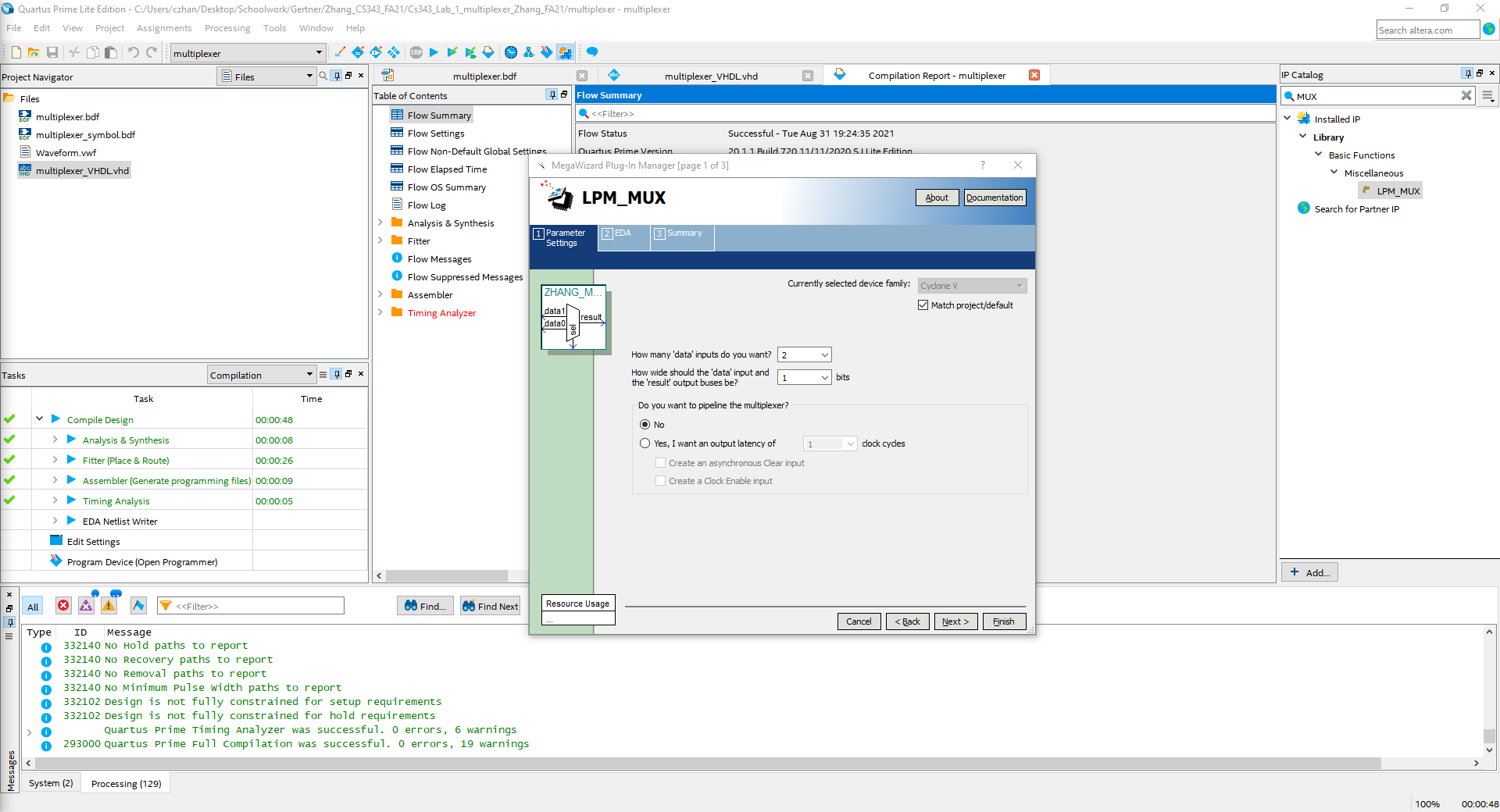
I compile with success



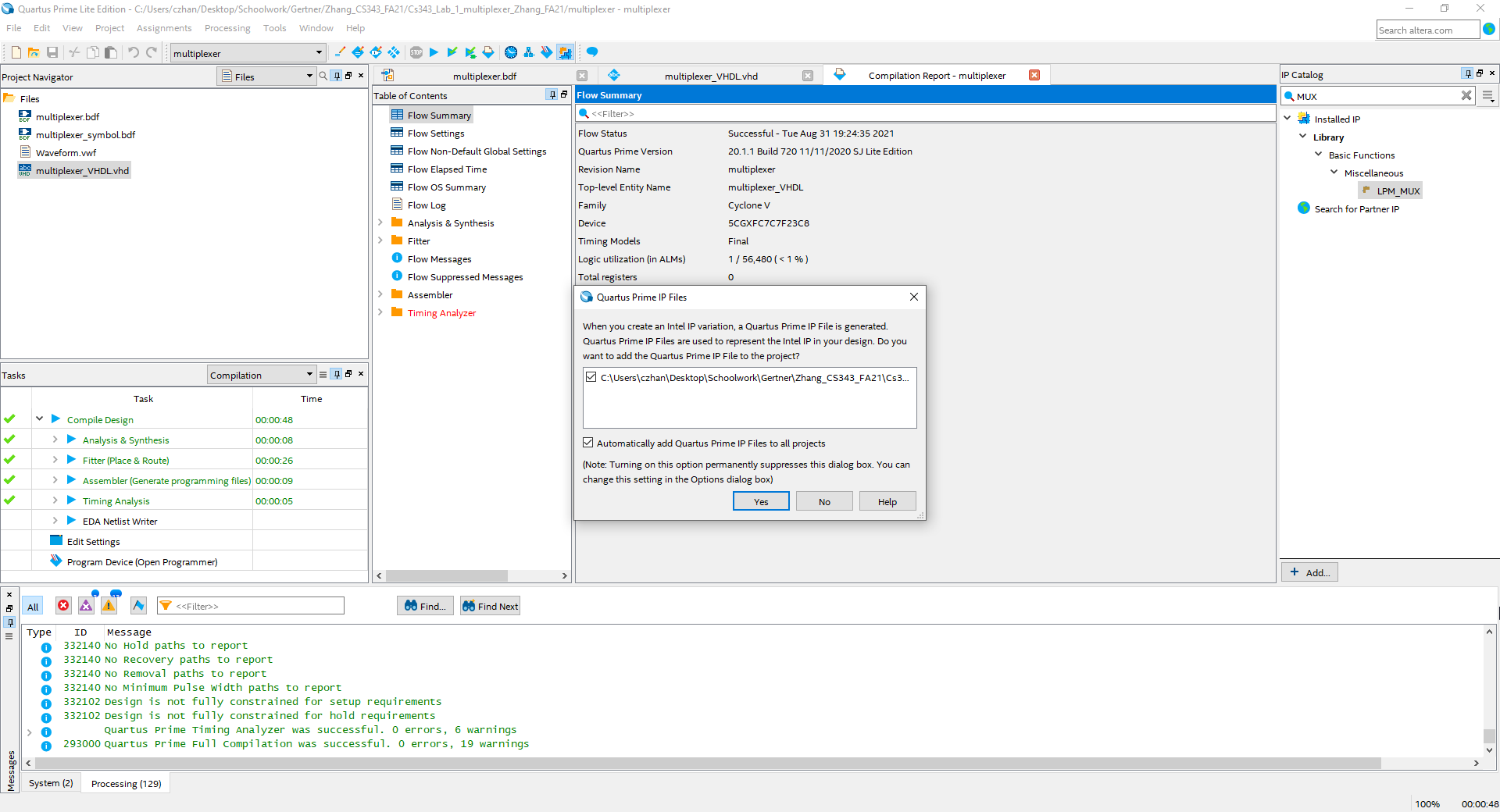
Here I ensure that the IP catalog is checked out and is available for me to use



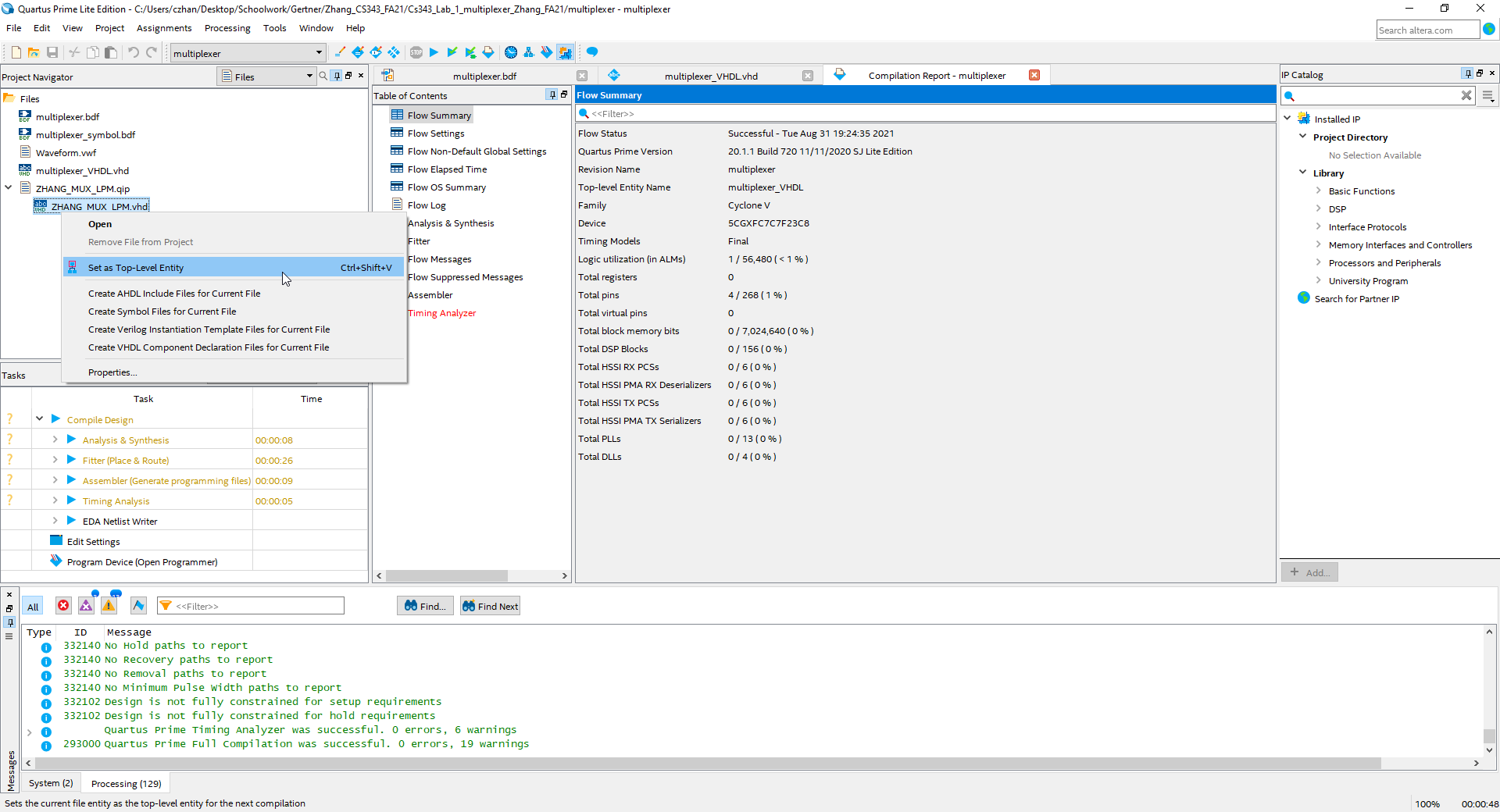
In the right where the IP catalog is, I type in MUX and a drop down showing LPM\_MUX shows up. I double click and press OK



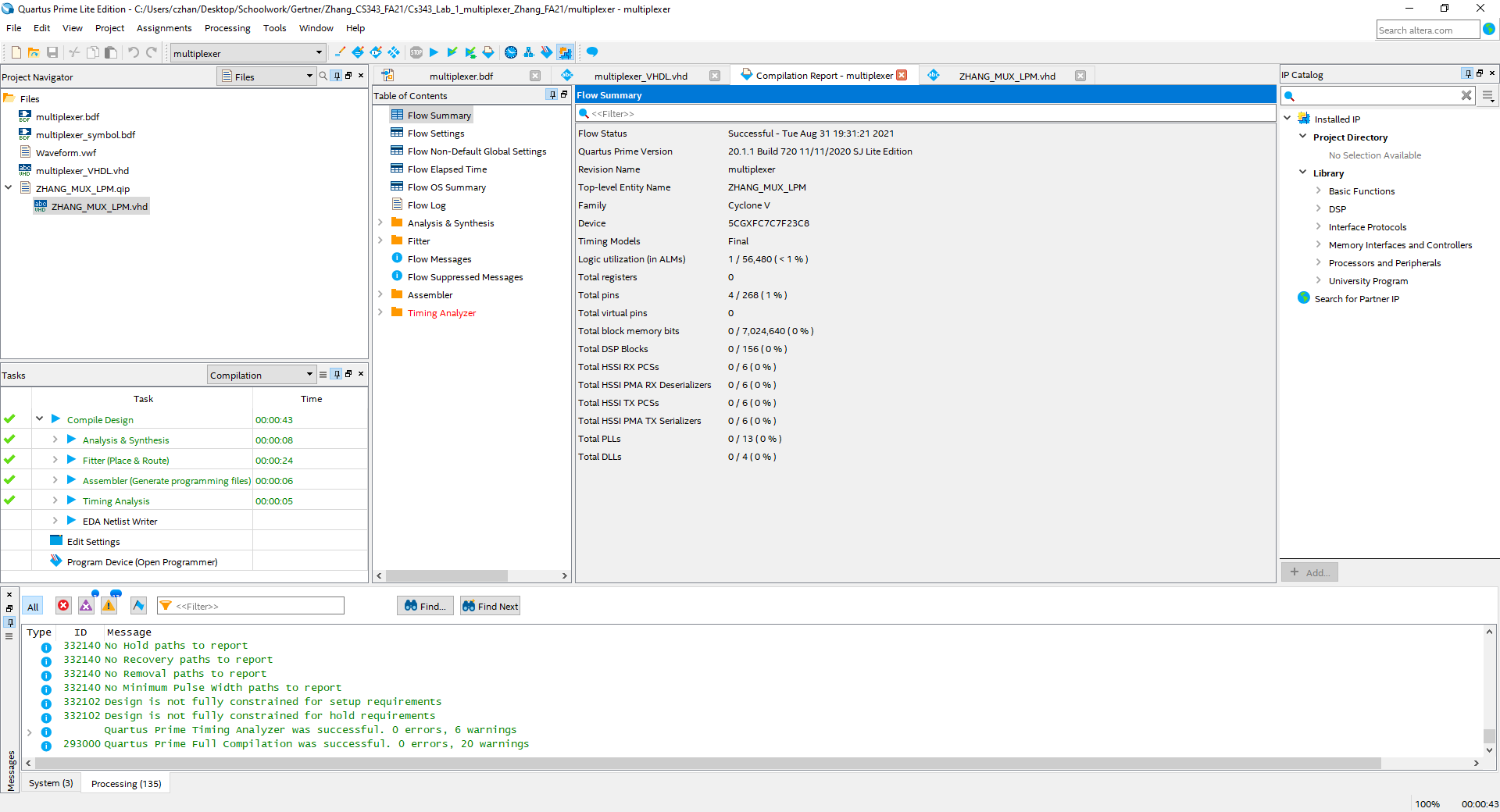
A pop up shows, I press next until I can no longer press next, then I press finish



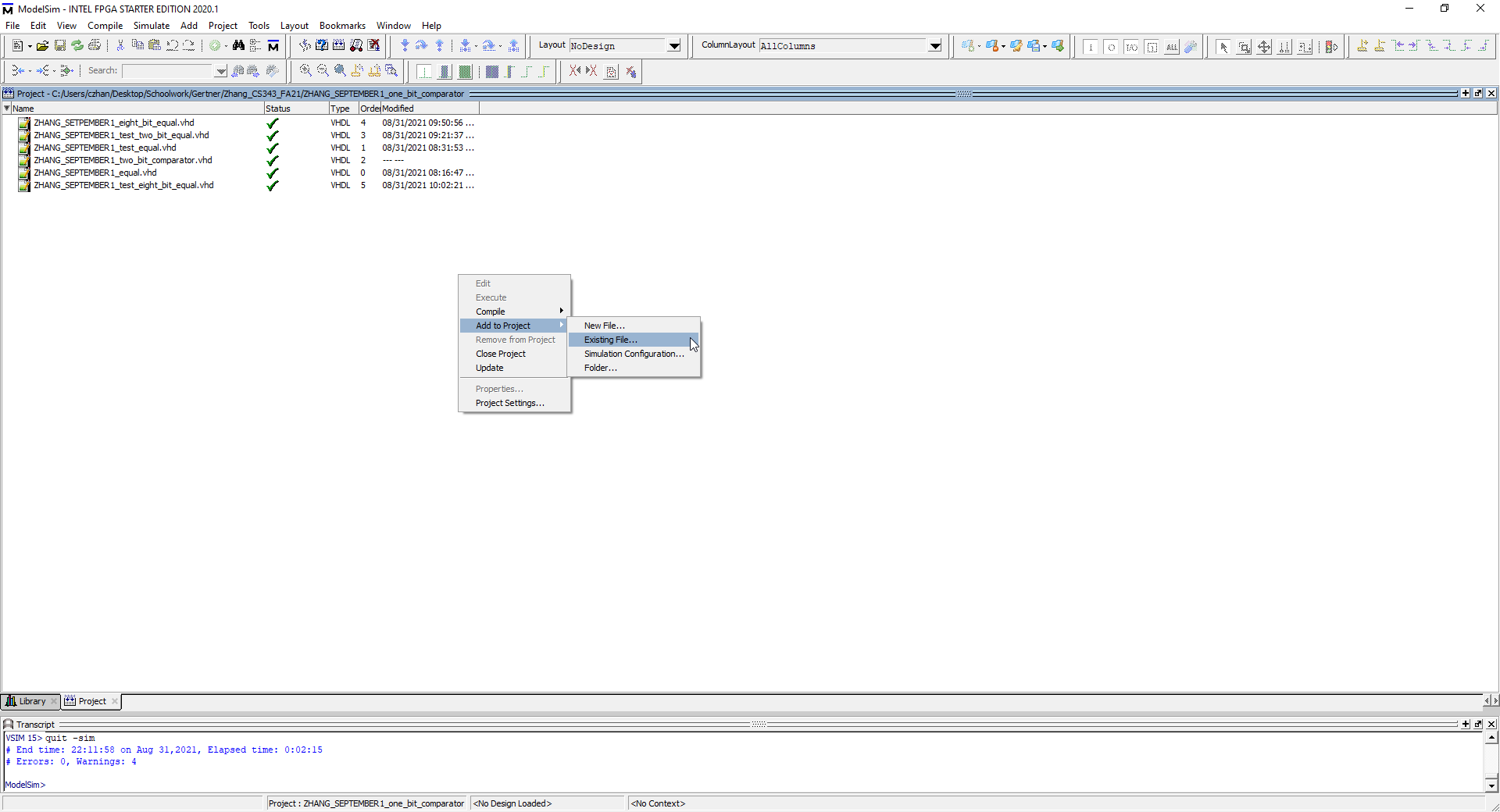
A pop up shows up and I check the box that says “automatically add quartus prime IP files to all projects” and press Yes



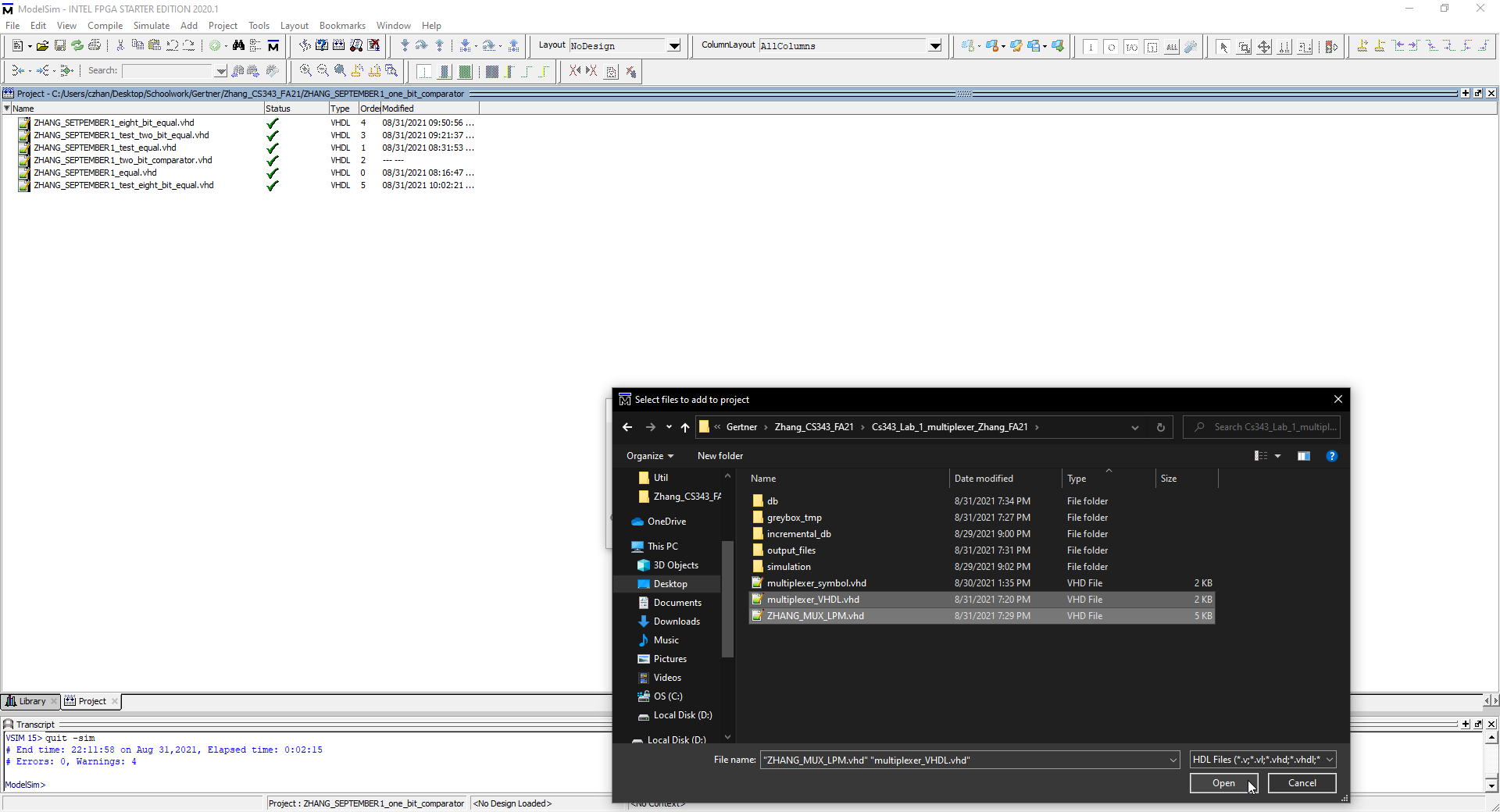
I set the new VHDL file as top level entity



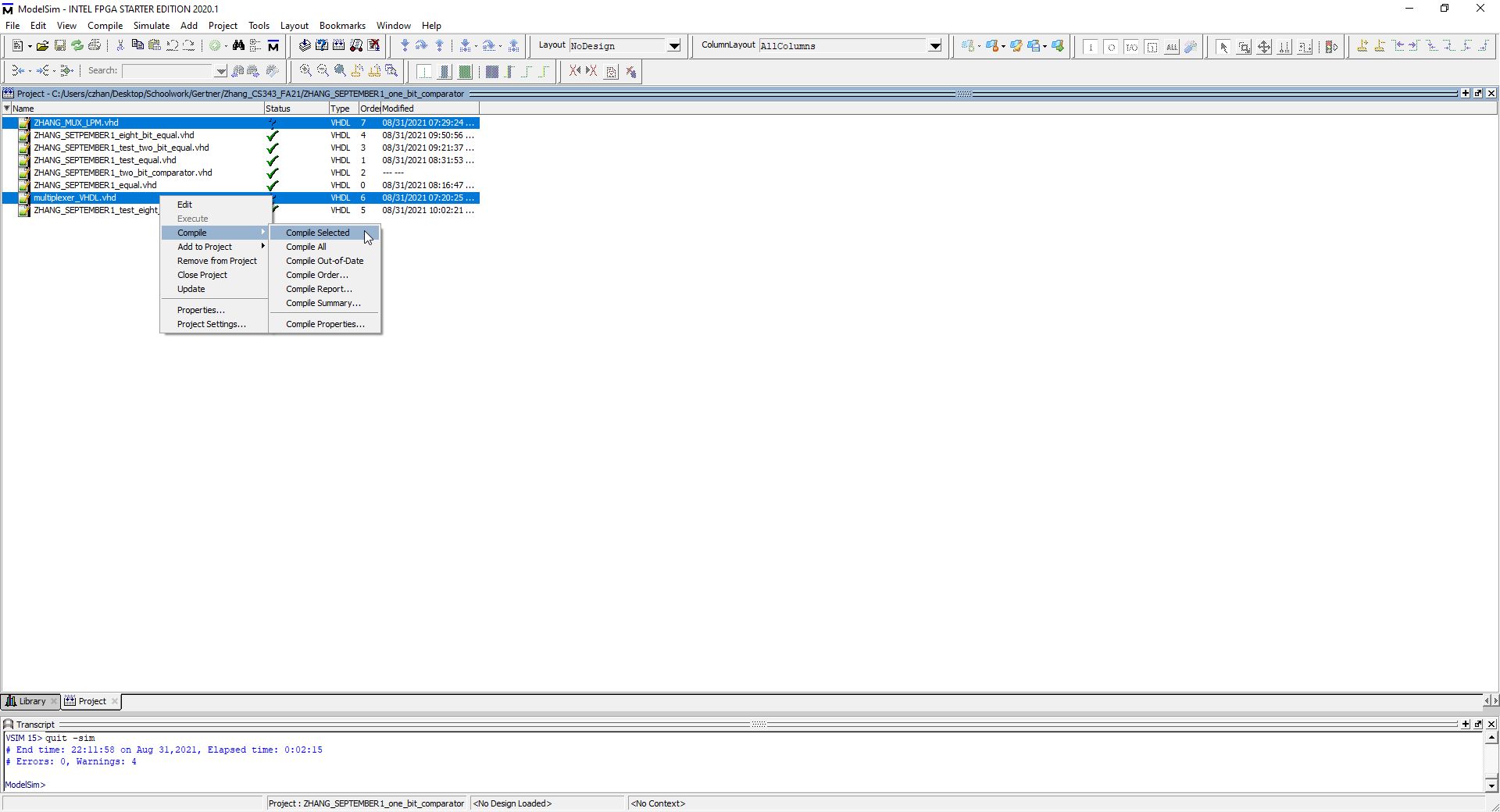
I compile with no erro



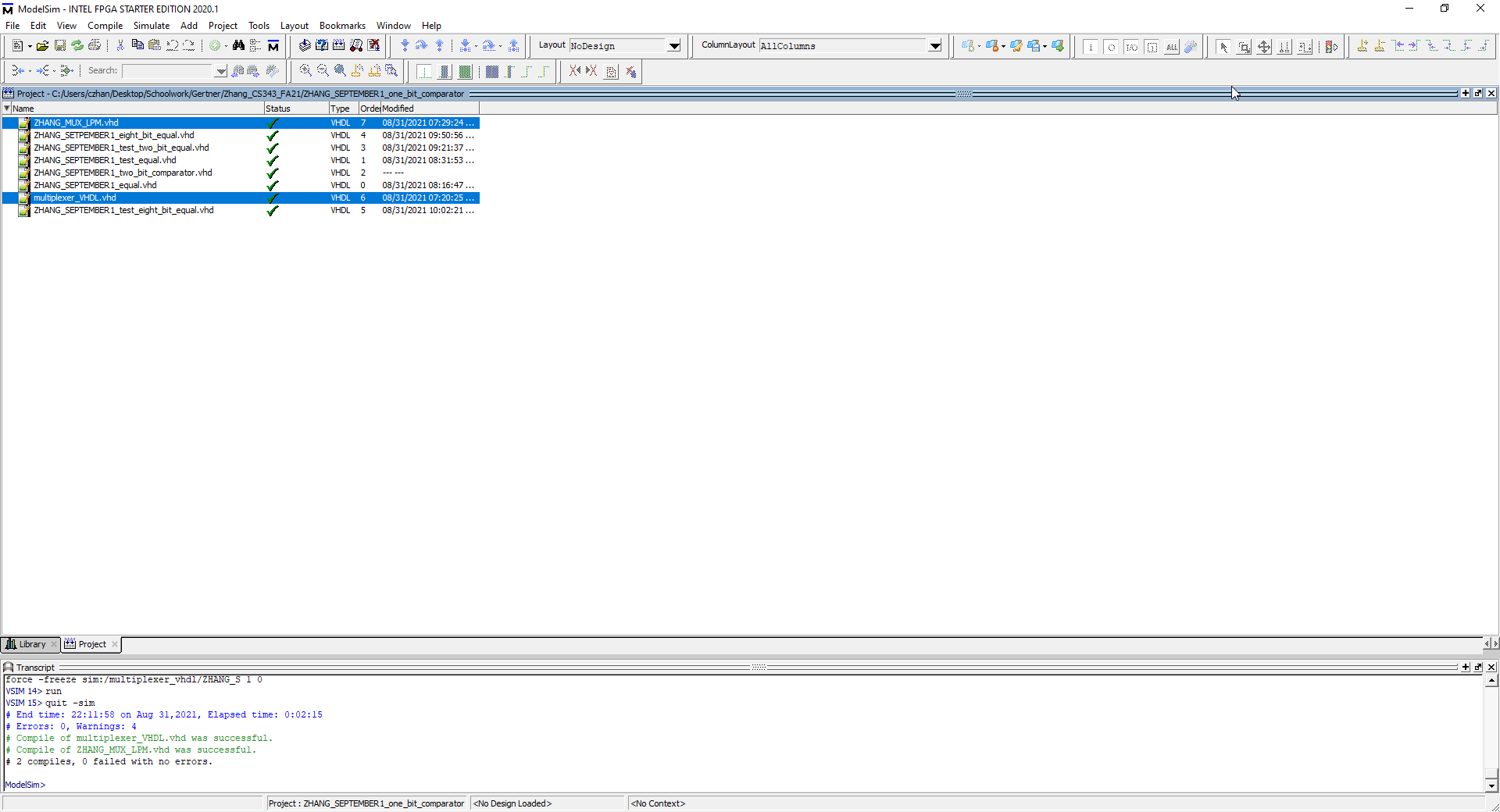
In ModelSim, I right click 🡪 Add to project 🡪 Existing file.. 🡪 and select the vhdl files necessary



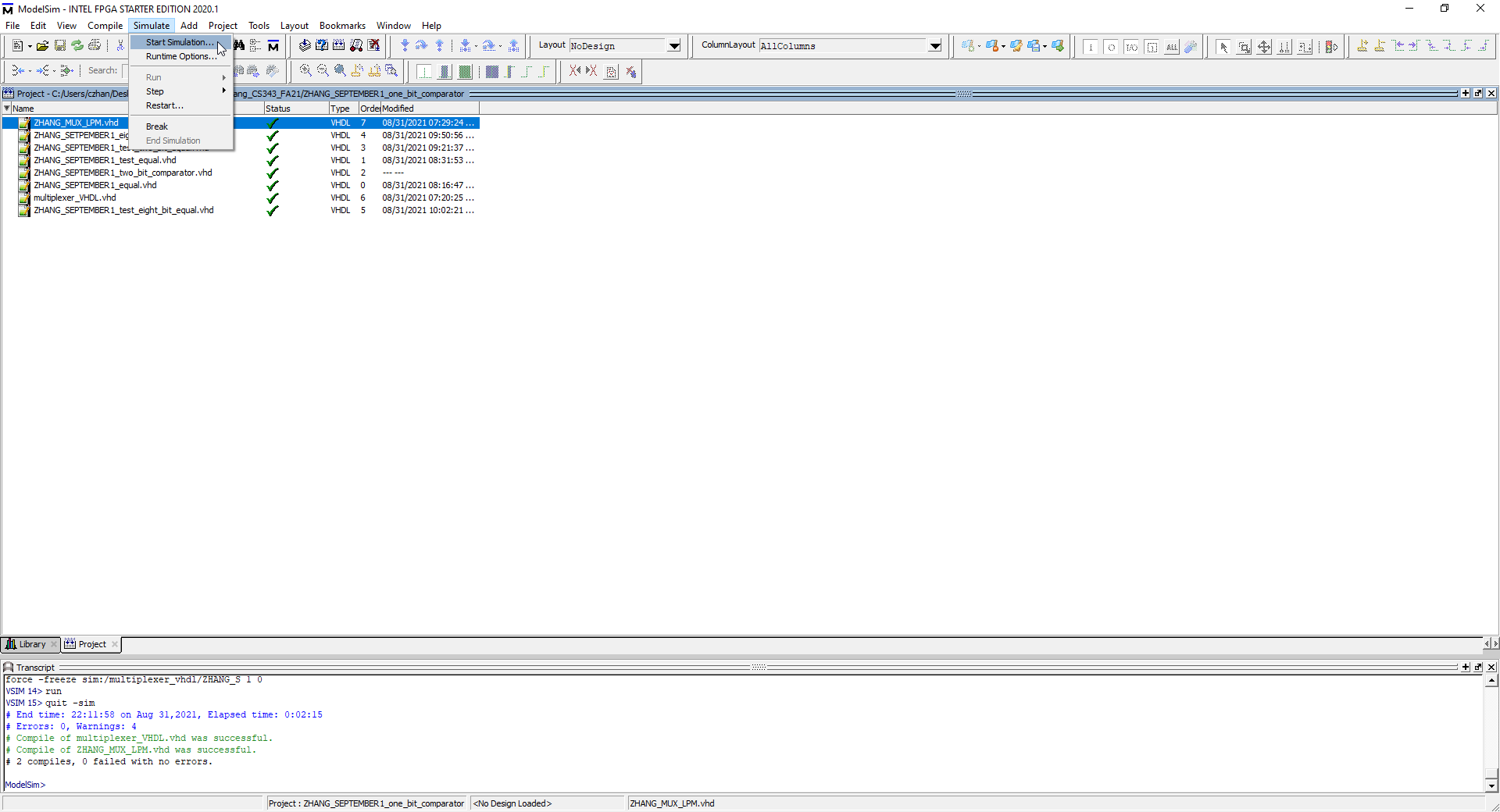
Here I am selecting the LPM MUX vhdl and the VHDL from my mux design



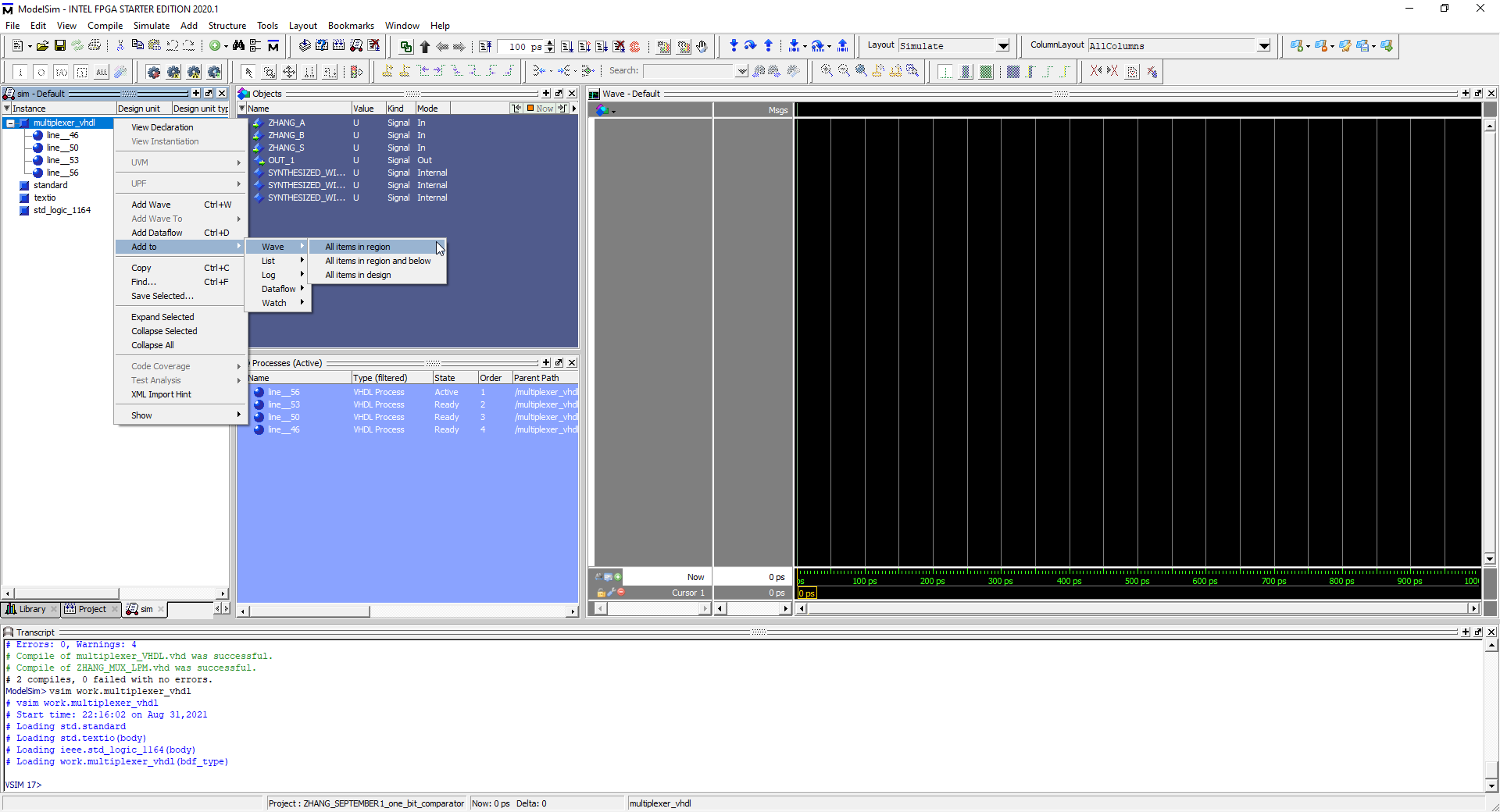
To ensure that they are correct, I compile both files by selecting both files 🡪 right click 🡪 compile 🡪 compile selected



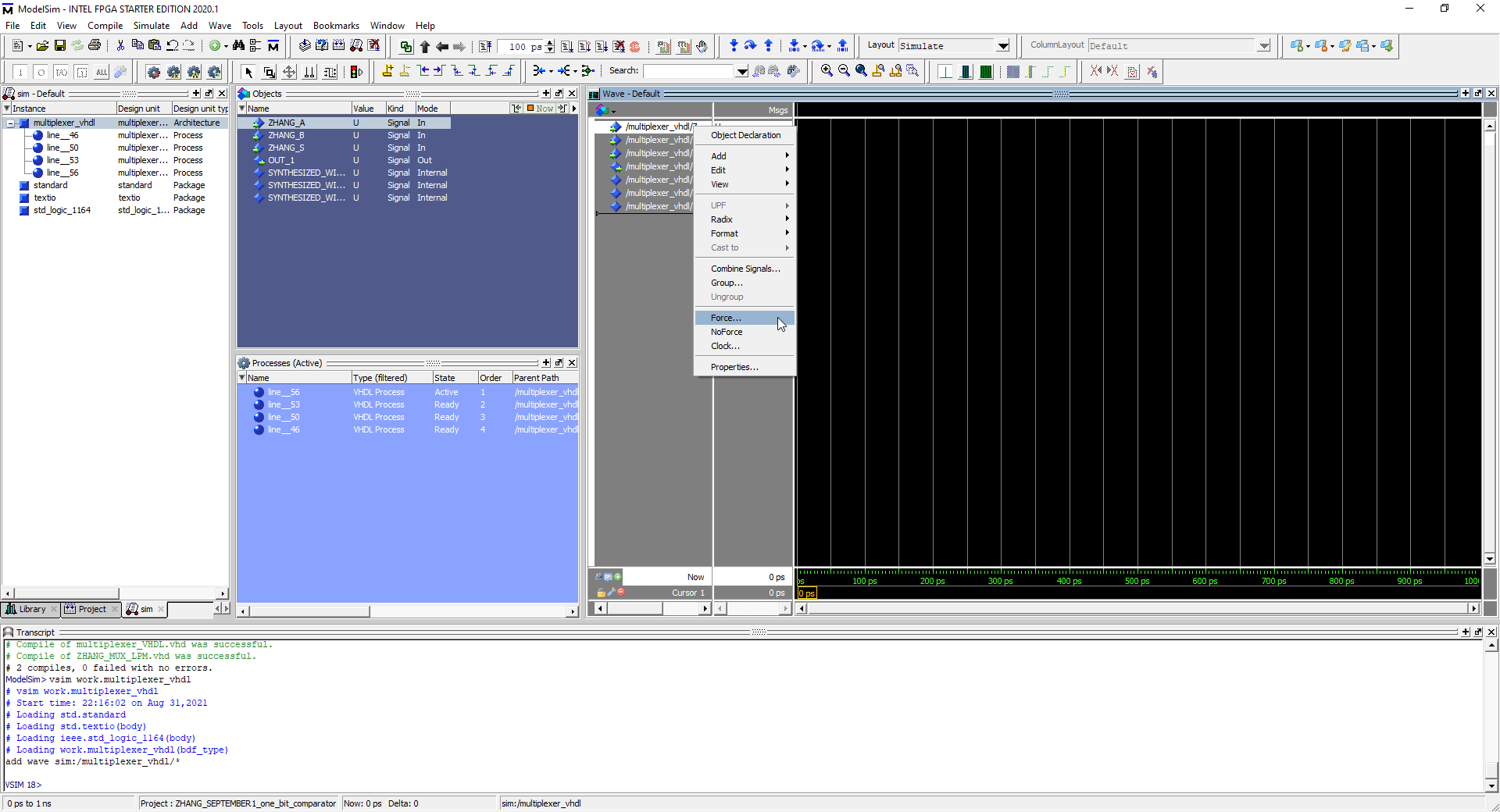
I have successfully compiled with no errors



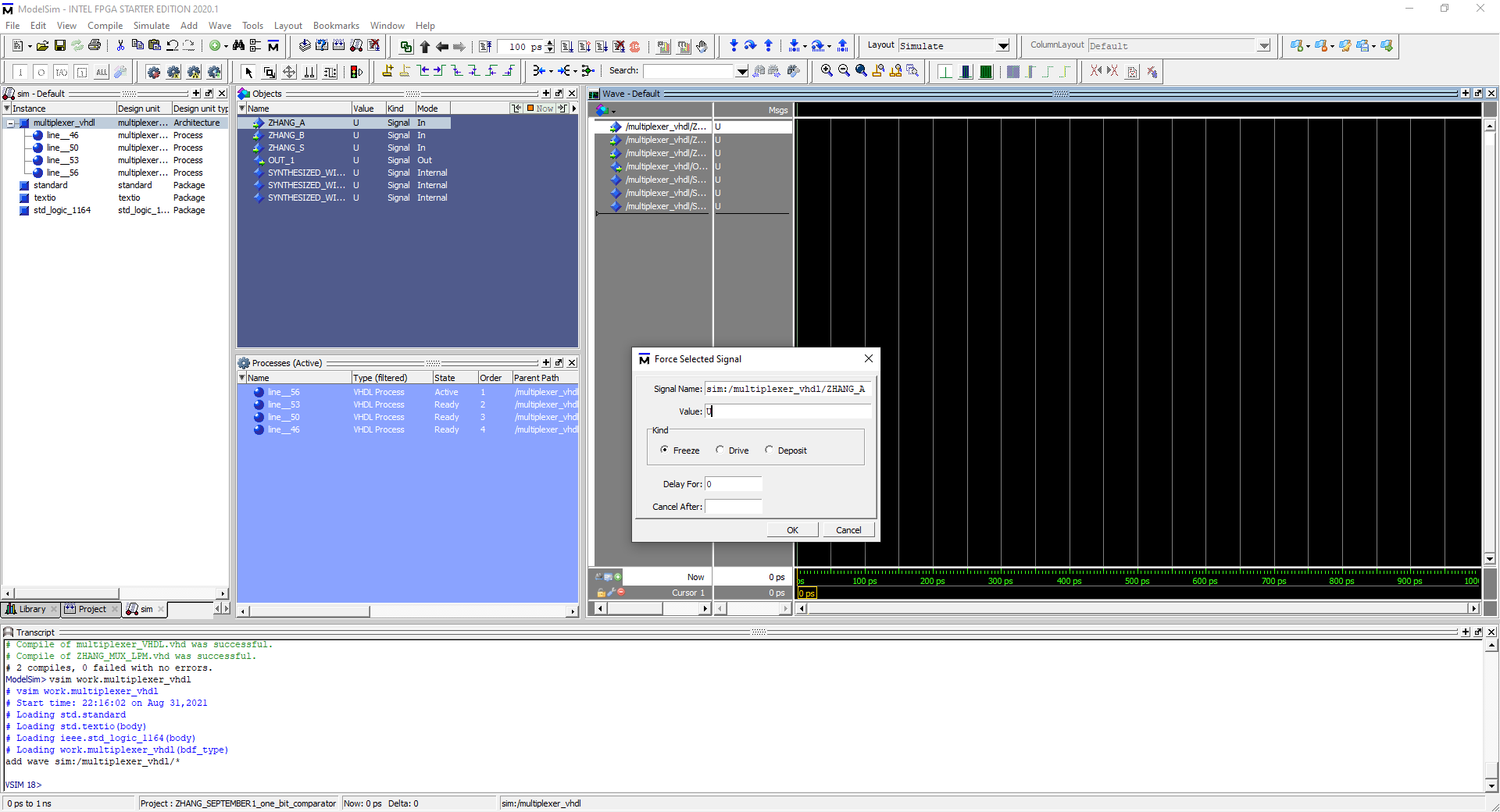
I will now proceed with simulations so on simulations 🡪 I press start simulation



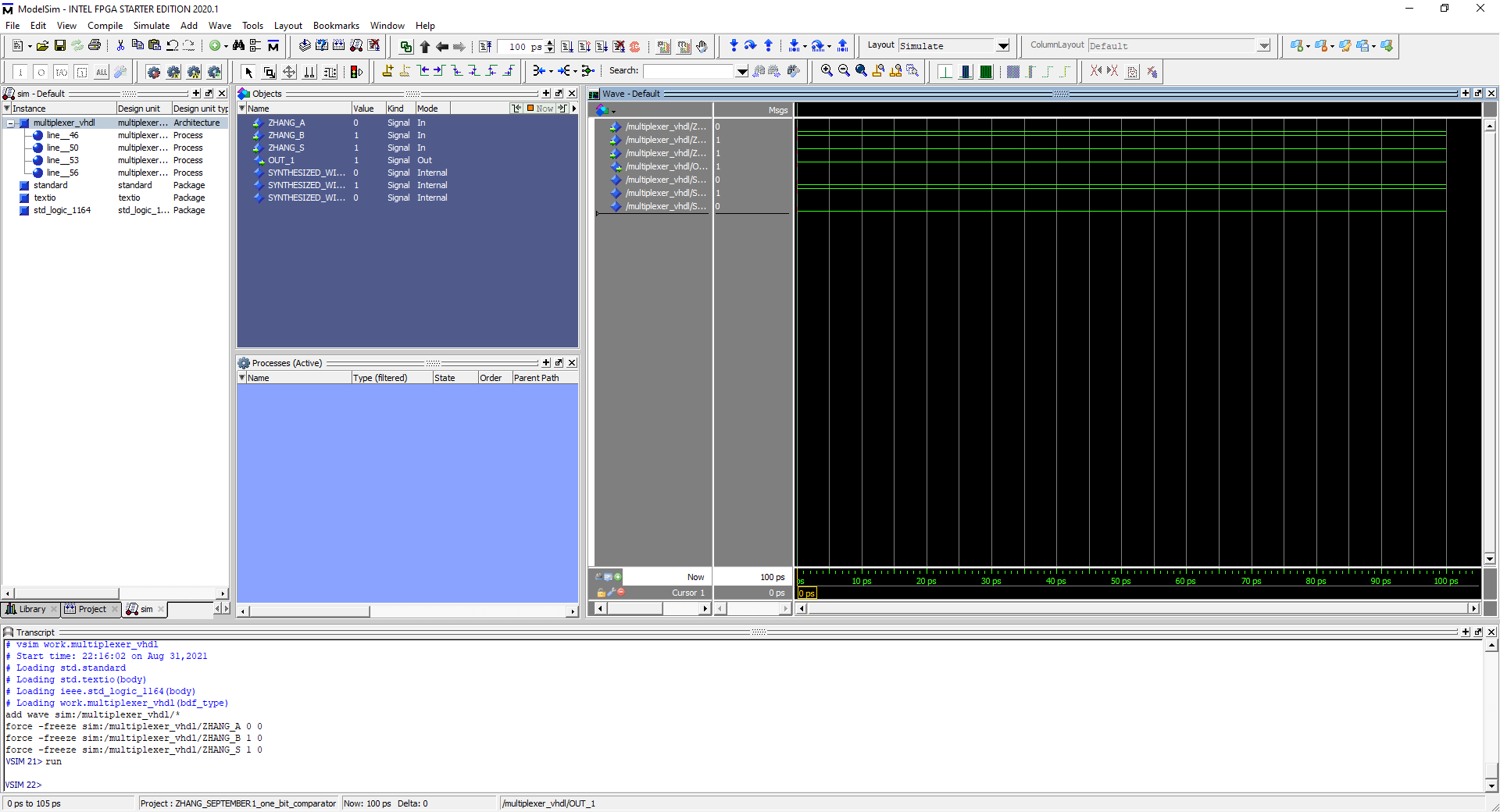
I right click the vhdl with the items in it and right click 🡪 add to 🡪 wave 🡪 add items in region



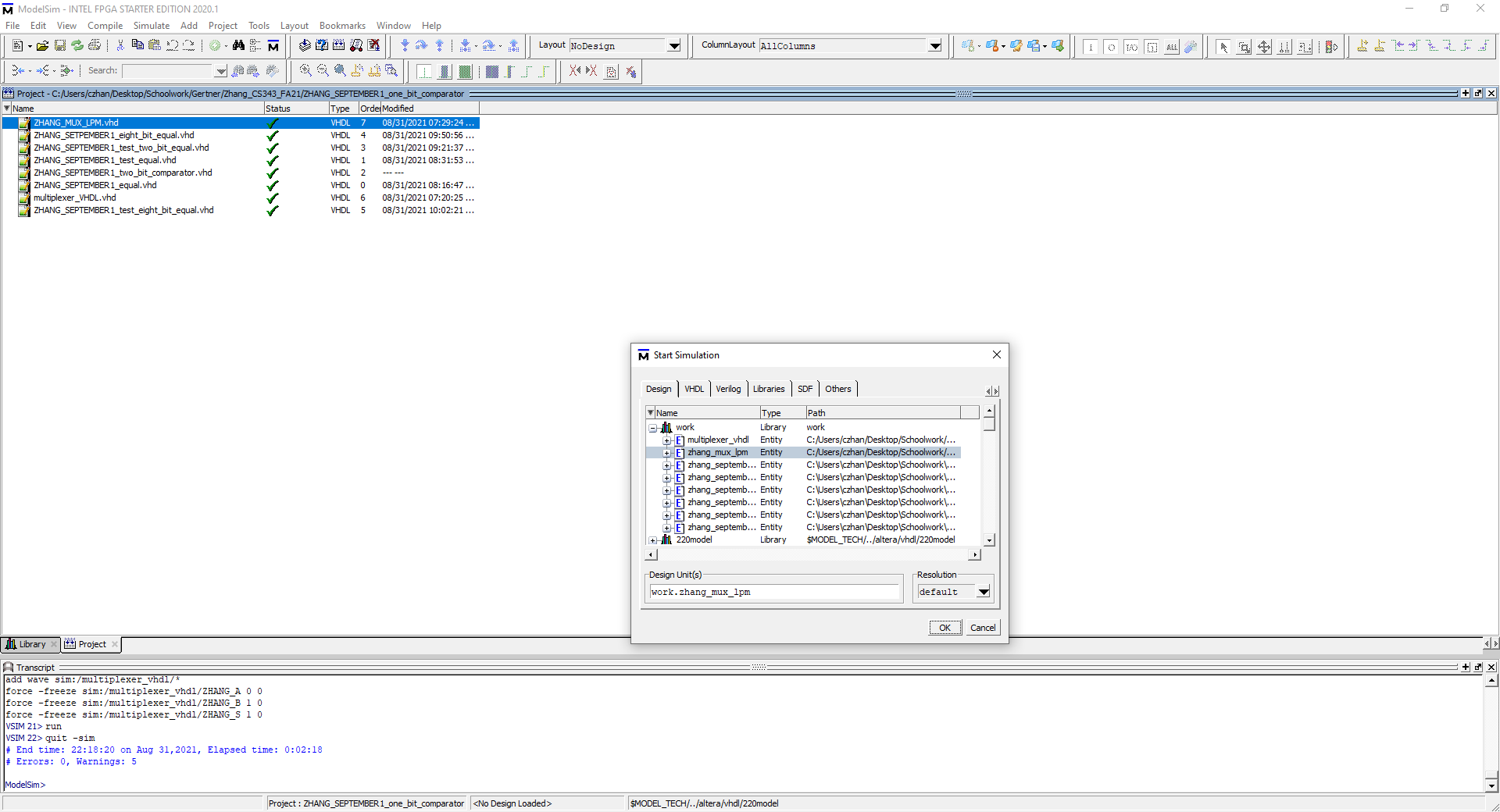
This adds all the files that I want to simulate in and then I right click ZHANG\_A input and press force



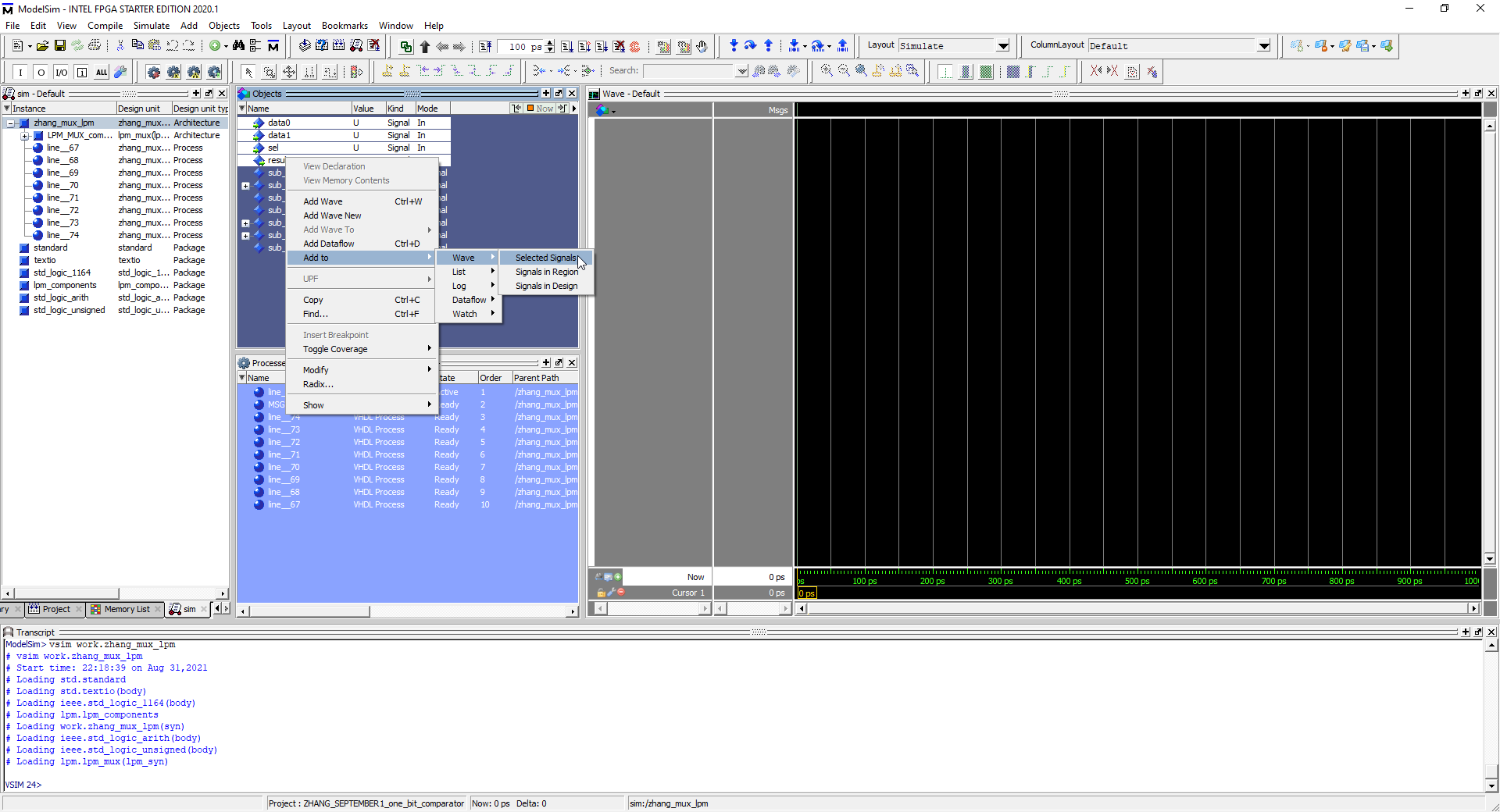
This gives me a popup menu where I can set values. For ZHANG\_A I set values to 0 and for ZHANG\_B and ZHANG\_S I set values to 1



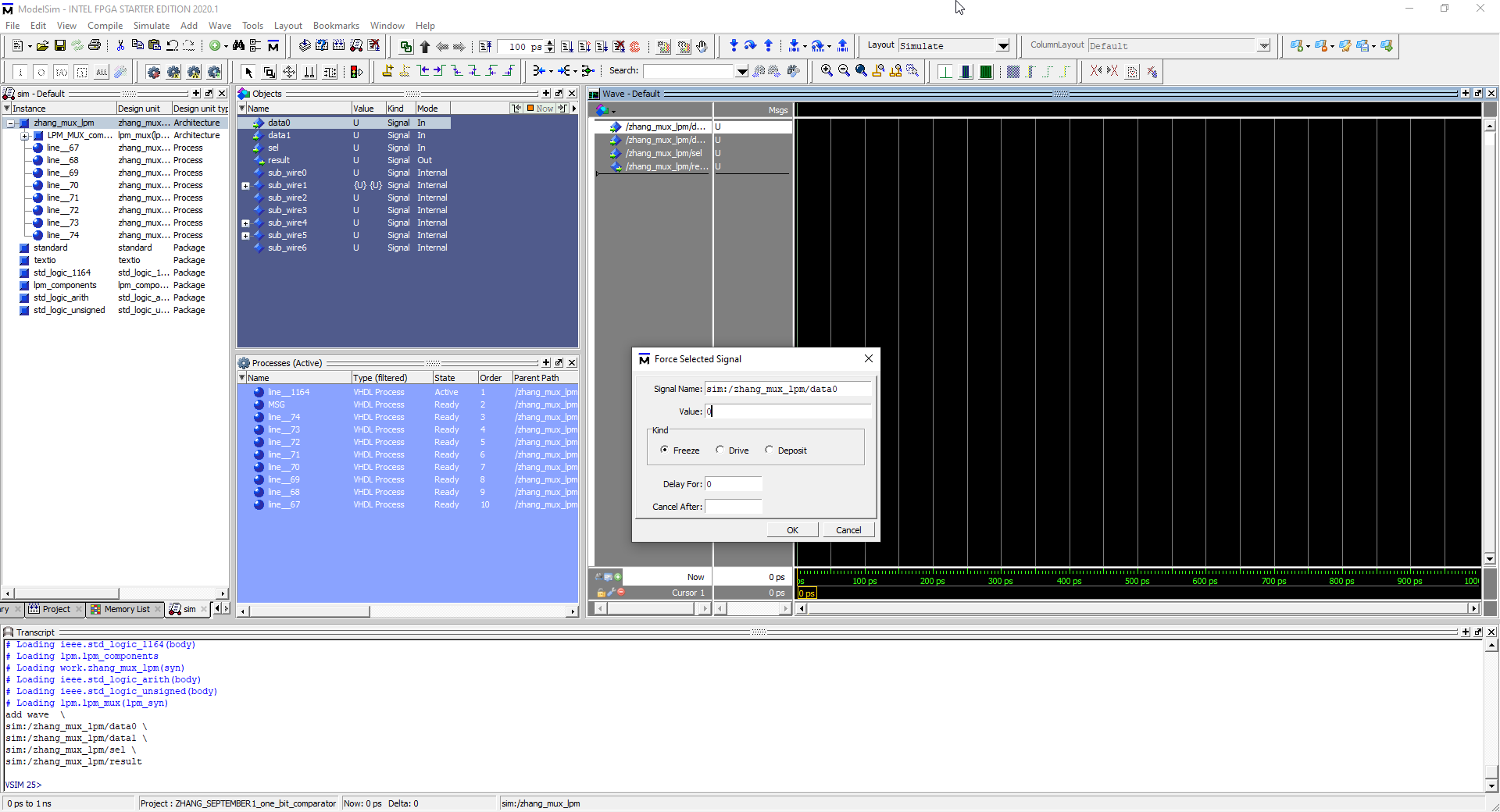
I then run the simulation and this is the output for my design’s, VHDL file. No errors



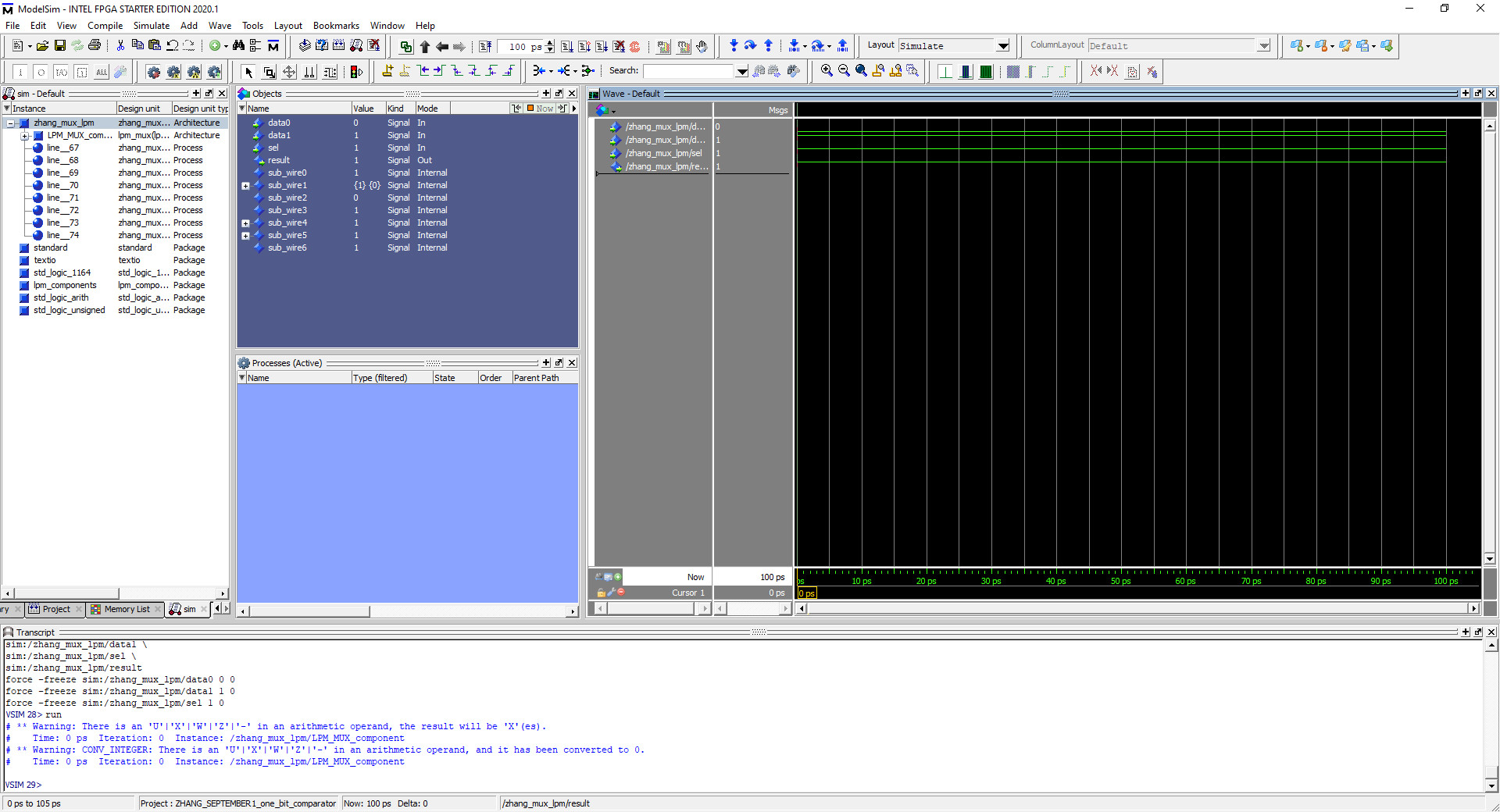
I follow the same steps as what I did for the previous VHDL file but instead, it is for the LPM MUX VHDL file



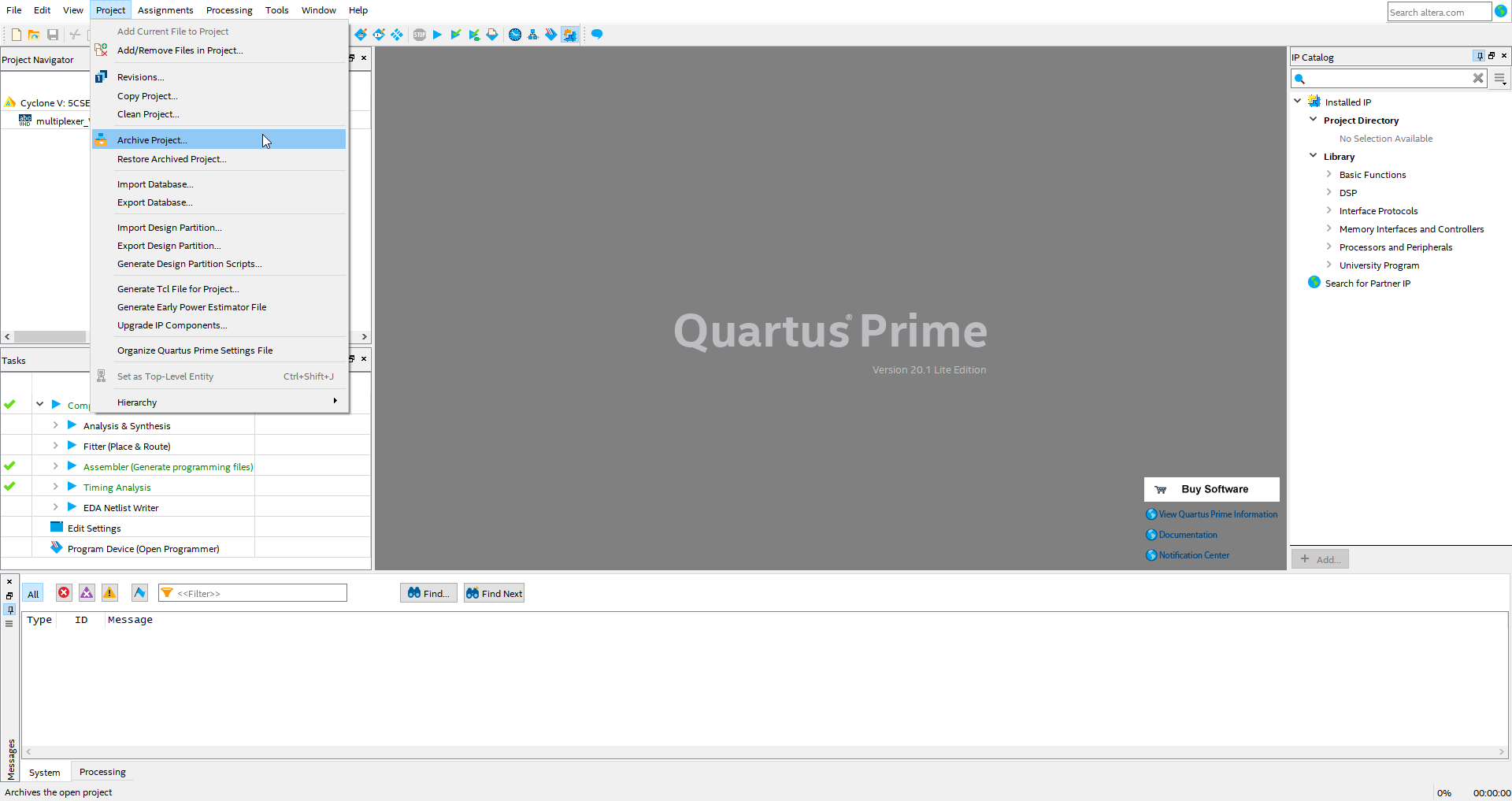
Like before, I add what I want to simulate however, I am only selecting the values necessary to be simulated with



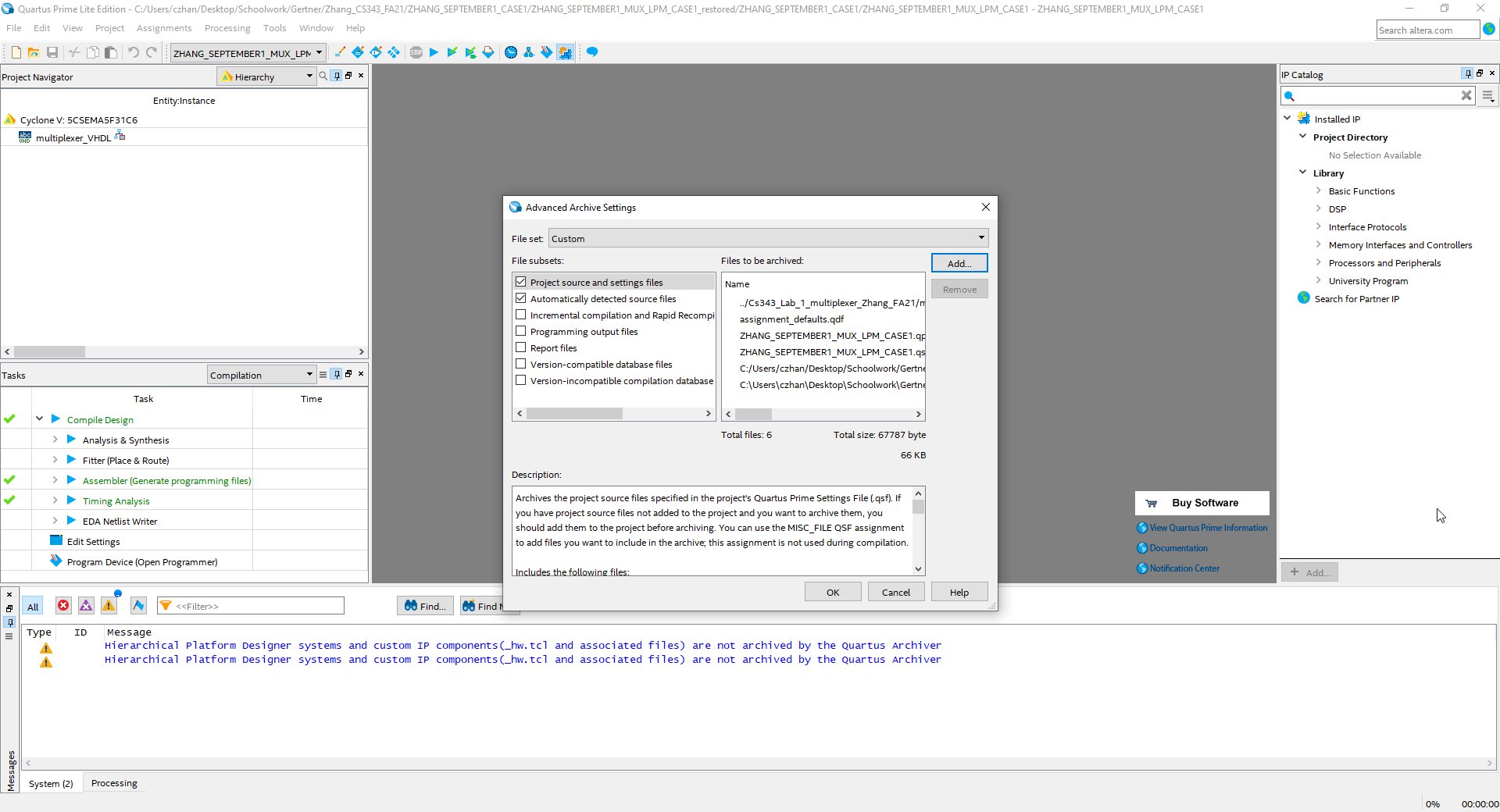
Like before, I right click on the inputs and I press force. Again will I set the values of data0 to “0” and data1 and sel to “1”



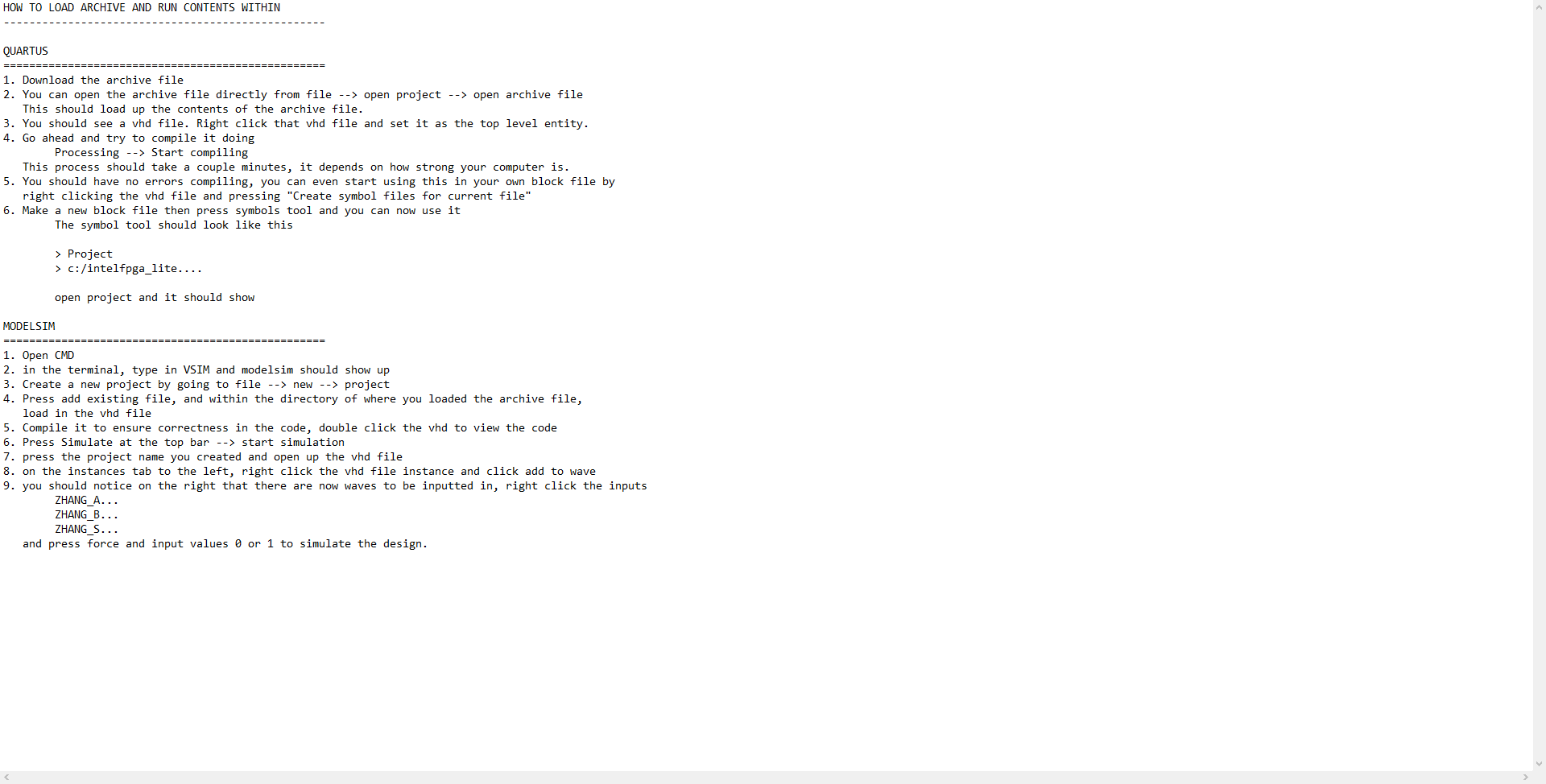
This is the output of the waveform. No errors



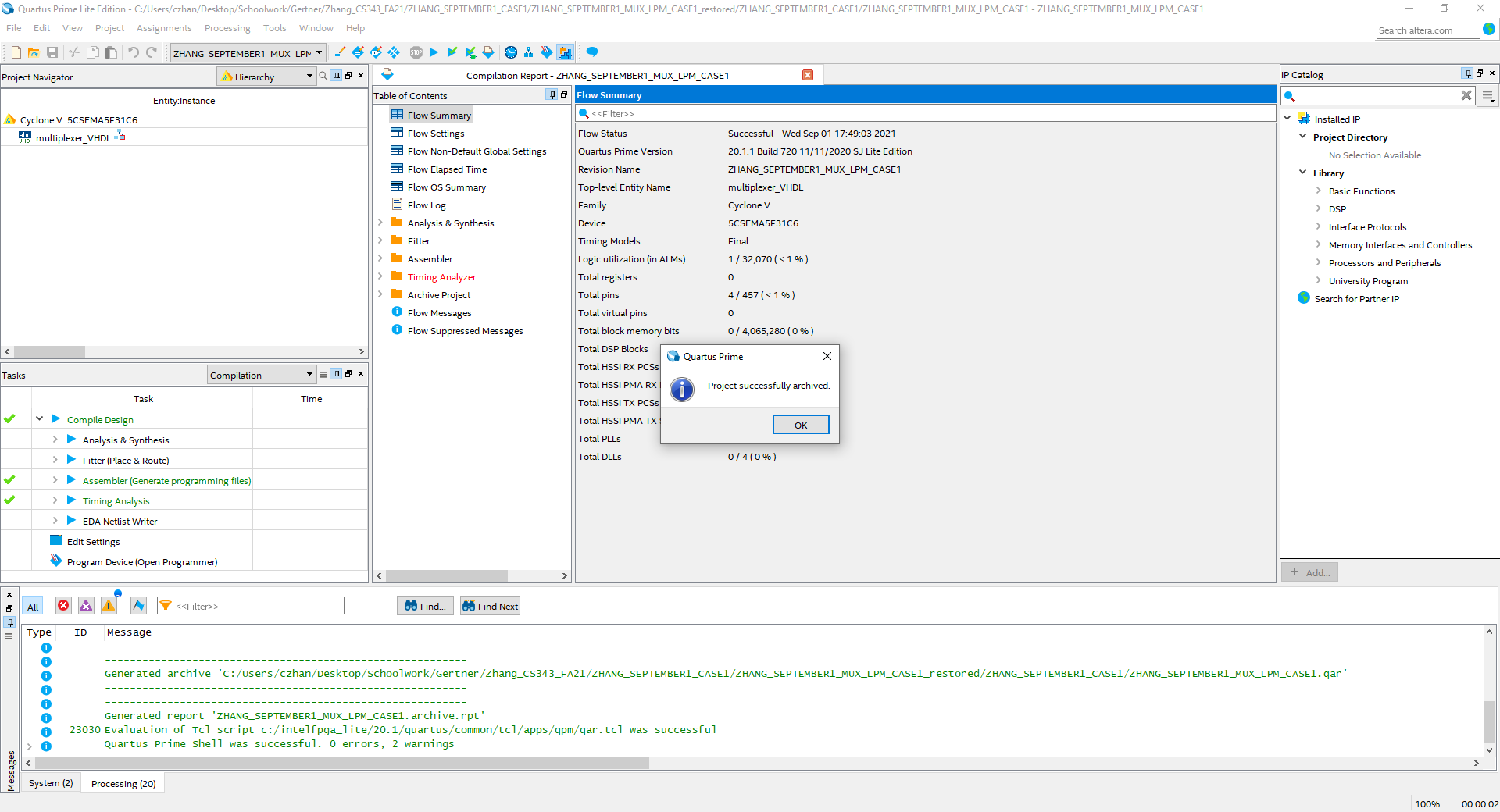
To archive a project, click on project 🡪 archive project



To add a README.TXT to the archive, press advanced 🡪 then the image above should show. Press add then add the respective file you wish to add in.



This is the readme file that I will be including in, complete the archive by pressing ok



Once the archived has been successfully created, a popup like this should show. Also refer to the green text below for success.