**電機工程學系 黃朝宗** **教授**

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紫色： scopus沒有建檔

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1. **Journal Papers and Book Chapters**

**==2015==**

1.C.-T. Huang, "Fast Distribution Fitting for Parameter Estimation of Range-Weighted Neighborhood Filters," *IEEE Signal Processing Letters*, accepted. [[web](http://www.ee.nthu.edu.tw/chaotsung/fast_fitting/index.html)]

2.C.-T. Huang, "Bayesian Inference for Neighborhood Filters with Application in Denoising," *IEEE Transactions on Image Processing*, vol. 24, no. 11, Nov 2015. [[web](http://www.ee.nthu.edu.tw/chaotsung/nnm/index.html)]

3. Chen, H.-H.a , Huang, C.-T.b , Wu, S.-S.a , Hung, C.-L.a , Ma, T.-C.a , Chen, L.-G.a

A 1920×1080 30fps 611 mW five-view depth-estimation processor for light-field applications

(2015)

**==2014==**

4. C.-T. Huang, M. Tikekar, and A. Chandrakasan, "Memory-Hierarchical and Mode-Adaptive HEVC Intra Prediction Architecture for Quad Full HD Video Decoding," *IEEE Transactions on Very Large Scale Integration Systems*, vol. 22, no. 7, pp1515-1525, July 2014.

5. M. Tikekar, C.-T. Huang, C. Juvekar, V. Sze, and A. Chandrakasan, "A 249Mpixel/s HEVC Video-Decoder Chip for 4K Ultra HD Applications," *IEEE Journal of Solid-State Circuits*, vol. 49, no. 1, pp61-79, Jan 2014.

6. M. Tikekar, C.-T. Huang, C. Juvekar, V. Sze, and A. Chandrakasan, "Decoder Hardware Architecture for HEVC," included in *High Efficiency Video Coding (HEVC): Algorithms and Architectures*, editors V. Sze, M. Budagavi, G. J. Sullivan, Springer, 2014.

7. Tikekar, M., Huang, C., Juvekar, C., Sze, V., Chandrakasan, A.P., A 249-mpixel/s hevc video-decoder chip for 4k ultra-hd applications (2014) Solid-State Circuits, IEEE Journal of, 49 (1), pp. 61-72;

**==2007==**

8. C.-C. Cheng, C.-T. Huang, C.-Y. Chen, C.-J. Lian, and L.-G. Chen, "On-Chip Memory Optimization Scheme for VLSI Implementation of Line-Based Two-Dimensional Discrete Wavelet Transform," *IEEE Transactions on Circuits and Systems for Video Technology*, vol. 17, no. 7, pp814-822, July 2007.

**==2006==**

9. C.-Y. Chen, C.-T. Huang, Y.-H. Chen, S.-Y. Chien, and L.-G. Chen, "System Analysis of VLSI Architecture for 5/3 and 1/3 Motion-Compensated Temporal Filtering," *IEEE Transactions on Signal Processing*, vol. 54, no. 10, pp4004-4014, Oct 2006.

10. C.-Y. Chen, C.-T. Huang, Y.-H. Chen, and L.-G. Chen, "Level C+ Data Reuse Scheme for Motion Estimation with Corresponding Coding Order," *IEEE Transactions on Circuits and Systems for Video Technology*, vol. 16, no. 4, pp553-558, April 2006.

11. H.-C. Fang, Y.-W. Chang, T.-C. Wang, C.-T. Huang, and L.-G. Chen, "High Performance JPEG 2000 Encoder with Rate-Distortion Optimization," *IEEE Transactions on Multimedia*, vol. 8 no. 4, pp645-653, Aug 2006.

12. L.-G. Chen, C.-T. Huang, C.-Y. Chen, and C.-C. Cheng, "VLSI Design of Wavelet Transform: Analysis, Architecture, and Design Examples", Imperial College Press, 2006.

**==2005==**

13. Tseng, P.-C.a b , Huang, C.-T.a , Chen, L.-G.a

Reconfigurable discrete wavelet transform processor for heterogeneous reconfigurable multimedia systems

(2005)

14. Huang, C.-T.a b , Tseng, P.-C.a c , Chen, L.-G.a

Generic RAM-based architectures for two-dimensional discrete wavelet transform with line-based method

(2005)

15. Huang, C.-T., Tseng, P.-C., Chen, L.-G.

VLSI architecture for forward discrete wavelet transform based on B-spline factorization

(2005)

16. Huang, C.-T., Tseng, P.-C., Chen, L.-G.

VLSI architecture for fifting-based shape-adaptive discrete wavelet transform with odd-symmetric filters

(2005)

17. Huang, C.-T., Tseng, P.-C., Chen, L.-G.

Analysis and VLSI architecture for 1-D and 2-D discrete wavelet transform

(2005)

**==2003==**

18. Huang, C.-T., Tseng, P.-C., Chen, L.-G.

Hardware implementation of shape-adaptive discrete wavelet transform with the JPEG2000 defaulted (9,7) filter bank

(2003)

**B.** Conference Papers

**==2016==**

1. L.-D. Chen, Y.-L. Hsiao, and C.-T. Huang, "VLSI Architecture Design of Weighted Mode Filter for Full-HD Depth Map Upsampling at 30fps", in IEEE International Symposium on Circuits and Systems, 2016.

2. L.-R. Huang, Y.-W. Wang, and C.-T. Huang, "Fast Realistic Block-Based Refocusing for Sparse Light Fields", in IEEE International Symposium on Circuits and Systems, 2016.

**==2015==**

3. L.-D. Chen, J.-J. Yu, W.-H. Cheng, and C.-T. Huang, "Sub-pixel Disparity Estimation in Continuous Space," in IEEE International Conference on Consumer Electronics - Taiwan, 2015.

4. C.-T. Huang, "Bayesian Inference for Neighborhood Filters with Application in Denoising," in IEEE Conference on Computer Vision and Pattern Recognition (CVPR), 2015. [[web](http://www.ee.nthu.edu.tw/chaotsung/nnm/index.html)]

5. C.-T. Huang, J. Chin, H.-H. Chen, Y.-W. Wang, and L.-G. Chen, "Fast Realistic Refocusing for Sparse Light Fields," in IEEE International Conference on Acoustics, Speech and Signal Processing, 2015. [[web](http://www.ee.nthu.edu.tw/chaotsung/sparse_lf_refocus/index.html)]

6. H.-H. Chen, C.-T. Huang, S.-S. Wu, C.-L. Hung, T.-C. Ma, and L.-G. Chen, "A 1920x1080 30fps 611mW Five-View Depth-Estimation Processor for Light-field Applications," in IEEE International Solid-State Circuits Conference (ISSCC), 2015.

**==2014==**

7. M. Tikekar, C.-T. Huang, V. Sze, and A. Chandrakasan, "Energy and area-efficient hardware implementation of HEVC inverse transform and dequantization," in IEEE International Conference on Image Processing, 2014.

**==2013==**

8. C.-T. Huang, C. Juvekar, M. Tikekar, and A. Chandrakasan, "HEVC Interpolation filter architecture for  Quad Full HD Decoding," in IEEE Visual Communications and Image Processing Conference, Nov 2013.

9. C.-T. Huang, M. Tikekar, C. Juvekar, V. Sze, and A. Chandrakasan, "A 249Mpixel/s HEVC Video-Decoder Chip for Quad Full HD Applications," in IEEE International Solid-State Circuits Conference (ISSCC), pp162-163, Feb 2013.

10. Huang, C.-T.a , Juvekar, C.b , Tikekar, M.b , Chandrakasan, A.P.b

HEVC interpolation filter architecture for quad full HD decoding

(2013) IEEE VCIP 2013 - 2013 IEEE International Conference on Visual Communications and Image Processing, 論文編號 6706371, .

**==2006==**

11. C.-C. Cheng, C.-T. Huang, J.-Y. Chang, and L.-G. Chen, "Line Buffer Wordlength Analysis for Line-Based 2-D DWT," in IEEE International Conference on Acoustics, Speech, and Signal Processing, 2006, vol. 3.

12. Fang, H.-C.b c , Chang, Y.-W.d , Wang, T.-C.b e , Huang, C.-T.b f , Chen, L.-G.a d

High-performance JPEG 2000 encoder with rate-distortion optimization

(2006)

**==2005==**

13. Chen, C.-Y., Huang, C.-T., Chen, Y.-H., Lian, C.-J., Chen, L.-G.

System analysis of VLSI architecture for motion-compensated temporal filtering

(2005)

14. Cheng, C.-C., Tseng, P.-C., Huang, C.-T., Chen, L.-G.

Multi-mode embedded compression codec engine for power-aware video coding system

(2005)

15. Chen, T.-C., Huang, Y.-W., Tsai, C.-Y., Huang, C.-T., Chen, L.-G.

Single reference frame multiple current macroblocks scheme for multi-frame motion estimation in H.264/AVC

(2005)

16. Cheng, C.-C.a , Huang, C.-T.a , Tseng, P.-C.a , Pan, C.-H.b , Chen, L.-G.a

Multiple-lifting Scheme: Memory-efficient VLSI implementation for line-based 2-D DWT

(2005)

17. Huang, C.-T., Chen, C.-Y., Chen, Y.-H., Chen, L.-G.

Memory analysis of VLSI architecture for 5/3 and 1/3 motion-compensated temporal filtering

(2005)

18. Tseng, P.-C., Chang, Y.-C., Huang, Y.-W., Fang, H.-C., Huang, C.-T., Chen, L.-G.

Advances in hardware architectures for image and video coding - A survey

(2005)

**==2004==**

19. Huang, C.-T., Tseng, P.-C., Chen, L.-G.

Memory analysis and architecture for two-dimensional discrete wavelet transform

(2004)

20. Tseng, P.-C., Haung, C.-T., Chen, L.-G.

Reconfigurable discrete cosine transform processor for object-based video signal processing

(2004)

21. Huang, C.-T., Tseng, P.-C., Chen, L.-G.

B-spline factorization-based architecture for inverse discrete wavelet transform

(2004)

22.Fang, H.-C., Huang, C.-T., Chang, Y.-W., Wang, T.-C., Tseng, P.-C., Lian, C.-J., Chen, L.-G.

81MS/s JPEG2000 single-chip encoder with rate-distortion optimization

(2004)

23. Huang, C.-T., Tseng, P.-C., Chen, L.-G.

Flipping Structure: An Efficient VLSI Architecture for Lifting-Based Discrete Wavelet Transform

(2004)

**==2003==**

24. Fang, H.-C., Huang, C.-T., Chang, Y.-W., Wang, T.-C., Tseng, P.-C., Lian, C.-J., Chen, L.-G.

81MS/s JPEG 2000 single-chip encoder with rate-distortion optimization

(2003)

25. Huang, C.-T., Tseng, P.-C., Chen, L.-G.

VLSI architecture for discrete wavelet transform based on B-spline factorization

(2003)

26. Tseng, P.-C., Huang, C.-T., Chen, L.-G.

Reconfigurable discrete wavelet transform architecture for advanced multimedia systems

(2003)

**==2002==**

27. Huang, C.-T., Tseng, P.-C., Chen, L.-G.

Efficient VLSI architectures of lifting-based discrete wavelet transform by systematic design method

(2002)

28. Wu, P.-C., Huang, C.-T., Chen, L.-G.

An efficient architecture for two-dimensional inverse discrete wavelet transform

(2002)

29. Tseng, P.-C., Huang, C.-T., Chen, L.-G.

VLSI implementation of shape-adaptive discrete wavelet transform

(2002)

30.Tseng, P.-C., Huang, C.-T., Chen, L.-G.

Generic RAM-based architecture for two-dimensional discrete wavelet transform with line-based method

(2002)

C. **US Patent**

**==2012==**

1. Y.-H. Lu and C.-T. Huang, "Adaptive canonical Huffman decoder and method thereof and video decoder," US Patent 8,306,108, 2012/11/6.

2. C.-T. Huang and Y.-W. Chang, "Bit rate control circuit and method for image compression," US Patent 8,300,967, 2012/10/30.

3. C.-T. Huang, "Operation method and apparatus for performing overlap filter and core transform," US Patent 8,285,774, 2012/10/9.

4. C.-T. Huang, and C.-P. Lin, "Method and apparatus for generating coded block pattern for highpass coefficients," US Patent 8,233,729, 2012/7/31.

**==2011==**

5. C.-T. Huang, "Method and apparatus for cost calculation in decimal motion estimation," US Patent 7,974,481, 2011/7/5.

6. C.-T. Huang and P.-C. Tseng, "Method and apparatus for motion estimation," US Patent 7,949,194, 2011/5/24.

**==2010==**

7. C.-T. Huang and P.-C. Tseng, "Apparatus and method for motion estimation supporting multiple video compression standards," US Patent 7,782,952, 2010/8/24.

**==2006==**

8. L.-G. Chen, C.-T. Huang, and P.-C. Tseng, "Flipping algorithm to architectures of hardware realization for lifting-based DWT," US Patent 7,076,515, 2006/06/11.