Table of Contents

Chapter 1 1
...1.1 Background 4
.....1.1.1 Algorithmic Complexity 8
.....1.1.2 Graph Theory 12
...1.2 Phases of Physical Design 14
.....1.2.2 Partitioning 22
.....1.2.3 Floorplanning 23
.....1.2.4 Placement 24
.....1.2.5 Global Routing 25
.....1.2.6 Detailed Routing 28
.....1.2.7 Compaction/Spacing 34
.....1.2.8 Design Verification 37
...1.3 Organization of the Thesis 38
Chapter 2 39
...2.1 Introduction 39
...2.2 Previous Work 42
...2.3 New Annealing Schedule 43
...2.4 Conclusions 49
Chapter 3 50
...3.1 Introduction 50
...3.2 Previous Work 50
...3.3 Macro Cell Placement and Routing Algorithm 60
.....3.3.1 Cost function C 62
.....3.3.1.1 Total Wire Length 62
.....3.3.1.2 The Overlap Penalty 63
.....3.3.1.3 The Timing Penalty 68
.....3.3.2 The Improved New State Selection Procedure 70
.....3.3.3 Stage 2 Placement Refinement 71
.....3.3.3.2 Global Routing 74
.....3.3.3.3 Compaction 75
.....3.3.3.4 Topology Preservation During Compaction 77
.....3.3.3.5 Adaptive Dynamic Wire Length Estimation 80
.....3.3.3.6 Detailed Routing 83
...3.4 Results 88
...3.5 Conclusions 90
Chapter 4 91
...4.1 Introduction 91
...4.2 Previous Work 92
...4.3 TimberWolf Mixed Macro / Standard Cell Flow Algorithm 93
.....4.3.1 Error Checking: Syntax 93
.....4.3.2 Standard Cell/Macro Cell Clustering 94
.....4.3.3 Floorplanning: TimberWolfMC 96
.....4.3.4 Standard Cell Row Generation: Genrows 98

.....4.3.5 Standard Cell Placement: TimberWolfSC 100
.....4.3.6 Row - Based Global Routing 101
.....4.3.7 Standard Cell Detailed Routing: Sc_route 101
.....4.3.8 Macro Cell Placement Refinement: TimberWolfMC 103
.....4.3.9 Macro Cell Detailed Routing: Mc_route 103
.....4.3.10 Results 104
...4.4 Conclusions 105
Chapter 5 107
...5.1 Introduction 107
...5.2 Previous Work 107
...5.3 Net Constraints 112
...5.4 Crosstalk Constraints 113
...5.5 Results 116
...5.6 Conclusions 117
Chapter 6 118
...6.1 Introduction 118
...6.2 Previous Work 124
...6.3 Algorithm 126
.....6.3.1 Critical Path Using Wire Length Constraints 126
.....6.3.2 Matched Critical Path Using Wire Length Constraints 127
.....6.3.3 Critical Path Using Timing Constraints 128
.....6.3.4 Matched Critical Path Using Timing Constraints 129
.....6.3.5 Critical Path Analysis Using Pin Pair Constraints 130
.....6.3.6 Matched Critical Path Analysis Using Pin Pair Constraints 139
...6.4 Results 140
...6.5 Conclusions 146
Chapter 7 147
...7.1 Introduction 147
.....7.1.1 Previous Work 147
.....7.1.2 Previous Work in Steiner Tree Generation 151
...7.2 Problems with Steiner Tree Algorithms 152
...7.3 New Global Router 153
.....7.3.2 Area Minimization 155
.....7.3.3 Feedthrough Assignment - Multiple Row Assignment 160
.....7.3.4 Feedthrough Assignment - Single Row Assignment 162
.....7.3.5 Cell Overlap Removal 164
.....7.3.6 Cell Swap Optimization 165
.....7.3.7 Switchable Segment Optimization 165
.....7.3.8 Maze Routing 165
.....7.3.9 Vertical Constraint Minimization 169
.....7.3.10 Route Verification 170
...7.4 Algorithmic Complexity 171
...7.5 Sea-of-Gates Extensions 172
...7.6 Row-based FPGA Extensions 173
...7.7 Results 174
...7.8 Conclusions 176
Chapter 8 177

...8.1 Introduction 177
...8.2 Previous Work 178
.....8.2.1 Design Management Systems 178
.....8.2.2 Software Engineering 178
...8.3 System control: twflow 183
.....8.3.3 Parallel execution 187
...8.4 Software Engineering 189
...8.5 Conclusions 199
Chapter 9 200
...9.1 Future Work 200
.....9.1.1 Simulated Annealing 200
.....9.1.2 Macro Cell Placement and Routing 200
.....9.1.3 Mixed Macro and Standard Cell Circuits 201
.....9.1.4 Detailed Routing 201
.....9.1.5 Analog 201
.....9.1.6 Timing 201
.....9.1.7 Global Routing 202
.....9.1.8 System Issues 202
...9.2 Summary 203