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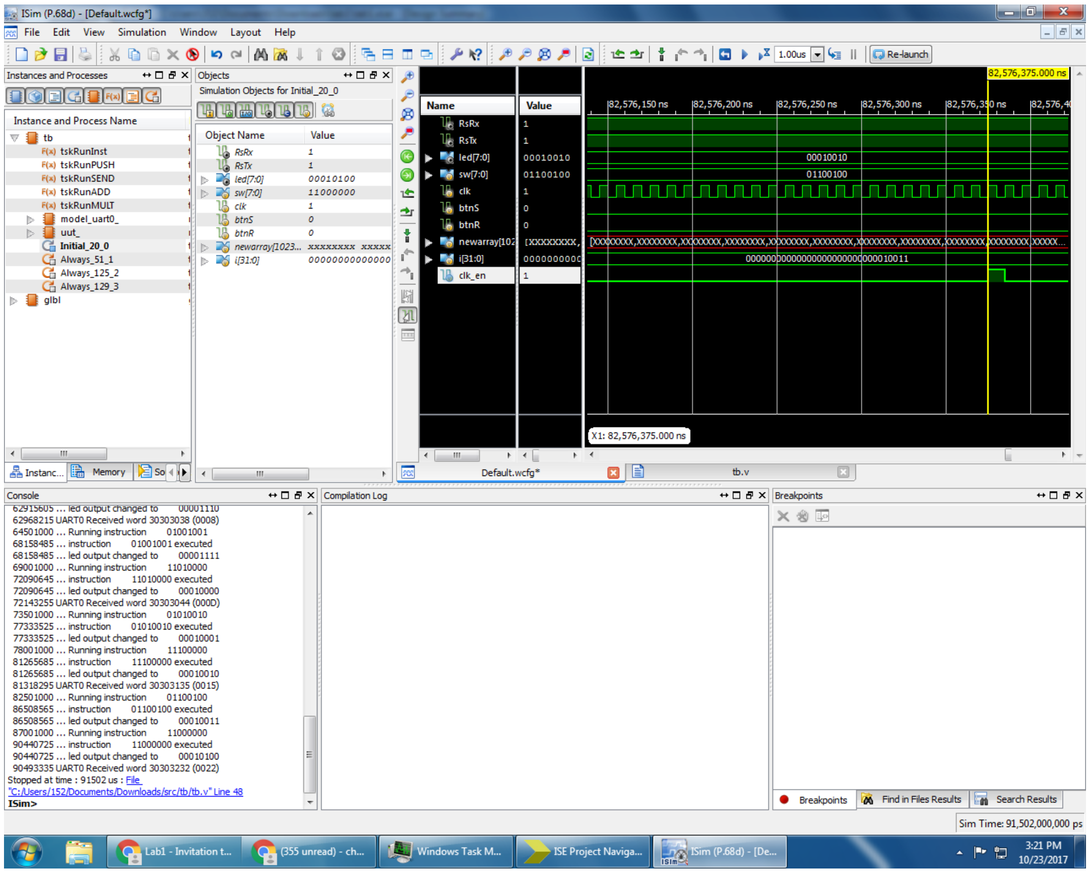
CSM152A

Lab 1 Report

Workshop 1

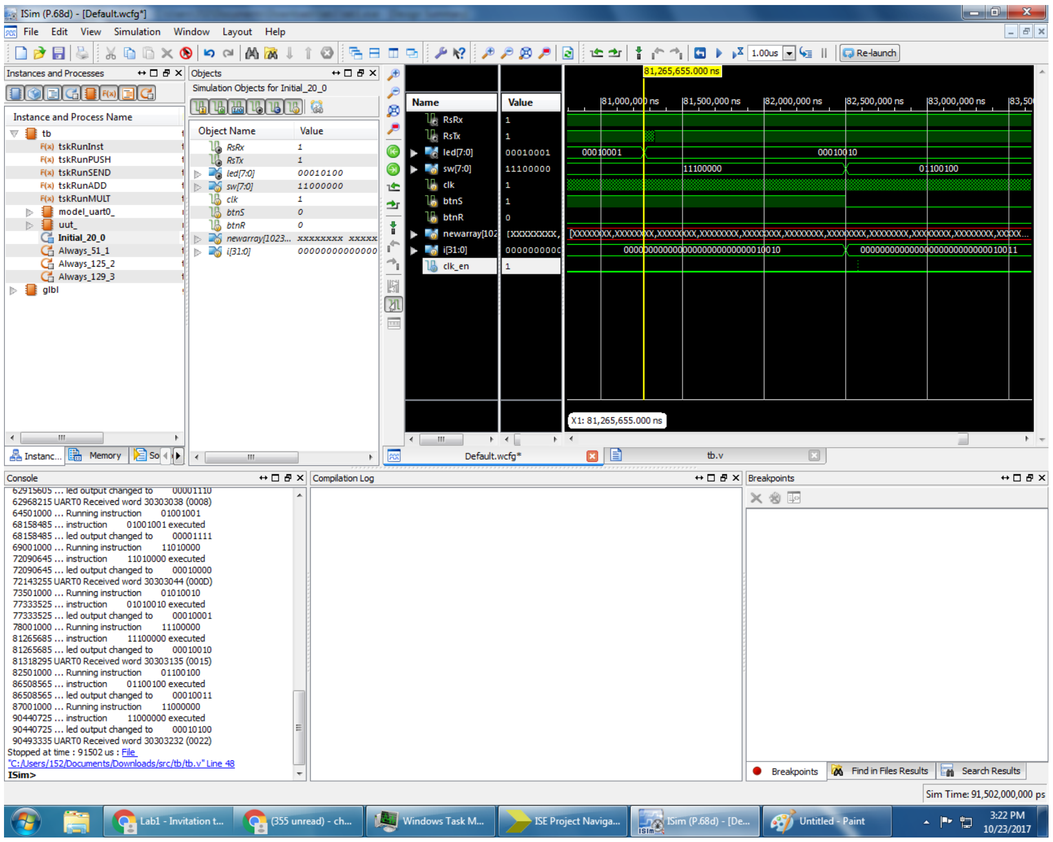
Clock Dividers

1. We did positive edge to consecutive positive edge to measure the period for clk_en. The first one happened at t 81,265,655.000 ns, and another one at t 82,576,365.000 ns. Subtracting the 2 times gives the period: 82,576,365.000 - 81,265,655.000 ns = 1,310,710 ns.



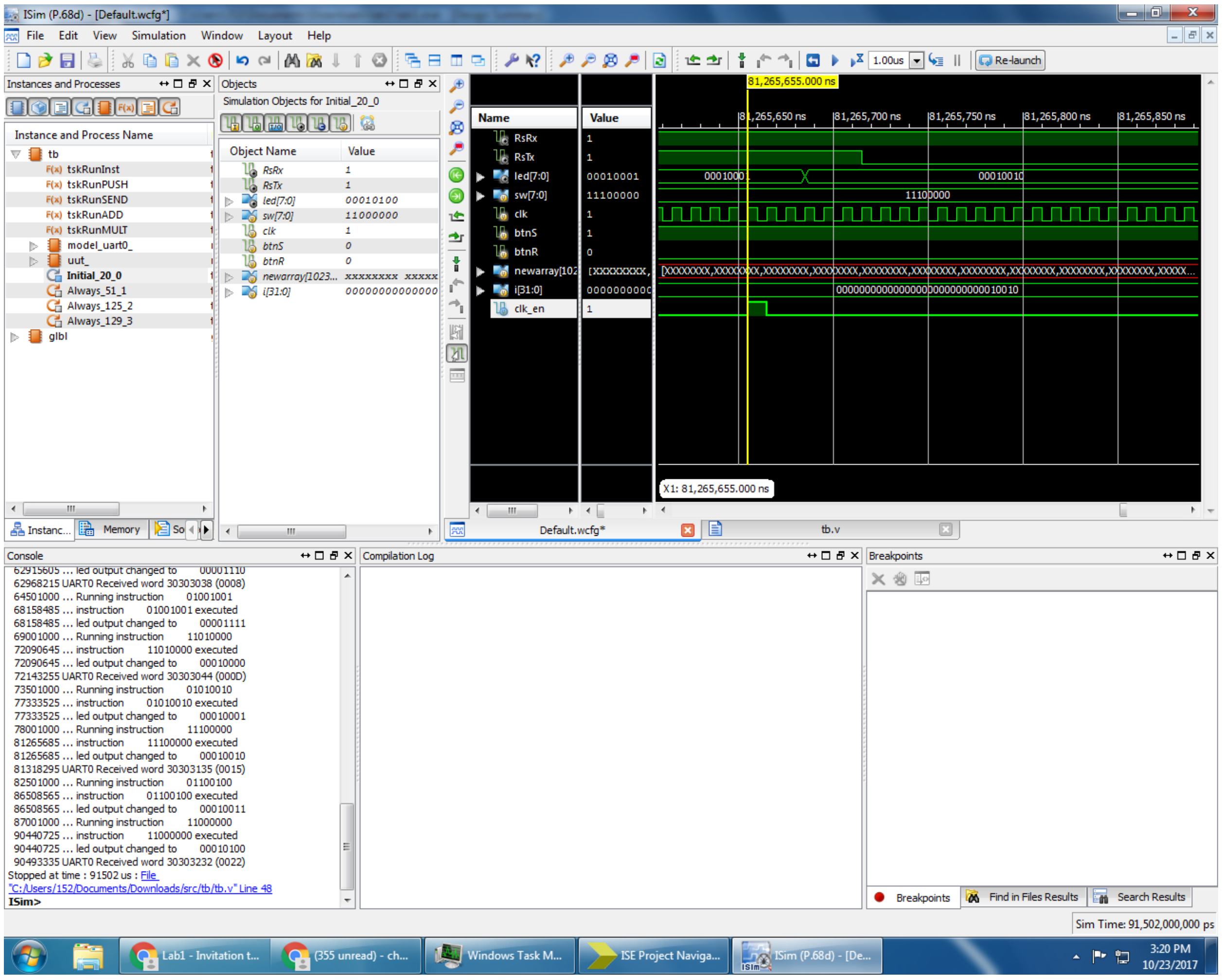
Name	Value
RsRx	1
RsTx	1
led[7:0]	00010010
sw[7:0]	01100100
clk	1
btnS	0
btnR	0
newarray[102	[XXXXXXXX,
i[31:0]	000000000
clk_en	1

```
62915605 ... led output changed to      00001110
62968215 UART0 Received word 30303038 (0008)
64501000 ... Running instruction      01001001
68158485 ... instruction      01001001 executed
68158485 ... led output changed to      00001111
69001000 ... Running instruction      11010000
72090645 ... instruction      11010000 executed
72090645 ... led output changed to      00010000
72143255 UART0 Received word 30303044 (000D)
73501000 ... Running instruction      01010010
77333525 ... instruction      01010010 executed
77333525 ... led output changed to      00010001
78001000 ... Running instruction      11100000
81265685 ... instruction      11100000 executed
81265685 ... led output changed to      00010010
81318295 UART0 Received word 30303135 (0015)
82501000 ... Running instruction      01100100
86508565 ... instruction      01100100 executed
86508565 ... led output changed to      00010011
87001000 ... Running instruction      11000000
90440725 ... instruction      11000000 executed
90440725 ... led output changed to      00010100
90493335 UART0 Received word 30303232 (0022)
Stopped at time : 91502 us : File
"C:/Users/152/Documents/Downloads/src/tb/tb.v" Line 48
ISim>
```


ISim (P.68d) - [Default.wcfg*]
File Edit View Simulation Window Layout Help
Re-launch
1.00us
81,265,655.000 ns
X1: 81,265,655.000 ns
Default.wcfg*
tb.v
Sim Time: 91,502,000,000 ps
3:22 PM
10/23/2017

Name	Value
RsRx	1
RsTx	1
led[7:0]	00010001
sw[7:0]	11100000
clk	1
btnS	1
btnR	0
newarray[102	[XXXXXXXX,
i[31:0]	000000000
clk_en	1

```
62915605 ... led output changed to      00001110
62968215 UART0 Received word 30303038 (0008)
64501000 ... Running instruction      01001001
68158485 ... instruction      01001001 executed
68158485 ... led output changed to      00001111
69001000 ... Running instruction      11010000
72090645 ... instruction      11010000 executed
72090645 ... led output changed to      00010000
72143255 UART0 Received word 30303044 (000D)
73501000 ... Running instruction      01010010
77333525 ... instruction      01010010 executed
77333525 ... led output changed to      00010001
78001000 ... Running instruction      11100000
81265685 ... instruction      11100000 executed
81265685 ... led output changed to      00010010
81318295 UART0 Received word 30303135 (0015)
82501000 ... Running instruction      01100100
86508565 ... instruction      01100100 executed
86508565 ... led output changed to      00010011
87001000 ... Running instruction      11000000
90440725 ... instruction      11000000 executed
90440725 ... led output changed to      00010100
90493335 UART0 Received word 30303232 (0022)
Stopped at time : 91502 us : File
"C:/Users/152/Documents/Downloads/src/tb/tb.v" Line 48
ISim>
```



Instance and Process Name
tb
tskRunInst
tskRunPUSH
tskRunSEND
tskRunADD
tskRunMULT
model_uart0_
uut_
Initial_20_0
Always_51_1
Always_125_2
Always_129_3
glbl

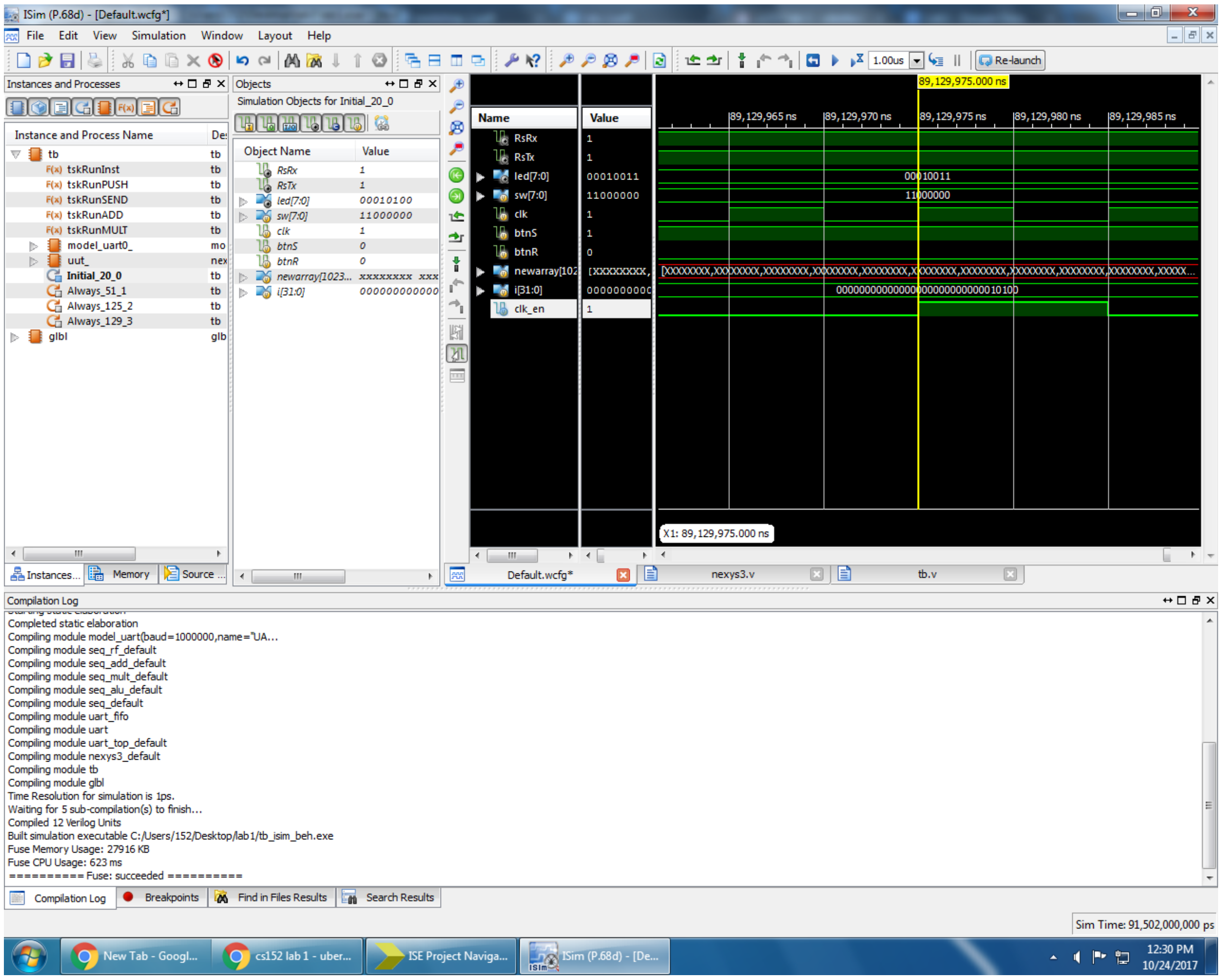
Object Name	Value
RsRx	1
RsTx	1
led[7:0]	00010100
sw[7:0]	11000000
clk	1
btnS	0
btnR	0
newarray[1023...	xxxxxxxx xxxxx
i[31:0]	0000000000000

Name	Value
RsRx	1
RsTx	1
led[7:0]	00010001
sw[7:0]	11100000
clk	1
btnS	1
btnR	0
newarray[102	[xxxxxxxxx,
i[31:0]	000000000c
clk_en	1

Console

```
62915605 ... led output changed to      00001110
62968215 UART0 Received word 30303038 (0008)
64501000 ... Running instruction      01001001
68158485 ... instruction      01001001 executed
68158485 ... led output changed to      00001111
69001000 ... Running instruction      11010000
72090645 ... instruction      11010000 executed
72090645 ... led output changed to      00010000
72143255 UART0 Received word 30303044 (000D)
73501000 ... Running instruction      01010010
77333525 ... instruction      01010010 executed
77333525 ... led output changed to      00010001
78001000 ... Running instruction      11100000
81265685 ... instruction      11100000 executed
81265685 ... led output changed to      00010010
81318295 UART0 Received word 30303135 (0015)
82501000 ... Running instruction      01100100
86508565 ... instruction      01100100 executed
86508565 ... led output changed to      00010011
87001000 ... Running instruction      11000000
90440725 ... instruction      11000000 executed
90440725 ... led output changed to      00010100
90493335 UART0 Received word 30303232 (0022)
Stopped at time : 91502 us : File "C:/Users/152/Documents/Downloads/src/tb/tb.v" Line 48
ISim>
```

2. D = T/P * 100% = 10/1,310,710 * 100% = 0.00763%

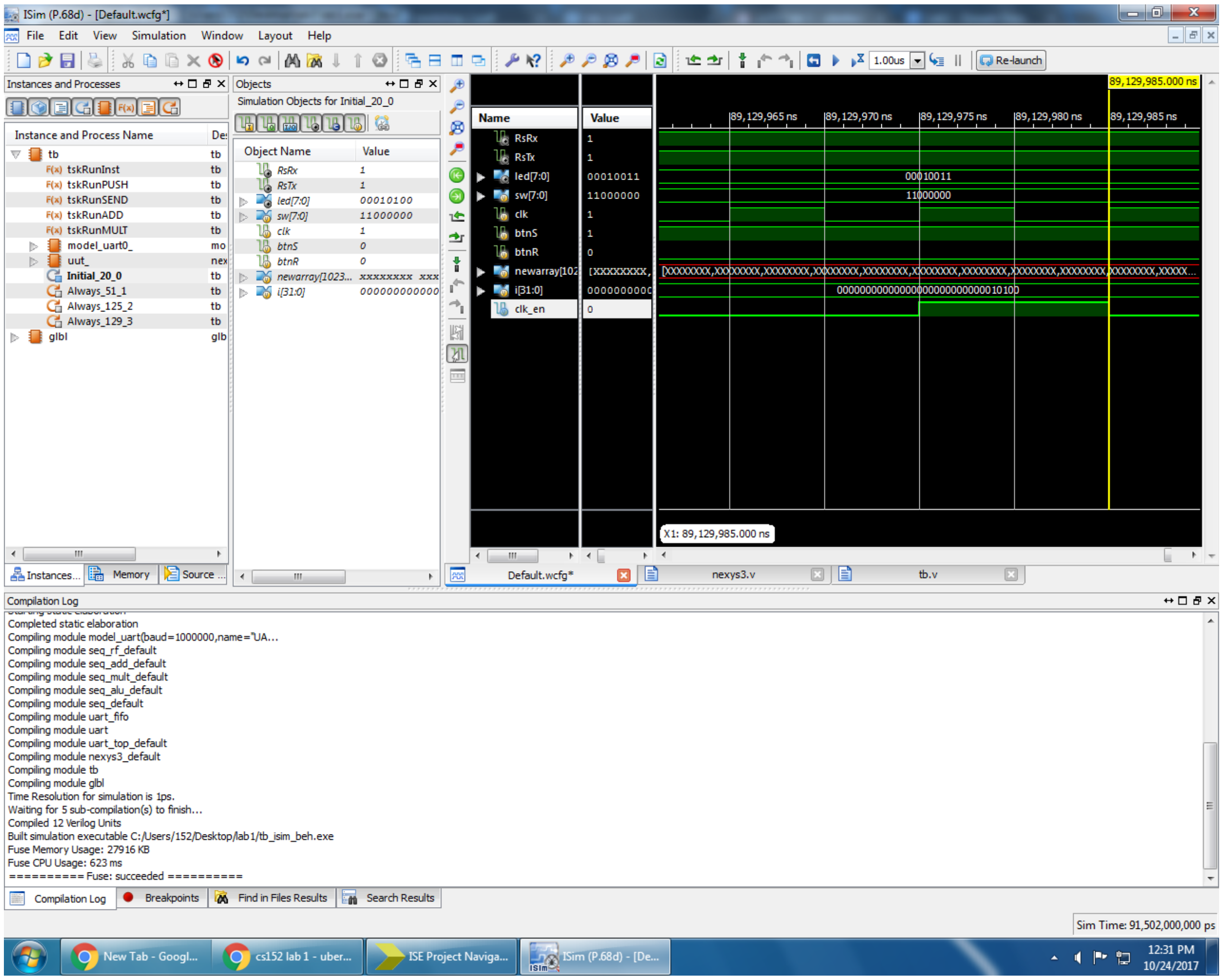


```
Instance and Process Name    De
tb                           tb
  tskRunInst                 tb
  tskRunPUSH                 tb
  tskRunSEND                 tb
  tskRunADD                  tb
  tskRunMULT                 tb
  model_uart0_               mo
  uut_                       nex
  Initial_20_0               tb
  Always_51_1                tb
  Always_125_2               tb
  Always_129_3               tb
glbl                         glb
```

```
Object Name          Value
RsRx                 1
RsTx                 1
led[7:0]             00010100
sw[7:0]              11000000
clk                  1
btnS                 0
btnR                 0
newarray[1023...     xxxxxxxx  xxx
i[31:0]              000000000000
```

```
Name             Value
RsRx             1
RsTx             1
led[7:0]         00010011
sw[7:0]          11000000
clk              1
btnS             1
btnR             0
newarray[102     [xxxxxxxx,
i[31:0]          000000000
clk_en           1
```

```
Compilation Log
Completed static elaboration
Compiling module model_uart(baud=1000000,name="UA...
Compiling module seq_rf_default
Compiling module seq_add_default
Compiling module seq_mult_default
Compiling module seq_alu_default
Compiling module seq_default
Compiling module uart_fifo
Compiling module uart
Compiling module uart_top_default
Compiling module nexys3_default
Compiling module tb
Compiling module glbl
Time Resolution for simulation is 1ps.
Waiting for 5 sub-compilation(s) to finish...
Compiled 12 Verilog Units
Built simulation executable C:/Users/152/Desktop/lab1/tb_isim_beh.exe
Fuse Memory Usage: 27916 KB
Fuse CPU Usage: 623 ms
========== Fuse: succeeded ==========
```



Instance and Process Name	De
tb	tb
tskRunInst	tb
tskRunPUSH	tb
tskRunSEND	tb
tskRunADD	tb
tskRunMULT	tb
model_uart0_	mo
uut_	nex
Initial_20_0	tb
Always_51_1	tb
Always_125_2	tb
Always_129_3	tb
glbl	glb

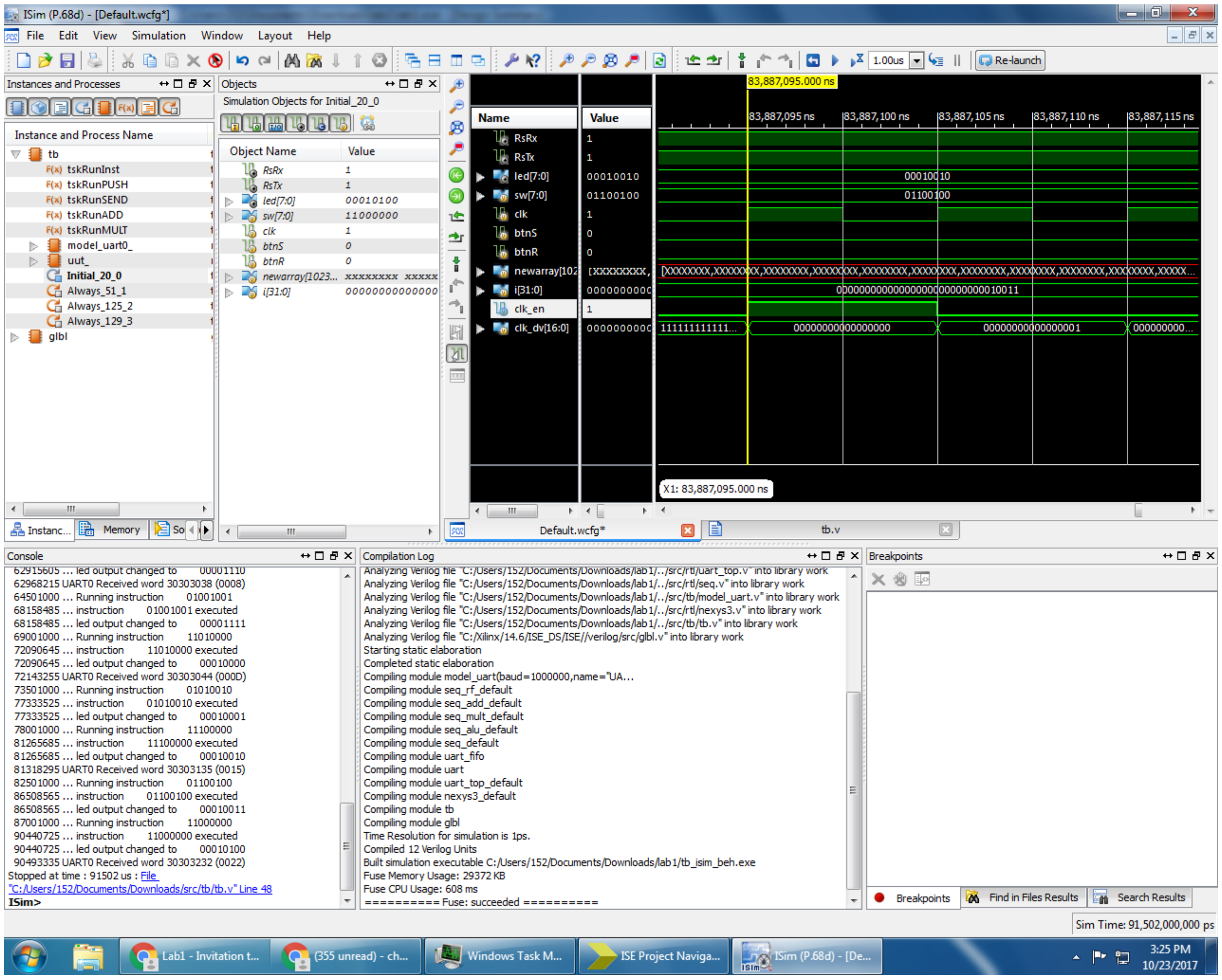
Object Name	Value
RsRx	1
RsTx	1
led[7:0]	00010100
sw[7:0]	11000000
clk	1
btnS	0
btnR	0
newarray[1023...	xxxxxxxx xxx
i[31:0]	000000000000

Name	Value
RsRx	1
RsTx	1
led[7:0]	00010011
sw[7:0]	11000000
clk	1
btnS	1
btnR	0
newarray[102	[XXXXXXXX,
i[31:0]	000000000
clk_en	0

```
00010011
11000000
[XXXXXXXX,XXXXXXXX,XXXXXXXX,XXXXXXXX,XXXXXXXX,XXXXXXXX,XXXXXXXX,XXXXXXXX,XXXXXXXX,XXXXXXXX,XXXXX...
00000000000000000000000000010100
```

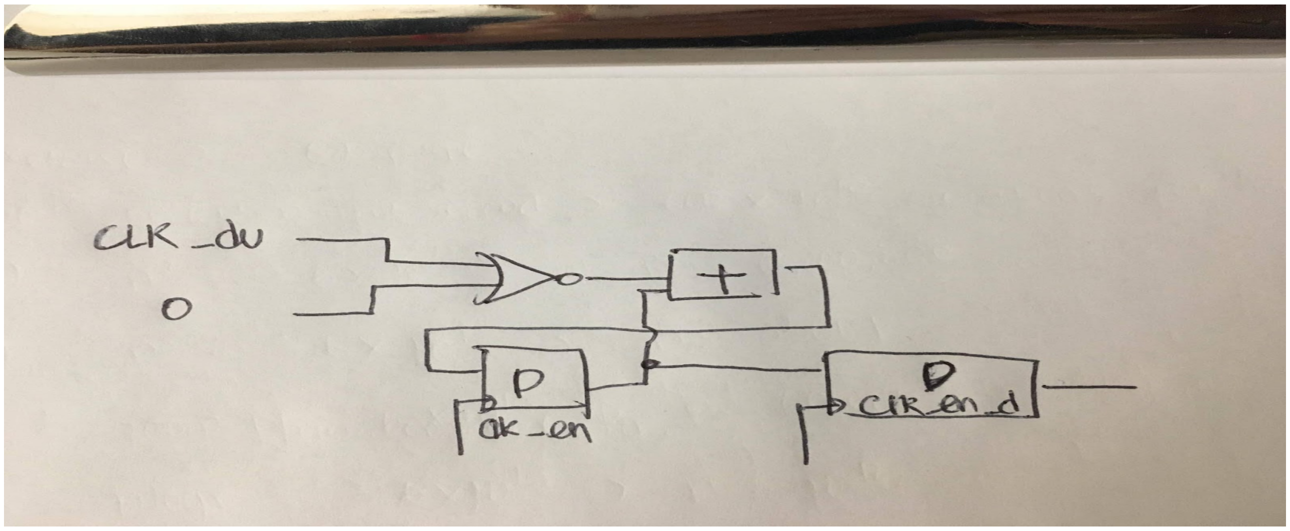
```
Completed static elaboration
Compiling module model_uart(baud=1000000,name="UA...
Compiling module seq_rf_default
Compiling module seq_add_default
Compiling module seq_mult_default
Compiling module seq_alu_default
Compiling module seq_default
Compiling module uart_fifo
Compiling module uart
Compiling module uart_top_default
Compiling module nexys3_default
Compiling module tb
Compiling module glbl
Time Resolution for simulation is 1ps.
Waiting for 5 sub-compilation(s) to finish...
Compiled 12 Verilog Units
Built simulation executable C:/Users/152/Desktop/lab1/tb_isim_beh.exe
Fuse Memory Usage: 27916 KB
Fuse CPU Usage: 623 ms
========== Fuse: succeeded ==========
```

3. Based on the waveform, we see that clk_dv is 00000000.



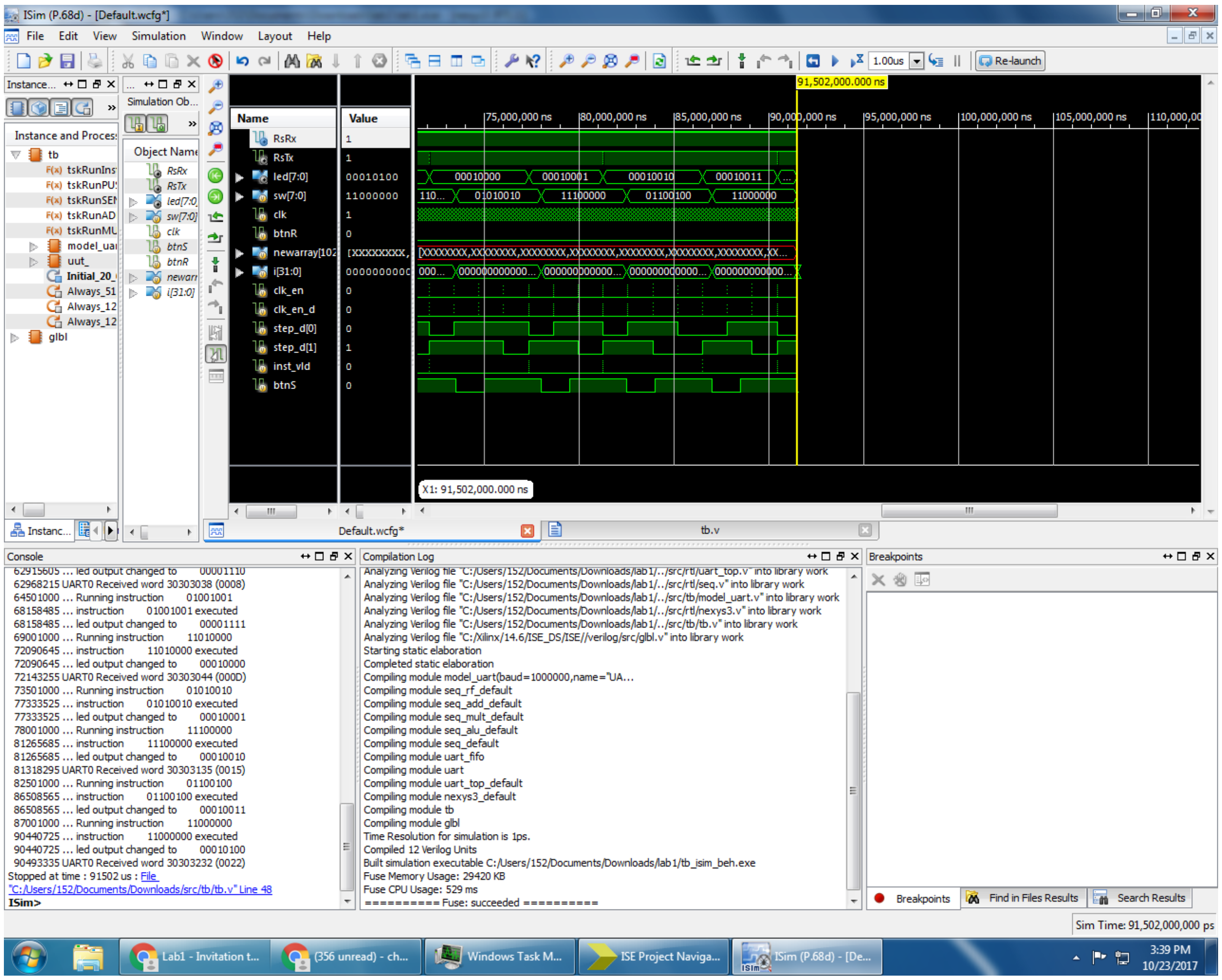
```
62915605 ... led output changed to      00001110
62968215 UART0 Received word 30303038 (0008)
64501000 ... Running instruction      01001001
68158485 ... instruction      01001001 executed
68158485 ... led output changed to      00001111
69001000 ... Running instruction      11010000
72090645 ... instruction      11010000 executed
72090645 ... led output changed to      00010000
72143255 UART0 Received word 30303044 (000D)
73501000 ... Running instruction      01010010
77333525 ... instruction      01010010 executed
77333525 ... led output changed to      00010001
78001000 ... Running instruction      11100000
81265685 ... instruction      11100000 executed
81265685 ... led output changed to      00010010
81318295 UART0 Received word 30303135 (0015)
82501000 ... Running instruction      01100100
86508565 ... instruction      01100100 executed
86508565 ... led output changed to      00010011
87001000 ... Running instruction      11000000
90440725 ... instruction      11000000 executed
90440725 ... led output changed to      00010100
90493335 UART0 Received word 30303232 (0022)
Stopped at time : 91502 us : File "C:/Users/152/Documents/Downloads/src/tb/tb.v" Line 48
ISim>
```

```
Analyzing Verilog file "C:/Users/152/Documents/Downloads/lab1/../src/rtl/uart_top.v" into library work
Analyzing Verilog file "C:/Users/152/Documents/Downloads/lab1/../src/rtl/seq.v" into library work
Analyzing Verilog file "C:/Users/152/Documents/Downloads/lab1/../src/tb/model_uart.v" into library work
Analyzing Verilog file "C:/Users/152/Documents/Downloads/lab1/../src/rtl/nexys3.v" into library work
Analyzing Verilog file "C:/Users/152/Documents/Downloads/lab1/../src/tb/tb.v" into library work
Analyzing Verilog file "C:/Xilinx/14.6/ISE_DS/ISE//verilog/src/glbl.v" into library work
Starting static elaboration
Completed static elaboration
Compiling module model_uart(baud=1000000,name="UA...
Compiling module seq_rf_default
Compiling module seq_add_default
Compiling module seq_mult_default
Compiling module seq_alu_default
Compiling module seq_default
Compiling module uart_fifo
Compiling module uart
Compiling module uart_top_default
Compiling module nexys3_default
Compiling module tb
Compiling module glbl
Time Resolution for simulation is 1ps.
Compiled 12 Verilog Units
Built simulation executable C:/Users/152/Documents/Downloads/lab1/tb_isim_beh.exe
Fuse Memory Usage: 29372 KB
Fuse CPU Usage: 608 ms
========== Fuse: succeeded ==========
```

4. 

Debouncing

1. The clk_en_d signal being high ensures that the clk_en signal is low. We want to be sure that clk_en is low, because that means the instruction word inst_wd is loaded. This is a requirement for us to safely set the instruction valid bit inst_vld to 1. We must use clk_en_d instead of clk_en, because inst_wd is assigned a value while clk_en is high. If we did use clk_en, then we could possibly set the inst_vld bit without properly loading inst_wd.
2. Yes, it would make the duty cycle 50% now because when you make it just clk_dv[16], instead of clk_en_dv[17], we don't set clk_en_dv[17] to 100….000 anymore, and the time the signal is high is much longer (2^16), while the period itself for the cycles stays the same. This gives us a result of D = T/P * 100% = 2^16 / 2^17 * 100% = ½ * 100% = 50%.
3. Look at waveform for this.



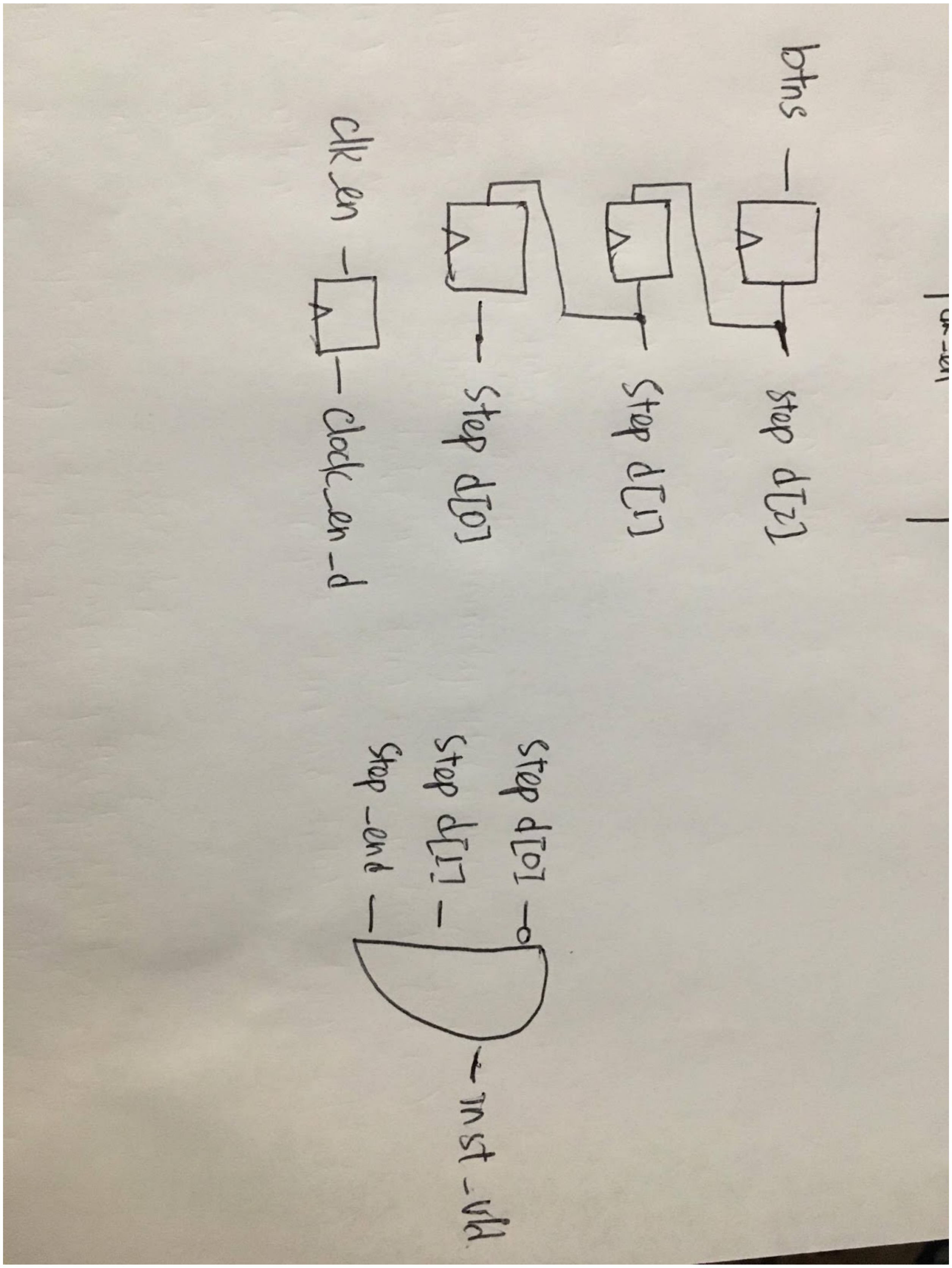
Console

```
62915605 ... led output changed to      00001110
62968215 UART0 Received word 30303038 (0008)
64501000 ... Running instruction      01001001
68158485 ... instruction      01001001 executed
68158485 ... led output changed to      00001111
69001000 ... Running instruction      11010000
72090645 ... instruction      11010000 executed
72090645 ... led output changed to      00010000
72143255 UART0 Received word 30303044 (000D)
73501000 ... Running instruction      01010010
77333525 ... instruction      01010010 executed
77333525 ... led output changed to      00010001
78001000 ... Running instruction      11100000
81265685 ... instruction      11100000 executed
81265685 ... led output changed to      00010010
81318295 UART0 Received word 30303135 (0015)
82501000 ... Running instruction      01100100
86508565 ... instruction      01100100 executed
86508565 ... led output changed to      00010011
87001000 ... Running instruction      11000000
90440725 ... instruction      11000000 executed
90440725 ... led output changed to      00010100
90493335 UART0 Received word 30303232 (0022)
Stopped at time : 91502 us : File "C:/Users/152/Documents/Downloads/src/tb/tb.v" Line 48
ISim>
```

Compilation Log

```
Analyzing Verilog file "C:/Users/152/Documents/Downloads/lab1/../src/rtl/uart_top.v" into library work
Analyzing Verilog file "C:/Users/152/Documents/Downloads/lab1/../src/rtl/seq.v" into library work
Analyzing Verilog file "C:/Users/152/Documents/Downloads/lab1/../src/tb/model_uart.v" into library work
Analyzing Verilog file "C:/Users/152/Documents/Downloads/lab1/../src/rtl/nexys3.v" into library work
Analyzing Verilog file "C:/Users/152/Documents/Downloads/lab1/../src/tb/tb.v" into library work
Analyzing Verilog file "C:/Xilinx/14.6/ISE_DS/ISE//verilog/src/glbl.v" into library work
Starting static elaboration
Completed static elaboration
Compiling module model_uart(baud=1000000,name="UA...
Compiling module seq_rf_default
Compiling module seq_add_default
Compiling module seq_mult_default
Compiling module seq_alu_default
Compiling module seq_default
Compiling module uart_fifo
Compiling module uart
Compiling module uart_top_default
Compiling module nexys3_default
Compiling module tb
Compiling module glbl
Time Resolution for simulation is 1ps.
Compiled 12 Verilog Units
Built simulation executable C:/Users/152/Documents/Downloads/lab1/tb_isim_beh.exe
Fuse Memory Usage: 29420 KB
Fuse CPU Usage: 529 ms
========== Fuse: succeeded ==========
```

4.


btns
step d[2]
step d[1]
step d[0]
clk_en
clock_en_d
step d[0]
step d[1]
step_end
inst_vld

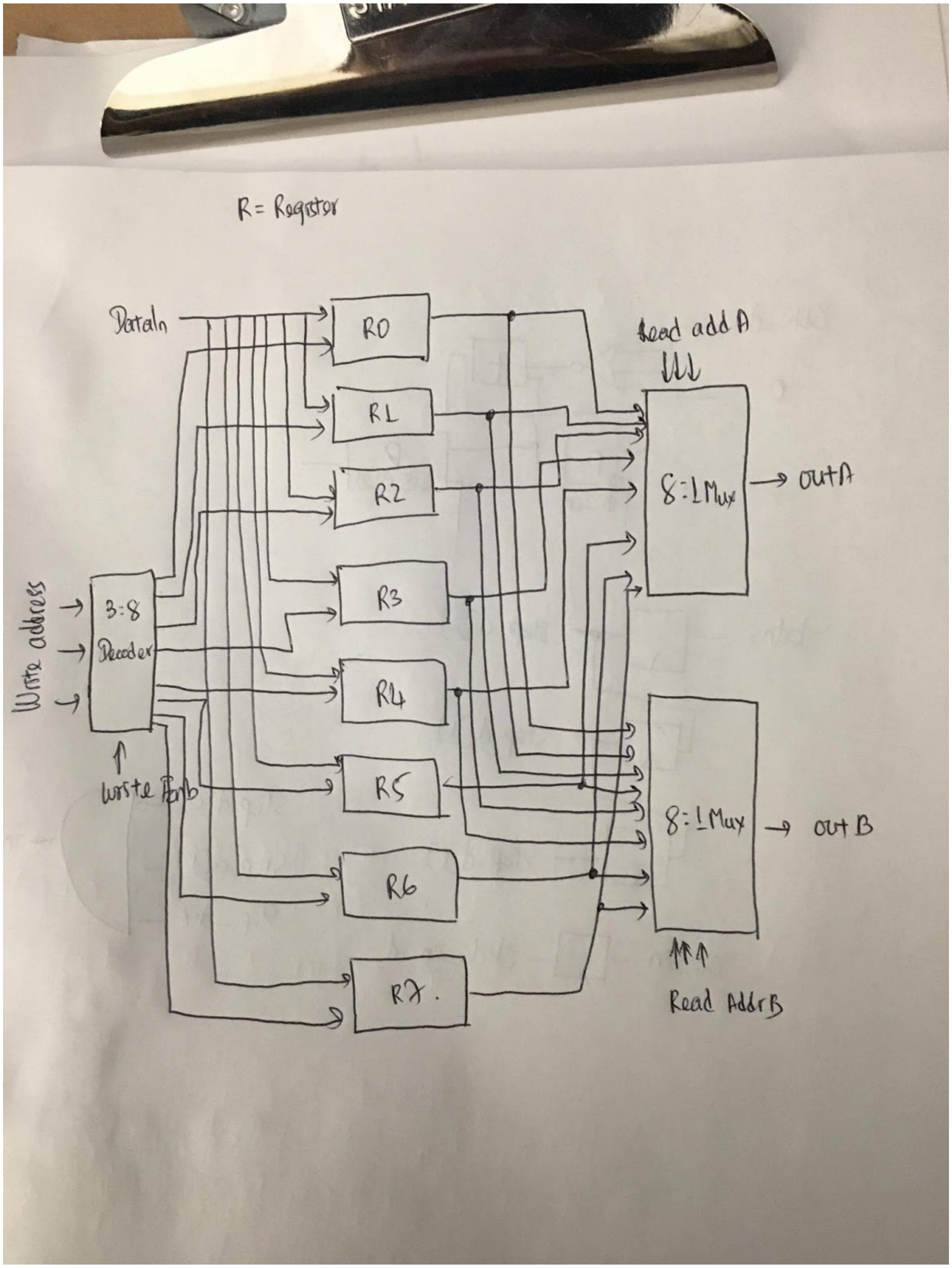
Register File

1. In the code below, the very last line, in the else if statement sends in non-zero values through the <= action. This is an example of sequential logic:

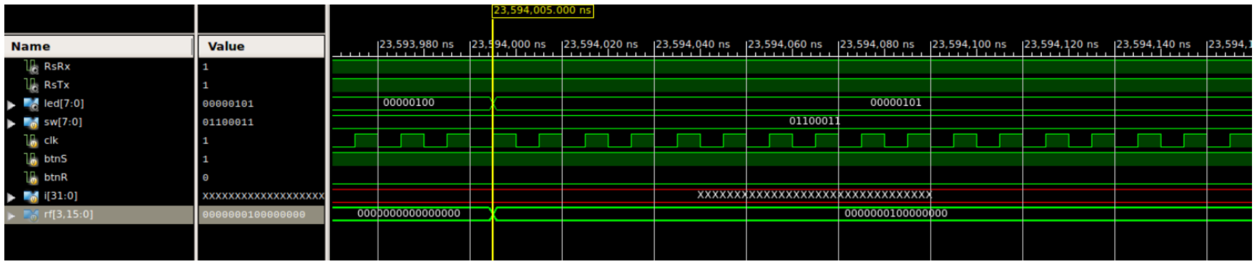
```
always @ (posedge clk)
    if (rst)
      begin
         for (i=0;i<seq_num_regs;i=i+1)
            rf[i] <= 0;
      end
    else if (i_wstb)
      rf[i_wsel] <= i_wdata;
```

2. This is a combinatorial logic. If we were to manually implement the readout logic, we would use register, decoder and multiplexer.

5.


R = Register
DataIn
R0
R1
R2
R3
R4
R5
R6
R7.
Read add A
8:1 Mux
out A
8:1 Mux
out B
Read Addr B
Write address
3:8 Decoder
write Enb

3.



Name	Value
RsRx	1
RsTx	1
led[7:0]	00000101
sw[7:0]	01100011
clk	1
btnS	1
btnR	0
i[31:0]	XXXXXXXXXXXXXXXXXXX
rf[3,15:0]	0000000100000000

Workshop 2

1. task tskRunInst;

```
            input [7:0] inst;
            begin
                        $display ("%d ... Running instruction %08b", $stime, inst);
                        sw = inst;
                         #1500000 btnS = 1;
                        #3000000 btnS = 0;
            end
endtask
```

2. task tskRunPUSH; task tskRunSEND; task tskRunADD; task tskRunMULT;