1. CSE 140L Lab 1

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Academic Integrity

Your work will not be graded unless the signatures of all members of the group are present beneath the honor code.

To uphold academic integrity, students shall:

- Complete and submit academic work that is their own and that is an honest and fair representation of their knowledge and abilities at the time of submission.
- Know and follow the standards of CSE 140L and UCSD.

Please sign (type) your name(s) below the following statement:

I pledge to be fair to my classmates and instructors by completing all of my academic work with integrity. This means that I will respect the standards set by the instructor and institution, be responsible for the consequences of my choices, honestly represent my knowledge and abilities, and be a community member that others can trust to do the right thing even when no one is watching. I will always put learning before grades, and integrity before performance. I pledge to excel with integrity.

(Wensheng Yu)
(Chuning Liu)

Free Response

Please answer the following questions.

1. How do we define the combinational logic in SystemVerilog? (Hint: Think about keywords)(1 pts)

   Keywords: always_comb, assign
   In a combinational circuit, the output depends only on the present value of the inputs.

2. What keyword do you use in SystemVerilog to indicate sequential logic? (1 pts)

   always_ff

3.

Code 1:

```
always @(posedge clk) begin
    b <= a;
    c <= b;
end
```

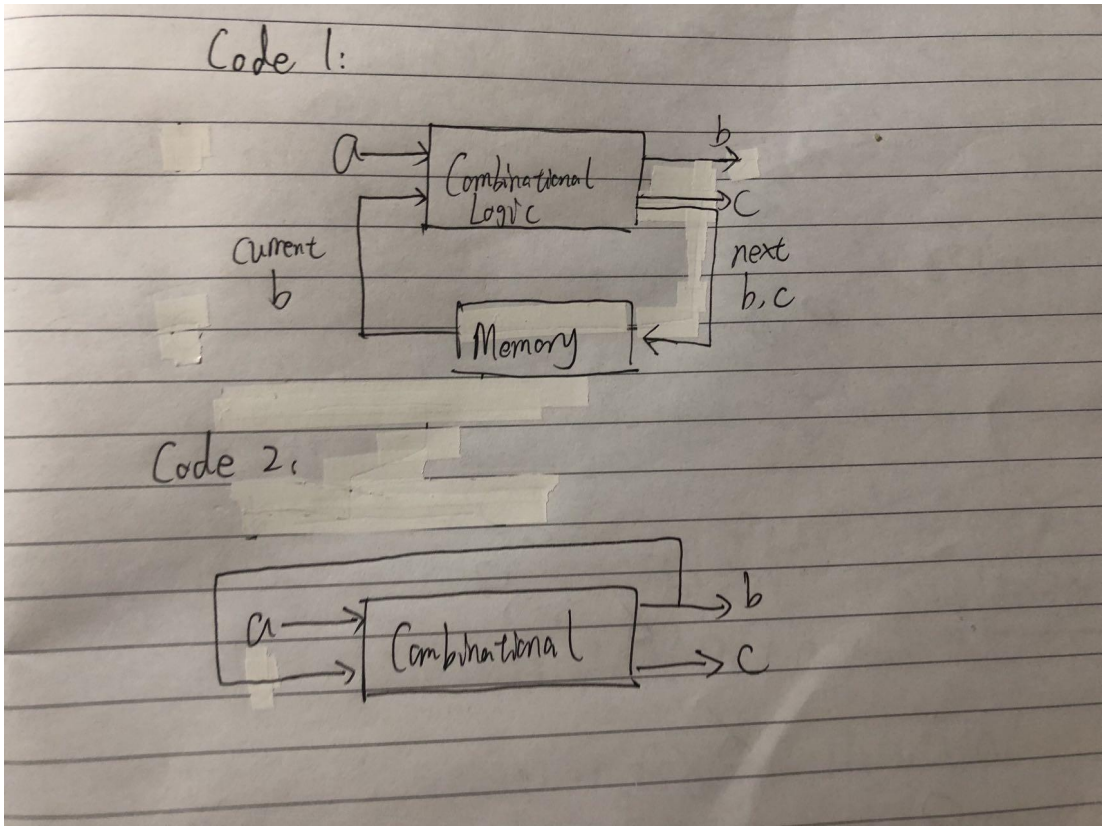
a, b and c are defined as logic.

Code 2:

```
always @(posedge clk) begin
    b = a;
    c = b;
end
```

What is the difference between Code1 and Code2? (1 pts)
Draw the Synthesized Circuit for both codes? (2 pts)

Code1 uses sequential logic and code2 uses combinational logic. In code 1, c is assigned to the current value of b in the memory, while in code 2 c is assigned to the value of a since the value of b changed in the last step.
Drawing:



4. Perform the following operations: (2 pts). (Write the output).

   Logical Left Shift of 00011010 by 3. (00011010 <<3)
   Arithmetic Right Shift of 11010011 by 4. (11010011 >>> 4).

Logical Left Shift: 11010000
Arithmetic Right Shift: 11111101

5. Why do we need nonblocking assignments in SystemVerilog? (2 pts)

Because we can use nonblocking assignments whenever we want to make several register assignments within the same time step without regard to order or dependence upon each other.

6. How do we represent the ternary operator in System Verilog? Why do we need it? (2pts)

Represent: <Condition> ? <variable 1> : <variable 2>

A ternary operator allows you to assign one value to the variable if the condition is true, and another value if the condition is false.

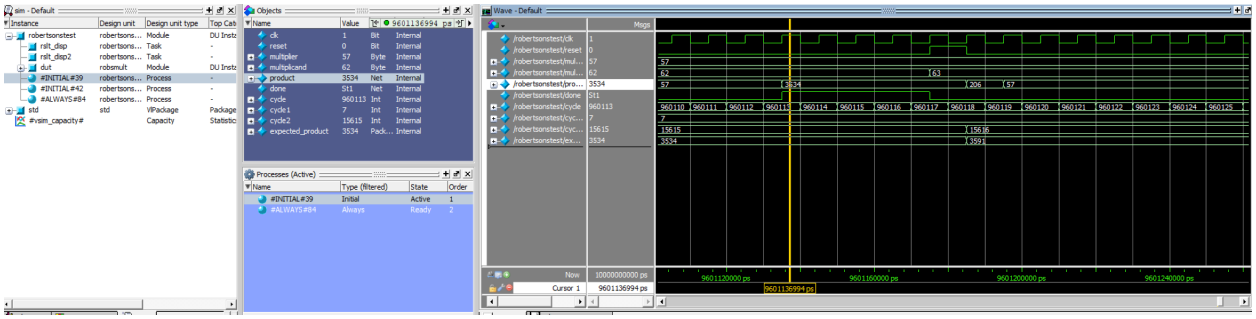
Screenshots

Screenshot of your ModelSim transcript, showing the expected results vs. yours. (2 pts)

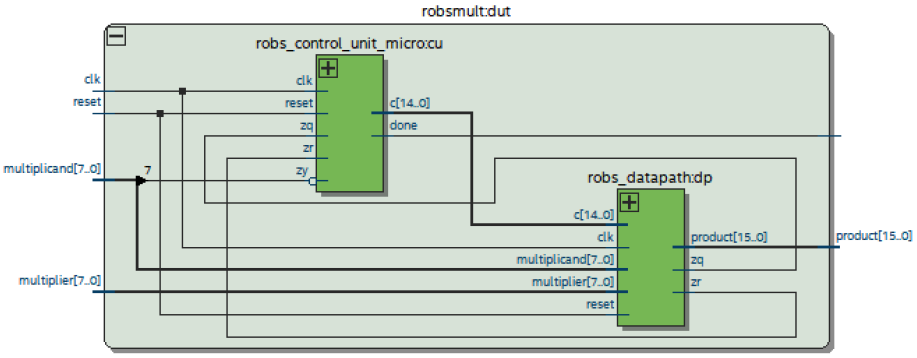
```
SIM 2> run -all
 Simulation succeeded 0000 = 0000 = 00 * 00
 Simulation succeeded       0 =       0 =     0 *     0
 Simulation succeeded 001e = 001e = 05 * 06
 Simulation succeeded      30 =      30 =     5 *     6
 Simulation succeeded ffdd = ffdd = 07 * fb
 Simulation succeeded     -35 =     -35 =     7 *    -5
 Simulation succeeded ffe2 = ffe2 = fb * 06
 Simulation succeeded     -30 =     -30 =    -5 *     6
 Simulation succeeded ffc8 = ffc8 = f9 * 08
 Simulation succeeded     -56 =     -56 =    -7 *     8
 Simulation succeeded 001e = 001e = fb * fa
 Simulation succeeded      30 =      30 =    -5 *    -6
 Simulation succeeded 0024 = 0024 = f7 * fc
 Simulation succeeded      36 =      36 =    -9 *    -4
** Note: $stop    : L:/My Documents/Lab1/robertsonstest.sv(39)
   Time: 10 ms  Iteration: 0  Instance: /robertsonstest
```

Screenshot a portion of your ModelSim waveform viewer, showing a done flag / reset cycle, the incoming operand values, and the product value. (3 pts)

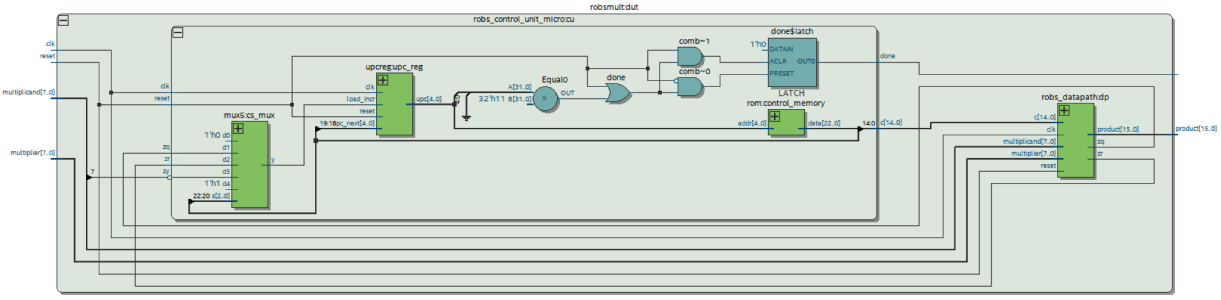
We want to see at least all the variables from `robertsontest`, this can be done by right clicking on `robertsontest` and then “Add wave.” Please zoom in to the level so that we can see when done is 1, you have the correct product for at least one pair of multiplier and multiplicand. It is fine if you show multiple pairs.



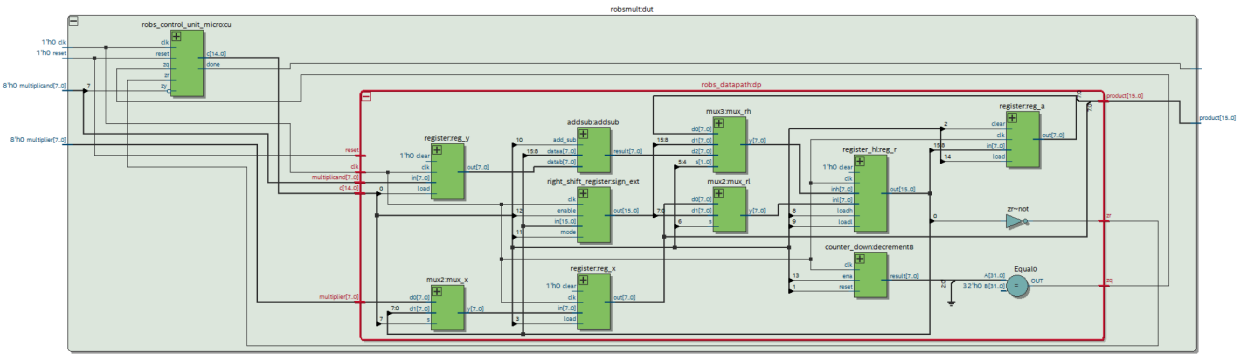
Screenshot of your Quartus RTL Viewer top level (control block and data path block) (3 pts)



Screenshot of your Quartus RTL Viewer top level of the control block (3 pts)



Screenshot of your Quartus RTL Viewer top level of the data path block (3 pts)



Please mention the contribution of the individual team members to the assignment. (0 pts)

Student 1 - Code and questions

Student 2 - Code and screenshots

Summary of success: we discussed in a group, and we searched on the internet or asked TA’s for help when facing questions.