Counters

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May 4, 2023

Objectives

The objective of this lab is to design and implement a decoder on the FPGA that can convert a 4-bit binary number inputted using the switches into a single digit of hexadecimal on the seven-segment display. The lab will involve creating a block diagram for the decoder design, determining the mapping for displaying each number 0-F on the seven-segment display, generating the functional truth table for the decoder, minimizing the logic for each segment of the decoder using Karnaugh Maps, simulating the design, and finally programming and testing the hardware implementation on the DE10-Lite. By completing this lab, participants will gain an understanding of the process involved in designing and implementing a decoder, become familiar with using Karnaugh Maps for logic minimization, and acquire hands-on experience in FPGA programming and testing. The lab aims to provide a comprehensive learning experience, covering the theoretical concepts and practical aspects of decoder design and FPGA implementation.

Equipment

- Quartus Prime Lite Edition V. 18.0/18.1
- DE10-Lite kit with MAX10 10M50DAF484C7G FPGA
- USB to USB-B cable
- The ECE 271 textbook, Digital Design and Computer Architecture by Drs. David and Sarah Harris

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Design

Design description, block diagram, pin placement labels

Simulation

Simulation description, results table

Implementation

Implementation description, results table, picture of implementation

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Observations

Observations of the lab

Conclusion

Summary of the lab and its outcomes

Study Questions

1. Study question 1

Answer to question 1

2. Study question 2

Answer to question 2

3. Study question 3

Answer to question 3

4. Study question 4

Answer to question 4

5. Study question 5

Answer to question 5

Appendix