Counters

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Objectives

The objective of this lab is to design and implement a counter system that utilizes T flip-flops to effectively slow down a 50 MHz clock frequency to achieve a frequency as close to 1 Hz as possible. The DE10-Lite will be utilized to drive all six digits of its seven-segment displays by outputting a counter to each digit, synchronized with the clock signal. This lab aims to enhance our knowledge and skills in digital logic design by introducing the concept of state memory and utilizing the FPGA's clock as a means of logic control. By successfully completing this lab, we will deepen our understanding of digital circuits and gain practical experience in implementing clock-controlled systems.

Equipment

- Quartus Prime Lite Edition V. 18.0/18.1
- DE10-Lite kit with MAX10 10M50DAF484C7G FPGA
- USB to USB-B cable
- The ECE 271 textbook, Digital Design and Computer Architecture by Drs. David and Sarah Harris

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Design

In the previous lab we developed a logic design that mapped a 4-bit binary number that was inputed via on board switches to a seven segment display which displayed the binary number in hexidecimal. This will be used as a basic building block for the design of a clock-controlled counter.

T Flip Flops will be used to divide the clock signal. When feeding a clock signal into a TFF the output will effectively output at half the frequency of the input clock. By cascading four of these TFF's we are able to output a four bit counter, theleast significant bit being the output clock of the first TFF and the most significant bit being the output clock of the fourth. These outputs will be mapped to the 6 seven-segment displays available on the board, the fastest digit on the right and the 1 Hz digit on the left.

Clock	**Reset**	**T**	**Q**
X	0	X	0
1	1	0	Q
1	1	1	$\sim Q$
1	1	X	Q

Table 1: T Flip-Flop Truth Table

In order to achieve this we need to pay close attention to the amount of TFF's we use. Each TFF is acts as a division by two to the input clock speed. For this implementation we will be using the DE110-Lite's 50 MHz clock. To find the number of TFF's needed to achieve a frequency of near 1 Hz we count how many times we need to divide 50,000,000 until we are as close to 1 as possible. The closest being 26 total TFF's. This should give us a counter frequency of approximately 0.75 Hz.

We know that there will be at least 24 flip flops used to output to the 6 seven-segment displays. This means there must be included some extra TFF's at the beginning of the schematic to act as a divider.

Simulation

Simulation description, results table

Implementation

Implementation description, results table, picture of implementation

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Observations

Observations of the lab

Conclusion

Summary of the lab and its outcomes

Study Questions

1. Study question 1

Answer to question 1

2. Study question 2

Answer to question 2

3. Study question 3

Answer to question 3

4. Study question 4

Answer to question 4

5. Study question 5

Answer to question 5

Appendix