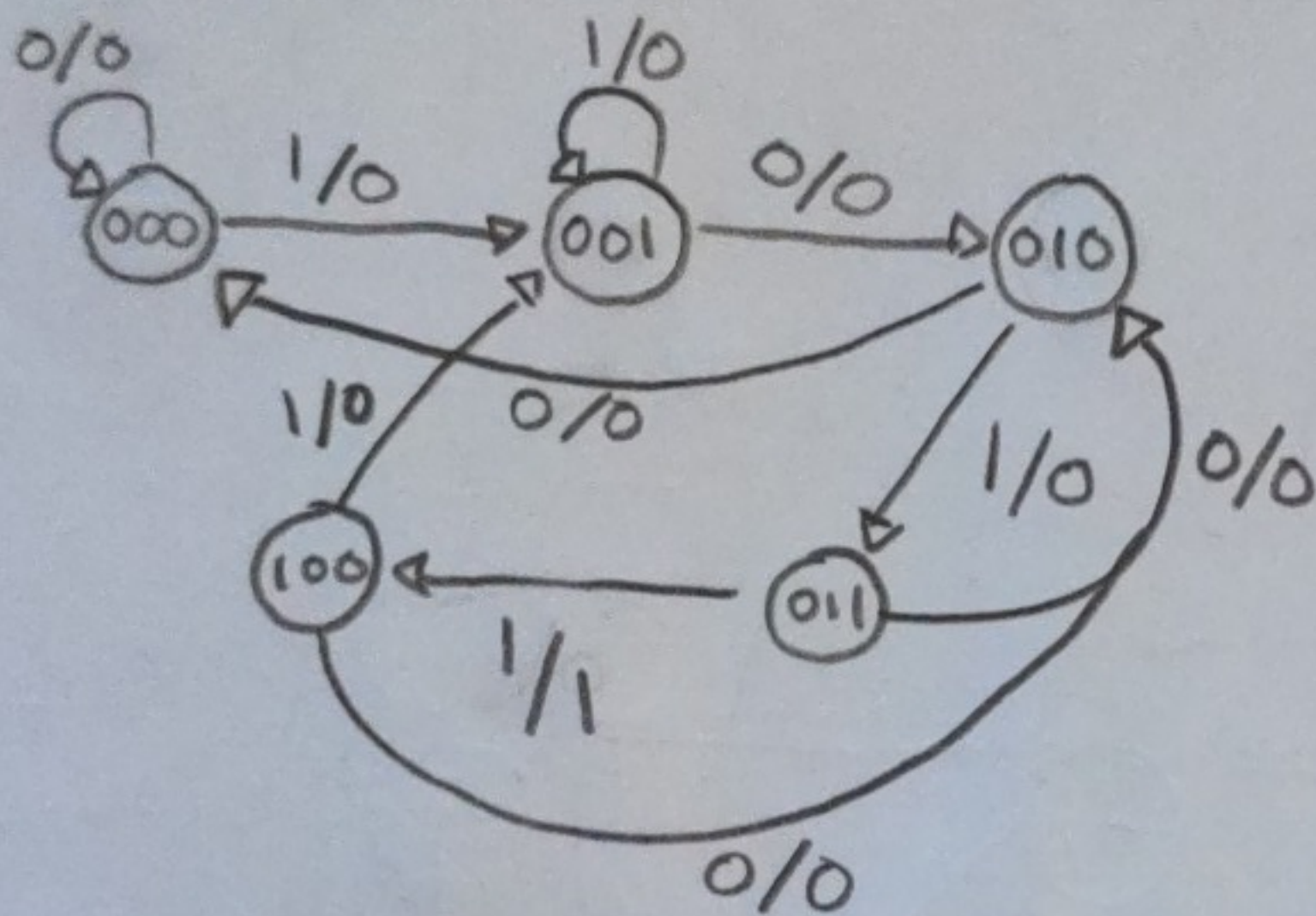


Show your work. The correct answer is only half the credit

1.) Design a Sequence Recognizer that will recognize the sequence 1011 by designing a finite state machine (FSM). The input will be (X), and when the pattern is seen, the output (Z) will be 1. Use the **Mealy Machine** model.

a.) Make a state diagram

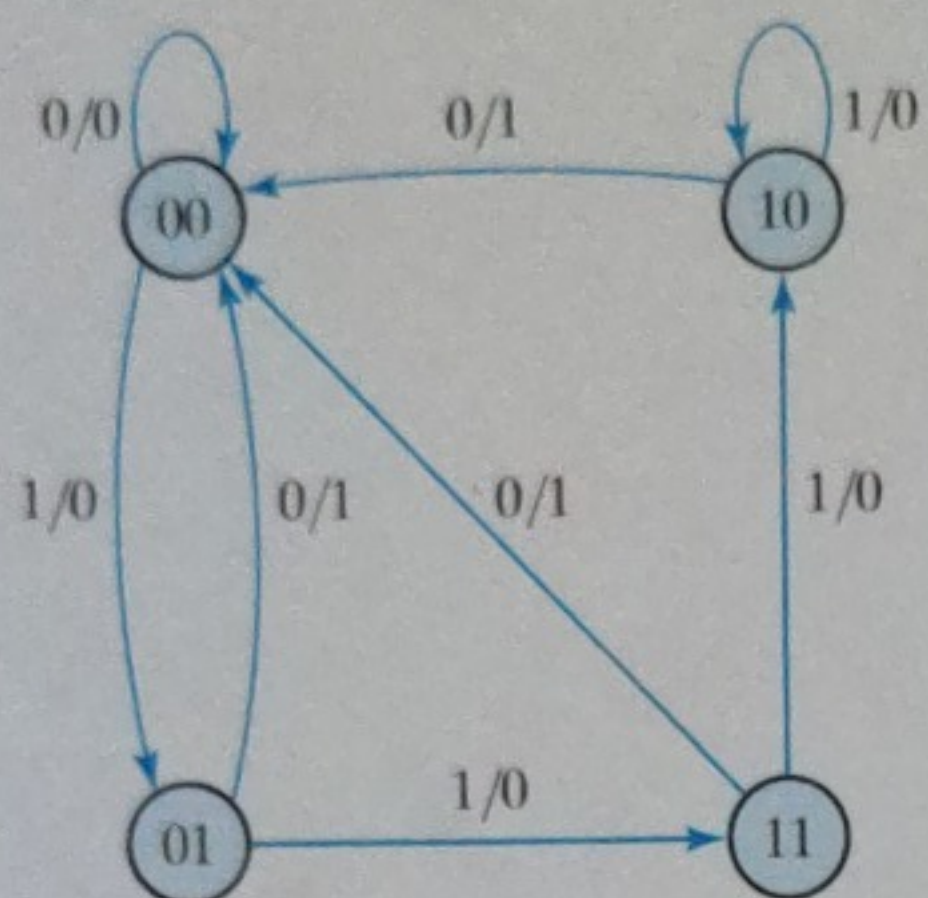
b.) Make a next state table



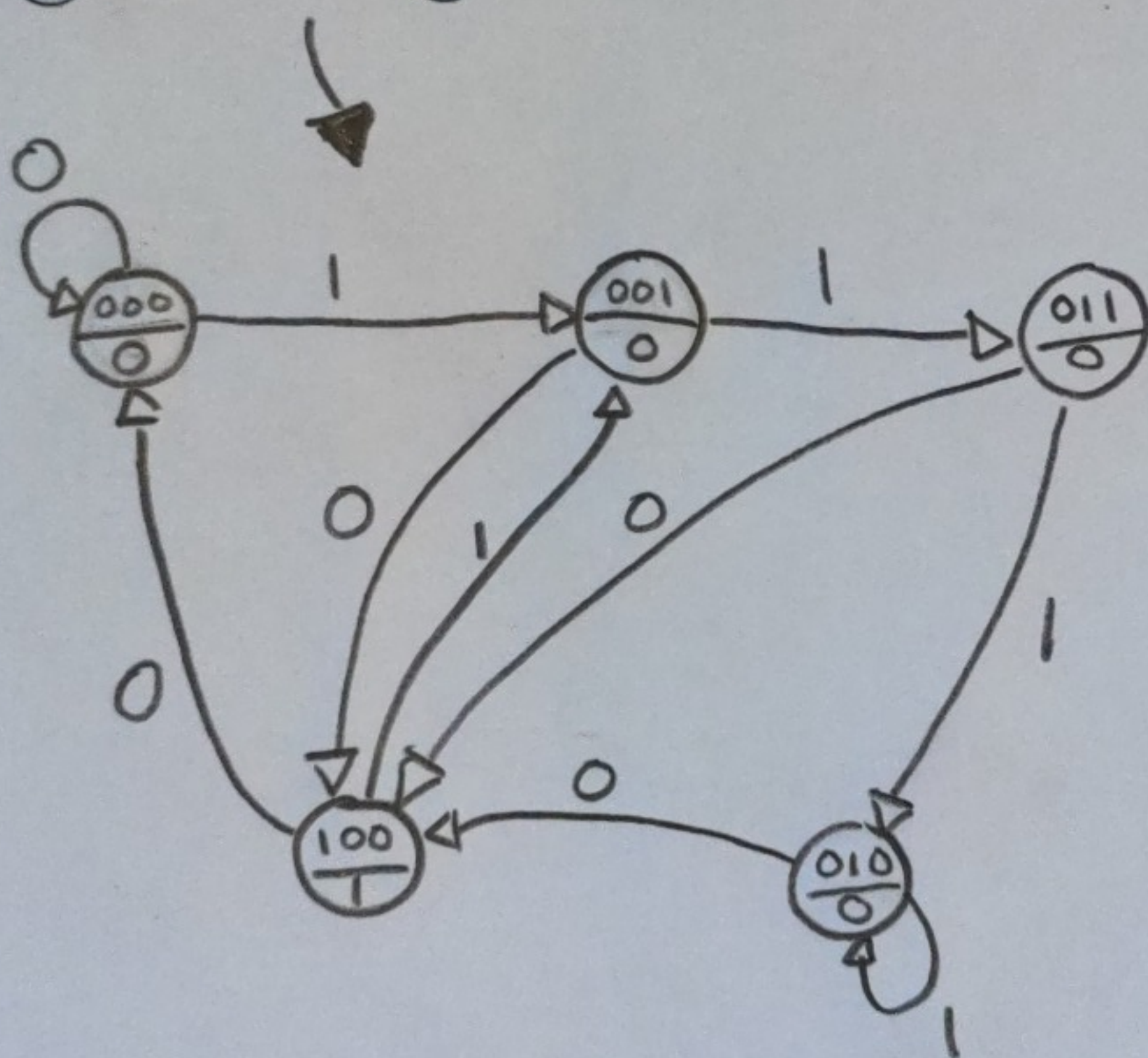
S_0 : none seen 5 states
 S_1 : "1" seen 3 Flip
 S_2 : "10" seen Flops
 S_3 : "101" seen needed
 S_4 : "1011" seen

[illegible]

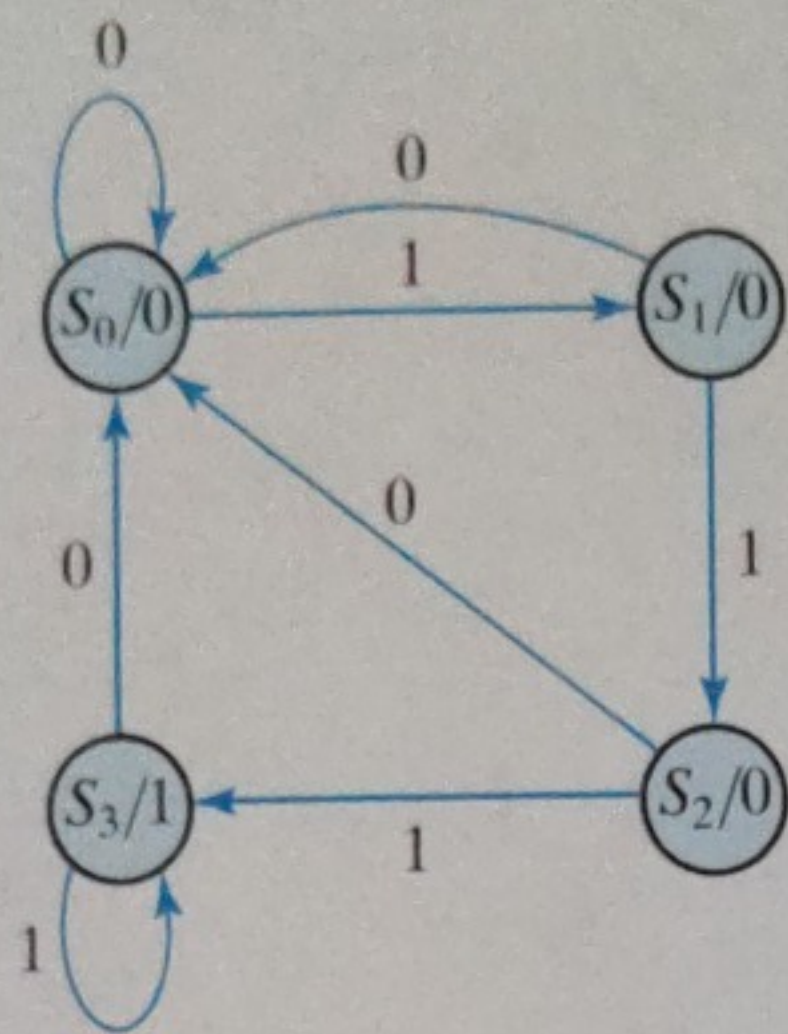
2.) Convert the state machine below from a Mealy state diagram to a Moore State diagram.



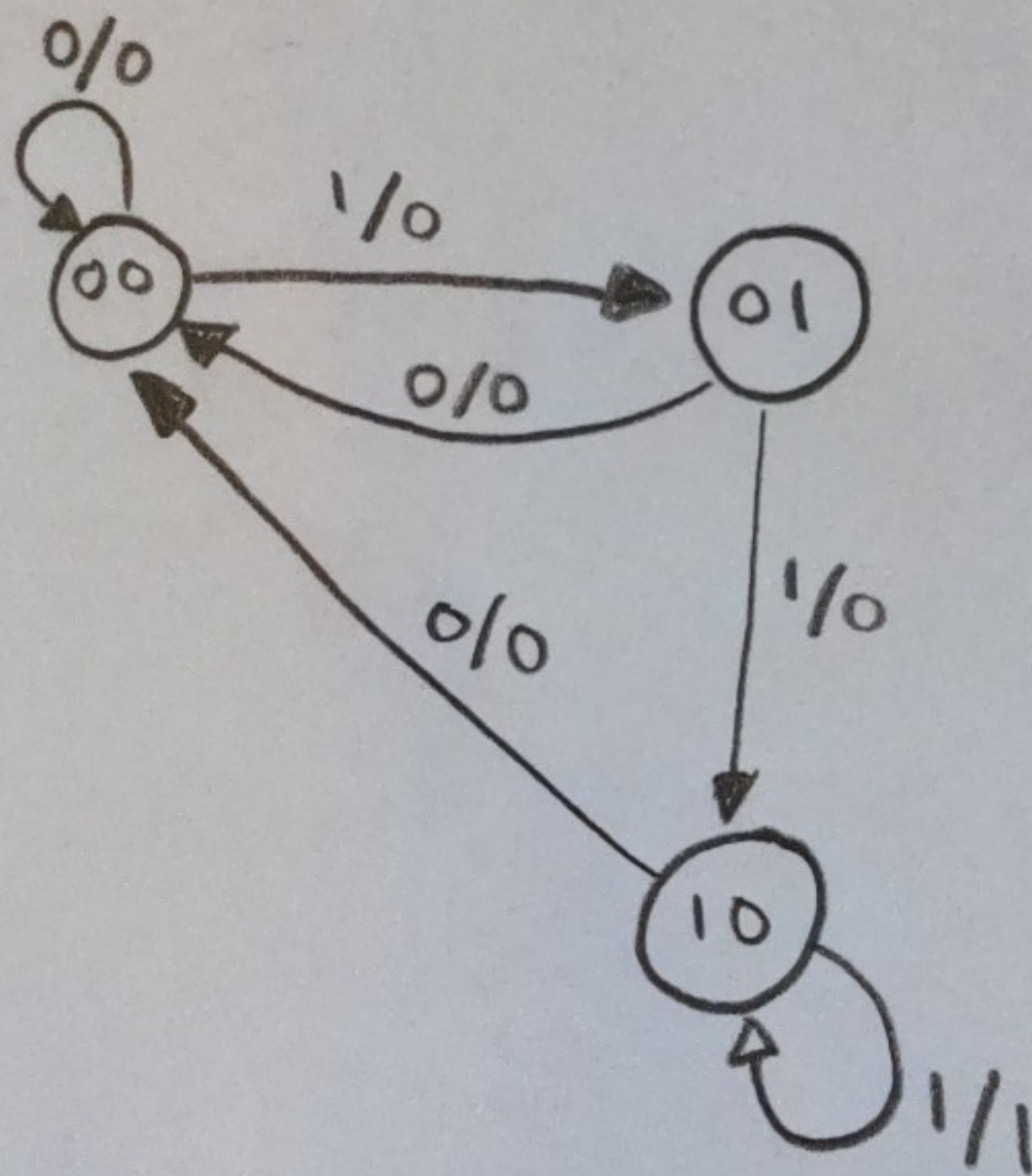
Needs one more state,
Will require 3 Ff instead
of 2.



3.) Convert the state machine below from a Moore state diagram to a Mealy State diagram.



Requires one less state.
Once you get to S_2 any input of 1 would bring you to output a 1 until 0 is detected.



4.) Registers are used to store data till it is ready to be used and is typically made with D flip-flops. One flip-flop is needed for each bit of data. Registers can load data in parallel and can also shift the data from left to right. A universal shift register talked about in class uses multiplexers to shift data into the flip-flops, in parallel, shift data to the right, shift data to the left or recycle the current value.

a. Draw the logic diagram of a Four-bit universal shift register using 4x1 multiplexers and D flip-flops that can load the data in parallel, shift the data left (Recycle MSB to LSB), shift the data right (Recycle LSB to MSB) or reload the current value depending on the select lines of the MUX. (This can be drawn by hand or by using the deeds software).

S1	S0	Action
0	0	Reload the current value
0	1	Shift the data right
1	0	Shift the data left
1	1	Load the data in parallel

