OSDT Meetup Hangzhou

2020-10-24 14:00 CST

- 吴伟 - 近期RISC-V基金会的动向以及参与的机会
- 史宁宁 - ART OptimizingCompiler 简析
- 李威威 - 学习 QEMU/RISU 的经验和讨论
- Free discussion

B站直播和TX会议在14:00前是静音的

放心，耳机没坏 ☺

近期RISC-V基金会的动向以及参与的机会

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关于我 | OSDT社区使命 | PLCT Lab 使命

OSDT社区负责人 / PLCT实验室创始人 / 连续创业者（迄今还没一个成功 ☺ ）

OSDT社区是为GCC/LLVM/Binutils/GDB/QEMU等底层开源开发工具的从业者和爱好者提供一个技术交流、聊天吐槽的小圈子

程序语言与编译技术实验室（PLCT）致力于成为编译技术领域的开源领导者，推进开源工具链及运行时系统等软件基础设施的技术革新， 具备主导开发和维护重要基础设施的技术及管理能力。与此同时，努力成为编译领域培养尖端人才的黄埔军校，推动先进编译技术在国内的普及和发展。

Changing Priorities

2010

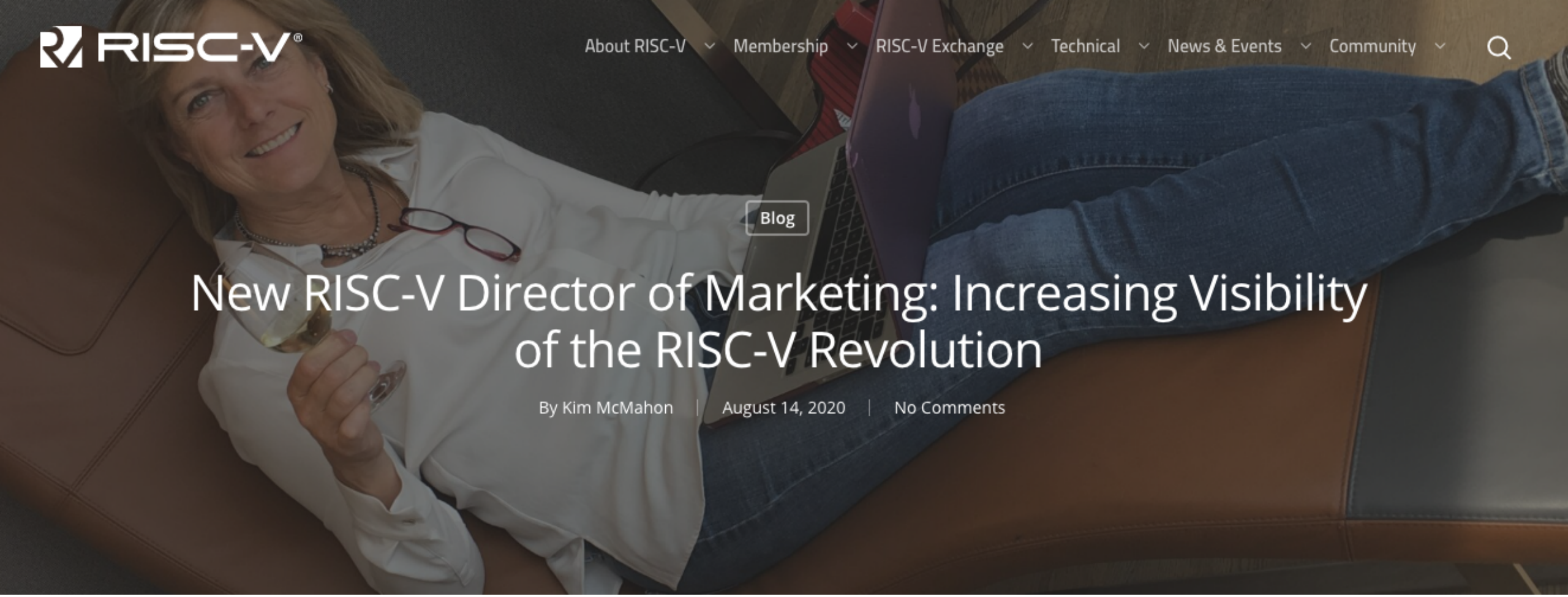
1. Be simple, efficient, extensible
2. Revisit legacy design decisions
3. Have basic software

(computer-architecture-driven project)

2020

1. Run all software
2. Be feature complete
   - ➢ see #1
3. Be stable
   - ➢ see #1
4. Support innovation
   - ➢ conflicts with #1,#2,#3?

(software-driven project)



Blog

New RISC-V Director of Marketing: Increasing Visibility of the RISC-V Revolution

By Kim McMahon | August 14, 2020 | No Comments

RISC-V International is at a pivotal point in its evolution. Through an open collaboration model, the RISC-V instruction set architecture (ISA) continues to increasingly gain momentum and disrupt the semiconductor industry. The global community is vast with domain expertise, industry experience, and geography which drives unconstrained opportunity. All this leads to an invested and healthy ecosystem in the RISC-V community.

When you look at the technology adoption lifecycle, I see RISC-V in the adoption stage with a healthy split between the organizations that are testing and developing on RISC-V to the organizations that have adopted the technology and are offering it to their customers. This is what I mean by a "pivotal point" – we are more than on the radar and deep in design wins!

RISC-V®

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Blog

RISC-V: Standing on the Shoulders of Giants

By Mark Himelstein | October 1, 2020 | No Comments

新设立的CTO职位；正在推送所有TG加速进度。
尤其是很多TG/SIG进展都说不上迅速或者高效。
TSC管理的部分正在 **大规模的** 调整和扩充。

RISC-V is officially a decade old. Here's a look at what the organization has accomplished and how it's moving forward with extensions targeting specific computing environments and the industry abroad.

Security

No matter the industry or implementation, companies must decide the level of security they need for their application. This is one of those cases where things have changed a lot since the beginning of RISC, from the need to use improved encryption standards like AES to guarding against malicious attacks such as Spectre and Meltdown.

The RISC-V cryptography task group, for example, has designed a number of instructions that are part of other extensions (e.g., RISC-V's Bit Manipulation Extension) and are devising cryptography specific extensions. So, if finance is securing every transaction, we define extensions that reduce the instructions needed by more than an order of magnitude for AES-128 encryption (from 1145 instructions down to 78 instructions on a 64-bit RISC-V design). With RISC-V's vector extension, high-performance implementations can further reduce the number of instructions down to less than one instruction per block while simultaneously providing improved resistance to side-channel attacks. RISC-V International is frugal in what we allow into our ISA, and the task groups must show the value of extensions and instructions to the community.

Vector Processing

Vector processing has been around for a long time since the ILLIAC, STAR, and, of course, CRAY-1 computers. It has always been valuable to market segments doing things like weather prediction and sonar. However, now with the renaissance in artificial intelligence (AI) and the proliferation of machine learning (ML) in all types of applications

RISC-V has the benefit of its time in histo
workloads. As a result, we have a set of
matrices.

Furthermore, because we're creating the
needed. For example, for the memory sy
tables and TLBs) and memory access (support for implementations to efficiently reduce cache impact for traversing operations).

安全领域几千个坑就有几千个机会
RVV 部分国内有PLCT、平头哥、卡姆派乐等
Code-size 有华为和PLCT在TG里

Reduced Code Size

Reduced code size requirements often emanate from embedded operations (such as IoT applications and computer devices). We created the C extension that supports 16-bit instruction versions for appropriate instructions that exist in our 32-bit-wide standard instruction set. As you might imagine, this reduces space requirements and improves cache locality.

RISC-V Catalyst for Change

By Calista Redmond | September 17, 2020 | No Comments

注意右边的中文版。中科院计算所包云岗教授推动。包老师进入了BoD之后开始积极推动RVI的几个方面。

Disruptions and plot twists are nothing new in the silicon industry. We've experienced full lifecycles from launch to exit. Pivots have been made in large architectures and small niche markets as the industry seeks better solutions to take on new workloads or improve competitive positions. Industry disruption holds the promise for all of us to take new approaches, engage with trusted partners, and solve complex challenges. With any disruption, there are discussions about the ripple effects on the industry. Today, many people are wondering whether companies will be investing more heavily in RISC-V as a result of our open model for licensing and collaboration or due to the potential limits placed by companies or nations on proprietary architectures. RISC-V is free and open so no single entity controls the technology. Companies, academia and institutions have freedom to innovate on the architecture and collectively can help to shape this rapidly evolving frontier of computing.

There is already a critical mass of more than 200 companies adopting RISC-V and actively contributing to the ecosystem from 50 countries, and that interest and investment in RISC-V will continue to grow from here. Many companies will look more closely at RISC-V for next generation designs, if

推动改变的RISC-V催化剂

在半导体行业，颠覆性故事和曲折的情节并不陌生。我们经常见证一个企业或一代产品从出现到消亡的整个生命周期。为应对新兴负载或提高竞争力，行业会寻求更好的解决方案，这驱动大众架构和小众市场汇聚到某个中心。行业中出现的颠覆让所有人有望获得新方法，找到信赖的盟友，解决复杂的问题。任何颠覆出现时，人们都会讨论它对于行业产生的连锁反应。如今，许多人想知道未来企业是否该在RISC-V上投入更多资金，一方面因为公司拥有的私有指令集可能会受到企业或国家的潜在限制，另一方面因为RISC-V倡导的开放许可和协作模式具有吸引力。RISC-V是免费且开放的，因此没有任何一个实体可以控制RISC-V技术。公司、学术界和机构都可以自由地在RISC-V指令集架构上进行创新，共同推动迅速发展的计算前沿。

目前，来自50多个国家超过200家企业已在使用RISC-V，为构建RISC-V生态做出了积极贡献，而对RISC-V的关注和投资也将会持续增长。许多当前尚未采用RISC-V的公司，也将会更加关注如何把RISC-V应用到它们的下一代产品中。对于企业与机构而言，RISC-V具有许多设计优势，是使产品组合多样化的一种好方法。RISC-V简单且可扩展的设计，能使其成为人工智能、汽车、云计算、边缘计算、物联网、机器学习、移动和5G等前沿应用的理想选择。

RISC-V Training Partners Bring professional learning to the worldwide community!

By Kim McMahon | August 17, 2020 | No Comments

PLCT 是第一批 PARTNER，感谢 Jesse Fang 教授引荐
同时正在积极成为 Online Learning 第一批PARNTER
（只要愿意花时间做贡献，就可以加入的）
（有很多收费项目的，不是必须免费）

When we think of learning at RISC-V International, it's a passion and drive to provide opportunities to the community to have access to the materials they want and need to further their education, make an impact in the RISC-V community, and improve themselves.

At this pivotal point in the RISC-V evolution, the technology is gaining momentum as it continues to disrupt the semiconductor industry by proving an open collaboration model is ideal to spur innovation. Learning and training are a priority. With this, we are pleased to announce the RISC-V Training Partner program.

RISC-V Training Partners are focused on providing RISC-V training in a professional setting. These partners enable expanded access to RISC-V topics from entry-level to deep dives in an effort to provide learning opportunities to a worldwide audience. More RISC-V engineers can gain the knowledge they need to become productive quickly while expanding the pool of talented people.

Blog

Welcoming RISC-V International Board Members

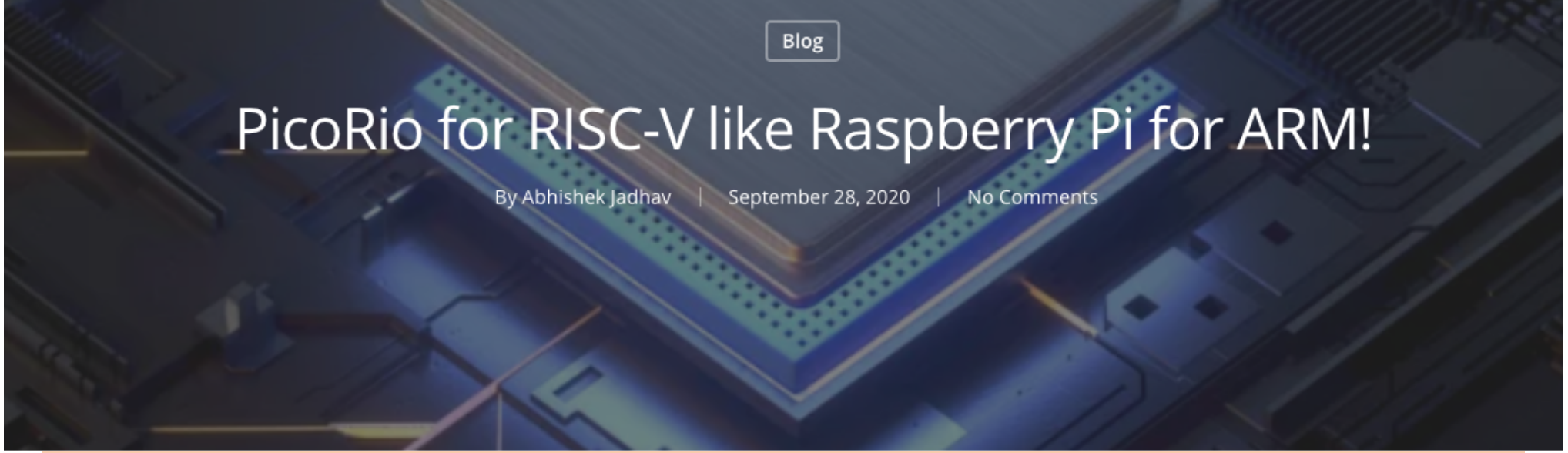
By Jeffrey Osier-Mixon | August 4, 2020 | No Comments

中科院计算所包云岗教授进入了BoD。
现在 RVI BoD 超过一半董事能听懂和说中文了。

个人竞选者 Wei Wu 输给了 Stefan Wallentowitz（

By Calista Redmond, August 3, 2020

The RISC-V community has grown and matured rapidly in the 10 years since RISC-V inception, and in our 5 year history as an organization. We've progressed together through **technology**, **opportunity**, and **community**. RISC-V has become a **disruptive technology**, spurred unprecedented semiconductor innovation, and demonstrated there is a simpler and modular way of building a chip. The **unconstrained opportunity** achieved by bringing together the global community with a range of domain expertise from many different industries drives this exponential growth. The RISC-V **community is engaged** with members from companies of all sizes, in geographies around the world, and expertise in the critical areas needed for a healthy ecosystem.



必须也必然会出现一个类似树莓派的RV生态成员。

HiFive Unleashed 超过1w且无货；FGPA大板子三万。
需要一个 1000 人民币以内可以跑Ubuntu的RV机器

Parameters	PicoRio	Raspberry Pi
Instruction Set	RISC-V	ARM

有哪些新的机会？

- 编译器（GCC、LLVM）二进制（Binutils）模拟器（QEMU）缺人
  - 导致了ISA的部分TG推进缓慢，缺少必要的资源
- 几乎所有需要JIT的软件都还没有得到有效的支持
- 即使功能性支持了，速度目前都还没有开始进行优化。100x 目标
- 即将成立 Code Speed Opt SIG
- 即将成立大量的 Software xxx SIG/TG 和 vertical SIGs

近期RISC-V基金会的动向以及参与的机会

感谢 & 提问

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