

RISC-V LLVM在过去一年进展

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LLVM小队成员简介

- 员工，现有4人
- 参与实习的同学
 - 新同学，3人
 - 现有，6人
 - LV2+ -> LV4

2022年回顾

- 完成2021年布局项目

- K扩展 - 汇编器, intrinsic
- Zfinx - 汇编器
- Zmmul

- 继续维护

- Zc*扩展
- Zfinx - codegen
- JITLink

- 更多的参与

- review代码
- 解决issue

- 仍需努力💪

- RVV

- 新增方向: <https://github.com/llvm/llvm-project>

- RISC-V子扩展
 - Zhintpause
 - Zhintntl
 - zfh, zfhmin
 - Zbpbo

- 标量优化
- LLDB
- flang

- gollvm: <https://go.googlesource.com/gollvm/>

- 支持香山处理器: <https://github.com/plctlab/llvm-project/tree/xiangshan>

- P扩展: <https://github.com/plctlab/llvm-project/tree/p-extension-andes-v1>

2023年工作内容

- Upstream, <https://github.com/llvm/llvm-project>
 - Z*inx
 - Zca,Zcb,Zcf,Zcd,Zcmp
 - 香山 - 处理器定义
 - riscv .option arch
 - XCV* - 汇编器
 - lldb - RV64F,RV32FC,D,rvv register
 - flang
 - 中端/后端标量优化
 - RVV向量优化
 - tsan

2023年工作内容

LLDB(RV64F,RV32FC,D)
InstCombine,CVP,SCCP,
LoopFusion,MemorySSA
RISC-V Codegen
Flang
Zca, Zcb

ValueTracking,InstCombine,CVP,
SCCP,LoopIdiom,
CodeGenPrepare, ConstraintElim,
MemoryDependencyAnalysis
Flang,Openmp
XCVbi,XCVsimd,XCValu
RVV RISC-V Codegen

1月- 3月

4月- 6月

7月- 9月

10月- 12月

lldb (rvv register)
SimplifyCFG, InstCombine ,
ValueTracking, LVI,
InstSimplify,LoopIdiom,Local
Z*inx
Zcmt,Zcmp
RISC-V Codegen
RISC-V.option arch

ConstantRange,InstComb
ine,ValueTracking,SCCP,
CVP,CodeGenPrepare
Flang
RVV RISC-V Codegen
香山
XCVmem,XCVelw
tsan

详见 : <https://github.com/plctlab/PLCT-Weekly>

2023年工作内容

- xtheadvector 的支持 , <https://github.com/ruyisdk/llvm-project>
 - 完成了汇编器支持
 - 大部分intrinsic支持
 - 第一个大佬评论 , <https://github.com/ruyisdk/llvm-project/pull/30#issuecomment-1835712978>
 - 第一个来自社区伙伴的pr , <https://github.com/ruyisdk/llvm-project/pull/35>

cmuellner commented 2 weeks ago

...

Oh, wow! I did not know that there is an LLVM implementation for XThreadVector.
Thanks for working on this!

I haven't looked into the details here, but XThreadVector support has a few small differences to RVV 0.7.1.

We've listed them in the specification: <https://github.com/T-head-Semi/thead-extension-spec/blob/master/xthead>

fix build by changing enum definition #35



Merged

ChunyuLiao merged 1 commit into [ruiysdk:xtheadvector](#) from [joennlae:fix-build](#) last week

Conversation 2

Commits 1

Checks 2

Files changed 1



joennlae commented last week

First of all, thank you for including the `xtheadvector` into llvm :-)

I tried to build it from scratch, and I got this error. The build works with the proposed fix.


```
/home/janniss/Documents/llvm-project/clang/utils/TableGen/TableGenBackends.h:32:20: error: found
32 | enum RVVHeaderType : uint8_t { RVV, XTHEADV_VECTOR };
    |
```

2023年工作内容

- Corev-llvm, <https://github.com/openhwgroup/corev-llvm-project>
 - 至少持续一年，没有活跃开发者
 - corev-llvm-project的intrinsic开发
 - 完成了upstream的MC开发
 - 吸引了来自全球不同公司的伙伴参与开发/测试

[RISC-V][Clang] Added code to generate clang error if immediate op

 Open adeel10x wants to merge 3 commits into [openhwgroup:development](#) from [10x-Engineers:Add-clang-check-for-simd-insert-](#)

 Conversation 7  Commits 3  Checks 0  Files changed 2



adeel10x commented 4 days ago

First-time contributor

...d of the following builtins is out of range:

CORE-V Hardware Loop Codegen Issues #86

 Open

PhilippvK opened this issue on Oct 30 · 3 comments



PhilippvK commented on Oct 30

Contributor



Jeremy Bennett 4:15 AM

 1 Jump

Some of the CORE-V Clang/LLVM team got to meet in person for the first time at [EuroLLVM 2023](#). From left-to-right, [@Charlie Keaney](#), [@Chunyu Liao](#), [@Jeremy Bennett](#) and Lewis Revill. Charlie will be presenting a talk on the joint work between Embecosm and PLCT to add support for CV32E40Pv2 tomorrow at 12:00 UK time. I'll post a link to the video later when it is available.



2023年工作内容

- 针对RISCV的优化实例

- a. [RISCV] Fold (select setcc, setcc, setcc) into and/or instructions
<https://reviews.llvm.org/D150286>
- b. [RISCV] Custom lower vector llvm.is.fpclass to vfclass.v <https://reviews.llvm.org/D151176>
- c. [SDAG][RISCV] Avoid expanding is-power-of-2 pattern on riscv32/64 with zbb
<https://reviews.llvm.org/D158673>
- d. [CodeGenPrepare][RISCV] Remove asserting VH references before erasing the dead GEP
<https://reviews.llvm.org/D153194>
- e. [CVP] Infer nneg on existing zext <https://github.com/llvm/llvm-project/pull/72052>

2023年工作内容

- 建立了回归测试CI, <https://lnt.rvperf.org>, <https://github.com/dtcxzyw/llvm-ci>
 - 886个 regression
 - 帮忙社区大佬测试pr, 第一次被大佬寻求帮忙测试<https://github.com/llvm/llvm-project/pull/73662#issuecomment-1841104665>

Size Regressions Report March 10th 2023, 2:39:25 am #8

New issue

 Closed  github-actions bot opened this issue on Mar 10 · 3 comments



github-actions bot commented on Mar 10

Metadata

- Workflow URL: <https://github.com/dtcxzyw/llvm-ci/actions/runs/4380744164>

Change Logs

from c417266db506c2e000931c1f7a78e81879135c0d to 7c2a3573b696afec91ca6345470dd9b09c4d41

[7c2a3573b696afec91ca6345470dd9b09c4d41](#) [Codegen][NFC] Replace 'RegisterRegAlloc::FunctionPassCtor' with 'RegisterRegAllocBase<T>::FunctionPassCtor'.
[7e9293572d332b812eb1e521f0a75a4e7034abbf](#) [RISCV] Set how many bytes load from or store to stack slot
[865fb2e44011c60d6d69154d205b55f4b44ff10b](#) [RISCV] Pre-commit test case for D140460
[bb01b9919fdd3d5f1b5d78dcb2aa502588618369](#) [ConstraintElimination] Fix UB after D145677
[882fba9ff275f724a998facba12ad8fc22ab54a3](#) [libc++] [ranges] Implement LWG-3865 Sorting a range of pairs




Regressions

Name	Baseline MD5	Current MD5
MultiSource/Applications/ClamAV/clamscan	944b300506413b8c42b64f1ba54d4225	d8c1c48cd2769d4736fcdc2b2!

Assignees

No one assigned

Labels

Projects

None yet

Milestone

No milestone

Development

No branches or pull requests

Notifications

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nikic commented last week

Rebased over the SCEV change. @dtcxzyw Can you please give it another try?



2023年工作内容

- 还有很多在review中的pr
- rv64ilp32
- flang , <https://github.com/sihuan/llvm-work/tree/master/spec2017>

2024年计划

- 继续完善现有项目
 - xtheadvector
 - zcmt
 - 香山
 - XCV*
 - flang
 - . . .
- 继续提升RISCV
 - 标量/向量
 - 中端/后端
- 更多测试，关注更多社区

致谢

- 感谢小伙伴们
- 感谢社区大佬帮忙review
- 感谢社区伙伴帮忙bug fix

- 欢迎交流，指正，许愿~