# Embedded Systems (ECE340) Project 1

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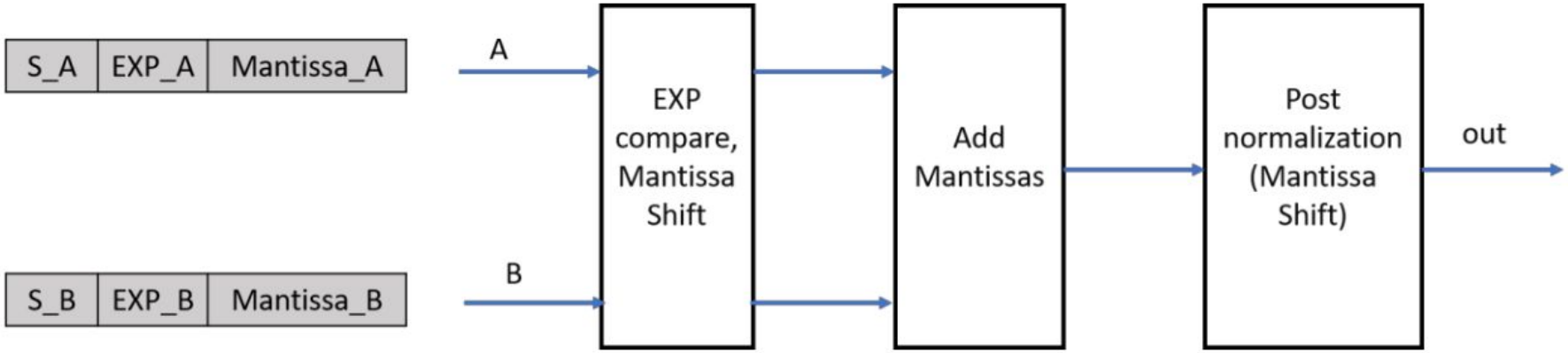
(3531 & 3796)

# Step 1: Design



# Step 1: Example

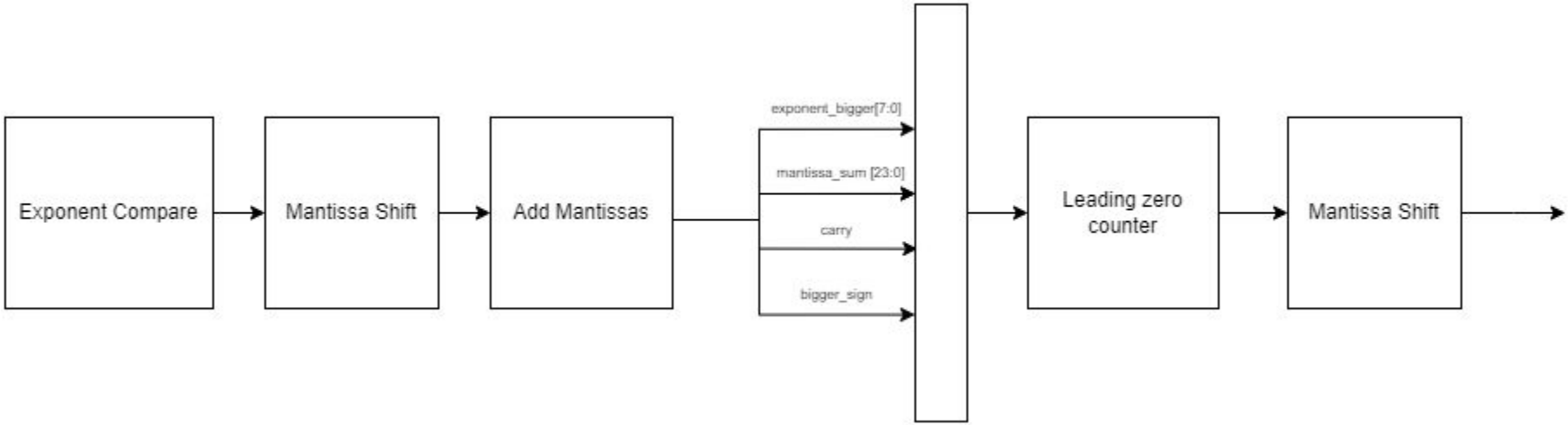
A: 1 10000101 10111101000000000000000 (−111.25)
B: 0 10001010 00101010101111000000000 (2389.875)

expA - expB = 138−133 = 5 (0 αν η διαφορά ≥24)
mantissa A >> 5 = 00001101111010000000000

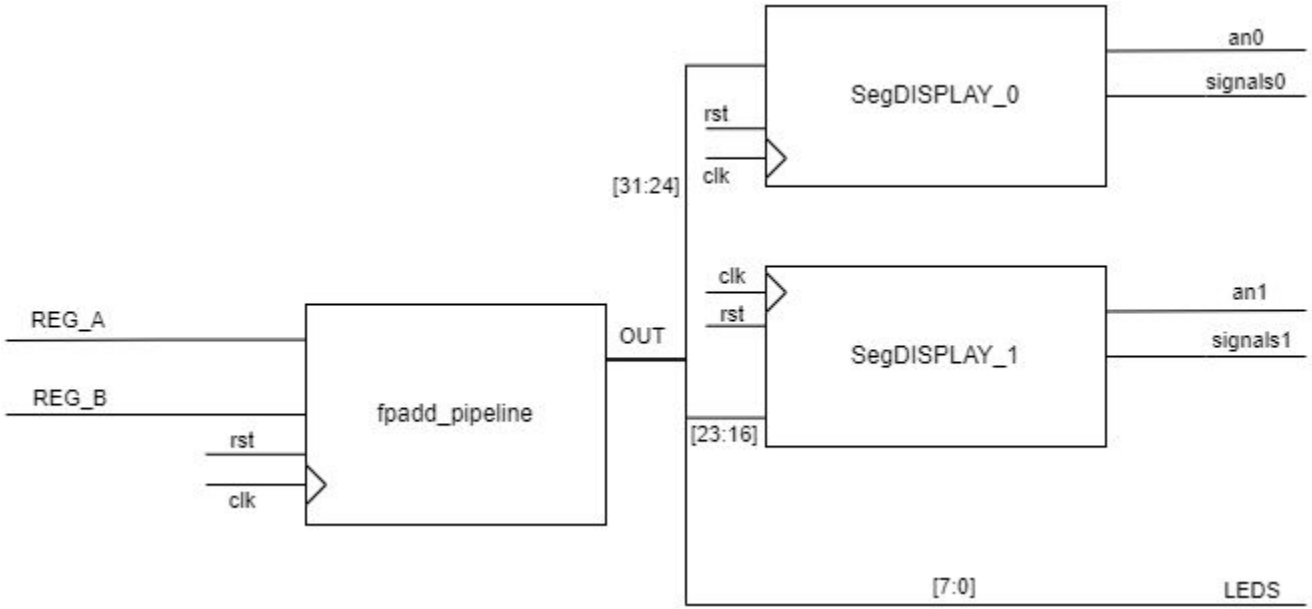
mantissa A + mantissa B = 0.0000110111101 + 1.00101010101111
= 1.00111000101001000000000

A + B = 0 10001010 00011100110101000000000 = 2278.625

# Step 2: Pipelined Design



# Step 3: Top diagram



# Step 3: Seven Segment Displays connections

**Table 16 - Pmod Connections**

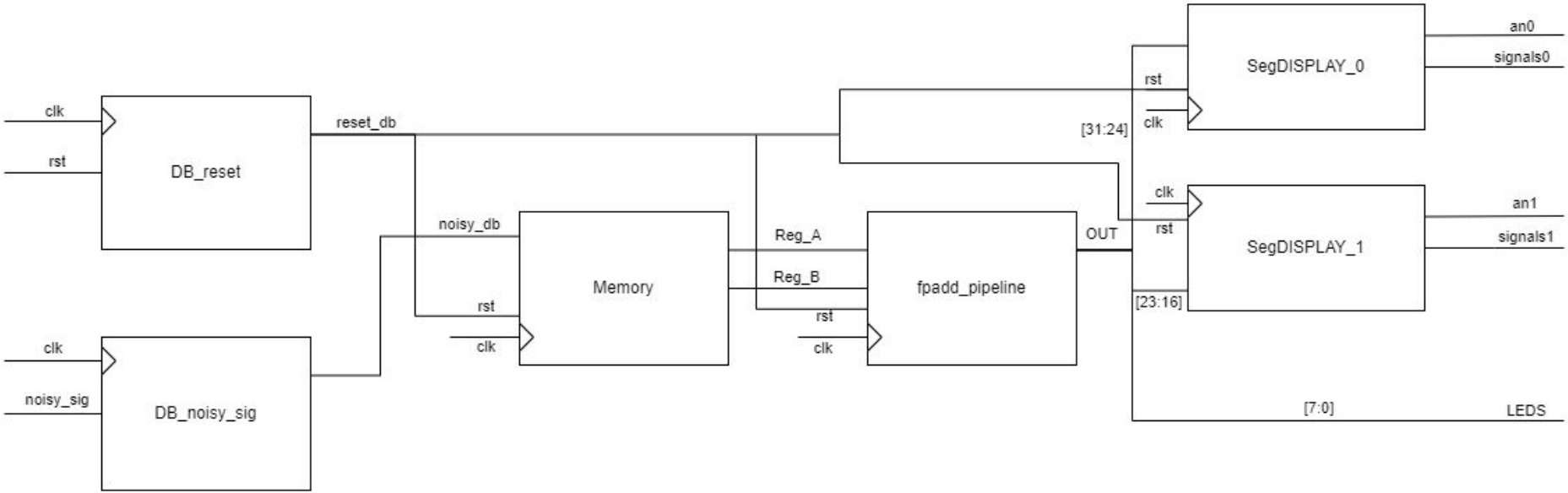
| Pmod | Signal Name | Zynq pin | Pmod | Signal Name | Zynq pin |
|---|---|---|---|---|---|
| JA1 | JA1 | Y11 | JB1 | JB1 | W12 |
| | JA2 | AA11 | | JB2 | W11 |
| | JA3 | Y10 | | JB3 | V10 |
| | JA4 | AA9 | | JB4 | W8 |
| | JA7 | AB11 | | JB7 | V12 |
| | JA8 | AB10 | | JB8 | W10 |
| | JA9 | AB9 | | JB9 | V9 |
| | JA10 | AA8 | | JB10 | V8 |

| Pmod | Signal Name | Zynq pin | Pmod | Signal Name | Zynq pin |
|---|---|---|---|---|---|
| JC1 Differential | JC1_N | AB6 | JD1 Differential | JD1_N | W7 |
| | JC1_P | AB7 | | JD1_P | V7 |
| | JC2_N | AA4 | | JD2_N | V4 |
| | JC2_P | Y4 | | JD2_P | V5 |
| | JC3_N | T6 | | JD3_N | W5 |
| | JC3_P | R6 | | JD3_P | W6 |
| | JC4_N | U4 | | JD4_N | U5 |
| | JC4_P | T4 | | JD4_P | U6 |

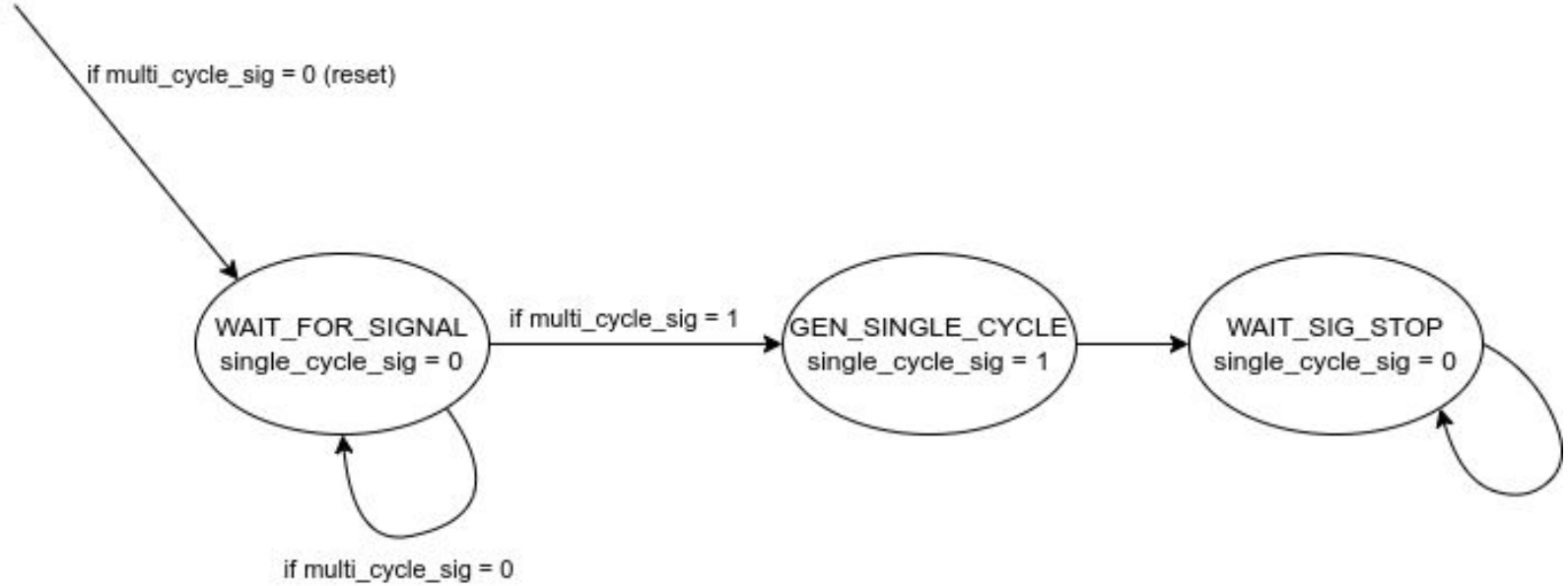
| Pmod | Signal Name | Zynq pin | MIO |
|---|---|---|---|
| JE1 MIO Pmod | JE1 | A6 | MIO13 |
| | JE2 | G7 | MIO10 |
| | JE3 | B4 | MIO11 |
| | JE4 | C5 | MIO12 |
| | JE7 | G6 | MIO0 |
| | JE8 | C4 | MIO9 |
| | JE9 | B6 | MIO14 |
| | JE10 | E6 | MIO15 |

Source: https://files.digilent.com/resources/programmable-logic/zedboard/ZedBoard_HW_UG_v2_2.pdf

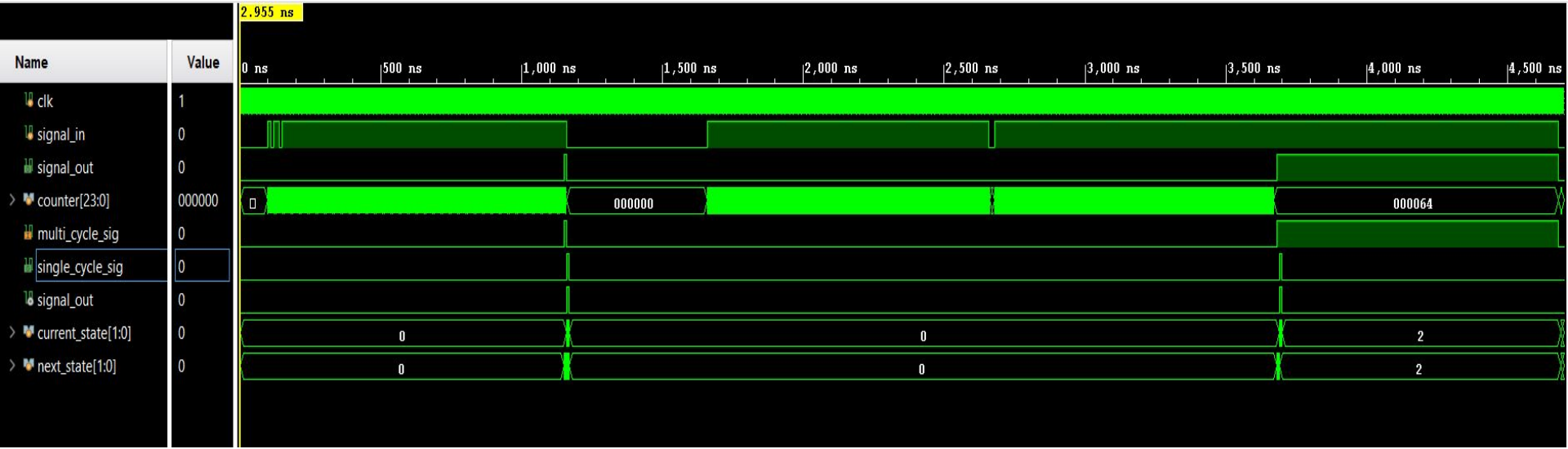
# Step 4: Top diagram



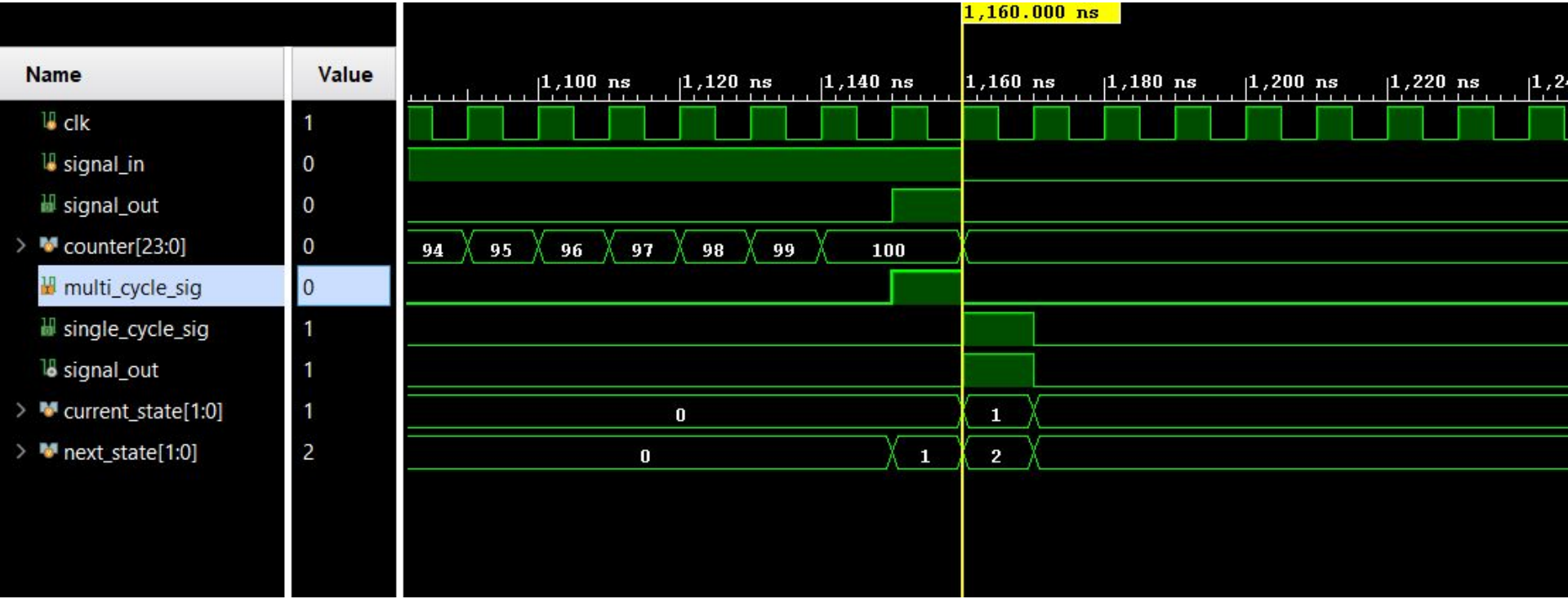
# Step 4: FSM


if multi_cycle_sig = 0 (reset)
WAIT_FOR_SIGNAL
single_cycle_sig = 0
if multi_cycle_sig = 1
GEN_SINGLE_CYCLE
single_cycle_sig = 1
WAIT_SIG_STOP
single_cycle_sig = 0
if multi_cycle_sig = 0

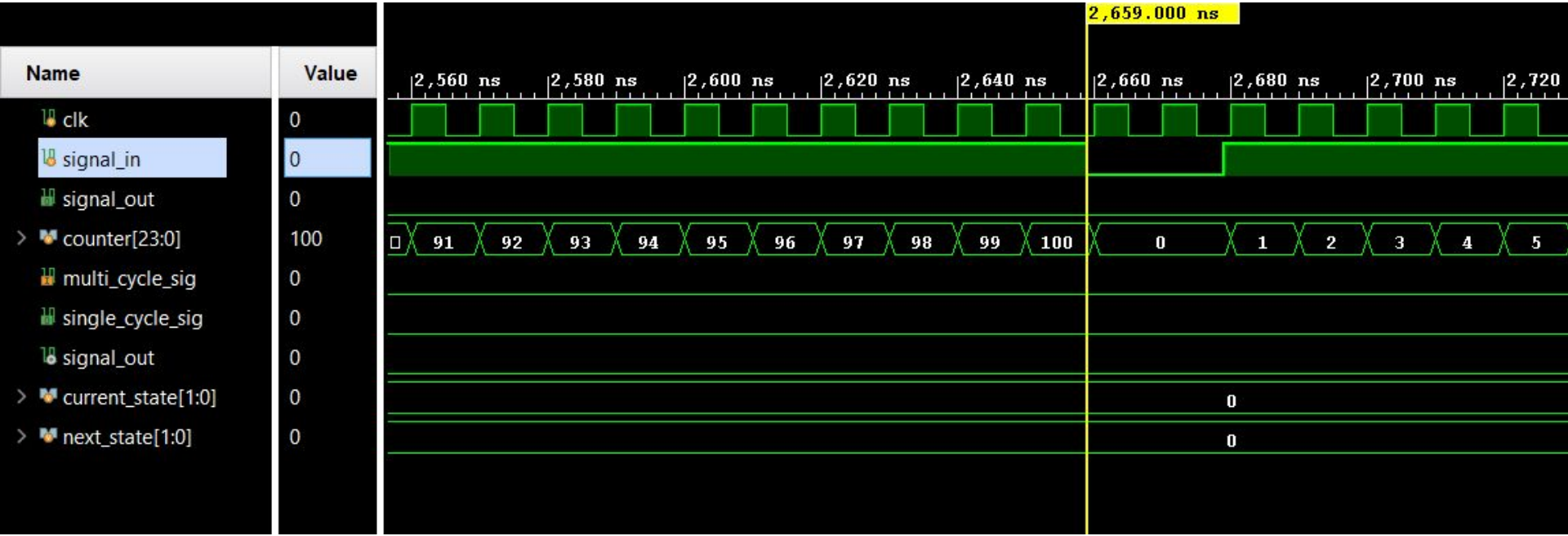
# Step 4: Debounce



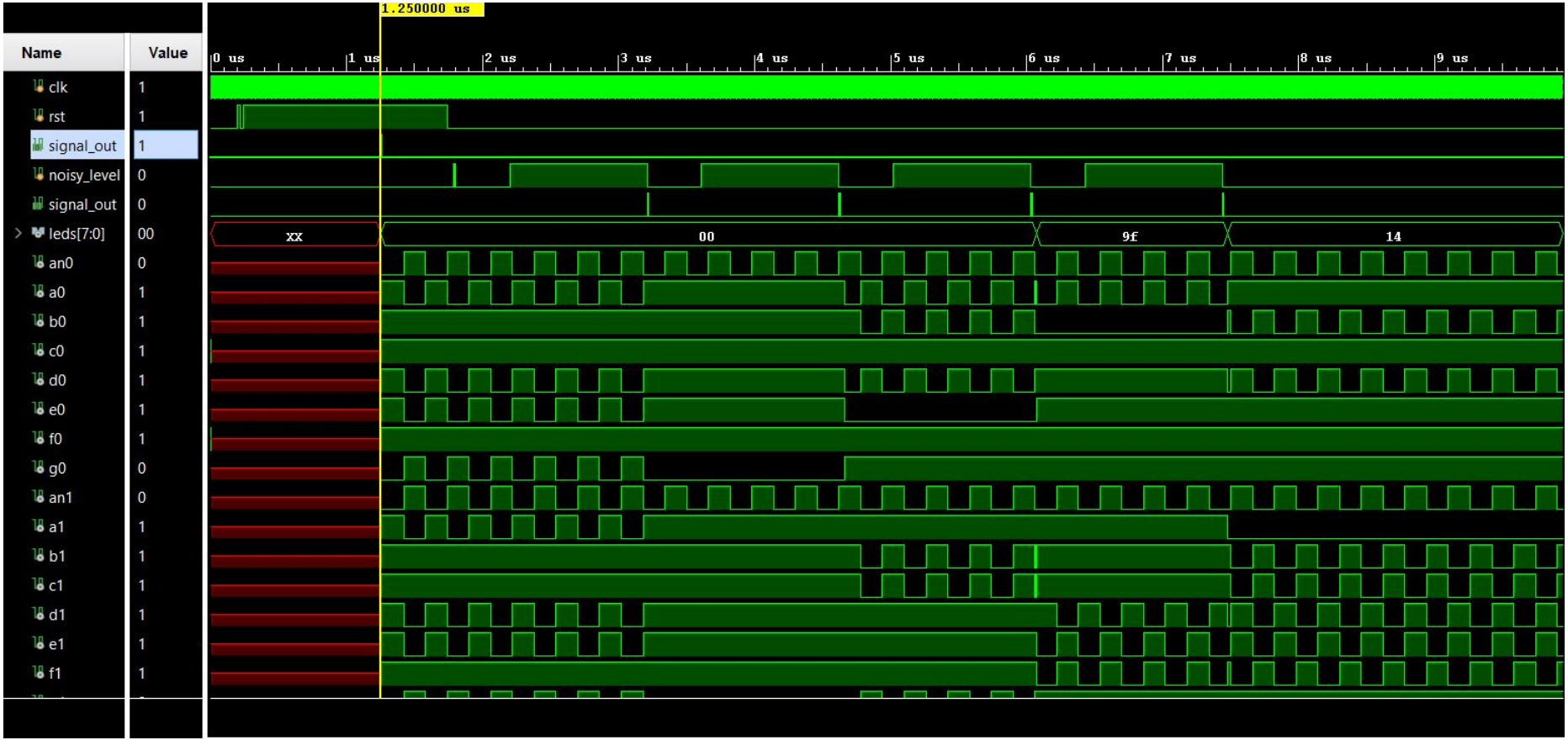
# Step 4: Limit case 1



# Step 4: Limit case 2



# Step 4: behavioral sim



# Step 4: Implementation sim