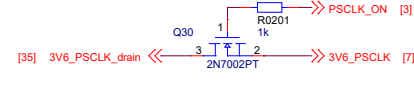
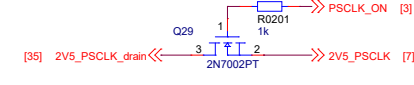
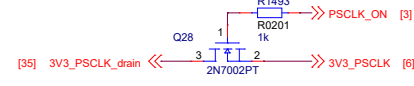
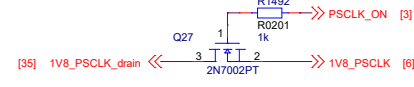
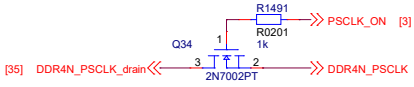
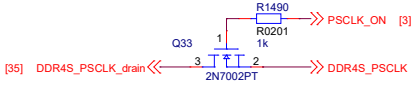
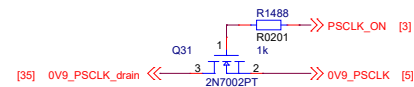
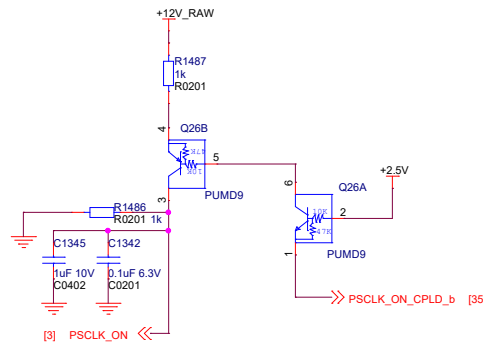
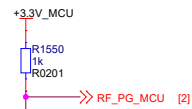
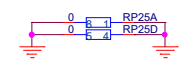
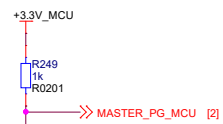
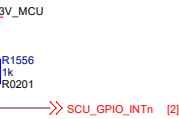
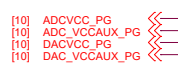
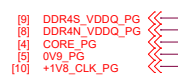
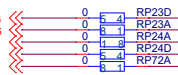
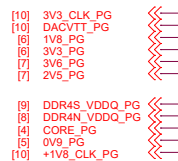
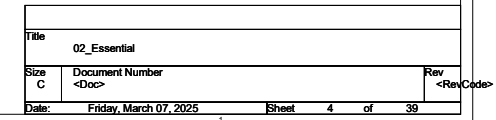


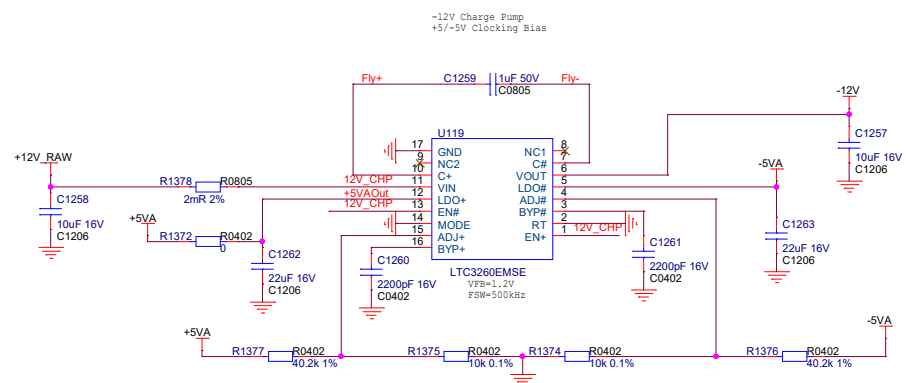
[37] DB0_INTn
[38] DB1_INTn
[39] CLKDB_INTn



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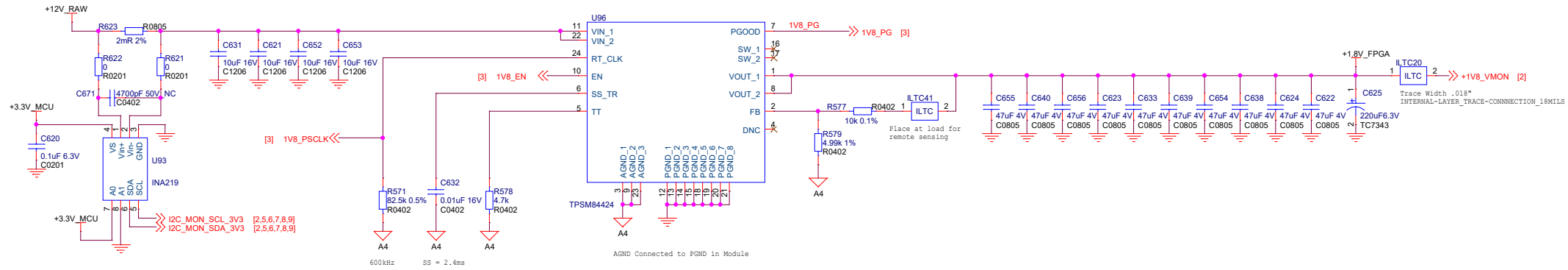
The schematic diagram illustrates the power management section for the TPS846C23MOLR. It features a +12V_RAW input connected to a network of decoupling capacitors (C242, C670, C739, C257, C259, C737, C254, C255, C267, C268, C262) and resistors (R1356, R1357, R257, R258). The U400 controller is connected to various pins including VIN_1, VIN_2, VIN_3, VIN_4, BP6, BP6_RTN, VINBP, BP_RTN, BP3, DATA, CLK, ALERT, CNTL, ADDR1, ADDR0, RT_SEL, and SYNC. The output stage includes a +0V85_CORE_VMON output, a +0.85V input, and a network of capacitors (C265, C764, C765, C264, C695, C763, C229, C658) and resistors (R1361, R0402, C1029). The diagram also shows the connection to the TPS846C23MOLR and the AGND connection to the module.



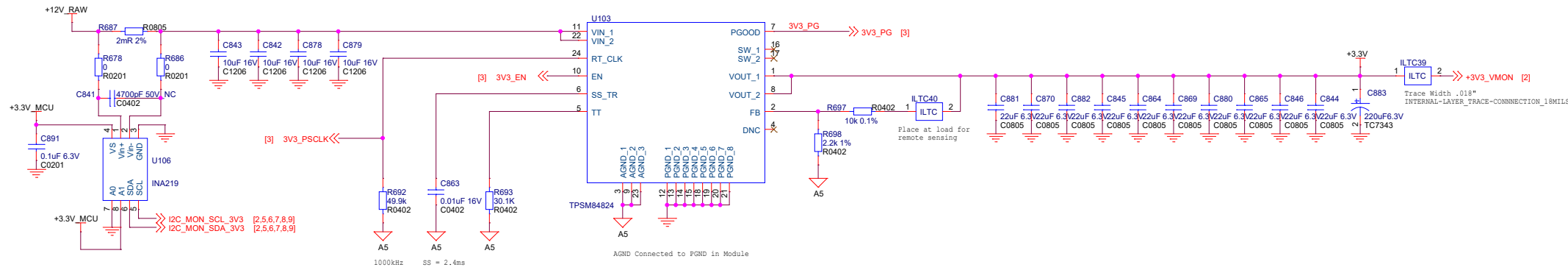


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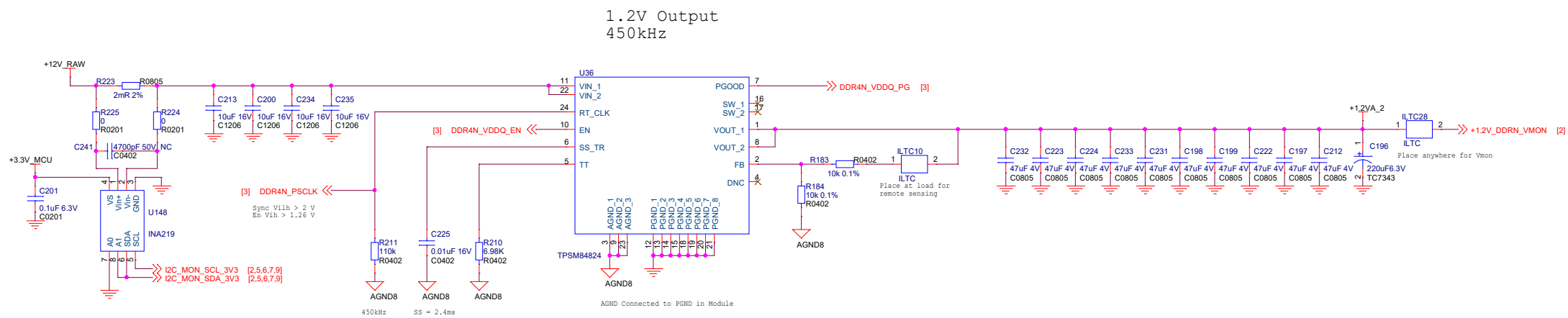
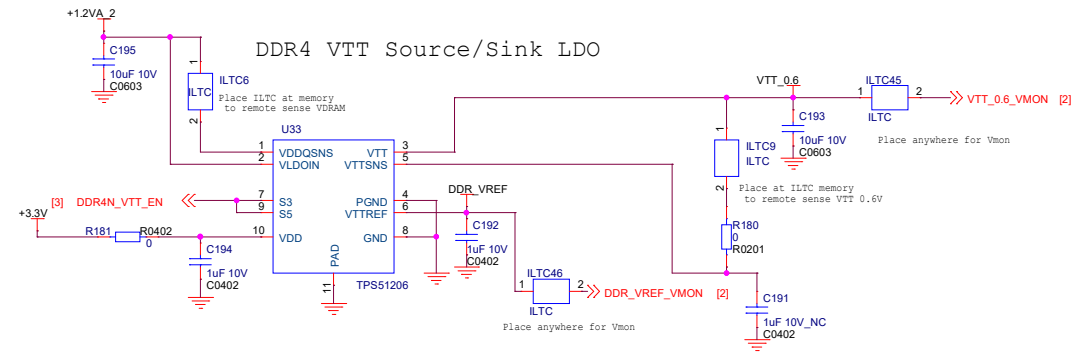
1.8V Output
600kHz



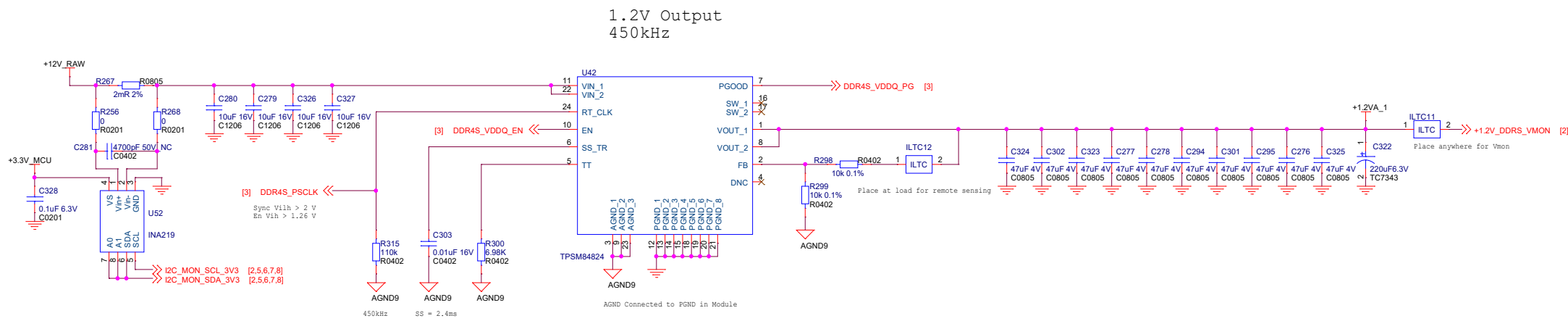
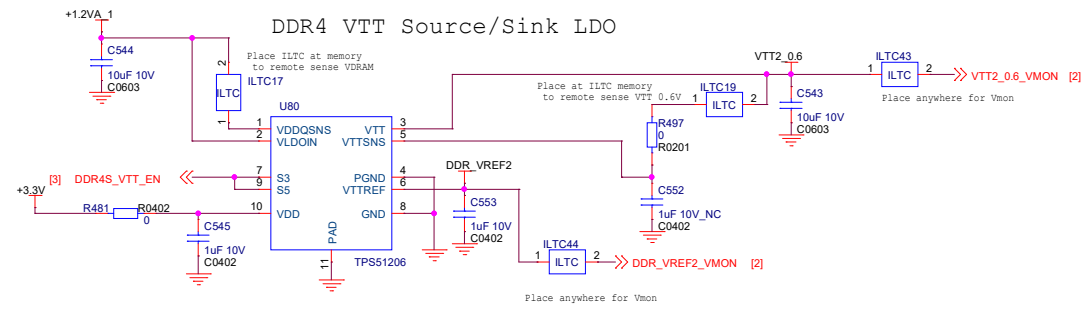
3.3V Output
1000kHz



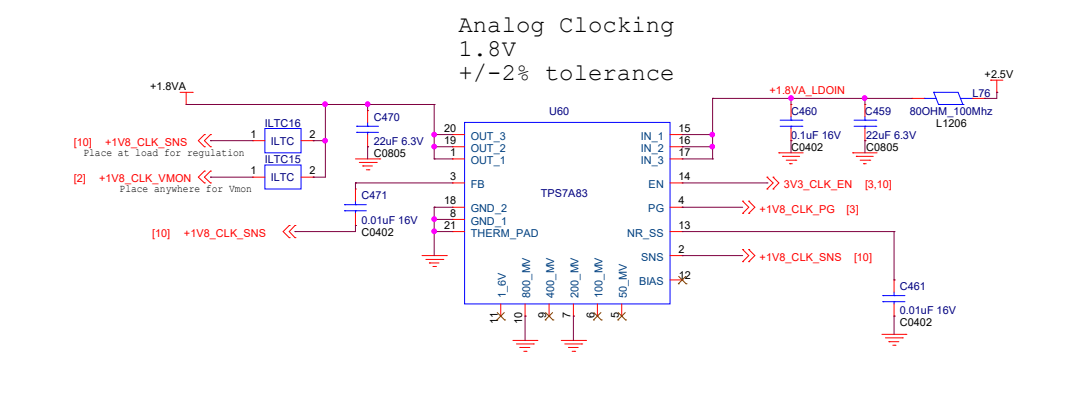
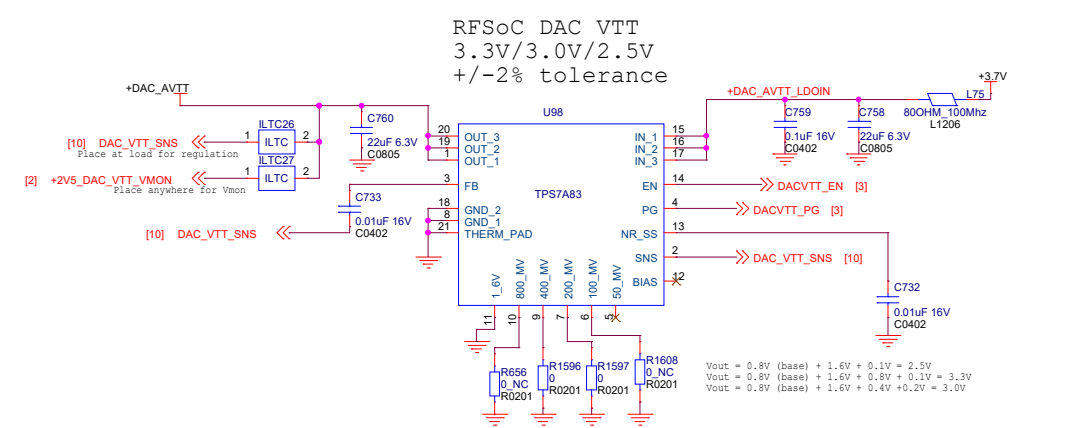
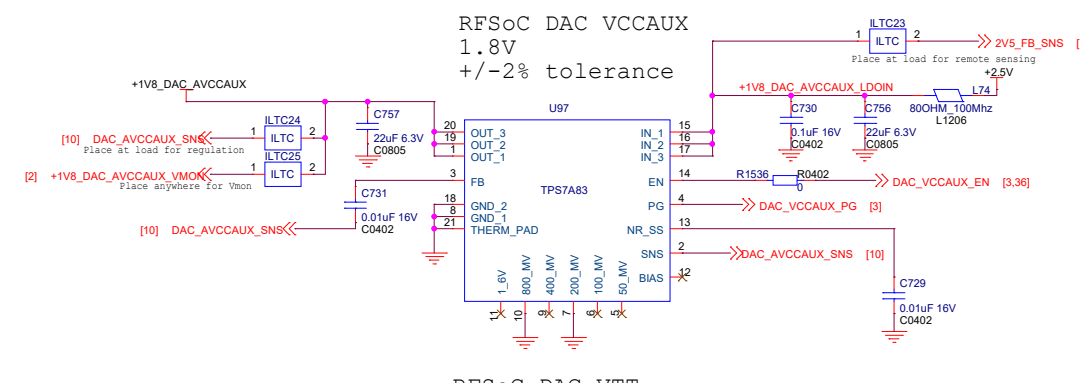
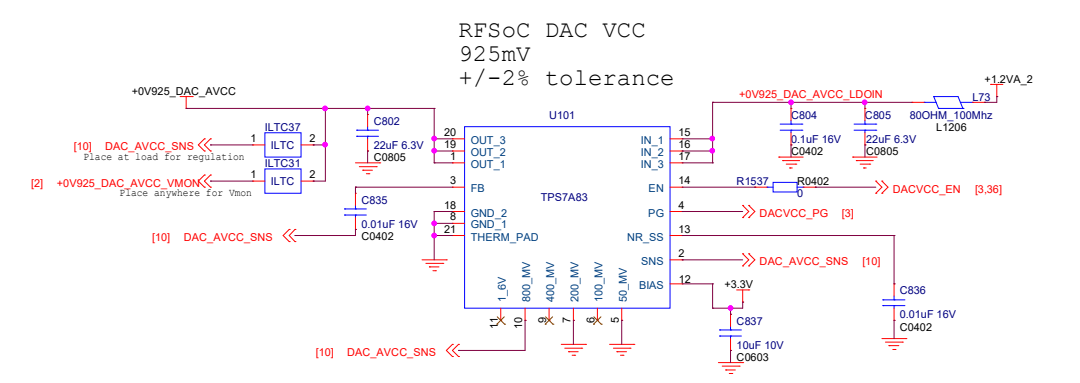
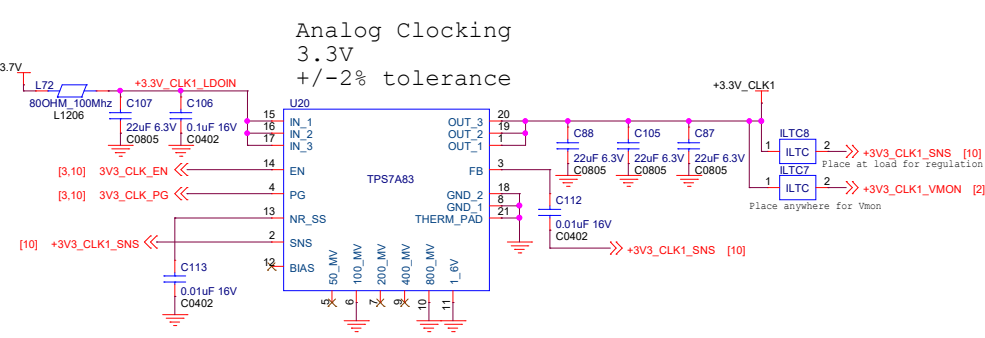
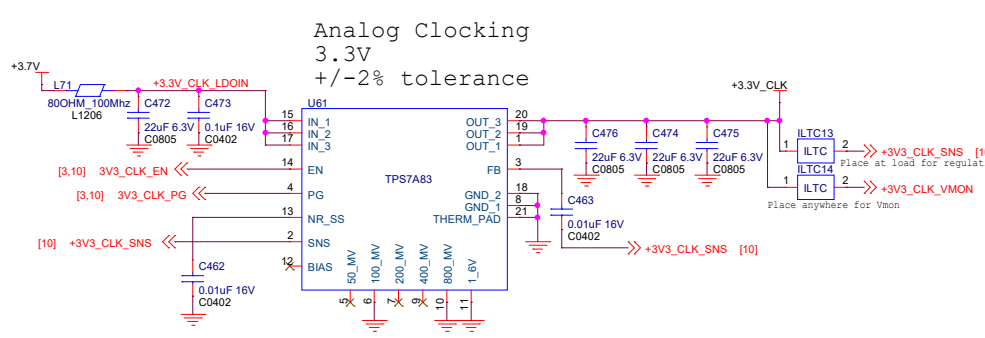
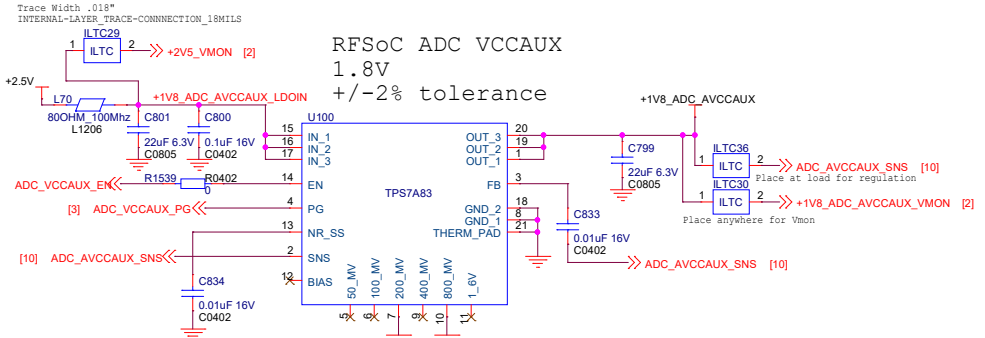
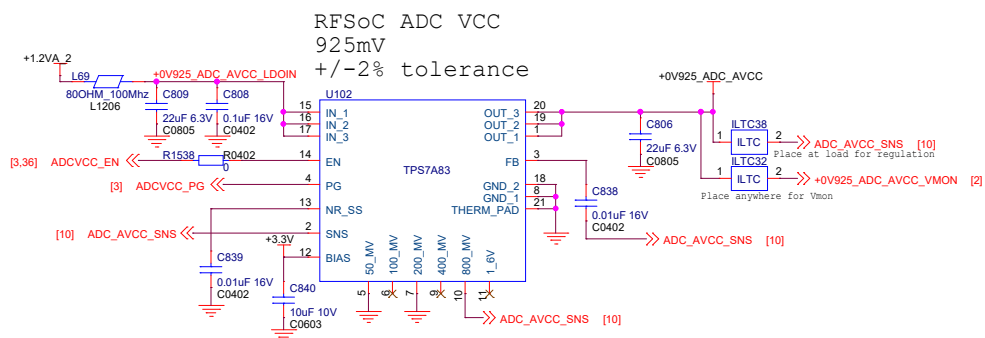
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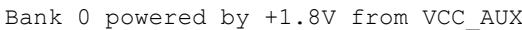


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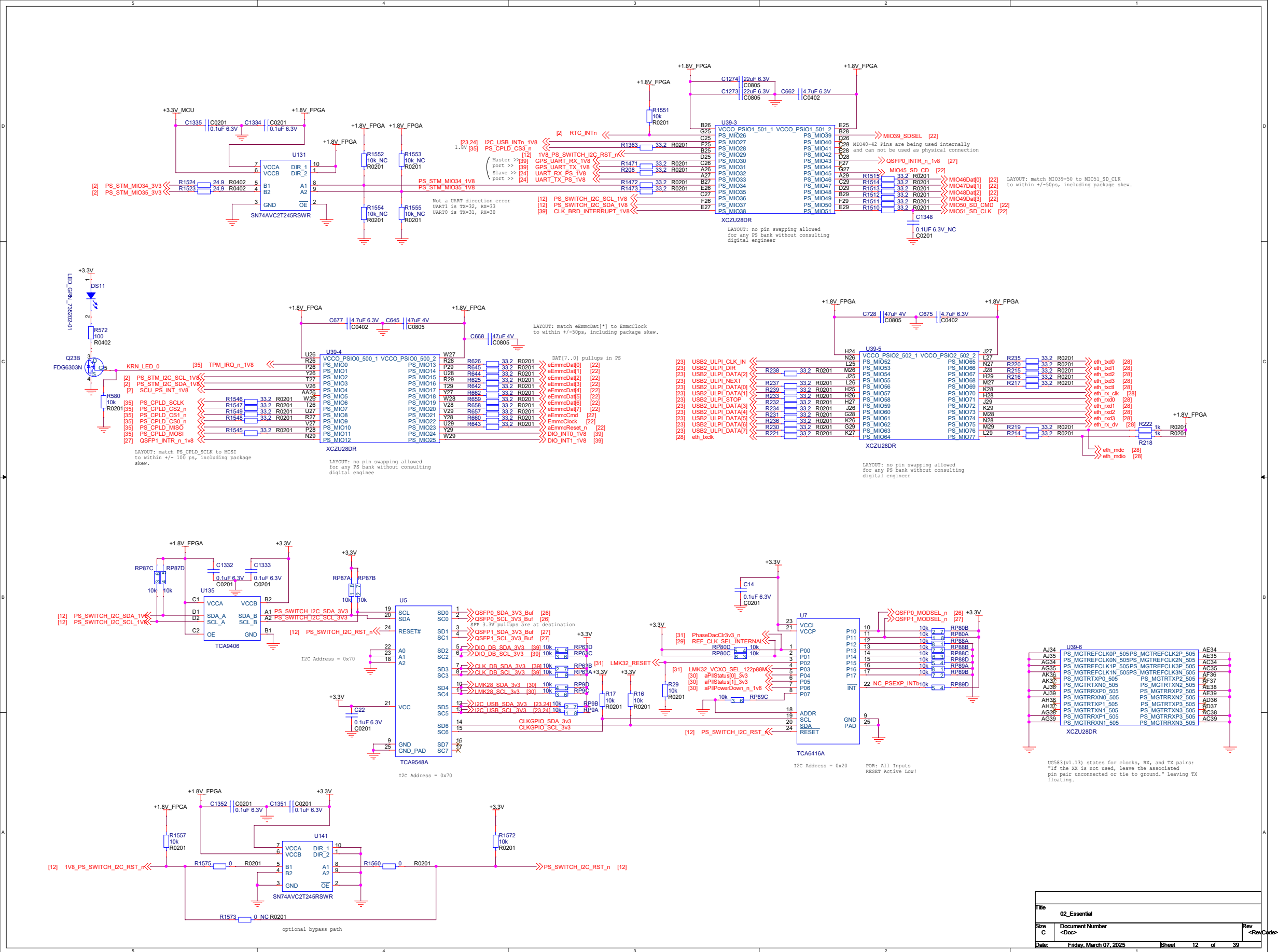


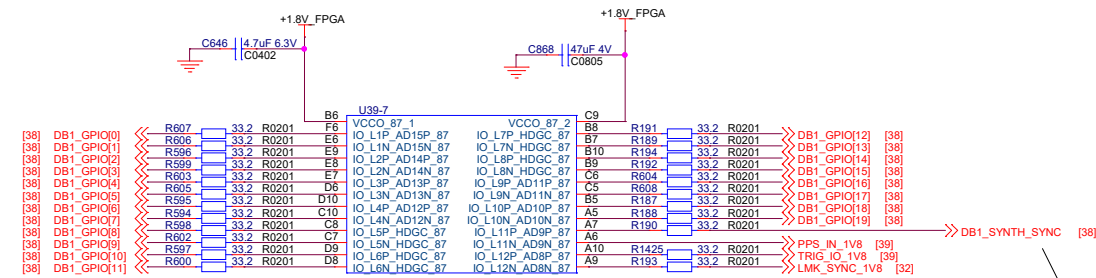
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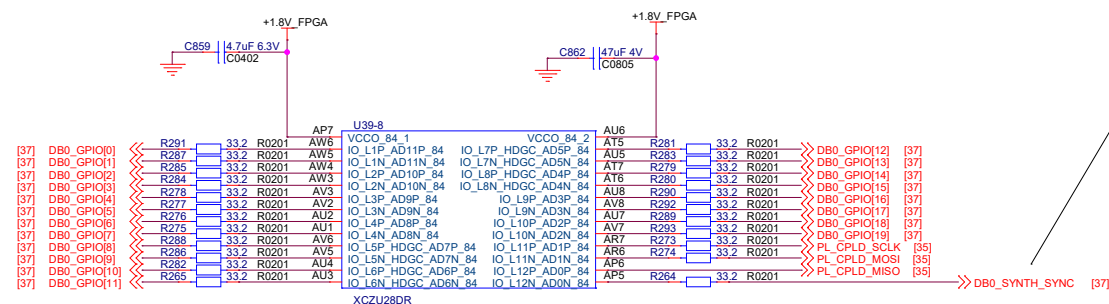


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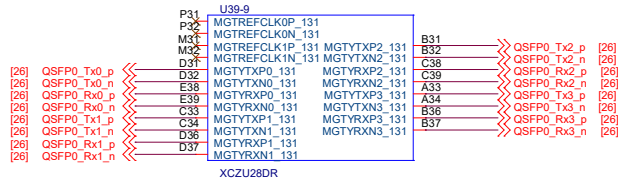
LAYOUT: any HD bank signals may be swapped.
No strict rules apply to any signals here



LAYOUT: DB* SYNTH_SYNC signals should
be length matched within 10th, including package
bond wire lengths

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UG578:
If reference pins are not used,
leave the associated pin pair
unconnected



Quad 131

+2.5V

4.7uF 6.3V

C834

C835

C836

C837

C838

C839

C840

C841

C842

C843

C844

C845

C846

C847

C848

C849

C850

C851

C852

C853

C854

C855

C856

C857

C858

C859

C860

C861

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C864

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C984

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C994

C995

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C997

C998

C999

C1000

C1001

C1002

C1003

C1004

C1005

C1006

C1007

C1008

C1009

C1010

C1011

C1012

C1013

C1014

C1015

C1016

C1017

C1018

C1019

C1020

C1021

C1022

C1023

C1024

C1025

C1026

C1027

C1028

C1029

C1030

C1031

C1032

C1033

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C1098

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C1100

C1101

C1102

C1103

C1104

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C1106

C1107

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C1110

C1111

C1112

C1113

C1114

C1115

C1116

C1117

C1118

C1119

C1120

C1121

C1122

C1123

C1124

C1125

C1126

C1127

C1128

C1129

C1130

C1131

C1132

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C1141

C1142

C1143

C1144

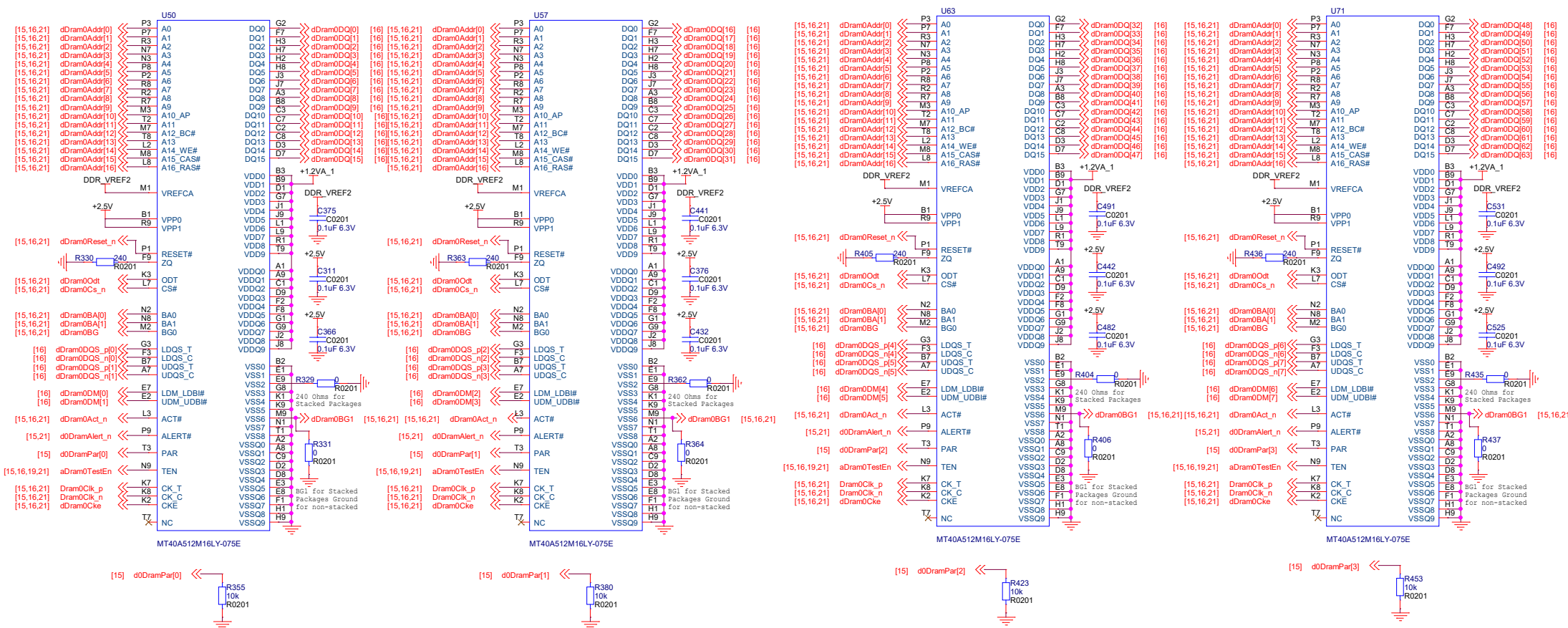
C1145

C1146

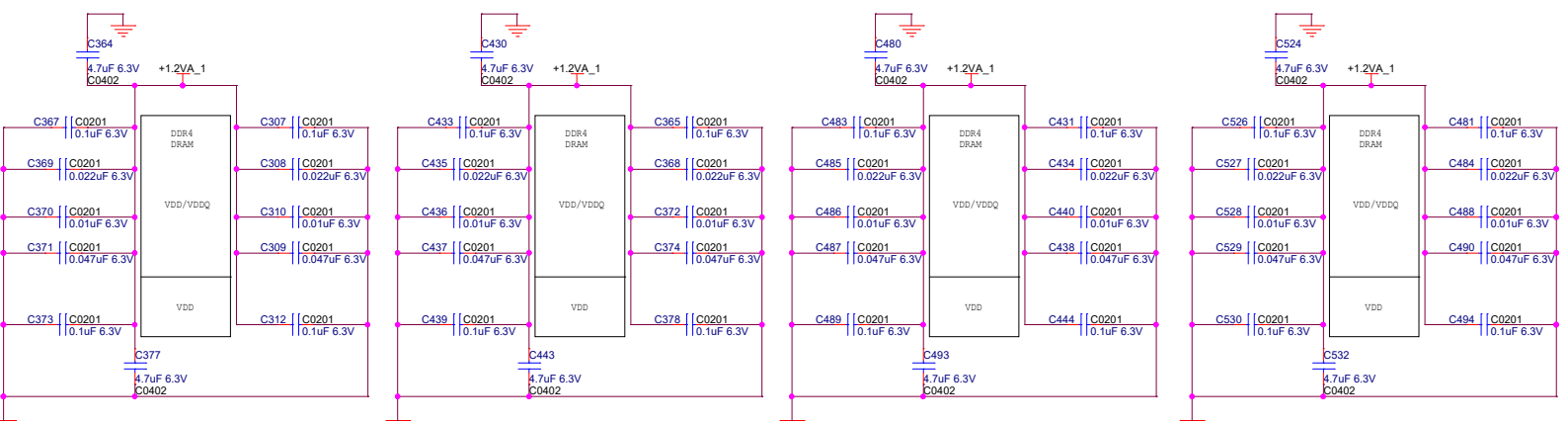
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C1148

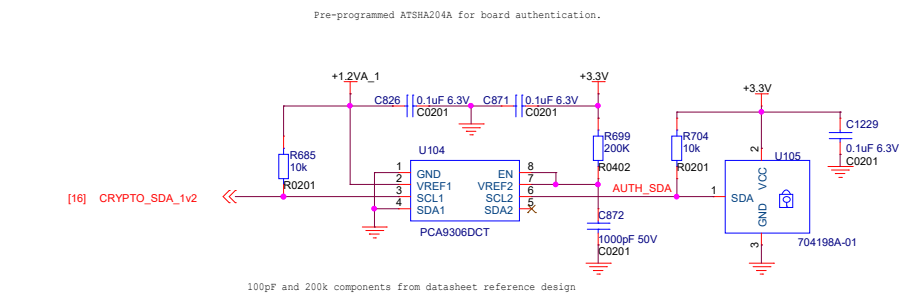
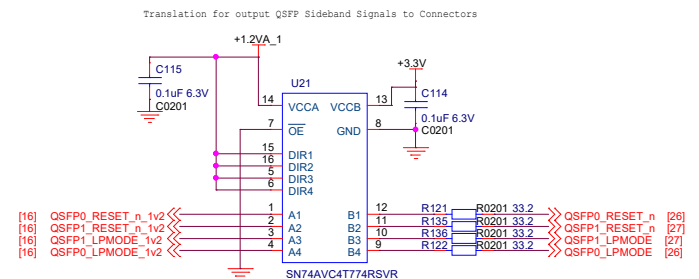
C1149



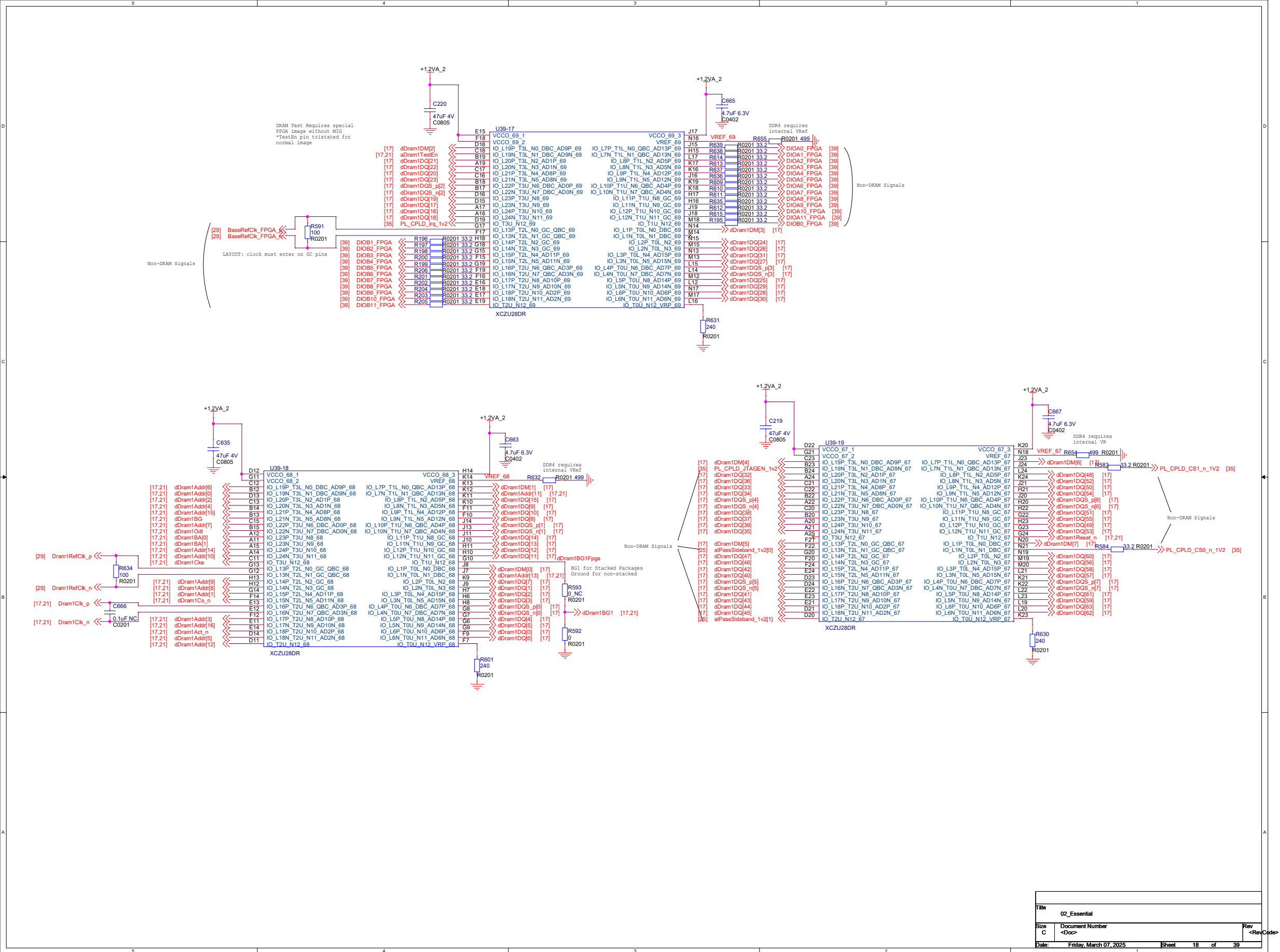
DDR4 Decoupling Cap Placement

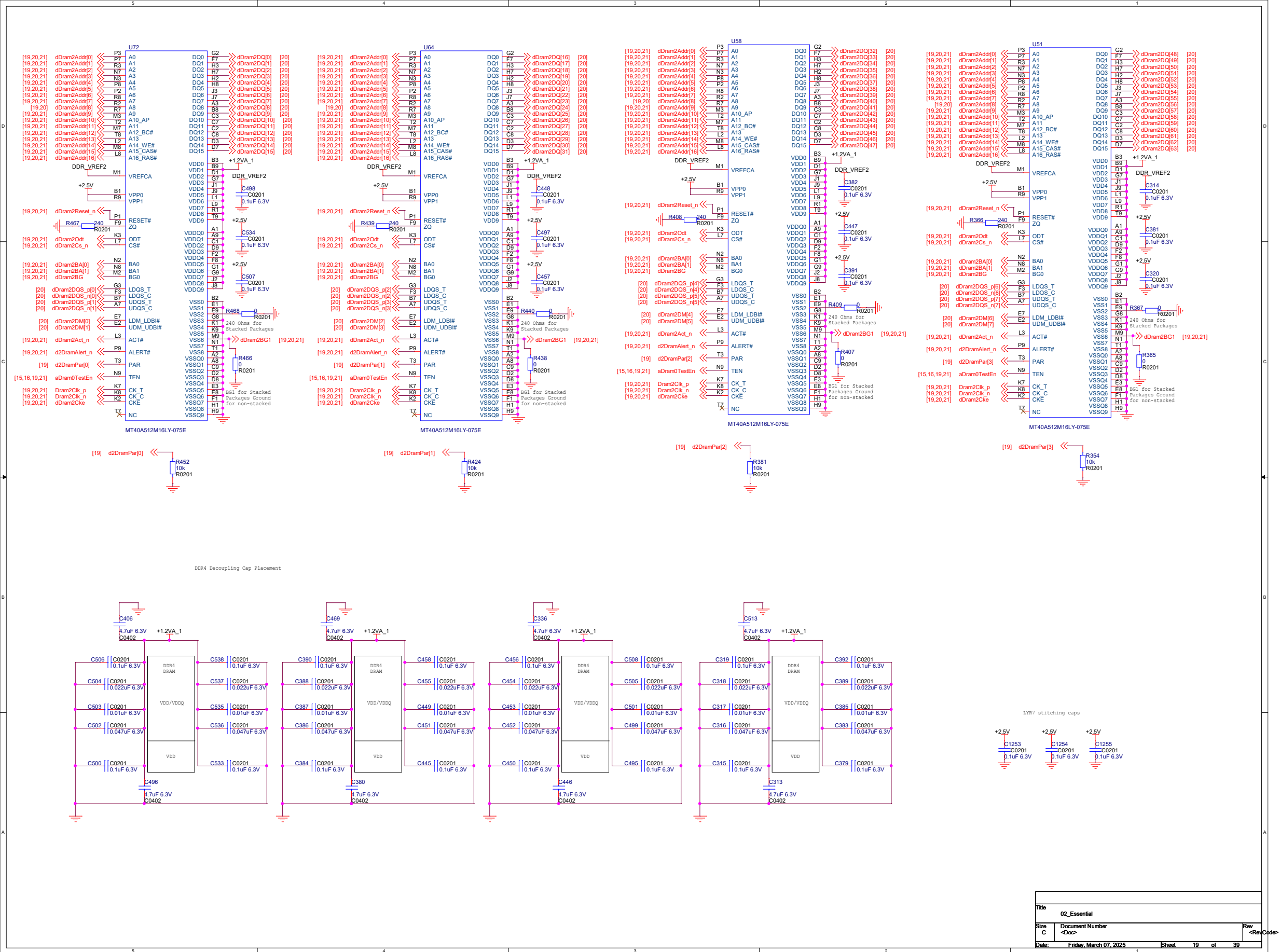


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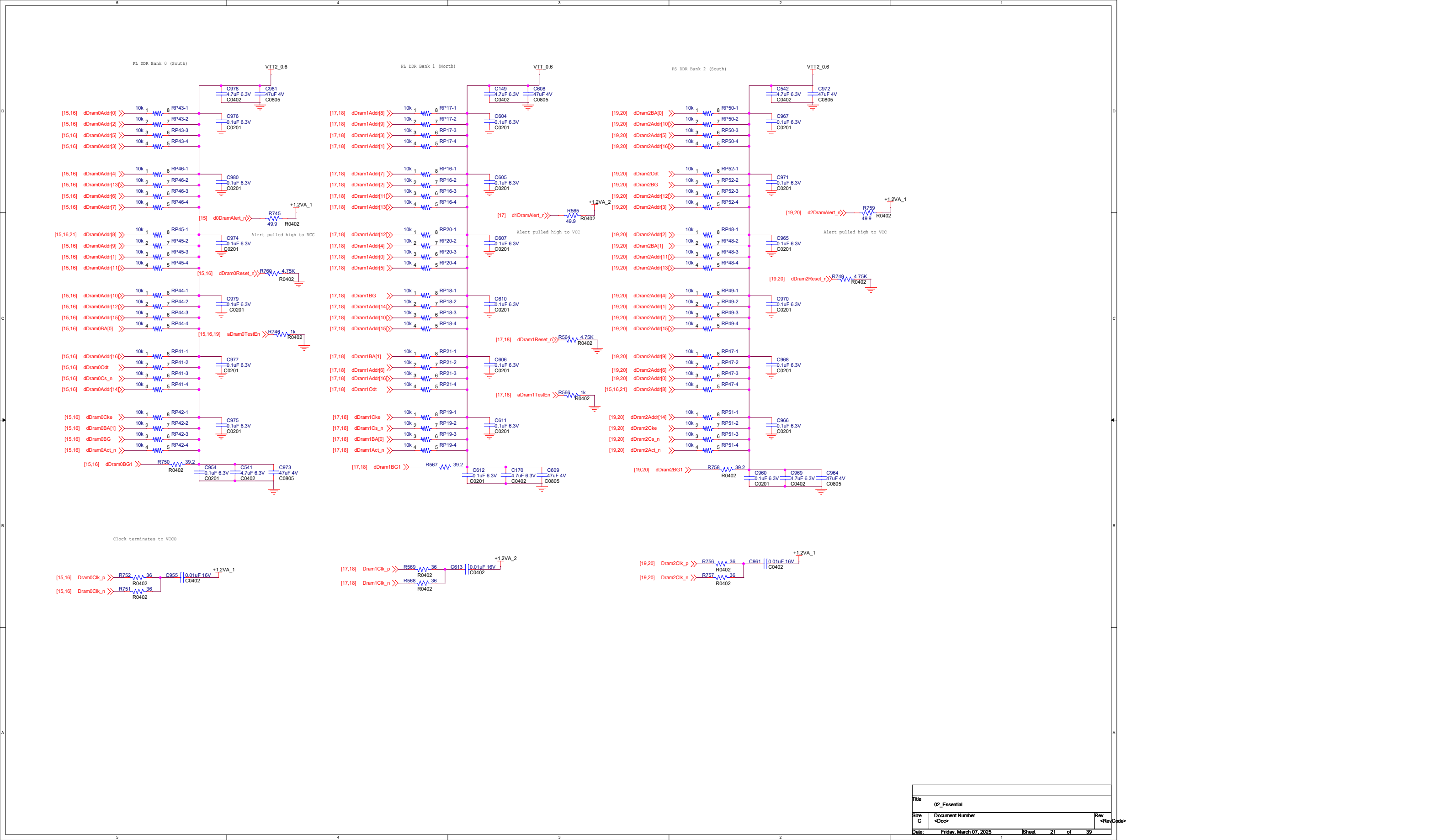


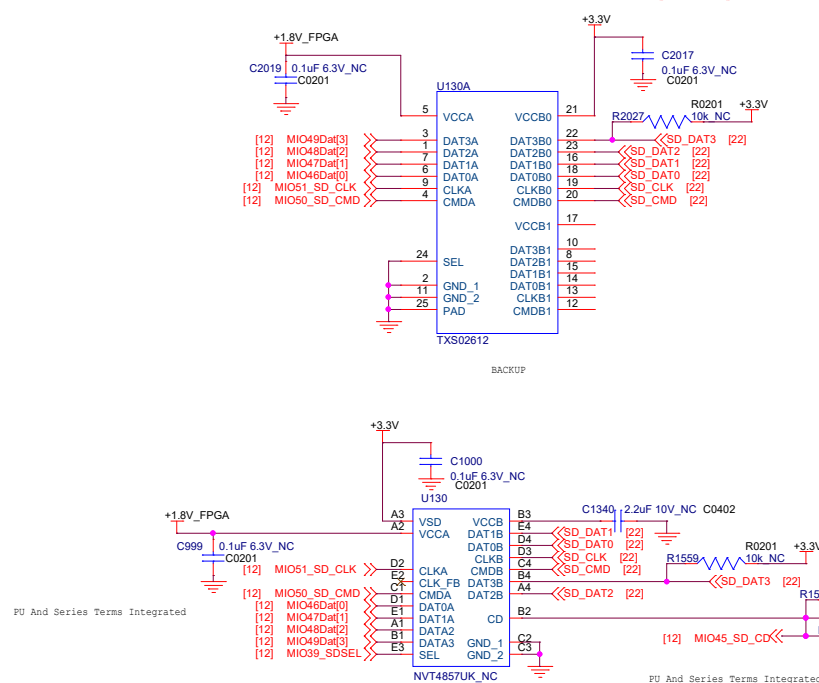
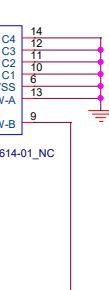
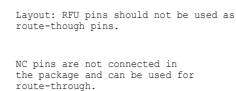




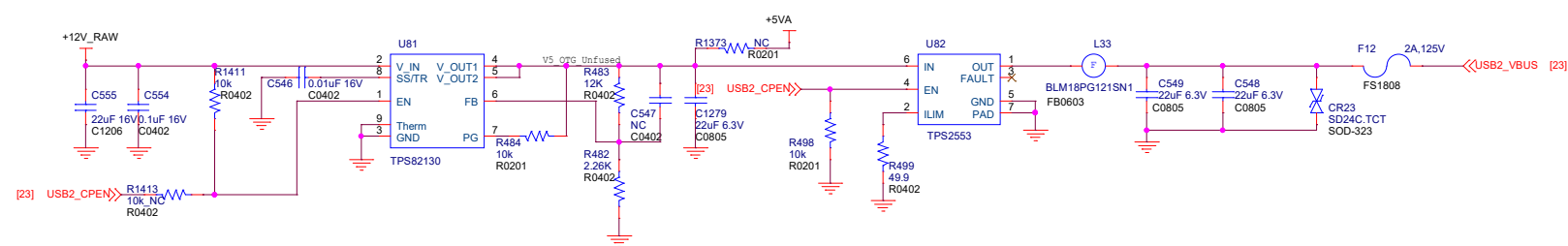
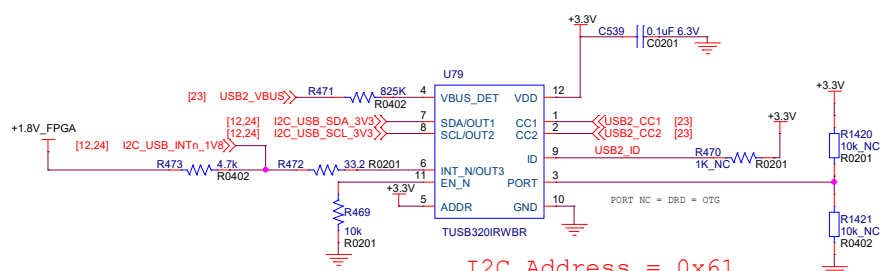
Lane 8 for ECC only,
unused in this design

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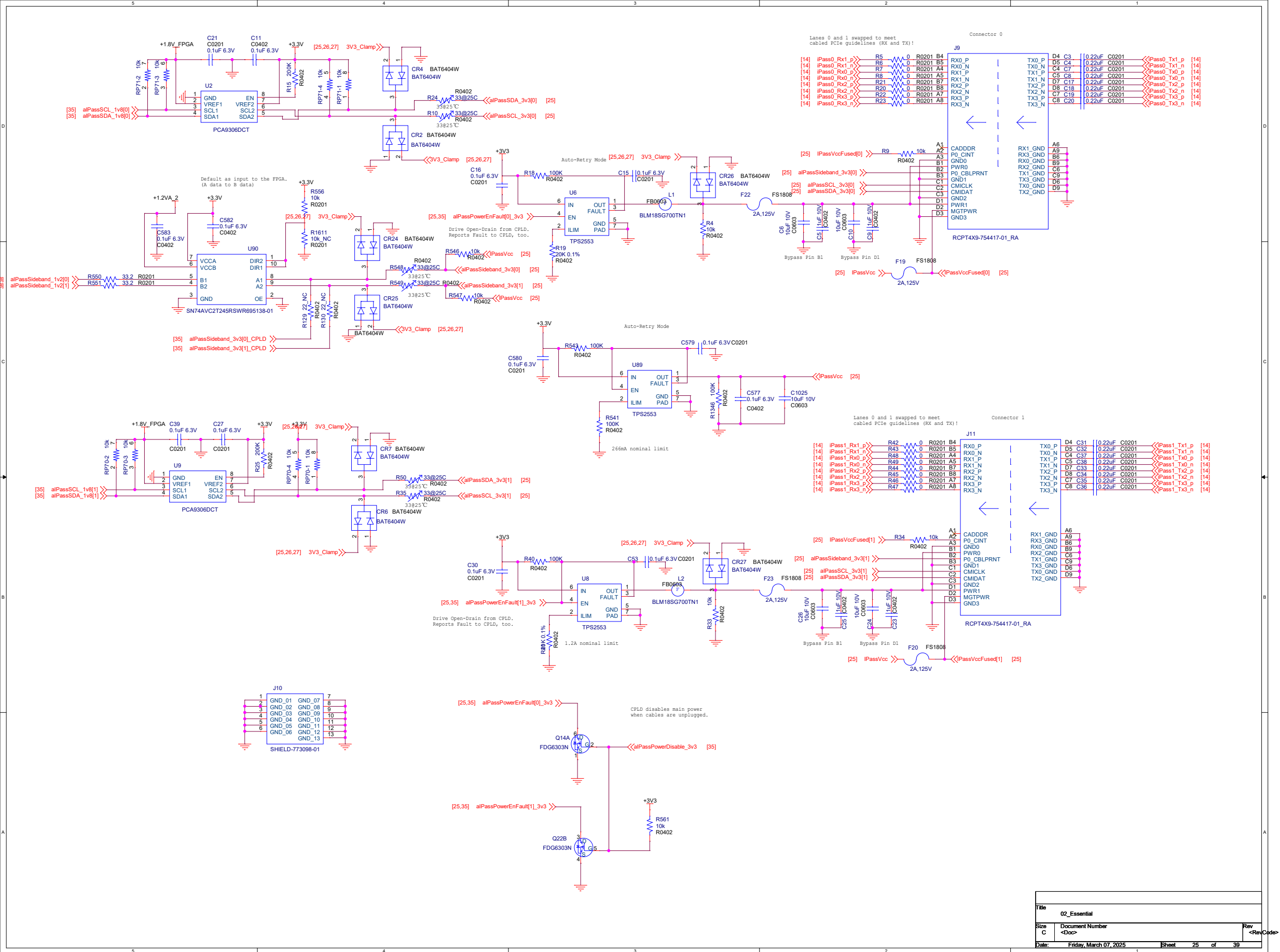


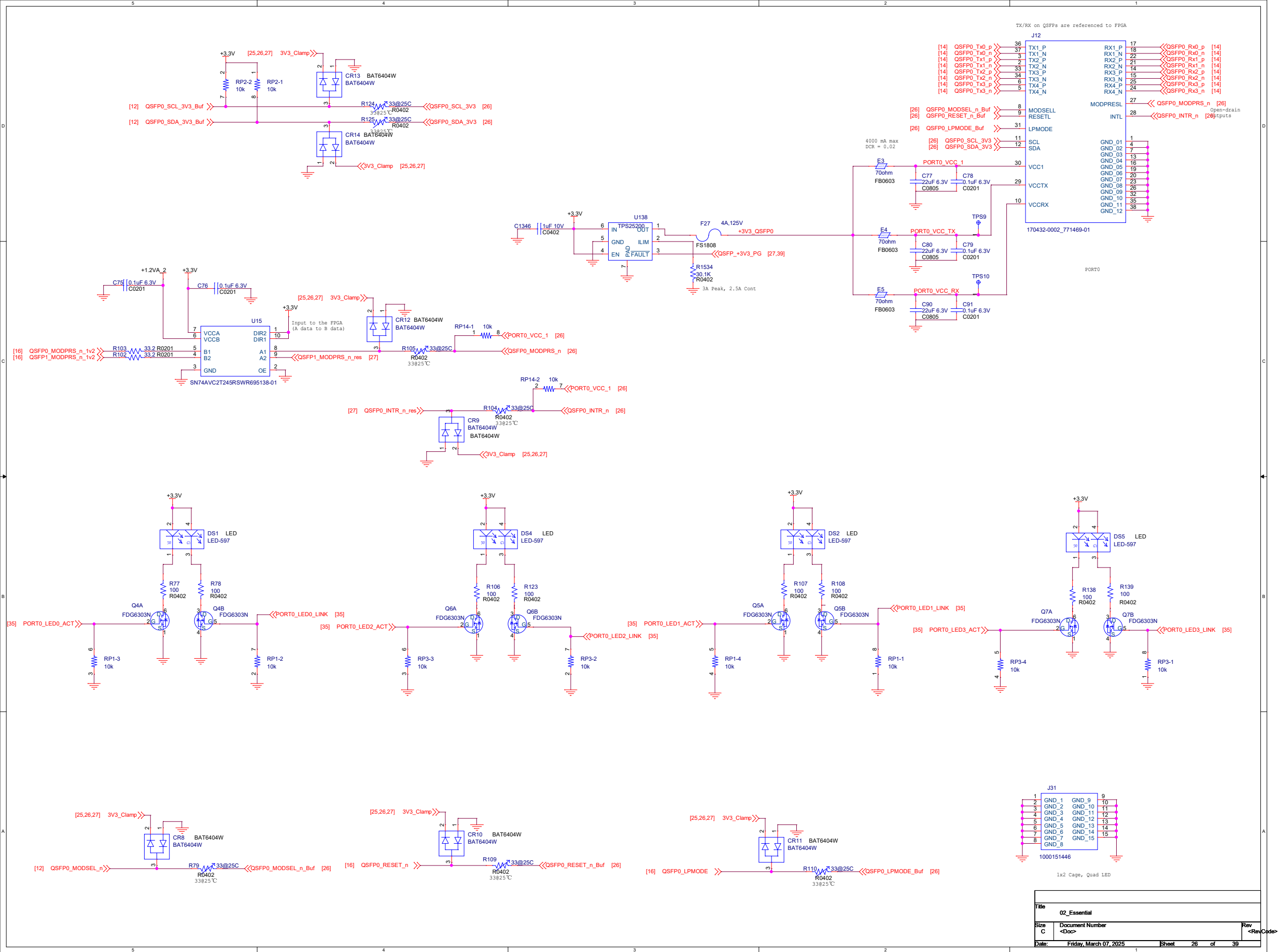


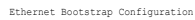
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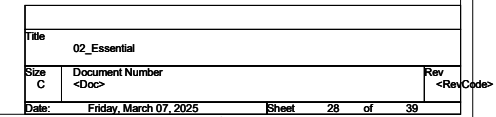


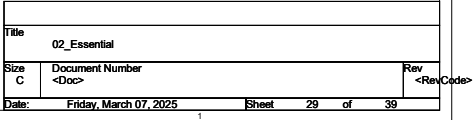
Mode/Clk Bootstraps Mode: 15, clk disabled

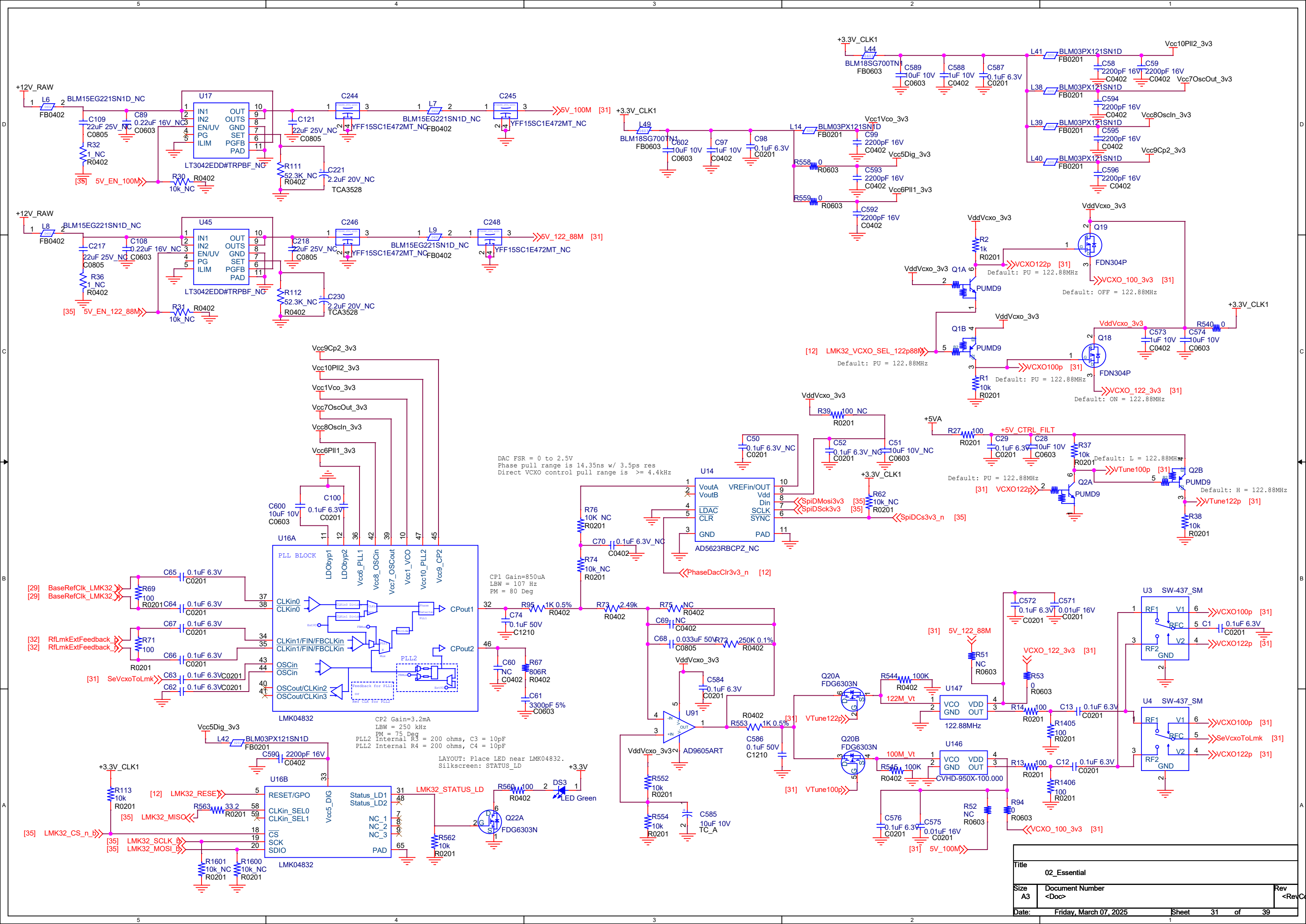
Address bootstraps
Currently configured for 0b111 (Phy address 7)

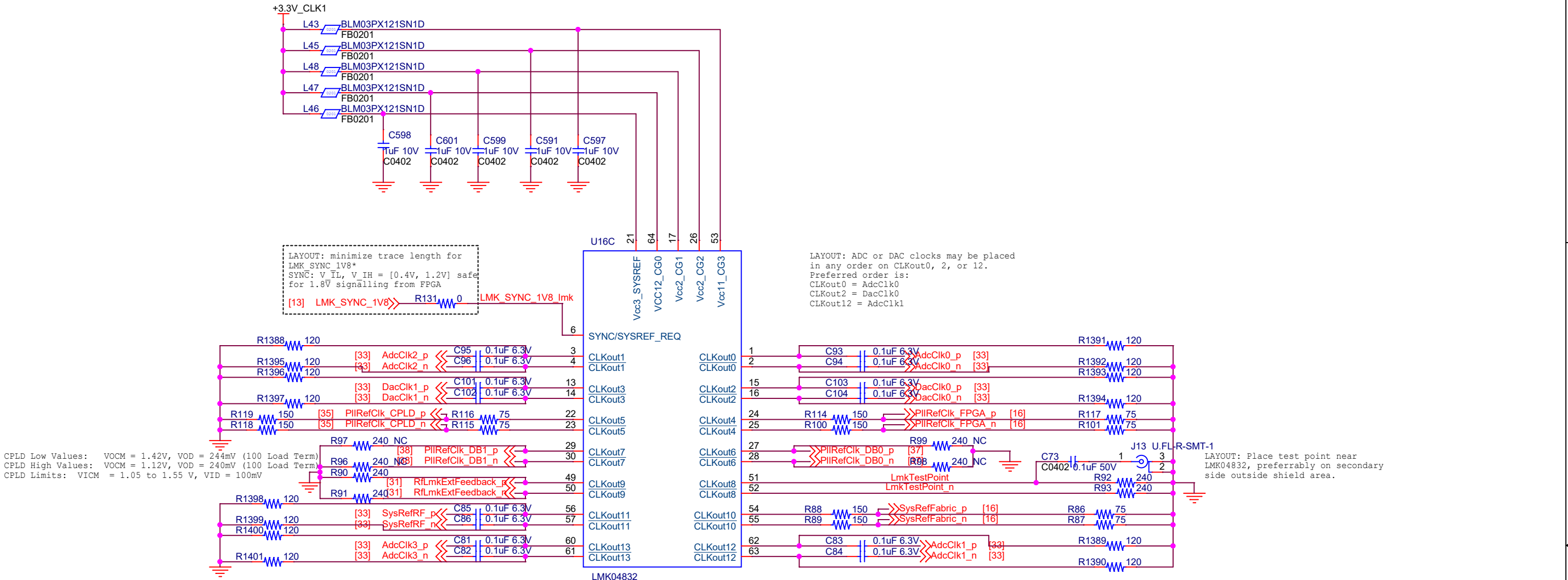


Layout has swapped from VA_2 to VA_1 due to placement

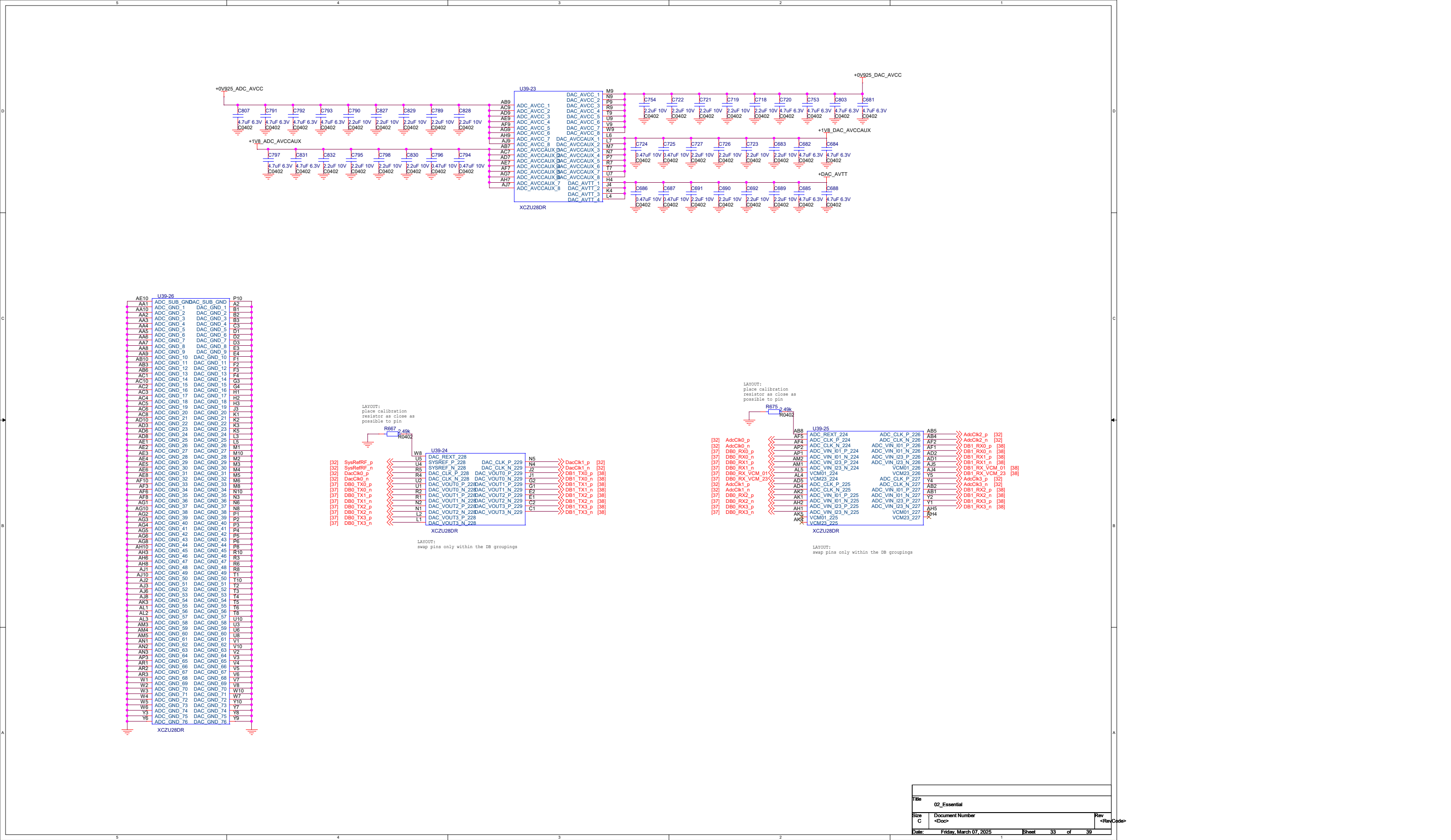


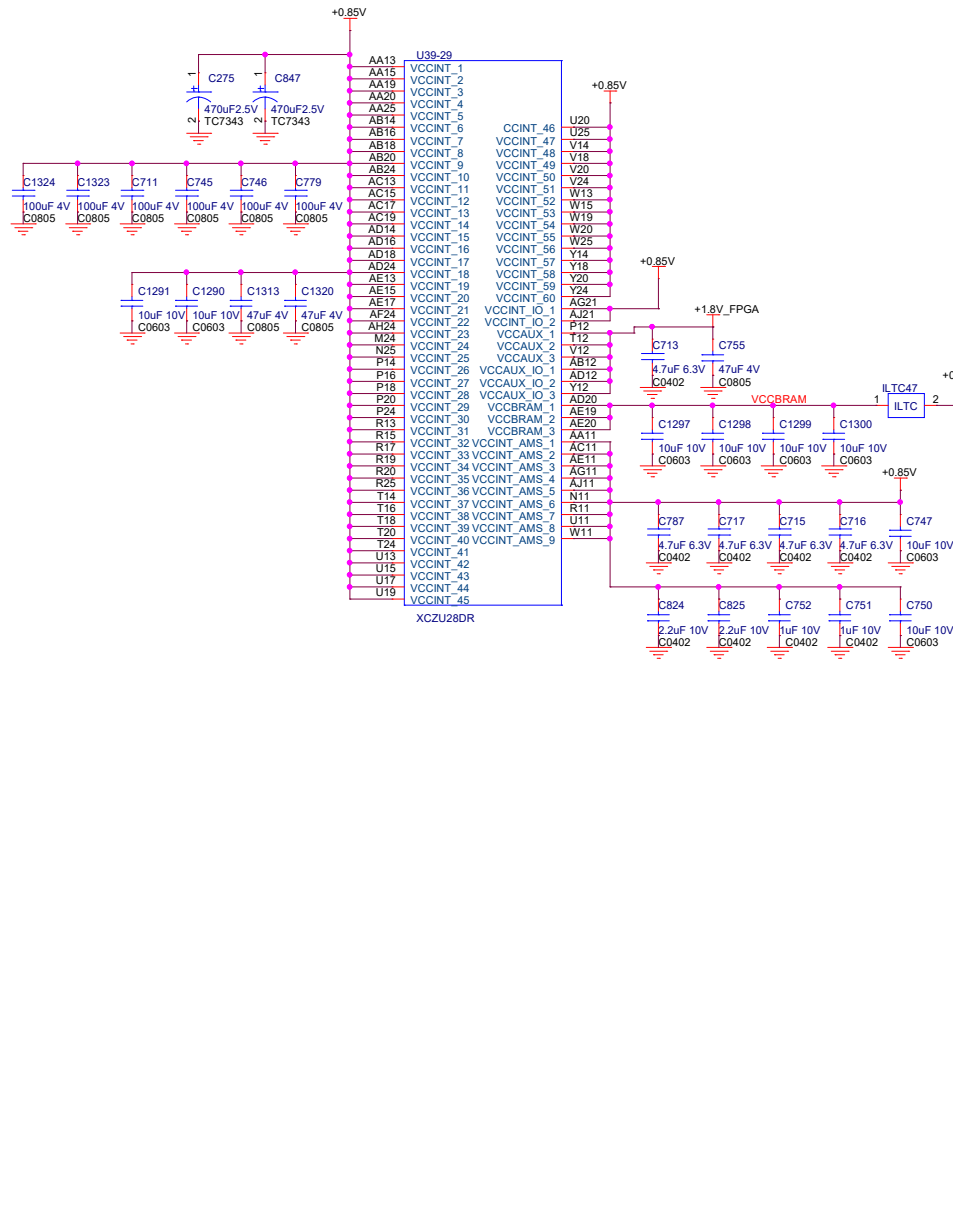
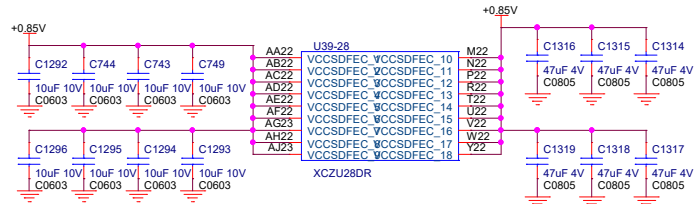




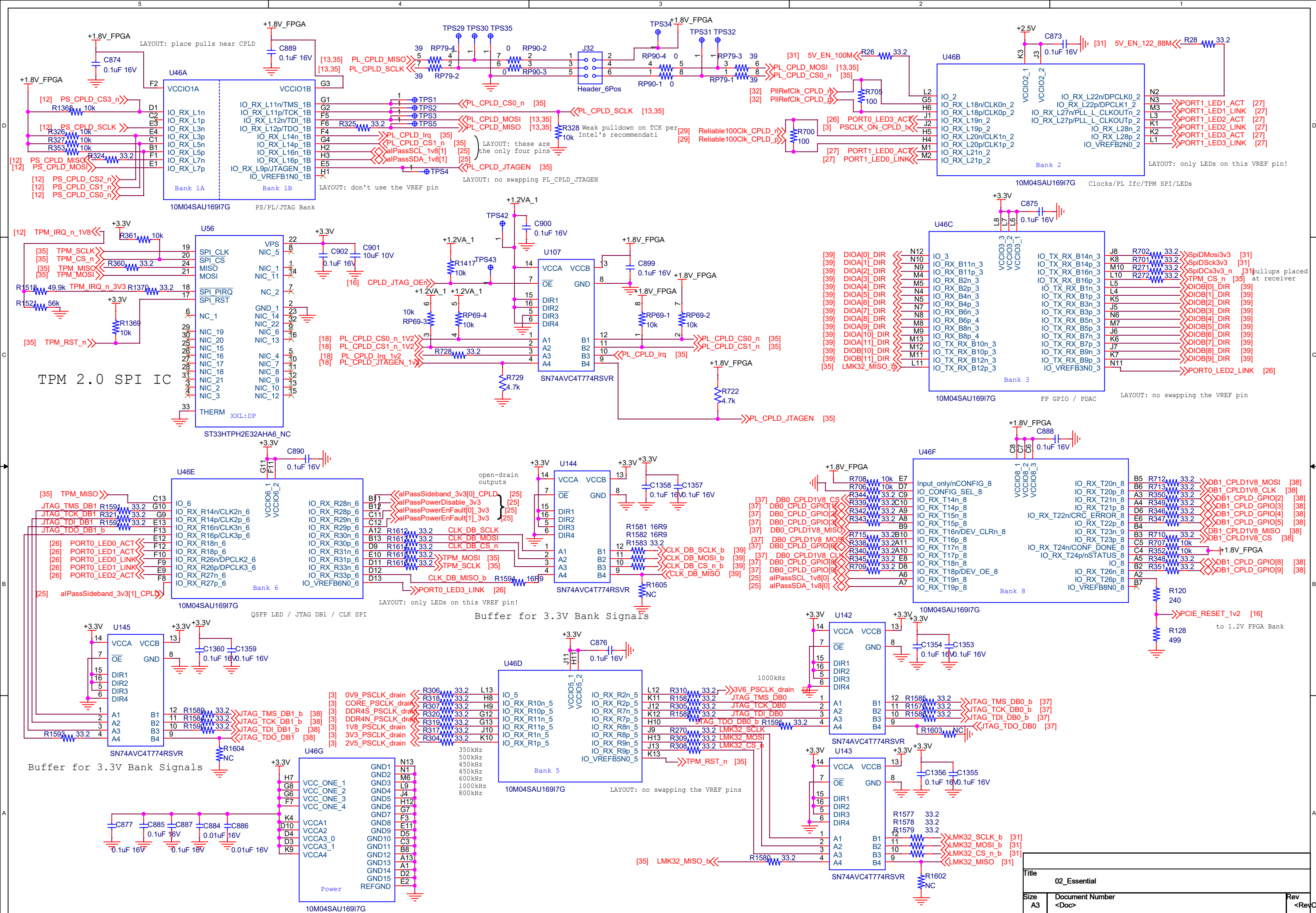


CPLD Low Values: V_{OCM} = 1.42V, V_{OD} = 244mV (100 Load Term)
CPLD High Values: V_{OCM} = 1.12V, V_{OD} = 240mV (100 Load Term)
CPLD Limits: V_{ICM} = 1.05 to 1.55 V, V_{ID} = 100mV

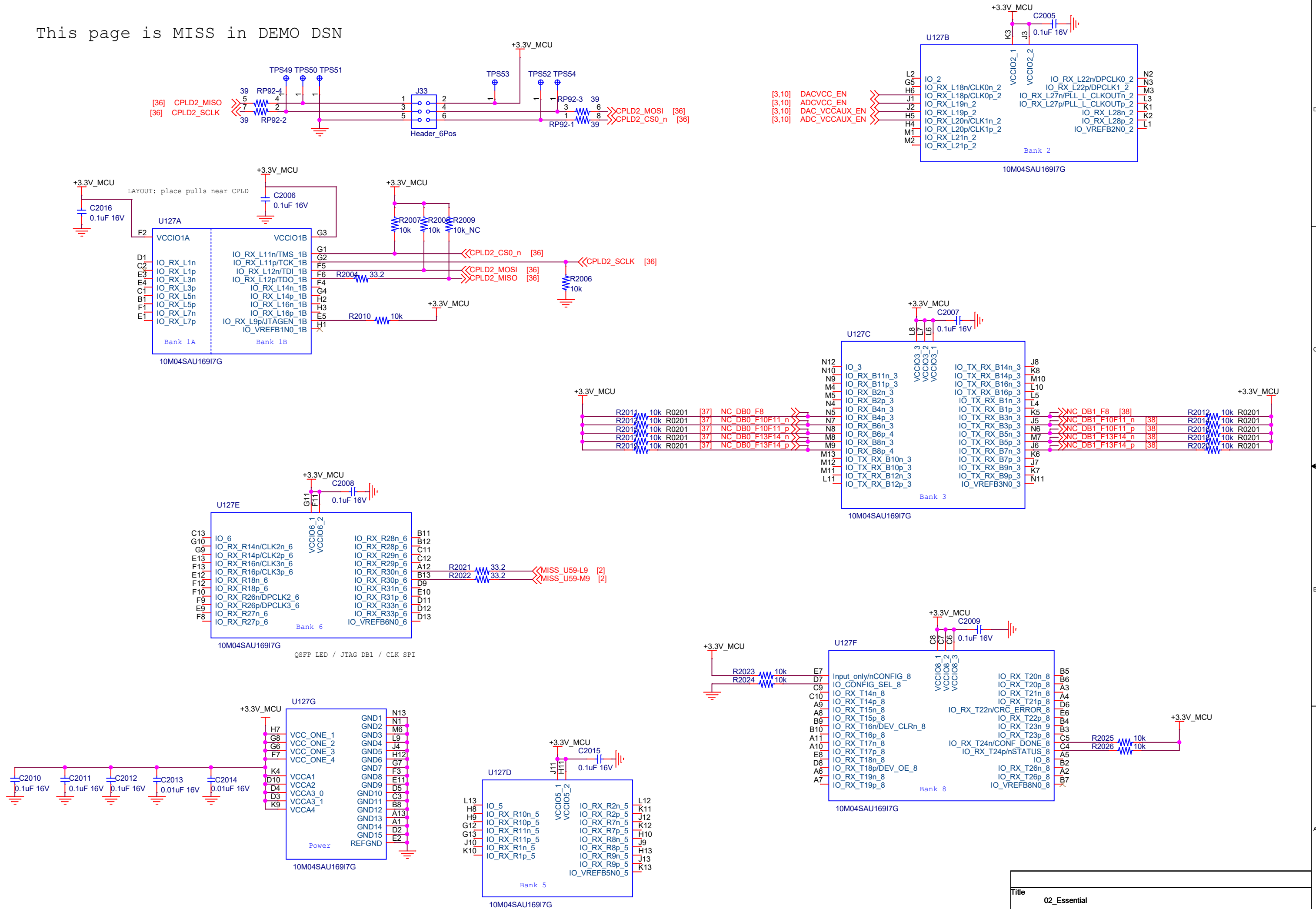




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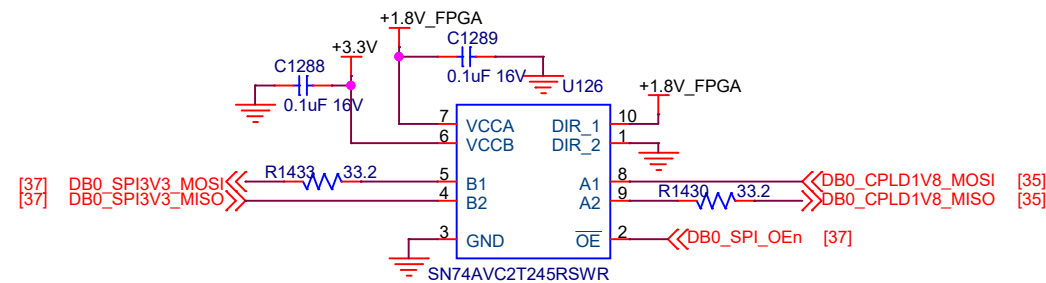
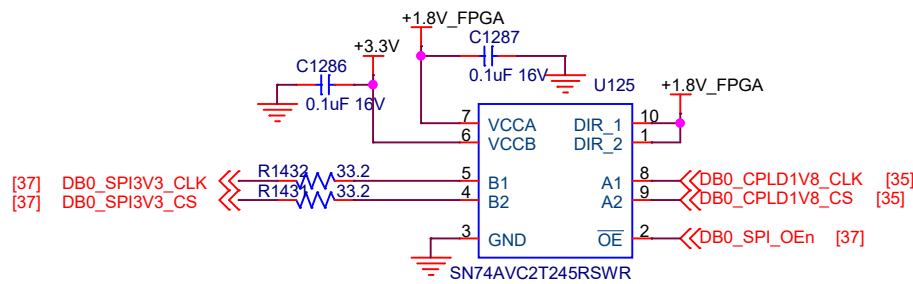
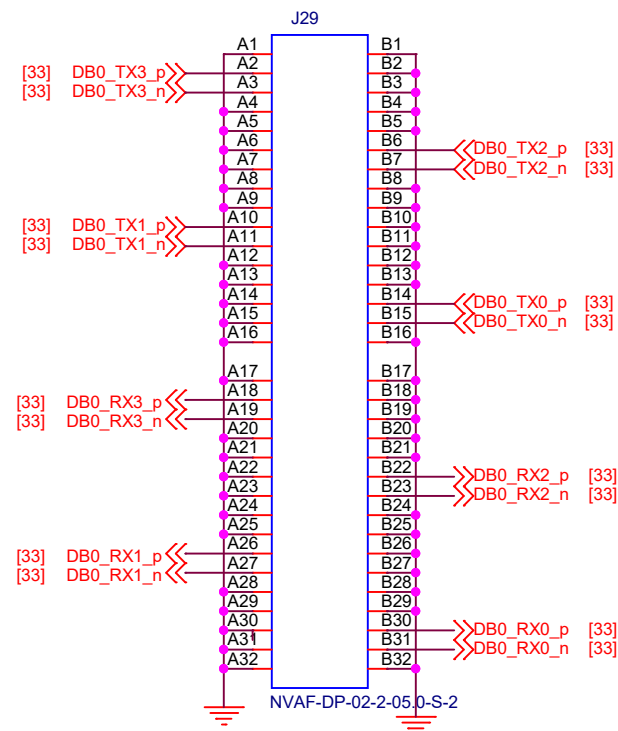


This page is MISS in DEMO DSN

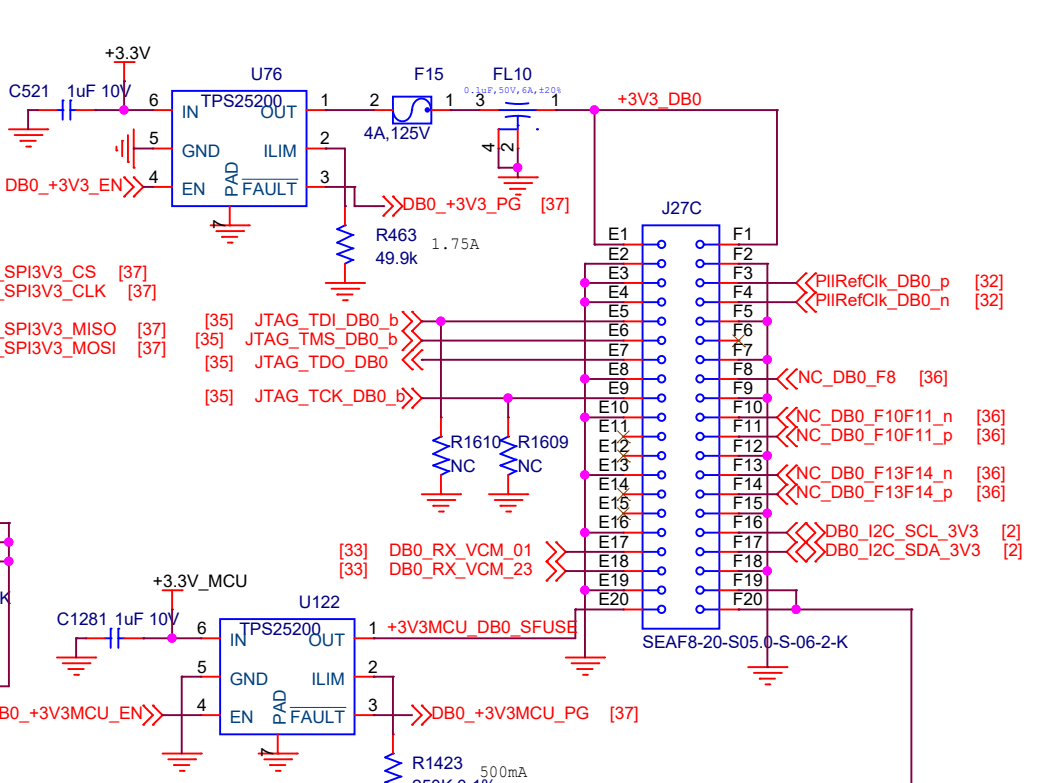
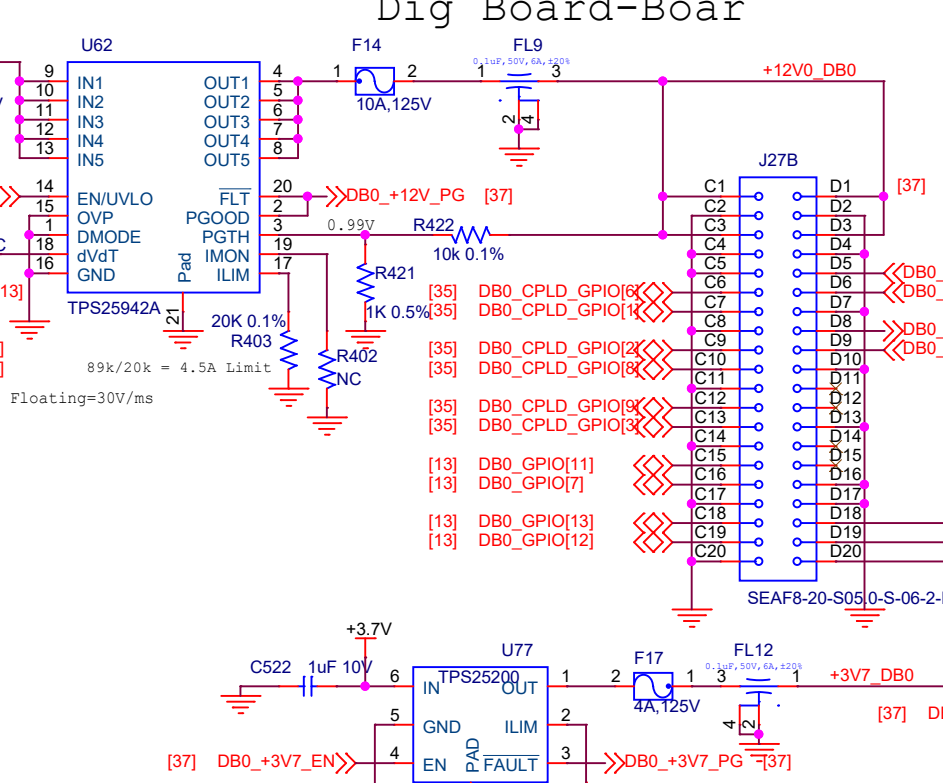
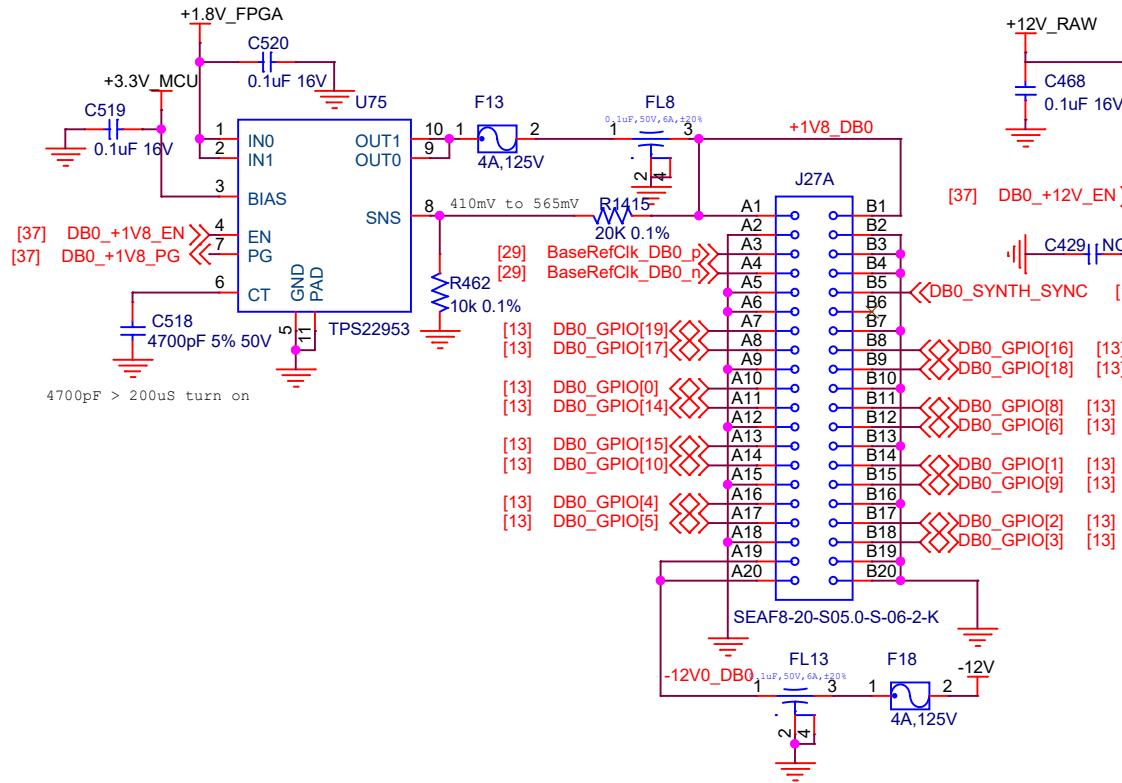


Title 02_Essential			
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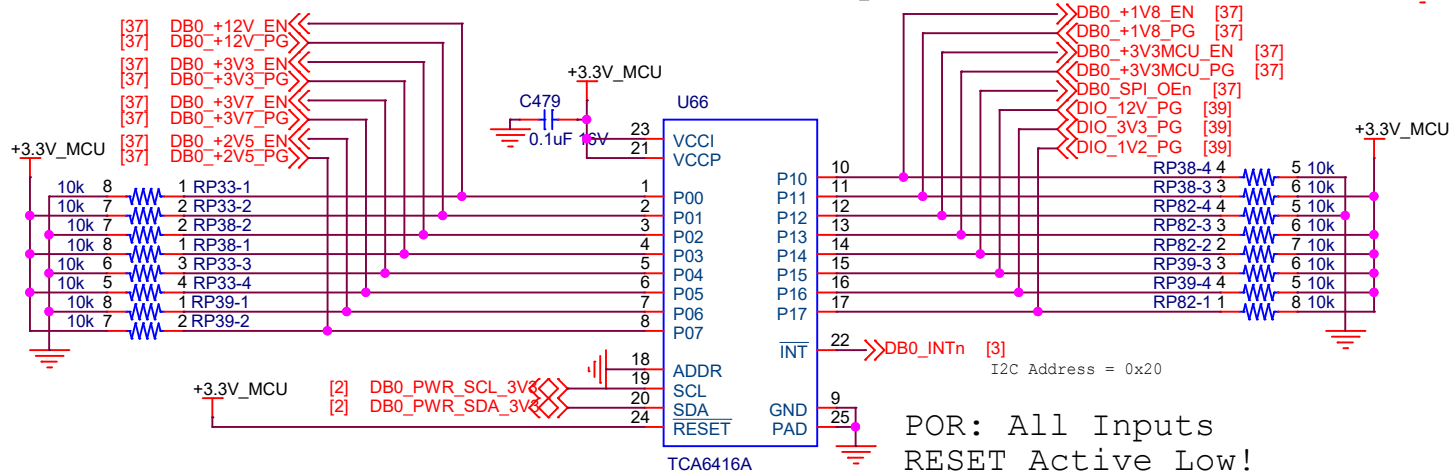
RF Board-Board



Dig Board-Boar



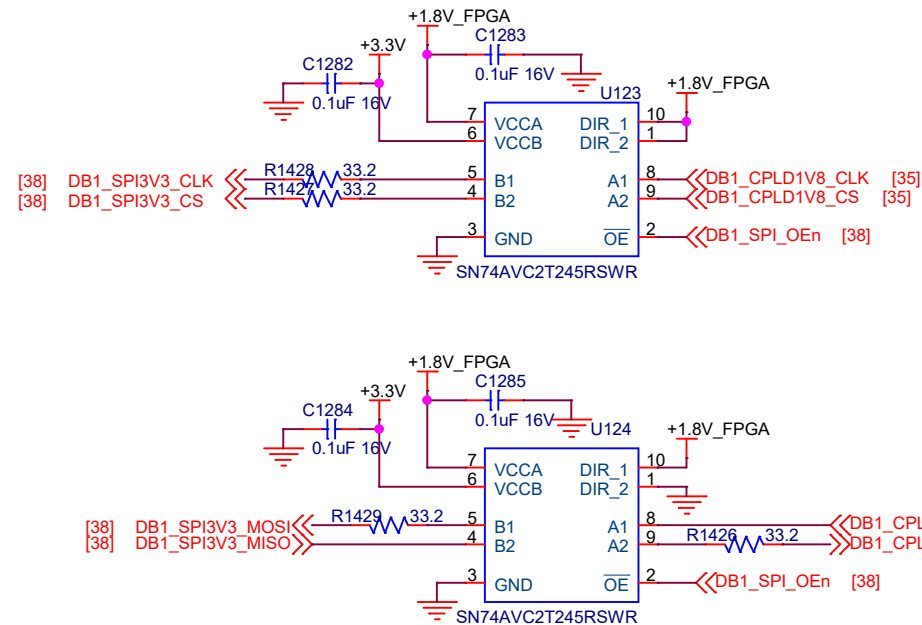
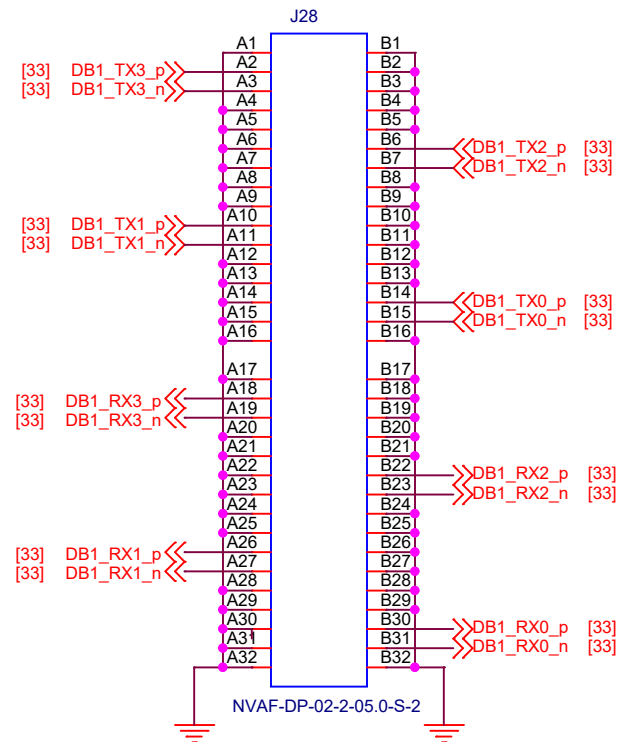
I2C GPIO Expander



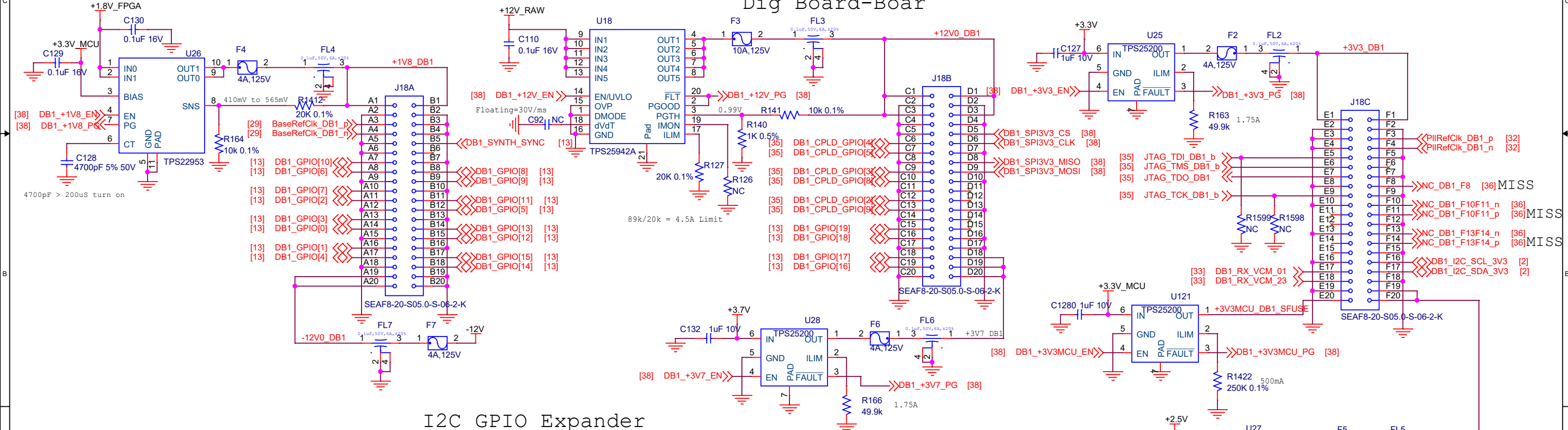
POR: All Inputs
RESET Active Low!

Title		
02_Essential		
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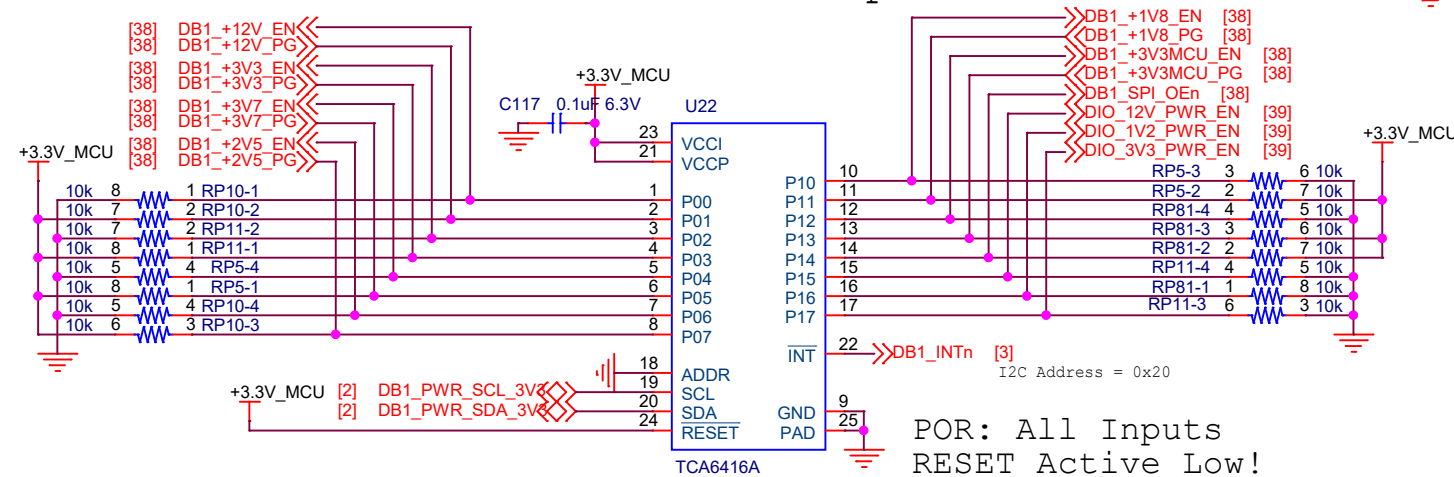
RF Board-Board



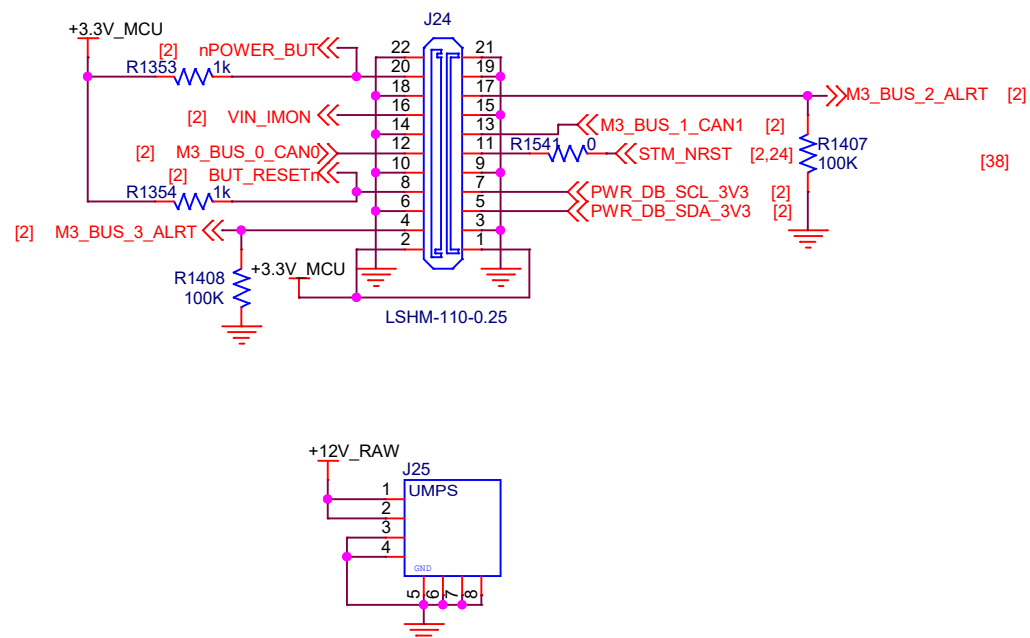
Dig Board-Boar



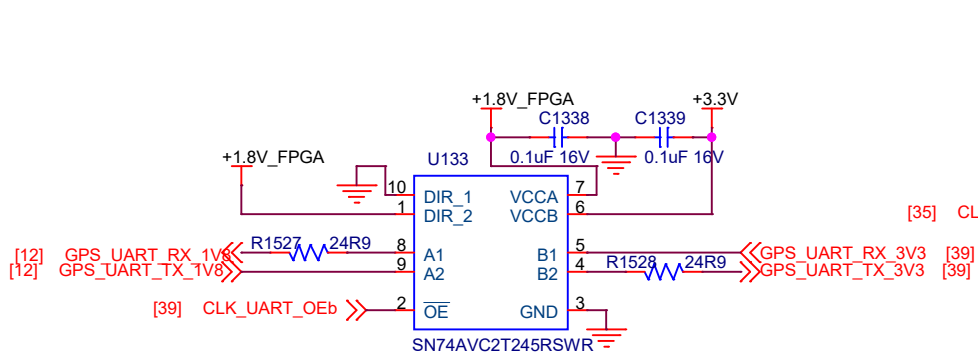
I2C GPIO Expander



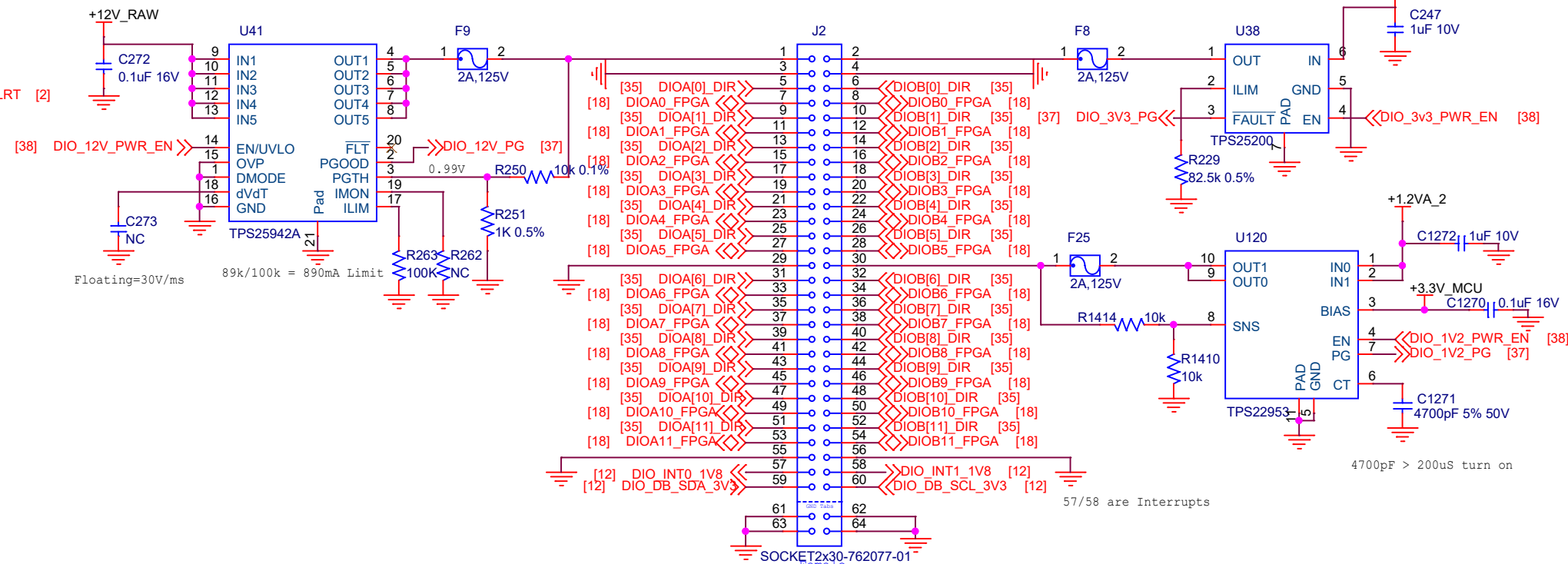
Power Aux Board



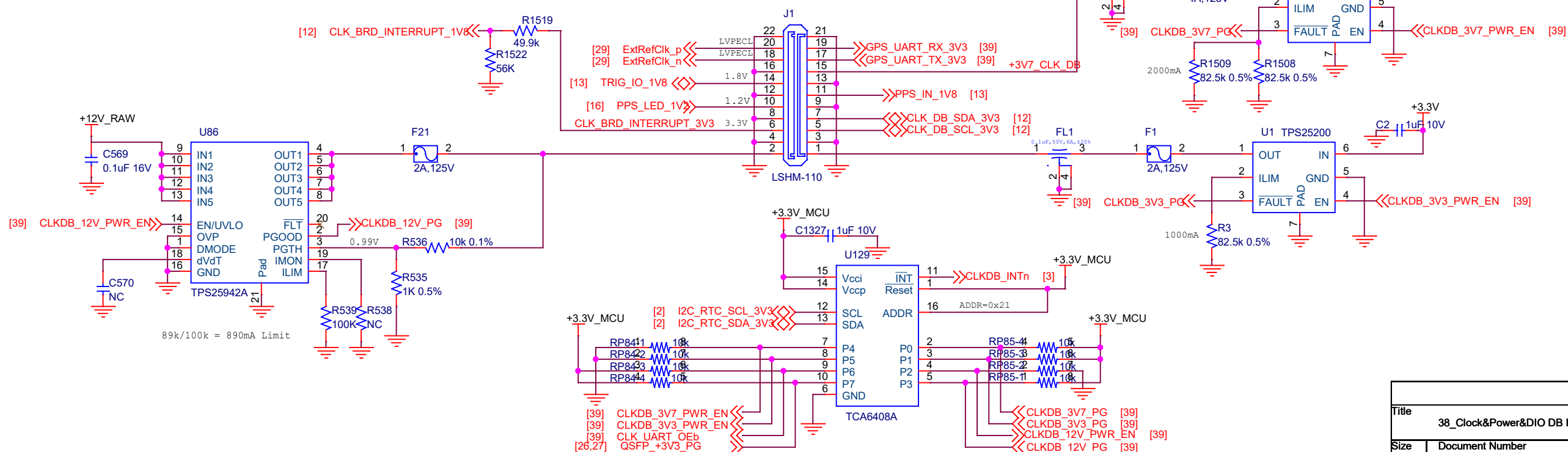
Samtec 20A Power Blade



DIO Aux Board



Clocking Aux Board



Title		
38_Clock&Power&DIO DB Interface		
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