7 Febbraio 2022 – Architetture dei Sistemi di Elaborazione

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Nome, MATRICOLA ....

Considerando il processore MIPS64 e l'architettura descritta in seguito:

- Integer ALU: 1 clock cycle
- Data memory: 1 clock cycle
- FP multiplier unit: pipelined 6 stages
- FP arithmetic unit: pipelined 2 stages
- FP divider unit: not pipelined unit that requires 6 clock cycles
- branch delay slot: 1 clock cycle, and the branch delay slot disabled
- forwarding enabled
- it is possible to complete instruction EXE stage in an out-of-order fashion.

Usando il frammento di codice riportato, si calcoli il tempo di esecuzione dell'intero programma in colpi di clock e si completi la seguente tabella.

```
;     for (i = 0; i < 100; i++) {
;           v5[i] = v1[i]*v2[i];
;           v6[i] = ((v2[i]/v1[i])/(v3[i])*v4[i]);
;}
```

.data																																												Clock cycles
V1: .double “100 values”																																												
V2: .double “100 values”																																												
V3: .double “100 values”																																												
V4: .double “100 values”																																												
V5: .double “100 values”																																												
V6: .double “100 values”																																												
.text																																												
main: daddui r1,r0,0	F	D	E	M	W																																						5
daddui r2,r0,100		F	D	E	M	W																																					1
loop: l.d f1,v1(r1)			F	D	E	M	W																																				1
l.d f2,v2(r1)				F	D	E	M	W																																			1
l.d f3,v3(r1)					F	D	E	M	W																																		1
l.d f4,v4(r1)						F	D	E	M	W																																	1
mul.d f5,f1,f2							F	D	x	x	x	x	x	x	M	W																											6
s.d f5,v5(r1)								F	D	E	s	s	s	s	S	M	W																										1
div.d f5,f2,f1									F	D	d	d	d	d	d	d	M	W																									1
mul.d f6,f3,f4										F	D	x	x	x	x	x	x	M	W																								1
div.d f7,f5,f6											F	D	s	s	s	s	s	d	d	d	d	d	d	M	W																		6
s.d f7,v6(r1)												F	s	s	s	s	s	D	E	s	s	s	s	S	M	W																	1
daddui r1,r1,8																		F	D	s	s	s	s	S	E	M	W																1
daddi r2,r2,-1																			F	s	s	s	s	s	D	E	M	W															1
bnez r2,loop																									F	s	D	E	M	W													2
halt																											F	-	-	-	-													1
Total					6+25*100																																						2506

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Nome, MATRICOLA .....

Domanda 2

Considerando il programma precedente e l'architettura del processore superscalare descritto in seguito; completare la tabella relativa alle prime 2 iterazioni.
Processor architecture:

- Issue 2 instructions per clock cycle
- jump instructions require 1 issue
- handle 2 instructions commit per clock cycle
- timing facts for the following separate functional units:
  i. 1 Memory address 1 clock cycle
  ii. 1 Integer ALU 1 clock cycle
  iii. 1 Jump unit 1 clock cycle
  iv. 1 FP multiplier unit, which is pipelined: 6 stages
  v. 1 FP divider unit, which is not pipelined: 6 clock cycles
  vi. 1 FP Arithmetic unit, which is pipelined: 2 stages
- Branch prediction is always correct
- There are no cache misses
- There are 2 CDB (Common Data Bus).

# iteration		Issue	EXE	MEM	CDB x2	COMMIT x2
1	l.d f1,v1(r1)	1	2m	3	4	5
1	l.d f2,v2(r1)	1	3m	4	5	6
1	l.d f3,v3(r1)	2	4m	5	6	7
1	l.d f4,v4(r1)	2	5m	6	7	8
1	mul.d f5,f1,f2	3	6x		12	13
1	s.d f5,v5(r1)	3	7m			13
1	div.d f5,f2,f1	4	6d		12	14
1	mul.d f6,f3,f4	4	8x		14	15
1	div.d f7,f5,f6	5	19d		25	26
1	s.d f7,v6(r1)	5	8m			26
1	daddui r1,r1,8	6	7i		8	27
1	daddi r2,r2,-1	6	8i		9	27
1	bnez r2,loop	7	10j			28
2	l.d f1,v1(r1)	8	9m		10	28
2	l.d f2,v2(r1)	8	10m		11	29
2	l.d f3,v3(r1)	9	11m		12	29
2	l.d f4,v4(r1)	9	12m		13	30
2	mul.d f5,f1,f2	10	12x		18	30
2	s.d f5,v5(r1)	10	13m			31
2	div.d f5,f2,f1	11	13d		19	31
2	mul.d f6,f3,f4	11	14x		20	32
2	div.d f7,f5,f6	12	25		31	32
2	s.d f7,v6(r1)	12	14m			33
2	daddui r1,r1,8	13	14i		15	33
2	daddi r2,r2,-1	13	15i		16	34
2	bnez r2,loop	14	17j			34