

COMP2300 Set 1 Practice Exam

Topics: Representation, Number Systems, Logic, CMOS Basics

Time: 120 minutes

Total: 100 marks

Instructions

- Answer in English.
- Part A is multiple-choice (concept-focused).
- Part B is computational. Show all working for full credit.
- Assume fixed-width arithmetic where width is explicitly given.

Part A: Multiple Choice (30 marks, 3 marks each)

Choose exactly one option for each question.

A1. In the transformation hierarchy, which is the hardware/software interface?

- (A) Algorithm
- (B) ISA
- (C) Microarchitecture
- (D) Circuits

A2. Which statement about ISA vs. microarchitecture is correct?

- (A) ISA is how transistors are wired.
- (B) Microarchitecture is the programmer-visible instruction definition.
- (C) Different microarchitectures can implement the same ISA.
- (D) ISA changes every time clock frequency changes.

A3. Why is binary preferred in digital systems?

- (A) It always uses less memory than decimal.
- (B) It simplifies hardware and improves reliability.
- (C) It removes the need for abstraction.
- (D) It avoids all overflow.

A4. Which is true for 2's complement representation?

- (A) It has two representations for zero.
- (B) It cannot represent negative numbers.

- (C) Ordinary binary addition can be used.
 - (D) Overflow is detected only by carry-out.
- A5.** For 2's complement addition, overflow occurs when:
- (A) Carry-out from MSB is 1.
 - (B) The addends have different signs.
 - (C) The addends have the same sign and result has opposite sign.
 - (D) Result is zero.
- A6.** Sign extension of an N -bit 2's complement value to M bits ($M > N$):
- (A) Always appends zeros.
 - (B) Always appends ones.
 - (C) Replicates the sign bit into new high bits.
 - (D) Inverts all bits.
- A7.** In CMOS logic, a valid steady state ideally has:
- (A) Pull-up ON and pull-down ON.
 - (B) Pull-up OFF and pull-down OFF.
 - (C) Exactly one of pull-up/pull-down ON.
 - (D) Both ON if output is 1.
- A8.** Which function outputs 1 when inputs are different?
- (A) AND
 - (B) OR
 - (C) XOR
 - (D) XNOR
- A9.** A bit mask is primarily used to:
- (A) Increase clock frequency.
 - (B) Select/clear specific bits.
 - (C) Convert analog to digital.
 - (D) Remove sign extension.
- A10.** A half adder computes:
- (A) Sum of two bits with carry-in.
 - (B) Sum and carry for two input bits (no carry-in).
 - (C) Product and quotient.
 - (D) Bitwise NOR and NAND.

Part B: Computational Problems (70 marks)

B1. Information content and encoding (5 marks)

- (a) How many bits are minimally required to encode 26 symbols?
- (b) How many bits are minimally required to encode 100 symbols?

B2. Base conversion I (6 marks)

Convert decimal 53_{10} to binary using any valid method.

B3. Base conversion II (6 marks)

Convert binary 11010110_2 to decimal.

B4. Binary/hex conversion (6 marks)

- (a) Convert 11110111_2 to hexadecimal.
- (b) Convert $D741_{16}$ to binary.

B5. Representable ranges (6 marks)

For $N = 8$, give the min and max for:

- (a) Unsigned
- (b) Sign/magnitude
- (c) 2's complement

B6. 2's complement encoding/decoding (8 marks)

Using 8 bits:

- (a) Encode -18 in 2's complement.
- (b) Decode 11101011_2 as a signed 2's complement integer.

B7. Unsigned addition and overflow (6 marks)

Add $1111_2 + 1111_2$ as 4-bit unsigned values.

Provide 4-bit result and state whether overflow occurs.

B8. 2's complement addition and overflow (8 marks)

Use 5-bit 2's complement arithmetic.

- (a) $01001_2 + 01011_2$
- (b) $10100_2 + 11010_2$

For each, report binary result, decimal interpretation, and whether overflow occurs.

B9. Sign extension (5 marks)

Sign-extend 1101_2 (4-bit 2's complement) to 8 bits, then give its decimal value.

B10. Bitwise operations (6 marks)

Let $A = 00110110_2$, $B = 00001111_2$. Compute:

- (a) $A \& B$
- (b) $A \mid B$
- (c) $A \oplus B$

B11. Bit mask tasks (6 marks)

Let $X = 10110010_2$.

- (a) Extract the lowest 4 bits of X (show mask and result).
- (b) Clear the lowest 2 bits of X (show mask and result).
- (c) Set the highest 2 bits of X to 1 (show mask and result).

B12. Logic/truth table and useful circuits (8 marks)

- (a) For $Y = (A + B)'$, complete the 2-input truth table (A,B,Y).
- (b) A 2:1 MUX has inputs $I_0 = 1$, $I_1 = 0$, select S . Write Y in terms of S , then evaluate for $S = 0$ and $S = 1$.
- (c) For a half adder with inputs $A = 1$, $B = 1$, compute Sum and Carry.