Jeu d’instructions R12 (version 1.0)

Instruction	Encodage sur 12 bits												Description
	11	10	9	8	7	6	5	4	3	2	1	0	
add	rd		rs1		rs2		0		0				Regs[rd] ← Regs[rs1] + Regs[rs2]
sub							1						Regs[rd] ← Regs[rs1] - Regs[rs2]
mult							2						Regs[rd] ← Regs[rs1] * Regs[rs2]
div							3						Regs[rd] ← Regs[rs1] / Regs[rs2]
mod							0		1				Regs[rd] ← Regs[rs1] % Regs[rs2]
and							1						Regs[rd] ← Regs[rs1] & Regs[rs2]
or							2						Regs[rd] ← Regs[rs1] | Regs[rs2]
xor							3						Regs[rd] ← Regs[rs1] ^ Regs[rs2]
beq							0		2				if (Regs[rs1] == Regs[rs2]) PC ← Regs[rd]
bne							1						if (Regs[rs1] != Regs[rs2]) PC ← Regs[rd]
blt							2						if (Regs[rs1] < Regs[rs2]) PC ← Regs[rd]
ble							3						if (Regs[rs1] <= Regs[rs2]) PC ← Regs[rd]
addi			rs		imm				3				Regs[rd] ← Regs[rs] + imm
subi									4				Regs[rd] ← Regs[rs] - imm
multi									5				Regs[rd] ← Regs[rs] * imm
divi									6				Regs[rd] ← Regs[rs] / imm
modi									7				Regs[rd] ← Regs[rs] % imm
shli									8				Regs[rd] ← Regs[rs] << imm
shri									9				Regs[rd] ← Regs[rs] >> imm
ld									10				Regs[rd] ← Mem[Regs[rs] + imm]
sd									11				Mem[Regs[rd] + imm] ← Regs[rs]
jalr									12				Regs[rd] ← PC + 1, PC ← Regs[rs] + imm
jal			imm (signé)						13				Regs[rd] ← PC + 1, PC ← PC + 1 + imm
bz									14				if (Regs[rd] == 0) PC ← PC + 1 + imm
bnz									15				if (Regs[rd] != 0) PC ← PC + 1 + imm