Monophono v2.5 board testing

note: EVERY test must successfully pass in order to proceed to the next one.

Continuity

- ☐ All p2p
- ☐ Isolation of traces

Power

- ☐ VCC = 5 VDC
- ☐ IC power
  - ☐ IC1 5V
  - ☐ IC2 5V
  - ☐ IC5 5V
  - ☐ IC6 VRAW (12V)
- ☐ Negative voltage generator
  - ☐ VOLTAGE = 5V
  - ☐ RIPPLE < 200mV
- ☐ DAC: PIN#5 @ JP4: V= 5V

Digital

- ☐ Multiplexer address test
  - ☐ IC1
  - ☐ IC2 *MUST PULL-DOWN PIN#6
- ☐ IC5 clock divider test: inject clock signal [16Hz Vp =5v] in PIN#1@JP3
  read @JP5:
  - ☐ PIN#2: 16 Hz
  - ☐ PIN#3: 8 Hz
  - ☐ PIN#4: 4 Hz
  - ☐ PIN#5: 2 Hz
  - ☐ PIN#6: 1 Hz

Analog

- ☐ CV bend circuit:
  - ☐ Bend Offset:
    - ☐ Force PIN2@JP7 to GND
    - ☐ Measure “Bend” voltage: adjust TM1 until v = 0V
    - ☐ Force PIN2@JP7 to +1V
    - ☐ Measure “Bend” voltage: adjust TM1 until v = 0V
    - ☐ Connect Bend Wheel and set it to the center
    - ☐ Measure “Bend” voltage: adjust TM1 until v = 0V
  - ☐ Bend Gain:
    - ☐ Force PIN2@JP7 to 1V
    - ☐ Measure “Bend” voltage: adjust TM2 until v = 1V
    - ☐ Set Bend Whee all the way up
    - ☐ Measure “Bend” voltage: adjust TM2 until v = 0,167V
- ☐ Bend circuit:
  - ☐ Force PIN2@JP9 to 1V
  - ☐ Measure “Exp_out” voltage: adjust TM3 until v = 2V

Software

- ☐ **HW**
  - ☐ Check DAC I2C address
  - ☐ Set DAC Vout = 2.5V and Force PIN2@JP7 TO GND:
    - ☐ “CV” voltage = 2.5v
    - ☐ “CV_bend” voltage = 3.5v
  - ☐ Software controlled IC2: read ~5V @selected address output
  - ☐ Software controlled IC1: read ‘HIGH’ @D6 when address matches Pulled-UP input
- ☐ **Keyboard**
  - ☐ Scan keyboard
  - ☐ Control DAC via MONO algorithm
  - ☐ Control GATE
- ☐ **Clock**
  - ☐ ‘CK_RATE’ input read
  - ☐ ‘CK_O’ control
  - ☐ ‘CK_I’ input read
- ☐ **Arpeggiator**
  - ☐ ‘OCT_SEL’ , ‘ARP_ENABLE’ and ‘ARP_MODE’ input read
  - ☐ Arpeggiator implementation
  - ☐ MIDI implementation