Getting Started with System Generator for DSP

Lab 5 – Multi-Rate Systems

XILINX®

Multi-Rate Systems

Introduction

In this lab you will explore the effects of the rate changing blocks available in System Generator including the **Up Sample**, **Down Sample**, **Serial to Parallel** and **Parallel to Serial** blocks. **Upsampling** is the process of increasing the sampling rate of a signal and **Downsampling** is the process of decreasing the sampling rate of a signal. It is common practice in signal processing systems to change the sample rate of a signal to simplify the hardware or processing tasks.

Note: The complete solution to this lab is in the following location:
…sysgen/examples/getting_started_training/lab5/solution

Objectives

After completing this lab, you will be able to:

- Change the sample rates in a DSP System
- Convert a serial stream of data to a parallel word
- Convert a parallel word of data into a serial stream

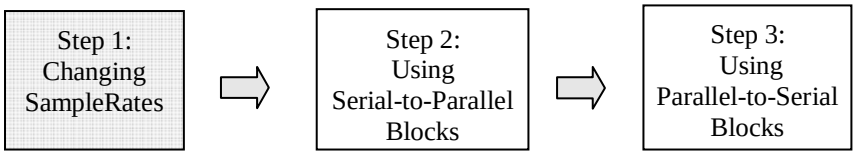
Lab Setup

Please check the System Generator for DSP release notes to insure that the proper versions of ISE Design Suite and MATLAB are installed on your machine. Failure to have the proper tool versions installed may result in unexpected behavior.

Procedure

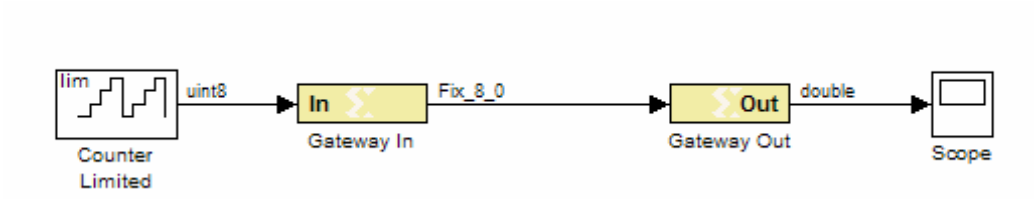
Changing Sample Rates — Step 1

General Flow for this Lab:

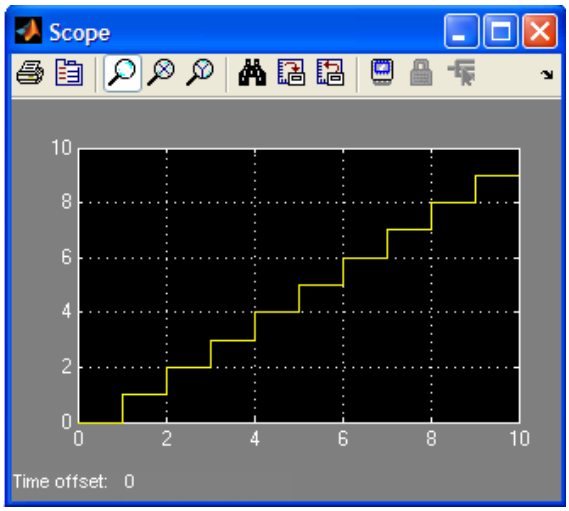


❶ Launch the MATLAB program and change the working directory to:
…sysgen/examples/getting_started_training/lab5

❷ Open a new Simulink diagram and create the simple diagram shown below. Use the **Counter Limited** block from the Simulink/Sources library and set the upper limit of the counter to **10**. Set the quantization of the **Gateway In** block to **fix [8 0]**.

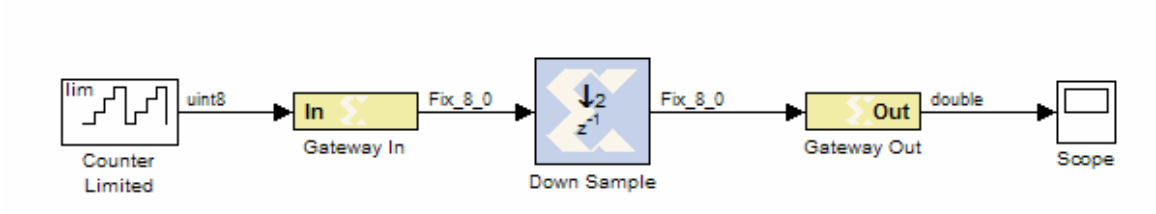


❸ Simulate the counter for 10 simulation cycles and observe the results.



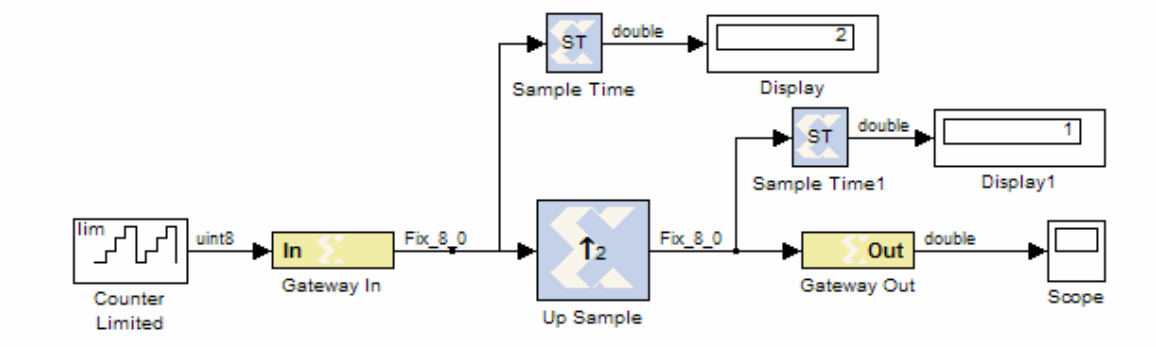
❹ As shown below, add a **Down Sample** block from the Xilinx Blockset/Index library between the **Gateway In** and **Gateway Out** blocks, then re-simulate the design. What do you observe?

_____



❺ Replace the **Down Sample** block with an **Up Sample** block and re-simulate the design. The **System Generator** token is going to generate an error that indicates your sample rate is incorrect.

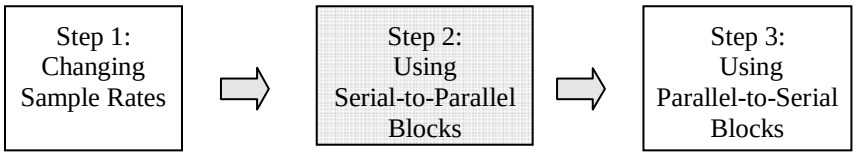
❻ Double-click on the **System Generator** token and change the **Simulink System Period** to ½ as the message suggests. Re-simulate the design. Add **Sample Time** probes from the Xilinx Blockset/Index library before and after the **Up Sample** block and connect the outputs of the probes to the Simulink/Sinks as shown in the figure below. These probes don't add any hardware to the design, but offer a powerful debugging tool for complex multi-rate systems Re-simulate the design to observe the sample rate in the **Display** sinks.



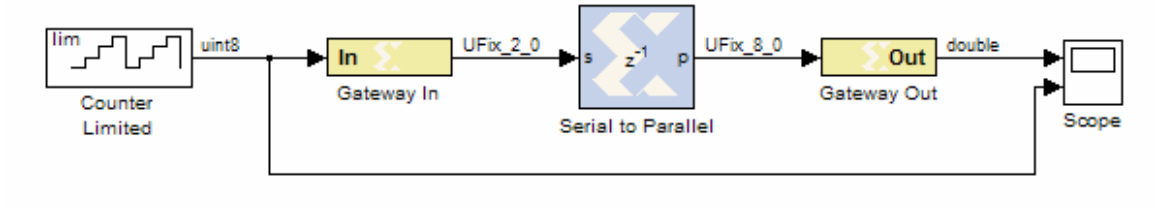
In the next two steps, you will explore the rate changing effects of using the **Serial to Parallel** and **Parallel to Serial** blocks from the Xilinx Blockset.

Using Serial-to-Parallel Blocks — Step 2

General Flow for this Lab:

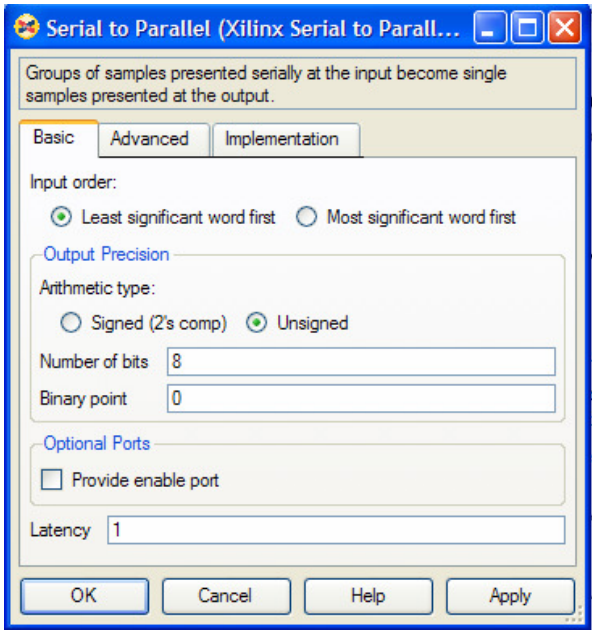


❶ Open a new blank model, and then create the design shown below.



❷ Set the limit on the **Counter Limited** block to **1**. This is simply going to generate the sequence **1010101010**.

❸ Set the output of the **Serial to Parallel** block to **Unsigned [8 0]**.



The **Serial to Parallel** block will impose a rate change on the system equal to the number of output bits / number of input bits. In this example, you have 8 output bits and 2 input bits so the rate change will be set to 4.

❹ Click **OK** on the Properties Editor form, than add sample rate probes to the input and output of the **Serial to Parallel** block. Re-simulate the design and observe the sample rates.

Input Sample Rate _____

Output Sample Rate _____

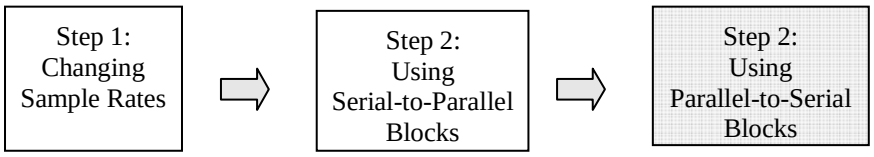
❺ Change the output quantization of the **Serial to Parallel** block to **fix [16 0]** and re-simulate. What are the sample rates now?

Input Sample Rate _____

Output Sample Rate _____

Using Parallel-to-Serial Blocks Step 3

General Flow for this Lab:



❶ Replace the **Serial to Parallel** block with the **Parallel to Serial** block. Leave the output quantization at the default **ufix [1 0]**.

❷ Change the sample rate in the **System Generator** token from **1** to ½, then click **OK**.

❸ Re-simulate the design and record the input and output sample rates.

Input Sample Rate _____

Output Sample Rate _____

Note: You may get an error with the Sample Time (ST) probe connected to the output. If this occurs, just temporarily connect the probe to the input signal, perform the simulation once, then reconnect the probe to the output signal again and re-simulate.

Solution

The complete solution to this lab is in the following location:

…sysgen/examples/getting_started_training/lab5/solution