Getting Started with System Generator for DSP

Lab 3 - Signal Routing

XILINX®

Signal Routing

Introduction

This lab introduces you to the System Generator features that you will use to convert fixed-point numbers from floating-point, re-define the fixed-point format, as well as perform bit slice, pad and unpad operations. You will also design and verify the padding and unpadding logic using the System Generator signal routing blocks.

Objectives

After completing this lab, you will be able to:

- Understand how signal routing blocks can be used redefine or modify a fixed-point number at the bit level
- Convert a fixed-point number into a new fixed-point number
- Slice bits from a fixed-point number
- Pad and Unpad a fixed-point number

Lab Setup

Please check the System Generator for DSP release notes to insure that the proper versions of ISE Design Suite and MATLAB are installed on your machine. Failure to have the proper tool versions installed may result in unexpected behavior.

Procedure

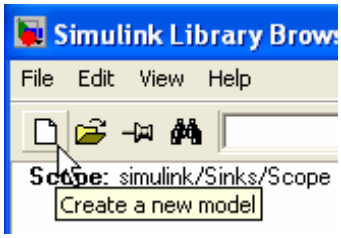
Designing Padding Logic — Step 1

General Flow for this Lab:

❶ Launch the MATLAB program and change the working directory to:
…sysgen/examples/getting_started_training/lab3

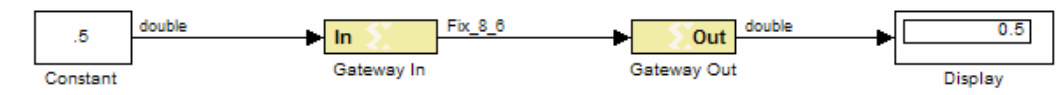
❷ Launch the Simulink library browser by clicking on the Simulink icon on the MATLAB toolbar

❸ As shown below, click the N**ew model** button in the Simulink Library Browser to create a new model blank sheet

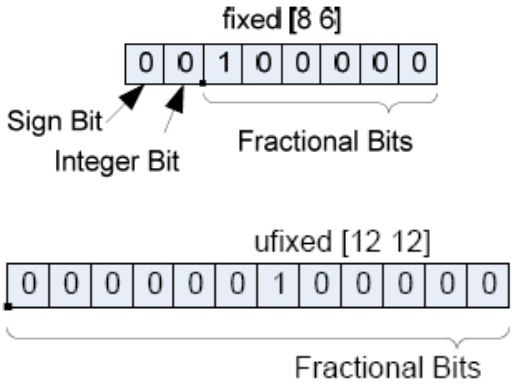


❹ Create the design shown below. Use a **Constant** block from the Simulink "sources" blockset and a **Display** block from the Simulink "sinks" blockset. Set the value of the constant to **.5**. Add a Xilinx **Gateway In** block quantized to **fixed_8_6** (Signed 2's comp). Remember that a **System Generator** token is also be required in this diagram.

To display the signal type **Fix_8_6** as shown below, select the work sheet menu item **Format → Port/Signal Displays → Port Data Types**, and then run a simulation.



The objective of this lab is to convert the binary representation of the number **.5** when quantized to **fixed [8 6]** to the number **.007813** when quantized to **ufixed [12 12**]

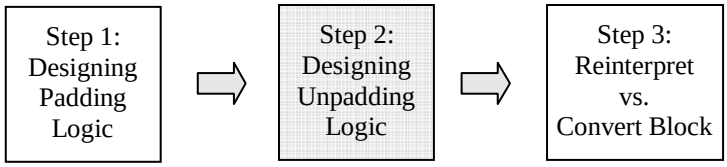


To accomplish this you are going to have to zero pad the MSBs and reinterpret the number. This will require the use of the **Concat** and **Reinterpret** blocks. Review the Help text for these blocks to gain a greater understanding of how they work.

❺ Modify the block diagram previously shown to convert the input constant value of **.5** to an output value of **.007813**. You will first need to use the **Reinterpret** block to convert the number to **ufix [8 0]**. You then use a **Constant** and **Concat** block to convert to **ufix [12 0]**, and then use another **Reinterpret** block to convert **ufix [12 12]**.

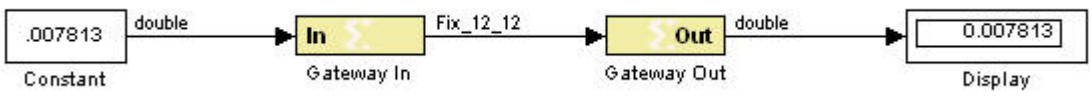
Designing Unpadding Logic — Step 2

General Flow for this Lab:



❶ You are going to perform an exercise similar to Step 1, but in the other direction. Here the input will be the constant **.007813** and you want the output to be converted to **.5** through bit manipulation, not arithmetic.

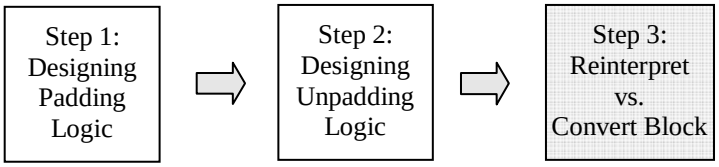
❷ Create the design shown in below. The input constant should be set to **.007813** and the input gateway can be set to **fix [12 12]**. Remember to include the **System Generator** token in the diagram.



Use the **Slice** and **Reinterpret** blocks to manipulate the binary number to achieve an output of **.5**. First, you need to use the **Slice** block to convert the number to **ufix [8 0]**, then use the **Reinterpret** block to get **fix [8 6]**. Refer to the binary diagrams in Step 1 of this lab.

Reinterpret vs. Convert Block — Step 3

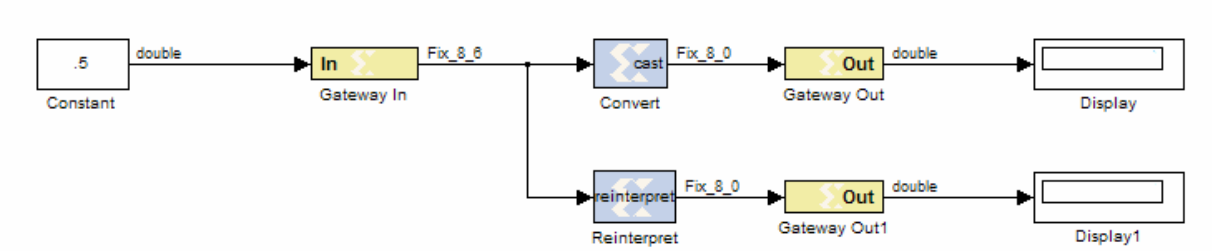
General Flow for this Lab:



In this step you will explore the differences in the effects of using the **Reinterpret** block vs. the **Convert** block

❶ Open a new Simulink design sheet by clicking on the **Create new Model** icon from the Simulink Library toolbar

❷ Create the design shown below. Set the input constant to .5, set the parameters of both the **Convert** and **Reinterpret** blocks as shown in the diagram below.



❸ Simulate the design. What are the values of **Display** and **Display1**. Why?

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Solution

The complete solution to this lab is in the following location:

…/sysgen/examples/getting_started_training/lab3/solution